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School of
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Minor Project II Report

on

Design and Implementation of 8 bit Current Steering DAC using 180nm Technology

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Semester: VI, 2023-2024

Under the Guidance of

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K.L.E SOCIETY'S
KLE Technological University.
HUBBALLI-580031
2023-2024

SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that project entitled " **Design and Implementation of 8 bit Current Steering DAC using 180nm Technology** " is a bonafide work carried out by the student team of "**Yatirajgouda Patil - 01FE21BEC083, Pratham Naik - 01FE21BEC103, Prateek Shettar - 01FE21BEC081, Sarpabhushan Angadi - 01FE21BEC069** ". The project report has been approved as it satisfies the requirements with respect to the mini project work prescribed by the university curriculum for BE (V Semester) in School of Electronics and Communication Engineering of KLE Technological University for the academic year 2023-2024.

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ACKNOWLEDGMENT

We extend our heartfelt gratitude to the KLE Technological University, Hubballi, for providing us with the resources and infrastructure necessary to successfully complete our project, "Design and Implementation of 8 bit Current Steering DAC using 180n Technology " We are deeply indebted to our esteemed guide, Dr. Sujata Kotabagi, for entrusting us with this challenging and enriching project. Her invaluable guidance, expert insights, and unwavering support throughout the journey helped us achieve remarkable results. We also express our sincere appreciation to Dr. Suneeta V Budihal, Dean of the School of Electronics and Communication, for providing crucial direction and steering us towards an industrial-scale perspective. A special thanks goes to the Prakalp team for their valuable recommendations and timely assistance, which significantly enhanced our project. We are forever grateful to our guardians for their unwavering support and encouragement. Their faith in our abilities provided us with the strength and motivation to persevere through challenges and ultimately achieve success. Finally, we acknowledge and cherish the contributions of everyone who, directly or indirectly, supported us and contributed to the joy of completing this project.

- Yatirajgouda, Pratham, Prateek, Sarpabhushan

ABSTRACT

The design and simulation of a current-steering digital-to-analog converter (DAC) using a segmented architecture and a specially created current source array are shown in this report. The suggested DAC takes advantage of the benefits of current steering, including high-speed operation and lower complexity, by using current-steering techniques rather than conventional DAC architecture . In a 180nm technology node, Cadence Virtuoso is used to implement the DAC architecture. The developed current-steering DAC's performance and usefulness are demonstrated by the simulation results. The DAC matches the project's standards thanks to its favorable features, which include excellent linearity, minimal harmonic distortion, and precise output current matching.When current-steering techniques are applied instead of resistor ladder-based solutions, the DAC performs better, offering better dynamic range and signal-to-noise ratio. The segmented architecture additionally enables scalability resolution and reduced power consumption, making it suitable for various applications requiring high-speed and high-precision analog signal generation.

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Chapter 1

Introduction

Digital-to-analog converters, or DACs, are crucial parts of contemporary electronic systems because they provide as a link between analog and digital signal processing. With the ongoing advancements in digital technology, there is an ever-growing need for high-performance digital audio converters. DACs are used in different domains, such as instrumentation, control systems, communication networks, audio and video processing.

The present steering DAC stands out among other DAC architectures because of its superior linearity and high-speed performance. Applications in need of high-resolution output and quick signal translation frequently adopt this design.The 8-bit resolution option offers a workable compromise between the degree of signal representation detail and design complexity.

The primary objectives of this project are to explore the design methodologies of current steering DACs, understand the challenges involved in high-speed and high-resolution DAC design, and implement a functional prototype using 180nm CMOS technology. By undertaking this project, we aim to gain hands-on experience in the entire design process, from initial concept and simulation to layout and verification.

1.1 Motivation

In the rapidly evolving field of electronics, the demand for efficient, high-performance digital-to-analog converters (DACs) has seen significant growth. DACs are critical components in a wide range of applications, from consumer electronics to industrial instrumentation, telecommunications, and data acquisition systems. They play a pivotal role in converting digital signals, which are prevalent in modern digital systems, into analog signals that can interact with the physical world.

Among various DAC architectures, the current steering DAC is particularly notable for its high speed and precision. This architecture is well-suited for applications requiring fast conversion rates and high resolution, making it ideal for use in modern communication systems, video processing, and high-speed data acquisition.The choice of 180nm CMOS technology for the implementation of the DAC is driven by several factors. Despite the availability of more advanced technologies, 180nm remains a popular choice due to its favorable balance of performance, power consumption, and cost. It offers sufficient speed and density for many high-performance analog and mixed-signal applications, while still being cost-effective and well-supported by a mature design ecosystem.

In summary, the motivation for this project stems from the widespread application of DACs in modern electronics, the specific advantages of the current steering architecture, and the educational value of designing and implementing a high-performance DAC in a widely-used technology node. This project not only addresses a significant practical need but also provides a platform for advancing our technical expertise and contributing to the broader field of analog and mixed-signal circuit design.

1.2 Objectives

The objectives of this project are outlined to guide the systematic development and evaluation of the designed 8 bit Current Steering DAC . The primary goals encompass both technical and practical aspects, aimed at achieving a comprehensive understanding of current steering DAC design principles and their application in real-world scenarios.

a. Design an 8-bit Current Steering DAC:

Develop a comprehensive design for an 8-bit current steering DAC that meets specified performance criteria in terms of speed, linearity, and power consumption.

b. Utilize 180nm CMOS Technology:

Implement the DAC design using 180nm CMOS technology, leveraging its advantages in terms of performance, power efficiency, and cost-effectiveness.

c. Achieve High-Speed Performance:

Ensure the DAC operates at high conversion speeds suitable for applications in communication systems and high-speed data acquisition.

d. Optimize for Linearity and Accuracy:

Focus on achieving high linearity and accuracy in the DAC output, minimizing errors and distortion.

e. Simulate and Validate the Design:

Use simulation tools to validate the performance of the DAC design under various conditions, ensuring it meets the required specifications before fabrication.

f. Analyze Power Consumption:

Evaluate the power consumption of the DAC design, aiming to optimize it for low-power applications without compromising performance.

1.3 Literature survey

The 8-bit current-steering DAC concept was proposed by P. Ramakrishna, M. Nagarani, and K. Hari Kishore. A newly created architecture that has been meticulously customized has yielded a conversion rate of 800 MHz. This DAC is made using 180nm CMOS technology with an operating voltage of 1V. The extremely low power dissipation is 42.92 uW. As a result, the DAC will provide an analog output that steps up until the voltage supply is attained or the digital input is satisfied. The static differential non-linearity error (DNL) is ±0.418 LSB, while the measured integral non-linearity (INL) is less than ±0.31 LSB.[1].

We have presented an 8-bit digital-to-analog converter in this research that operates using weighted current sources.The suggested DAC is developed using UMC180nm technology, which has a 1.8 V reference voltage and 1.8 V supply voltage. The purpose of a current reference with a 3.2µA reference current is to bias the buffer and obtain binary weighted current sources. In order to make the output load independent, the currents corresponding to the high bits of the digital input are added using a resistor, and the voltage that results is then buffered at the output. The step size of the analog voltage output is 7 mV. About the best fit transfer curve, the measured integral non-linearity falls between 0.6LSB and -0.6LSB. and there is better differential non-linearity than 0.8LSB as seen.[2].

This article explores various methods to solve the less-than-ideal characteristics of a current-steering digital-to-analog converter (CSDAC) and discusses the design concerns of a CSDAC. We construct a 12-bit CSDAC in TSMC 40nm technology node and present the simulation results to comprehend the design concerns and how non-idealities impact a CSDAC's performance.[3].

This explores the design and operation of current steering digital-to-analog converters (DACs). The paper likely delves into various aspects of current steering DACs, including their architecture, principles of operation, performance metrics, and applications. These DACs are essential components in various analog and mixed-signal systems, including communication systems, audio equipment, and instrumentation. Razavi's work likely contributes to advancing the understanding and implementation of current steering DACs, potentially offering insights into improving their performance, efficiency, or versatility.[4].

"CMOS Circuit Design, Layout, and Simulation" by R. Jacob Baker, in its third edition, is a comprehensive guide to the design, layout, and simulation of CMOS (Complementary Metal-Oxide-Semiconductor) circuits. This book, part of the IEEE Series on Microelectronic Systems, offers a detailed exploration of CMOS technology, covering fundamental principles, advanced techniques, and practical applications. Topics likely include transistor-level circuit design, layout strategies, simulation methodologies, and optimization techniques. With a focus on CMOS technology, the book provides valuable insights for both beginners and experienced engineers in the field of microelectronics. It likely serves as an essential reference for academics, researchers, and professionals involved in designing integrated circuits for various applications.[5].

The effect of segmentation on current-steering digital-to-analog converters (DACs) is examined in this work. Although segmentation has costs associated with it, it can be utilized to enhance the converter's dynamic behavior. A technique for lowering the degree of segmentation is provided. The 10-bit binary-weighted current-steering DAC that is being shown has ¿60 dB SFDR at 250 MS/s from DC to Nyquist. We ran the device in 9-bit unary, 1-bit binary-weighted mode at 62.5 MHz signal frequency and 250 MS/s. The measurement's

produced 60 dB SFDR shows that the SFDR was unaffected by the converter's binary character. In addition to load currents, the chip consumes 4 mW from two 1.5 V/1.8 V supplies. In a typical 1P-5M, the active area is smaller than 0.35 mm/sup 2/ in a standard 1P-5M 0.18-/spl mu/m 1.8-V CMOS process. Both INL and DNL are below 0.1 LSB.[6].

1.4 Application

The 8-bit current-steering DAC's precision, scalability, and fast speed make it ideal for a wide range of applications. Typical uses for them include:

a. Audio Systems:

Digital audio players, amplifiers, and sound processing devices are just a few examples of the many audio applications that use current-steering digital audio converters (DACs). They are perfect for transforming digital audio signals into high-quality analog waveforms because of their strong linearity and low distortion.

b. Communication Systems:

DACs are used for signal creation, modulation, and demodulation in wireless communication systems. Applications including base stations, transceivers, and software-defined radios that demand quick data translation and good signal fidelity are well suited for current-steering DACs.

c. Medical Imaging:

DACs transform digital data from imaging sensors into analog signals for display or additional processing in medical imaging systems such as magnetic resonance imaging (MRI) and ultrasound devices. The high-speed and high-resolution conversion needed in these applications can be provided by current-steering DACs.

d. Automotive Electronics:

In automotive electronics, DACs are used in applications such as engine control units (ECUs), infotainment systems, and advanced driver assistance systems (ADAS). Current-steering DACs can provide the high-speed and high-resolution conversion required for processing sensor data and controlling various vehicle functions.

e.Video Display Systems:

DACs are used in video display systems, such as monitors, TVs, and projectors, to convert digital video signals into analog signals for driving the display. High-resolution DACs can ensure sharp and accurate image reproduction.

Chapter 2

System design

An 8-bit binary weighted current steering DAC digital input into an analog output by steering currents through a set of weighted current sources. The primary advantage of this design is its high-speed performance.

a. Binary Weighted Current Sources:

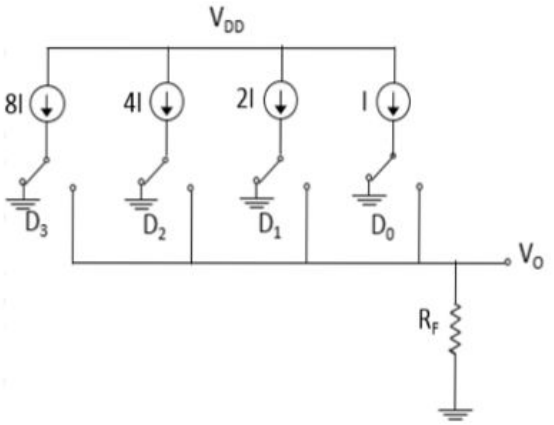

Figure 2.1: Current Steering DAC with 4 bit binary weight

A set of current sources with weights corresponding to the binary input bits.Firstly, it provides high resolution, ensuring precise control over output current levels by leveraging binary-weighted inputs. This high resolution is accompanied by a reduced component count, simplifying circuit design and reducing production costs. Additionally, binary weighted current sources offer fast response times, making them suitable for applications requiring rapid adjustments. Their inherent linearity and the integration of an 8-bit synchronous up-down counter further enhance flexibility, allowing bidirectional current adjustments for dynamic signal processing. Overall, these advantages make binary weighted current sources a robust choice for applications demanding accuracy, efficiency, and versatility in current control.

b. Current Steering Network:

Incorporating PMOS current mirrors and a current steering network into your design offers several notable advantages. When you connect a resistor from VDD to the gate of a PMOS transistor, it acts as an approximation of a current source. However, the output current can be quite sensitive to changes in VDD, which is not ideal for stable operation.To make the output current less sensitive to VDD, the circuit is designed to bias itself. This means that the reference current (IREF) used in the circuit should somehow be derived from the output current (Iout). The goal is to make IREF a replica of Iout so that changes in VDD have less impact on the output current.

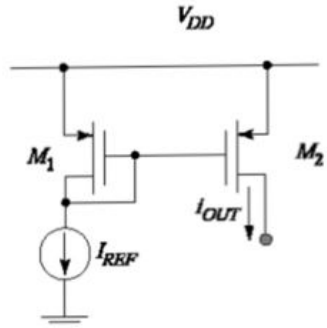

Figure 2.2: PMOS Current Mirror

The use of a current steering network further enhances the versatility and functionality of the design. By dynamically routing currents based on control signals, the current steering network enables flexible current distribution and allocation, facilitating complex operations such as bidirectional current steering or multi-channel current control. This flexibility is particularly valuable in applications requiring adaptive current management or variable current levels based on changing conditions.

c. MOS switch

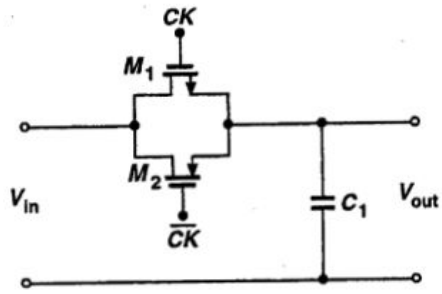

Figure 2.3: Complementary switch

In actuality, due to the significant rise in switch resistance and the ensuing frequency-dependent harmonic distortion, the input swing scarcely surpasses (VDD - VTH)/2.

If the switch is implemented as a complementary pair, then this 12-range can be extended to supply rails.In order to achieve this, complementary clocks are used to control the gates of an NMOS and a PMOS device, causing the two devices to switch on and off concurrently. A rail-to-rail input and output range is provided in this circuit by the NMOS transistor conducting for 0 Vin ¡ VDD - VTHN and the PMOS device being on for —VTHP— ¡ Vin VDD.

In comparison to a single NMOS or PMOS device, the equivalent on-resistance of a CMOS switch changes far less with respect to input voltage. When the on-resistance of a complementary MOS switch, a PMOS, and an NMOS are plotted against the input voltage, the CMOS on-resistance only shows a little peak close to the middle of the range. Reasonable switch sizes are made possible by the relatively constant on-resistance throughout the whole input/output range, which also reduces harmonic distortion brought on by switch resistance change.

2.1 Functional block diagram

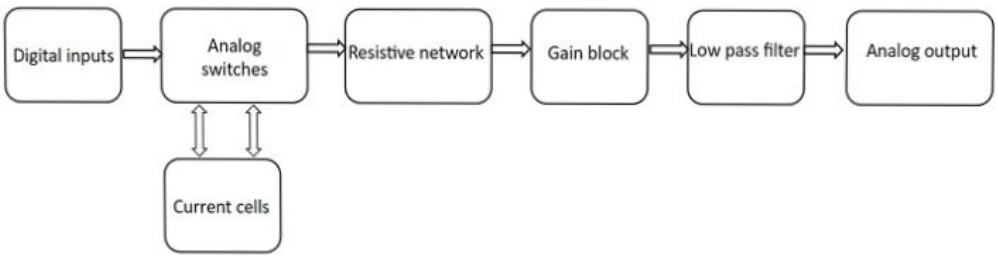

Figure 2.4: Block diagram of Current steering DAC

The block diagram illustrates the system design of an 8-bit Current Steering Digital-to-Analog Converter (DAC). The system begins with digital inputs that feed into the analog switches, which are responsible for routing the appropriate currents from the current cells. The current cells generate precise currents corresponding to each digital input. These currents are then combined in the analog switches based on the digital input values. This current-steering mechanism allows for precise control and conversion of digital signals into corresponding current levels, which are essential for the subsequent conversion stages.

Following the analog switches, the combined currents are passed through a resistive network. This network helps in summing and converting the current into a voltage. The resulting voltage is then fed into a gain block, which amplifies the signal to the required level. Post amplification, the signal passes through a low pass filter, which smooths out high-frequency components and noise, ensuring a clean analog output. The low pass filter is crucial for eliminating any spurious signals or glitches from the conversion process, providing a stable and accurate analog signal. The final analog output is a smooth, continuous representation of the original digital input, suitable for various analog applications.

2.2 Design alternatives

a. DAC using p-mos as switch

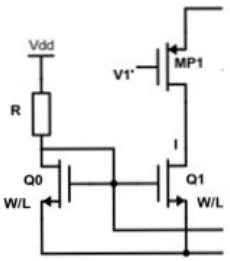

Figure 2.5: DAC current cell

- On-Resistance: PMOS transistors generally have higher on-resistance compared to NMOS transistors. To mitigate this, the PMOS switches need to be properly sized to ensure that their on-resistance does not significantly affect the performance. Optimizing the width-to-length (W/L) ratio of the PMOS transistors can help in reducing the on-resistance.
- Switching Speed: PMOS transistors switch slower than NMOS transistors due to lower carrier mobility of holes compared to electrons. Ensuring sharp control signals and minimizing parasitic capacitances can help improve the switching speed. Additionally, using high-speed design techniques and careful layout can mitigate this issue.
- Threshold Voltage: The threshold voltage (Vth) of PMOS transistors is typically higher than that of NMOS transistors. This can impact the switching performance and the control voltage range. Proper biasing and selection of transistor dimensions are necessary to ensure reliable operation within the desired voltage range.
- Gate Drive Considerations: Driving the gates of PMOS transistors requires a different approach compared to NMOS transistors. The gate voltage must be sufficiently lower than the source voltage to turn the PMOS transistor on. This requires careful design of the gate driver circuitry to ensure proper switching without introducing delays or errors.

b. DAC using n-mos as switch

- Substrate Noise: NMOS transistors can inject more noise into the substrate compared to PMOS transistors. This noise can degrade the performance of the DAC, particularly in sensitive mixed-signal environments. Proper isolation techniques, such as deep n-wells or triple-well processes, can be employed to mitigate this issue.
- Leakage Currents: Although NMOS transistors have lower on-resistance, they can exhibit higher leakage currents in the off state compared to PMOS transistors. Managing these leakage currents is crucial to maintaining the accuracy and stability of the DAC output.
- Gate Drive Requirements: Driving NMOS gates requires a voltage level higher than the source voltage for switching them on. This necessitates careful design of the gate drive

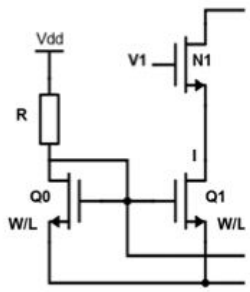

Figure 2.6: DAC current cell

circuitry to ensure robust switching performance without excessive power consumption or delays.

- Charge Injection and Clock Feedthrough: NMOS switches are prone to charge injection and clock feedthrough, which can introduce errors into the analog output.

2.3 Final design

DAC using transmission gate as switch

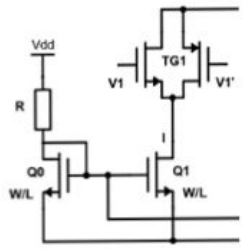

Figure 2.7: DAC current cell

- Bidirectional Conductivity: Transmission gates, composed of parallel NMOS and PMOS transistors, can conduct current in both directions, making them highly versatile for switching applications in DACs. This bidirectional capability ensures efficient current steering regardless of the direction of the current flow.
- Low On-Resistance: When both NMOS and PMOS transistors in a transmission gate are turned on, their combined on-resistance is significantly lower than that of either transistor alone. This results in minimal voltage drop across the switch, enhancing the overall linearity and performance of the DAC.
- Wide Operating Range: Transmission gates provide a wide operating voltage range because they can effectively pass both high and low voltage levels. This is particularly useful in mixed-signal designs where the signal levels can vary widely.
- Reduced Charge Injection and Clock Feedthrough: By balancing the charge injection of NMOS and PMOS transistors, transmission gates can significantly reduce the overall charge injection and clock feedthrough effects, leading to more accurate and stable analog output.

Chapter 3

Implementation details

3.1 Specifications and final system architecture

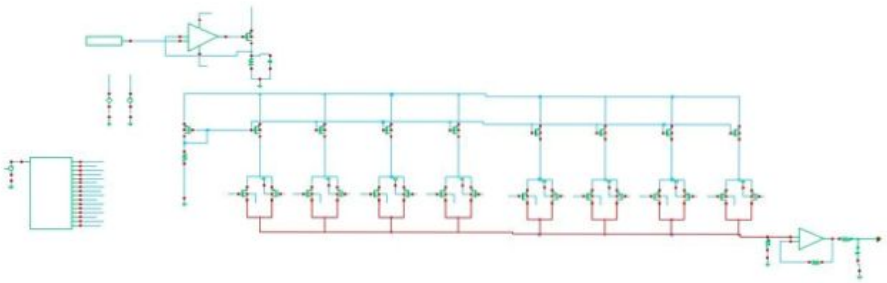

Figure 3.1: Proposed DAC architecture

Firstly, we employ an 8-bit synchronous up/down counter to generate digital inputs for the DAC. This choice ensures precise control over the input states, with synchronous operation guaranteeing simultaneous changes across all bits on a clock edge. The up/down functionality adds versatility by allowing us to increase or decrease the output voltage as needed, contributing to the DAC's flexibility in operation.

Next, the digital inputs are fed into transmission gate switches within the binary weighted current steering network. These switches, composed of PMOS and NMOS transistors, selectively pass the weighted currents based on the input bits. The decision to use binary weighting stems from its exponential increase in current levels for each bit. For example, in an 8-bit system, the LSB represents $\frac{1}{256}$of the full-scale current, while the MSB represents $\frac{128}{256}$of the full-scale current. This binary weighting scheme allows for fine resolution in output voltage steps.

Within the DAC, PMOS current mirrors are utilized to replicate and scale the reference current provided by the bandgap reference (BGR). These mirrored currents serve as the basis

Specification	Ideal value	Obtained value
Full scale voltage	1.8 V	1.65 V
INL (LSB)	less than 1 LSB	less than 0.6 LSB
DNL (LSB)	less than 1 LSB	0.8 LSB
Offset	0 V	4 mV
Gain	7 mV/LSB	5.5 - 7 mV/LSB
Latency	0 sec	1 u sec
Dynamic range	48.16 dB	48.16 dB

Table 3.1: Performance Specifications of the DAC

for the binary weighted current sources, ensuring accurate current replication with minimal variation. This choice is crucial for maintaining precision and stability in the DAC's output.

To convert the summed current to a voltage signal, an operational amplifier (op-amp) gain block is employed. The op-amp's gain is set to convert the current signal to a suitable voltage level. This gain calculation involves determining the ratio of the output voltage to the input current, ensuring accurate voltage representation of the DAC's output.

In addition to the circuit components mentioned, a bandgap reference (BGR) current reference is integrated to generate a stable and precise reference current. This reference current serves as the foundation for the mirrored currents and contributes to consistent performance across varying operating conditions, such as temperature changes.

Finally, an RC filter is incorporated into the circuit to smooth the output voltage. This filter attenuates high-frequency noise and ripple, resulting in a clean and stable analog output. The cutoff frequency of the RC filter is determined based on the desired trade-off between bandwidth and noise filtering, optimizing the DAC's performance.

3.2 Algorithm

Step 1: Receive digital input signals from 8-bit synchronous up-down counter. Ensure proper formatting and timing of digital inputs.

Step 2: Transmission Gate Switches. Design transmission gate switches to control current flow based on digital inputs. Implement control logic for transmission gates to ensure accurate switching.

Step 3: Interface with Current Cells. Interface transmission gate switches with current cells.Ensure bidirectional communication between transmission gate switches and current cells to regulate current accurately. Design current cells to generate precise current levels based on input control signals from the transmission gates. Current is taken from the BGR current reference of 10uA.

Step 4: Resistive Network. Design and implement a resistive network to convert the controlled current into a proportional voltage. Ensure the resistive network has appropriate impedance to match the current levels from the current cells.

Step 5: Gain Block. Integrate a gain block to amplify the signal from the resistive network.

Design the gain block to maintain linearity and minimize distortion in the amplified signal.

Step 6: Low Pass Filter. Design and implement a low pass filter to remove high-frequency noise and smooth the output signal. Ensure the cutoff frequency of the low pass filter is appropriate for the desired output signal bandwidth.

Step 7: Generate Analog Output. Combine the processed signal from the low pass filter to generate the final analog output. Ensure the analog output accurately represents the input digital signal.

Chapter 4

Optimization

4.1 Introduction to optimization

We have investigated the effectiveness of several switch designs in the segmented DAC design in our paper. Three architectures—NMOS, PMOS, and transmission gate-based designs—were carefully examined. Every design has unique switching components as well as a shared current mirror component. Unwanted results, characterized by large glitches and low linearity, were obtained from the NMOS switch-based architecture. Specifically, noticeable errors happened when digital inputs changed, which resulted in inconsistent output step sizes. The integral non-linearity (INL) and differential non-linearity (DNL) errors were both negatively impacted by this discrepancy. Analogous problems were also present in the PMOS switch-based architecture, where output did not increase in step with growing digital inputs.On the other hand, a viable substitute was found in the transmission gate architecture. This design significantly reduced glitches and made sure that current output increased continuously, which helped to mitigate DNL and INL problems. The superiority of the suggested current steering DAC using transmission gate switches was highlighted by graphical representations of INL and DNL.

4.2 Types of Optimization

The way in which the current steering DAC can be designed is by using transmission gate.

Transmission Gate Configuration

Identified significant glitches in NMOS and PMOS switch-based architectures, particularly during transitions in digital inputs. Transmission gate architecture exhibited a notable reduction in glitches, enhancing the stability and reliability of the DAC output. Observed poor linearity in NMOS and PMOS switch-based architectures due to glitches and inconsistent output responses. Transmission gate architecture offered improved linearity by ensuring a continuous rise in current output, minimizing INL and DNL errors.

4.3 Selection and justification of optimization method

The main focus of the optimization that has been highlighted is on improving the efficiency and performance of DAC by carefully choosing and implementing switch designs. More specifically, the goal is to minimize glitches and maximize the linearity of the circuit.

1. **Switch Architecture Optimization**:
    - Choosing the best switch architecture from NMOS, PMOS, and transmission gate-based designs is the primary goal. This entails assessing each architecture's performance in terms of improved linearity and glitch reduction.
2. **Linear Optimization**:
    - The goal of linearity optimization is to reduce the errors associated with differential and integral non-linearity (DNL) in DAC systems. The process of optimization entails locating and reducing the elements that lead to linearity mistakes, such as bugs and irregular output reactions to modifications in digital input.
3. **Glitch Reduction Optimization**:
    - To guarantee fluid and consistent output responses, the emphasis here is on minimizing glitches, especially during transitions in digital inputs. The goal of this modification is to improve the DAC outputs' stability and dependability under various input scenarios.
4. **Noise Margin Optimization**:
    - To address the problems brought on by a smaller noise margin in the transmission gate arrangement, the mix of PMOS and NMOS transistors should be optimized. This improvement reduces the circuit's vulnerability to noise interference and guarantees reliable circuit operation.
5. **Power Efficiency Optimization**:
    - Taken into account the effects of every switch architecture on power consumption. evaluated the transmission gate architecture's potential to provide higher power efficiency than NMOS and PMOS switches because of its constant current rise and decreased glitches.
6. **Robustness and Reliability**:
    - The DAC architecture's resilience and robustness under varied operating circumstances and environmental influences were given top priority. The transmission gate architecture is known for providing exceptional resilience and dependability because of its steady current rise characteristics and decreased susceptibility to glitches, which provide stable performance over time.

Chapter 5

Results and discussions

5.1 Result Analysis

The result obtained for the proposed current steering DAC by providing input from designed counter designed is given below.

a. Proposed DAC simulation result.

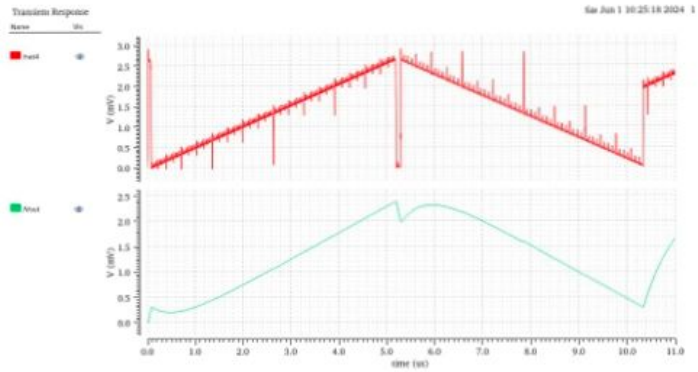

Figure 5.1: DAC results for the proposed model.

PVT analysis is a semiconductor manufacturing methodology that evaluates how fluctuations in supply voltage, operating temperature, and process factors affect integrated circuit (IC) performance. Through PVT analysis, engineers and designers assess how variations in these parameters impact critical performance indicators like IC speed, power consumption, and reliability. They can optimize the design and manufacturing processes to satisfy performance criteria and raise the overall quality of the product by knowing how sensitive the integrated circuit is to changes in procedure, voltage, and temperature.

b. Results from PVT analysis is provided below.

PVT analysis - 1

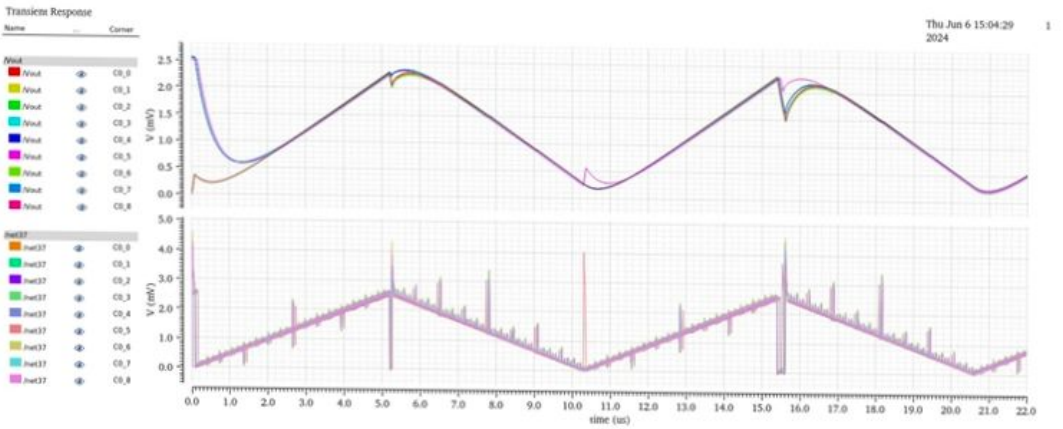

Figure 5.2: PVT analysis - 1.

PVT analysis - 2

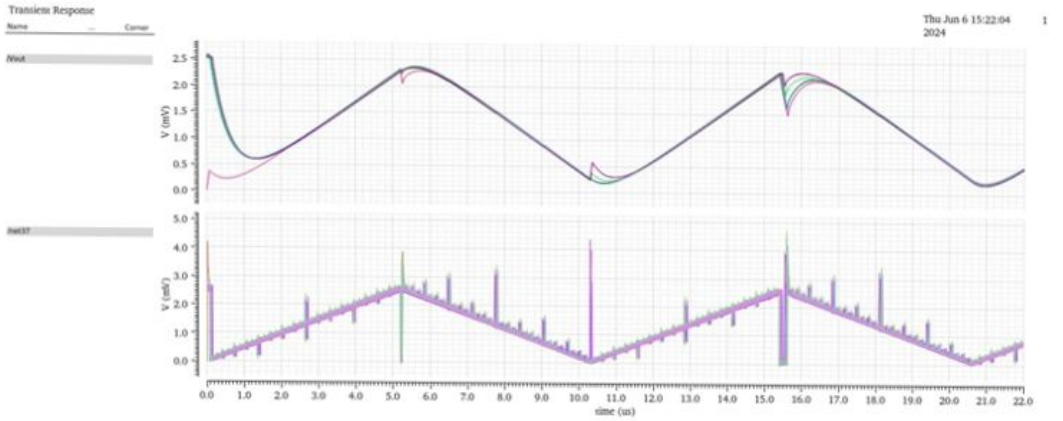

Figure 5.3: PVT analysis - 2.

PVT analysis - 3

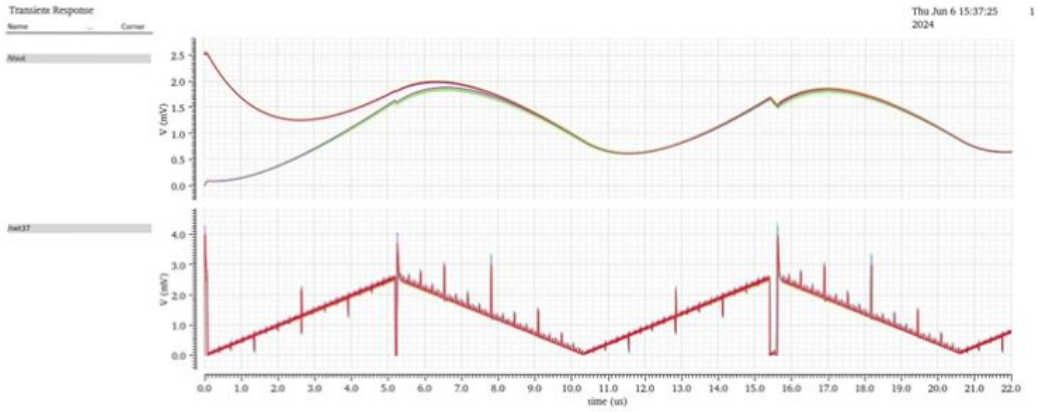

Figure 5.4: PVT analysis - 3.

PVT analysis - 4

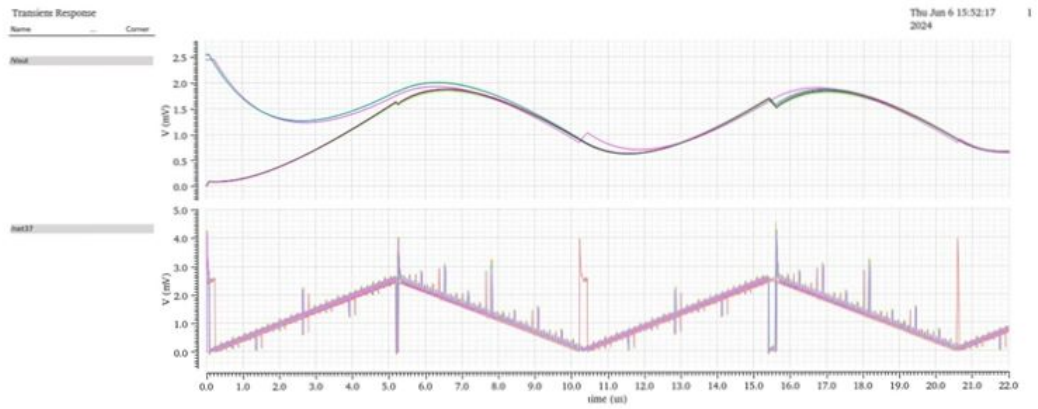

Figure 5.5: PVT analysis - 4.

Chapter 6

Conclusions and future scope

6.1 Conclusion

In conclusion, this project successfully designed and simulated a 8-bit Digital-to-Analog Converter (DAC) using Virtuoso 6.1.6 and UMC180nM technology. By adopting transmission gate instead of conventional switches, the DAC demonstrated superior performance, showcasing high precision and low sensitivity to process variations. The implementation in Cadence Virtuoso at a 180nm technology node yielded simulation results that met the specified project requirements and the transfer curve of the DAC is monotonic for all the digital inputs from [00000000] to [11111111]. It is almost similar to the ideal DAC transfer curve and a slight gain variation is observed only for higher digital word above [10101010]. The advantages of transmission gate optimisation were evident, as the DAC exhibited enhanced linearity and noise rejection compared to conventional resistor-based designs. This study highlights the efficacy of the proposed design in achieving, thereby contributing valuable insights to the field of data convertor design.

6.2 Future scope

The successful design and simulation of the 8-bit Digital-to-Analog Converter (DAC) circuits present promising avenues for future applications in various societal contexts. Here are some potential future scopes and applications:

Embedded Systems: Integration of the DAC circuits into embedded systems for applications such as sensor interfacing, audio processing, and motor control in IoT devices, wearable technology, and smart appliances.

Industrial Automation: Deployment of DAC circuits in industrial automation systems for process control, instrumentation, and monitoring applications, optimizing production efficiency and quality control processes.

Test and Measurement Equipment: Integration of DAC circuits into test and measurement equipment for calibration, signal generation, and waveform synthesis, facilitating accurate and reliable testing across various industries.

Consumer Electronics: Integration of DAC circuits into consumer electronics products such as smartphones, tablets, and gaming consoles, enabling high-quality audio/video playback, immersive gaming experiences, and multimedia content creation.

Medical Devices: DACs are integrated into medical imaging and diagnostic equipment such as MRI machines, ultrasound devices, and CT scanners for converting digital image data into analog signals used to drive display screens or to modulate signals for imaging purposes. They ensure accurate representation of medical images for diagnosis and treatment planning.

Automotive Electronics: Integration of DAC circuits in automotive electronics for vehicle control systems, infotainment systems, and driver assistance features, improving vehicle performance, safety, and user experience.

Data Acquisition Systems: DACs are incorporated into data acquisition systems for converting digital sensor readings, measurements, or control commands into analog signals for processing, analysis, and visualization. They enable the acquisition and conversion of digital data from sensors, transducers, and measurement devices into analog signals for monitoring and control purposes.

Power Electronics: DACs are employed in power electronics applications for generating analog control signals used in power converters, inverters, and motor drives for controlling the operation of power electronic devices such as switches, thyristors, and transistors. They enable precise control and modulation of power conversion processes.

Avionics and Aerospace Systems: DACs are used in avionics and aerospace systems for converting digital signals into analog signals used in flight control systems, navigation equipment, and communication systems on aircraft, spacecraft, and satellites. They ensure accurate control and communication in aerospace applications.

Security and Surveillance Systems: DACs are integrated into security cameras, surveillance systems, and video capture devices for converting digital video signals into analog signals used for display, recording, and transmission. They enable the conversion of digital video streams from surveillance cameras into analog signals for monitoring and surveillance applications.

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