CMOS

OPEN ENDED

# 3 BIT PARALLEL ADDER USING CMOS AND PSEUDO NMOS LOGIC

Team 23

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# CMOS LOGIC:

Fig a. Full adder Schematic

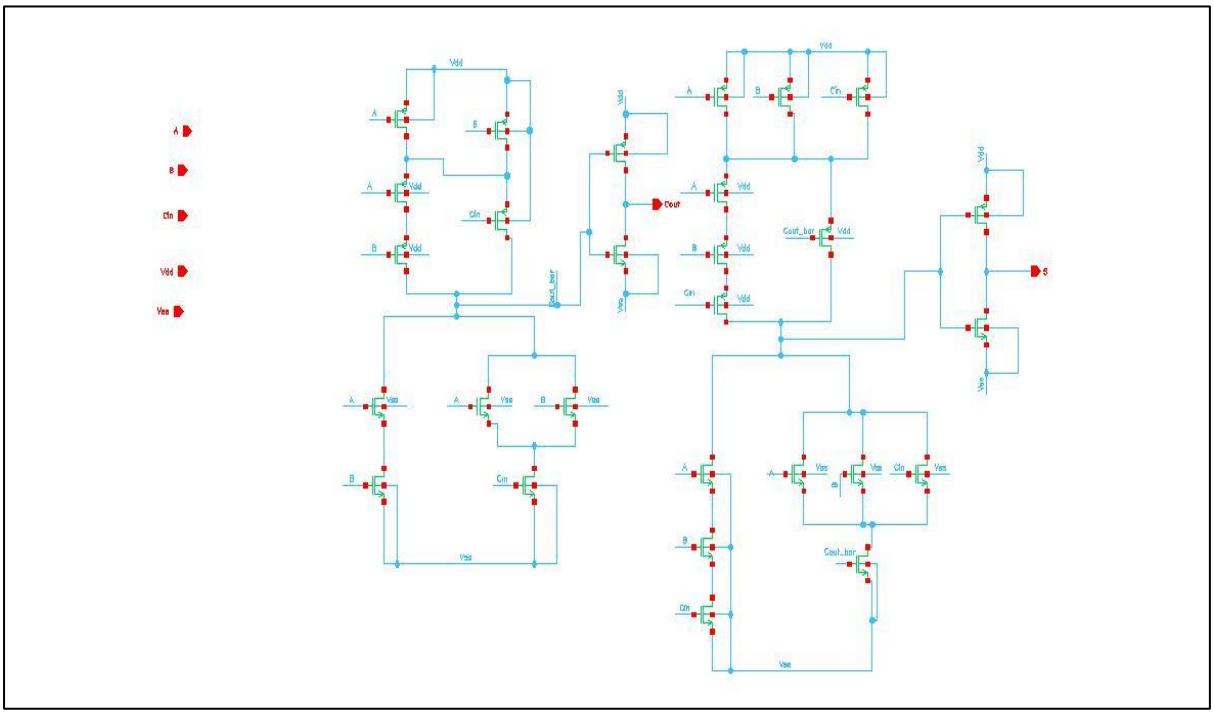


Fig b. Full adder Symbol

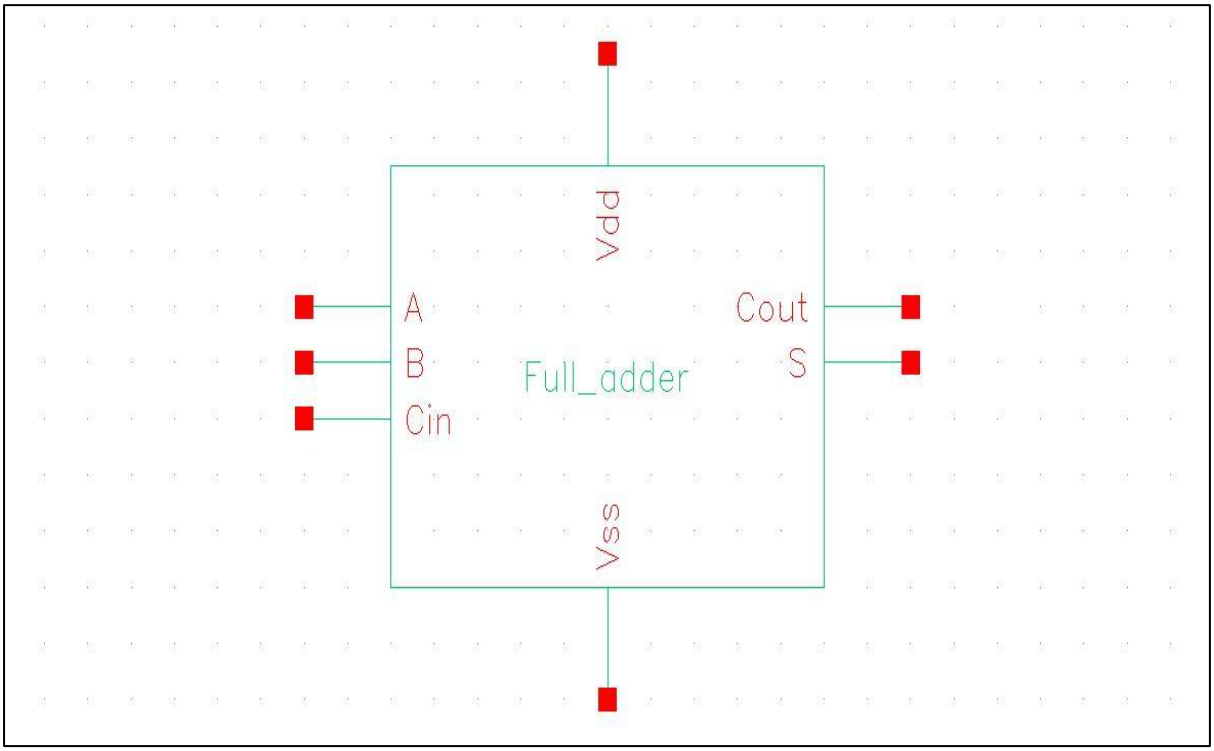
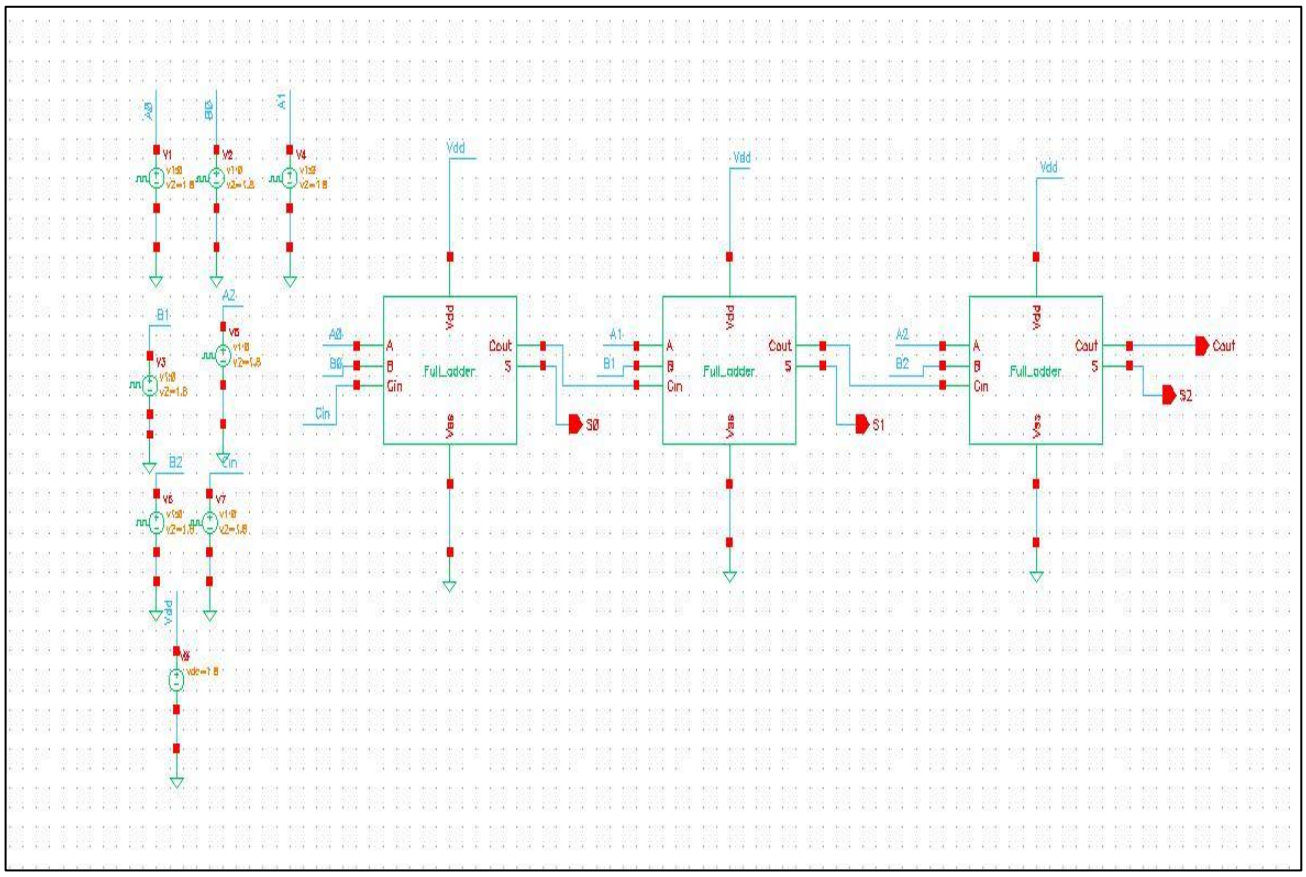


Fig c. 3-bit parallel adder test circuit



# PSEUDO NMOS LOGIC:

Fig a. Full adder Schematic

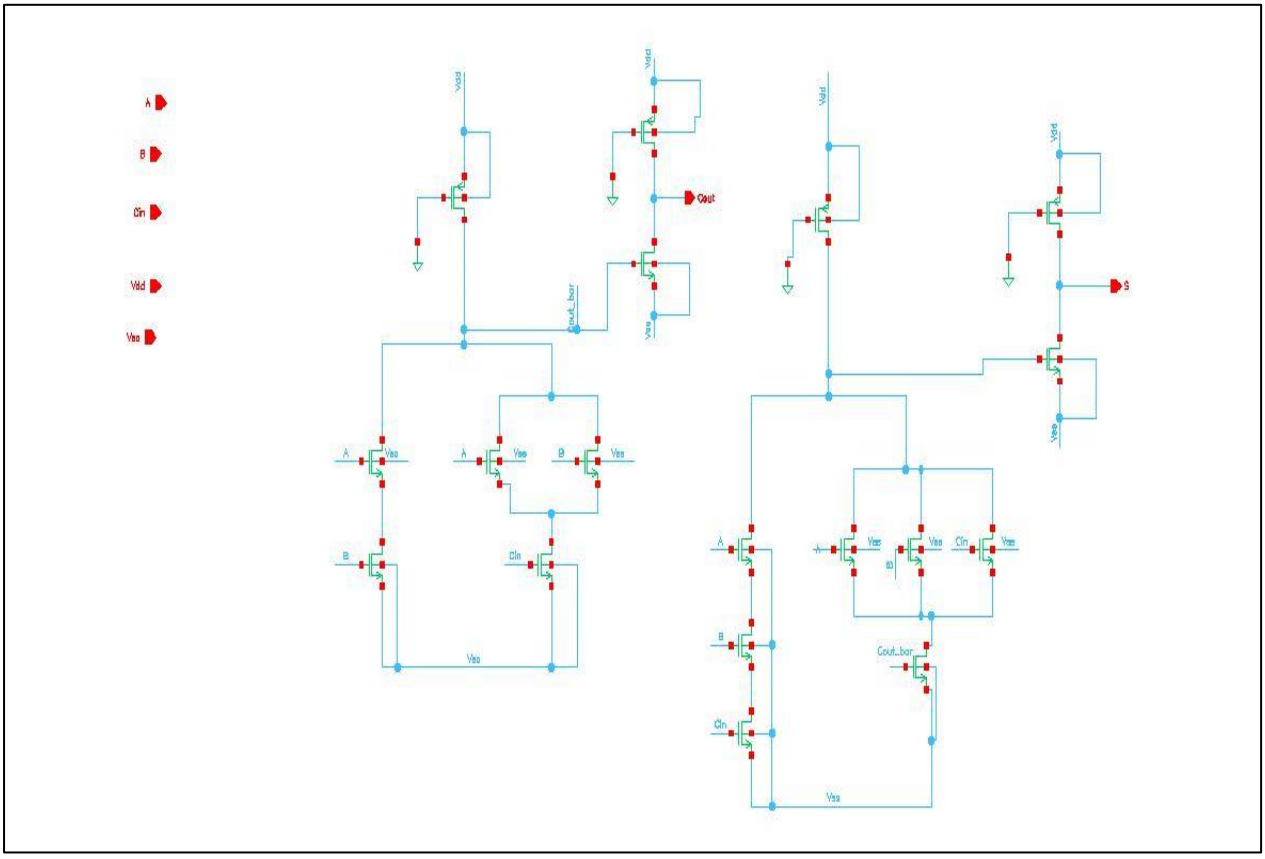



Fig b. Full adder symbol

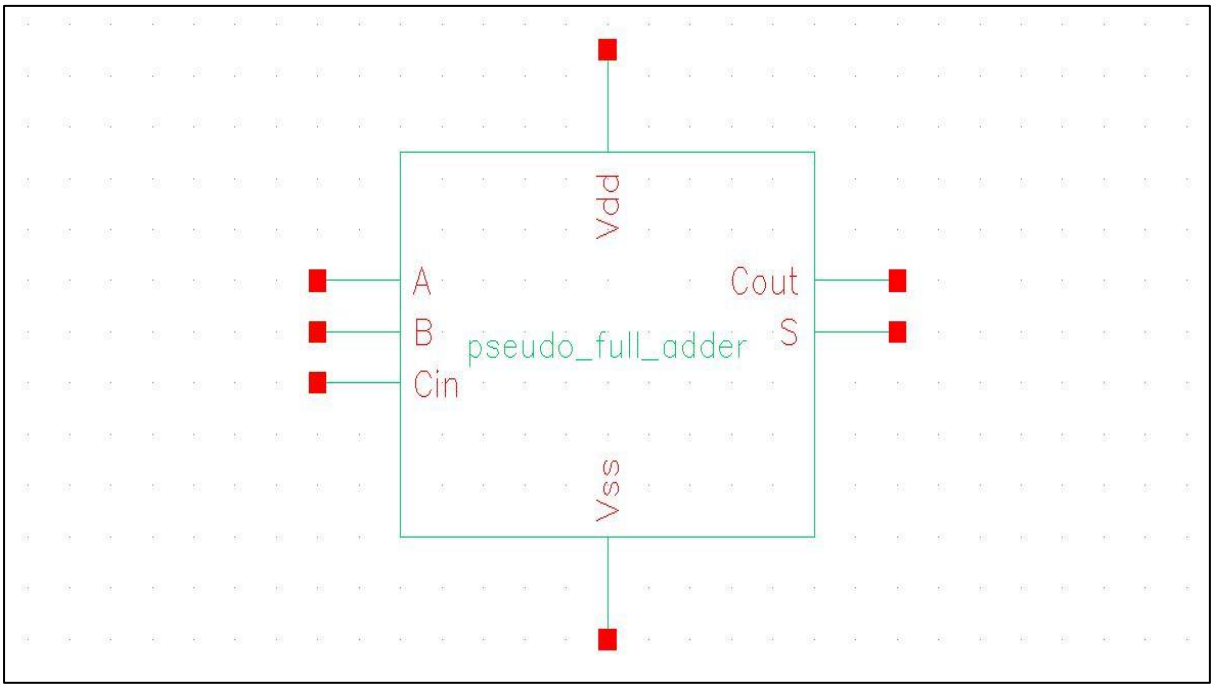
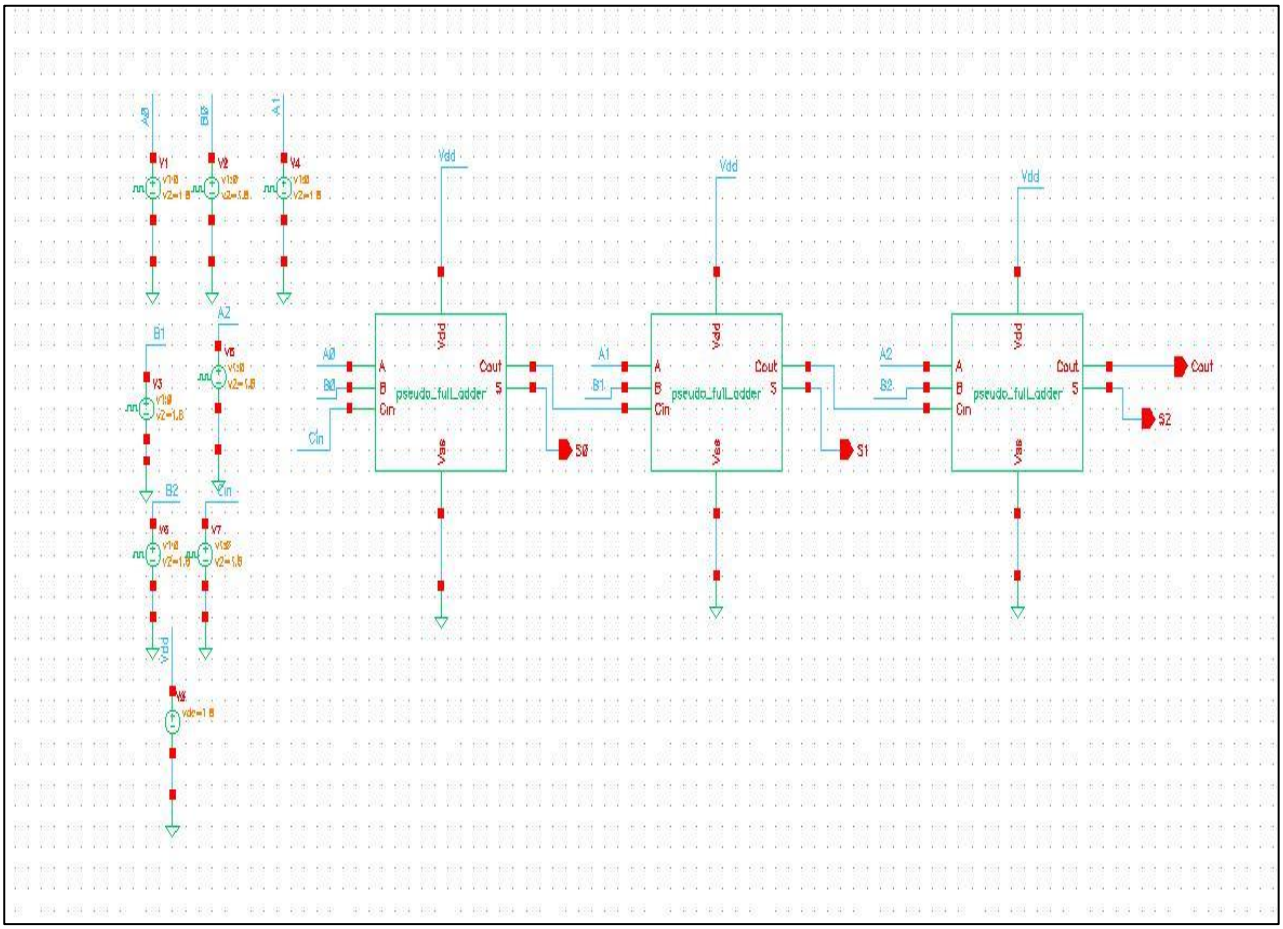
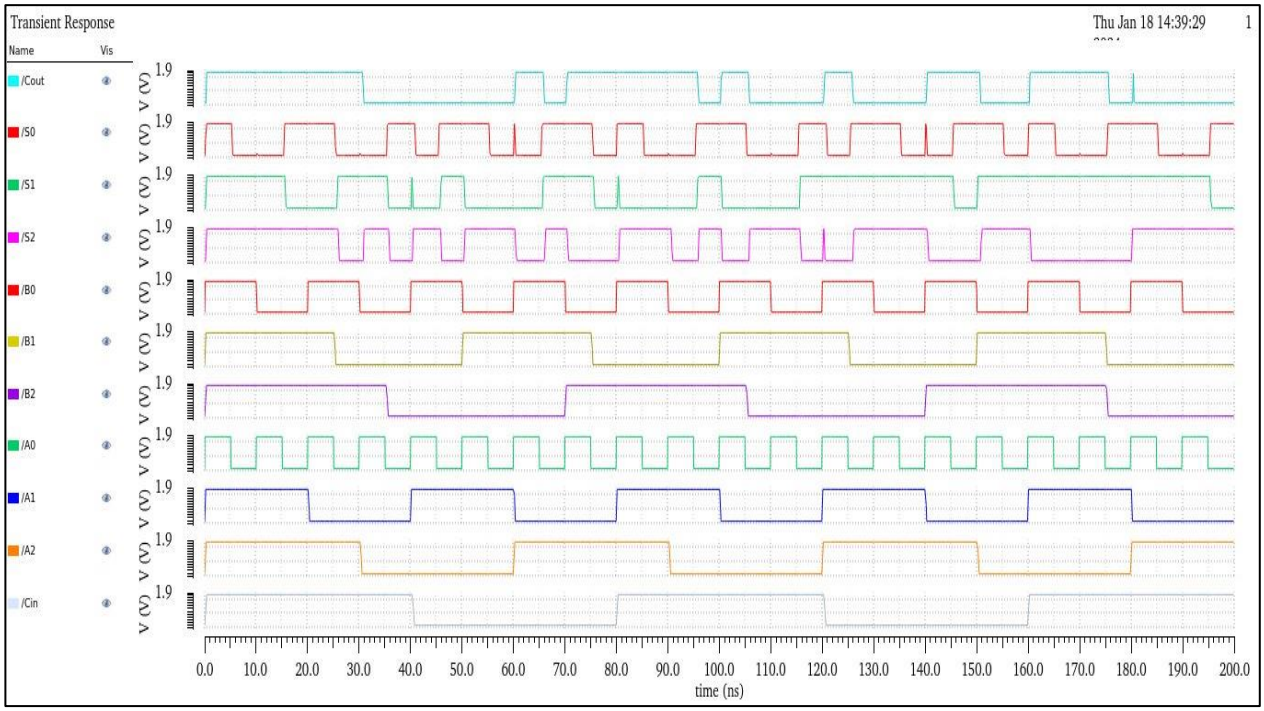


Fig c.3-bit parallel adder test circuit

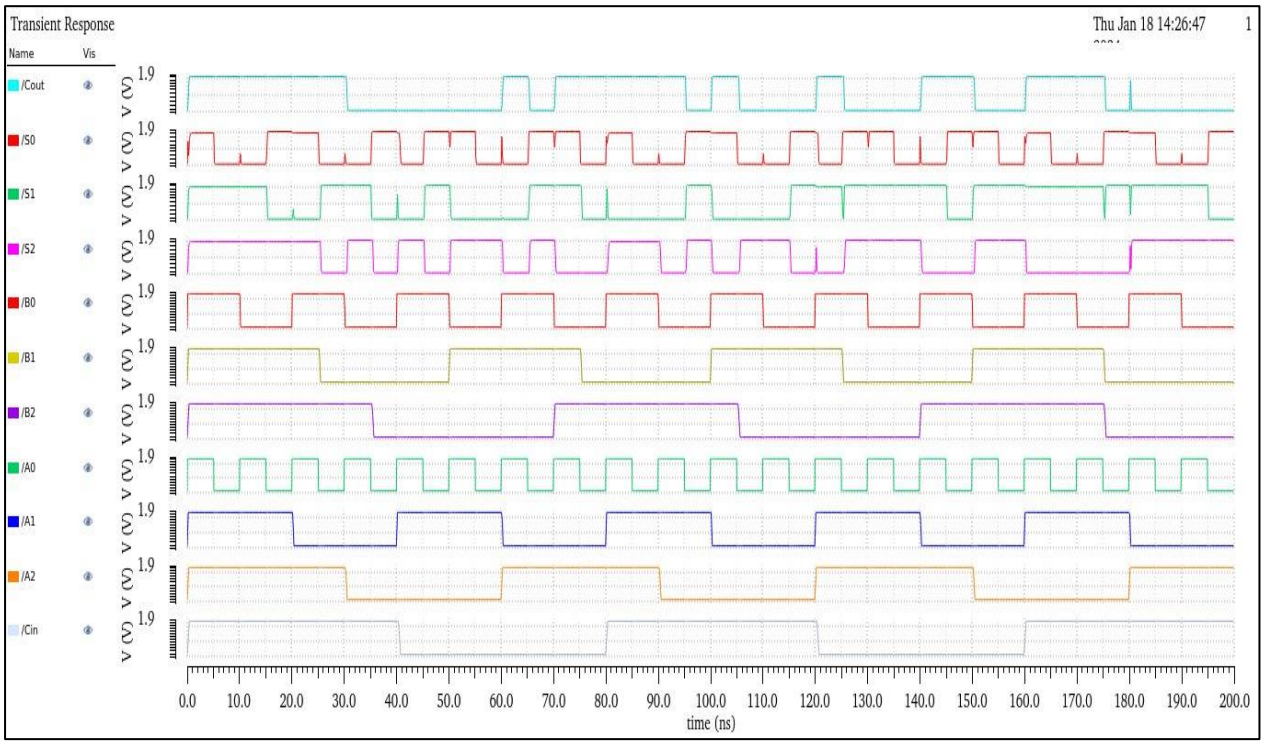


# RESULTS:

- ## CMOS LOGIC:




- ## PSEUDO NMOS LOGIC:



# CONCLUSION:

| | CMOS LOGIC | PSEUDO NMOS LOGIC |
|---|---|---|
| Delay(td) | 228.3 ps | 154.3 ps |
| Power | 886.3 mW | 907.4mW |
| Area (no of transistors) | 84 | 54 |

- Pseudo nmos logic is better compared to cmos logic in delay time
- Cmos logic is better compared to pseudo nmos in terms of average power
- Pseudo nmos occupies less area compared to cmos logic
- Overall Pseudo nmos logic is better than cmos logic for the design of 3 bit parallel adder.