

EE618 - CMOS Analog VLSI Design

Electrical Engineering Department

IIT-Bombay

Autumn 2021

COURSE Project: Autumn 2021

Total Marks : 100

Task : Design and simulate Operational Transconductance Amplifier With Class-B Slew-Rate Boosting for Fast High-Performance Switched Capacitor Circuits in PTM 130nm technology

Submission Deadline: 11:55 pm, Friday, 5th Nov. 2021.

Reference paper

M. H. Naderi, S. Prakash and J. Silva-Martinez, "Operational Transconductance Amplifier With Class-B Slew-Rate Boosting for Fast High-Performance Switched-Capacitor Circuits," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3769-3779, Nov. 2018, doi: 10.1109/TCSI.2018.2852273.

General Instructions:

- The report submission is through the link provided on EE618 Moodle webpage.
- In this project you will design an OTA specified in the reference paper.
- Use PTM 130nm CMOS technology model with $V_{DD} = 1.5$ V, $V_{SS} = 0$ V.
- Maximum transistor length in the design should not be more than $2\text{ }\mu\text{m}$.
- Bulk of NMOS transistor should be connected to VSS & Bulk of the PMOS transistor should be connected to its Source.
- Use practical MOSFET based current source & current mirrors.
- The submission report should be neatly formatted.

Target Specifications of the OTA:

Parameters		Specifications
Static Power Consumption	Bias circuit + Pseudo class AB Amplifier	$<4.5 \text{ mW}$
	Bias circuit + Pseudo class AB Amplifier with SR boosting	$<5.25 \text{ mW}$
Input DC common mode voltage		0.75V
DC Voltage Gain		$>70 \text{ dB}$
Small signal GBW, Gain Bandwidth Product, (UGF) of voltage gain		$>1\text{GHz}$
Open Loop Phase Margin		$>60^\circ$
Load Capacitance		0.5pF
Slew Rate	Pseudo class AB Amplifier	$>400 \text{ V}/\mu\text{S}$
	Pseudo class AB Amplifier with SR boosting	$>900 \text{ V}/\mu\text{S}$
Input referred Noise ($V_{in,n}(\text{rms})$) (1Hz to 250 MHz)		$<200 \text{ nV}_{rms}$
Maximum fully differential Output swing		$\pm 1.3\text{V}$
1% settling time	Pseudo class AB Amplifier	$<4\text{ns}$
	Pseudo class AB Amplifier with SR boosting	$<3\text{ns}$
CMRR for input offset = 20mV		$>100 \text{ dB}$

Note : In each section, 1 mark is allotted for clarity of plots, annotations and explanation of graphs. Submission document should be neatly formatted.

1. Pseudo class AB design [20 + 1 Marks]

1. Report the design flow of the OTA in the form of step-by-step procedure. Design flow involves determining bias currents, voltages, and size of transistors to meet target specifications. [10 Marks]
2. The design procedure may not achieve the target specs in a single iteration. Hence, show successive iterations of design flow that finally achieve the target specs. [8 Marks]
3. Clearly show bias currents and voltages on the schematic. [1 Mark]
4. Write size of transistors in a table. (Keep names of transistors same as reference paper) [1 Mark]

2. Auxiliary circuit design (refer to the reference paper) [10 + 1 Marks]

1. Report the design flow of the auxiliary circuit in the form of step-by-step procedure. [5 Marks]
2. Show successive iterations, if any (as explained in 1.2 above). [3 Marks]
3. Clearly show bias currents and voltages on the schematic. [1 Mark]
4. Write size of transistors in a table. (Keep names of transistors same as reference paper) [1 Mark]

3. Current Reference Generator Circuit Design [10 + 1 Marks]

In this section of the project, you will design a reference generator circuit of your choice. Reference generator circuits include reference current source (I_{ref}) of your choice and current mirrors that use I_{ref} to generate bias voltages.

1. Draw the Reference current source for ($I_{\text{ref}} = 50 \mu A$), and current mirrors that you use to generate bias voltages for main class AB amplifier as well as auxiliary circuit. [4 Marks]
2. Report the step-by-step design procedure for reference generator circuits. [5 Marks]
3. Tabulate the size of transistors used in the circuit. [1 Mark]

4. DC Operating point simulations [6 + 1 Marks]

- Apply DC common mode voltage (VCM) to the input terminals of the OTA.
- Run DC simulations on the OTA and the Auxiliary circuit including reference generator and find DC operating points.
- DC operating points should clearly show all the node voltages and currents through each transistor.

5. AC simulations [12 + 1 Marks]

1. For pseudo class AB amplifier:

- Plot the open loop fully differential voltage gain (in dB) and phase (in degrees) as a function of frequency (Bode plot). (Use common mode DC voltage: 0.75 V, AC signal for $V_{in}^+ = 1$ and $V_{in}^- = 0$). [3 Marks]
- Highlight clearly GBW, Gain cross over frequency and phase cross over frequency. [2 Mark]
- Report Phase margin, small signal GBW and Open loop gain in dB. [1 Mark]

2. For pseudo class AB amplifier with auxiliary class B booster circuit:

- Plot the open loop fully differential voltage gain (in dB) and phase (in degrees) as a function of frequency (Bode plot). (Use common mode DC voltage: 0.75 V, AC signal for $V_{in}^+ = 1$ and $V_{in}^- = 0$) [3 Marks]
- Highlight clearly GBW, Gain cross over frequency and phase cross over frequency [2 Mark]
- Report Phase margin, small signal GBW and Open loop gain in dB. [1 Mark]

6. Settling Time & Slew rate calculation [18 + 1 Marks]

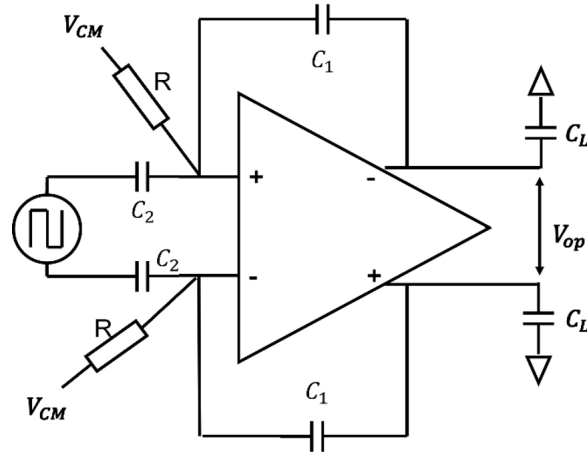


Figure 1: Settling Time setup

1. Connect the OTA as shown in fig. 1 with gain -1 and plot the fully differential output voltage. Choose appropriate value of C_1 and C_2 and R . consider $V_{CM} = 0.75V$. (To avoid loading effect, C_1 and C_2 should be less than $0.1 * C_L$.) [2 Marks]

- Square wave specification:

- $T_{rise} = T_{fall} = 1 \text{ ps}$
- $V_{pp} = 0.5V$
- $T_{on} = 100ns$
- $T_{period} = 200ns$

2. Plot V_{op} for [4 marks]

- Pseudo class AB amplifier only
- Pseudo class AB amplifier with auxiliary class B booster circuit

3. Calculate Slew rate by calculating time required for V_{out} to reach from 0V to 0.3V & 0.5V to 0.2V [4 Marks]

- $SR^+ = \frac{0.3V}{\text{time required for } V_{out} \text{ to reach from } 0V \text{ to } 0.3V}$
- $SR^- = \frac{0.3V}{\text{time required for } V_{out} \text{ to reach from } 0.5V \text{ to } 0.2V}$

4. Report average SR for [4 marks]

- Pseudo class AB amplifier only
- Pseudo class AB amplifier with auxiliary class B booster circuit
- $SR_{average} = \frac{SR^+ + SR^-}{2}$

5. Report 1% settling time for [4 Marks]

- Pseudo class AB amplifier only
- Pseudo class AB amplifier with auxiliary class B booster circuit

7. Noise Analysis [10 + 1 Marks]

1. Plot Input referred noise voltage for [4 Marks]
 - Pseudo class AB amplifier only
 - Pseudo class AB amplifier with auxiliary class B booster circuit
2. Report Total Integrated input referred noise for 1Hz to 250MHz for [3 Marks]
 - Pseudo class AB amplifier only
 - Pseudo class AB amplifier with auxiliary class B booster circuit
3. Calculate Flicker noise corner frequency for [3 Marks]
 - Pseudo class AB amplifier only
 - Pseudo class AB amplifier with auxiliary class B booster circuit

8. Common Mode analysis [6 + 1 Marks]

1. Calculate Common mode input range for the designed OTA for $|(V_{GST})_{min}| = 0$ V. [2 Marks]
2. Report CMRR value [2 Marks]

$$CMRR = 20 \log \frac{A_{DM}}{A_{CM-DM}},$$

where A_{DM} is the differential mode gain & A_{CM-DM} is the common mode to differential mode gain.

Apply DC offsets at the input terminals along with common mode small signal input as shown in fig. 2 and simulate the common mode to differential gain (A_{CM-DM}). The DC offset voltages model the mismatch in threshold voltage of input transistors.

3. Plot fully differential common mode AC magnitude and phase response of the Pseudo class AB OTA. [2 marks]

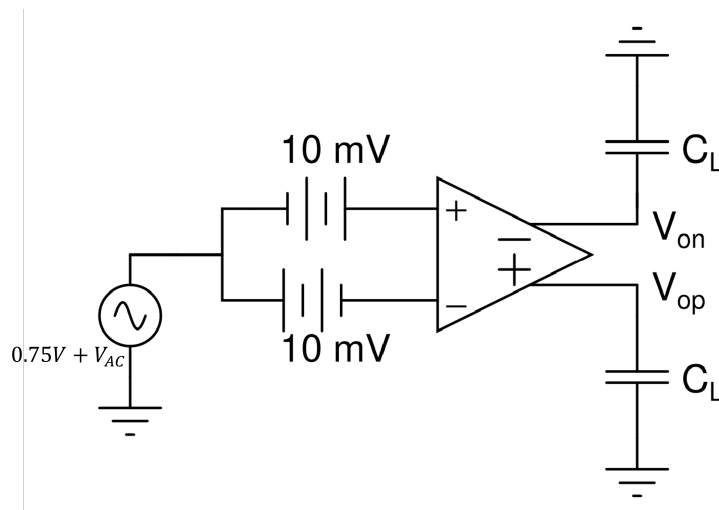


Figure 2: CMRR measurement setup

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Work contribution template

- You have to write work contribution from each member of your group at the end of project report using this template.
- Write the names of your group members in place of Member 1 and Member 2. For each question number, put a checkmark (✓) in Member 1 column or Member 2 column to specify whether the question is solved by Member 1 or Member 2 respectively.
- You may add any comments if you have in the same columns corresponding to every question.

Example to fill up the table :

Question Number	Harry	Ron
1.1	{✓} Comment 1	
1.2		{✓} Comment 2
1.3	{✓} Comment 3	

Table to be filled up:

Question Number	Student 1	Student 2
1.1		
1.2		
1.3		
1.4		
2.1		
2.2		
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8.1		
8.2		
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