Experiment 5 – Design of an Operational Amplifier Using PSpice

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Abstract

The experiment mainly focused on the design process of a functional operational amplifier circuit with certain design specifications. After having integrated the component stages and configured the relevant bias resistors of the circuit, the component constants and design specifications were verified and validated using PSpice simulation. In this process, the Q2N2222 NPN and Q2907 PNP transistor output characteristic were obtained; then, graphs generated from input DC sweep, input transient, input AC sweep simulation were used to either acquire the input offset voltage perfecting the prototype design or verify the design specification; after that, comparison between the original frequency response of the designed amplifier and the compensated design were investigated using the gain and phase Bode plots; finally, the common-mode response was investigated.

Declaration

I confirm that I have read and understood the University's definitions of plagiarism and collusion from the Code of Practice on Assessment. I confirm that I have neither committed plagiarism in the completion of this work nor have I colluded with any other party in the preparation and production of this work. The work presented here is my own and in my own words except where I have clearly indicated and acknowledged that I have quoted or used figures from published or unpublished sources (including the web). I understand the consequences of engaging in plagiarism and collusion as described in the Code of Practice on Assessment (Appendix L).

Table of Contents

1. Introduction

1.1. Background

As one of the most widely used electronic devices, operational (op-amp) amplifier has many merits. Besides its ability to perform high gain voltage operation over the differential input and return with the single-ended output (Figure 1.1.1), an op-amp is well capable of operating nearly independent of the variation in temperature and manufacture process with the external components setting the negative feedback. Thus, with these qualities, they are broadly used for commercial, industrial and scientific purposes [1].

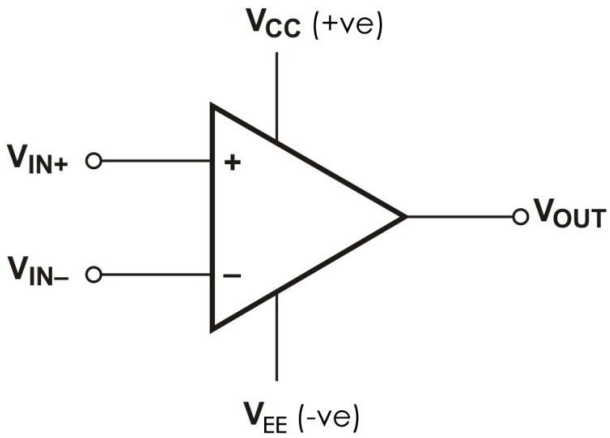


Figure 1.1.1 Op-amp Symbol

1.2. Objective

There are two main purposes of the experiment:

- be familiar with the concepts of different building blocks constructing an op-amp: the emitter follower, the common emitter amplifier, the current mirror circuit, and the differential input stage (long-tailed pair).
- design a functional op-amp with the aid of PSpice simulation with following specifications:
    a) Differential input impedance greater than 100 kΩ.
    b) Voltage gain (that is, 'open loop gain') greater than 500,000.
    c) Output impedance less than 1kΩ.
    d) Output voltage to be approximately zero volts for zero input.
    e) Frequency response down to DC (0 Hz).
    f) Supply voltage +9 to -9 volts.
    g) Total current consumption not greater than 5 mA.

1.3. Theory

The op-amp is composed of four building block circuits (as shown in Figure 1.3.1) :

a) An emitter follower
b) A common emitter amplifier
c) A current mirror circuit

d) A differential stage (long-tailed pair)

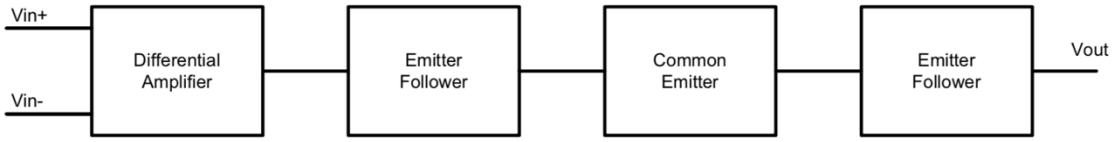


Figure 1.3.1. 4-stage block diagram of the op-amp

As shown in the following Figure 1.3.2.:

- Stage 1 sets the DC bias for all stages (Current Mirror).
- Stage 2 and 4 provides high voltage gain (Differential Amplifier and Common Emitter).
- Stage 3 match the gain stages to avoid loading effects (Emitter Follower).
- Stage 5 provide low output resistance (Emitter Follower).

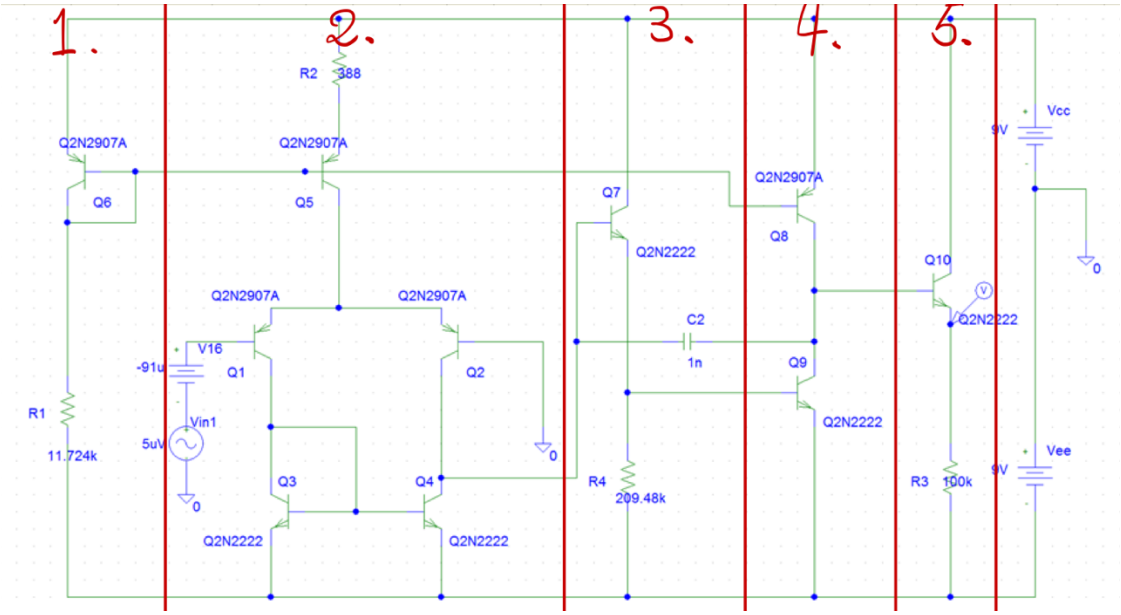


Figure 1.3.2. Schematic of the op-amp divided into 5 stages

2. Material List

2.1. Experiment 5 Lab Script

2.2. PSpice

3. Procedures and Results

3.1. Part I: Transistor Output Characteristics

3.1.1. NPN Transistor (Q2N2222)

3.1.1.1. Task1: Circuit Schematic

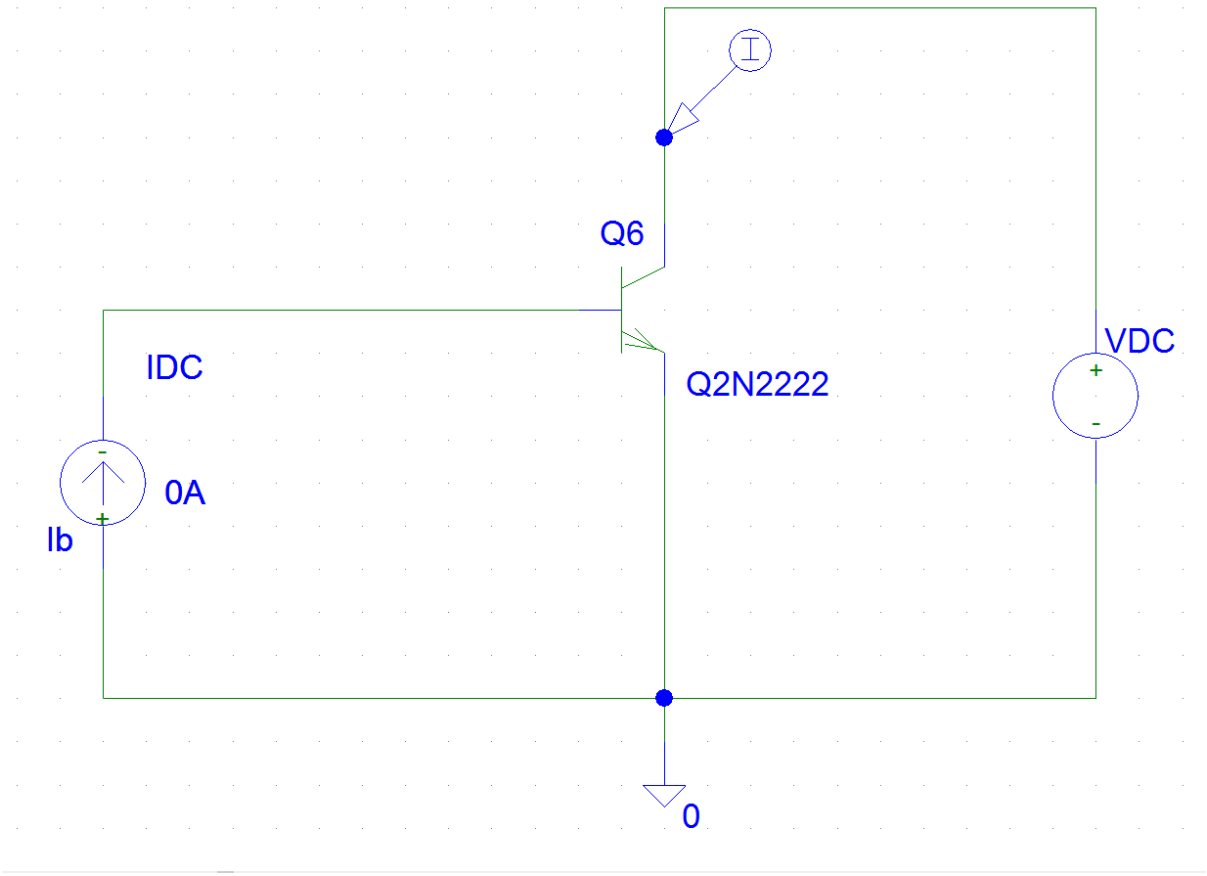


Figure 3.1.1.1. NPN transistor output characteristics schematic

3.1.1.2. Task2-4: V_{CE}-I_C plot for given I_B (0, 4, 8 … 40 µA), V_{CE} swept from 0 to 20 V

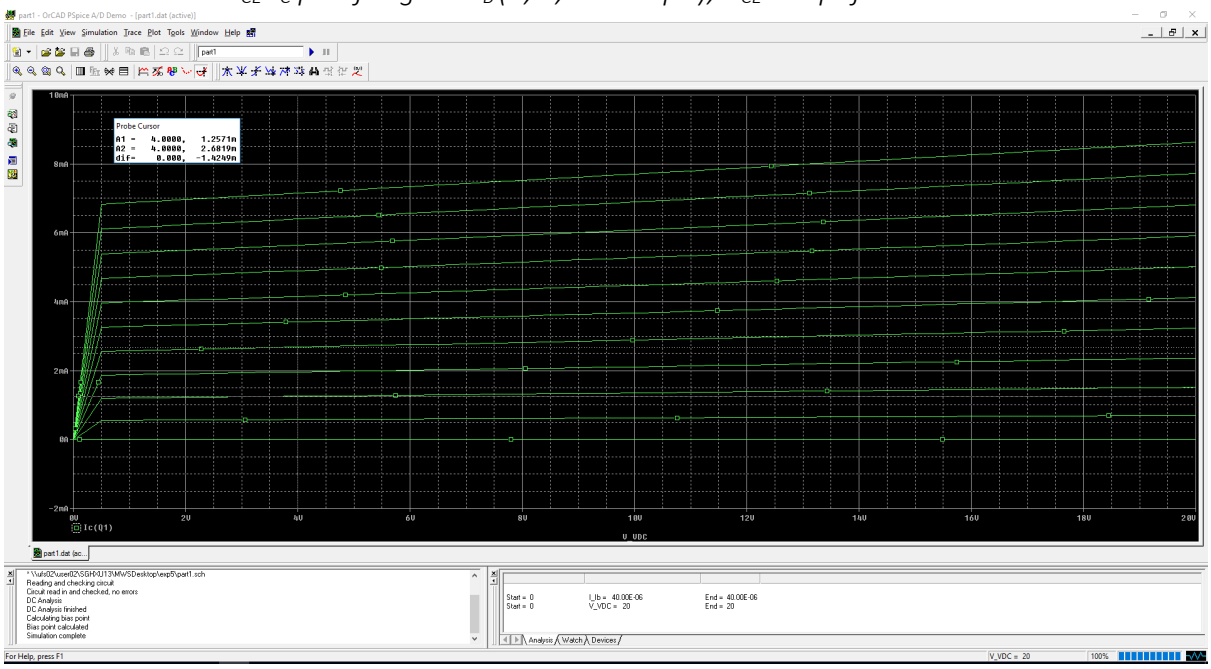


Figure 3.1.1.1. NPN transistor V_{CE}-I_C plot

Since $\beta = \frac{I_C}{I_B}$ and $\beta_0 = \frac{i_C}{i_B}$, using the data obtained by the probe cursor shown in Figure 3.1.1.1.

We have the DC current gain $\beta(npn) = \frac{I_C}{I_B} \approx 166.6$,

and the AC current gain $\beta_0(npn) = \frac{i_C}{i_B} \approx 178.1$

3.1.2. PNP Transistor (Q2N2907)

3.1.2.1 Task1: Circuit Schematic

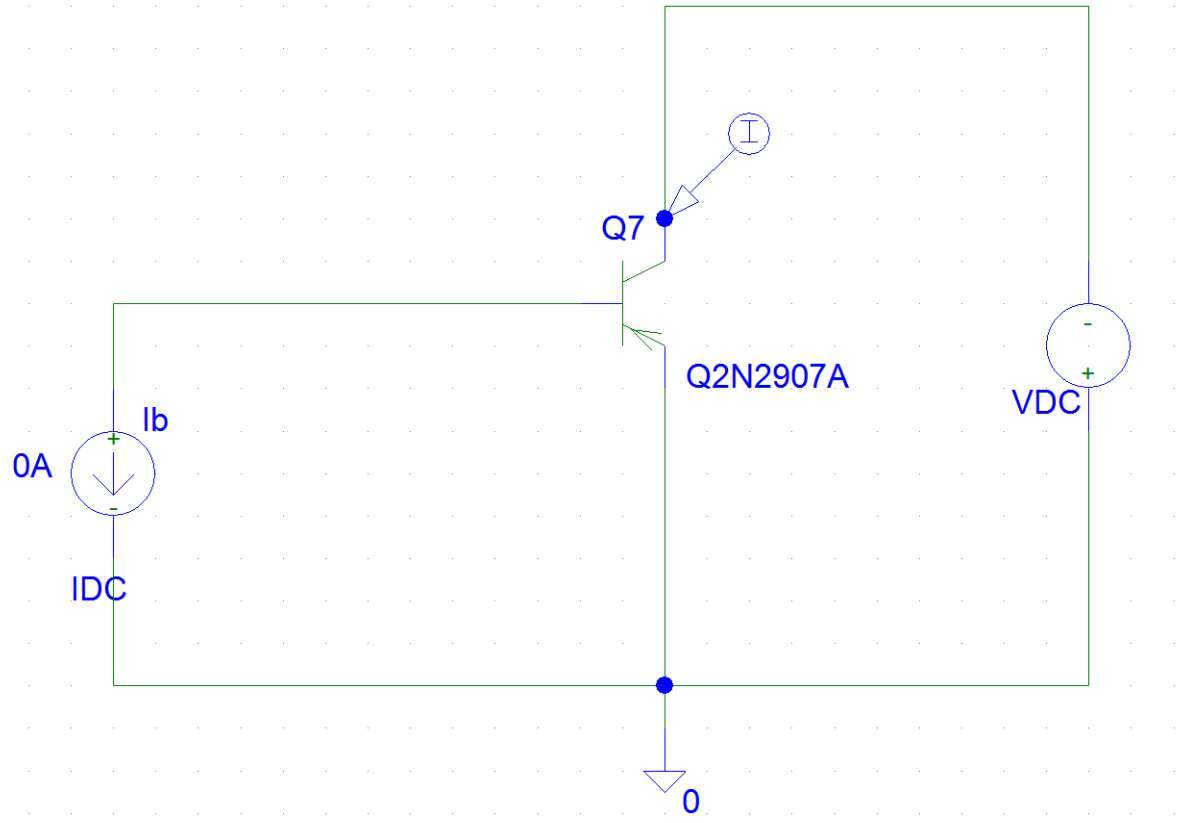


Figure 3.1.2.1. PNP transistor output characteristics schematic

3.1.2.2 Task2-4: V_{CE}-I_C plot for given I_B (0, 4, 8 … 40 μA), V_{CE} swept from 0 to 20 V

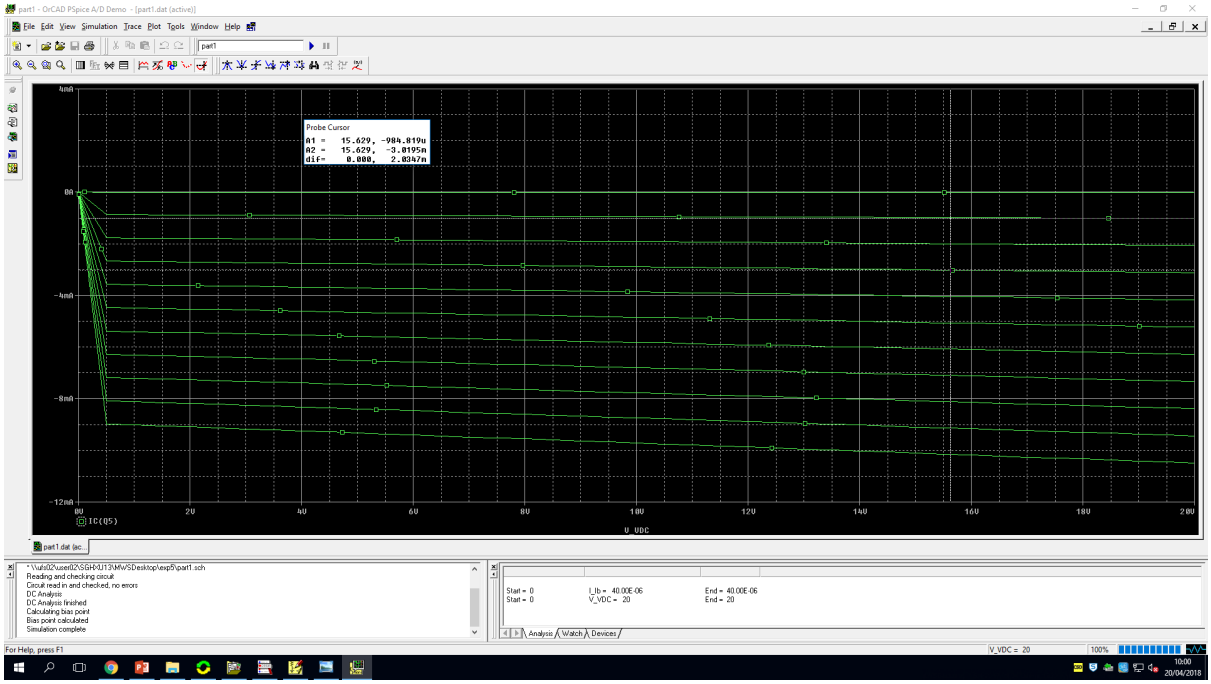


Figure 3.1.2.2. PNP transistor V_{CE}-I_C plot

Since $\beta = \frac{I_C}{I_B}$ and $\beta_0 = \frac{i_C}{i_B}$, using the data obtained by the probe cursor shown in Figure 3.1.2.2.

We have the DC current gain $\beta(pnp) = \frac{I_C}{I_B} \approx 195.4$,

and the AC current gain $\beta_0(pnp) = \frac{i_C}{i_B} \approx 254.3$

3.2. Part II: Achieving the specification of the operational amplifier

3.2.1. Task1: Complete op-amp schematic

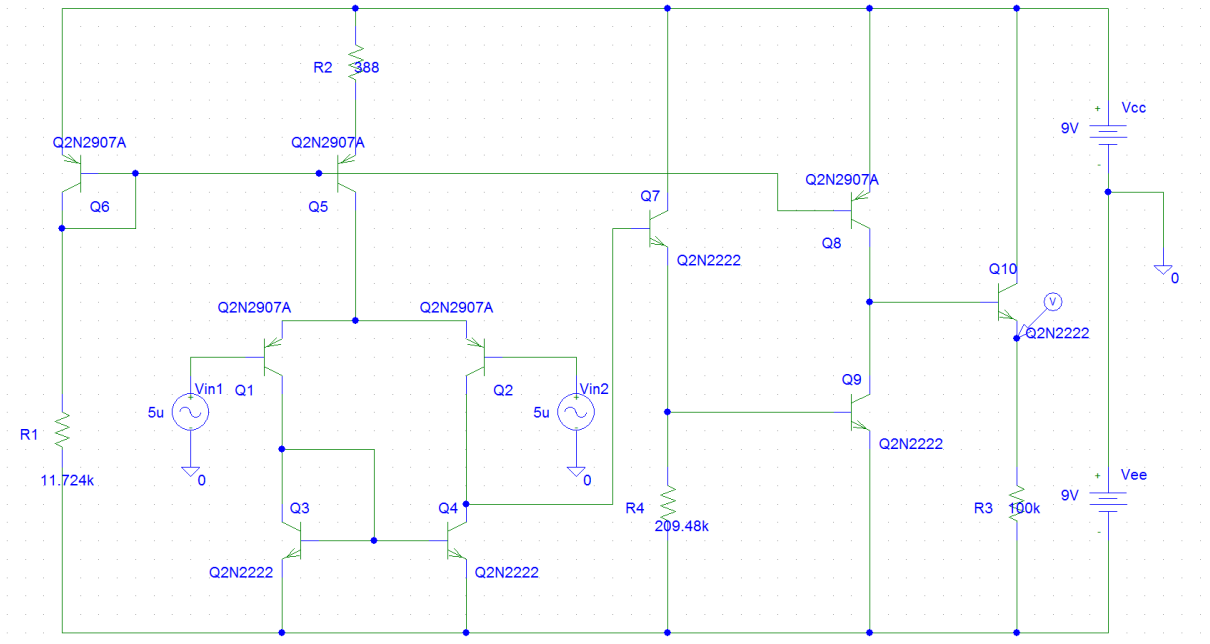


Figure 3.2.1. Complete op-amp schematic

As stipulated by the design specification, the differential input impedance should be no less than 100kΩ, so let the input impedance to be 171.36kΩ for convenience,

that is $R_{id} = 171.36k\Omega$.

Adverting to the small signal model of the differential amplifier, it can be obtained that $R_{id} = 2r_{be}$ and since $r_{be} = \frac{\beta}{I_C}$, we have:

$$R_{id} = 2r_{be} = \frac{2 * \beta_o(pnp)}{40 * I_{C1}} = 171.36\,k\Omega$$

Meanwhile, since Q3 and Q4 sets up a current mirror, yielding $I_{C1} \approx I_{C3} = I_{C4} \approx I_{C2,}$ thus we have $IC1 = 1/2*I_{C5,}$ which gives:

$$R_{id} = 2r_{be} = \frac{2 * \beta_o(pnp)}{40 * 0.5 * I_{C5}} = \frac{\beta_o(pnp)}{10 * I_{C5}} = 171.36k\Omega$$

$$\text{Thus, } I_{C5}(I_o) = \frac{\beta_o(pnp)}{10*R_{id}} = \frac{254.3}{10*171.36k} = 1.484*10^{-4}\,A$$

- **R_1**

Set $I_{C6}(I_{ref}) = 10\ I_O = 1.484*10^{-3}$ A, with $V_{be6} = 0.6V$, we can then write:

$$R_1 = R_{ref} = \frac{V_{EE}+V_{CC}-V_{be}}{I_O} = \frac{9+9-0.6}{1.484*10^{(-3)}} = 11.724k\Omega$$

- **R_2**

Since Q5 and Q6 forms an Widlar current mirror, we get $R_E I_O = V_T \ln(\frac{I_{ref}}{I_O})$,

$$\text{thus, } R_2 = R_E = \frac{V_T}{I_O}\ln(10) = \frac{0.025}{1.484*10^{(-4)}}\ln(10) = 388\Omega$$

- **R_3**

Referring to the small signal model of the emitter follower, we have:

$$R_{CC} = R_{out} = \frac{r_{be}+R_S}{1+\beta_o} /\!/\ R_E = \frac{r_{be10}+R_S}{1+\beta_o(npn)} /\!/\ R_{3,}$$

$$\text{since } \frac{r_{be,(Q_{10})}+(r_{be,(Q_8)} /\!/ r_{be,(Q_9)})}{\beta_{0,NPN}+1} \text{ is already less than } 1k\Omega,$$

Thus, R3 cane be directly chosen to be 100 kΩ with intuition.

- **R_4**

The output resistance of the differential amplifier stage is given by:

$$R_O^{DA} = r_{ce,Q_2} /\!/ r_{ce,Q_4}$$

Adverting to the small signal model of the emitter follower, we have:

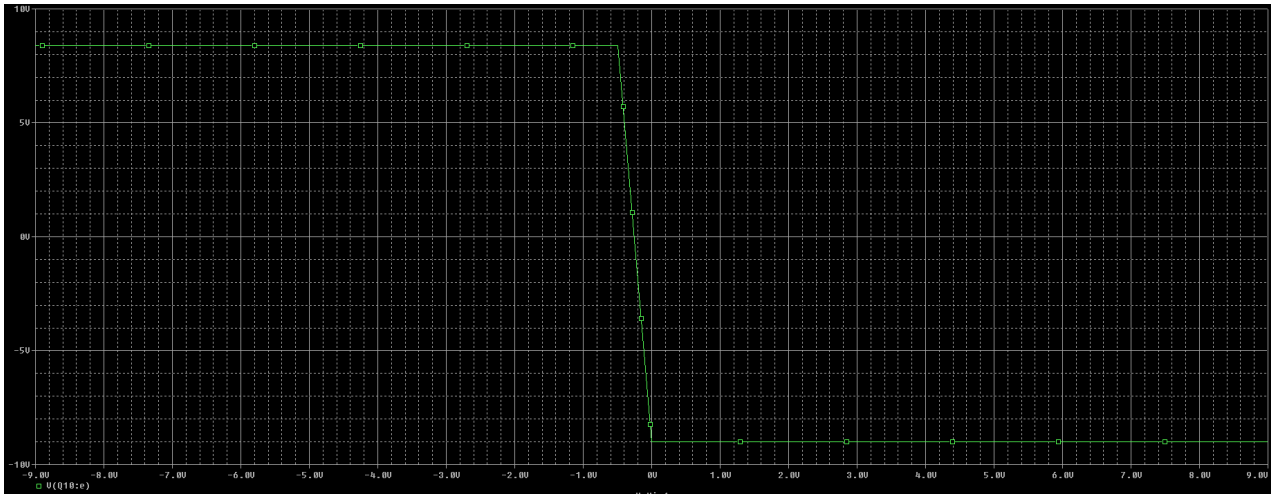
$$R_i(CC) = r_{be}(CC) + (1 + \beta_o)R_E \,//\, R_{L,}$$

which can be written as: $R_i(CC) = r_{be}(CC) + (1 + \beta_o)\beta_o \frac{R_E r_{be}(CE)}{R_E + r_{be}(CE)}$

solving the quadratic equation, we have R_4= 209.475 kΩ

To sum up, with the ideal differential input impedance of 171.36kΩ, the bias resistors should be R_1=11.724kΩ R_2=388Ω R_3=100KΩ R_4=209.475 kΩ to meet the design specification.

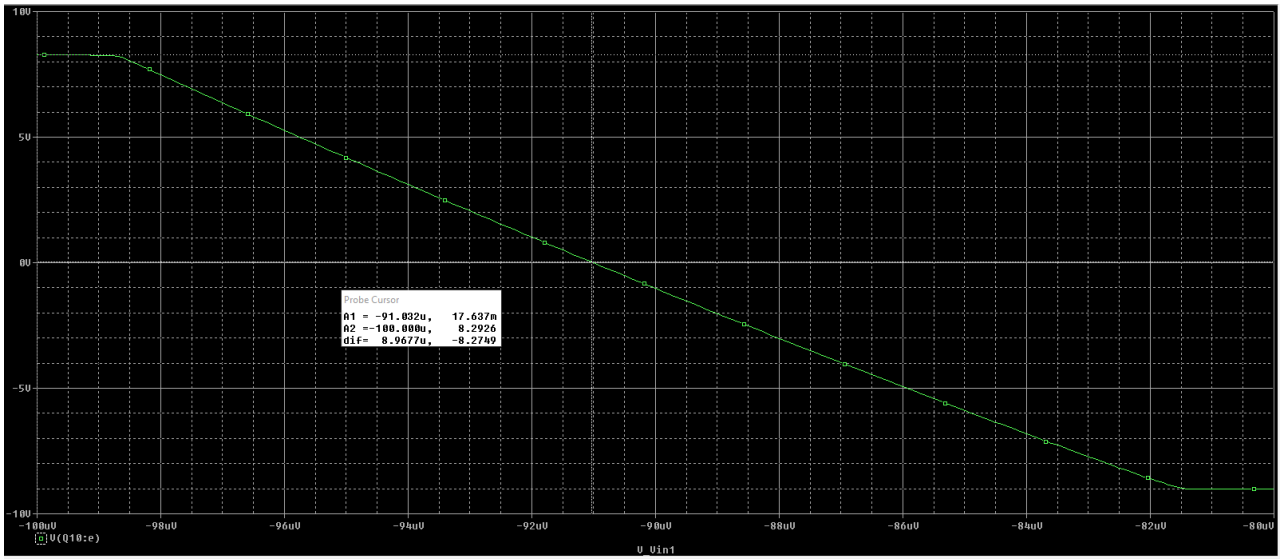
3.2.2. Task2: Transfer characteristics of the op-amp (DC sweeping from -9V to +9V on



input)

Figure 3.2.2.1 Transfer characteristics of the op-amp

As shown in Figure 3.2.2.1, the plot of the op-amp's transfer characteristic swept from -9V and 9V was insufficient for the identification of the useful operating range. Thus,



the sweep range was narrowed as below.

Figure 3.2.2.2 Useful range of the op-amp's transfer characteristics

It can be determined from Figure 3.2.2.2, after narrowing the sweep range to between -100μV and -80μV, the accurate useful range is approximately from -98μV to -82μV, which is the useful range for the calculation of the open-loop gain.

3.2.3. Task3: Open loop gain (A_{ol}) of the op-amp

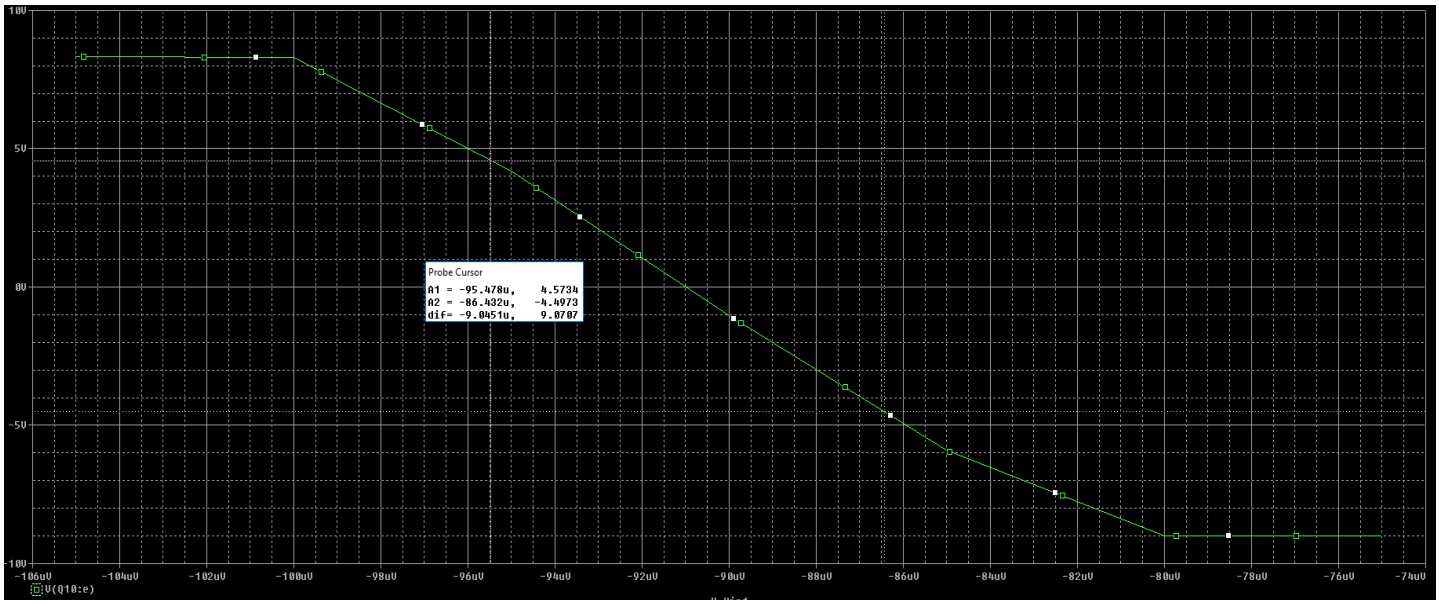


Figure 3.2.3.1 Open loop gain of the op-amp

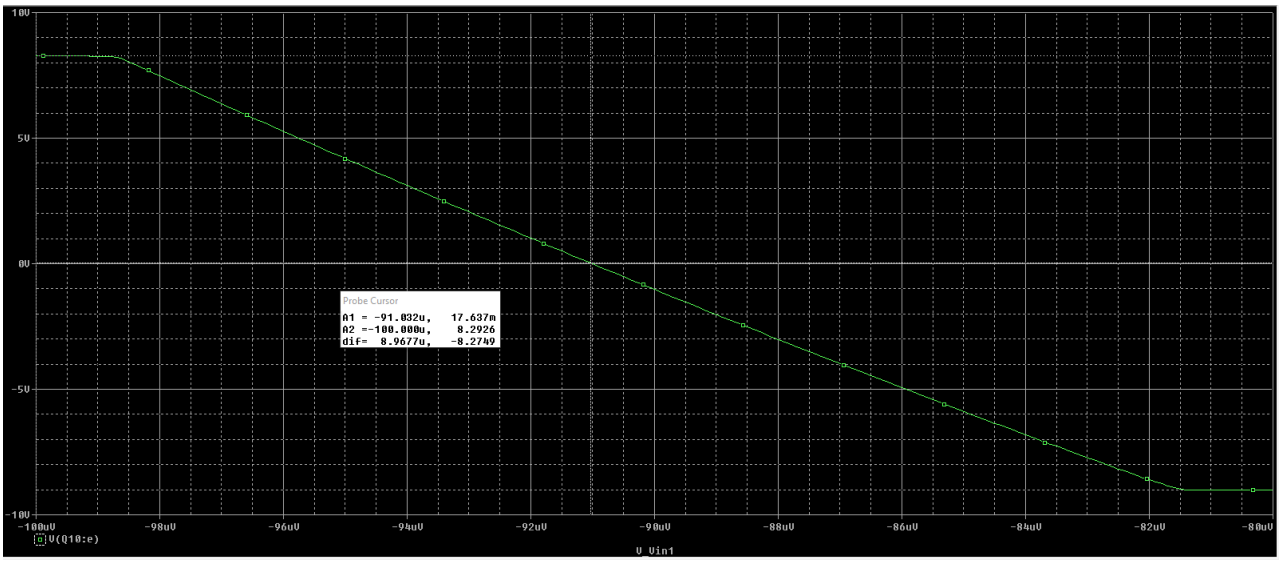
As labelled in Figure 3.2.3.1, the two sampling point on the useful range of the transfer characteristics are:

A_1(-95.478μV, 4.5734V) and A_2(-86.432μV, -4.4973V)

Thus, the open-loop gain is:

$$A_{ol} = \left|\frac{A_{1y} - A_{2y}}{A_{1x} - A_{2x}}\right| = \left|\frac{dif_y}{dif_x}\right| = \frac{9.0707}{-9.0451\mu} = 1.003 * 10^6 > 500{,}000$$

Therefore, the designed voltage gain is $1.003 * 10^6$, which is much greater than the prescribed voltage gain, thus satisfying the design specification.



3.2.4. Task4: Determination of the required DC voltage offset

Figure 3.2.4.1 DC voltage offset

Referring to Figure 3.2.4.1, as can be deduced from the plot of the useful range of the op-amp's transfer characteristics, the centre of the useful transfer characteristic located approximately at point (-91µV,17.6mV). Accordingly, the input DC offset should be 91µV to centre the output close to zero.

3.2.5. Task5: Input/output waveforms from the transient simulation

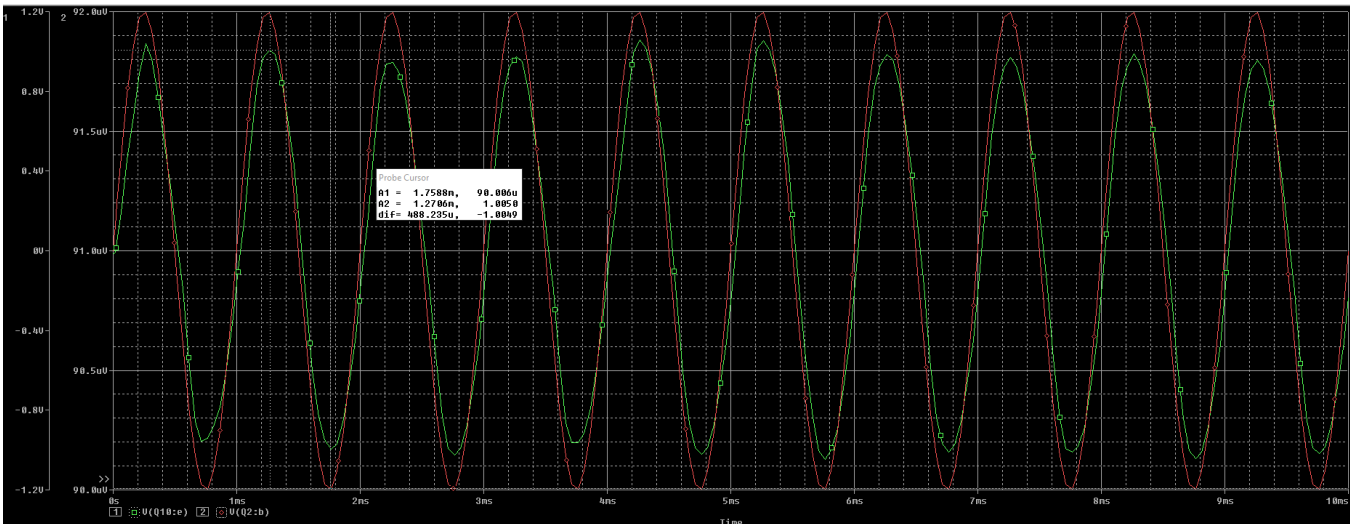


Figure 3.2.5.1 Input/output waveforms with input amplitude set to 1µV

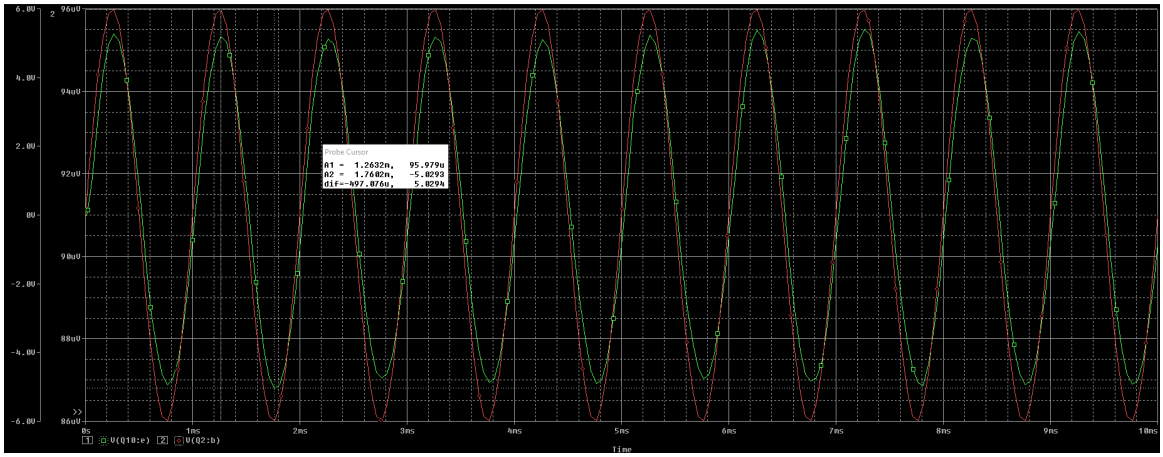


Figure 3.2.5.2 Input/output waveforms with input amplitude set to 5μV

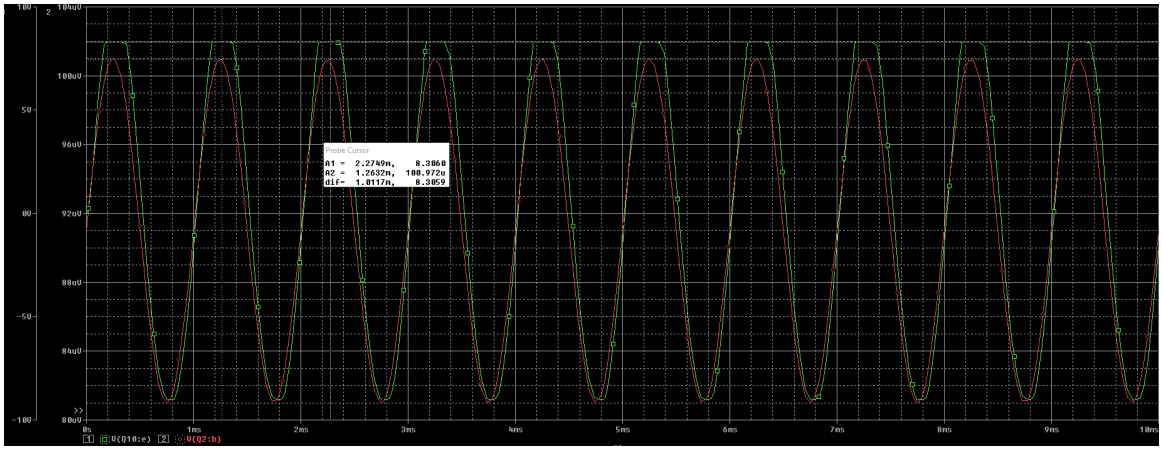


Figure 3.2.5.1 Input/output waveforms with input amplitude set to 10μV

As shown in Figure 3.2.5.1, 3.2.5.2, 3.2.5.3, the input waveform amplitudes were chosen to be 1μV, 5μV, 10μV to give a rough estimation of the useful range without output distortion. The 3 plots give that the input amplitude should be less than 10μV for the op-amp to operate within useful range.

Amplitude of input(μV)	$V_{max}(V)$	$V_{min}(V)$	Voltage gain(M)
1	0.9998	-1.0387	1.0193
2	1.9569	-1.9171	0.9685
3	3.0307	-2.8934	0.9874
4	4.1848	-4.0219	1.0258
5	5.3300	-4.8255	1.0156
6	6.1611	-5.7677	0.9941
7	7.4415	-6.8011	1.0173
8	8.2510	-7.5505	0.9876
9	8.2881	-8.3380	0.9237
10	8.3048	-9.0094	0.8657

Table 3.3.5.1. Input/output waveforms' amplitude parameter with corresponding voltage gain

The voltage gain of the op-amp was calculated using the equation below:

$$A_V = \frac{V_{\max\,(out)} - V_{\min\,(out)}}{2 * V_{IN}}$$

As demonstrated by the statistics in Table 3.3.5.1., the voltage gain is around 990,000 > 500,000 with the input amplitude no larger than 8μV. However, when the input signal amplitude is larger than 8μV, distortion will occur since the top of the output signal will be clipped off.

Generally, the design specification on the voltage gain is met with a rough voltage gain around 990,000 which is much greater than the specified gain of 500,000 with input amplitude smaller than 8μV.

3.3.6. Task6: Input and output impedance of the op-amp circuit

As shown below in Figure 3.3.6.1, the green line denotes the input impedance and the red line denotes average of input impedance in response to different frequency of input.

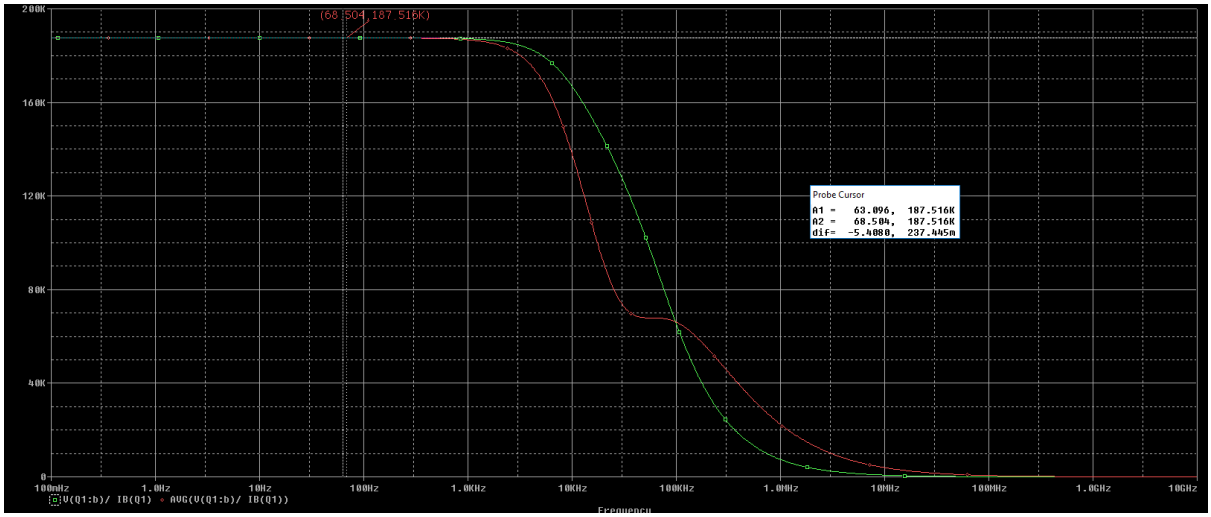


Figure 3.3.6.1. Input impedance of the op-amp circuit

It can be concluded from Figure 3.3.6.1. that when the input signal frequency is between 0 and 1kHz, the input impedance remains almost a constant, 187.516kΩ, which is within 10% deviation from the assumed differential input impedance, 171.36kΩ. The input impedance then drops quickly with the frequency of the input signal going up. Obviously, 171.36kΩ of input impedance satisfy the specification on 'no less than 100kΩ differential input impedance'.

Below is the schematic for measuring output impedance of the op-amp, with the input signal suppressed to zero and an AC signal applied to the output terminal.

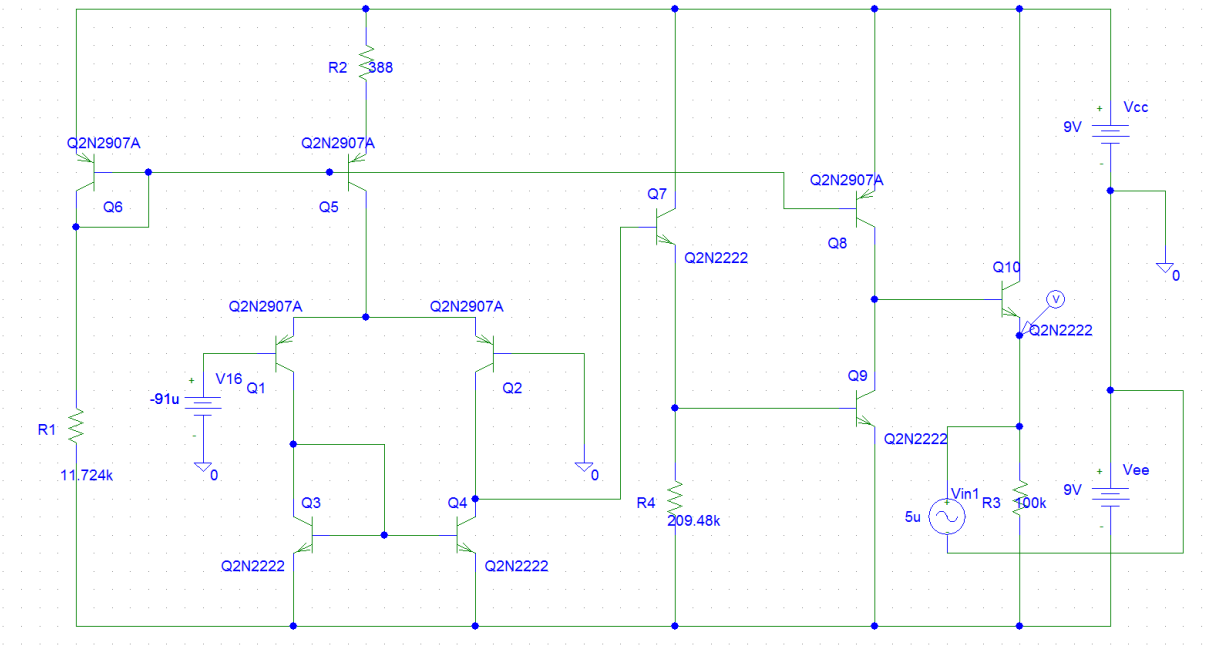


Figure 3.3.6.2 Schematic for measuring the output impedance

Here is the plot of the output impedance (the green trace) and the value of the average output impedance (the red line):

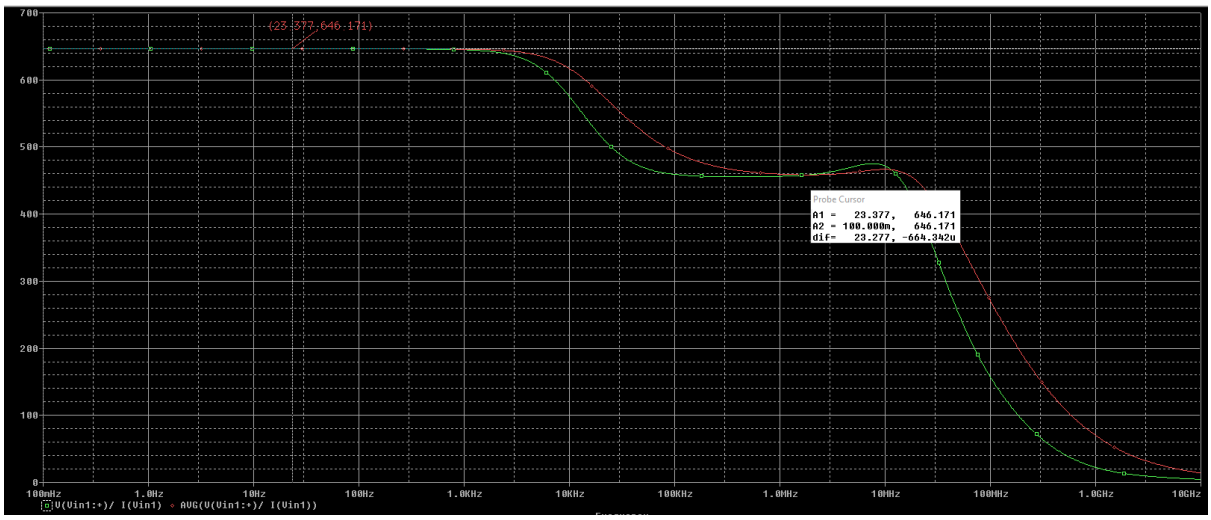


Figure 3.3.6.1 Input impedance of the op-amp circuit

As labelled by the probe cursor in Figure 3.3.6.1, the output impedance is stable when the output signal frequency is between 0 and 1kHz, approximately, 646.171Ω. The input impedance then drops quickly with increasing frequency of the input signal. It is verified by simulation that the designed output impedance complies with the 1kΩ output impedance specification.

To summary the simulated input impedance is 187.516kΩ and the output impedance is 646.171Ω with useful input frequency range from 0 to 1kHz, verified to satisfy the design specification.

3.2.7. Task7: DC voltage levels and total current consumption

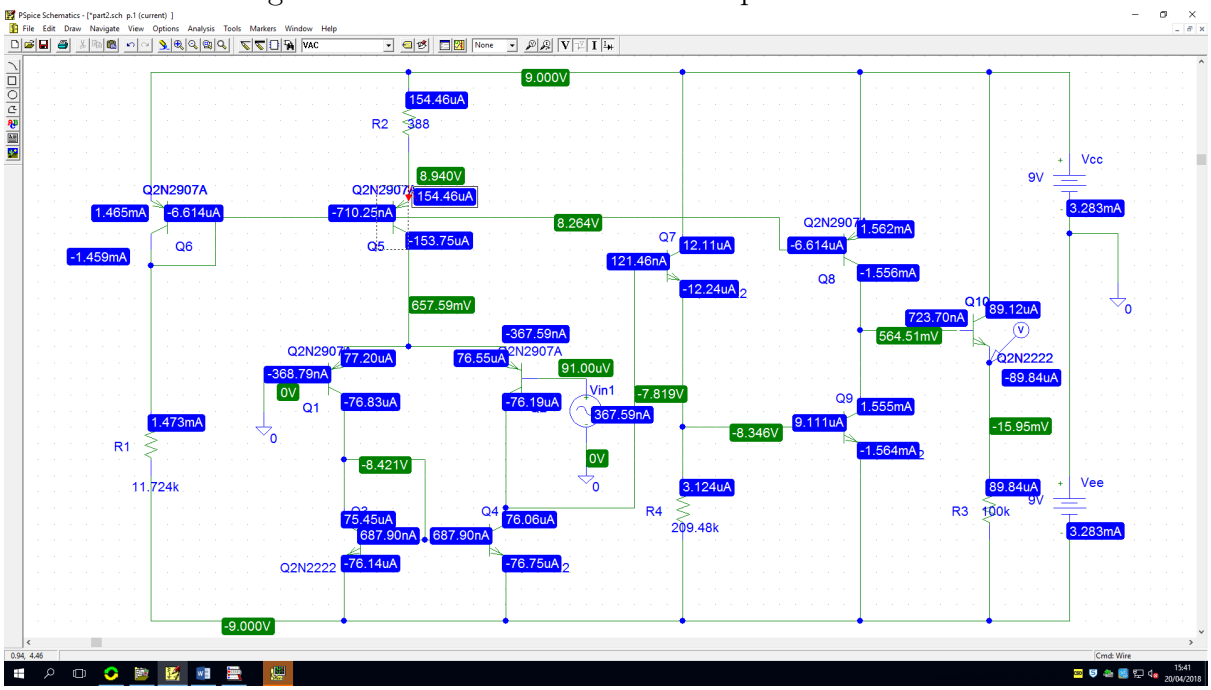


Figure 3.2.7.1. Op-amp schematic labelled by all DC voltage levels and current values

As seen from the labelled schematic, the output voltage is displayed as 89.12μV ≈ 0V, and the total current consumption is determined to be 3.283mA, which less than the specified maximum current consumption of 5mA.

3.3. Part III: Obtaining the frequency response of the designed amplifier

3.3.1. Task1: Frequency response of the op-amp in Bode plots (gain and phase)

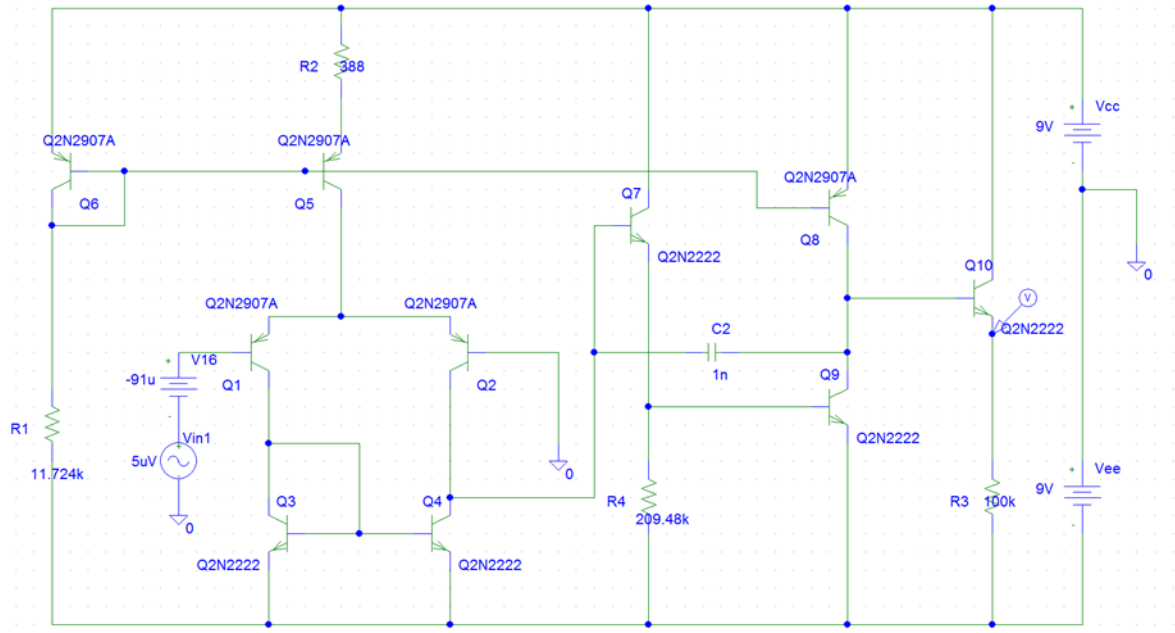


Figure 3.3.1.1 Schematic for obtaining the Bode plots of the op-amp

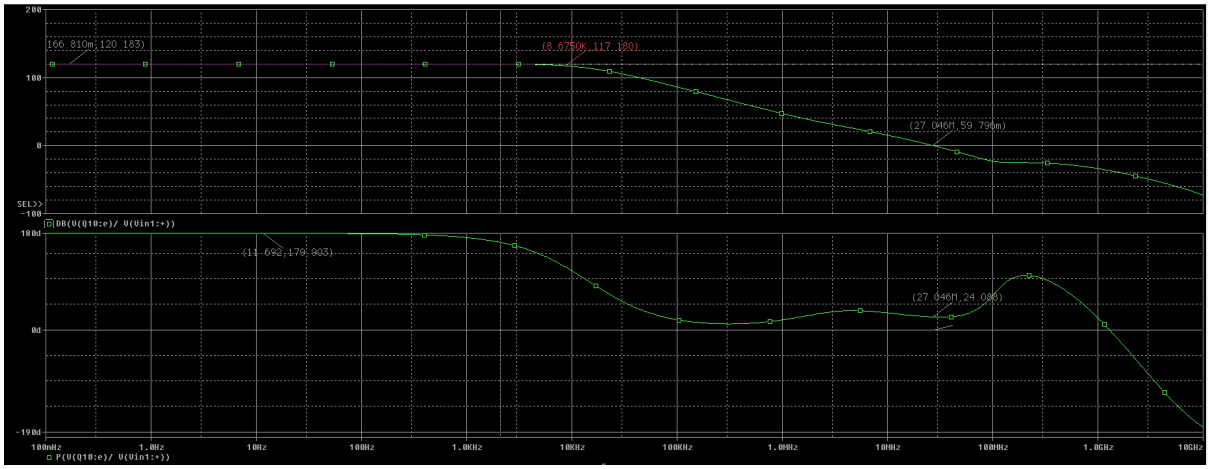


Figure 3.3.1.2 Bode plots (gain and phase of) the designed op-amp

- Bandwidth
  Decibels are calculated using the following formula:
  $$\mathrm{dB} = 20 * log_{10} \frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}} = 20 * log_{10} A_{ol}$$
  In this case, as shown by the label in the plot, the open-loop gain stabilizes around 120.18dB in frequency range from 0Hz to 1kHz.
  By definition, the gain of the upper point which determines the bandwidth of an op-amp is of -3dB, that is 70.7%, of its maximum output voltage gain. In this design case, it is 117.18dB, corresponding to 8.675kHz.
- Phase
  As shown in the lower half of Figure 3.3.1.2, the gain of the open-loop op-amp is relatively stable within the range 0 - 8.675kHz.
  Phase margin is the difference of the between 180 degree and the phase shift at which the voltage gain is 0dB. When the voltage gain is approximate to 0dB at (27.046MHz, 59.769mdB) in the upper gain plot, the corresponding point in the phase plot turns out to be (27.046MHz, 24.088d). Thus, the phase margin is 27.502d.

Thus, the open-loop bandwidth of the designed op-amp is 8.675kHz.

3.3.2. Task2: Frequency response of the op-amp after capacitance compensation

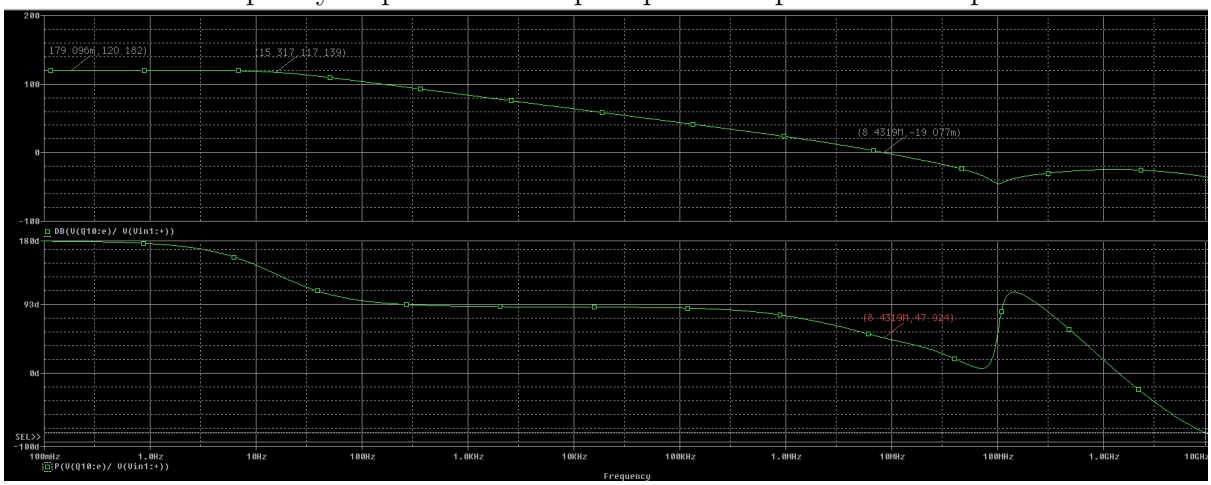


Figure 3.3.2.1 Bode plots (gain and phase of) the designed op-amp after capacitance compensation

- Bandwidth
  Apply the formula from previous section to calculate Decibels.
  In this case, as shown by the label in the Figure 3.3.2.1, the capacitor-compensated gain still stabilizes around 120.18dB, but in frequency range from 0Hz to 10Hz.
  Still by definition, the gain of the upper point which determines the bandwidth of an op-amp is of -3dB, that is 70.7%, of its maximum output voltage gain. In this design case, it is 117.18dB, corresponding to 15.317Hz.
- Phase
  As shown in the lower half of Figure 3.3.1.3, the gain of the capacitor-compensated op-amp is relatively stable within the range 0 - 1Hz.
  When the voltage gain is approximate to 0dB at (8.4319MHz, 47.924mdB) in the upper gain plot, the corresponding point in the phase plot turns out to be (8.4319MHz, 47.924d). Thus, the phase margin is 47.924d.

3.4. Bonus Part: Response to common-mode signal

3.4.1. Common-mode configuration of the op-amp

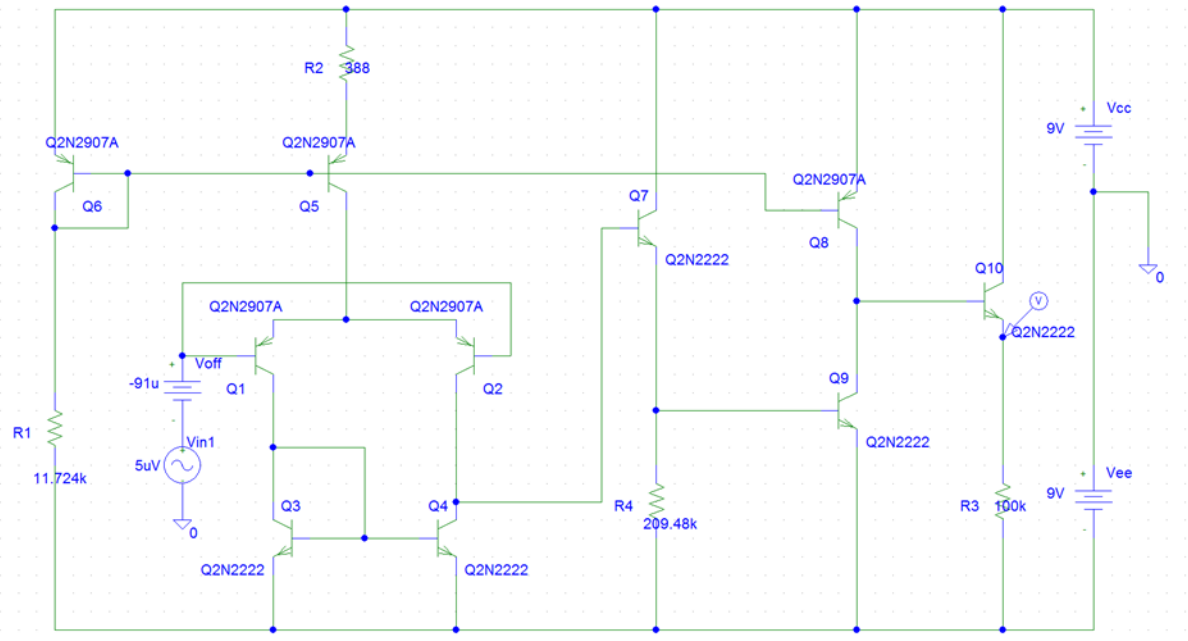


Figure 3.4.1.1. Schematic of the op-amp under common-mode input configuration

3.4.2. Common-mode frequency response of the op-amp

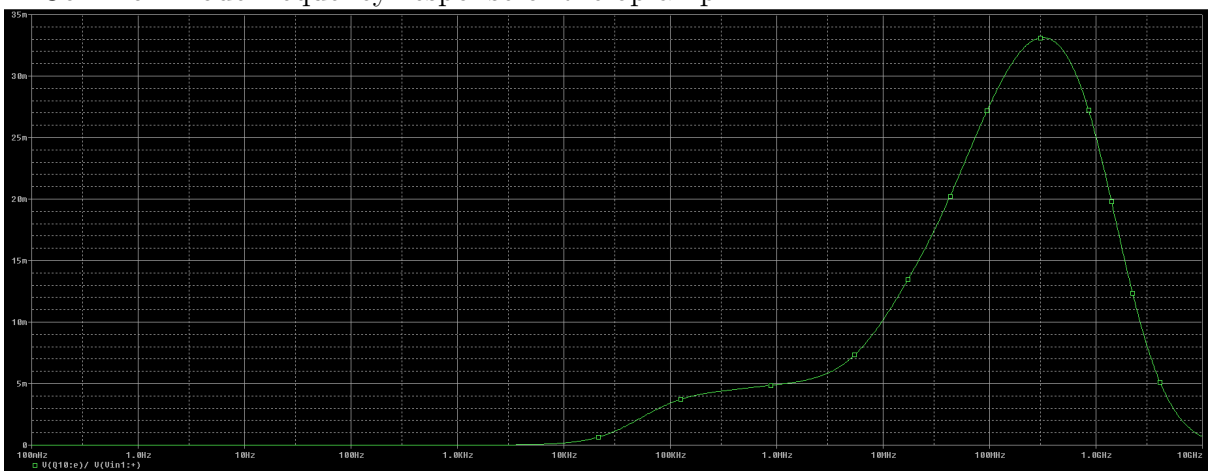


Figure3.4.2.1. Common-mode frequency response of the op-amp

As shown in Figure3.4.2.1., the common-mode gain is determined to be no larger than 0.035, indicating that the common-mode signal will hardly be of any consequence to the output signal.

3.4.3. Common-mode output voltage of the op-amp (Input swept from -9V to 9V)

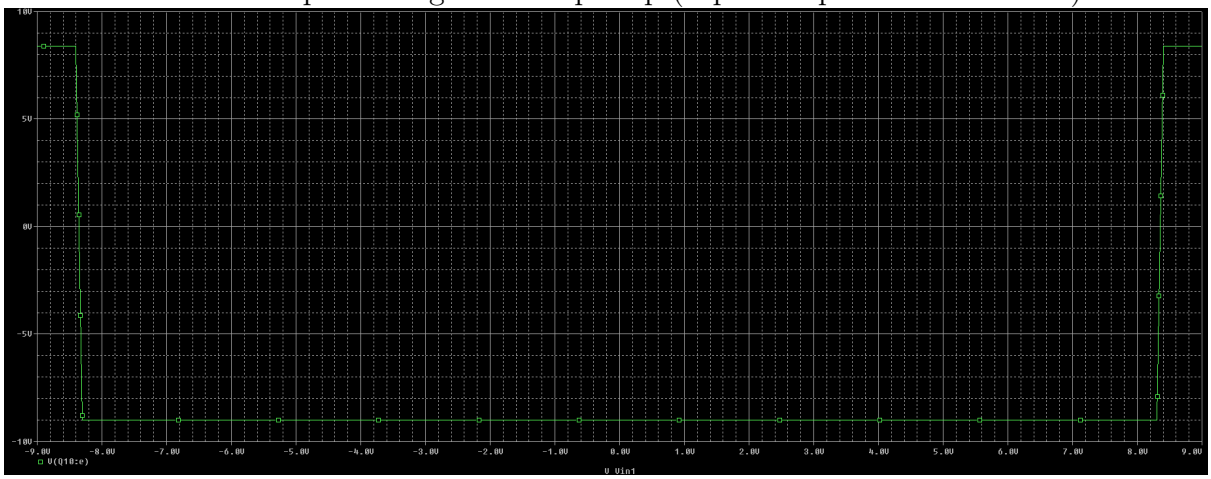


Figure 3.4.3.1. Common-mode output voltage of the op-amp (Input swept from -9V to 9V)

As shown in Figure 3.4.3.1., the output voltage is equal to -9V in operating range, implying that the op-amp is out of function with regard to input common-mode signal.

To sum up the two sections, the designed op-amp is excellent in common-mode rejection.

3.5. Design Specification

Parameter	Specification	Your value	Comment on the value obtained
Differential input impedance	>100kΩ	187.516kΩ	The input impedance remains almost a constant, 187.516kΩ, which is within 10% deviation from the pre-assumed differential input impedance for calculation, 171.36kΩ. The input impedance then drops quickly with the frequency of the input signal going up. Obviously, 171.36kΩ of input impedance satisfy the specification on 'no less than 100kΩ differential input impedance'.
Open loop voltage gain	> 500,000	1.003M	The designed voltage gain is $1.003 * 10^6$, which is much greater than the prescribed

			voltage gain, thus satisfying the design specification.
Output impedance	<1kΩ	646.171Ω	The output impedance is stable when the output signal frequency is between 0 and 1kHz, approximately, 646.171Ω. The input impedance then drops quickly with increasing frequency of the input signal. It is verified by simulation that the designed output impedance complies with the 1kΩ output impedance specification.
DC output voltage	~0V	-15.95mV	As seen from the labelled schematic, the output voltage is displayed as 89.12μV which can be approximate to 0V comparing with normal output voltage magnitude, and thus satisfying the specification of 0V.
DC offset voltage	None given	-91μV	As can be deduced from the plot of the useful range of the op-amp's transfer characteristics, the centre of the useful transfer characteristic located approximately at point (-91μV,17.6mV). Accordingly, the input DC offset should be 91μV to centre the output close to zero.
Frequency response	Down to DC (0 Hz)		By definition, the gain of the upper point which determines the bandwidth of an op-amp is of -3dB, that is 70.7%, of its maximum output voltage gain. In this

			design case, it is 117.18dB, corresponding to 8.675kHz (Also with relatively stable phase response in the useful range).
Total current consumption	<5 mA	3.283 mA	The total current consumption is determined to be 3.283mA, which less than the specified maximum current consumption of 5mA.
Bandwidth with compensation capacitor	None given	15.317Hz	The capacitor-compensated gain still stabilizes around 120.18dB, but in frequency range from 0Hz to 10Hz. Still by definition, the gain of the upper point which determines the bandwidth of an op-amp is of -3dB, that is 70.7%, of its maximum output voltage gain. In this design case, it is 117.18dB, corresponding to 15.317Hz. However, the phase response only stabilizes between 0-1Hz.

4. Discussions

4.1. General questions

a) What can you deduce about the stability of your amplifier from the Bode plots in Part III?

- The designed op-amp, capacitor compensated or not, is observed to be stable when the frequencies of the input signals are in the corresponding ranges of bandwidth. Thus, it is necessary to compare the phase margin of the designed op-amp under these two types of configuration – the original and the capacitor-compensated configuration.
- As can be estimated from the Bode plots of the two configurations from part III, the designed op-amp under capacitor-compensated configuration has a much larger phase margin of 47.924d comparing with the op-amp under the original

configuration which is equal to 24.088d. That is, the op-amp under capacitor compensation is more stable than the original op-amp configuration.

b) What is the purpose of the 'Phase compensating capacitor'?
As can be deduced from comparison of the Bode plots (gain and phase) of the op-amp under different configurations in Part III, the capacitor-compensated op-amp exhibits a limited bandwidth but an increased phase margin, providing more stability without sacrificing the voltage gain.

4.2 Challenges and Solutions

The first major challenge was the calculation of R_3, which is given by a complex formula:

$$R_{OUT} = \frac{r_{be,(Q_{10})} + (r_{be,(Q_8)} // r_{be,(Q_9)})}{\beta_{0,NPN}+1} // R_3$$, while satisfying R_{OUT} less than 1kΩ

However, after reflection the first part of the parallel, $\frac{r_{be,(Q_{10})} + (r_{be,(Q_8)} // r_{be,(Q_9)})}{\beta_{0,NPN}+1}$, turned out to be already less than 1kΩ. Thus, R3 was chosen to be 100kΩ.

5. Conclusions

5.1. Objective accomplishment

The two main aims of the experiment are both met in that:

- familiarity of the knowledge and techniques required in designing a functional op-amp was developed successfully.
- the designed op-amp meets all the required specifications successfully.

5.2. Limitations and Suggestions

Though the design of the op-amp was successful in a general sense, issues still exists in practical implementation of the op-amp. For instance, the resistors used in simulation, such as R_1=11.724kΩ, R_2=388Ω and R_4=209.475 kΩ are not values for standard resistors. The solution to this problem can be as simple as applying the closest value of combination of standard resistors to replace these resistors. Further simulation may be necessary for a rather accurate outcome.

6. References

[1] A.AI.Ataby, "Experiment 5-Design of an Operational Amplifier Using PSpice", Department of Electrical Engineering & Electronics, Feb 2015, Ver 4.

[2] S Hall, Lecture notes-Module ELEC271, 2015.