Modelling Electrical Properties of Thin High-k Gate Stacks (HfSiO, 70% Hf)

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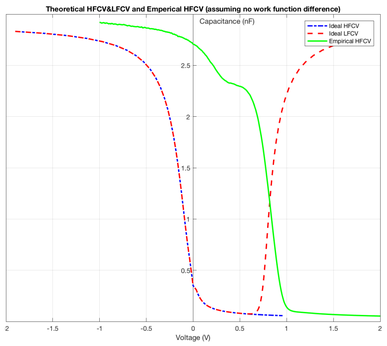
Work Description

In this project, the electrical properties of a specific thin high-k gate stacks (HfSiO, 70% Hf) were analysed and modelled both statistically and visually with MATLAB using empirical CV characteristic data from IMEC. Meanwhile, another control project group were set up to study the electrical properties of thin high-k gate stacks (HfSiO 50% Hf) for comparison.

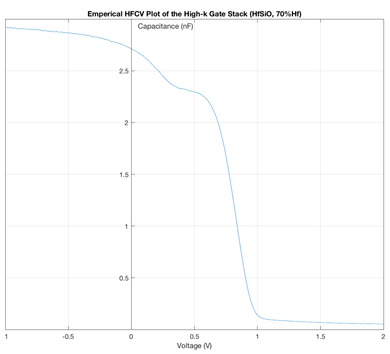
An Intuitive Insights



Au Gate
3.3nm High-k
1.6nm SiOx
Silicon Substrate

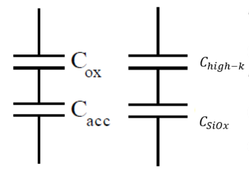
The stack's schematic diagram and ideal/emperical CV plots were drawn to initiate the research with intuition.

Substrate Type



The silicon substrate was determined to be p-type. In the accumulation mode, the holes react quickly to the measuring signal yielding a Cmax. While in the depletion mode, the HF capacitance drops drastically until the inversion region is reached yielding a Cmin, with holes being modualated at the depletion edge.

Oxide Relative Permittivity



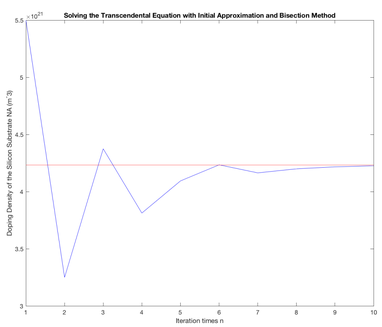
Accumulation Mode AC Equivalent (L) and Oxide Capacitance Equivalent (R)

The combined oxide relative permittivity is 6.80. The high-k relative permittivity is 10.64. The oxide capacitance was approximated to Cmax, which can be obtained from the empirical HFCV plot. Then, the relative permittivity of the two oxides were calculated respectively.

Equivalent Oxide Thickness(EOT)

The EOT of the combined oxide layer is calculated to be 2.81 nm and that of the high-k layer is 1.21 nm. Using Cmax from the previous section, the EOT of the combined oxide layer can be calculated from $\epsilon_0\epsilon_{SiO2}\frac{A}{EOT} = C$ and since the thickness of the oxide layer is given, the EOT of the high-k layer can be directly obtained from $EOT_{ox} - t_{SiO2}$.

Substrate Doping Density

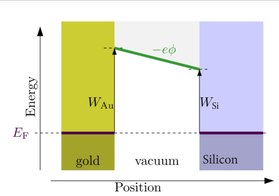


The doping density of the silicon substrate is found to be $4.23*10^{21}$. The determination of the substrate doping density involved solving a transcendental equation:

$$N_A = \frac{4KT}{A^2q^2\epsilon_o\epsilon_s}\left[\frac{1}{C_{min}} - \frac{1}{C_{max}}\right]^{-2} \ln\frac{N_A}{ni}.$$

Approximation and Bisection were used in a visual approach to tackle the problem.

Work Function Difference

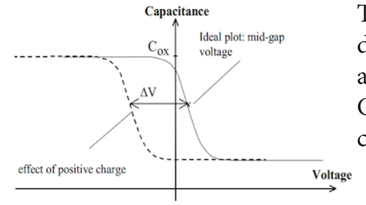


The work function difference between the gold gate and the p-type substrate yielded to be Φ_{AuS} = 0.065 eV, indicating an increase the threshold voltage. That is, in the absence of an applied gate voltage, the semiconductor layer is slightly accumulated.

Flatband & Midgap Voltage

The flatband voltage is calculated to be 0.93V using Debye length, $L_D = \sqrt{\frac{\epsilon_0\epsilon_s V_t}{qN_D}}$. The midgap voltage is 1.36V. A search program was developed to find the midgap capacitance and then calculate the midgap voltage.

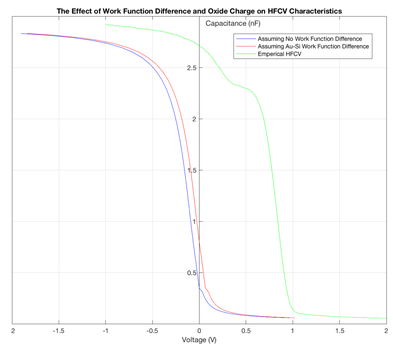
Oxide Charge Density

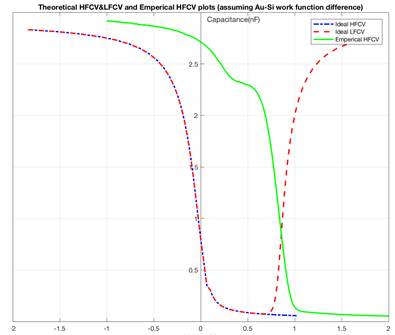


The oxide charges at flat-band condition is $-6.64*10^{12}$ C•cm^{-2}, and that at mid-gap condition is $-6.90*10^{12}$ C•cm^{-2}, corresponding to -157.76 cm^{-2} and -163.96 cm^{-2} respectively.

Comparison & Conclusion

%Hf	Relative Permittivity k	EOT(nm)	Flatband Voltage(V)	Per Unit Area Oxide Charge(C/cm^2)	High-k Layer Thickness(nm)
50	8.6	3.04	0.52	-5.3x10^12	3.2
70	10.6	2.79	0.93	-6.6x10^12	3.3





With plausible reasoning, the comprarison of data in the table above suggest that with the Hf concentration rising, the relative permittivity of the high-k layer will increase and consequently, EOT will decrease. However, it is still unsure whether a *positive* correlation exists between the hafnium concentration and the *negative* oxide charge per unit area since oxide charges are formed for various reasons.

Addionally, the control variable HFCV plot demonstrates oxide charge a potent factor in influencing the HFCV. The ideal HFCV/LFCV are also drawn in contrast to the empirical HFCV, noting the gap between theory and practice, which may need further attention.