Sustainable Development and Ethical Aspects of the Design

Modelling electrical properties of thin high-k gate stacks (HfSiO, 70% Hf)

Description

With Moore's Law setting the pace, the number of transistors in a dense integrated circuit doubles approximately every two years. Most of these achievements are accredited to the miniaturisation of MOS transistor [1]. As the size of the transistor scales down, the thickness of the silicon dioxide gate dielectric decreases with increasing gate capacitance to drive current and thus raising device performance. However, as the oxide thickness scales below 2 nm, the tunnelling effect will cause drastic current leakage rendering the device high-power consuming and unreliable [2]. Nevertheless, the contradiction can be resolved by replacing the silicon dioxide gate dielectric with a high-k material rendering increased capacitance while preventing the tunnelling effects. Thus, a thorough research of the design is needed for industrial implementation.

In this project, the electrical properties of a specific thin high-k gate stacks (HfSiO, 70% Hf) were analysed and modelled both statistically and visually using MATLAB with empirical data from IMEC. Meanwhile, another control project group were set up to study the electrical properties of thin high-k gate stacks (HfSiO 50% Hf) for comparison.

Regulatory Considerations

Though most of the project work is done through computer-based analysis and modelling of secondary data from IMEC, the successful determination of the high-k gate stacks' electrical properties may well lead to large-scale application of these novel stacks on semiconductor chips in place of traditional gate stacks, which may raise considerable regulatory concern.

One obvious regulatory concern is the Restrictions of Hazardous Substances Regulations (RoHS) which restricts the use of ten hazardous substances including lead, mercury, cadmium, hexavalent chromium, 2 fire retardants and 4 phthalates [3]. Directly, the application of the innovative technology will not introduce any of these hazardous substances into the semiconductor chips and would thus be in compliance with RoHS, providing that the original design complies with the restriction.

Another regulation which should be noted is the Waste Electrical and Electronic Equipment Regulations (WEEE) which help the collection, recycling and recovery of electrical and electronic equipment (EEE) product in representation of the producer [4]. By the principles to access and classify EEE as B2C/B2B, since the high-k gate stack is meant to be a subcomponent of a semiconductor chip which will also later be integrated with other components to produce functional devices (Category 3, Term 3) and be only supplied through distribution channels available to non-household users (Step3), the chip integrating the gate stack should be classified as B2B EEE/WEEE. Thus, to ensure the conformity with the WEEE regulation, if less than 5 tones of semiconductor chips incorporating high-k gate stacks are delivered to UK market, the producer should register direct with your environmental regulator as a small producer and identify the product as B2B EEE/WEEE; otherwise, if 5 tones of the innovative chips or more are placed on UK market, the producer must join a producer compliance scheme (PCS) to avoid offence and potential enforcement.

SD/Ethical Implications of large scale manufacture and sale

As illustrated in the description, the high-k gate stacks are designed to be an advanced alternative subcomponent of a semiconductor chip which will be further integrated by other manufacturers to produce functional devices. This indicates that the chip manufactured with the specific technology as a B2B product will have no immediate sustainability or ethical influences in large scale sale and adoption.

However, in a broader sense of sustainability, one obvious new concern does arise during the manufacture and disposal phase of these unconventional chips. These chips adopting the high-k gate stack technology would inevitably contain *hafnium oxide*, which is toxic to human bodies when overexposed to. Over chronic exposure, hafnium oxide can induce liver damage and pneumoconiosis [5]. Thus, health and security concerns should be considered specifically and separately with regard to the newly introduced hafnium oxide layer.

SD/Ethical Implications of follow-on products/markets

In prior analysis and modelling of the thin high-k gate stacks, the novel gate dielectric material has demonstrated excellence in desired electrical properties which can be applied to design advanced MOS transistors. This new design approach will hopefully resolve the contradiction between increasing MOS capacitance and avoiding the leakage current, keeping the Moore's Law holding true for the coming decades and allowing faster processors to be made. However, several problems remain unresolved in manufacturing these devices with desired precision. The impact of surface cleanness and surface conditioning before high-k disposition and varying post annealing parameters on the electrical properties of the gate stack should be studied to better comprehend and control the manufacturing process. Interactive effects within the gate stack process modules and the subsequent integrated circuit fabrication process should also be analysed and modelled to achieve desired IC performance characteristics to produce chips living up to industrial standards [6]. Thus, additional funding is expected for further research project to commercialize the design.

References:

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