Year 2 Project

Modelling electrical properties of thin high-k gate stacks (HfSiO, 70% Hf)

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Abstract

This project aims to develop analytical techniques to model the electrical properties of thin high-k gate stacks through intensive investigation of the specific high-k gate stack's (HfSiO (70%Hf)/SiO_2/Si) surface field effect.

With the aid of MATLAB, the gate stack's empirical specification and high-frequency current-voltage (HFCV) characteristic data were processed and/or visualized. Key device constants such as the substrate's type and doping density, oxide layer's relative permittivity and equivalent thickness, and the gate's work function difference and mode-transition voltage were calculated or identified. Then, non-ideal factors were taken into account and the bias dependent oxide charge densities were calculated at both the flatband and the midgap condition. Finally, having analysed all the desired device properties, meaningful interpretations were drawn through comparisons with the control group (50% Hf) and an ideal HFCV plot was modelled and drawn by using MATLAB. The comparison of the results with the control group also indicates a strong positive correlation between the Hafnium concentration and the oxide relative permittivity and the number of negative oxide charges per unit area, which can be exploited to further understand the behaviour of Hafnium-based high-k gate stacks.

Declaration

I confirm that I have read and understood the University's definitions of plagiarism and collusion from the Code of Practice on Assessment. I confirm that I have neither committed plagiarism in the completion of this work nor have I colluded with any other party in the preparation and production of this work. The work presented here is my own and in my own words except where I have clearly indicated and acknowledged that I have quoted or used figures from published or unpublished sources (including the web). I understand the consequences of engaging in plagiarism

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Chapter 1

Introduction

1.1 Background and Motivation

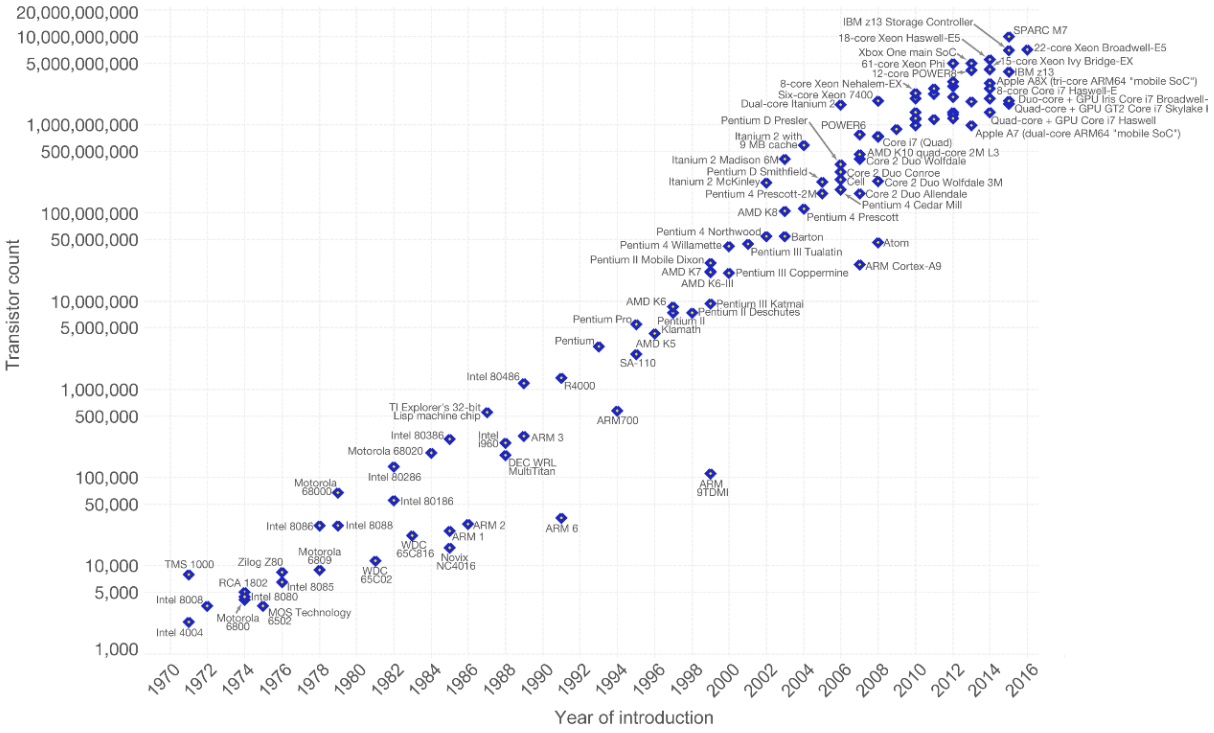

Fig. 1.1.1. Moore's Law- The number of transistors on integrated circuit chips. (1971-2016) [1].

With Moore's Law setting the pace(shown in figure 1.1.1), the number of transistors in a dense integrated circuit doubles approximately every two years. Most of these achievements are accredited to the miniaturization of MOS transistor and capacitor [1]. As the size of the transistor scales down, the thickness of the silicon dioxide gate dielectric decreases with increasing gate capacitance to drive current and thus raising device performance. However, as the oxide thickness scales below 2 nm, the quantum tunnelling effect will cause drastic current leakage, rendering the device high-power consuming and unreliable [2]. Nevertheless, the contradiction can be resolved by

replacing the silicon dioxide gate dielectric with high-k material with increased capacitance while preventing the tunnelling effects. Thus, a thorough research of the design is needed for industrial implementation.

1.2 Objectives

In this project, the electrical properties of a specific thin high-k gate stacks (HfSiO, 70% Hf) were analysed and modelled both statistically and visually using MATLAB with empirical data from IMEC. Meanwhile, another control project group were set up to study the electrical properties of thin high-k gate stacks (HfSiO 50% Hf) for comparison.

Chapter 2

Material List

Group2-HFCV_70%Hf.txt

MATLAB 2017a

Chapter 3

Procedures and Results

3.1 Substrate Type

To determine the type of the semiconductor substrate, empirical high-frequency capacitance voltage characteristics data were plotted using MATLAB as below.

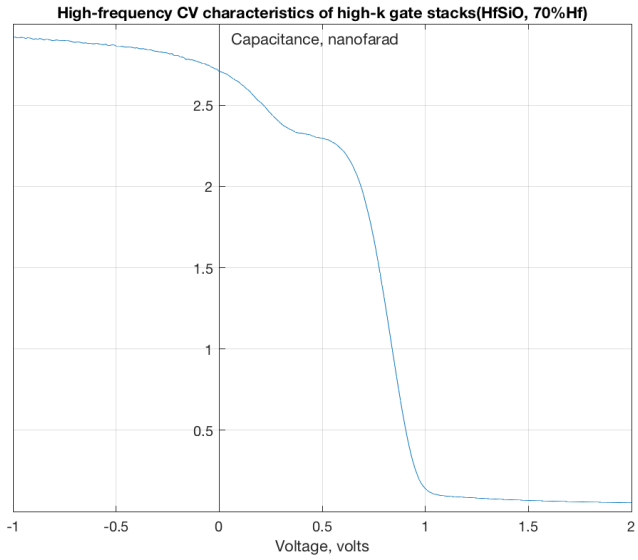

Fig. 3.1.1. High-frequency CV characteristics of high-k gate stacks.

The semiconductor substrate was identified as p-type. Explanations follow with consideration of different bias mode: accumulation, depletion and inversion.

Accumulation: adverting to figure 3.1, when the MOSC is negatively biased, charges being modulated were majority carriers which react quickly to the measuring signal. Thus, the oxide and the accumulation layer act together in series (Fig) to form the capacitance of the MOSC, which yields:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{acc}} \qquad (3.1.1)$$

Due to the exponential growth[?] of C_{acc} with the surface voltage φ_s when the MOSC is sufficiently negatively biased, we have

$$C_{acc} >> C_{ox} \qquad (3.1.2)$$

and therefore, we can write

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{acc}} \cong \frac{1}{C_{ox}} \qquad (3.1.3)$$

This approximation indicates that when the p-type MOSC is adequately negatively biased the MOSC capacitance will approach a constant value C_{max} which is equal to C_{ox}.

Depletion: as the gate voltage becomes positive, holes are driven away from the semiconductor surface and a depletion region develops. Thus, the MOSC capacitance is given by:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \qquad (3.1.4)$$

When an evenly doped semiconductor is assumed, the depletion region capacitance is given by:

$$C_{dep} = \frac{\varepsilon_o \varepsilon_s}{W} = \sqrt{\frac{qN_D \varepsilon_o \varepsilon_s}{2\varphi_s}} \qquad (3.1.5)$$

In other words, C_{dep} decreases with the gate voltage and so does the measured voltage as shown in Fig.3.1.

Inversion: Finally, the gate is biased positive enough to surpass the threshold voltage with the semiconductor surface filled with electrons. Now, the MOSC capacitance comprises the oxide capacitance and the semiconductor capacitance:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \qquad (3.1.6)$$

The semiconductor capacitance is given by the sum of the depletion region capacitance and the inversion layer capacitance in parallel:

$$Cs = C_{dep} + C_{inv} \qquad (3.1.7)$$

However, since the input measuring signal is at high frequency in which case the minority carrier electron cannot follow, the capacitance of the inversion layer is assumed to be zero. Thus, we obtain:

$$Cs = C_{dep} \qquad (3.1.8)$$

Nota bene that the depletion width remains unchanged with the gate charge from dc component being cancelled out by the inversion charge and the majority holes continues to be modulated at the depletion edge. By equ.3.3, C_{dep} is a constant with width unchanged. Thus, the MOSC capacitance is a constant with both Cdep and Cox being constant. Therefore, the MOSC capacitance reaches a constant minimum much smaller than C_{ox} as shown in Fig. 3.1.1.

To sum up, the plotted high-frequency capacitance voltage characteristics data of the MOSC conforms to that of a MOSC with p-type substrate and thus the semiconductor substrate was identified as p-type.

3.2 Oxide Relative Permittivity

3.2.1 Theory and Analysis

In the accumulation region, the equivalent circuit for the MOS capacitor is shown below.

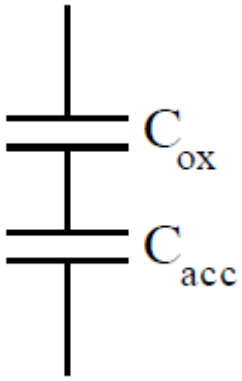

Figure 3.2.1. The AC equivalent circuit in accumulation [1]

Because in the accumulation region the accumulation capacitance C_{acc} is much greater than the oxide capacitance, thus $C_{max} \approx C_{ox}$, where C_{max} is the maximum capacitance in the C-V data. According to the theory of parallel plate capacitor:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \text{ [3]} \qquad (3.2.1)$$

The C_{max} （per area）is given by:

$$C_{max} = \frac{C_{ox}}{A_C} = \frac{\varepsilon_0 \varepsilon_r}{t_{total}} \qquad (3.2.2)$$

Where A_C is the area of the MOS capacitor:

$$A_C = \pi r^2 = \pi(\frac{d}{2})^2 \qquad (3.2.3)$$

t_{total} is the combined oxide thickness, which is the sum of the thickness of the layers high-k and SiOx:

$$t_{total} = t_{high-k} + t_{SiOx} \qquad (3.2.4)$$

Substituting equations (3.2.2) and (3.2.3) into (3.2.1) gives the relative permittivity of the combined oxide:

$$\varepsilon_r = \frac{t_{total} C_{ox}}{\varepsilon_0 A_C} \qquad (3.2.5)$$

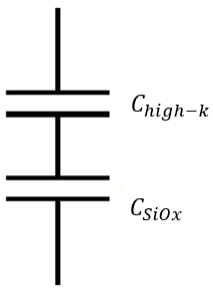

Figure 3.2.2. the equivalent circuit for two layers oxide stack.

This combined oxide capacitor can be equivalent to two parallel plate capacitors in series (shown in figure 3.2.2), thus they have relationship:

$$C_{high-k} = \frac{C_{max} * C_{SiOx}}{C_{max} + C_{SiOx}} [4] \qquad (3.2.6)$$

Apply equation (3.2.1), C_{SiOx} is given by

$$C_{SiOx} = \frac{\varepsilon_0 \varepsilon_{SiO2} A_C}{t_{ox}} \qquad (3.2.7)$$

Finally, the high-k layer relative permittivity:

$$\varepsilon_{high-k} = \frac{C_{high-k} t_{high-k}}{\varepsilon_0 A_C} \qquad (3.2.8)$$

MATLAB command line results:

```
The combined oxide relative permittivity is 6.802548
The high-k relative permittivity is 10.643037
```

3.3 Equivalent Oxide Thickness

The Equivalent Oxide Thickness (EOT) is distance of silicon oxide film and usually in nanometer, it need to produce a same effect used high-k material.

$$\epsilon_0 \epsilon_{SiO2} \frac{A}{EOT} = C \ [5] \qquad (3.3.1)$$

$$\epsilon_0 \epsilon_{SiO2} \frac{A}{C} = EOT \ [5] \qquad (3.3.2)$$

In the equation (3.3.1) and (3.3.2), ϵ_0 is the permittivity of vacuum is $8.85*10^{-12}$, ϵ_{SiO2} is the permittivity of SiO_2 is 3.9, A is the area of capacitor is $2.3758*10^{-6}$, C is capacitance is $2912*10^{-9}$F.

The Equivalent Oxide Thickness of oxide is 2.81nm.

The EOT(ox) be calculated by another formula as (3.3.4):

$$EOT_{ox} - t_{SiO2} = t_{high-k}\left(\frac{k_{SiO2}}{k_{high-k}}\right) \qquad (3.3.3)$$

$$EOT_{ox} = t_{high-k}\left(\frac{k_{SiO2}}{k_{high-k}}\right) + t_{SiO2} \qquad (3.3.4)$$

Where t_{high-k} is the thickness of the high-k layer being 3.3nm, k_{SiO2} the permittivity of the SiO_2 layer being 3.9, k_{high-k} the permittivity of the high-k layer being 10.643, t_{SiO2} the thickness of SiO2 being 1.6nm.

The EOT(high-k) calculated by another formula as 3.5:

$$EOT_{high-k} = t_{high-k}\left(\frac{k_{SiO2}}{k_{high-k}}\right) \qquad (3.3.5)$$

t_{high-k} is thickness of high-k layer (3.3nm), k_{SiO2} is the permittivity of SiO2 which is 3.9, k_{high-k} is permittivity of high-k layer which is 10.643

The Equivalent Oxide Thickness of high-k layer is 1.21nm.

3.4 Substrate Doping Density

3.4.1. Theory and Analysis

In the inversion region, the surface potential is given by:

$$\emptyset_S = 2\emptyset_F \text{ [6]} \qquad (3.4.1)$$

Where $\emptyset_F$ is fermi-potential, which can be calculated by:

$$\emptyset_F = V_t \ln\left(\frac{N_A}{n_i}\right) \qquad (3.4.2)$$

Where V_t is the thermal voltage:

$$V_t = \frac{kT}{q} \qquad (3.4.3)$$

As for the p-type substrate, the depletion capacitance is given by

$$C_{dep} = \frac{\epsilon_0 \epsilon_s}{W} = \sqrt{\frac{qN_A \epsilon_0 \epsilon_s}{2\emptyset_S}} \qquad (3.4.4)$$

The total capacitance can be calculated by

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \qquad (3.4.5)$$

integrating equations (3.4.1) to (3.4.5), doping density of silicon substrate can be find by:

$$N_A = \frac{4kT}{A^2 q^2 \varepsilon_o \varepsilon_s}\left[\frac{1}{C_{min}} - \frac{1}{C_{max}}\right]^{-2} \ln\frac{N_A}{ni} \qquad (3.4.6)$$

Where k is Boltzmens's constant, A is area of the capacitor, T is room temperature (300K), q is the elementary charge, ε_o, ε_s are permittivity of free space and relative permittivity of silicon respectively, ni is the intrinsic carrier concentration, C_{max} and C_{min} is the maximum and minimum capacitance in the C-V datasheet(approximation: $C_{max} \approx C_{ox}, C_{min} \approx C_{dep}$) and N_A is the doping density which needs to be solved.

3.4.2 Methods and Implementation

3.4.2.1 Use MATLAB Function "solve" to Solve Equation (3.4.6)

Equation 3.4.6 is a transcendental equation, which means we can't solve it directly. However, MATLAB has provided a function 'solve' which can solve most algebra equation:

```
>> double(na)

ans =

   1.0e+21 *

    4.2321
    0.0000
```

Figure 3.4.1. The solution returned by MATLAB.

Figure 3.4.1 shows that "solve" function will return 2 solutions: $na_{(1)}$=4.23207*10^21 and $na_{(2)}$=0(which is impossible), abandon the impossible solution and the doping density is 4.2321*10^21 m^{-3}.

3.4.2.2 Use Bisection and Iteration Method to Solve Equation (3.4.6)

i) Initial approximation

Firstly, estimate the solution and define the initial interval including the solution, in this case after simplifying the equation (3.4.6):

$$N_A = 3.267 * 10^{20} * \ln\frac{N_A}{n_i} \tag{3.4.7}$$

Since the this is a p-type substrate, $N_A > n_i$, therefore, $\ln\frac{N_A}{n_i} > 1$, thus $N_A > 3.267 * 10^{20}$. Try a possible solution$N_A = 10^{22}$, this gives us $10^{22} > 4.613 * 10^{21}$ so the solution of the equation must smaller than$10^{22}m^{-3}$.

Therefore, the initial interval was chosen as (10^{20}, 10^{22}).

ii) Use bisection method and MATLAB to find more accurate solution.

The algorithm for the bisection method:

$$c_n = \frac{a_n + b_n}{2}$$

$$\begin{cases} a_{n+1} = c_n, b_{n+1} = b_n (c_n > expected\ value) \\ b_{n+1} = c_n,\ a_{n+1} = a_n (c_n < expected\ value) \end{cases} \text{[7]} \tag{3.4.8}$$

Where c_n is the result after n times iteration and $a_n,\ b_n$ is the n^{th} upper and lower boundary (In this case $a_1 = 10^{22}$,$b_1 = 10^{20}$). Use "for" loop to implement this algorithm and store the c_n in an array "result". Plot the graph of doping density

versus the iteration times, using the result obtained by the 'solve' function as reference.

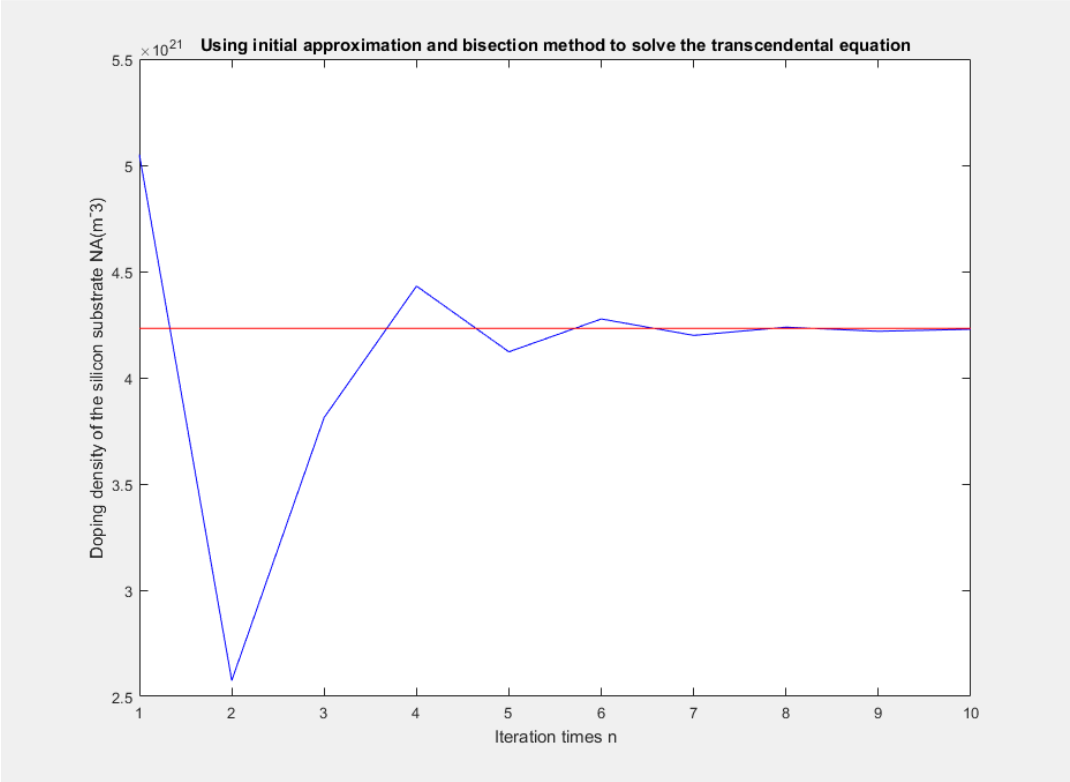

Figure 3.4.2. Using initial approximation and bisection method to solve the transcendental equation.

Figure 3.4.2 shows that the result is very close to the solution found by "solve" after 10 times iteration.

iii) Discussion

If the iteration times is defined large enough (such as 100), the result will not change any more after 54 times iteration, and the final result is the same as the result obtained by MATLAB function "solve".

3.5 Work Function Difference Assuming Au Gate

The work function difference can be calculated from:

$$\Phi_{AuS} = \Phi_{Au} - \Phi_S \quad (3.5.1)$$

For the gold gate, the work function is measured as:

$$\Phi(Au) = 5.1 \text{ eV} \quad (3.5.2)$$

The work function for the semiconductor substrate given by:

$$\Phi_S = \chi(Si) + E_g(Si)/2 + \varphi_F(Si) \quad (3.5.3)$$

where $\chi(Si) = 4.14$ eV and $E_g(Si) = 1.12$ eV.

The Fermi potential of a p-type substrate is defined as:

$$\varphi_F = V_t \ln(N_A/n_i) \quad (3.5.4)$$

where the acceptor doping concentration is calculated in section 3.4

with $N_A = 4.23 * 10^{21}$ and the thermal voltage is defined as $V_t = kT/q = 25$ mA

Apply 3.5.2, 3.5.3 and 3.5.4 to 3.5.1, we have:

$$\Phi_{AuS} = \Phi(Au) - (\chi(Si) + E_g(Si)/2 + kT/q*\ln(N_A/n_i))$$

which yields by MATLAB:

$$\Phi_{AuS} = 0.065 \text{ eV}$$

which indicates that Φ_{AuS} serves to increase the threshold voltage. That is, in the absence of an applied gate voltage, the semiconductor layer is slightly accumulated.

3.6 Flatband Voltage

The equivalent circuit at flatband is shown in Figure 3.6.1.

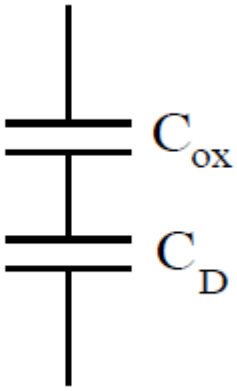

Figure 3.6.1. The equivalent circuit for flatband condition.

The Cox is the oxide capacitance and the C_D can calculated by equation 3.6.1.

$$C_D = \frac{\varepsilon_0 \varepsilon_s}{L_D} \quad (3.6.1)$$

L_D is the Debye length and can calculated by equation 3.6.2.

$$L_D = \sqrt{\frac{\varepsilon_0 \varepsilon_s V_t}{q N_D}} \quad (3.6.2)$$

N_D is the doping density calculated in section 3.4 and the result is $4.2556 \times 10^{21} m^{-3}$, therefore, L_D is $6.1839 \times 10^{-8} m$, C_D is $3.9782 \times 10^{-10} F$ and equivalent capacitance equation at flatband is shown in equation 3.6.3.

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{C_D} \quad (3.6.3)$$

$C_{FB} = 3.5010 \times 10^{-10} F$, and find the corresponding flatband band voltage in C-V characteristics which is 0.93V.

3.7 Midgap Voltage

3.7.1 Theory and Analysis

Assuming a uniformly doped semiconductor, the depletion capacitance at midgap condition is given by:

$$C_{dep} = \frac{\varepsilon_0 \varepsilon_S}{W} = \sqrt{\frac{qN_D \varepsilon_0 \varepsilon_r}{2\emptyset_F}} \qquad (3.7.1)$$

Since in midgap condition the surface potential of the substrate is equal to the semiconductor's Fermi level:

$$\emptyset_{S(midgap)} = \emptyset_F \qquad (3.7.2)$$

As the equivalent circuit discussed in section 3.1, the MOS capacitor in depletion region is equivalent to a depletion capacitor and an oxide capacitor connected in series, that is

$$C_{mg} = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}} \qquad (3.7.3)$$

After the midgap capacitance is obtained(7.4895×10^{-11}F), the corresponding midgap voltage can be find by check the C-V datasheet using CV_search function, and the result midgap voltage is 1.367V.

3.7.2 Methods and Implementation

CV_search function (see Appendix A) can find out the corresponding gate voltage value of the input capacitance value in the C-V data sheet. Firstly, this function will find the closest capacitance C_n to the aim capacitance and record the corresponding voltage V_n and relevant capacitances: C_{n-1} and C_{n+1}(n is the index which means this value is the n^{th} value in the voltage or capacitance array) After that, compare the aim capacitance with the closest value, since the data in the data sheet are discrete, the voltage interval between two point is 0.01V, and the final result was calculated by Linear Approximation:

$$\mathrm{V} = \begin{cases} V_n + 0.01\left(\frac{C_n - C_{aim}}{C_n - C_{n+1}}\right), & \mathrm{C_{aim}} < C_n \\ V_n - 0.01\left(\frac{C_{aim} - C_n}{C_{n-1} - C_n}\right), & \mathrm{C_{aim}} \geq C_n \end{cases} \qquad (3.7.4)$$

The MATLAB command line result:

```
The equivalent capacitance at midgap condition is 7.4895e-11F
The midgap voltage is 1.367214V
```

3.8 Oxide Charge Density

3.8.1 Flat-band Condition

According to the definition of capacitor:

$$Q = CV \tag{3.8.1}$$

So, the charge in the flat-band condition per unit area can be calculated by 3.8.2

$$Q_{ox} = \frac{-C_{ox}(V_{flatband} - \Phi_{MS})}{A} \tag{3.8.2}$$

C_{ox} is the maximum capacitance of oxide is 2.919×10^{-9} , $V_{flatband}$ is flat-band voltage calculated in Task 6 which is 0.93V, Φ_{MS} is work function difference calculated in Task 5 which is 0.0652eV, A is the area of the MOS capacitor. Through calculation, charge per unit area is $-1.0625 \times 10^{-6} C/cm^2$.

The charge density can be calculated by equation 3.8.3

$$N_{ox} = \frac{Q_{ox}}{q} \tag{3.8.3}$$

q is elementary charge which is $-1.602 \times 10^{-19} C$, thus the charge density per unit area is $-6.6325 \times 10^{12} C/cm^2$.

The total charges at flat-band condition is $N_{ox} \times A = -157.5765\ C$.

3.8.2 Midgap Condition

Firstly, calculate the ideal gate voltage using equation 3.8.4 and the result is 0.4674V:

$$V_G = \frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} \sqrt{\frac{2qN_A\phi_F}{\varepsilon_0 \varepsilon_{ox}}} + \phi_F + \Phi_{MS} \tag{3.8.4}$$

The mid gap voltage shift can be calculated by equation 3.8.5 which is -0.9026V:

$$\Delta V = V_G - V_{midgap} (3.8.5)$$

The charger per unit area calculated by equation 3.8.6 and result is

$-0.109 \times 10^{-6} C/cm^2$:

$$Q_{ox} = \frac{C_{ox}\Delta V}{A} (3.8.6)$$

Finally, the charge density is $-6.9226 \times 10^{12} C/cm^2$:

$$N_{ox} = \frac{Q_{ox}}{q} (3.8.7)$$

The total charges at mid-gap condition is $N_{ox} \times A = -164.4686\, C$.

3.9 Comparison with Control Group

The high-k gate stack studied in this project is composed by HfSiO (70%Hf), SiO_2 and Si. The comparisons of the electrics properties of the 70% Hafnium and 50% Hafnium HfSiO gate stack are shown in the table below:

%Hf	Relative Permittivity k	EOT(nm)	Flatband Voltage(V)	Per Unit Area Oxide Charge(C/cm^2)	High-k Layer Thickness(nm)
50	8.6	3.04	0.52	-5.3x10^12	3.2
70	10.6	2.79	0.93	-6.6x10^12	3.3

Table.1: the electric properties of 70% Hf HfSiO and 50% Hf HfSiO high-k gate stacks.

The relative permittivity of $HfSiO_4$ is 11 and the relative permittivity of SiO_2 is 3.9 [1], thus the relative permittivity of the oxide layer increased with the concentration of Hf. As the data listed in table 1, when the percentage of Hf in the gate stack is increased from 50% to 70%, the relative permittivity of the high-k layer is increased from 8.6 to 10.6 as expected. Since the EOT is given by:

$$EOT = t_{high-k}\left(\frac{k_{SiO2}}{k_{high-k}}\right) \quad (3.9.1)$$

The EOT is decreased from 3.04 to 2.79 for 70% Hf gate stack as the dominator is increased. Moreover, the reasons of the oxide charge formation are complicated, most of which mainly come from incomplete oxidation, poor quality control of chemicals, slow trapping, hot electron degradation and radiation [2]. Therefore, the theoretical relationship between the concentration of Hf and the oxide charge density is difficult to determine. Table 1 indicates that with the increasing concentration of Hafnium in the gate stack, the magnitude of the per unit area oxide charge increased from -5.3×10^{12} C/cm^2 to -6.6×10^{12} C/cm^2 .

Furthermore, in flatband condition:

$$V_{FB} = \Phi_{MS} - \frac{Q_{ox}}{C_{ox}} \quad (3.9.2)$$

Where Φ_{MS} is the metal semiconductor work function difference, the Q_{ox} is the oxide charge which is given by:

$$Q_{ox} = A\rho_{ox} \quad (3.9.3)$$

where ρ_{ox} is the oxide charge density, and C_{ox} is the oxide capacitance, which can be expressed as:

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{EOT} = \frac{\varepsilon_o \varepsilon_{ox} A}{t_{high-k}\left(\frac{\varepsilon_{SiO2}}{\varepsilon_{high-k}}\right) + t_{SiO_x}} \quad (3.9.4)$$

Therefore, the theoretical flatband voltage:

$$V_{FB} = \Phi_{MS} - \frac{\rho_{ox}[t_{high-k}\left(\frac{\varepsilon_{SiO2}}{\varepsilon_{high-k}}\right) + t_{SiO_x}]}{\varepsilon_o \varepsilon_{ox}} \quad (3.9.5)$$

In this case, comparing to 50% Hafnium, 70% Hafnium gate stack has a higher relative permittivity ε_{ox} and ε_{high-k}, thicker high-k layer thickness t_{high-k} and denser oxide charge density ρ_{ox}. The result shows that flatband voltage for 70% Hf gate stack(0.93V) is much higher than 50% Hf case(0.52V), this is mainly because the oxide charge density ρ_{ox} difference as equation (3.9.5) and table.1 implied.

3.10 Ideal HFCV Plot

3.10.1 General Description

In order to plot the ideal C-V characteristic curve, the relationship between the gate voltage and the capacitance must be found. It is very difficult to express the gate voltage in terms of capacitance directly, however, the gate voltage can be expressed as a function of the surface potential $V(\emptyset_S)$ and the relationship between the capacitance and the surface potential is also clear $C(\emptyset_S)$. Therefore, start with substituting a series of value for $\emptyset_S$ into the functions of $V(\emptyset_S)$ and $C(\emptyset_S)$ and a discreet function $V[C]$ can be obtained. Finally, the ideal C-V characteristic can be plotted using the scatter points in this discreet function.

3.10.2 The relationship between the gate voltage and surface potential $V(\emptyset_S)$

In general, the gate voltage can be expressed as the sum of the flatband voltage, the voltage across the oxide and the surface potential:

$$V_g = V_{FB} + \emptyset_S + V_{ox} \tag{3.10.1}$$

In ideal case where no charge presents in the oxide layer:

$$V_{FB} = \Phi_{MS} \tag{3.10.2}$$

Where Φ_{MS} is the work function difference between silicon and metal (gold in this case). In absolutely ideal condition, we assume$\Phi_{MS} = 0$, this will be discussed in the section 3.10.5.

V_{ox} can be expressed in terms of electric field:

$$V_{ox} = \frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} E_s(\emptyset_S) \tag{3.10.3}$$

Where ε_s is the relative permittivity of silicon, ε_{ox} is the relative permittivity of the oxide layer, t_{ox} is the total thickness of the combined oxide layer. $E_s(\emptyset_S)$ is the electric field as a function of surface potential, which can be derivate from one dimensional Poisson's equation:

$$\nabla^2 \emptyset = \frac{d^2 \emptyset}{dx^2} = \frac{-\rho}{\varepsilon_0 \varepsilon_s} \tag{3.10.4}$$

Where ρ is the charge density, according to the charge conservation law:

$$\rho = q(p + {N_d}^+ - n - {N_a}^-) \tag{3.10.5}$$

Under thermal equilibrium, p and n can be expressed as a function of the potential $\emptyset(x)$. Where $\emptyset(x)$ is a function about distance.

$$\text{p}=n_i e^{\frac{q(\emptyset_F - \emptyset(x))}{kT}} \tag{3.10.6}$$

According to mass action law:

$$n=\frac{{n_i}^2}{p}=n_i e^{\frac{-q(\emptyset_F-\emptyset(x))}{kT}} \tag{3.10.7}$$

In high frequency, deep depletion cases, the generation of the electrons at the oxide semiconductor interface can't follow the change of gate voltage, in deep depletion region, we assume:

$$n=0 \tag{3.10.8}$$

Integrating equations (3.10.5), (3.10.6) and (3.10.7):

$$\rho=q(n_i e^{\frac{q(\emptyset_F-\emptyset(x))}{kT}}+{N_d}^+-n_i e^{\frac{-q(\emptyset_F-\emptyset(x))}{kT}}-{N_a}^-) \tag{3.10.9}$$

When x(distance from the surface) is large enough, $\emptyset(x)=0$ and $\rho=0$, thus:

$${N_d}^+-{N_a}^-=n_i e^{\frac{-q\emptyset_F}{kT}}-n_i e^{\frac{q\emptyset_F}{kT}}=-2n_i sh\left(\frac{\emptyset_F}{V_T}\right) \tag{3.10.10}$$

Therefore, substituting equations (3.10.10) into (3.10.9), the low frequency formula becomes:

$$\frac{d^2\emptyset}{dx^2}=\frac{2qn_i}{\varepsilon_0\varepsilon_s}\left[sh\left(\frac{\emptyset-\emptyset_F}{V_T}\right)+sh\left(\frac{\emptyset_F}{V_T}\right)\right] \tag{3.10.11}$$

Similarly, integrating equations (3.10.5) (3.10.7), (3.10.8) and (3.10.10) we have:

$$\rho=q\left(n_i e^{\frac{-q\left(\emptyset_F-\emptyset(x)\right)}{kT}}+{N_d}^+-{N_a}^-\right)=qn_i e^{\frac{\emptyset-\emptyset_F}{V_T}}-2qn_i sh\left(\frac{\emptyset_F}{V_T}\right) \tag{3.10.12}$$

Substituting equation (3.10.12) into (3.10.4):

$$\frac{d^2\emptyset}{dx^2}=\frac{qn_i}{\varepsilon_0\varepsilon_s}\left[2sh\left(\frac{\emptyset_F}{V_T}\right)-e^{\frac{\emptyset_F-\emptyset}{V_T}}\right] \tag{3.10.13}$$

According to Maxwell equations, the electric field intensity is equal to the negative potential gradient:

$$E=-\frac{d\emptyset}{dt} \tag{3.10.14}$$

Substituting equation (3.10.14) into (3.10.13) and (3.10.11):

The low frequency cases:

$$E(\emptyset)_{LF} = sign(\emptyset)\sqrt{\frac{4qn_iV_T}{\varepsilon_0\varepsilon_s}[ch\left(\frac{\emptyset-\emptyset_F}{\emptyset_T}\right) + \frac{\emptyset}{V_T}sh\left(\frac{\emptyset_F}{V_T}\right) + K} \quad (3.10.15)$$

Where K can be determined by using the boundary condition: $E(+\infty) = 0$, which give us: $K = -ch(\frac{\emptyset_F}{V_T})$ (3.10.16)

Combine equations (3.10.12) and (3.10.13), the electric field in low frequency case can be expressed as

$$E(\emptyset)_{LF} = sign(\emptyset)\sqrt{\frac{4qn_iV_T}{\varepsilon_0\varepsilon_s}[ch\left(\frac{\emptyset-\emptyset_F}{\emptyset_T}\right) + \frac{\emptyset}{V_T}sh\left(\frac{\emptyset_F}{V_T}\right) - ch(\frac{\emptyset_F}{V_T})]} \quad (3.10.17)$$

In high frequency condition and deep depletion region (the premise is (3.10.8)), the oxide electric field can be calculated as:

$$E(\emptyset)_{HF} = sign(\emptyset)\sqrt{\frac{2qn_iV_T}{\varepsilon_0\varepsilon_s}[2\frac{\emptyset_S}{V_T}sh\left(\frac{\emptyset_F}{V_T}\right) + e^{\frac{\emptyset_F}{V_T}}(e^{-\frac{\emptyset_S}{V_T}} - 1)]} \quad (3.10.18)$$

Integrating equations (3.10.1), (3.10.2), (3.10.3), (3.10.17) can obtain the relationship between the gate voltage and surface potential for low frequency cases, combine equations (3.10.1), (3.10.2), (3.10.3), (3.10.18) can find this relationship in high frequency deep depletion region, these operation are implemented in the MATLAB code.

3.10.3 The relationship between the capacitance and surface potential C($\emptyset_S$)

According to the definition of capacitance:

$$C = |\frac{dQ}{dV_g}| \quad (3.10.19)$$

According to Gaussian's law:

$$dQ = \varepsilon_0 \varepsilon_s dE \tag{3.10.20}$$

Apply differential chain rule:

$$C = \left|\frac{dQ}{dV_g}\right| = \frac{\varepsilon_0 \varepsilon_s dE}{d\emptyset_S}\frac{d\emptyset_S}{dV_g} \tag{3.10.21}$$

In general, the MOS capacitor can be equivalent to a substrate capacitor and an oxide capacitor connected in series

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_S} \tag{3.10.22}$$

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} A}{t_{ox}} \tag{3.10.23}$$

Therefore, the substrate capacitance can be obtained by substituting the electric field equations (3.10.17) and (3.10.18) and the MOS capacitor equations (3.10.21) and (3.10.22) into (3.10.23):

Low frequency cases:

$$C_{S,LF}(\emptyset_S) = \varepsilon_S \frac{dE(\emptyset)_{LF}}{d\emptyset_F} A = A \frac{2qn_i sign(\emptyset_S)}{E(\emptyset)_{LF}} \left| sh\left(\frac{\emptyset_S - \emptyset_F}{V_T}\right) + sh\left(\frac{\emptyset_F}{V_T}\right) \right| \tag{3.10.24}$$

High frequency deep depletion cases:

$$C_{S,dd}(\emptyset_S) = \varepsilon_S \frac{dE(\emptyset)_{HF}}{d\emptyset_F} A = A \frac{qn_i sign(\emptyset_S)}{E(\emptyset)_{HF}} \left[2sh\left(\frac{\emptyset_F}{V_T}\right) - e^{\frac{\emptyset_F - \emptyset_S}{V_T}} \right] \tag{3.10.25}$$

Again, equation (3.10.25) is only valid in deep depletion region.

3.10.4 Special cases

Under flat band condition ($|\emptyset_S| < V_t$), the capacitance is given by:

$$C_{FB} = A\sqrt{\frac{\varepsilon_0 \varepsilon_S V_t}{qN_A}} \tag{3.10.26}$$

Which has been discussed in section 3.6 in this report.

3.10.5 Result and discussion

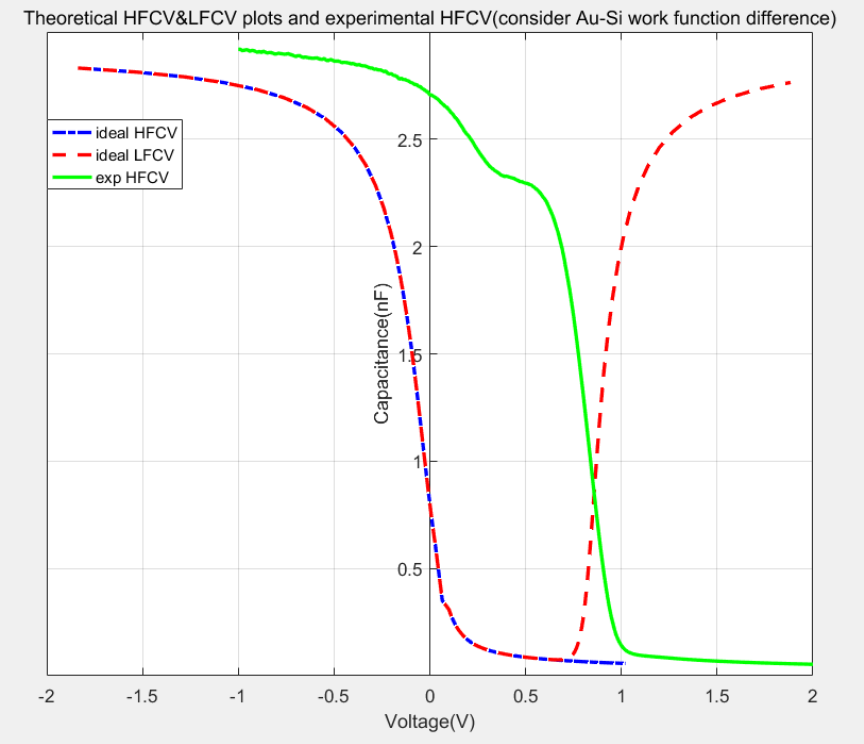

Figure 3.10.1. The HFCV&LFCV plots and experimental HFCV (consider Au-Si work function difference)

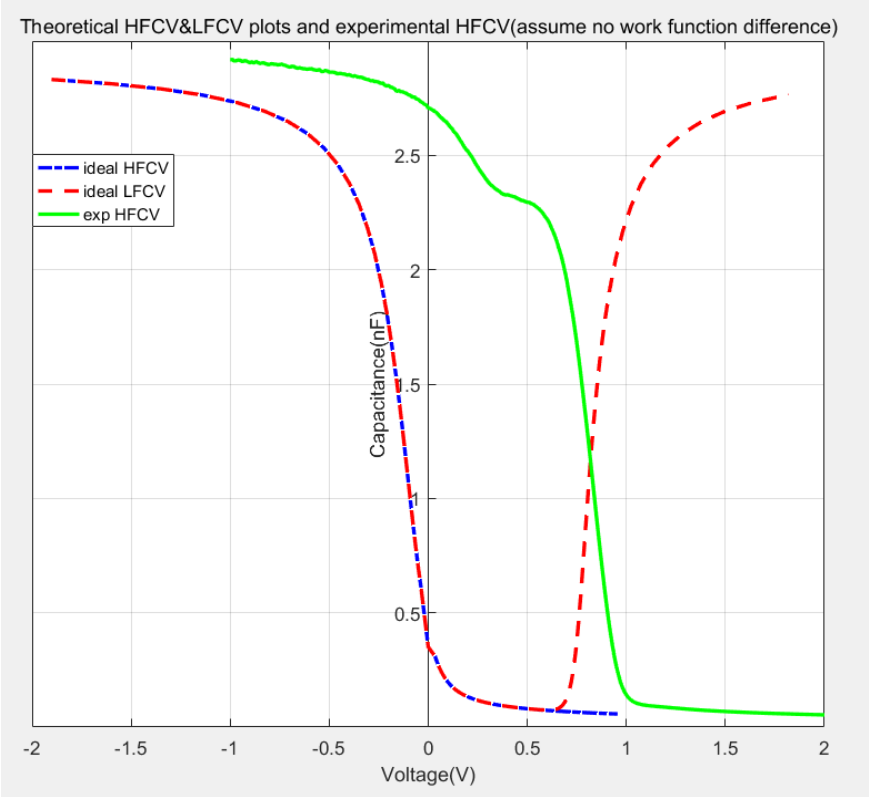

Figure 3.10.2. The HFCV&LFCV plots and experimental HFCV (assume no Au-Si work function difference, absolutely ideal)

Since the negative oxide charge is ignored in the ideal case, the ideal plot shown in figure 3.10.1 is shifted to left compare to the empirical result. Due to the reason discussed in previous section (the difference between equations (3.10.7) and (3.10.8)), the low frequency equivalent capacitance increases to C_{max} again whereas the high frequency equivalent capacitance goes to C_{min} in the deep depletion region. Figure 3.10.2 shows the CV characteristic curve under absolute ideal conditions where $V_{FB} = 0V$, the gold-silicon work function difference was ignored, thus the plot shifted to left further.

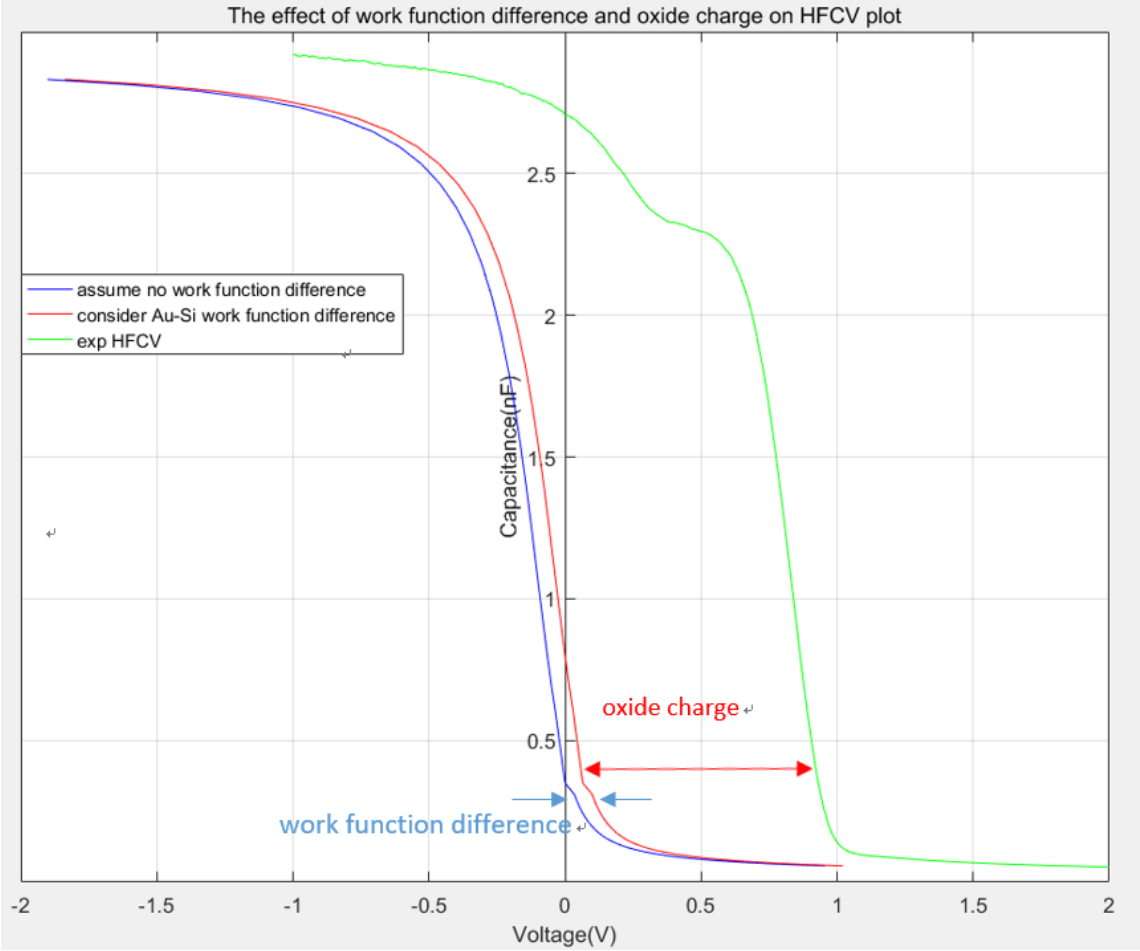

Figure 3.10.3. the effect of work function difference and oxide charge on HFCV plot

Figure 3.9.3 shows three different HFCV plot and the relationship between them.

3.10.6 Limitation and Further Research

i) In this program, when the absolute value of surface potential $\emptyset_S$ is smaller than the thermal voltage (equation (3.10.26)), the program will consider this as flat band condition and set the gate voltage to V_{FB} and capacitance to C_{FB}, this leads to a slightly distortion in the plot. More precise formula is needed for flat band condition capacitance to obtain a better plot.

ii) Formula (3.10.25) is only an approximate solution, which introduces an error which is less than 7% [8], the exact expression for the high frequency capacitance is [8]:

$$C_{S,dd}(\emptyset_S) = \varepsilon_S \frac{dE(\emptyset)_{HF}}{d\emptyset_F} A = A \frac{qn_i sign(\emptyset_S)}{E(\emptyset)_{HF}} [2sh\left(\frac{\emptyset_F}{V_T}\right) - e^{\frac{\emptyset_F - \emptyset_S}{V_T}}]$$

$$C_{S,HFexact} = \frac{qn_i sign(\emptyset_S)}{E_S(\emptyset_S)} \left\{ e^{\frac{\emptyset_F}{V_T}} \left[1 - e^{-\frac{\emptyset_S}{V_T}} \right] + e^{-\frac{\emptyset_F}{V_T}} [e^{-\frac{\emptyset_S}{V_T}} - 1](1 + \Delta) \right\} \quad (3.10.27)$$

where Δ is a fraction taking into account the constancy of inversion layer charge and its spatial redistribution.

Chapter 4

Discussion and Conclusion

4.1 Discussion

The MOS capacitor is the basic structure of the MOSFET, thus the electrical properties of MOS capacitor is closely related to the electrical characteristics of MOSFET and its industrial applications.

i. Switching Speed

Subthreshold swing (S factor) is a factor measures how quickly a MOSFET turn on and off, which is given by [9]:

$$S = mV_T \ln(10) \quad (4.1.1)$$

Where V_T is the thermal voltage:

$$V_T = \frac{kT}{q} \quad (4.1.2)$$

The m factor is defined as:

$$m = \frac{dV_G}{d\Phi_s} = 1 + \frac{C_S}{C_o} \quad (4.1.3)$$

where C_S is the capacitance of semiconductor substrate and C_o the gate oxide capacitance. As the analysis presented in section 3.9, the 70% Hafnium gate stack has

a higher relative permittivity thinner EOT compared with 50% Hafnium gate stack, which means under the same conditions (such as oxide thickness and capacitor area), the 70% Hf gate stack will have a higher oxide capacitance C_o, thus smaller m factor and consequently smaller S factor and higher speed.

However, the threshold voltage for a MOSFET is given by:

$$V_{TH} = t_{ox}\frac{\varepsilon_s}{\varepsilon_{ox}}\sqrt{\frac{2qN_A \cdot 2\Phi_F}{\varepsilon_0\varepsilon_s}} + 2\Phi_F + \frac{Q_f}{C_{ox}} + \frac{Q_{ss}(V_G)}{C_{ox}} + \Phi_{MS} \qquad (4.1.4)$$

As the analysis presented in section 3.9, the fixed oxide charge Q_f will increase with the concentration of Hafnium and this will cause the threshold voltage increasing, which will slow down the transistor switching speed [9].

ii. Power Consumption

The total power consumption of the MOS circuit consists of static power consumption and dynamic power consumption [9] [10]:

$$P_{total} = P_{dynamic} + P_{static} \qquad (4.2.5)$$

Transform equation (4.2.5) into energy form, the average energy consumed per micron of transistor width is given by [10]:

$$E_{total} = E_{dynamic} + E_{static} = C_{eff}V^2 + I_S e^{\frac{V_{TH}}{V_o}} VT_C \qquad (4.2.6)$$

Where C_{eff} is the average capacitance switched every cycle per micron of transistor width, V is the supply voltage, I_S is zero-threshold leakage current, V_o is the subthreshold slope which is the inverse of subthreshold swing S, V_{TH} is the threshold voltage and T_C is the cycle time. Equation (4.2.6) shows that high threshold voltage will leads to high static energy consumption, meanwhile, in order to guarantee the MOSFET switching speed for a relative high threshold voltage, the supply voltage should also be designed higher and this will result in high dynamic power consumption

[9]. Therefore, lowering the threshold voltage is generally advantageous for minimize the power consumption [4]. On the contrary, the smaller subthreshold swing will improve the ratio of $\frac{I_{on}}{I_{off}}$ and this will reduce the static power consumption [11](also reflected in equation (4.2.6)).

The electrical properties of 50% and 70% gate stack were summarized in figure 4.2.1.

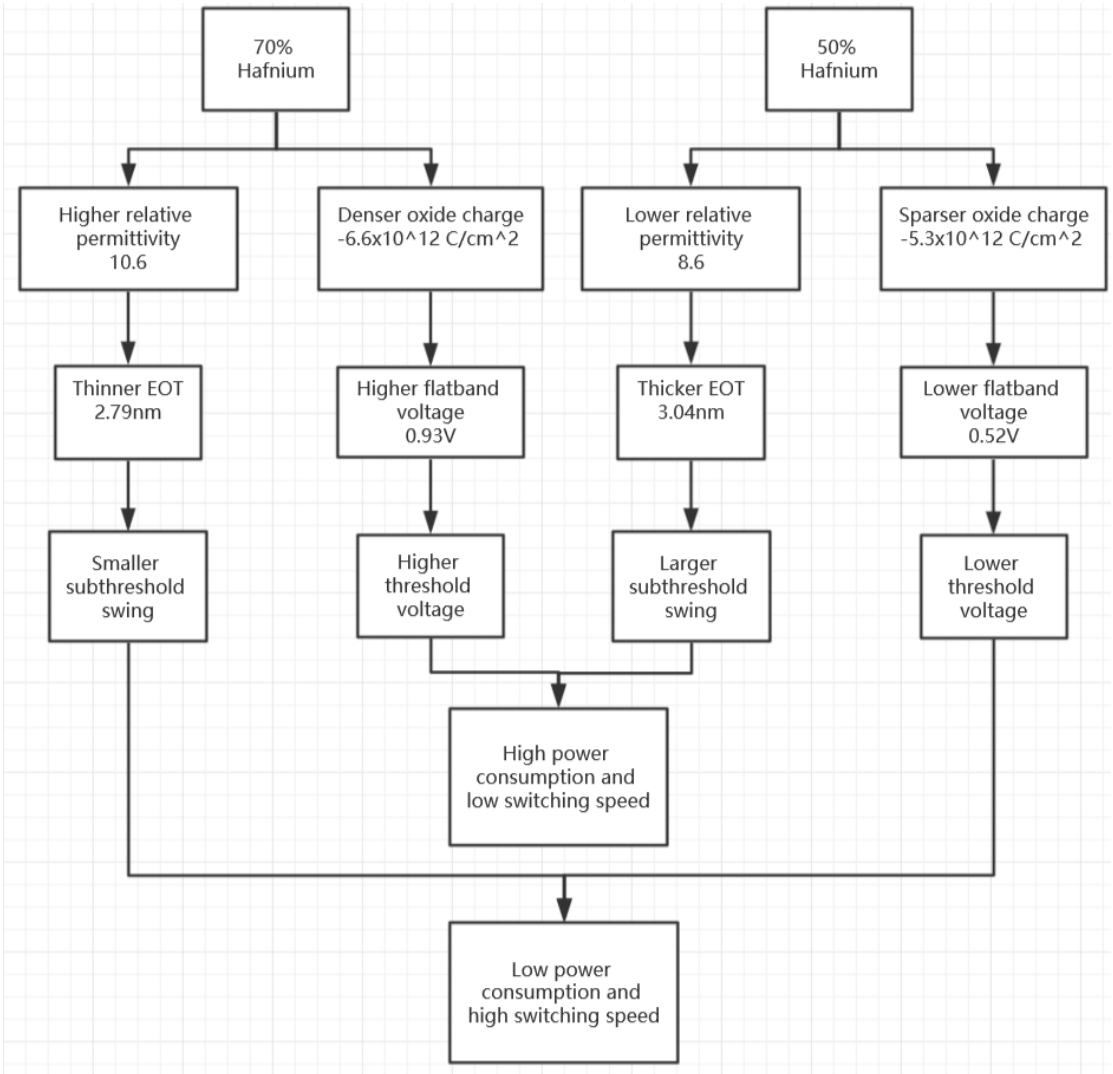

Figure 4.2.1. Causality between electrical parameters and comparison of %50Hf and %70Hf gate stack electrical properties.

In the industrial design and application, designers should balance power consumption and switching speed to meet the requirements specification. Therefore, the optimal concentration of Hf should be further studied based on the specific issues.

4.2 Conclusions

In conclusion, the electrical properties of the thin high-k gate stack (HfSiO, 70% Hf) were determined and analysed in this project.

i) Comparing to traditional SiO_2 gate dielectric, the high-k gate stack had a thickness of 4.9nm with EOT of only 2.79nm, which could prevent leakage current caused by tunnelling effect while still providing sufficiently high oxide capacitance even with reduced area.

ii) Compared with the 50% hafnium high-k gate stack, the 70% hafnium gate stack was found to have a greater relative oxide permittivity and consequently a thinner EOT, which would be of significance in manufacturing high-speed integrated circuit. However, with higher hafnium presented in stack oxide, the oxide charge density went higher, leading to higher flatband and midgap voltage which would result in higher power consumption.

iii) In comparison with ideal MOS capacitor, there existed a shift in the real high-k MOS capacitor's C-V characteristic curve which is due to oxide charge and work function difference.

In summary, high-k gate stack has a wide range of application prospects in the manufacture of integrated circuits, however, there is still considerable room for improvement in the selection of high-k materials and in the optimization of element concentrations.

4.3 Self Evaluation

Through the project, the analytical techniques in modelling MOS capacitors were developed, merits of high-k gate stacks were verified, and the implementation skills with MATLAB to solve practical problems were consolidated. This project was completed successfully, in that all the objectives were achieved accredited to the neatly-organized teamwork. All the group members had a sense of great achievement

in the end of the project and deemed that the skill and knowledge gained in this project will benefit future study.

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Appendices

Appendix A

Project Management Forms

(original copy submitted to supervisor)

Appendix B

Complete Executable MATLAB Code

The necessary files to execute Y2_project_G2.m:

1. **Group2-HFCV_70%Hf.txt**
2. **CV_search.m:**

```
function [ V_aim ] = CV_search( C_aim,C,V )

%This function can find out the corresponding gate
voltage value of the input capacitance value in the C-V
data sheet.

%C_aim in Fara and V in Volt
```

```
C_aim=C_aim*10^12;
d_min=min(abs(C_aim-C));
for b=1:length(C)
if d_min==abs(C(b)-C_aim)
    temp_V=V(b);
    temp_C=C(b);
    temp_C_1=C(b+1);
    temp_C_2=C(b-1);
end
end
    if C_aim<temp_C% formula (3.7.4)
        temp_V=temp_V+((temp_C-C_aim)/(temp_C-
temp_C_1))*0.01;
    else
        temp_V=temp_V-((C_aim-temp_C)/(temp_C_2-
temp_C))*0.01;
    end
V_aim=mean(temp_V);
end
```

3. Y2_project_G2.m:

```
clear
%MOSC SPECICICATION
d_MOSC = 0.55*10^(-3);
t_HiK = 3.3*10^(-9);
t_SiOx = 1.6*10^(-9);
```

```
A_MOSC = pi*(d_MOSC/2)^2;%Derived MOSC Area


%PHYSICAL CONSTANTS
q = 1.602*10^(-19);
p_Vaccum = 8.85*10^-12;
p_SiO2 = 3.9;
p_Si=11.7;              %Sillicon relative permittivity
k_B = 1.38*10^(-23);  %Boltzmann's constant J/K
ni_Si = 1*10^16;
Eg_Si = 1.12;
T = 300;
Chi_Si = 4.14;  %Electron affinity of Silicon
PHI_Au = 5.1;   %Work function of Au


%Task1: High frequency C-V characterictic
Table = readtable('Group2-HFCV_70%Hf.txt');
Table.Properties.VariableNames{1} = 'V';
Table.Properties.VariableNames{2} = 'C';
Table.Properties.VariableNames{3} = 'R';
figure,plot(Table.V, Table.C*10^-3);
title('High-frequency C-V characteristics of high-k gate
stacks(HfSiO, 70%Hf)');
xlabel('Voltage£¨V£©');
ylabel('Capacitance (nF)');
ax = gca;
ax.YAxisLocation = 'origin';
```

```
grid on;

fprintf('It can be analysed from the plot that the
substrate is p-type \n');

%Task2: oxide relative permittivity

C_max = max(Table.C)*10^(-12);           %Obtain the
maximum capacitance from the datasheet

C_ox = C_max;                            %The oxide
capacitance is approximately equal to the maximum
capacitance in accumulation region

t_total=t_HiK+t_SiOx;                    %The toltal
thickness is the sum of the high-k layer thickness and
the oxide layer thickness (3.2.4)

p_ox = C_ox*t_total/(A_MOSC*p_Vaccum);   %Calculate the
effective relative permittivity (3.2.5)

C_SiOx = p_SiO2*p_Vaccum*A_MOSC/t_SiOx;  %Calculate the
capacitance of the SiO2 layer (3.2.7)

C_HiK = C_ox*C_SiOx/(C_SiOx-C_ox);       %Calculate the
capacitance of the high-k layer (3.2.6)

p_HiK = C_HiK*t_HiK/(p_Vaccum*A_MOSC);   %Calculate the
raletive permitivity of the high-k layer (3.2.8)

fprintf('The combined oxide relative permittivity is
%f\n', p_ox);

fprintf('The high-k relative permittivity is %f\n',
p_HiK);



%Task3: Equivalent oxide thickness

EOT_HiK = t_HiK*(p_SiO2/p_HiK);

EOT_ox = EOT_HiK+t_SiOx;

fprintf('The EOT of the high-k layer is %f nm \n',
EOT_HiK*10^9);
```

```
fprintf('The EOT of the combined oxide layer is %f nm\n',
EOT_ox*10^9);


%Task4: (using solve function): Doping density of the
silicon substrate

C_min=min(Table.C)*10^(-12);              %obtain the
minimum capacitance from the datasheet

syms na;                                  %declare na as
a symbolic variable

na=solve(na==(4/A_MOSC^2)*(k_B*T/q^2)*(1/(p_Vaccum*p_Si))
*(((1/C_min)-(1/C_max))^(-2))*log(na/ni_Si));

%equation (3.4.6)

NA=double(na(1));%abandon the unreasonable solution and
change the symbolic variable in to double type

fprintf('The doping density of the silicon substrate is
%g \n',NA);

%Task4: (using bisection method): Doping density of the
silicon substrate

iteration_times=10;                          %define the
iteration times

init_upper_bound=10^22;                      %define the
initial upper boundary

init_lower_bound=10^21;                      %define the
initial lower boundary

upper=init_upper_bound;                      %assign the
initial boundaries

lower=init_lower_bound;

%             flag=1;

for n=1:iteration_times

    result(n)=(upper+lower)/2;             %use array to
record the result
```

```
    LEFT=result(n);                          %left side of
the equation


RIGHT=(4/A_MOSC^2)*(k_B*T/q^2)*(1/(p_Vaccum*p_Si))*(((1/C
_min)-(1/C_max))^(-2))*log(result(n)/ni_Si);   %right
side of the equation

    if(LEFT>RIGHT)                           %in this
situation the value of NA is too large, the solution
should smaller than this value

        upper=result(n);                     %assign the
new upper boundary

    else if(LEFT<RIGHT)                      %in this
situation the value of NA is too small, the solution
should larger than this value

            lower=result(n);                 %assign the
new lower boundary

%          else if((LEFT==RIGHT)&&flag)
%the equation holds, this is the final solution

%            fprintf('the result will not change any more
after %d times iteration\n',n); %54 for initial upper
boundary is 10^22 and lower boundary is 10^21

%            flag=0;

%          end

        end

    end

end


N_A=result(iteration_times);

%fprintf('The doping density of the silicon substrate is
%g \n',N_A);

x=1:iteration_times;
```

```
for i=1:iteration_times

reference(i)=NA;

end

figure,plot(x,result,'-b',x,reference,'-r');

xlabel('Iteration times n');

ylabel('Doping density of the silicon substrate NA(m^-
3)');

title('Using initial approximation and bisection method
to solve the transcendental equation');


%Task5: Work function difference

phi_FS = k_B*T/q*log(NA/ni_Si);

PHI_S = Chi_Si + Eg_Si/2 + k_B*T/q*log(NA/ni_Si);

PHI_AuS = PHI_Au - (Chi_Si + Eg_Si/2 +
k_B*T/q*log(NA/ni_Si));

fprintf('The Fermi potential of the semiconductor
substrate is %fV \n', phi_FS);

fprintf('The work function the semiconductor substrate is
%feV \n', PHI_S);

fprintf('The work function difference between the Au gate
and the semiconductor substrate is %feV \n', PHI_AuS);

%Task 6 flatband voltage

Vt=0.025;

L_d=sqrt((p_Vaccum*p_Si*Vt )/(q*N_A));

C_d1=(p_Vaccum*p_Si)/L_d;

C_d=C_d1*A_MOSC;

C_total=((C_ox*C_d)/(C_ox+C_d));
```

```
fprintf('The equivalent capacitance at flatband condition
is %gF \n',C_total);

V_fb=CV_search(C_total,Table.C,Table.V);

fprintf('The flatband voltage is %gV \n',V_fb);

%Task7: midgap voltage

C_dep_mg=sqrt(q*N_A*p_Vaccum*p_Si/(2*phi_FS))*A_MOSC;%in
mid_gap situation phi_FS=PHI_S

C_mg=C_ox*C_dep_mg/(C_ox+C_dep_mg);
%total capacitance at midband

V_midgap=CV_search(C_mg,Table.C,Table.V);            %use
CV_search function find the corresponding voltage

fprintf('The equivalent capacitance at midgap condition
is %gF \n',C_mg);

fprintf('The midgap voltage is %fV \n',V_midgap);

%Task 8

Q_ox=((-C_ox)*(V_fb-PHI_AuS)/(A_MOSC*10^4));

N_ox=Q_ox/q;

V_G=(p_Si/p_ox)*t_SiOx*sqrt((2*q*N_A*phi_FS)/p_Vaccum*p_S
i)+phi_FS+PHI_AuS;

D_V=V_G-V_midgap;

Q_ox2=(C_ox*D_V)/(A_MOSC*10^4);

N_ox2=Q_ox2/q;

Q_flatband=N_ox*A_MOSC;

Q_midgap=N_ox2*A_MOSC;

Charge_FB=N_ox*(A_MOSC/10^4);

Charge_MD=N_ox2*(A_MOSC/10^4);

fprintf('The oxide charges at flat-band condition is
%gC/cm^-2 \n',N_ox);
```

```
fprintf('The oxide charges at mid-gap condition is
%gC/cm^-2 \n',N_ox2);

fprintf('The charges at flat-band condition is %gcm^-2
\n',Charge_FB);

fprintf('The charges at mid-gap condition is %gcm^-2
\n',Charge_MD);

%Task 10

FAI_S=-0.28;%define the initial value of the surface
potential

for a=1:121

E_s_L(a)=sign(FAI_S)*sqrt(4*q*ni_Si*Vt*(cosh((FAI_S-
phi_FS)/Vt)+(FAI_S/Vt)*sinh(phi_FS/Vt)-
cosh(phi_FS/Vt))/(p_Vaccum*p_Si)); %(3.10.17)

E_s_H(a)=sign(FAI_S)*sqrt((2*q*ni_Si*Vt/(p_Si*p_Vaccum))*
((2*FAI_S/Vt)*sinh(phi_FS/Vt)+exp(phi_FS/Vt)*(exp(-
FAI_S/Vt)-1)));%(3.10.18)

Vg_H(a)=(p_Si/p_ox)*t_total*E_s_H(a)+FAI_S+PHI_AuS;
%(3.10.1)(3.10.2)(3.10.3)

Vg_L(a)=(p_Si/p_ox)*t_total*E_s_L(a)+FAI_S+PHI_AuS;
%(3.10.1)(3.10.2)(3.10.3)

C_dd(a)=(A_MOSC*q*ni_Si*sign(FAI_S)/E_s_H(a))*(2*sinh(phi
_FS/Vt)-exp((phi_FS-FAI_S)/Vt));%(3.10.25)

C_LF(a)=A_MOSC*2*q*ni_Si*sign(FAI_S)/E_s_L(a)*abs(sinh((F
AI_S-phi_FS)/Vt)+sinh(phi_FS/Vt));

%(3.10.24)


if abs(FAI_S)<Vt%(3.10.26)

    C_dd(a)=C_d;

    C_LF(a)=C_d;

    Vg_H(a)=PHI_AuS;
```

```
    Vg_L(a)=PHI_AuS;
end
if FAI_S<phi_FS
  %only valid in deep depletion region
    C_dd(a)=C_LF(a);
end
C_min_app=sqrt((q*NA*p_Vaccum*p_Si)/(2*(2*phi_FS+Vt)))*A_
MOSC;
%minimum depletion capacitance

    if C_dd(a)<C_min_app

C_dd(a)=sqrt((q*NA*p_Vaccum*p_Si)/(2*(2*phi_FS+Vt)))*A_MO
SC;
    if(Vg_H(a-1)<2)
    Vg_H(a)=Vg_H(a-1)+0.1;
    else
    Vg_H(a)=Vg_H(a-1);
    end
end
C_total_H(a)=C_ox*C_dd(a)/(C_ox+C_dd(a));%(3.10.22)
C_total_L(a)=C_ox*C_LF(a)/(C_ox+C_LF(a));%(3.10.22)
FAI_S=FAI_S+0.01;
end
figure,plot(Vg_H,C_total_H*10^9,'-
.b',Vg_L,C_total_L*10^9,'--r',Table.V, Table.C*10^-3,'-
g','linewidth',2);
ax = gca;
```

```
ax.YAxisLocation = 'origin';

xlabel('Voltage(V)');

ylabel('Capacitance(nF)');

title('Theoretical HFCV&LFCV plots and experimental
HFCV(consider Au-Si work function difference)');

grid on;

legend('ideal HFCV','ideal LFCV','exp HFCV');

figure,plot(Vg_H-PHI_AuS,C_total_H*10^9,'-.b',Vg_L-
PHI_AuS,C_total_L*10^9,'--r',Table.V, Table.C*10^-3,'-
g','linewidth',2);

ax = gca;

ax.YAxisLocation = 'origin';

xlabel('Voltage(V)');

ylabel('Capacitance(nF)');

grid on;

legend('ideal HFCV','ideal LFCV','exp HFCV');

title('Theoretical HFCV&LFCV plots and experimental
HFCV(assume no work function difference)');

figure,plot(Vg_H-PHI_AuS,C_total_H*10^9,'-
b',Vg_H,C_total_H*10^9,'-r',Table.V, Table.C*10^-3,'-g');

ax = gca;

ax.YAxisLocation = 'origin';

xlabel('Voltage(V)');

ylabel('Capacitance(nF)');

grid on;

legend('assume no work function difference','consider Au-
Si work function difference','exp HFCV');
```

```
title('The effect of work function difference and oxide
charge on HFCV plot');
```