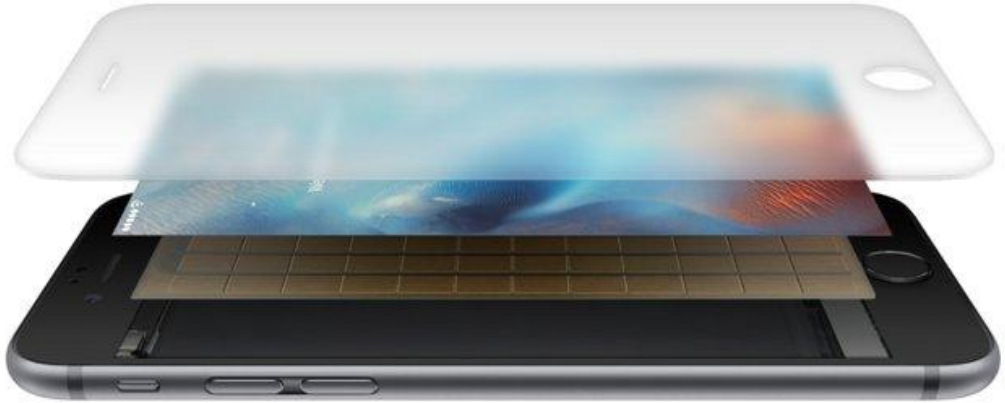
Fabrication of 3D Touch Sensors in OLED Smart Phones

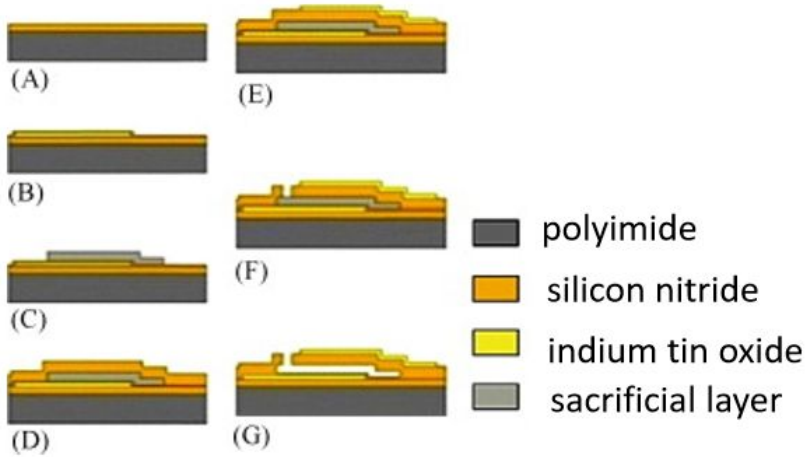


1:00 – 1:15 Wednesday, 12/6/2017

Maximilian Sokoluk, Ka Chun Wong, and Yaxin Zhu

Contents

1. Deposit Si_3N_4 layer
2. Deposit ITO layer as bottom electrode
3. Deposit sacrificial layer with SiO_2
4. Deposit Si_3N_4 sensing membrane
5. Deposit ITO layer as top electrode
6. Make an opening from the top
7. Remove the sacrificial layer



Few points to consider

- Tolerance temperature - continuous use 232 °C (450 °F); short excursions 400 °C (752 °F).
- Find the suitable material to mask the Silicon Nitride
- Set specific rpm for different thicknesses
- Find suitable deposition methods depending on the required layer quality

1. Deposit Si_3N_4 layer by PECVD

- Goal: Deposit a thin silicon nitride layer with the thickness of 500nm on the polyimide layer using PECVD

$$SiH_4 + 4NH_3 \rightleftharpoons Si(NH_2)_4 + 4H_2$$

$$3Si(NH_2)_4 \rightleftharpoons Si_3N_4 + 8NH_3$$

- Comparisons
  - LPCVD: high temperature (550-600 ℃)
  - Evaporation: no good for composites

1. Deposit Si_3N_4 layer by PECVD

- Substrate Temperature: 150 ℃
- Radio frequency: 13.6MHz
- Power: 40W
- Chamber Pressure: 600 mTorr
- Gas rate: $SiH_4 : NH_3 : N_2 = 1:10:20$
- Deposition rate: 6 nm/min

Table 1
PECVD conditions

Parameter	Value
Gas flow ratio: $SiH_4/NH_3/N_2$	1/10/20
Substrate temperature (°C)	125, 150, 200, 300
Radio frequency (RF), Power (W)	40, 120, 200
Chamber pressure (mTorr)	200, 600
Radio frequency (MHz)	13.6

Table 2
Mechanical properties of PECVD thin films under various deposition conditions

Substrate temperature (°C)	RF power (W)	Chamber pressure (mTorr)	Film thickness (nm)	Density (Mg/m^3)	Elastic modulus (GPa)	Hardness (GPa)
125	120	600	600, 1195	2.2 ± 0.2	106.8 ± 2.5	11.9 ± 0.5
150	120	600	650	2.3 ± 0.2	124.8 ± 2.5	13.5 ± 0.4
200	120	600	605, 1190	2.6 ± 0.3	140.2 ± 3.4	15.6 ± 0.7
300	120	600	585	2.8 ± 0.3	198.1 ± 1.8	22.1 ± 0.5
150	40	600	595	2.0 ± 0.2	110.6 ± 2.2	11.4 ± 0.7
150	200	600	1210	2.4 ± 0.2	130.3 ± 2.1	14.4 ± 0.6
150	120	200	715	2.5 ± 0.3	142.1 ± 1.8	15.4 ± 0.6

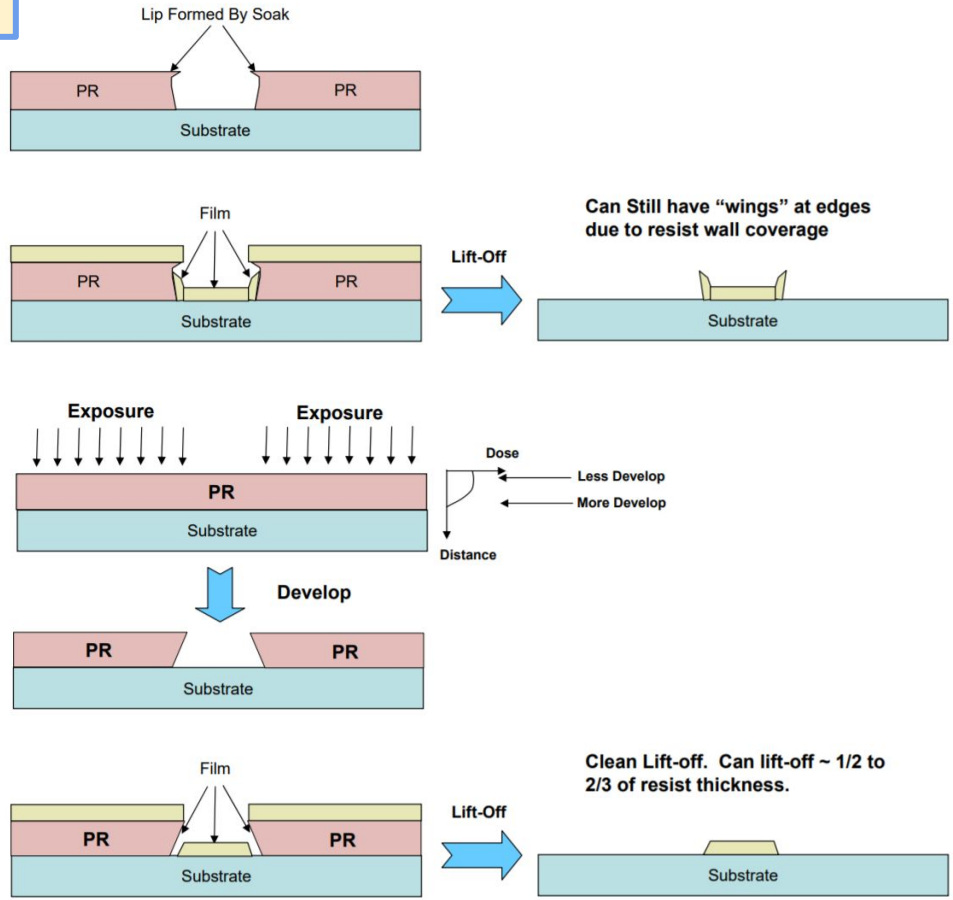
Huang, Han, et al. Materials Science and Engineering, 2006

2. Deposit ITO layer as bottom electrode

- Goal: deposite 50 nm thick, 5um wide ITO layer
- Steps
  - Pattern the photoresist
  - Lift Off: ITO deposition with E-beam evaporation ; Clean the photoresist by acetone
- Comparison: sputtering, lithography, etching

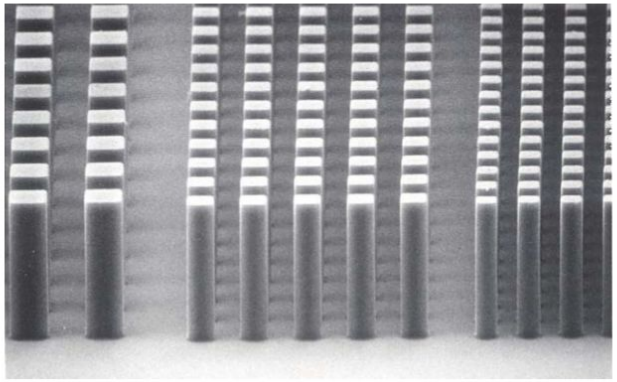
2.1 Pattern the photoresist

1. Positive PR will have the “wings” at edge;
2. Negative PR is good.



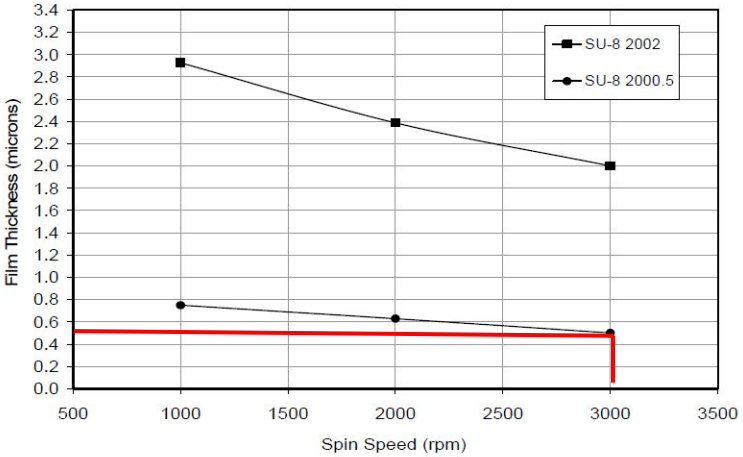
2.1 Pattern the photoresist

- Goal: deposit Negative Photoresist with 500 nm
- Type: SU-8 2000.5
- Light Source: UV (350-400 nm), (i-line 365 nm recommended)
- Spin Rate : 3000 rpm, 30 sec



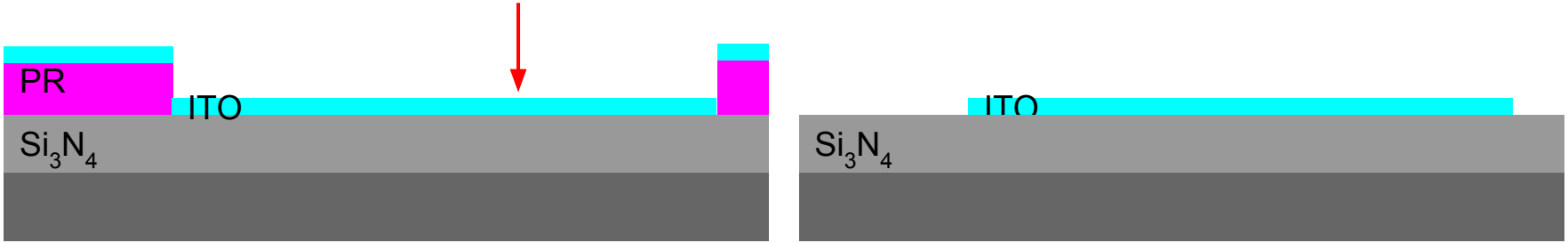
10 um features, 50 um SU-8 2000 coating

Figure 1.a. SU-8 2000 Spin Speed vs. Thickness



2.2 Lift-off

- Steps:
  - ITO deposition with E-beam evaporation
  - Clean the photoresist by acetone
- Comparison: Sputtering (better for uniform coating)



3. Deposit sacrificial layer-SiO_2 by PECVD

- Goal: deposit a silicon oxide layer with the thickness of 800 nm on the device using PECVD

3. Deposit sacrificial layer-SiO_2 by PECVD

- Substrate Temperature: 200 ℃
- Power: 75W
- Gas: Tetraethoxysilane (TEOS)

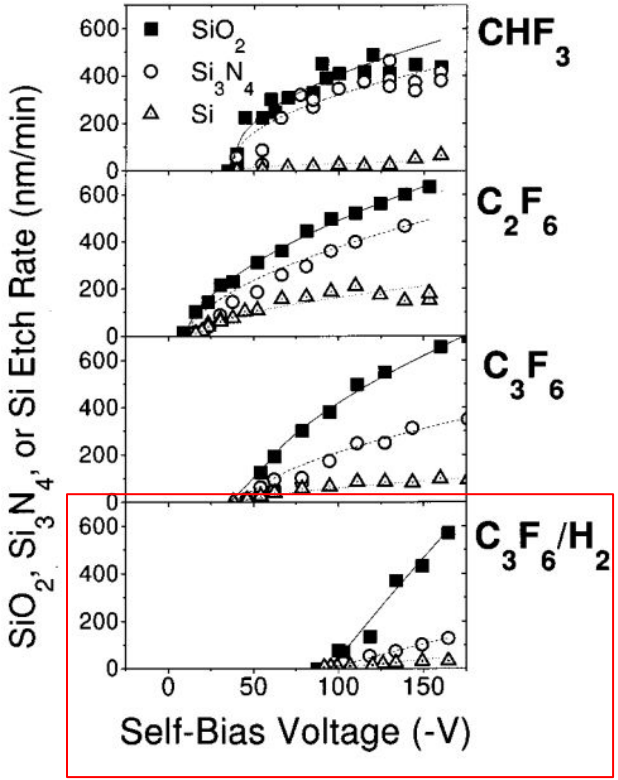
Table 1
Deposition parameters and properties of the deposited SiO_2 films

TEOS (sccm)	Microwave power (W)	Sample temperature (°C)	Deposition rate (nm/min)	Final thickness (nm)	Void in the SiO_2 (%)	Refractive index ($\lambda = 633$ nm)	Etch chemical rate (nm/min)	XPS Stoichiometry O/Si	XPS at.% C/O
2.5	75	200	2.45 ± 0.1	79 ± 0.5	-0.5 ± 0.2	1.459 ± 0.001	16.0 ± 0.2		
2.5	75	200	2.50 ± 0.1	108 ± 0.1	0.07 ± 0.2	1.456 ± 0.001		2.18 ± 0.5	2.03 ± 1.0
3.75	75	200	4.43 ± 0.1	153 ± 0.5	-1.3 ± 0.2	1.463 ± 0.001	13.6 ± 0.2		
5	75	200	6.88 ± 0.1	168 ± 0.5	-1.0 ± 0.2	1.462 ± 0.001		2.00 ± 0.5	0.34 ± 1.0
2.5	100	200	3.16 ± 0.1	116 ± 0.5	-0.3 ± 0.2	1.458 ± 0.001	15.5 ± 0.2	2.08 ± 0.5	1.05 ± 1.0
2.5	75	350	2.10 ± 0.1	87 ± 0.5	-0.1 ± 0.2	1.457 ± 0.001			
Thermal oxide					0 ± 0.2	1.457 ± 0.001	6.5 ± 0.2		

C. Martinet Département de Physico-chimie des Matdriaux, 2010

3. RIE Etching

- Substrate Temperature: 150 ℃
- Radio frequency: 13.6MHz
- Power: 1400W
- Voltage: 150V
- Chamber Pressure: 6 mTorr
- Gas ratio: $C_3F_6/H_2 = 11:3$



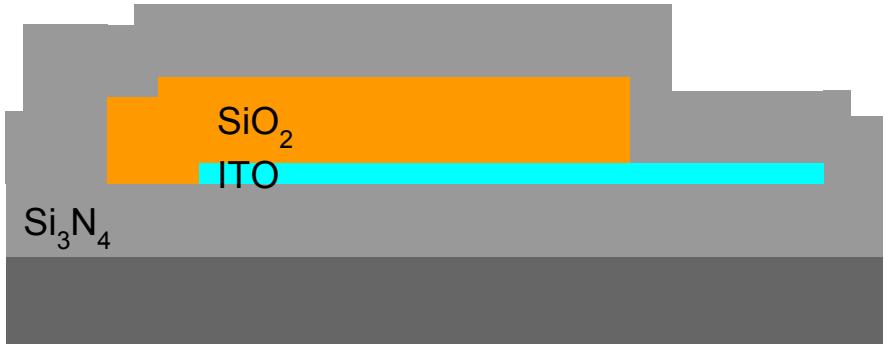
M. Schaepkens, et al. State University of New York

4. Deposit Si_3N_4 sensing membrane

- Goal: deposit a thin silicon nitride layer with the thickness of 500nm on the device using PECVD

$$SiH_4 + 4NH_3 \rightleftharpoons Si(NH_2)_4 + 4H_2$$

$$3Si(NH_2)_4 \rightleftharpoons Si_3N_4 + 8NH_3$$



Huang, Han, et al. Materials Science and Engineering, 2006

4. Deposit Si_3N_4 sensing membrane

- Substrate Temperature: 150 ℃
- Radio frequency: 13.6MHz
- Power: 40W
- Chamber Pressure: 600 mTorr
- Gas ratio: $SiH_4 : NH_3 : N_2 = 1:10:20$

Table 1
PECVD conditions

Parameter	Value
Gas flow ratio: $SiH_4/NH_3/N_2$	1/10/20
Substrate temperature (°C)	125, 150, 200, 300
Radio frequency (RF), Power (W)	40, 120, 200
Chamber pressure (mTorr)	200, 600
Radio frequency (MHz)	13.6

Table 2
Mechanical properties of PECVD thin films under various deposition conditions

Substrate temperature (°C)	RF power (W)	Chamber pressure (mTorr)	Film thickness (nm)	Density (Mg/m^3)	Elastic modulus (GPa)	Hardness (GPa)
125	120	600	600, 1195	2.2 ± 0.2	106.8 ± 2.5	11.9 ± 0.5
150	120	600	650	2.3 ± 0.2	124.8 ± 2.5	13.5 ± 0.4
200	120	600	605, 1190	2.6 ± 0.3	140.2 ± 3.4	15.6 ± 0.7
300	120	600	585	2.8 ± 0.3	198.1 ± 1.8	22.1 ± 0.5
150	40	600	595	2.0 ± 0.2	110.6 ± 2.2	11.4 ± 0.7
150	200	600	1210	2.4 ± 0.2	130.3 ± 2.1	14.4 ± 0.6
150	120	200	715	2.5 ± 0.3	142.1 ± 1.8	15.4 ± 0.6

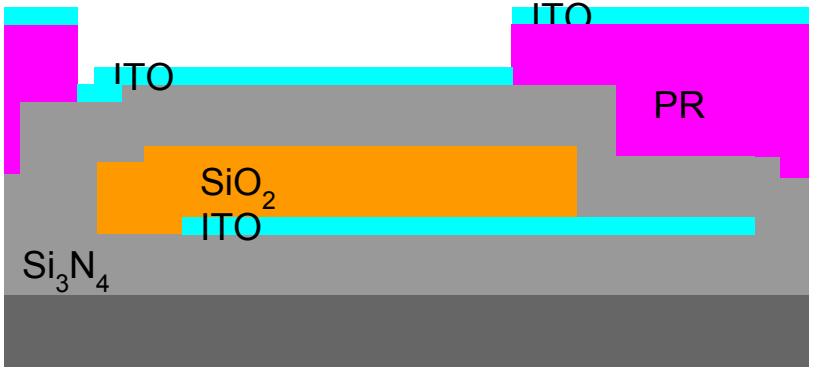
Huang, Han, et al. Materials Science and Engineering, 2006

5. Deposit ITO layer as top electrode

- Goal: deposit a thin ITO layer with the thickness of 50nm on the device using Electron Beam Evaporation / Lift Off

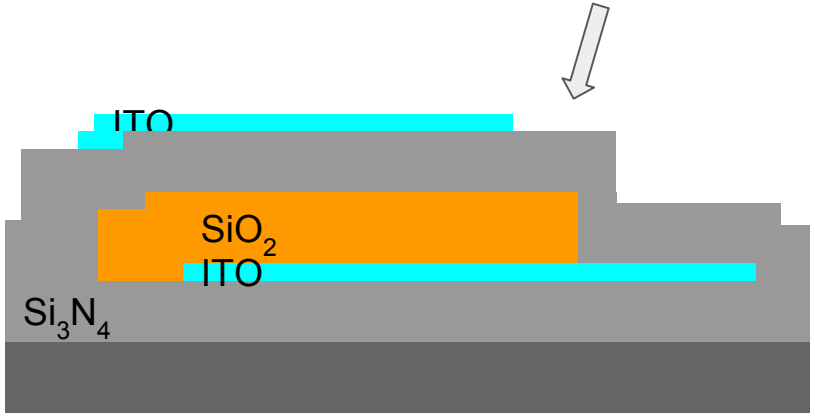
5. Deposit ITO layer as top electrode

- Steps
  - Electron Beam Evaporation the ITO layer with 50 nm thickness and 8 um wide
  - Remove the photoresist by acetone



6. Fabricate release hole in Si_3N_4

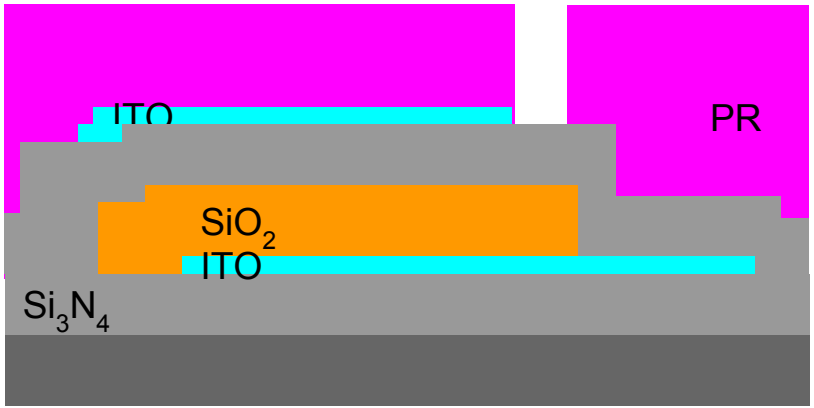
- Steps: fabricate hole in sensing membrane to release sacrificial Silicon Oxide layer

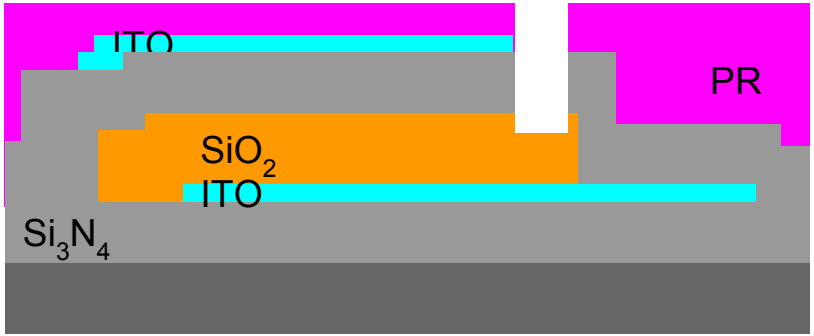


6. Fabricate release hole in Si_3N_4

- Spin coat Olin Hunt 6512
- RPM: 1000 - 2000
- Thickness: 500 nm

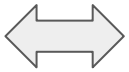
- RIE settings: 200W, gap= 2.6 mm 13.56Hz, 200 ℃
- Gas: CF_2+CHF_3+He (10:5:10 sccm)
- Etch rate: 130 nm/sec
- 13s etching





7. Remove the sacrificial layer

- HNA wet etch
- SiO_2 etch rate: 30 nm/min
- Etches nitride



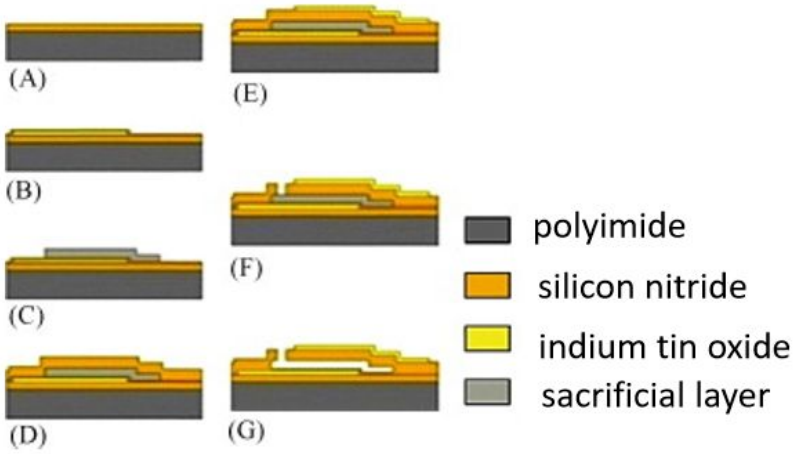
- HF Vapor
- SiO_2 etch rate: 40 nm/s
- Thickness: 500 nm

Reference

1. Huang, Han, et al. "Effect of deposition conditions on mechanical properties of low-temperature PECVD silicon nitride films." Materials Science and Engineering: A 435 (2006): 453-459.
2. C. Martinet, V. Paillard, A. Gagnaire, J. Joseph, Deposition of SiO2 and TiO2 thin films by plasma enhanced chemical vapor deposition for antireflection coating, In Journal of Non-Crystalline Solids, Volume 216, 1997, Pages 77-82
3. J Buhler, F-P Steiner and H Baltes “Silicon dioxide sacrificial layer etching in surface micromachining” J. Micromech. Microeng. 7 (1997) R1–R13
4. Kirt R. Williams, Kishan Gupta, and Matthew Wasilik “Etch Rates for Micromachining Processing—Part II” JOURNAL OF MICROELECTROMECHANICAL SYSTEMS, VOL. 12, NO. 6, DECEMBER 2003
5. M. Schaepkens, et al. “Study of the SiO2-to-Si3N4 etch selectivity mechanism in inductively coupled fluorocarbon plasmas and a comparison with the SiO2-to-Si mechanism”. State University of New York, Albany, New York 1998
6. Karabacak T, Zhao Y P, Wang G C, et al. Growth front roughening in silicon nitride films by plasma-enhanced chemical vapor deposition[J]. Physical Review B, 2002, 66(7): 075329.

Thank you!

Q&A



The goal of the project is to develop a process to fabricate a microscale 3D touch based on polymer materials used in the OLED circuitry. The fabrication process is shown schematically above. The sensing membrane is made of silicon nitride (SiN_x) while the top and bottom electrodes are made of indium tin oxide (ITO). (A) The fabrication process starts by covering a polyimide substrate with a 500 nm-thick of SiN_x layer. (B) A 50 nm-thick and 5 μm-wide ITO layer is fabricated as a bottom electrode. (C) An 800 nm-thick and 5 μm-wide sacrificial layer is fabricated. (D) A 500 nm-thick top SiN_x sensing membrane is fabricated. (E) A 50 nm-thick and 8 μm-wide ITO layer is fabricated as a top electrode. (F) A hole with a diameter of 500 nm is fabricated via the top SiN_x layer. (G) The sacrificial layer is removed.