Engineering Portfolio

Engineer Information:

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Portfolio Access on Github:

https://github.com/YaxinDeng/Engineering-Portfolio

Project Lists:

Fully Synthesizable NoC Verilog-based Multi-core System

Abstract:

This project is designed and implement Verilog based for 3x3 mesh network with credit-based flow control under dimension order routing algorithm. Current progress is editing the processing element nodes, designing instruction fetch stage, and implementing the performance for NoC with parallel programming application.

Principle modules (including FIFO, Round Robin, CRC, Sequence Detector, SIPO, PISO etc.) in behavioral level are presenting by using NCSIM and QuestaSim, and design system from spec down to gdsII format. The current step is achieve on some principle parts for pre-synthesis, and using Innovus for post-synthesis generating.

Sample code for FIFO:

```verilog
module FIFO1 #(parameter WIDTH = 8,
            parameter DEPTH = 16,
            parameter WIDTH_ptr = 5)(
        input rclk,
        input wclk,
        input reset,
        input put,
        input get,
        input [WIDTH-1:0]data_in,
        output  empty_bar,
        output  full_bar,
        output reg [WIDTH-1:0]data_out);

//Dual-Port RAM register: 16x8
reg [WIDTH-1:0] Data [0:DEPTH-1];
wire full, empty;

//pointer for the read and write
reg [WIDTH_ptr-1:0] rd_ptr; //initial read pointer address
reg [WIDTH_ptr-1:0] wr_ptr; //inital write pointer address
reg [WIDTH_ptr-1:0] rd_ptr_s;   //receive in a graycode style
reg [WIDTH_ptr-1:0] wr_ptr_s;   //receive in a graycode style
reg [WIDTH_ptr-1:0] rd_ptr_ss;  //double sync
reg [WIDTH_ptr-1:0] wr_ptr_ss;  //double sync

//prt graycode calculation:
wire [WIDTH_ptr-1:0]rd_ptr_gray;
wire [WIDTH_ptr-1:0]wr_ptr_gray;

//[Read Domain]consider update the rd_ptr & transfer the binary code to gray code
always @ (posedge rclk, posedge reset)begin
    if (reset == 1'b1)
        rd_ptr <= 0;
    else if (get == 1'b1 && empty == 1'b0)
        rd_ptr <= rd_ptr +1'b1;
    else
        rd_ptr <= rd_ptr;
end
    assign rd_ptr_gray = (rd_ptr>>1)^rd_ptr; //get gray code for input counter

//[Write Domain]consider update the wr_ptr & transfer the binary code to gray code
always @ (posedge wclk, posedge reset)begin
    if (reset == 1'b1)
        wr_ptr <= 0;
    else if (put == 1'b1 && full == 1'b0)
        wr_ptr <= wr_ptr +1'b1;
    else
        wr_ptr <= wr_ptr;
end
    assign wr_ptr_gray = (wr_ptr>>1)^wr_ptr; //get gray code for input counter
```

```verilog
`include "./include/gscl45nm.v"

`timescale 1ns / 1ps
module tb_FIFO1_pnr;
    // Inputs
    reg rclk, wclk, reset, put, get;
    reg [7:0]data_in;
    wire empty_bar, full_bar;
    wire [7:0]data_out;

    FIFO1 UUT (
        .rclk(rclk),
        .wclk(wclk),
        .reset(reset),
        .put(put),
        .get(get),
        .data_in(data_in),
        .empty_bar(empty_bar),
        .full_bar(full_bar),
        .data_out(data_out));


//test for case 1: 60 MHz for rclk, and 30 MHz for wclk
    initial begin
        rclk = 0;
        forever #8.3333  rclk=!rclk;
    end

    initial begin
        wclk = 0;
        forever #16.6667 wclk=!wclk;
    end

    initial begin
        data_in = {$random} % 255;
        put = 0;
        get = 0;
        reset = 1;
        #155;

        //resting pure write function
        reset = 0;

        repeat(17) begin
            data_in = {$random} % 255;
            put = 1;
            #50;

            data_in = {$random} % 255;
            put = 0;
            #50;
        end
```

Figure 1.1. FIFO module and testbanch on Verilog

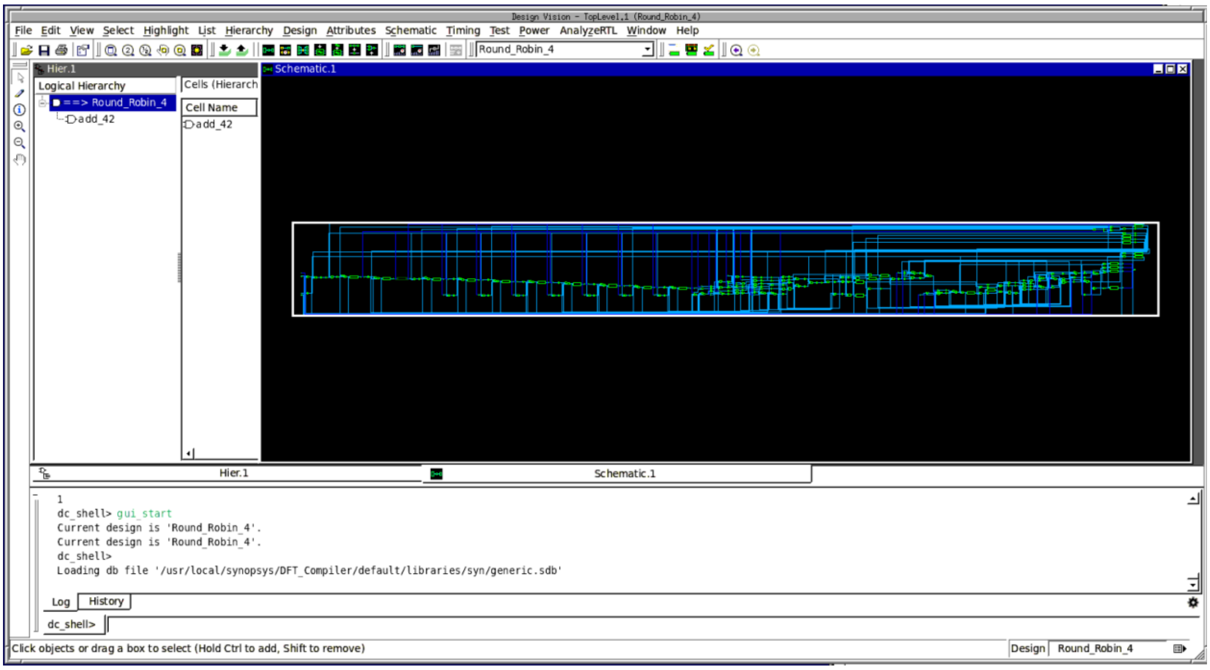


Figure 1.2. NCsim synthesis schematic

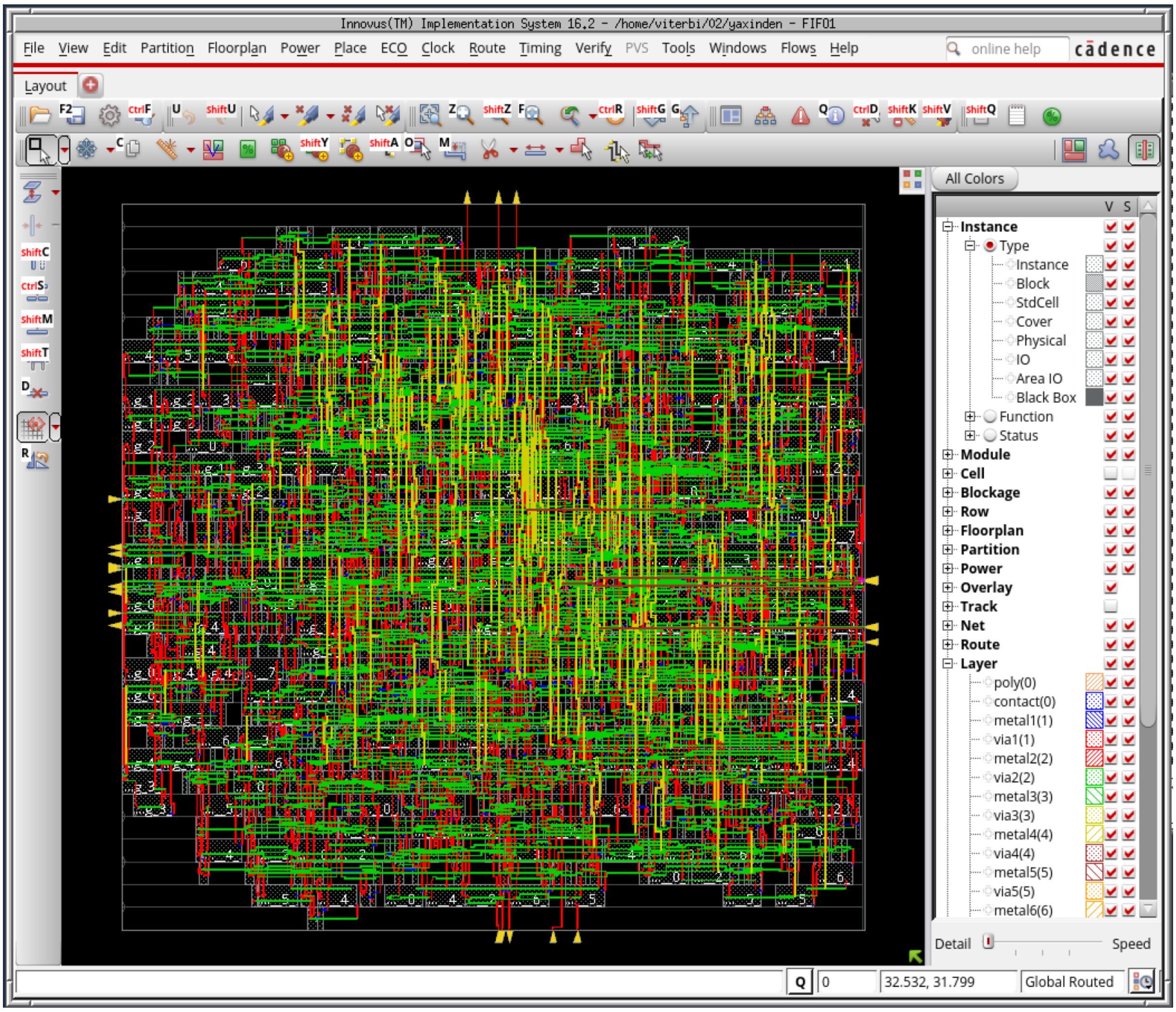


Figure 1.3. Innovus

General Purpose CPU

Abstract:

This Project is desire to design a 5 stage MIPs pipeline architecture CPU with Out of Order execution Instruction. There are five stages in the pipeline structure of this project, namely, IF, ID, EX, MEM, and WB. This project is working from two tracks: a full custom design under 45nm technology under Cadence Virtuoso, and a Verilog design direction by using QuestaSim, NCSIM, and Innovus.

Cadence Virtuoso Base design presenting a 1.25GHz CPU with full custom principle circuit including SRAM, ALU etc. and the Instruction and branch prediction unit is control by Python program. Optimization present mainly in decreasing general average (including dynamic/static) power consumption by clock gating and circuit isolation, and reducing clock cycle by balancing critical path and transistor sizing.

Full Report access through Github link (https://github.com/YaxinDeng/Engineering-Portfolio/blob/master/Projects'%20Report/General%20Purpose%20CPU%20Report.pdf)

Design Overview:

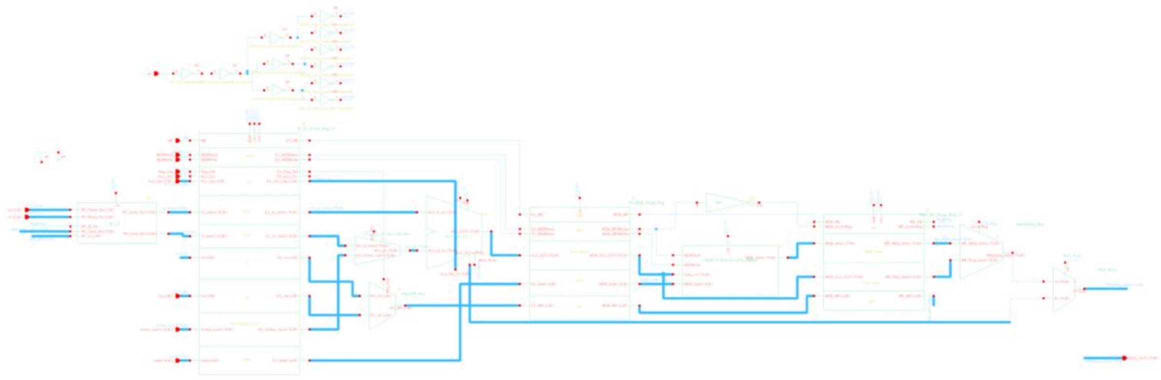


Figure 2.1. General CPU Design Overview

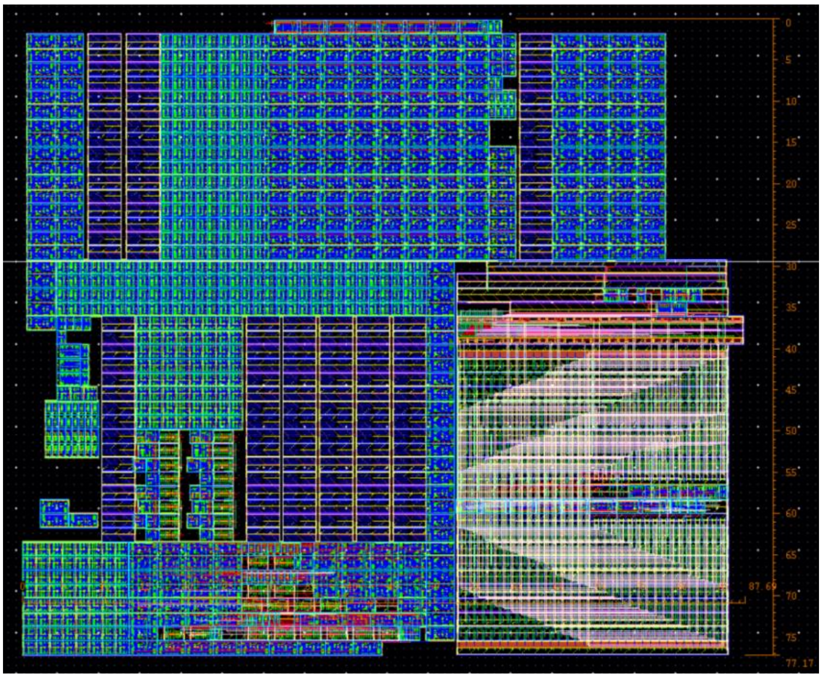


Figure 2.2. General CPU Design Layout Overview

Partial Circuit Present:

ALU Schematic:

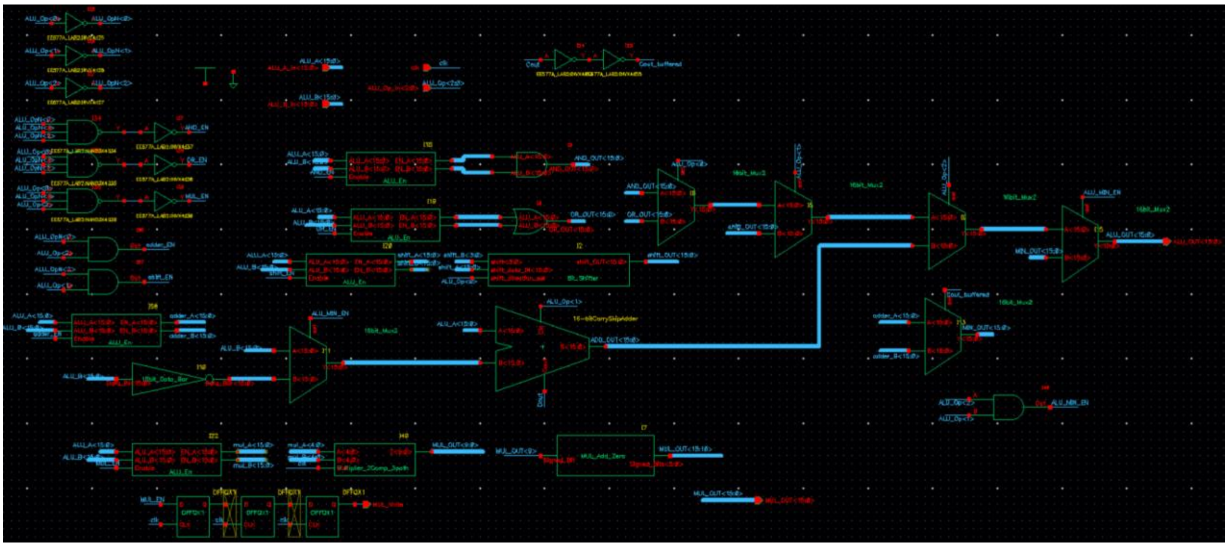


Figure 2.3. ALU design Overview

Mem stage schematic:

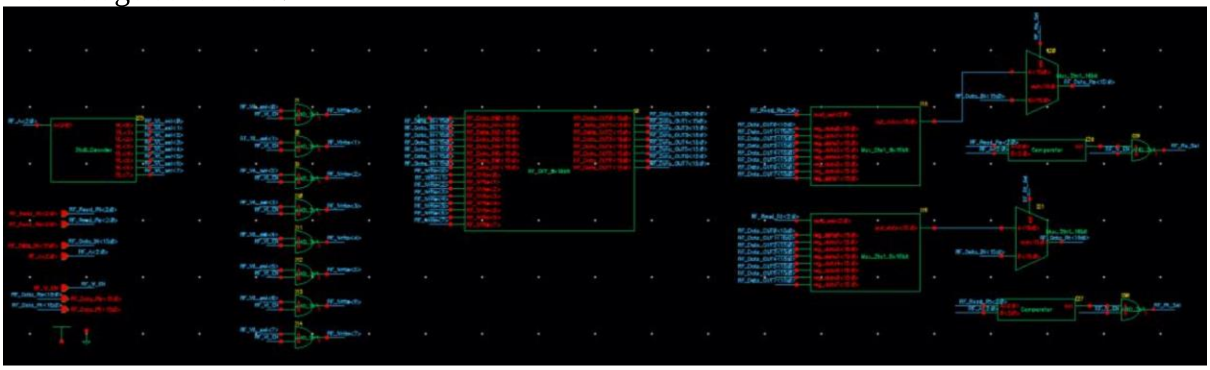


Figure 2.4: Mem stage schematic

Partial Layout:

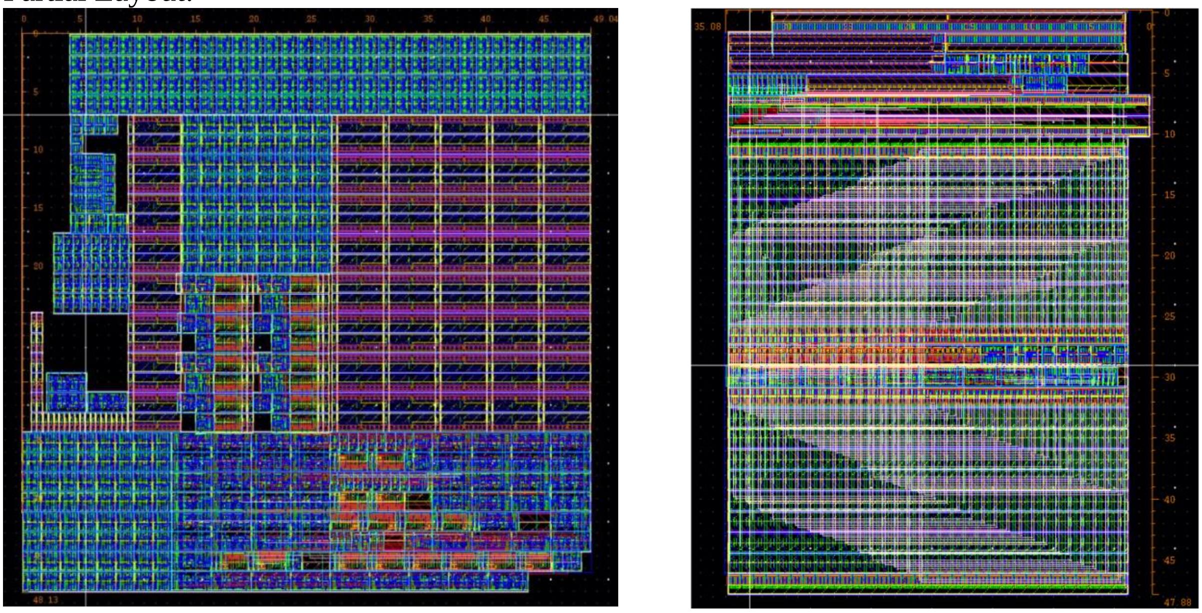


Figure 2.5: Partial layout for ALU and SRAM

Location-Broadcasting Bio-Chips(USC IMedE Lab)

Abstract:

The fundamental goal for this project is to develop a Location-Broadcasting Bio-Chips for localization of microscale devices by embodying the principles of nuclear magnetic resonance in a silicon integrated circuit, and paralleled with PCB level design for algorithm verification. Me and my teammates are designing the system based on the principle for MRI nuclear spinning theory that our professor Monge researching on, and engineered the RF transmitter can encode the location in space by shifting the output frequency in a local magnetic field.

My responsibility in this project is to design a DPLL schematic and layout design for a DPLL under 180-nm technology in Cadence Virtuoso, and do the Altium design by using an ATtiny841 as MCU, and 915MHz transceiver, magnetic sensor, ceramic antenna. Coin battery, voltage regulator, voltage boost converter.

Design Image:

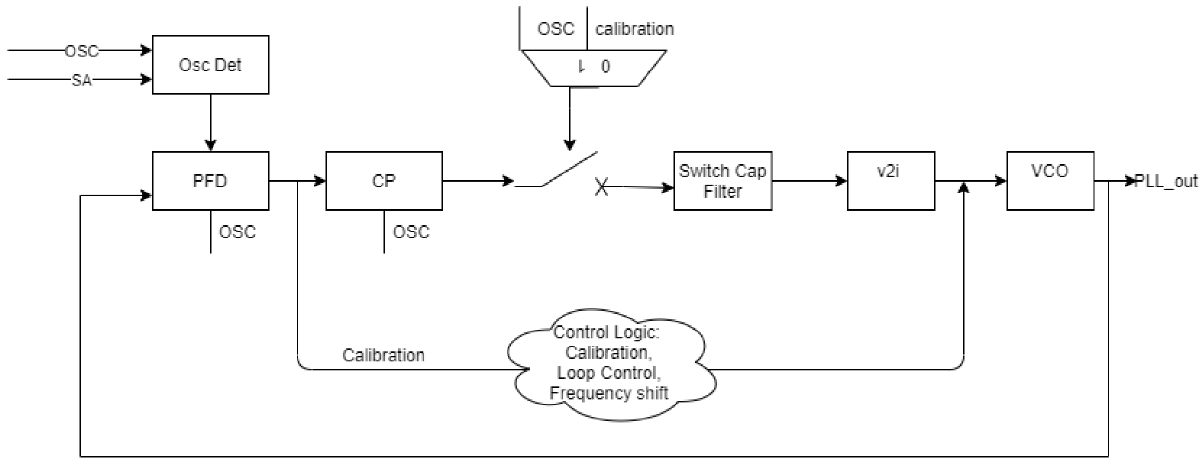


Figure 3.1. Design PDLL Diagram

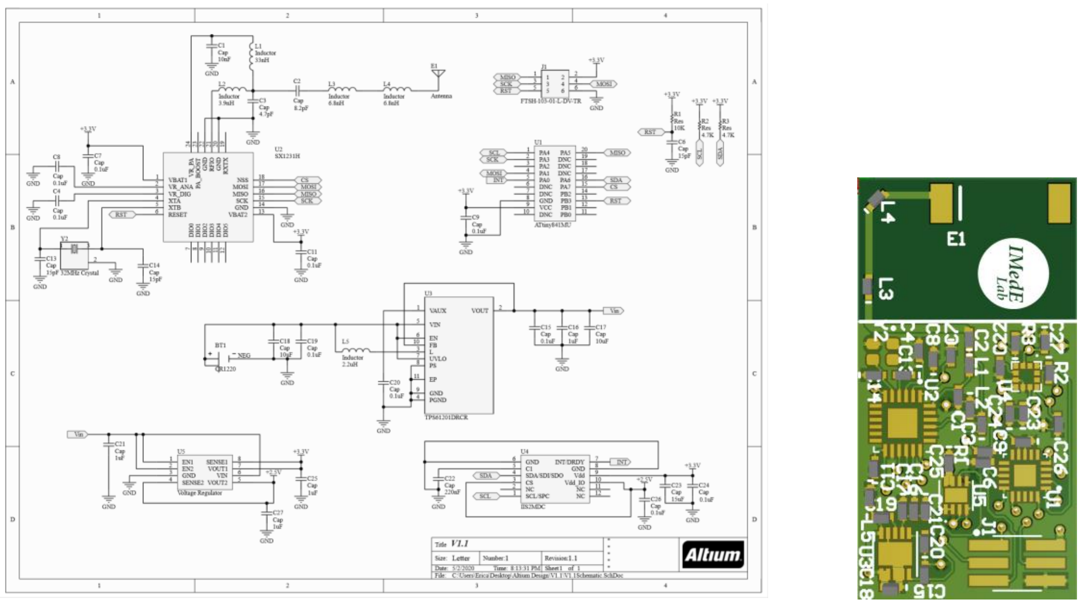


Figure 3.2. Overlook for Schematic and Layout Design

Bubtech - Micro-Nanobubble Wound Healing Medical Device

Abstract:

Bubtech is a dual component system that combines both negative pressure wound therapy and micro-nanobubble technology for removing bacterial on skin surface. With both technologies, our product will provide a steady stream of super-oxygenated fluid to irrigate and aerate the wound through a foam dressing while simultaneously acting as a vacuum to suck up all the debris, fluid, and infected tissue in and around the wound into a waste collection system. The main contribution is customized PCB with ATMega2560 as the microcontroller, designed communicating through FTDI interface, integrated level sensor circuit and relay circuit. Software design for Arduino bootloader style code, Negative feedback loop control, State machine approach, LCD user interface.

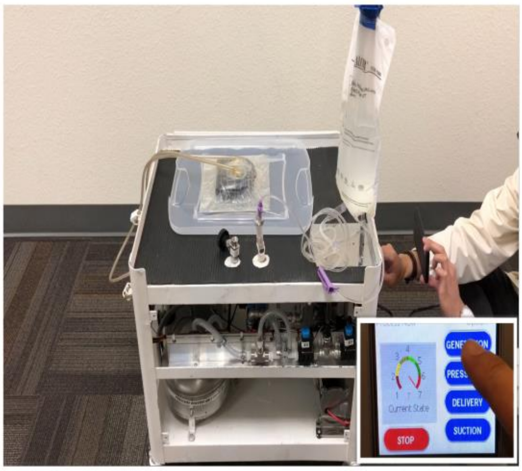


Fig 4.1 Device operated by LCD touch screen

Fig 4.2 Device inner view

Fig 4.3 Device in a close case

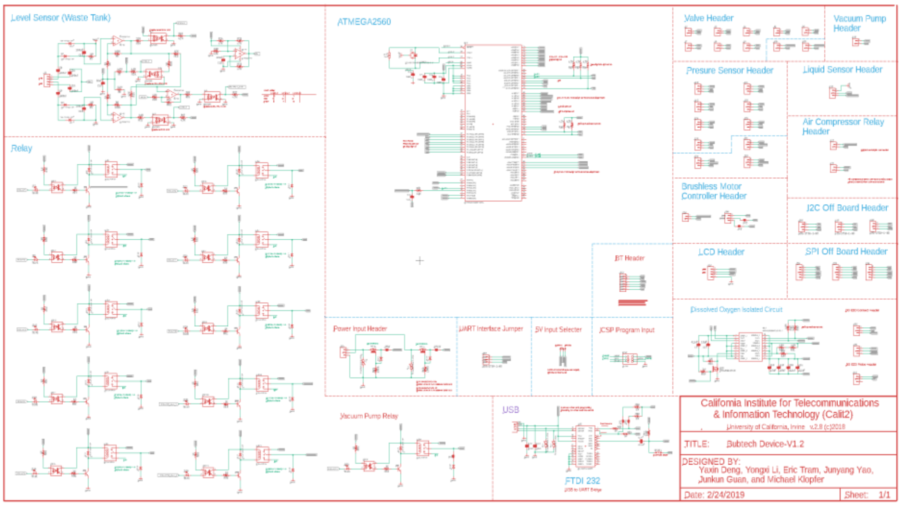
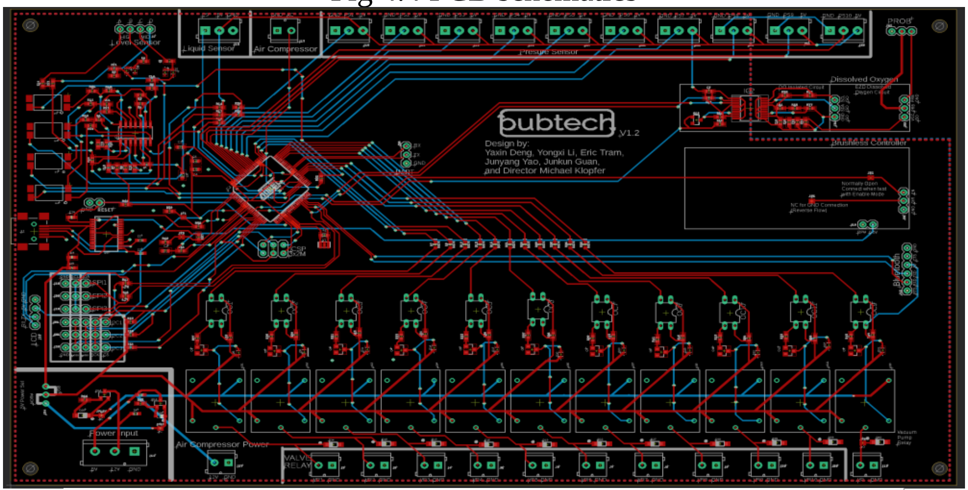


Fig 4.4 PCB schematics



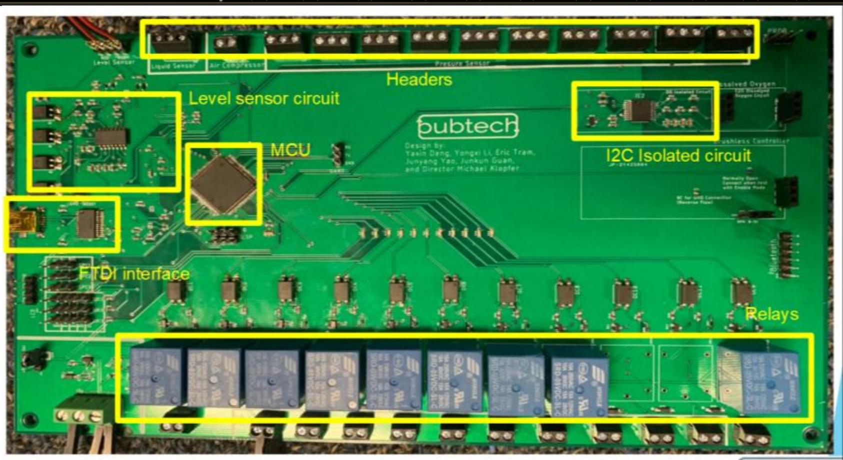


Fig 4.5 PCB layout

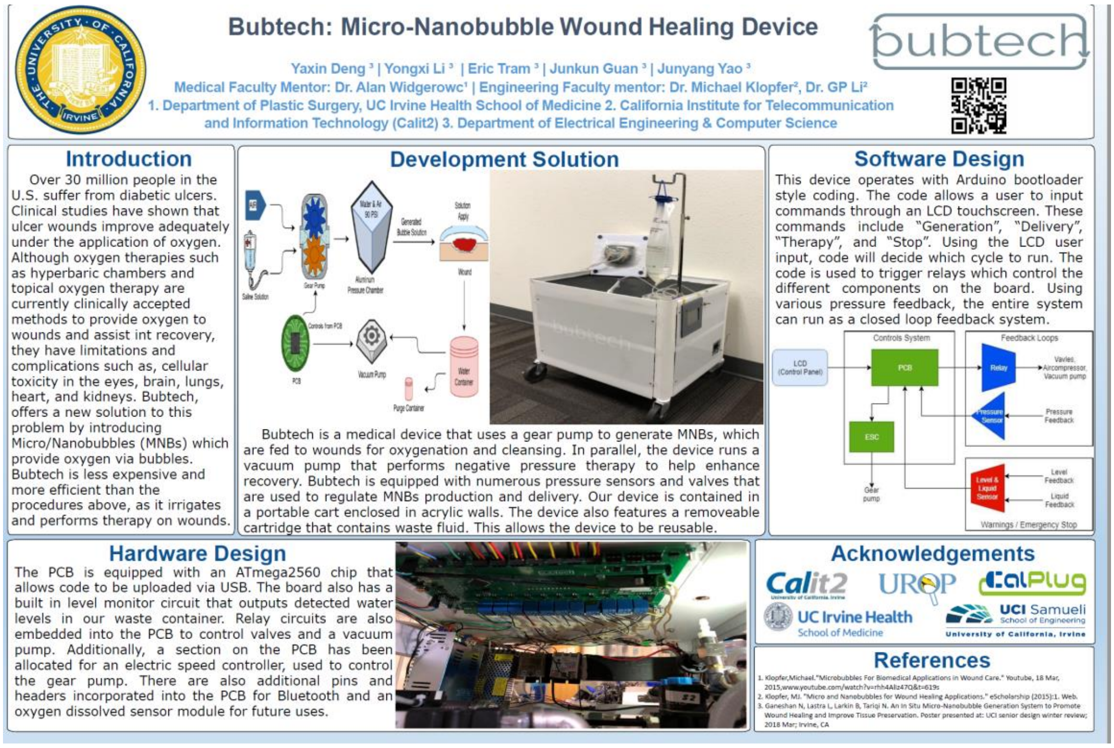


Fig 4.6 Poster

"The idea with Bubtech is several treatments at the bedside over the course of a couple weeks, and you're looking at a high chance of recovery for people with painful open wounds like diabetic ulcers."

"We realized the bubbles could dynamically act like reservoirs for oxygen and provide wound-cleaning properties," says Klopfer. "We explored different balances of oxygen. You can take pure oxygen, or you can balance it with another gas, such as nitrogen or helium, to provide improved healing for different cell types and treatment conditions. The bubble sizing is critical."

Microbubbles exist from 100 microns to about 1 micron (the size of a human hair to smaller than a bacterium). Even tinier nanobubbles range in size from 1 micron down to 50 nanometers (below the wavelength of light) and can be very long lived. Smaller than approximately 50 microns (half the width of a human hair), the bubbles shrink and deliver the contained gas into the surrounding solution. These bubbles attach to surfaces, provide cleaning action and break up biofilms.

When MNBs are produced in water using oxygen or air as gas in their core, their negatively charged surfaces not only prevent them from merging, which would cause them to lose their properties, but help them attract particulate matter and assist in the removal of debris. In addition, MNBs generate free radicals as they shrink, potentially contributing to their antibacterial effects.

One dissertation (Klopfer's), three engineering student-design teams and four years later, Widgerow and Klopfer are on the cusp of clinical trials with a patent pending. A true translational project between medicine and engineering, Bubtech is a dual-component point-of-care system that combines both MNB technology and negative-pressure wound therapy (NPWT). It provides a steady stream of super-oxygenated fluid (bubbles) to irrigate and aerate a wound through a foam dressing secured under a silicone patch. Simultaneously, it acts as a vacuum aspiration system, sucking up all the debris, fluid and infected tissue in and around the wound and depositing the waste into a disposable container.

The Bubtech researchers believe their device will kick-start the healing process, prevent bacterial infection and reduce the time a patient spends in the hospital as well as the cost of treating wounds and further complications that might require surgery.

"I knew wound healing would be a primary indication due to the amazing capability of these bubbles to store and slowly release oxygen," says Widgerow, whose team, headed by Dr. Ross Sayadi and in collaboration with the Beckman Laser Institute, has been conducting animal studies on the technology. "We've used an animal burn wound model and demonstrated dramatically increased wound healing, tissue oxygenation and collagen formation with the bubbled solution as compared to saline alone."

On the CALIT2 side, Klopfer and the engineering students have been working on refining device designs and creating upgrades. Last year's student team, working with Klopfer and UCI biomedical engineering professor Michelle Khine, won the UCI BioENGINE Fellowship Award ($15,000) and a space in Applied Innovation's Wayfinder incubator.

This year's team consists of five electrical engineering students who created a closed-loop control system to ensure patient safety and consistent device performance.

"We make sure at every single stage, the fluid is being generated and delivered correctly," says Yaxin Deng, a fourth-year student and project lead. "Our pressure sensors, relays and valves all need to perform properly to ensure the safety of the device." An LCD touch screen and Bluetooth compatibility allow for easy setup and use, as the proof-of-concept device transitions into an early product.

Approximately 6.5 million Americans suffer from chronic or non-healing wounds, according to the National Institutes of Health. The cost of managing these patients' wounds and related complications exceeds $25 billion per year.

Bubtech would cost less than current treatments, which include negative pressure, cell graft, surgery and hyperbaric oxygen therapy. In addition, it's portable and can be tailored to the patient's needs. Bubtech is a rapid, wound-healing device on wheels that delivers custom-controlled oxygen content to help heal diabetic foot ulcers and a range of other open wounds.

Electrical engineering students (from left) Junyang Yao, Junkun Guan, Yaxin Deng, Yongxi Li and Eric Tram present the current version of the Bubtech wound-healing device at UCI Samueli School of Engineering's 2019 Winter Design Review.

"This would be suited to medevac cases with major soft-tissue injuries in the military as well as other acute burn and chronic wound situations," says Widgerow.

Klopfer is excited to see the device progress. "The idea with Bubtech is several treatments at the bedside over the course of a couple weeks, and you're looking at a high chance of recovery for people with painful open wounds like diabetic ulcers."

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Fig 4.7 Article published in *Interface*

Urology Version 1

This project is to build a prototype device to measures the force level corresponding to urological access sheath to remove the kidney stone and operate other kidney surgeries with by cooperated with UCI Department of Urology Clinical surgery. Allowed MQTT though WIFI communication with Android tablet and documentary testing result in a designing IOS APP.

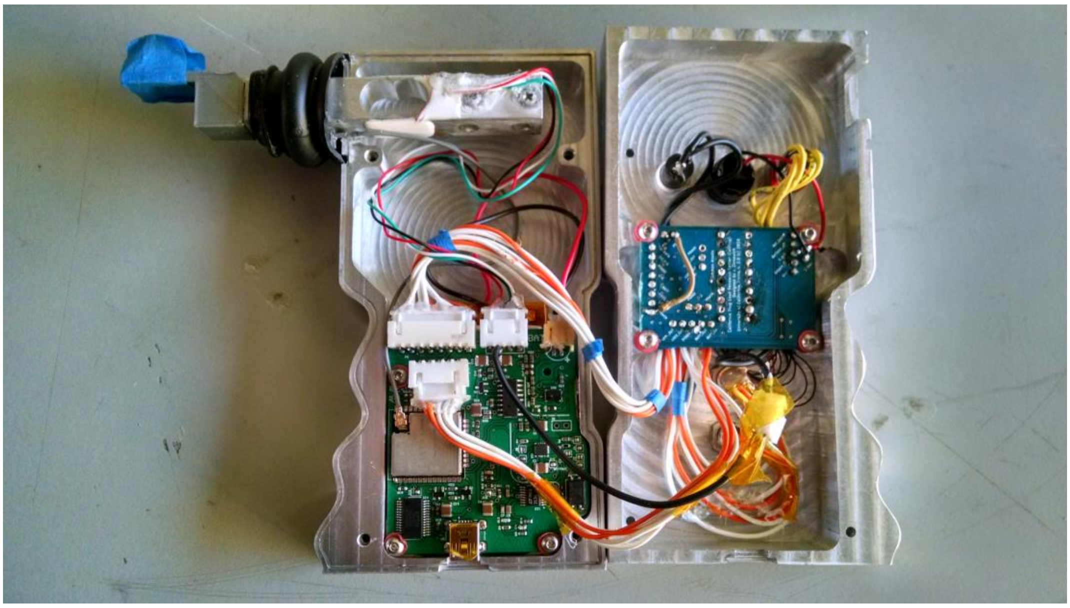


Fig 5.1 Device inner view

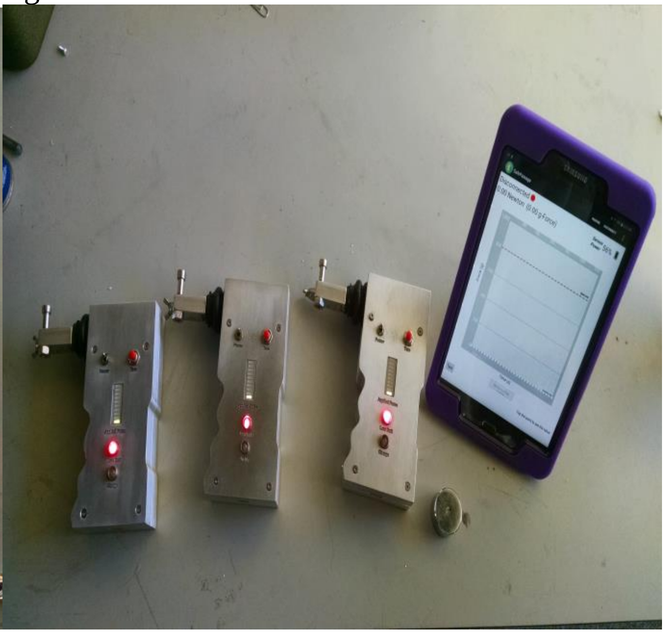


Fig 5.2 Device front view

Fig 5.3 Device with tablet

PCB Schematics:

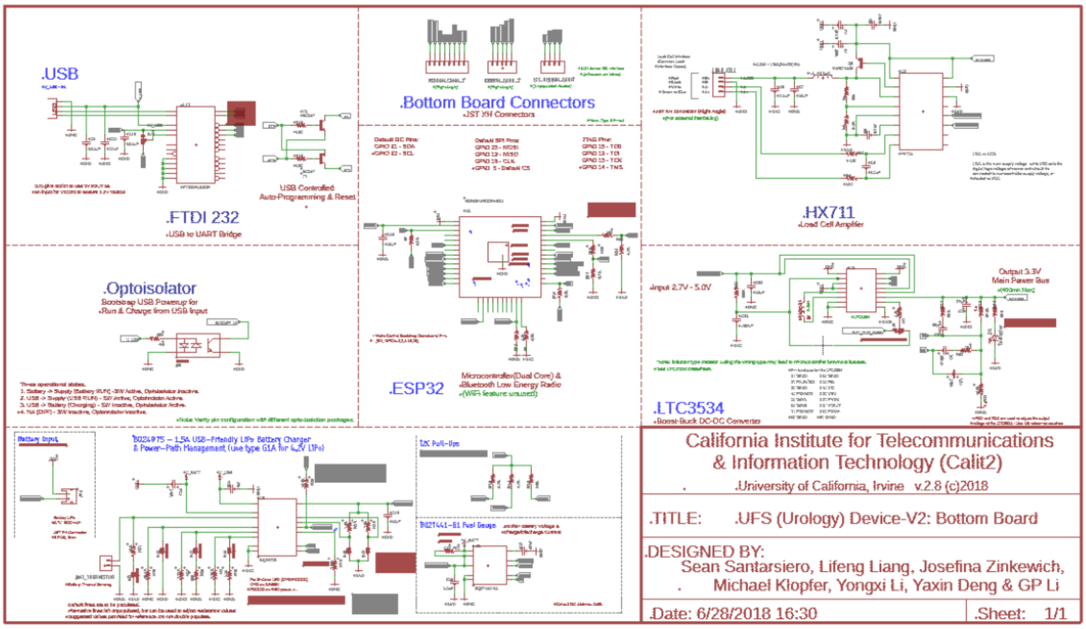


Fig 5.4 Main board schematics

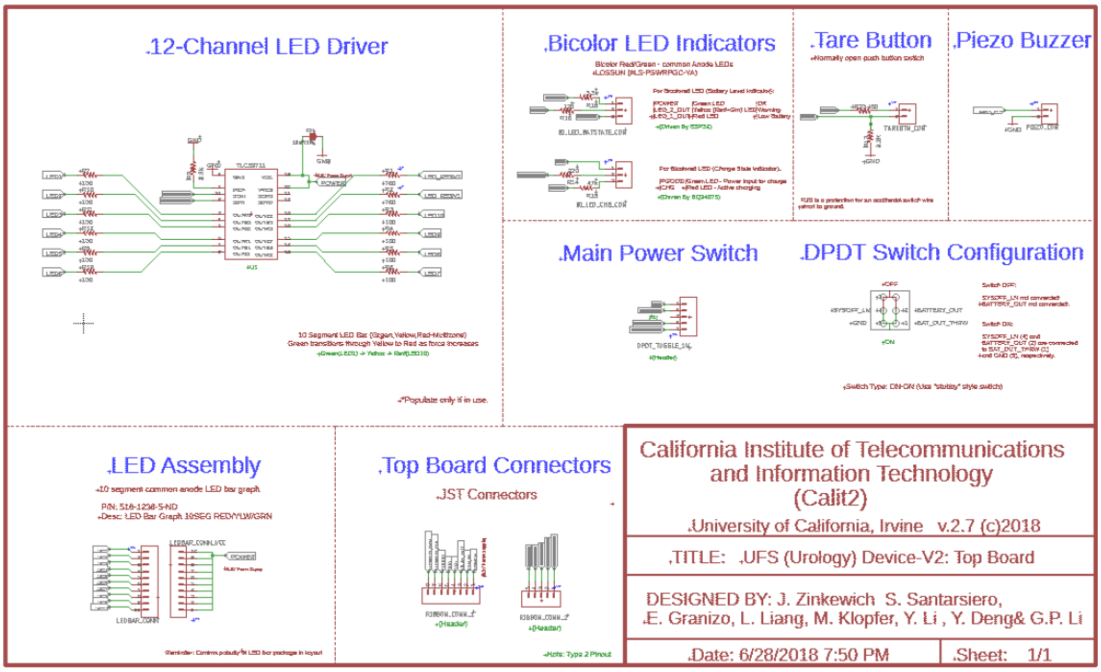


Fig 5.5 Top board schematics

PCB Layout:

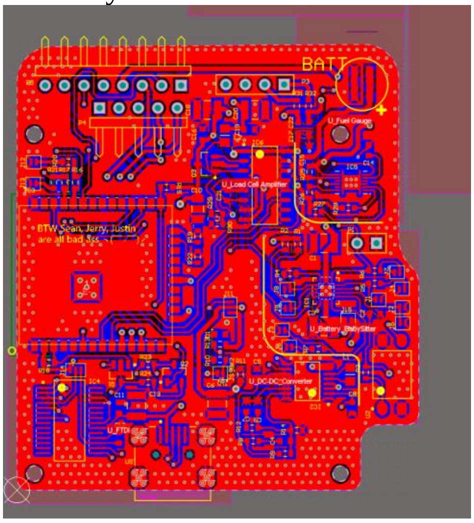


Fig 5.6 Main board layout

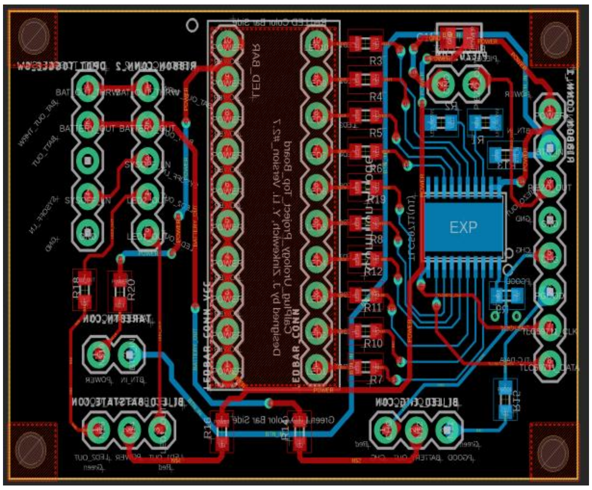


Fig 5.7 Top board layout

Instruction for Users (IFU):

California Plug Pload Research Center

EN

Access Sheath Insertion Force Detection System Instructions For Use

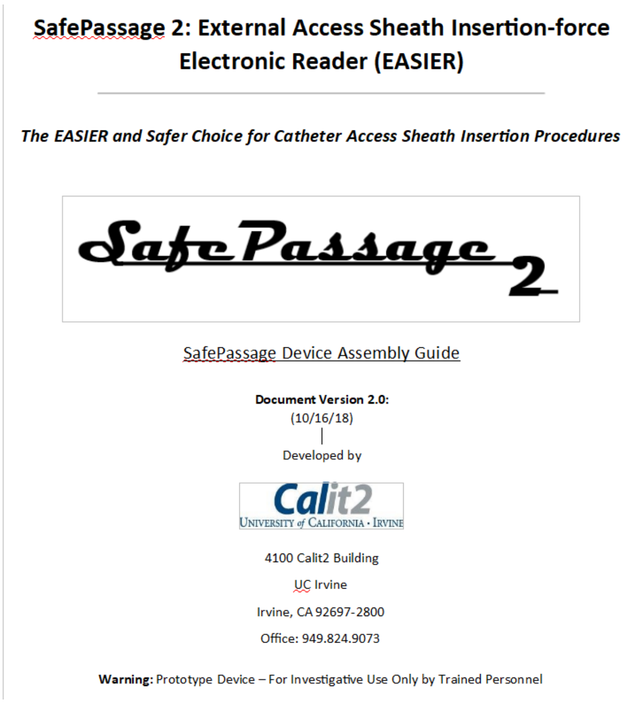
Quick Start

Getting Started:

1. Make sure the device is charged for at least 1hour and 30 minutes for full charge before usage.
2. Turn on the Tablet.
3. Open the Android app "Catheter Sensor graph."
4. Turn on the device and wait for the bottom most LED light indicating the deviced is fully booted.
5. Click the <**Connect**> button on the tablet.
6. Now, choose **"RNBT-XXXX"**, to connect the device.
7. Device is now connected. If the device fails to connect, please refer to "Troubleshooting" section.

Device Operation:

Fig 5.8 First page of IFU



SafePassage 2: External Access Sheath Insertion-force Electronic Reader (EASIER)

The EASIER and Safer Choice for Catheter Access Sheath Insertion Procedures

SafePassage 2

SafePassage Device Assembly Guide

Document Version 2.0:
(10/16/18)

Developed by

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Irvine, CA 92697-2800
Office: 949.824.9073

Warning: Prototype Device – For Investigative Use Only by Trained Personnel

Fig 5.9 First page of Assembly Guide

Urology Version 2

Prototype of Project:

Fig 6.1 Device front and inner view

Fig 6.2 SolidWorks model

PCB Schematics:

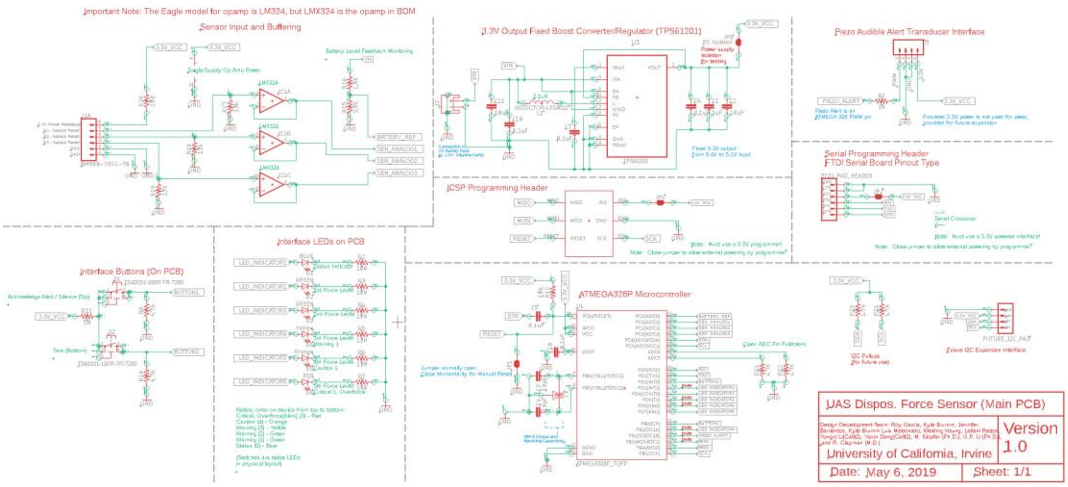

Fig 6.3 PCB schematics

PCB Layout:

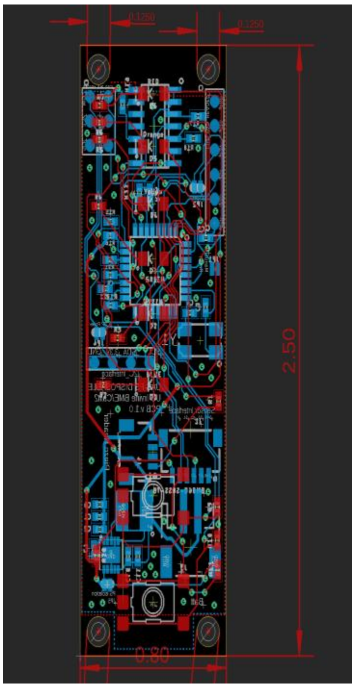

Fig 6.4 PCB layout

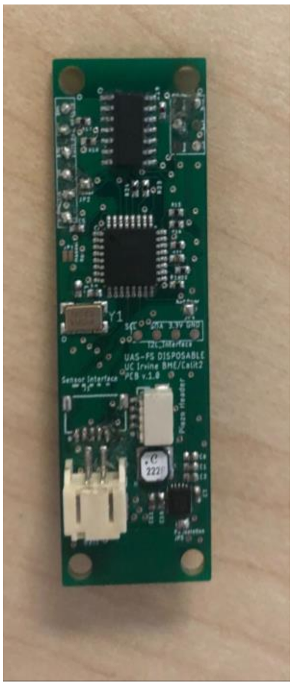

Fig 6.5 PCB front view

Assembly Guide:

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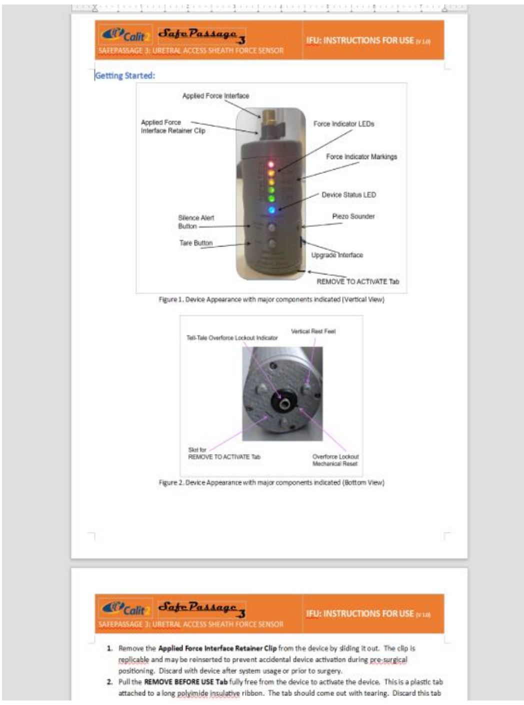

Fig 6.7 First page of IFU

Wattmeter

Abstract:

Designed PCB for three phase IoT Device on both I2C and SPI flavor to assess the device's energy-saving effect by mobilized ADE7943, and presented project with power isolated circuit and calibration result.

Project is public on (https://github.com/CalPlug/ADE7953-Wattmeter)

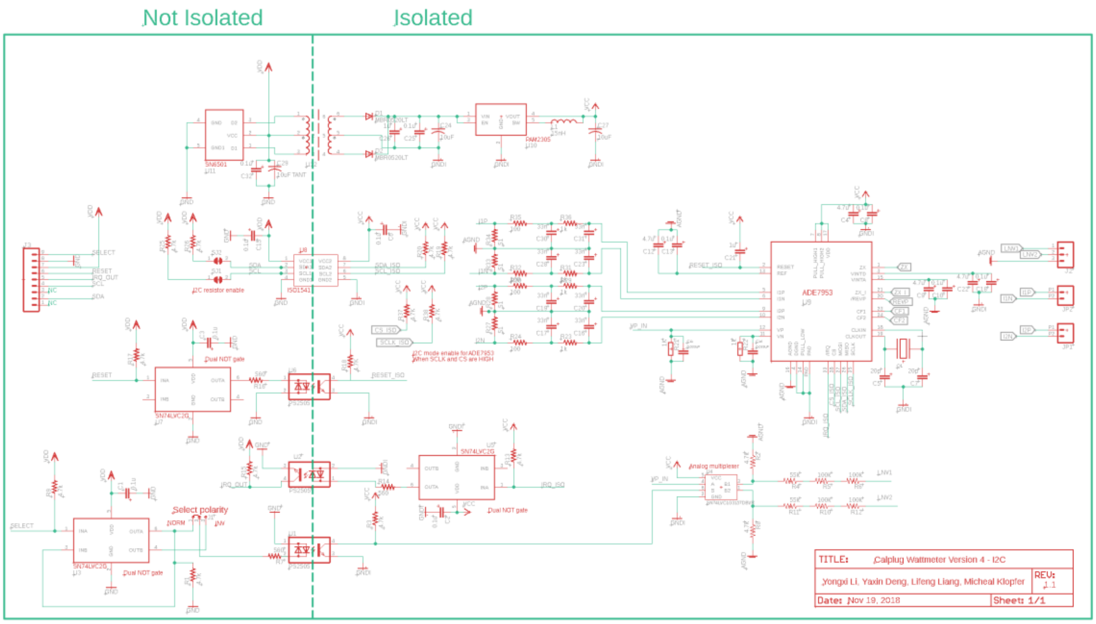

Fig 7.1 I2C Version PCB schematics

PCB Layout:

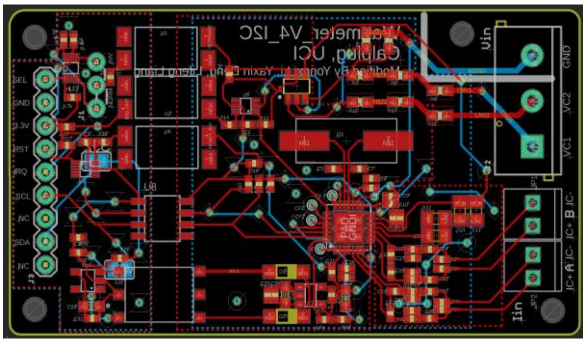

Fig 7.2. I2C Version PCB layout

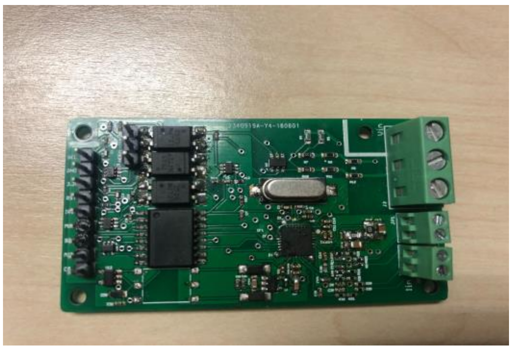

Fig 7.3. I2C Version PCB

Intermittent Computing Devices Chain-based Programming

Intermittent devices have a unique place in the low-power device space because they are batteryless. This comes with benefits and consequences. The purpose of this paper is to introduce intermittent systems along with the inherent complications, to propose a framework for simulation environments for intermittent devices to test program structure and model intermittent behavior based on varying inputs, to propose algorithmic changes to Chain-based methodology to improve performance, and to evaluate the framework using probabilistic modeling.

Full Report can be access by https://github.com/YaxinDeng/Engineering-Portfolio/blob/master/Projects'%20Report/Intermittent%20Computing%20Devices%20Chain-based%20Programming.pdf

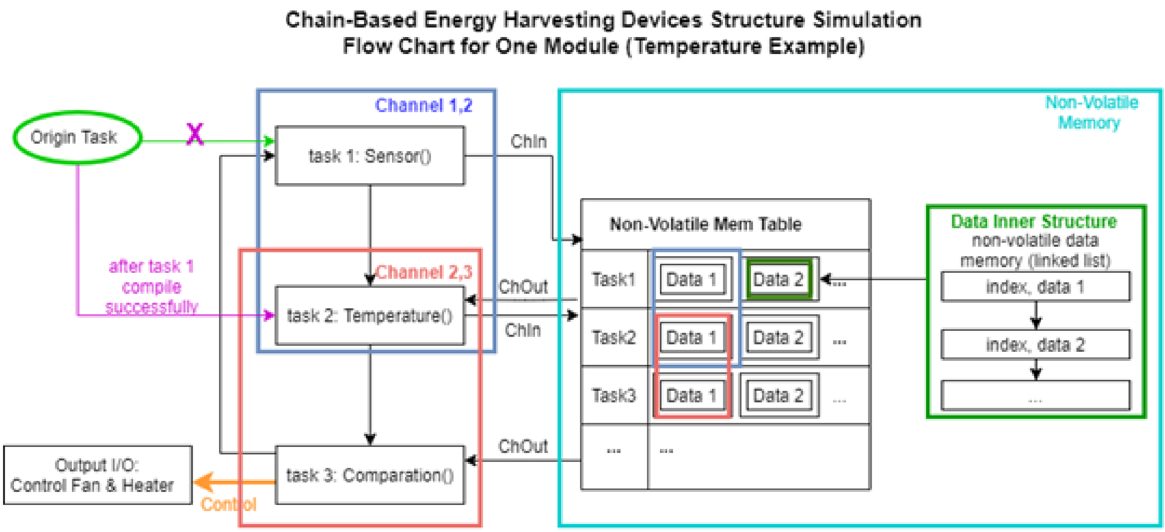

Figure 8.1 Memory Exchange Structure

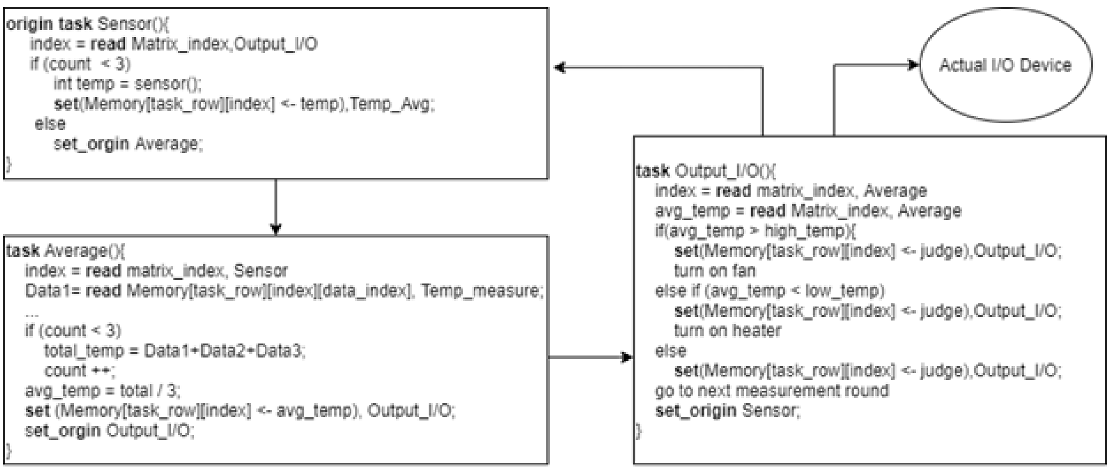

Figure 8.2: An Example pseudo-code to describe the Temperature function control loop.