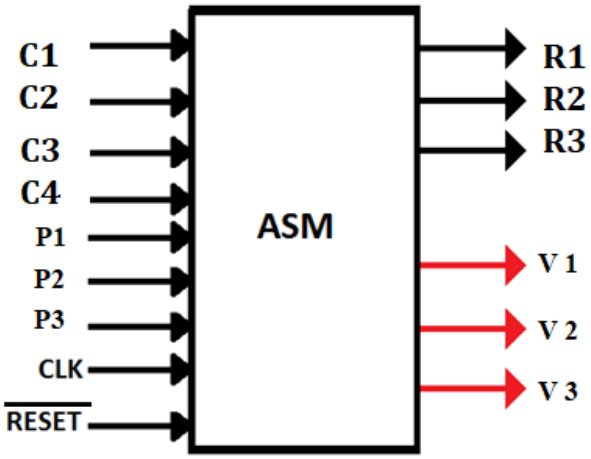
An-Najah National University
Faculty of Engineering and Information Technology
Computer Engineering Department

Digital Circuit Design II (10636321)
Due to 31/07/2021

HW1: (ILOs: **III**)	Points:**20**

Given the ASM chart in the attached image file for the following machine



Write a complete **VHDL** code to implement the architecture **using 3 processes**.
(Use a positive edge **CLK** and a low-level asynchronous **Reset**)

```
Entity ASM is
      port(      CLK, RESET, P1, P2, P3, C1, C2, C3, C4 : in std_logic;
                 V1, V2, V3, R1, R2, R3: out std_logic);
end ASM;
architecture BEHAVIOR of ASM is
```

`

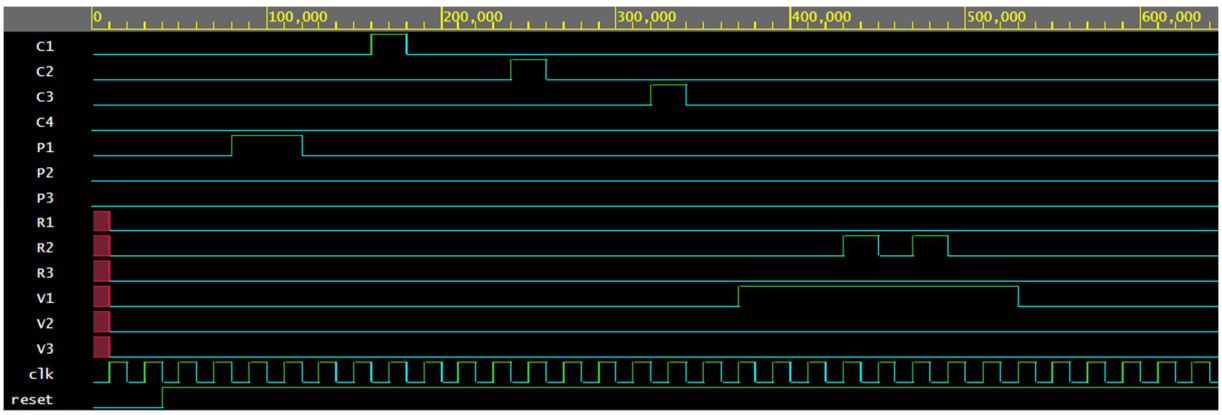
You have to submit two files:

1. A VHDL code to implement your ASM.
2. A testbench file to simulate and test your design. You should cover the following two test cases in the following sequence:

Test Case #1:

Reset	P1	P2	P3	C1	C2	C3	C4	Duration
0	-	-	-	-	-	-	-	2 Clock Cycles
1	0	0	0	0	0	0	0	2 Clock Cycles
1	1	0	0	0	0	0	0	2 Clock Cycles
1	0	0	0	0	0	0	0	2 Clock Cycles
1	0	0	0	1	0	0	0	1 Clock Cycle
1	0	0	0	0	0	0	0	3 Clock Cycle
1	0	0	0	0	1	0	0	1 Clock Cycle
1	0	0	0	0	0	0	0	3 Clock Cycle
1	0	0	0	0	0	1	0	1 Clock Cycle
1	0	0	0	0	0	0	0	10 Clock Cycles

The expected result: one pulse on V1 and 2 pulses on R2



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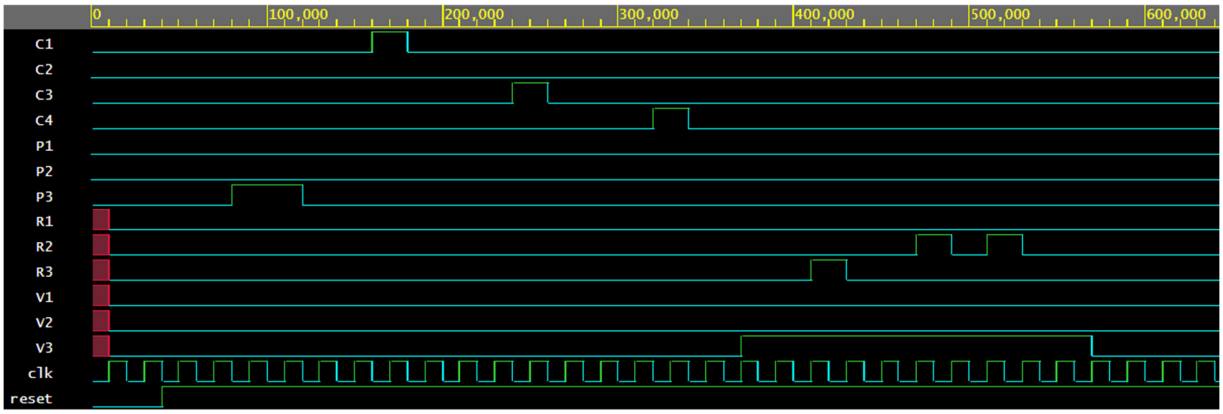
Test Case #2:

Reset	P1	P2	P3	C1	C2	C3	C4	Duration
0	-	-	-	-	-	-	-	2 Clock Cycles
1	0	0	0	0	0	0	0	2 Clock Cycles
1	0	0	1	0	0	0	0	2 Clock Cycles
1	0	0	0	0	0	0	0	2 Clock Cycles
1	0	0	0	1	0	0	0	1 Clock Cycle
1	0	0	0	0	0	0	0	3 Clock Cycle
1	0	0	0	0	0	1	0	1 Clock Cycle
1	0	0	0	0	0	0	0	3 Clock Cycle
1	0	0	0	0	0	0	1	1 Clock Cycle
1	0	0	0	0	0	0	0	10 Clock Cycles

The expected result: one pulse on V3, 2 pulses on R2 and 1 pulse on R3



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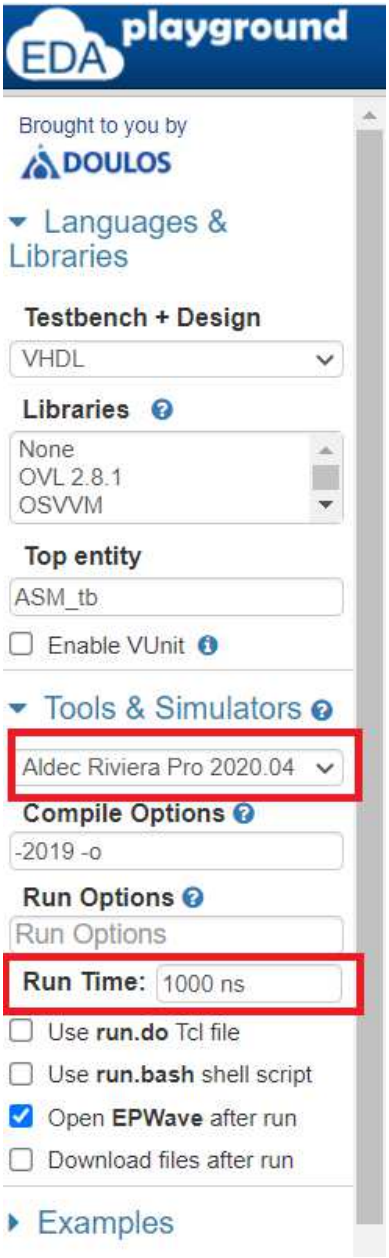
Note: When you select the simulation tool to be “**Aldec Rivera Pro 2020.04**”, do not forget to set the **Run Time** to be sufficient to cover the previous test cases.



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