An-Najah National University
Faculty of Engineering and Information Technology
Computer Engineering Department

Digital Circuit Design II (10636321)

29/07/2021
Duration: 50 Minutes

Online Assignment # 2 : (ILOs: **III**)	Points:**15**

Complete the following VHDL design to implement a digital system that calculates the length of the longest sequence of consecutive zeros. This system can load an input data (10-bit) value when the **Load** input is asserted, and then compute the result on the positive edge of the input clock.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity Length_Calculator is
  port(   CLK, Load, Clear : in  std_logic;
          Data    : in  std_logic_vector(9 downto 0);
          Length  : out std_logic_vector(3 downto 0)
          Valid   : out std_logic);
end Length_Calculator;

architecture behavioral of Length_Calculator is
```

Your design should include the following pins:

1. **CLK:** (positive edge trigger input clock)
2. **Load:** Synchronous **Active High** Load signals
3. **Clear:** Asynchronous **Active Low** Input (Clear the outputs)
4. **Length:** The output result which represents the length of the longest sequence of zeros in the loaded data.
5. **Valid:** An output flag to indicate that the output Length is valid. This output should be set to '0' when the input Data has no zeros

e.g.

Load = 1 & Data = 1010000100 ➔ Length = 0100 & Valid = 1
Load = 1 & Data = 1000110001 ➔ Length = 0011 & Valid = 1
Load = 1 & Data = 1111111111 ➔ Length = 0000 & Valid = 0

Notes:

- Use behavioral description
- The calculation should be synchronous with the clock when the load signal is equal to 1. (*the length of longest consecutive zeros should be calculated in a single clock cycle at the rising edge*)

You have to submit two files:

1. **A VHDL code to implement your Design.**
2. **A testbench file to simulate and test your design:**
    a. You have to give a test case for the Asynchronous **Clear**,
    b. You have to cover all the possible cases for the input **Data** (1024 different cases)
        - For each case you have to:
            1. Select a different value for the input **Data**
            2. Set the **Load** signal to **'1'**
            3. Wait for two clock cycles

    c. You have to give a test case to show that no change will occur when the **Load** signal is **'0'**.