COMPENG 2EI4
Design Project #4

Yazan Khatib
Instructor. Dr. Yasser M. Haddara

Department of Electrical and Computer Engineering, McMaster University
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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Yazan Khatib, khatiy2, 400531344]**

Problem Statement

Design, build, and test a MOSFET based XOR gate.

Circuit Schematic

To determine the circuit schematic, we must first determine the boolean expression for an XOR gate:

Y = A (+) B

Y = (A'B + B'A)

Y = (A'B + B'A)''

Y = ((A+B')(B+A'))' = ((AB) + (AB)')'

Using this information it is pretty easy to design the circuit.

PUN will be built with PMOS while PDN will be built using NMOS,

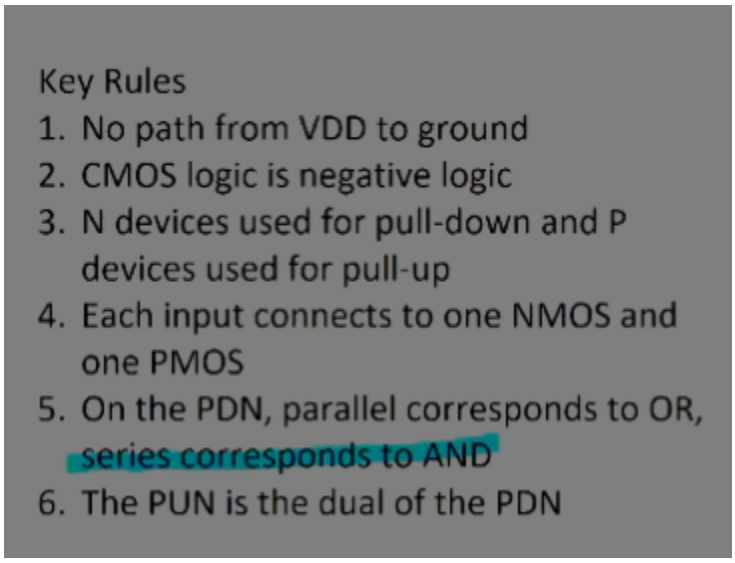
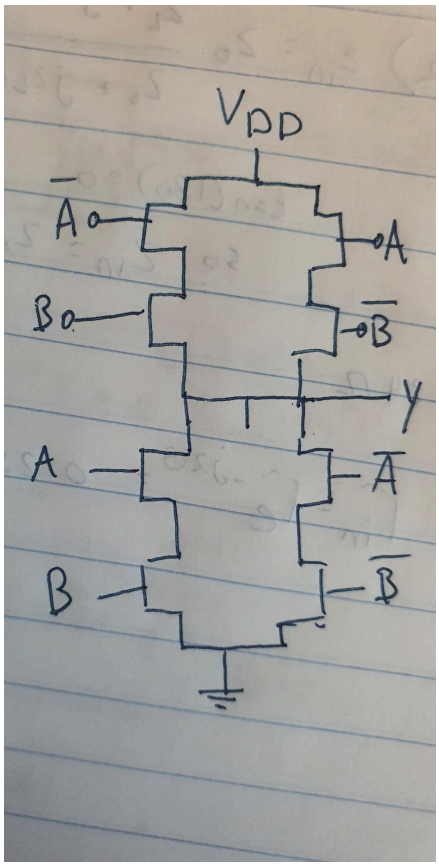


Figure 1: CMOS circuit rules.

For PUN we know that parallel is AND and series is OR, and vice versa for PDN.

Which gives us:



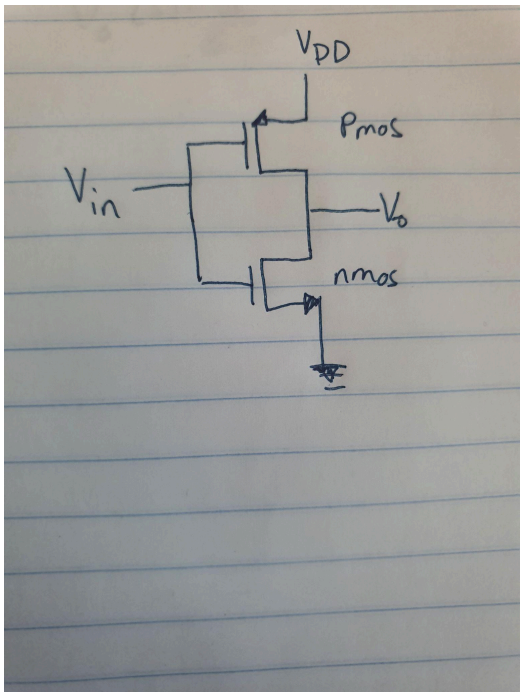


Figure 3: NOT gate

Figure 2: XOR gate

As seen above, 2 logic gates are needed, the XOR gate alongside the inverter for A'/B' inputs. A total of 12 MOSFETs are needed, 6 PMOS and 6 NMOS.

Ideal Sizing:

To minimize the time delay of the circuit, we need a 1:1 ratio between the PUN and PDN of the circuit. Since PUNs are made of NMOS and PDNs are made of PMOS, we must keep in mind the speed difference between holes and electrons, which is approximately a factor of 2.5. Due to this (W/L)p = 5/1 and (W/L)n = 2/1.

In order to determine the ideal sizing of this circuit, we must first look at the longest path worst case scenario of the circuit, which for all branches is 2 MOSFETS.

Therefore:

Rref = 2R = Ra + Rb.

So for PDN, (W/L)a = (W/L)b = 2n

And for PUN (W/L)a = (W/L)b = 2p.

Given this information, It is unlikely that we can implement this ideal sizing in our hardware design since we are stuck with whatever dimensions were manufactured in our given IC. Because of this it is expected that the circuit will suffer from asymmetric propagation delays.

Testing

For the physical circuit model, the CD4007CN chip was utilized. The final circuit can be seen below.

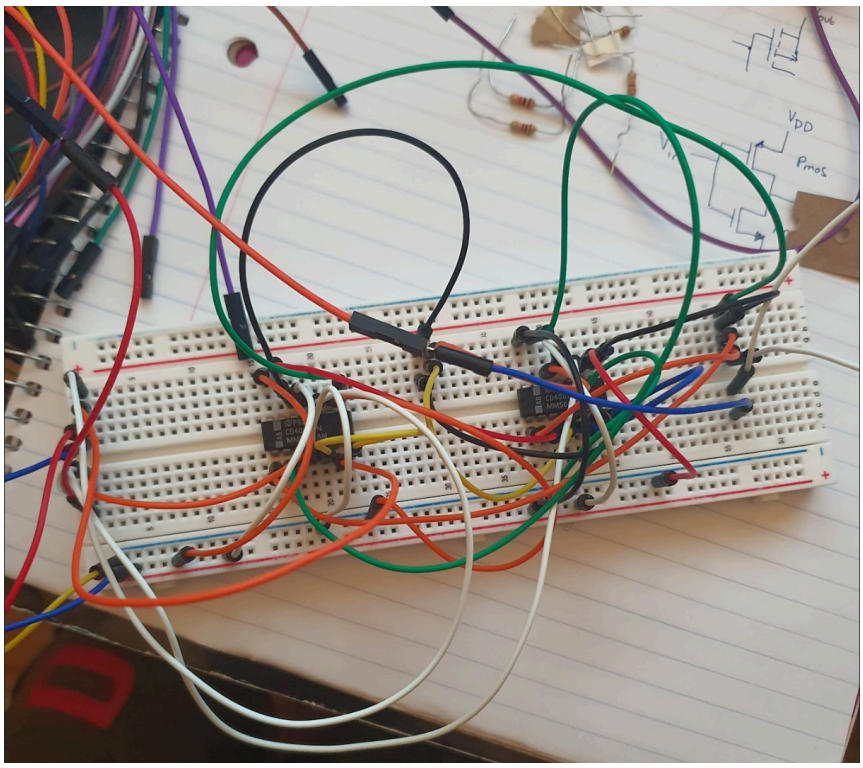


Figure 4: Completed XOR gate circuit

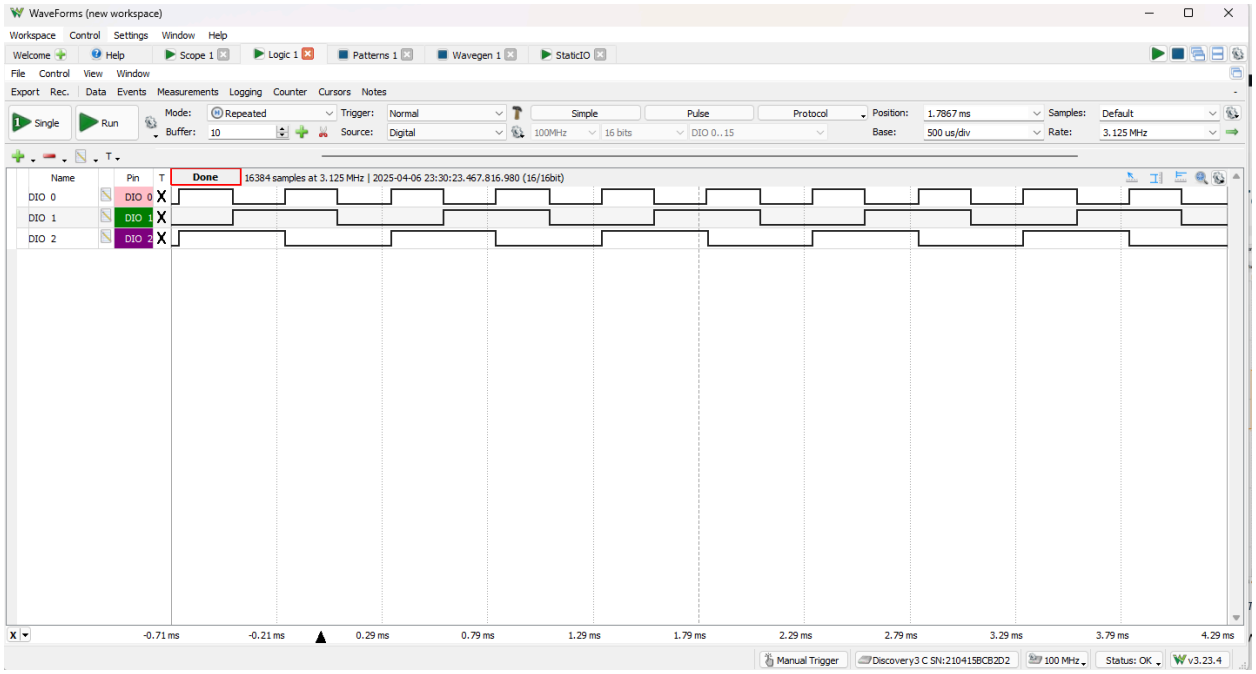


Figure 5: Logic Testing the CMOS XOR gate (DIO 0 = A, DIO 1 = B, DIO 2 = Y)

After building the circuit and using digital I/O pins (0/1) for A and B, we can give them different frequency clock cycles and check the output Y (I/O pin 3), and as we can observe on waveforms, the circuit is implementing the XOR function (only on iff 1 input is on)

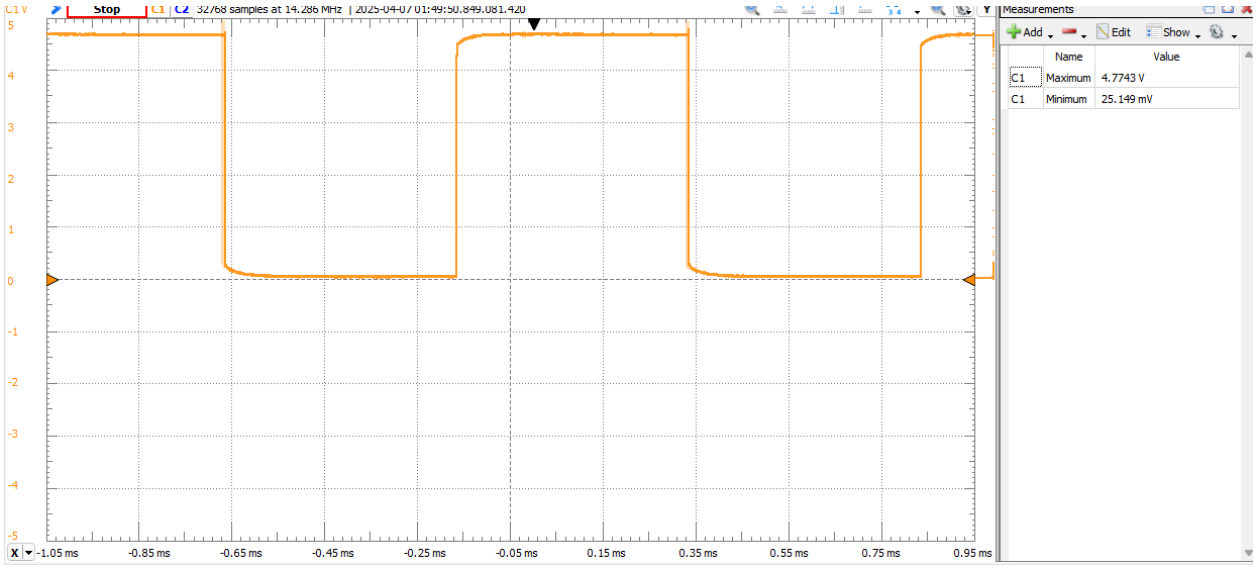


Figure 6: Static Testing (A = 5v DC, B = 0-5V Square Wave)

When setting A to a 5v DC signal and B to a square wave between 0-5v, we can observe that the output has a VH of ~4.77V and VL of ~25mV

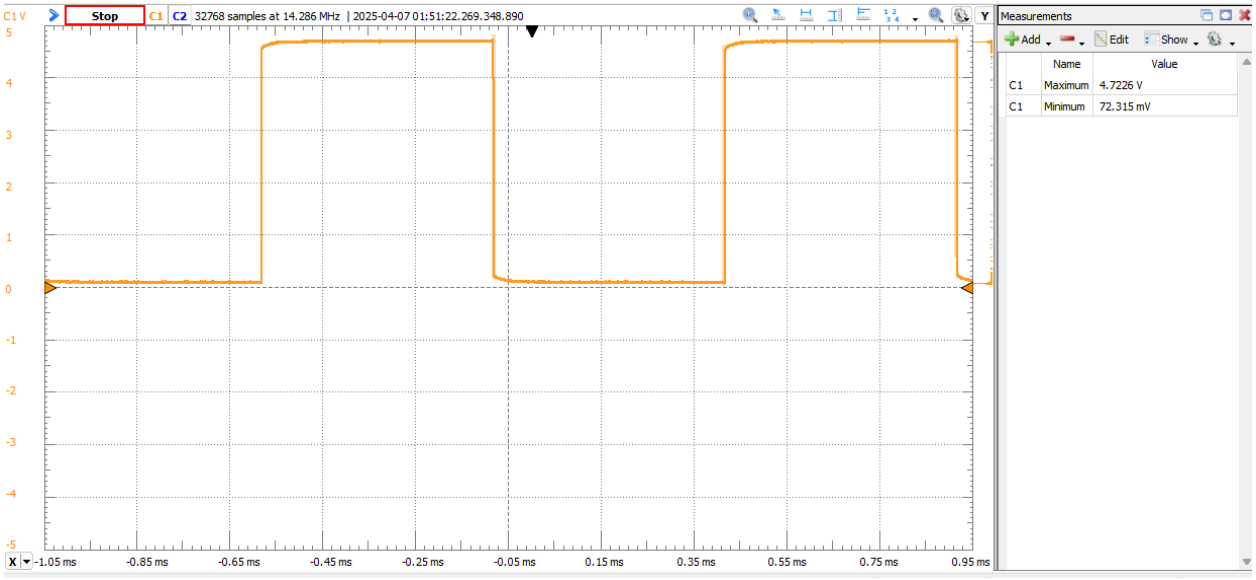


Figure 7: Static Testing (A = 0 - 5v Square Wave, B = 5V DC)

When switching the inputs, we can see the waveform stays the same, and VH/VL still remains quite similar, with VH being 4.71V and BL being 72mV.

Timing

For timing, input A was set to a logic 1 while input B was set to a square wave between 0 and 5v. A 100nf capacitor was connected at the load.

We can obtain the rise time and fall time by making use of the measurements in Waveforms, and we can also manually check them via cursors. As we can observe from the waveform, the XOR gate output has a rise time of 320us and a fall time of 217us. From these values we can determine that Tphl = (0.5)(320) = 160us and Tplh = (0.5)(217) = 108.5us, and Tp = (108.5 + 160)/2 =134.25us

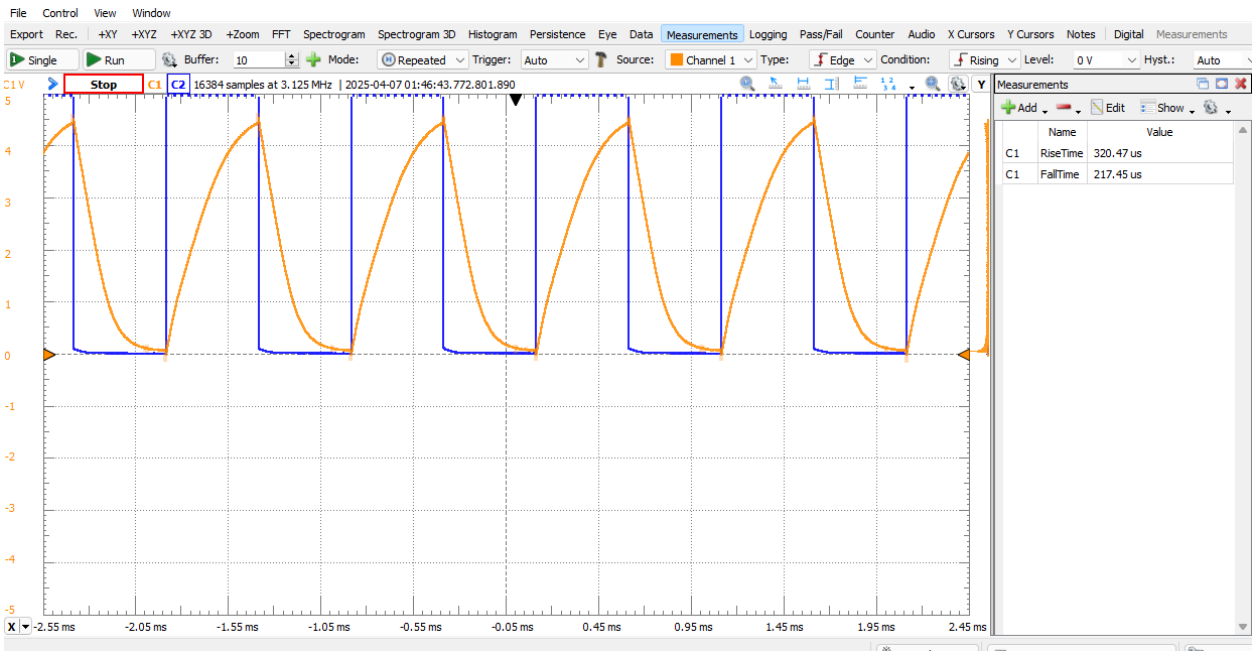


Figure 8: Timing Analysis using 100nF Capacitive Load.