

COMPENG 2EI4

Project 2: Design Project #2

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Yazan Khatib, khatiy2, 400531344]**

Project Purpose: Design and Test an Ideal Switch.

Important Properties of an Ideal Switch

An ideal switch has several key properties that define its perfect performance. The most important properties are:

1. **Zero On-Resistance ($R_{on} = 0 \Omega$ ON State):** When the switch is closed, it acts as a perfect conductor, allowing current to flow without any resistance. [1]
2. **Infinite Off-Resistance ($R_{off} = \infty \Omega$ OFF State):** When the switch is open, it completely blocks current flow, acting as a perfect insulator. [1]
3. **No Leakage Current ($I = 0$ OFF State):** In the off state, there is no unintended current flow through the switch. [1]
4. **No Voltage Drop in On-State ($V_1 = V_2$ ON State):** When conducting, the voltage across the switch remains at zero. [1]
5. **No Current or Voltage Limitations:** The switch can handle any voltage and current (and any current direction) without constraints.[2]
6. **No relationship between terminals in OFF State:** When the switch is turned OFF, the two terminals are not related to each other and can have any voltage.[2]

Non-Idealities of Real Switches and Their Measurement

Real-world switches exhibit non-ideal behaviors due to physical constraints. These non-idealities can be measured using standard techniques:

1. **On-Resistance ($R_{on} \neq 0 \Omega$):**
 - **Effect:** Causes a voltage drop and power dissipation in the closed state.
 - **Measurement:** Measure voltage drop across the switch and divide by current ($V/I = R_{on}$). Ensure that the same value of R_{on} is observed for $V_1 < V_2$ and $V_1 > V_2$. [2]
2. **Off-State Leakage Current ($I_{off} \neq 0$):**
 - **Effect:** Allows unintended current flow even when the switch is off.
 - **Measurement:** Use a sensitive ammeter to measure leakage current in the off state. [3]
3. **Voltage Range Limitations ($V_{min} < V_1, V_2 < V_{max}$):**
 - **Effect:** The switch may not operate correctly for voltages outside a specific range.
 - **Measurement:** Test the switch over a range of voltages to determine the minimum and maximum operational limits. [1]
4. **Breakdown Voltage Limitations:**
 - **Effect:** If exceeded, the switch may fail or allow current to flow uncontrollably.
 - **Measurement:** Apply increasing voltage until breakdown occurs and record the maximum safe voltage [1]

By understanding these non-idealities and measuring them effectively, we can design practical voltage-controlled switches that closely approximate ideal behavior.

Test Plan - Switch Type 1

- V control will be a pulse wave between 0 and 5V
- V supply will be a 5 volt DC value
- V1 will be connected to V supply ($V1 = Vs$)
- The First non-ideality will be the voltage drops across the switch when its on
 - This can be measured by taking the voltage at V1 and subtracting it from the voltage at V2
- The Second non-Ideality will be the current when the switch is open
 - This can be measured by looking at the voltage across the load and dividing it by the resistor when the switch is open.
- The Third non-Ideality will be the voltage range limitations
 - This will be testing by applying an AC input from 0 - 5 volts at V1 and checking how the circuit behaves
- The fourth non-Ideality is checking bidirectionality
 - This can be tested by swapping V1 and V2 and checking the behavior is similar

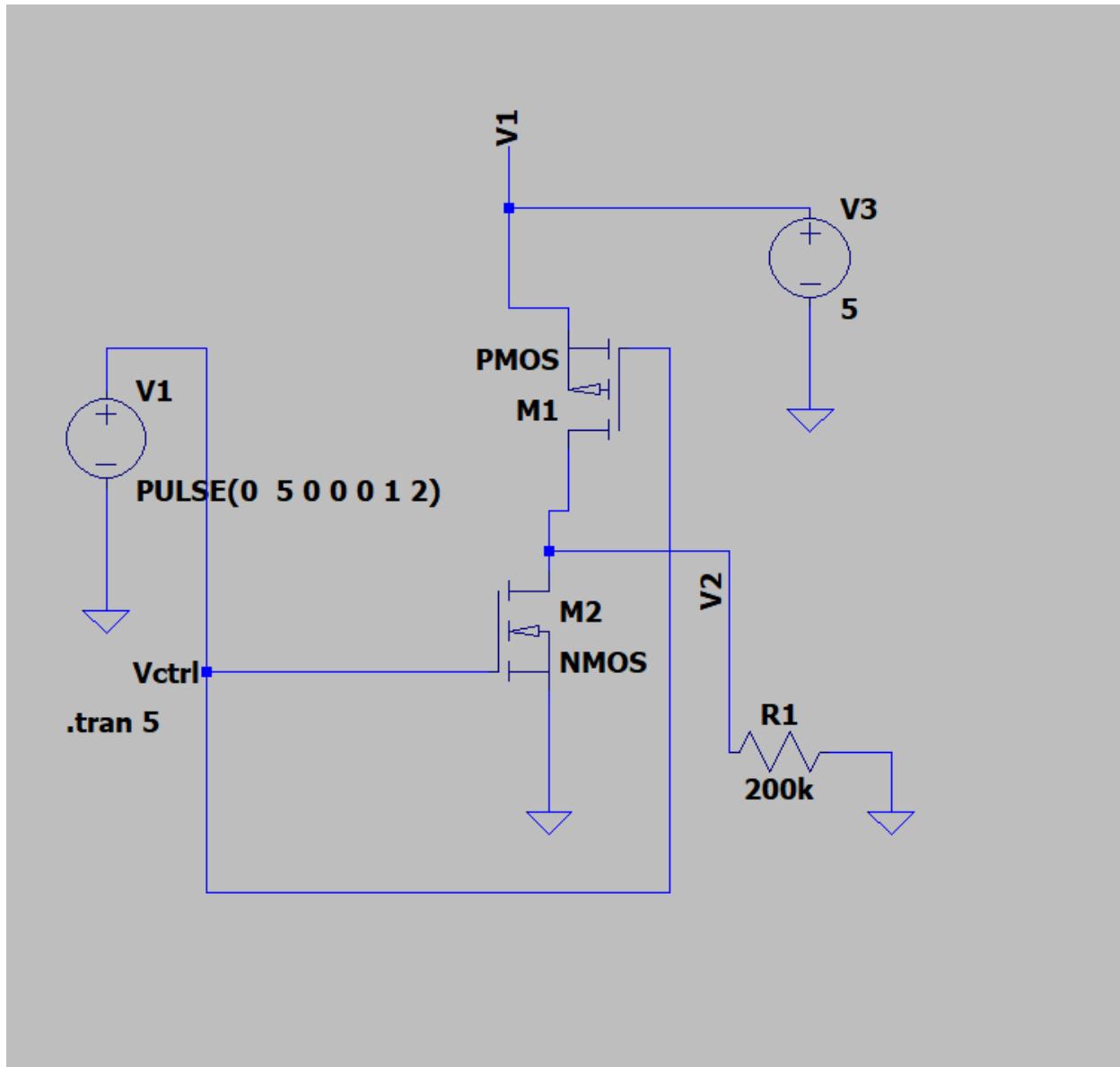
Test Plan - Switch Type 2

- $V_{supply} = 5V$ DC
- $V1 = 5V$ DC
- $V_{control} = 0V$ to $5V$ square wave

Non-Idealities & Test Metrics:

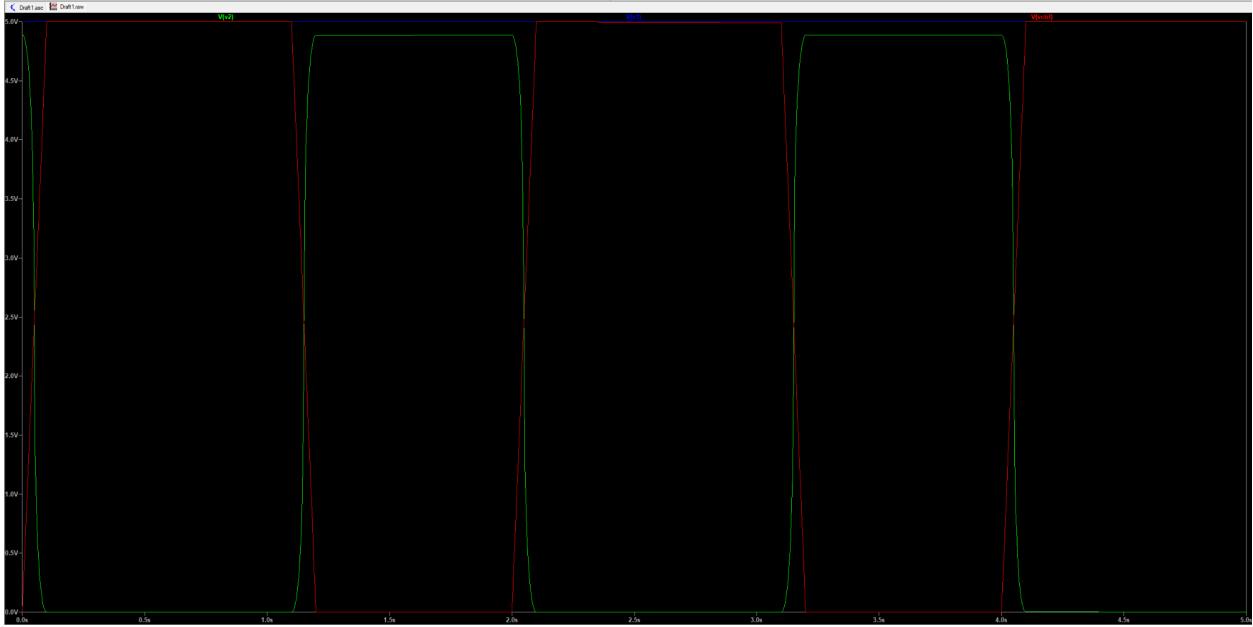
1. Voltage Drop in ON State (Switch Closed, $V_{control} = 0V$)
 - Expect a small voltage drop across the switch.
 - Metric: Measure V_{out} (V_A, V_B) and compare with V_{in} to determine drop.
2. Leakage Current in OFF State (Switch Open, $V_{control} = 5V$)
 - A real switch has some leakage current.
 - Metric: Measure V_{out} (V_A, V_B) and divide by resistance to compute leakage current.
3. Bidirectionality Limitation
 - A real switch may not be fully bidirectional in conduction.
 - Metric:
 - Check if swapping inputs have similar behavior.
4. Operational Voltage Range
 - The switch operates only over a specific input range.
 - Metric: Apply a ramp function (0V to 5V) to the supply and observe when the switch behaves unexpectedly.

Switch Type 1

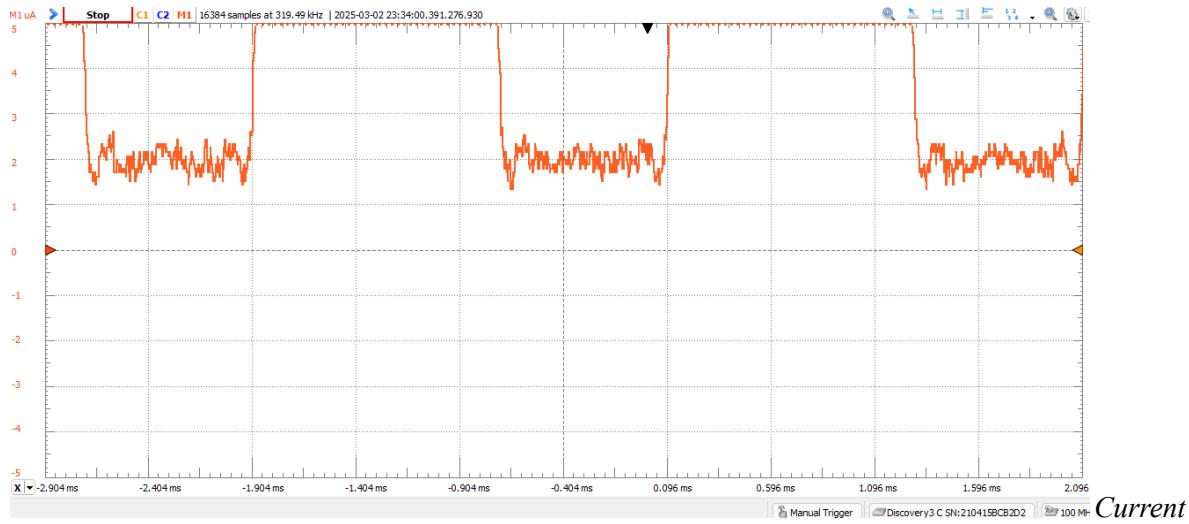


Circuit Schematic

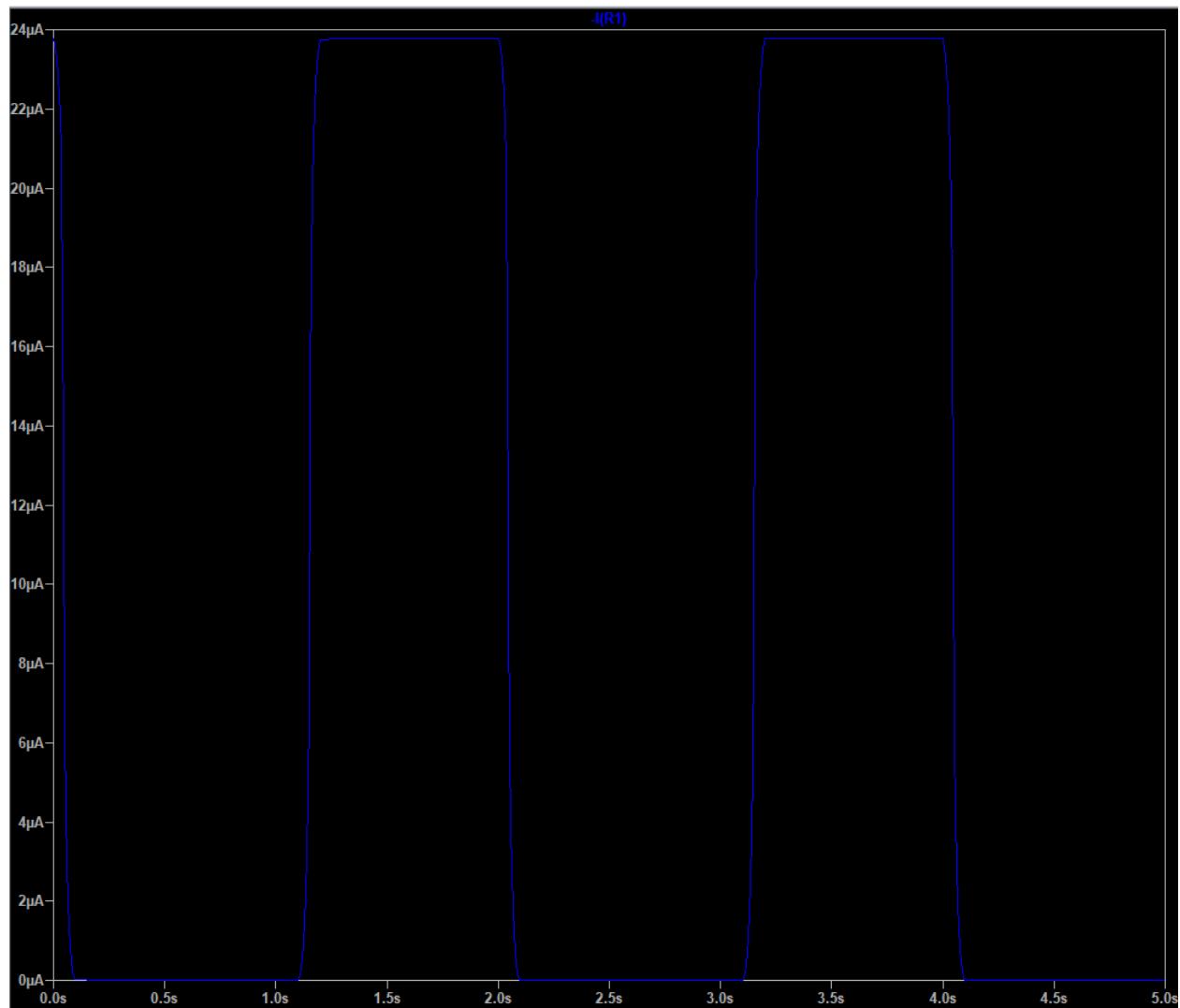
Measurements



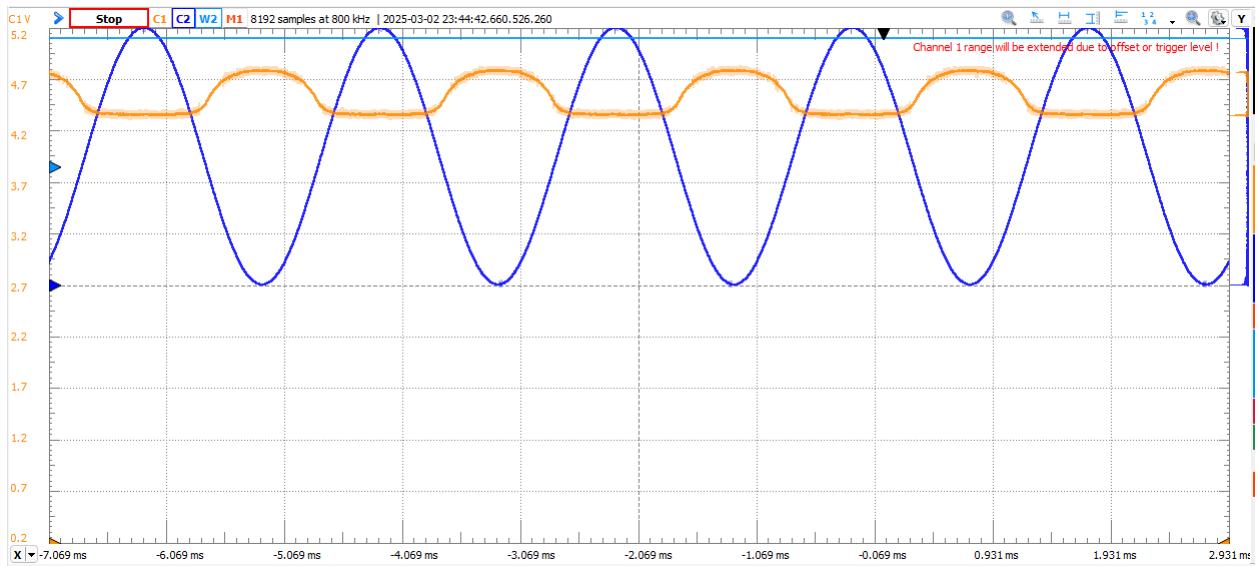
Measurements on LTSpice for V control(red), $V1$ (blue), and $V2$ (green) (checking for non-Ideality I)



measured via AD3. (checking for non-Ideality 2)



Current measurement on resistor.



Switch tested with V_1/V_2 swapped. (checking for non Ideality 3)



V_1 / V_2 tested for inputs between 0 - 5V (checking non-Ideality 4) (1.74V seems to be the minimum)

THEORETICAL CALCULATIONS

PMOS Transistor

- Threshold voltage, $V_{\text{th}} = 1.7 \text{ V}$
- Transconductance parameter, $K = 4.4 \mu\text{A/V}$

NMOS Transistor

- Threshold voltage, $V_{\text{th}} = 1.75 \text{ V}$
 - Transconductance parameter, $K = 7.3 \mu\text{A/V}$ [4]
-

Voltage Drop in the ON State (Control = 0 V)

- **NMOS Analysis:**

With the gate-to-source voltage for the NMOS, $V_{\text{GS}} = 0 \text{ V}$ (which is less than or equal to V_{th}), the NMOS is in cutoff. Consequently, the drain current (I_{DS}) is 0 mA.

- **PMOS Analysis:**

For the PMOS, the source-to-gate voltage is calculated as:

$$V_{\text{SG}} = 5 \text{ V} - 0 \text{ V} = 5 \text{ V}$$

Since 5 V is greater than $-V_{\text{th}}$ (or equivalently $5 \text{ V} > 1.7 \text{ V}$), the PMOS operates in either the saturation or the linear region. Assuming it is in saturation, the drain current is given by:

$$\begin{aligned} I_{\text{DS}} &= (K/2) \times (V_{\text{SG}} + V_{\text{th}})^2 \\ &= (4.4 \times 10^{-6} \text{ A/V} / 2) \times (5 \text{ V} - 1.7 \text{ V})^2 \\ &\approx 2.39 \times 10^{-5} \text{ A} \end{aligned}$$

With this current, the voltage at the drain (V_{D}) can be found using the load resistor ($R_{\text{L}} = 200 \text{ k}\Omega$):

$$\begin{aligned} V_{\text{D}} &= I_{\text{DS}} \times R_{\text{L}} \\ &= (2.39 \times 10^{-5} \text{ A})(200,000 \Omega) \\ &= 4.79 \text{ V} \end{aligned}$$

Therefore, the voltage drop across the PMOS during the ON state is:

$$\begin{aligned} \text{Voltage drop} &= V_{\text{S}} - V_{\text{D}} \\ &= 5 \text{ V} - 4.79 \text{ V} \\ &= 0.21 \text{ V} \end{aligned}$$

Current Leakage in the OFF State (Control = 5 V)

For the OFF state, the PMOS has a source-to-gate voltage of:

$$V_{\text{SG}} = 5 \text{ V} - 5 \text{ V} = 0 \text{ V}$$

Since 0 V is less than or equal to V_{th} ($0 \text{ V} \leq 1.7 \text{ V}$), the PMOS remains in cutoff and no drain current flows ($I_{\text{DS}} = 0 \text{ mA}$). This indicates that there is no leakage current.

Voltage Supply Range

- **ON State (Control = 0 V):**

The PMOS must remain in saturation, which requires:

$$\begin{aligned}V_{SD_2} &\geq (V_{SG_2} + V_{I2}) \\&= 5 \text{ V} - 1.7 \text{ V} \\&= 3.3 \text{ V}\end{aligned}$$

- **OFF State (Control = 5 V):**

To ensure the PMOS remains in cutoff, the condition is:

$$V_{SG_2} \leq -V_I$$

which means:

$$\begin{aligned}V_{S_2} - V_{G_2} &\leq 1.7 \text{ V} \\ \text{so } V_{S_2} &\text{ must be } \leq 1.7 \text{ V} + 5 \text{ V} = 6.2 \text{ V}\end{aligned}$$

However, the project specification requires that the supply voltage does not exceed 5 V.

Experimental Measurements:

Voltage drop during ON State

- $V_1 - V_2 = 5 - 4.89\text{v} = 0.11\text{V}$
- Current Leakage = $\sim 2\mu\text{A}$
- Voltage supply range= According to the graph with the ramp up function, switch operates properly between $\sim 1.74\text{V}$ and 5V for ON State
- Current for ON State = $\sim 25 \mu\text{A}$

Experimental Measurements VS Theory

After testing the physical circuit and comparing the measured values to the theoretical predictions, several observations were made. First, the voltage drop across the switch in the physical circuit was actually smaller than the calculated and simulated value. This suggests that, in this aspect, the physical circuit behaved closer to an ideal switch than the models had predicted.

Another non-ideality observed was the leakage current in the OFF state. While the theoretical model predicted a leakage current of 0 mA, the physical design exhibited a very small leakage current of $2 \times 10^{-6} \text{ A}$, demonstrating that the real switch is not entirely ideal.

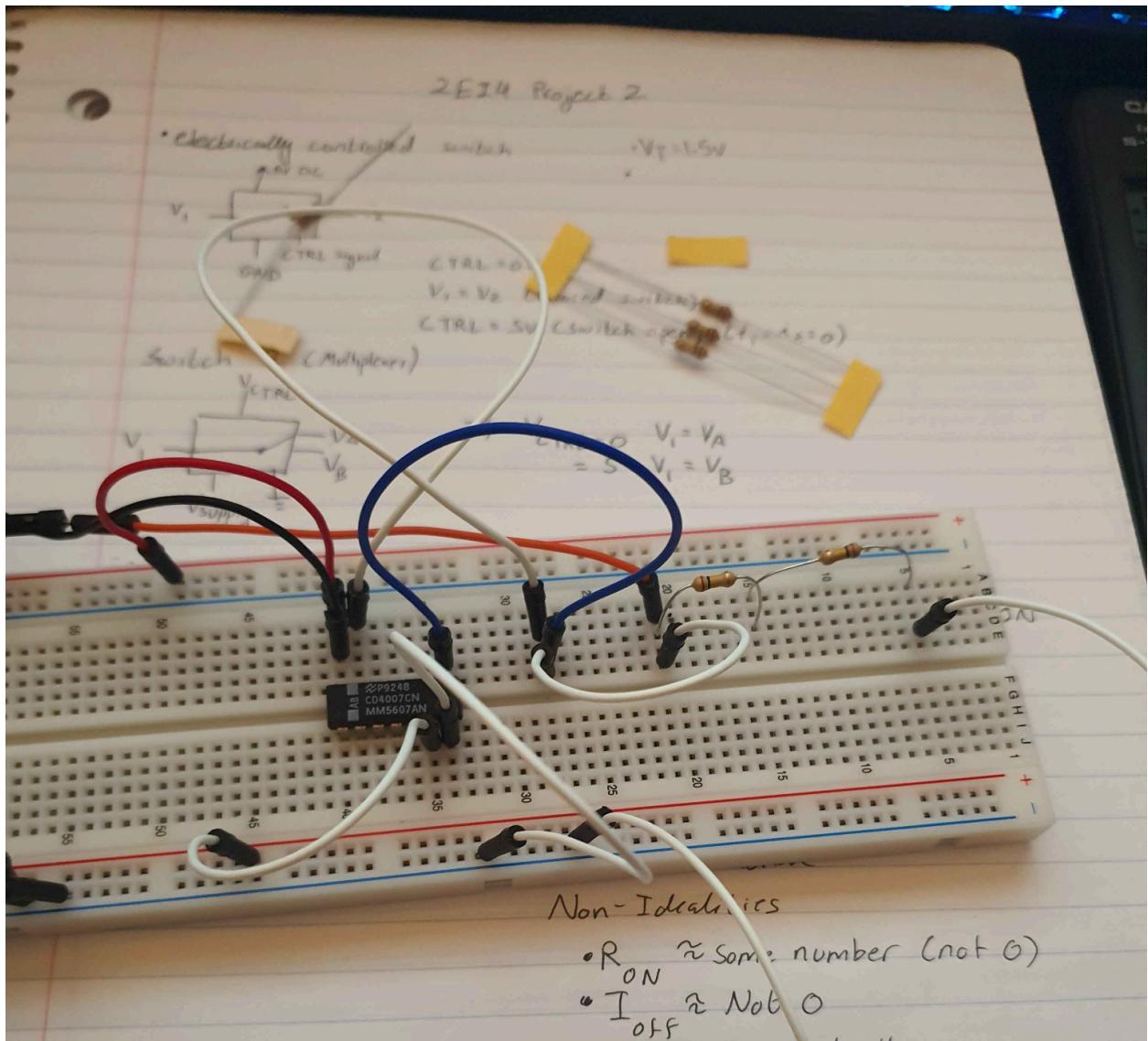
It can also be observed that the switch is not fully bidirectional, while $V_1=V_2$ during the ON State, the switch does not act like an open switch during the OFF state.

Finally, the operating supply voltage range of the switch in the ON state was examined. The predicted requirement was that V_{SD_2} should be at least 3.3 V. However, the physical measurements **showed that** the ON state supply voltage ranged from 1.74 V up to 5 V. Throughout this range, the output voltage

closely followed the input voltage, which is exactly the behavior expected when the switch is in the ON state.

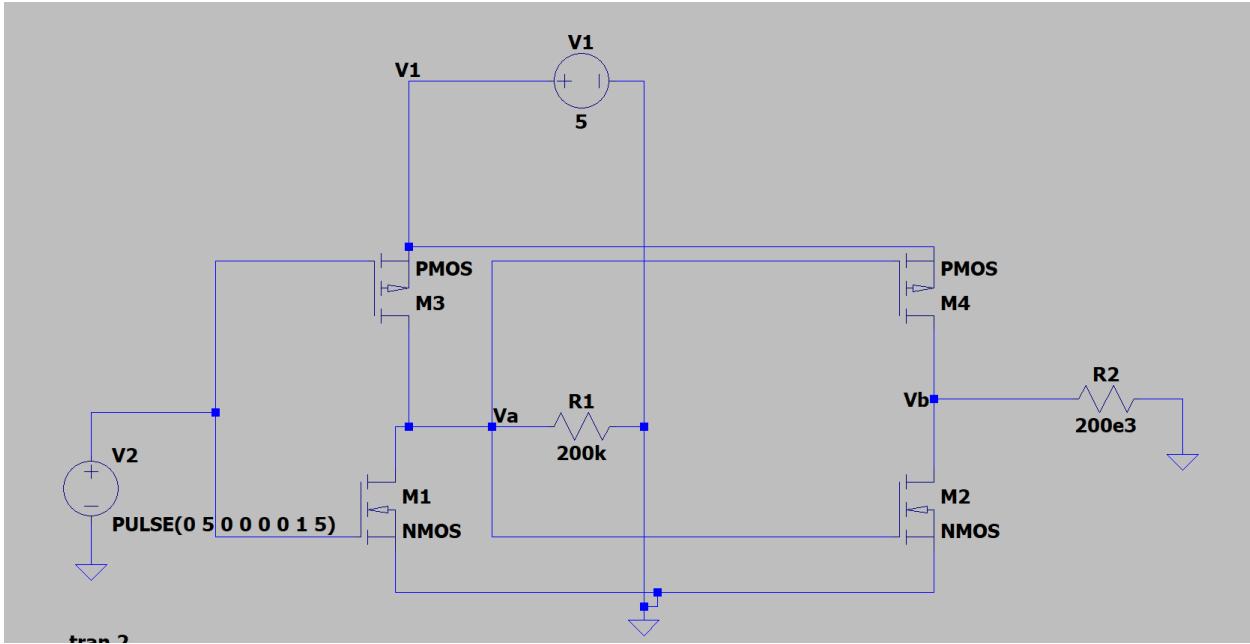
Design Tradeoffs

In our design, we intentionally prioritized simplicity and cost efficiency by using only two resistors, two enhancement-mode MOSFETs, and a single voltage supply. While there were designs that could use a single PMOS MOSFET, these seem to require extra components such as a BJT or an Inverter which while they may increase performance, they come at the cost of complexity (and price of additional components). This circuit's minimal component count keeps the design straightforward and reduces both manufacturing complexity and overall cost (with resistors at about \$0.06 each and the CD4007CN MOSFET IC around \$0.58 per chip). The tradeoff, however, is that the limited number of components—along with a narrow operating supply range—may restrict the circuit's flexibility and performance under varying conditions. There were designs that could in theory solve some of the non-idealities of this switch (Notably Bi-directionality of the back-to-back Mosfet circuit) but those would have been too complex and costly, making it quite hard to test and build given the available materials.



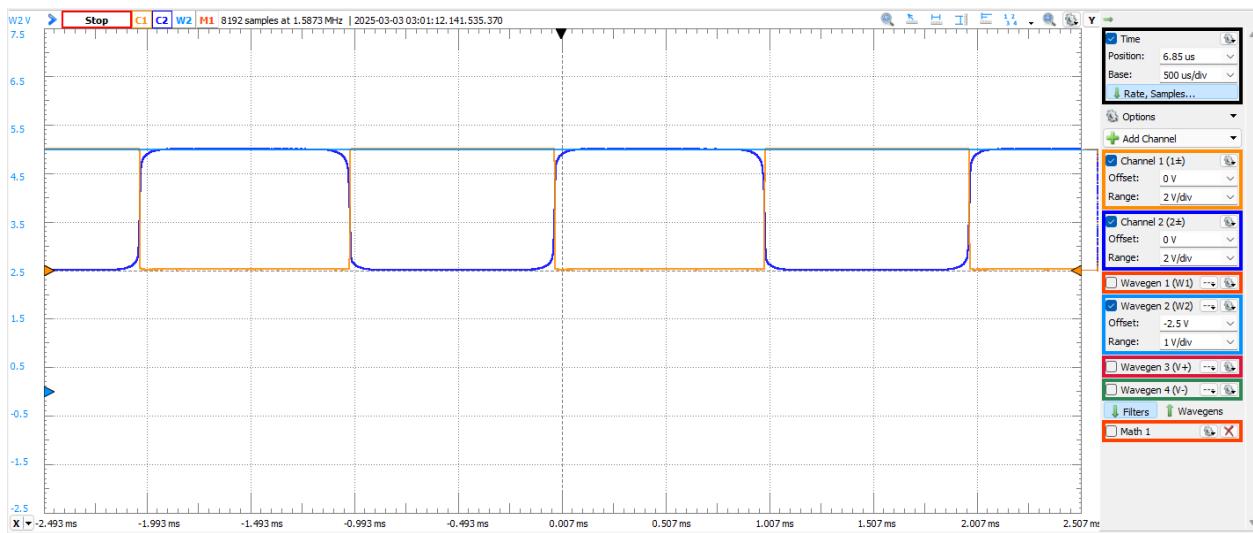
Physical Circuit.

Switch Type 2

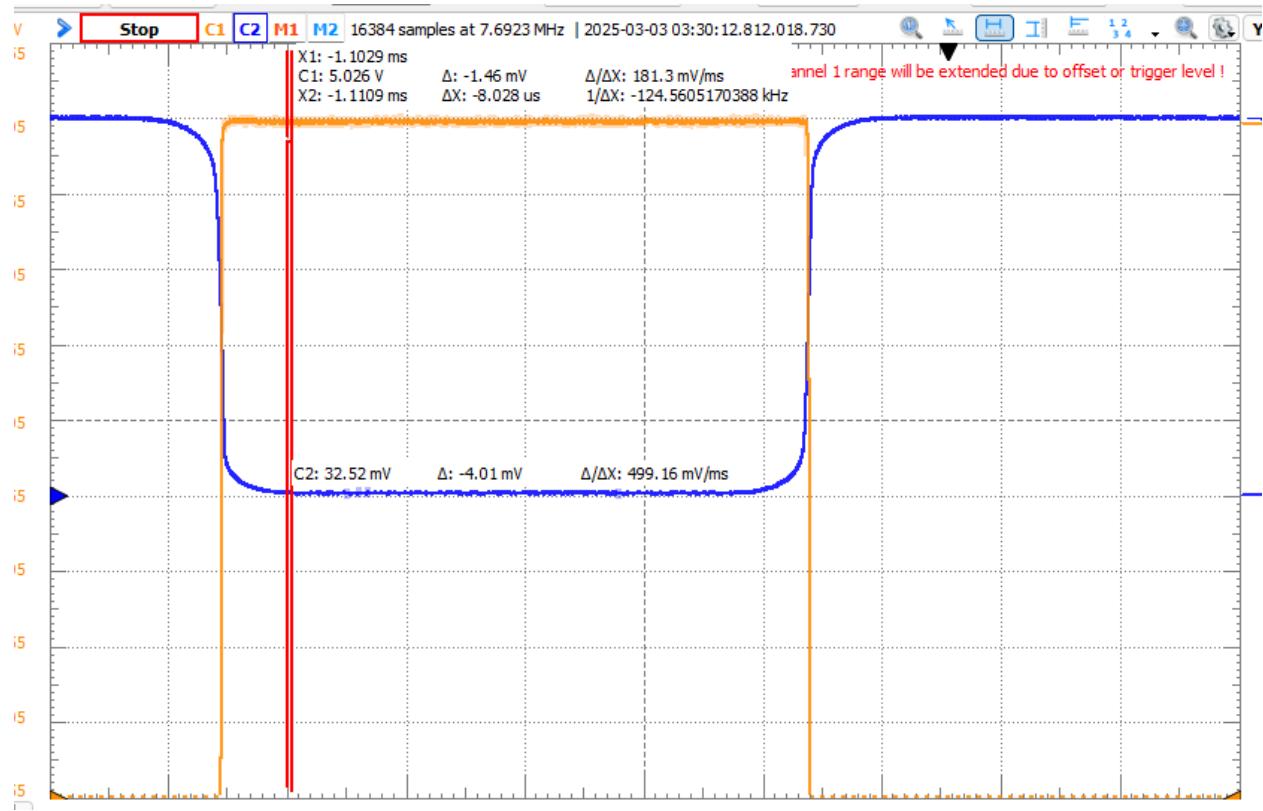


Circuit Schematic

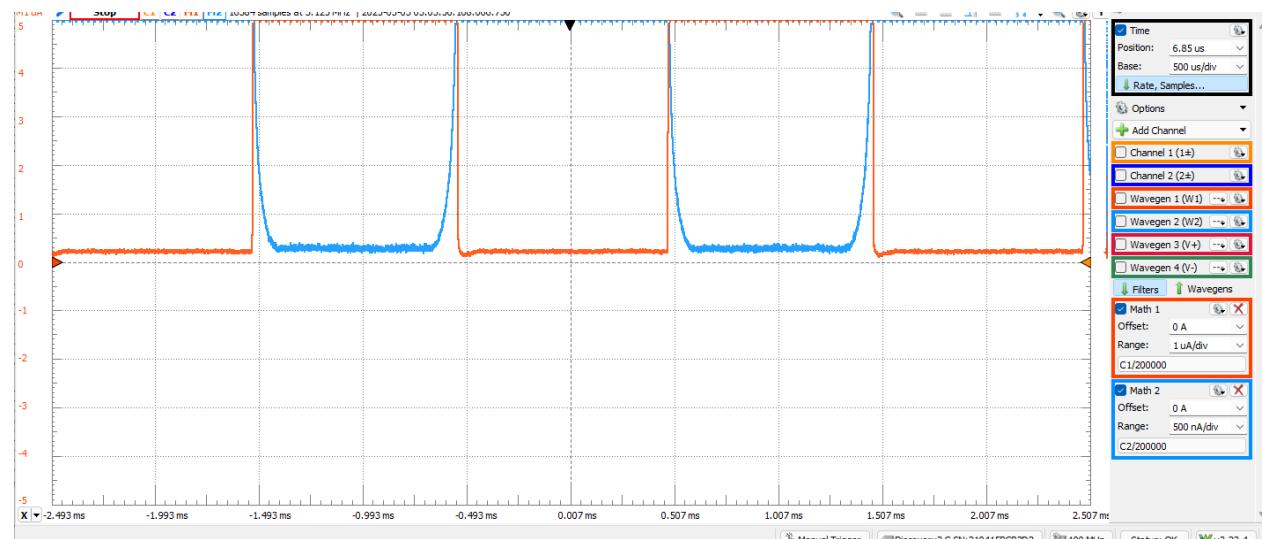
Measurements



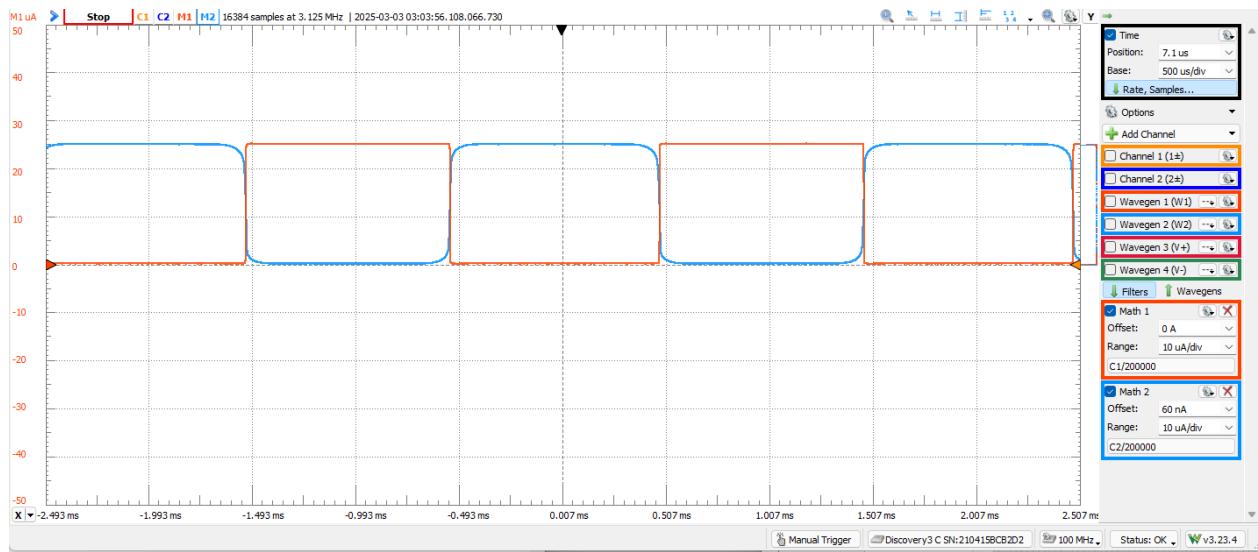
AD3 Measurements for Va (Orange) Vb (Blue) and V1 (Light blue)



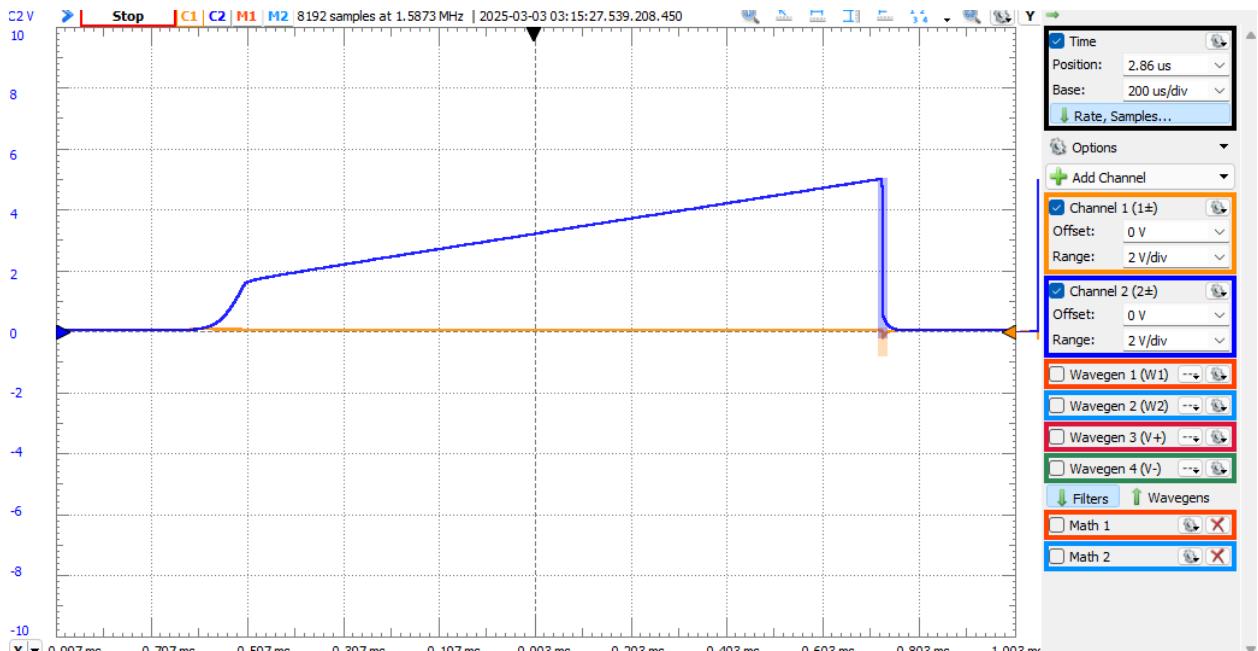
VA/VB difference (~.026v drop)



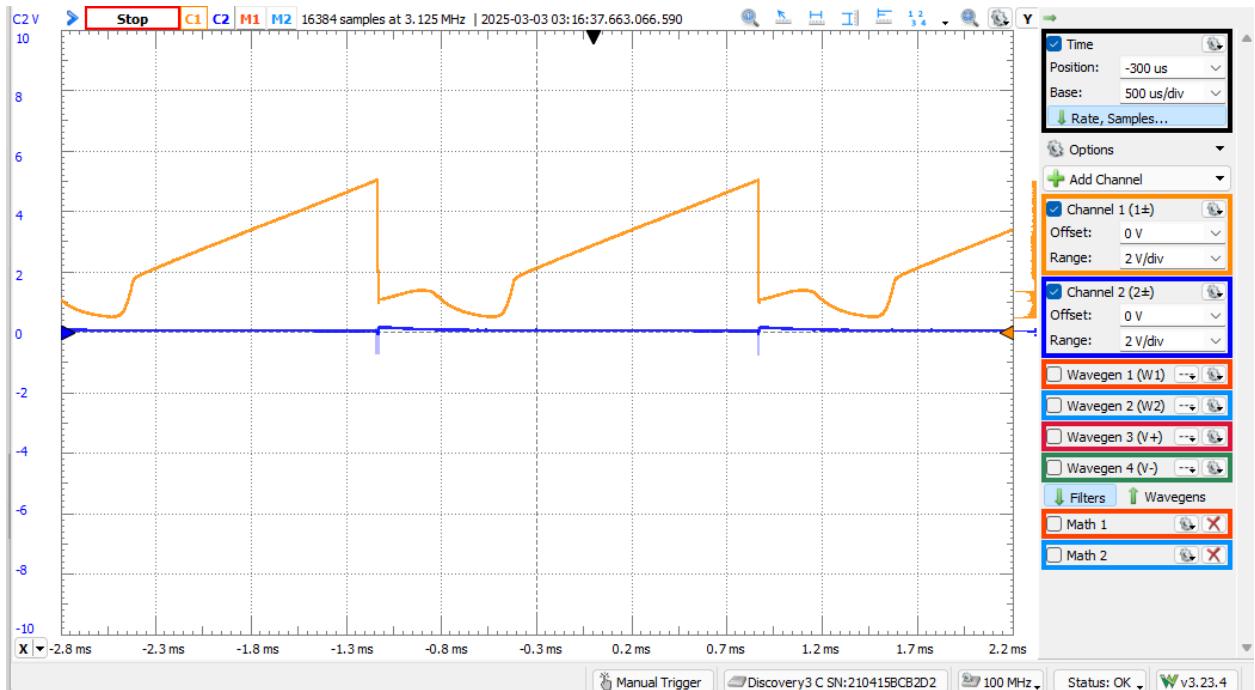
Leakage current measurements at R1/R2 (~.3 - .4 uA)



Current measurements for R1/R2 (25 uA)



Ramp function for V1 to test Va (V control is 0) (1.6v required)



Ramp function for V1 to test Vb (V control is 5) (1.7v required)

Theoretical Calculations

PMOS Transistor

- Threshold voltage, $V_{\text{th}} = 1.7 \text{ V}$
- Transconductance parameter, $K = 4.4 \mu\text{A/V}$

NMOS Transistor

- Threshold voltage, $V_{\text{th}} = 1.75 \text{ V}$
- Transconductance parameter, $K = 7.3 \mu\text{A/V}$ [4]

Due to the extremely similar design of this circuit, the calculations are expected to be identical to the ones found in the first switch, as these are two switches tied together such that when one is in the OFF state the other is in the ON state and vice versa, but in terms of calculations the numbers are pretty much identical.

NMOS Analysis:

- $V_{\text{GS}_1} = 0 \text{ V} (\leq V_{\text{th}})$, NMOS in **cutoff**
- $I_{\text{DS}} = 0 \text{ mA}$

PMOS Analysis:

- $V_{\text{SG}_2} = 5 \text{ V} - 0 \text{ V} = 5 \text{ V}$
- $5 \text{ V} > 1.7 \text{ V} \rightarrow \text{PMOS in saturation}$
- $I_{\text{DS}} = (4.4 \times 10^{-6} \text{ A/V} / 2) \times (5 \text{ V} - 1.7 \text{ V})^2 \approx 2.39 \times 10^{-5} \text{ A}$
- $V_{\text{D}_2} = I_{\text{DS}} \times R_{\text{L}} = (2.39 \times 10^{-5} \text{ A})(200 \text{k}\Omega) = 4.79 \text{ V}$

- **Voltage drop across PMOS:** $5\text{ V} - 4.79\text{ V} = \mathbf{0.21\text{ V}}$

OFF State (Control = 5 V):

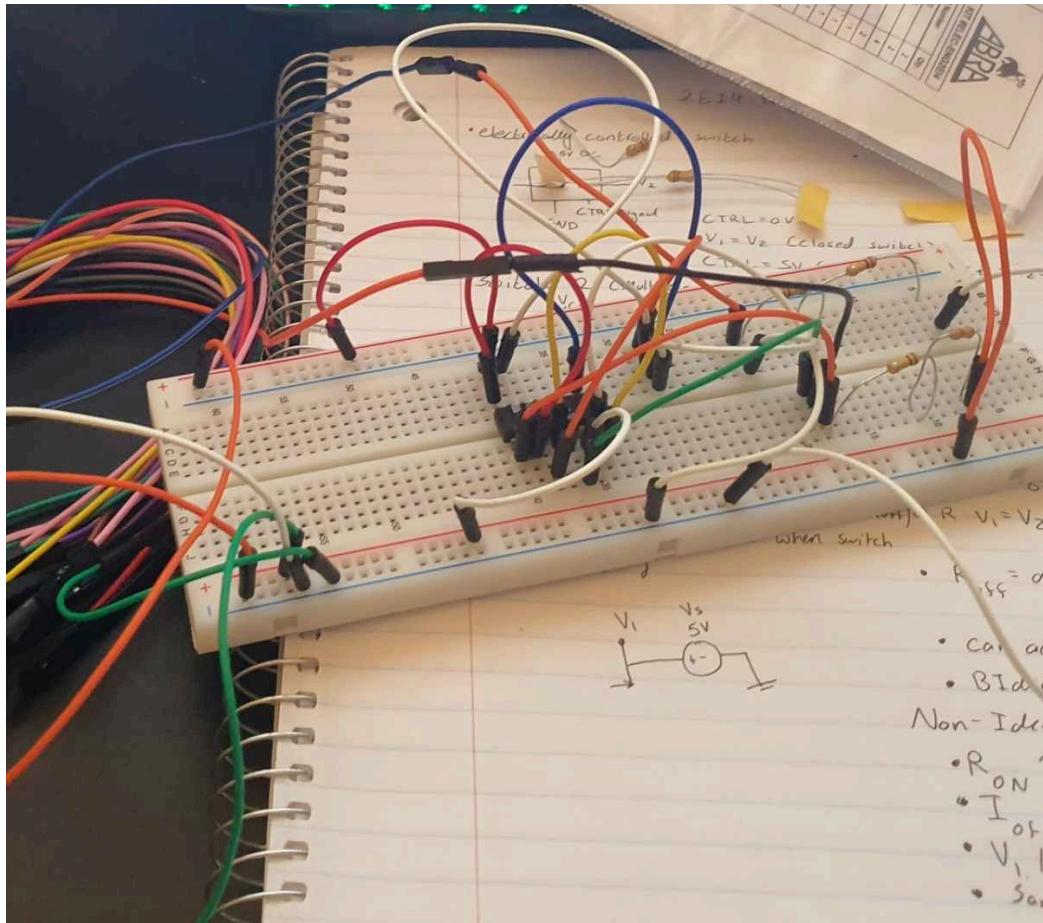
- $V_{SG} = 5\text{ V} - 5\text{ V} = 0\text{ V}$
- $0\text{ V} \leq 1.7\text{ V} \rightarrow \mathbf{\text{PMOS in cutoff}}$
- $I_{DS} = 0\text{ mA (no leakage current)}$

Voltage Supply Range:

- **ON State (Control = 0 V):**
 - $V_{SD_2} \geq (V_{SG_2} + V_{I2}) \rightarrow V_{SD_2} \geq \mathbf{3.3\text{ V}}$
- **OFF State (Control = 5 V):**
 - V_{S_2} must be $\leq 1.7\text{ V} + 5\text{ V} = \mathbf{6.2\text{ V}}$
- Supply voltage **must not exceed 5 V** per project specs.

Experimental Measurements vs Theory

After testing the physical circuit, we can observe some differences between the theoretical and experimental results. Theoretically, we were expecting that when VA or VB are conducting, there are 0 drops between V1 and Va/Vb, but it was measured that there was a $\sim 0.026\text{v}$ drop, which shows that MOSFETS are not ideal switches and have some resistance. The next non-Ideality was the leakage current when the switch was OFF, theoretically there should be 0 current leaking, but in the experiments there was an observed small amount of current ($\sim .3 - .4\text{ uA}$) for both Va and Vb when they were not conducting, this also confirms that these are not ideal switches (resistance is not infinity). Bidirectionality was not tested in this device, because from the results of the first one it can be determined that these are not bidirectional, as this device is basically 2 copies of the first circuit connected together. The Final non-Ideality that was tested is the range at which the voltage and Va/Vb conducts, it was expected they'd behave very similarly to the first switch and in measuring we can see that we only require about 1.6 - 1.7V to conduct for Va and Vb, which is very close the the value from switch 1.



Picture of built Circuit

Design Tradeoffs:

This design maintains a relatively simple structure but is slightly more complex than the initial version. It requires four resistors, four enhancement-mode MOSFETs, and a single voltage supply. Despite the increased component count, the circuit remains straightforward, and its small operating supply range further simplifies its implementation (The circuit is just 2 copies of the first connected together). However, the additional components result in a slightly higher cost. The resistors are priced at approximately \$0.06 each, while the CD4007CN MOSFET IC costs around \$0.58 per chip.

technically this circuit can be done using BJTs as BJTs do have a lower threshold voltage, meaning the range at which V_a/V_b can conduct could be way smaller, but For switching applications, digital logic, and power electronics, MOSFETs are almost always the better choice due to lower power dissipation, higher speed, easier control, and better thermal stability. Building a circuit with BJTs would also be more complex, due to their current-driven nature, the need for biasing, thermal considerations, and slower switching speeds.

Datasheet used: <https://www.onsemi.com/pdf/datasheet/mc14007ub-d.pdf>

Works Cited

- [1] 3.General switching characteristics 3.1 the ideal switch,
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- [4] CMOSedu.com, https://cmosedu.com/jbaker/courses/ee420L/s19/students/kerstett/lab_8/lab_8.htm (accessed Mar. 1, 2025).