COMPENG 2EI4
Design Project #3

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Yazan Khatib, khatiy2, 400531344]**

Problem Statement

Design, simulate, and build an amplifier that can take an input of ±0.5V from a source with an internal resistance of 100 and deliver it to a 100 load with good linearity and less than 10% attenuation.

Circuit Schematic

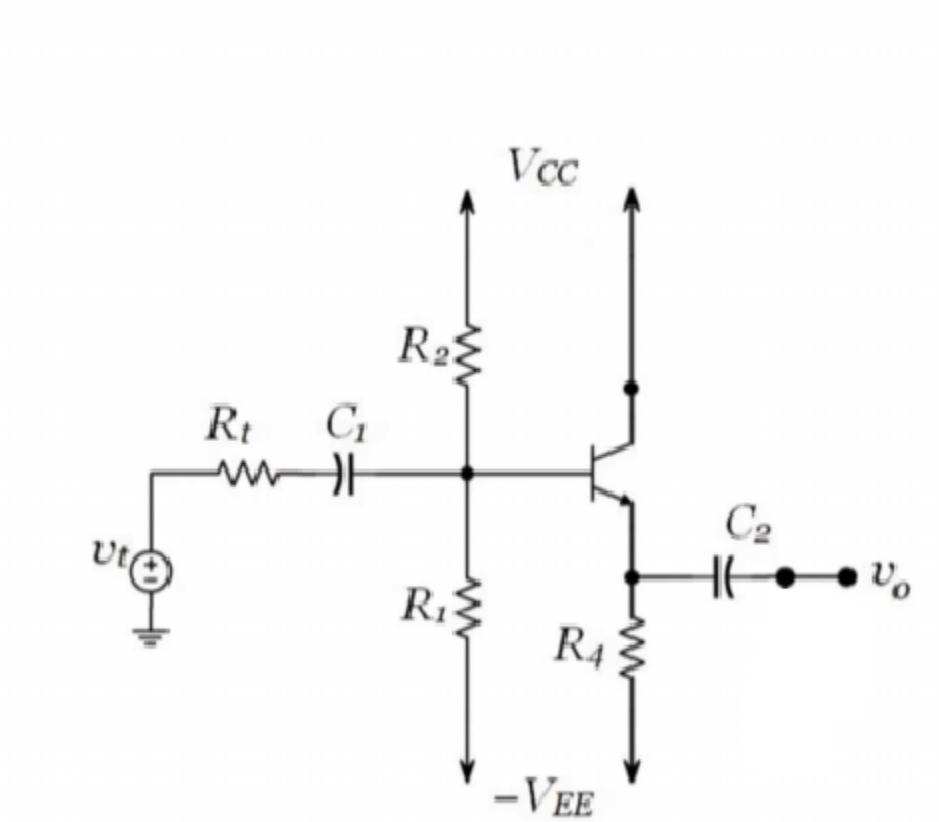


Figure 0: Circuit Diagrma

What type of transistor did you choose (MOSFET/BJT)? Why?

The first step was to determine what type of transistor should be chosen, and it was decided that this design would use the given 2N3904 BJT provided in the 2EI4 kit. A BJT was chosen due to their better performance in small signal applications due to their high transconductance (gm) allowing the transistor to satisfy all the

constraints of the design. They also offer higher gain compared to mosfets at low currents, alongside being far more linear than mosfets due to the gain being independent of the bias voltage.

What amplifier topology (CE/CS/CD/etc.) did you choose? Why?

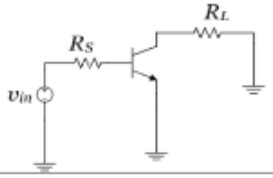
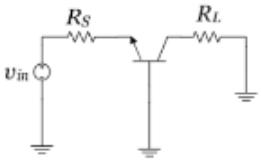
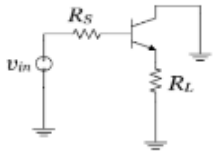
	Common Emitter	Common Base	Common Collector
Circuit			
$A_v = \frac{v_o}{v_{in}}$	$-g_m(R_L \parallel r_o)\frac{r_\pi}{R_S + r_\pi}$	$\frac{+g_m(R_L \parallel r_o)}{1+g_m R_S}$	$\frac{g_m R_L}{1+g_m R_L}\cdot\frac{R_{in}}{R_{in}+R_S} \approx 1$
R_{in} (to the right of R_S)	r_π	$1/g_m$	$r_\pi(1+g_m R_L)$
R_{out} (to the left of R_L)	r_o	$r_o(1+g_m R_S)$	$\frac{\alpha}{g_m}+\frac{R_S}{\beta+1}$
Allowed input signal range	$0.2V_T$	$0.2V_T(1+g_m R_S)$	$0.2V_T(1+g_m R_L)$

Figure 1: Common BJT amplifier configuration characteristics

Given we have already selected BJTs, we are left with 3 topologies to choose from (CE/CB/CC). For our project we are trying to achieve a gain within 1 - 0.9, which requires high input resistance and low output resistance. Both common emitter and common collector equations result in a higher input resistance than common base, and common collector also has a very low output resistance compared to common emitter, alongside having a medium/high signal swing, which fits according to our specifications (+-0.5v signal swing considered large).

What calculations did you use to determine the required component values?

- Calculations

- Need gm, R1, R2
- Given RL = 100 = Rt
- Av >= 0.9, Vin = +-0.5v AC

Solve for gm:

Vin = 0.2(0.025)(1+gm(100))

0.5 >= 0.2(0.025)(1+gm(100))

- **990ms >= gm**

Solve for R1/R2

0.9 <= (990(100))/(1 + 990(100)) * (Rin/(100+Rin))

900 <= Rin

Rin = R1//R2//(Rpi(1 + gm(100)))

Rpi = 100/.99 = 101

R1//R2 = Rp

Rin = Rp//(101(1+(990)(100)))

Rp >= 988

R1//R2 have to be bigger than or equal 988 ohms when in parallel

- **R1 = 2k ohms**
- **R2 = 3.33k ohms**
- For the capacitors a **10uF capacitor** was chosen.

Simulation

Below is the circuit schematic in Pspice.

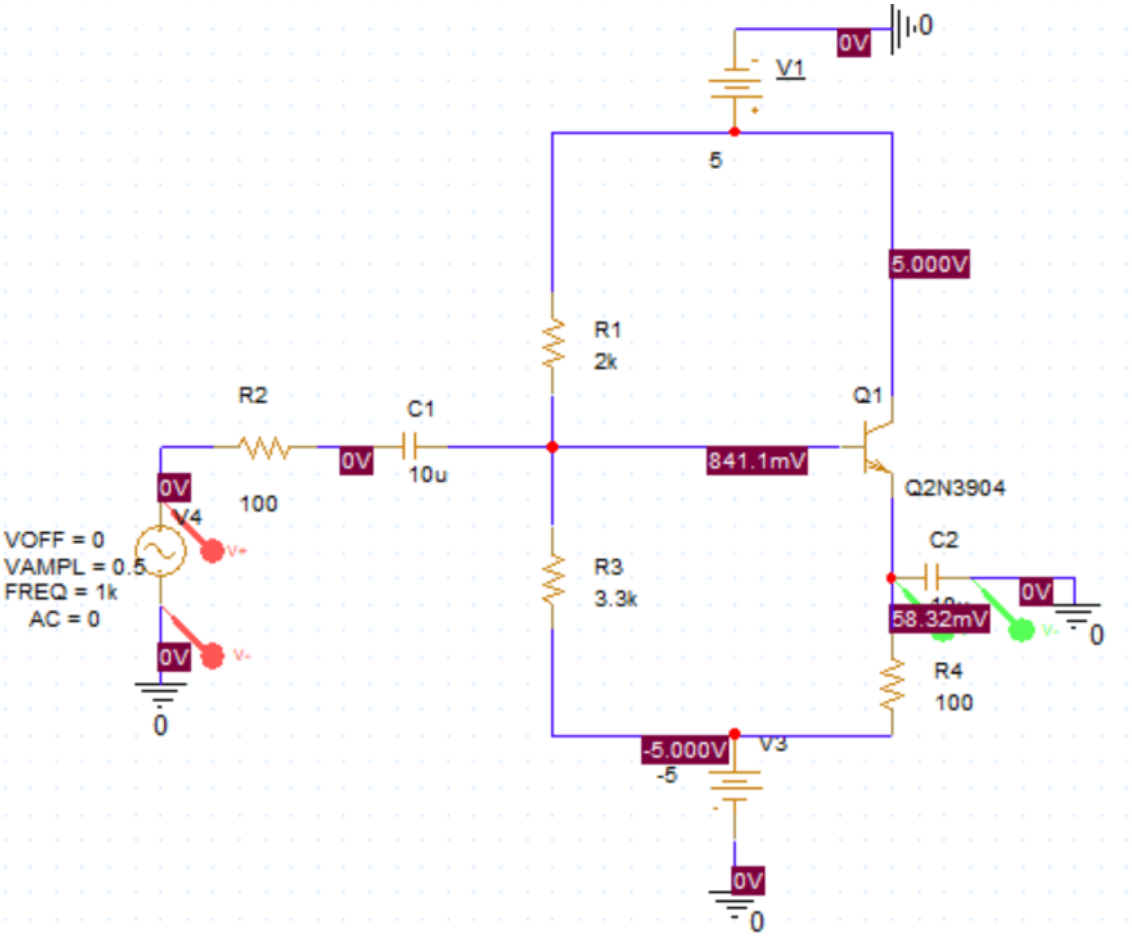


Figure 2: Pspice schematic

(5) How did you model the transistor in the simulator you used?

The transistor was modeled by finding the exact part in the Pspice components list.

What settings did you use for each simulation (transient/dc sweep/frequency sweep/etc.)?

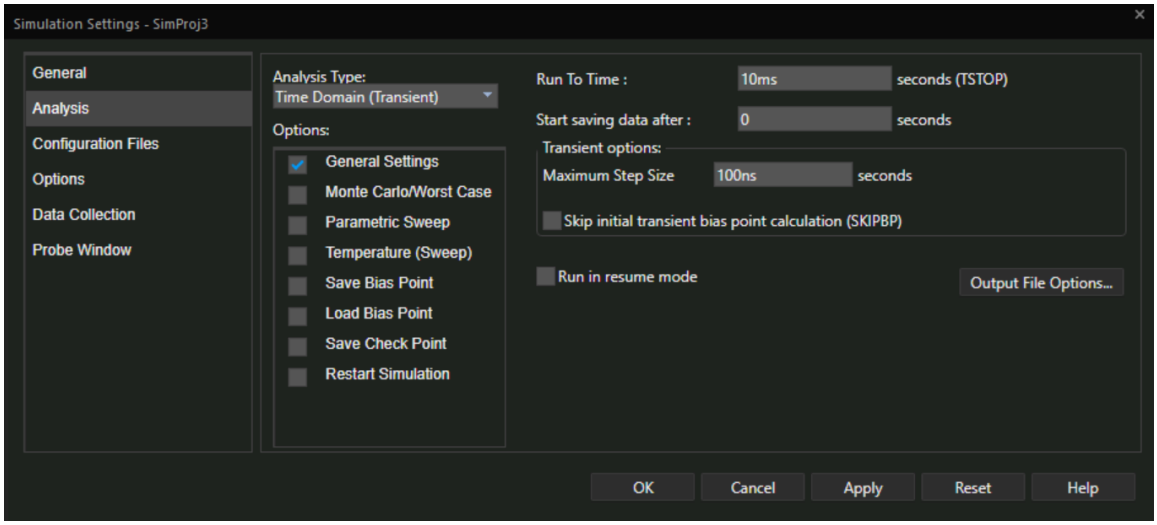


Figure 3: Pspice transient analysis configuration

The simulation was done via transient analysis with a step size of 100ns and a total run time of 10ms

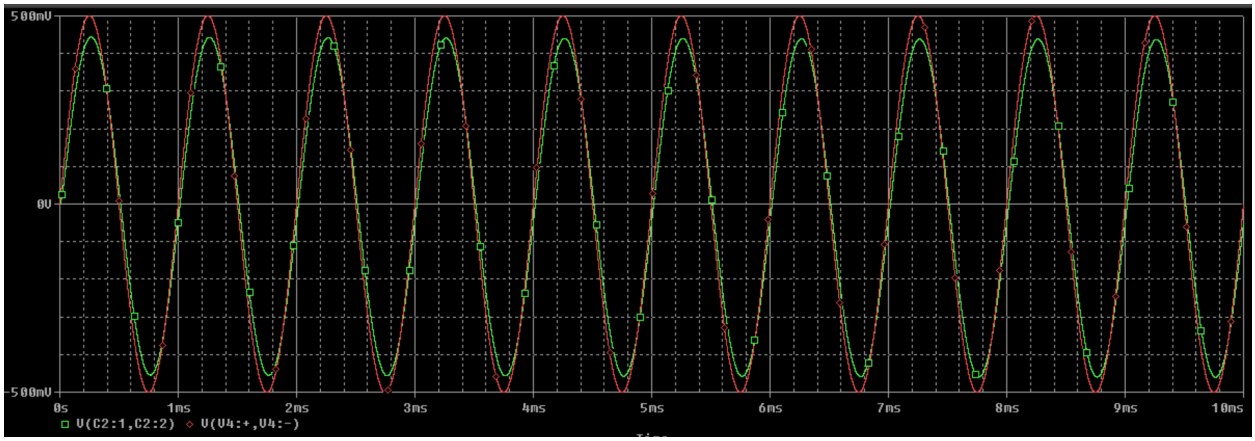


Figure 4: Vin (red) and Vout (green) waveforms

Cursor

Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)		399.401m		
	X Values	2.3333m	0.000	2.3333m	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(C2:1,C2:2)	400.332m	930.524u	399.401m	0.000	0.000	400.332m	930.524u	200.631m
	V(V4:+,V4:-)	433.007m	3.1416u	433.004m	32.675m	-927.383u	433.007m	3.1416u	216.505m

Figure 5: Vin/Vout measurements from simulation

c. (5) The overall gain determined from the simulations.

The gain determined by the simulation can be found by dividing Vo/Vin, which in this case 400/433 = ~0.92, which is within our specification

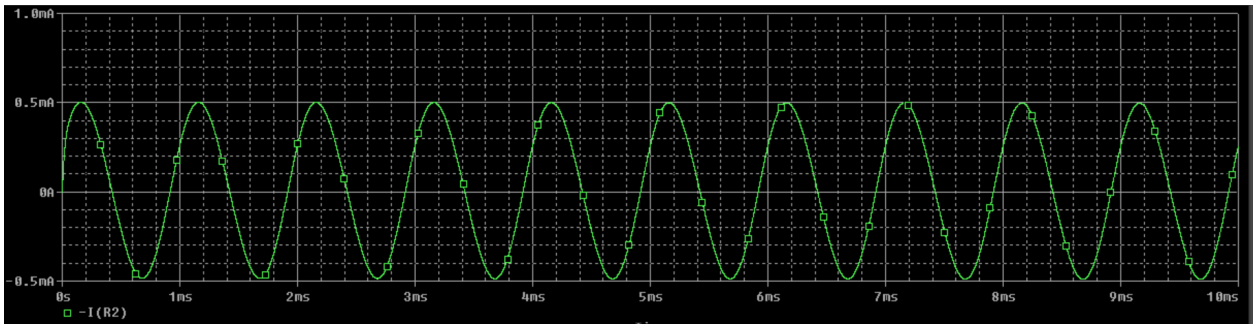


Figure 6: I(in) measurements from simulation

d. (5) Other performance parameters determined from the simulations.

We can also observe from this graph of I(in) that Rin can be calculated as Vin/Iin = 0.5/500ua = 1000 ohms.

Physical Circuit

4. Show your physical circuit on camera. Point to the wires from input to output to show how the circuit is connected in a way corresponding to your schematic.

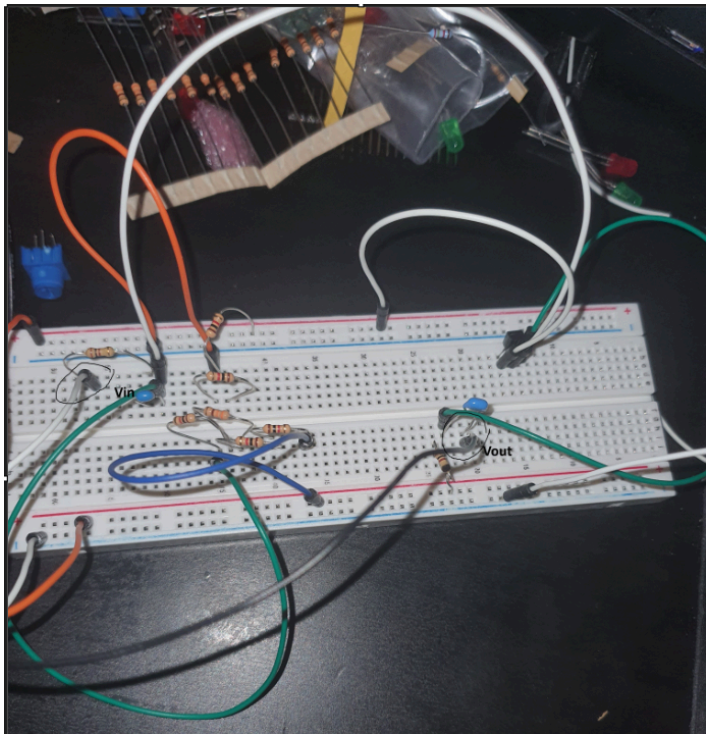


Figure 7: Physical circuit with labeled Vin/Vout nodes

5. **Share your screen to show your waveforms measurements.**

   a. (5) What measurements did you do? (E.g. waveforms as functions of time, XY plot, network analyzer, etc. You decide which measurements are beneficial and explain why you used them.)

   b. (5) How did you determine the midband gain for your amplifier? What value did you obtain? Compare your value with what was expected from calculations and simulations.

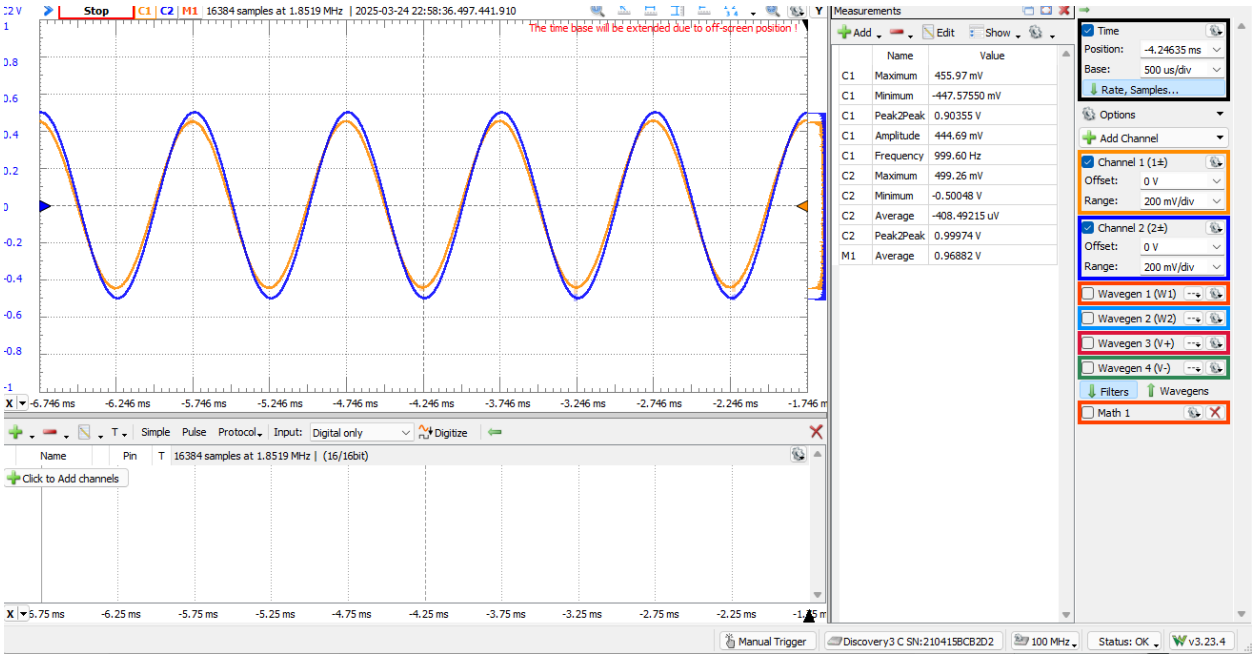


Figure 8: Vin/Vout waveforms measurement (Vin is C2 and Vout is C1)

I measured Vin and Vout using the scope (waveforms as a function of time) and checked to see if the gain was similar to the simulation, to which from the graph we can tell it's quite similar. I also created a custom math channel for the gain (C2/C1) where channel 2 is the input and channel 1 is the output, and as we can see it's on average about 0.96 gain, and when calculating gain from both maximums we can see that Av = 455/499 = 0.91 which is very similar to what we obtained earlier.

c. (5) Demonstrate linearity at an input amplitude of 0.5V.

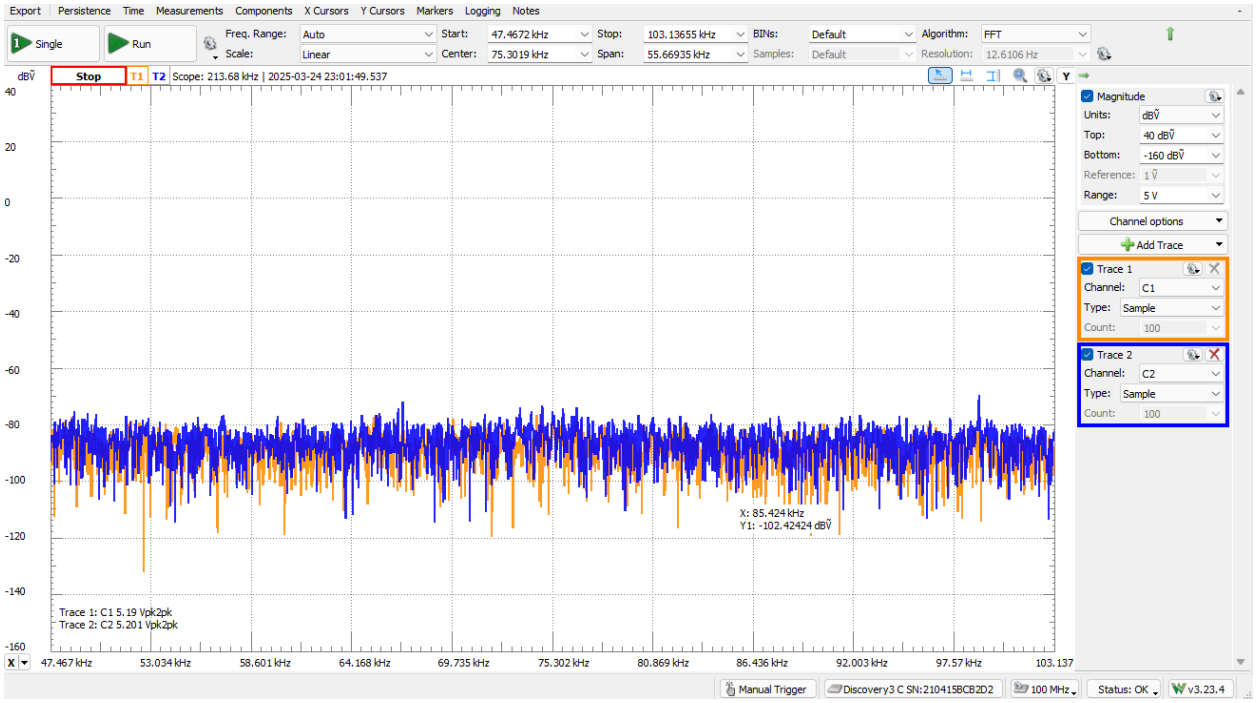


Figure 9: Vin/Vout spectrogram

To demonstrate linearity, we can see that when using a spectogram, we see that our frequencies are nearly identical, which shows good linearity for an input of 0.5v.