Assignment 2:
Computer Architecture

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1 Question 1:

A cache consists of 128 lines. The main memory contains 8192 blocks of 256 words each. Design the address format if the cache is

(a) Direct Mapped

(b) Associative Mapped

(c) Set Associative with four-line per sets

1.1 Shared:

- One memory address bit length: $\log_2(8192 * 256) = \log_2(2097152) = 21$ bits

1.2 Part A: Direct Mapped

For the direct mapped cache, we need to know three things:

- Required cache lines bit length: $\log_2(128) = 7$ bits
- Required word offset bit length: $\log_2(256) = 8$ bits
- Required tag bit length: $21 - 7 - 8 = 6$ bits

The design is: 6 Tag Bits — 7 Line Bits — 8 Word Offset Bits

1.3 Part B: Associative Mapped

1.4 Part C: Set Associative with four-line per sets

2 Question 2:

TODO :D