ECE 546 Project Proposal

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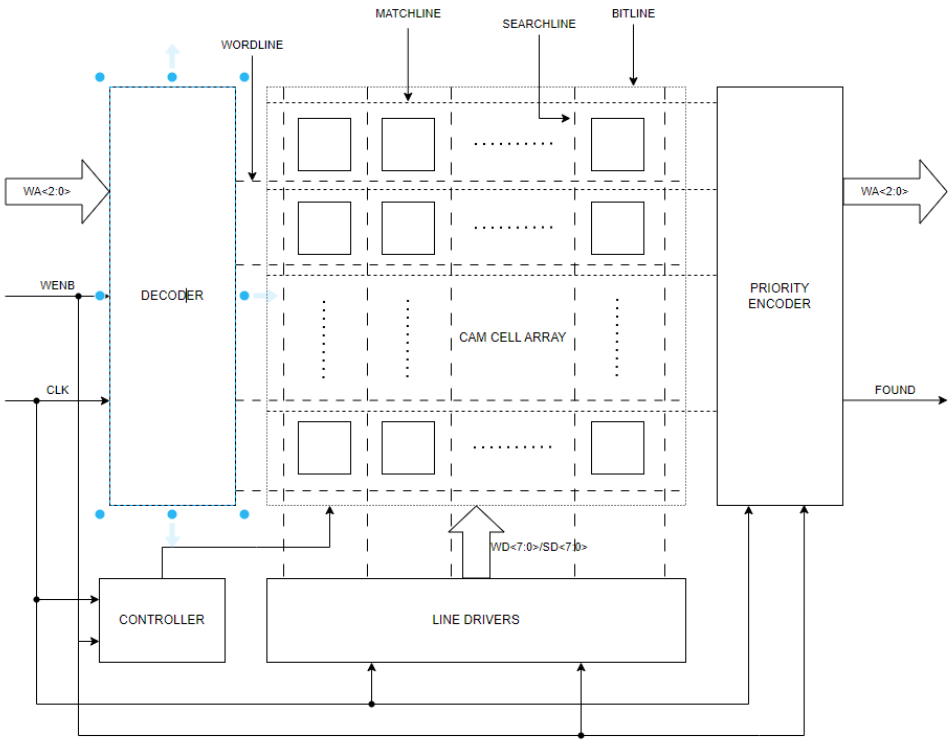
Introduction

Our project, guided by the principles outlined by Prof. W. Rhett Davis at NC State University and drawing upon the foundational works of Rabaey, Chandrakasan, and Nikolić, aims to design a 64-bit (8x8) Synchronous Content Addressable Memory (CAM) system. This endeavor is not just about achieving functional correctness; it is a challenge to optimize the energy-delay-area (EDA) product, underscoring the importance of efficiency in VLSI Systems Design. As we embark on this project, we aim to navigate the complexities of digital circuit design, aiming for a solution that stands testament to the innovative and optimization-driven ethos of modern VLSI systems.

Rough Floorplan



Design Options to be Explored

CAM Bit-Cells

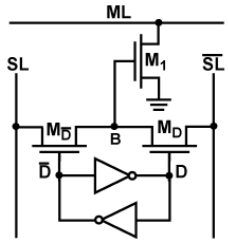
- **Description:**
    - A CAM cell serves two basic functions: bit storage (as in RAM) and bit comparison (unique to CAM). The bit storage is an SRAM cell where cross-coupled inverters implement the bit-storage nodes D and $\underline{D}$.
    - There are generally four types of CAM core cells: 10-T NOR type, 9-T NAND type, and their variants 9-T NOR type and 10-T NAND type.
    - The NOR cells are connected in parallel and the NAND cells are connected in serial.
    - The 10-T NOR cell is that it provides a full rail voltage at the gates of all comparison transistors.
    - One of the shortcomings of 9-T NAND is that it provides a reduced logic “1” voltage at node B(single transistor), which can reach only $V_{DD} - V_{Tn}$ when the searchlines are driven to V_{DD}.
    - The 10-T NAND cell doubles the number of transistors in series compared to the 9-T NAND cell.
    - The 9-T NOR cell has only a single transistor in the pulldown path, the node B can only rise to $V_{DD} - V_{Tn}$.
    - In general, 9-T type requires less power consumption and area than 10-T type (less transistors), while it offers lower performance and reliability (single transistor for pull down).

  For a small-scale implementation like an 8x8 bit CAM, the decision might lean more heavily towards considerations of power and area, especially in embedded or power-sensitive applications, making the 9-T option more attractive.

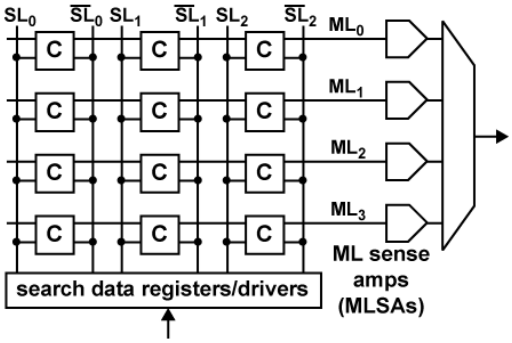
  For the simplicity of design, we plan to choose 9-T NOR cell for our project.

- **Schematics:**

The schematic for 9-T NOR cell:



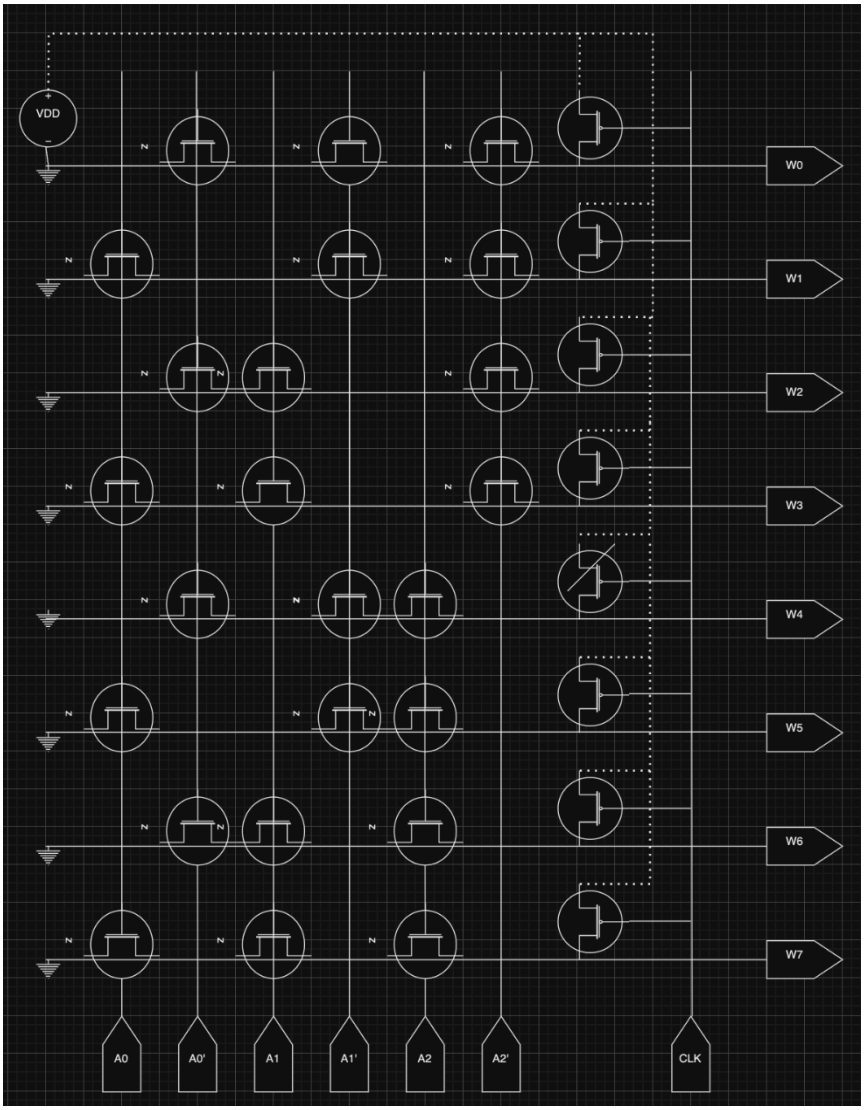
This is an instance of the schematic. The actual cell array contains 8x8 cells.



- **References:** Pagiamtzis & Sheikholeslami, JSSC '06

Decoder

- **Description:**
  - Whenever a memory allows for random address-based access, address decoders must be present.
  - NOR dynamic decoders are substantially faster, but they consume more area than their NAND counterparts and dramatically more power.
  - A 3-to-8 tree based column decoder used as a row decoder will be investigated.
  - Simple and gate configuration will also be investigated.
  - A 3-to-8 dynamic NAND decoder will be chosen to optimize area and power within the peripheral circuitry.
- **Schematics:**



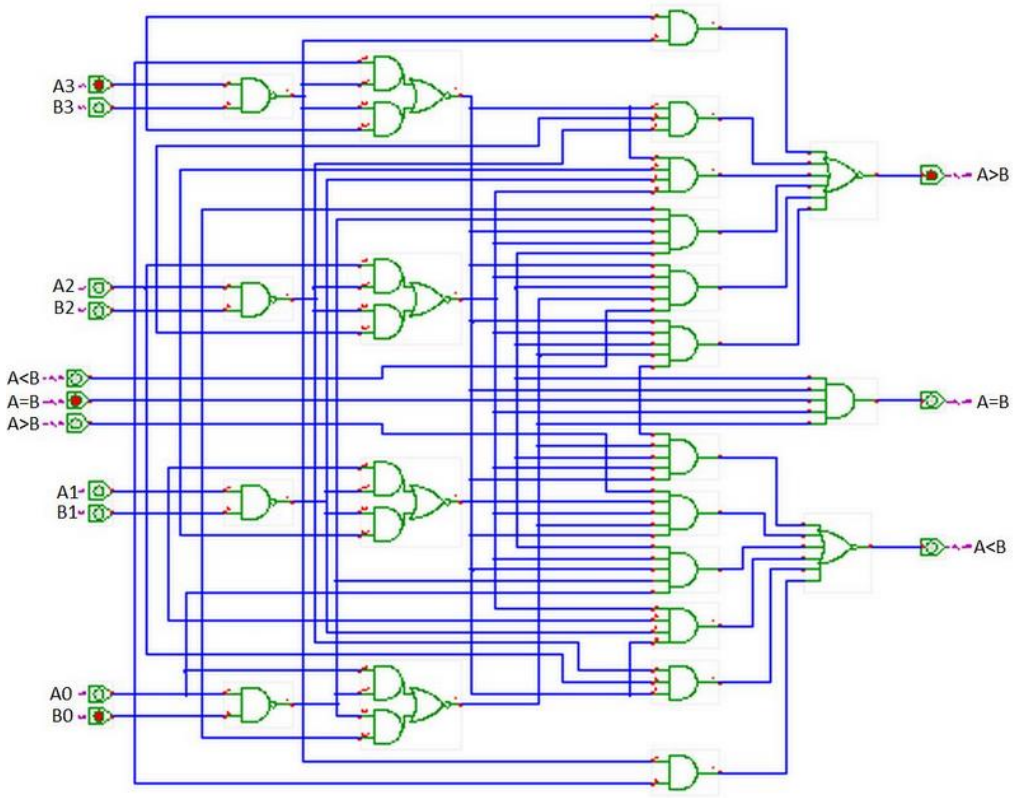
- **References:** **“**Digital Integrated Circuits” by Jan M. Rabaey

Encoder

- **Description:** The inputs of the encoder consist of the match lines from the CAM bitcell. Encode should produce two outputs: Match Address (MA 2:0) and Found signal based on the control signals: Clk and write enable signal.

- **Schematics:**

Example Schematic for comparing two addresses :



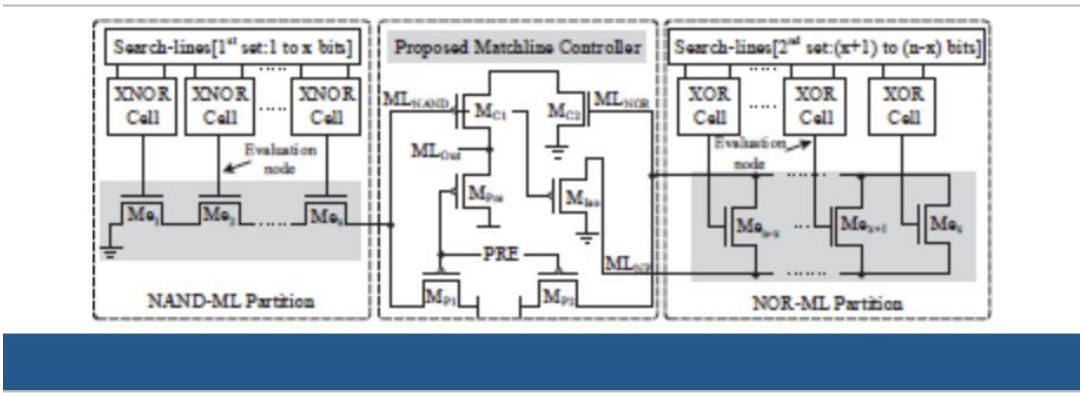
- **References:**

Controller

- **Description:**
    - For SRAM the complete address word is presented at once, and circuitry is provided to automatically detect any transitions on that bus. No external timing signals are needed. All internal timing events, such as the enabling of the decoders and sense amplifiers are derived from the internally generated transition signal.
    - SRAM Memories use a clever approach called address-transition-detection (ATD) to automatically generate the internal signals such as PC and SE upon detection of a change in the internal environment.
    - A triggering of the ATD pulse causes the precharging and the equalizing of the bit lines of the selected block with the aid of the BEQ control signal. Lowering BEQ starts the read process. One of the word lines is enabled, and the appropriate bit lines start to discharge.
    - To write to the memory, the appropriate value and its complement are imposed on the I/O and its complement. After which the appropriate row, column, and block addresses are enabled.

- **Schematics:**

Example Controller:



- **References:**
  - **“**Digital Integrated Circuits” by Jan M. Rabaey
  - S. W. Hussain, T. V. Mahendra, S. Mishra and A. Dandapat, "Efficient Matchline Controller for Hybrid Content Addressable Memory," 2019 IEEE 2nd International Conference on Electronics and Communication Engineering (ICECE), Xi'an, China, 2019, pp. 418-422, doi: 10.1109/ICECE48499.2019.9058537. keywords: {Cams;Discharges (electric);Transistors;Associative memory;MISO communication;Delays;Arrays;Content Addressable Memory (CAM);high-speed;hybrid-type CAM;low-power;matchline (ML);NAND-ML;NOR-ML},

FLIP Flops

- **Description:**
  - Flip-flops are fundamental building blocks in digital electronics, serving as the core memory elements in various kinds of digital circuits, including storage registers, counters, and shift registers. Unlike SRAM, which accesses data using a complete address word, flip-flops operate on the principle of storing a single bit of data based on clock signals and input triggers. They play a crucial role in sequential logic circuits by providing stable states (0 or 1) that can change only at specific moments, determined by the clock or control inputs.
  - There are several types of flip-flops, including Set-Reset (SR), Data (D), Toggle (T), and JK flip-flops, each with unique characteristics and operational requirements. For instance, a D flip-flop captures the value of the data input (D) at a rising or falling edge of the clock signal and maintains this value until the next clock edge, effectively acting as a 1-bit memory cell.

- Flip-flops use feedback and gating techniques to control the flow of data and stabilize the stored bit. The precise timing of signal transitions, controlled by the clock, ensures that flip-flops can reliably store and transfer data in synchronous systems. Internal circuitry, such as the clock's edge detection mechanism, enables flip-flops to respond to specific changes in input conditions, thereby allowing for controlled state transitions.

- **Schematics:**
  Low power MS Flip Flop that we are using

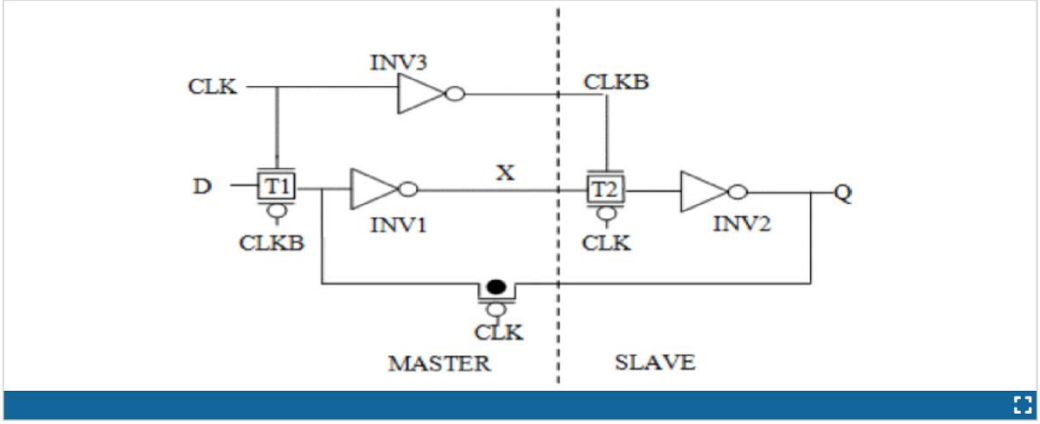


Figure 4. Proposed Design.

Show All

- **References:**
  - K. Singh, S. C. Tiwari and M. Gupta, "A high performance flip flop for low power low voltage systems," 2011 World Congress on Information and Communication Technologies, Mumbai, India, 2011, pp. 257-262, doi: 10.1109/WICT.2011.6141254. keywords: {Clocks;Transistors;Flip-flops;Delay;Power dissipation;Inverters;Power demand;Flip flops;low voltage;power-delay product;VLSI},

Division of Labor

Tristan Wood: Will spearhead the development of the decoder and controller components. These elements are crucial for directing the flow of data within our CAM system and ensuring that the correct data is stored and retrieved in response to user queries. Given the interconnected nature of these components, focusing on them collectively will enable the development of a more integrated and efficient system architecture.

Sukhanshu Dukare: Tasked with designing the encoder component of our system. The encoder plays a vital role in converting the match line signals to appropriate match address and checking if the desired data has been found, making it essential for the overall functionality and performance of the project.

Yazhuo Gao: Will concentrate on the bit cells, which are the fundamental storage elements of our CAM system. The design and optimization of bit cells are critical for ensuring the system's storage efficiency and speed of data retrieval.

Our approach is collaborative and flexible; should any team member complete their primary tasks ahead of schedule, they will assist with unfinished components. This strategy ensures that all parts of our project progress at a balanced pace and that knowledge and expertise are shared across the team. It also prepares us to efficiently address any unforeseen challenges that may arise during the design and implementation phases.

Conclusion

In conclusion, for our ECE 546 Project Proposal at NC State University, we have chosen to embark on designing a 64-bit (8x8) Synchronous Content Addressable Memory (CAM) system, prioritizing the optimization of the energy-delay-area (EDA) product in alignment with the principles of VLSI Systems Design. Our decision to utilize the 9-T NOR cell for the CAM bit-cells stems from its advantages in power consumption and area efficiency, which are paramount for our project's success. The division of labor among team members—Tristan Wood focusing on the decoder, multiplexer, and controller; Sukhanshu Dukare on the encoder; and Yazhuo Gao on the bit cells—ensures a concentrated effort on each critical component, fostering an integrated system architecture. This strategy not only leverages individual strengths but also promotes a collaborative environment for overcoming challenges and achieving our project goals efficiently.