ECE 546 Milestone 2

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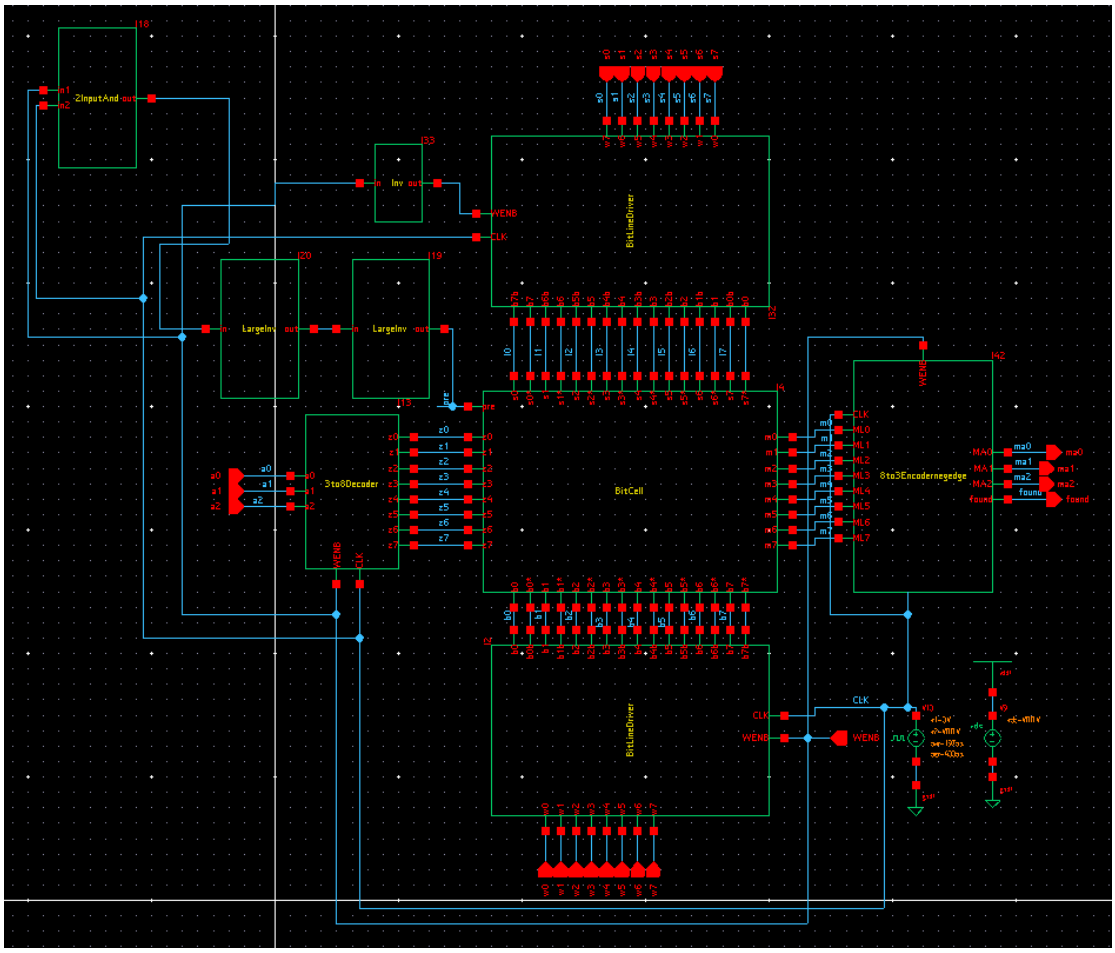
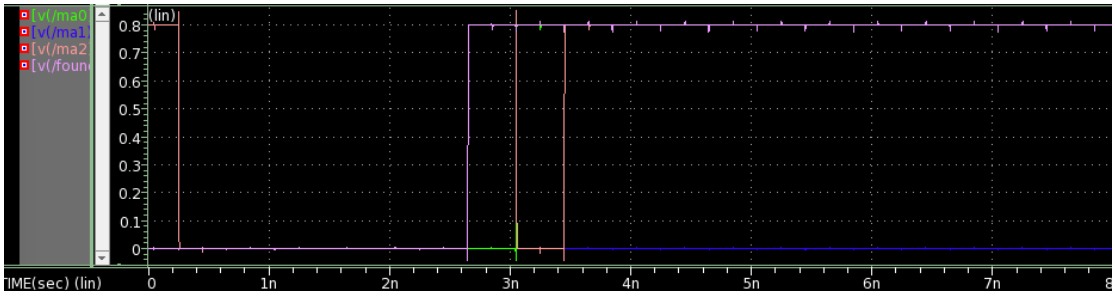
- Plot of complete schematics

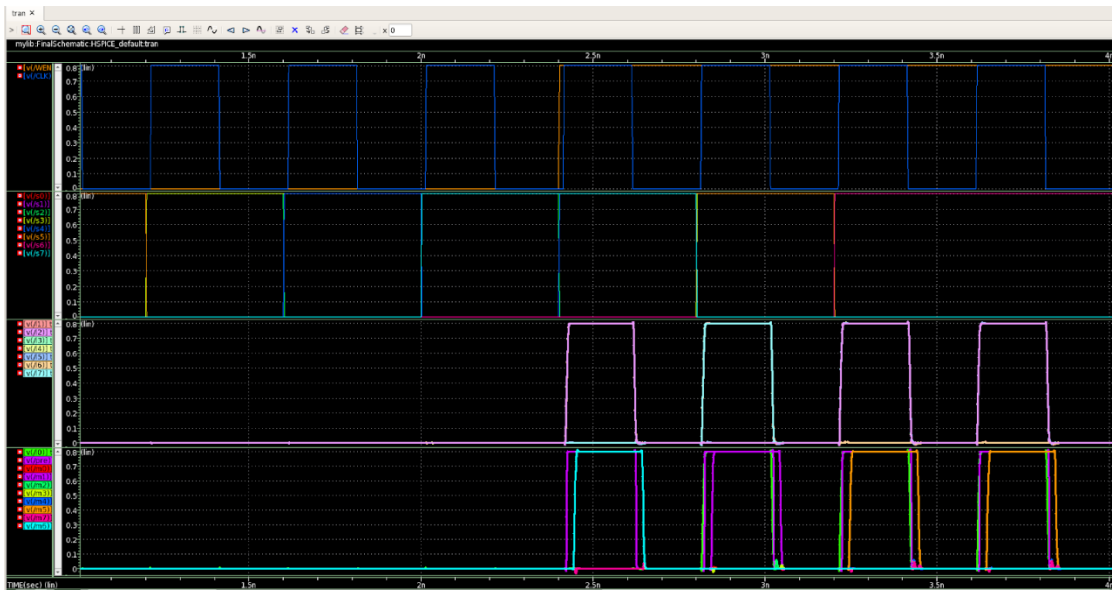


- Plot of simulated waveforms

Based on this list of vectors. We should match address 6 then 1 then 5, which we do.

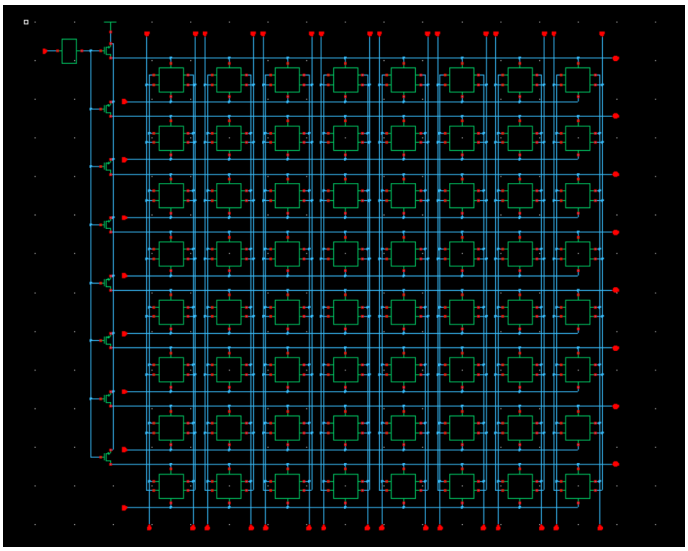
Test Vectors
write
2 72 14 0
6 cd 4c 0
5 42 85 0
1 34 70 0
not found
2 98 18 1
2 54 65 1
read
2 be cd 1
2 03 34 1
4 bc 42 1

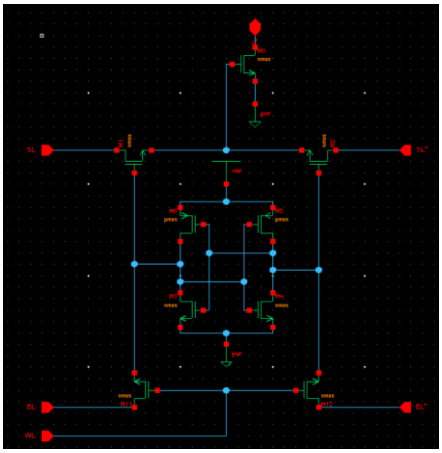




- Design
    1. CAM Bit-Cells

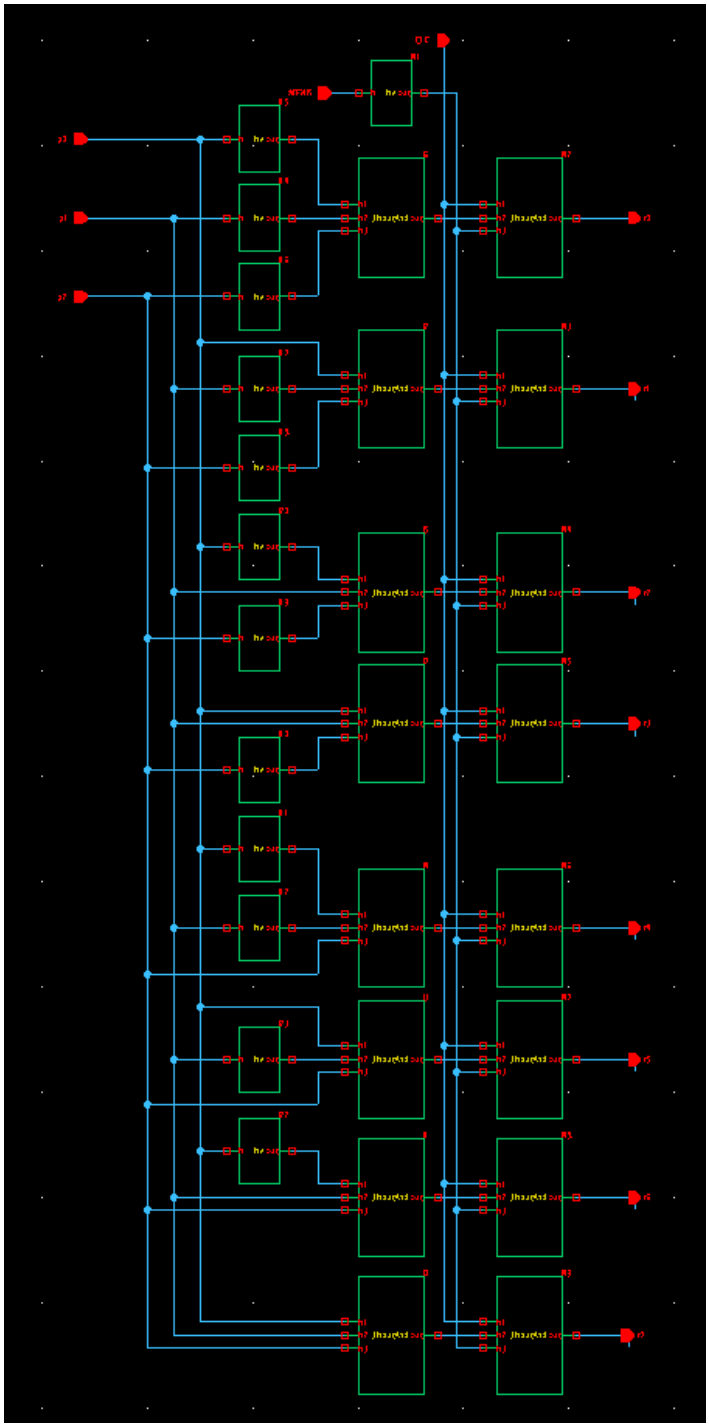
The CAM bit-cell uses 8x8 9-T NOR type cells. It writes data with the control of wordline and bitline, also reads data with the control of searchline and outputs results to the matchline. The 9-T NOR type cell has advantages on power and area over traditional 10-T NOR type.





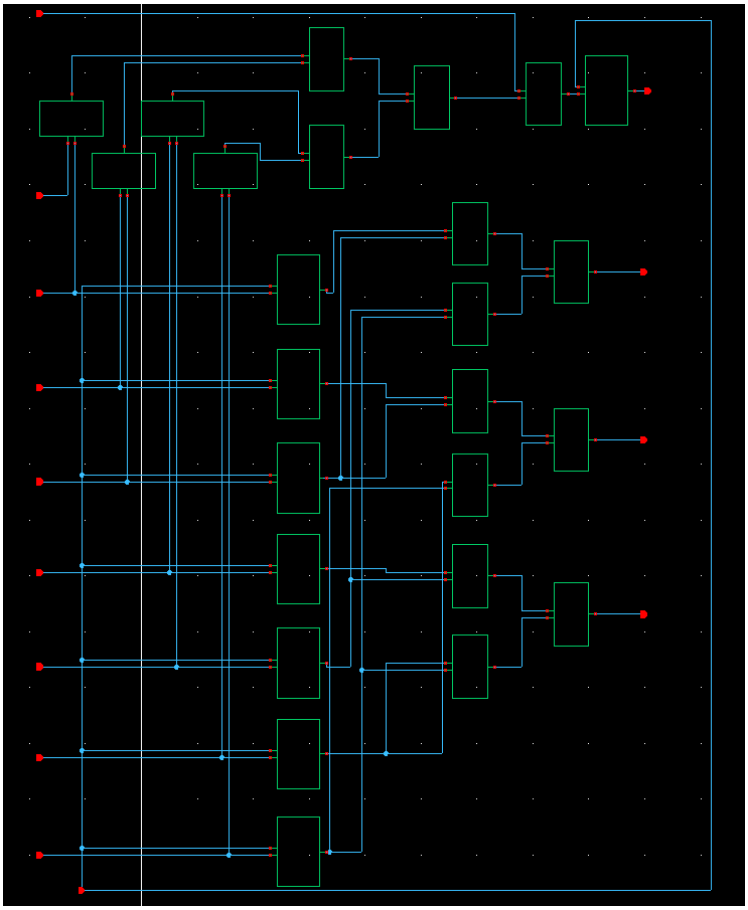
2. Decoder

A 3-to-8 dynamic NAND decoder is implemented to optimize area and power within the peripheral circuitry.



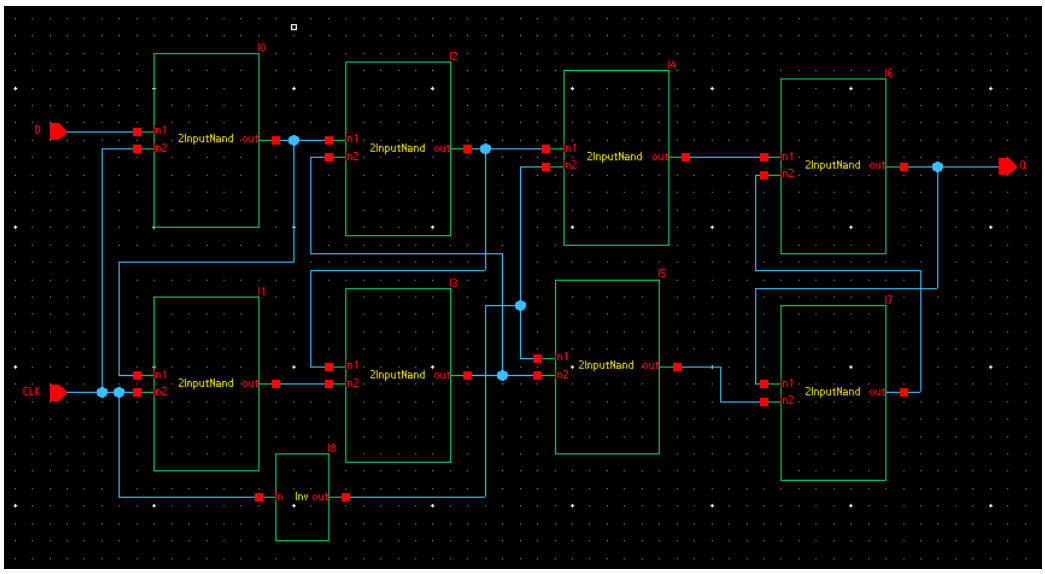
3. Encoder

A simple 8:3 Encoder is built to take Match Lines from the bitcell as inputs along with Write enable and converted into match address. Found signal is triggered when one of the match lines go high.



4. Flip-flop

The low power MS Flip Flop is utilized in our design.



5. Bitline Driver

The Bitline driver receives input word bits from the decoder and assigns it to the bit cells when WENB is low.