Ultra-High-Speed 64-bit (8x8) Synchronous CAM at 3 nm: A 10 GHz Design with Sub-4 pW Power Consumption

Tristan Wood, Sukhanshu Dukare, Yazhuo Gao.
ECE Department, NCSU.

INTRODUCTION

In the rapidly evolving landscape of semiconductor technologies, the 8x8 CAM design stands out by advancing the integration and efficiency of memory systems within SoCs. Our design intricately combines a CMOS-based 3-to-8 row decoder, a 9-T NOR bit cell, line drivers, and a streamlined encoder to tackle the challenges of power efficiency, area minimization, and performance maximization. The row decoder employs a mix of NAND gates and inverters tailored to reliably select memory rows, reducing power consumption and silicon footprint. Our custom bit cell design features advanced precharging strategies and transistor configurations to enhance power efficiency without compromising signal stability, accommodating 64 cells in a compact array that maximizes space utility. The line drivers, crucial for write and search operations, utilize minimalistic logic to improve performance, while the encoder manages non-mutually exclusive inputs with reduced complexity, ensuring system robustness. Together, these components exemplify a sophisticated approach to CAM design, pushing the boundaries of memory technology to meet the high-performance demands of modern integrated circuits, setting a foundation for future advancements in memory architecture.

DESIGN-DESCRIPTION

Tristan Wood was responsible for designing and laying out the dynamic decoder, bitline and searchline drivers, final design schematics, and debugging DRC/LVS errors. Sukhanshu Dukare designed the priority encoder, while Yazhuo Gao handled the 9-T NOR cell and bit cell array, along with the final design layout. The final report was a collaborative effort among Tristan, Sukhanshu, and Yazhuo.

3-to-8 Row-Decoder

The row decoder utilizes a CMOS 3-to-8 configuration, strategically designed to select memory rows from address signals with reliability. This setup includes a mix of 2-input and 3-input NAND gates paired with inverters. Opting for this straightforward gating approach not only mitigates the charge loss associated with dynamic logic but is also essential due to the uncertain final clock speed.[1] All circuit components are minimum-sized except for the size 3 inverters, which are crucial for enhancing the rise and fall times of the clock and wordline signals. The physical layout focused on aligning gates in rows with outputs at the bottom and inputs at the top. This arrangement allows for an increase in height where necessary, effectively managing the limited space. Importantly, inputs that arrive last, such as the clock signal, are strategically placed closer to VDD and GND to reduce switching times.

Bit Cell and Bit Cell Array

In our 8x8 CAM memory design, we employ a custom 9-T NOR bit cell utilizing two NMOS and two PMOS transistors to store bit values, with additional NMOS transistors handling inputs on both the bit-line and search-line.[2] A distinctively configured 6-fin NMOS on the match-line stabilizes and speeds up precharging, enhancing power efficiency while slightly increasing cell size.

The CAM bit cell array, compactly arranged in a rectangular layout, holds all 64 cells, facilitating efficient integration with bit-lines and word-lines. Precharging is managed through a 2-input NAND gate, responsive to high clock and WENB signals, which activates a series of three inverters. These inverters ensure that the match-line goes high synchronously with the search line and only when a match occurs, effectively conserving power by preventing unnecessary activation. Additionally, row buffers at the ends of each 8-cell row enhance the rise and fall times of the match-line signals, ensuring sharp and precise signal transitions critical for reliable operation during search activities.

Line Drivers

The bit-line and search-line drivers are crucial for managing write and search operations respectively. Each driver processes 8 address inputs and delivers 16 outputs, including both the original signals and their inversions. Despite sharing the same hardware configuration, activation conditions differ: the bit-line is active low WENB, whereas the search-line is active high WENB. To improve performance, size 3 inverters are utilized to enhance the rise and fall times at the outputs and for the CLK. The physical layout is meticulously designed, with gates aligned in rows and outputs strategically positioned near the bit cell array to align with it effectively. The design also adopts a stack of five gates to scale with the width, optimizing the use of limited space. Additionally, critical outputs are placed close to VDD and GND to minimize switching times, which significantly accelerates the response time. [1]

Encoder

In our 8x8 CAM memory design, the encoder is ingeniously adapted to handle non-mutually exclusive input activations with a prioritization protocol that favors match-line 0 (ML0) over others. Instead of a conventional priority encoder, which would increase gate count and complexity[4], a streamlined logic modification coerces all output lines to a logic low state when ML0 is asserted, efficiently achieving priority encoding with fewer gates.

The encoder's reliability is ensured by integrating 11 edge-triggered D flip-flops at both input and output stages, latching and retaining signals during the computational evaluation of output addresses. The logic network is comprised of 11 two-input OR gates, one two-input AND gate, and three three-input AND gates, supplemented by three single-size inverters and one triple-size inverter. This arrangement optimizes the physical layout, which prioritizes vertical space by aligning gates in rows with inputs at the bottom and outputs at the top.

RESULTS AND CONCLUSION

At room temperature (25°C), our synchronous CAM system operates impressively at 10 GHz with a power dissipation of just 3.784 picojoules, as detailed in the post-layout using a 0.8V supply voltage. As presented in Table 1, our design achieved a total energy consumption of 3.027 picojoules and occupies a total die area of 33.9110 square micrometers, with a transistor density of 47.36 transistors per μm^2.

While our 64-bit CAM, utilizing 3 nm technology node, has successfully met high-performance targets, several areas for future improvement have been identified. Primarily, integrating the searchline and bitline drivers and relocating them to the bottom left corner could enhance area efficiency by eliminating unnecessary space. Additionally, aligning the active layer and buried power rails (BPR) of the decoder and encoder with the bitcell array, could facilitate closer component connections, potentially reducing the overall footprint.

Investigations into dynamic decoding, alternative line drivers, and different flip-flop configurations could further optimize performance and power consumption.[3] Future redesigns will aim to refine these aspects by employing advanced power gating techniques, re-engineering pass transistor logic in flip-flops to reduce transistor counts, and unifying driver functionalities to maximize spatial efficiency.

REFERENCES

[1] Class notes "ECE 546" , Dr. W.R Davis.
[2] K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory (CAM) circuits and architectures: a tutorial and survey," in IEEE Journal of Solid-State Circuits, vol. 41, no. 3, pp. 712-727, March 2006, doi: 10.1109/JSSC.2005.864128.
[3] Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic. 2008. Digital Integrated Circuits (3rd. ed.). Prentice Hall Press, USA.
[4] Kathuria, J., & Sharma, M. (2019, September). Novel tree based priority encoder design technique. In *2019 International conference on computing, power and communication technologies (GUCON)* (pp. 593-599). IEEE.

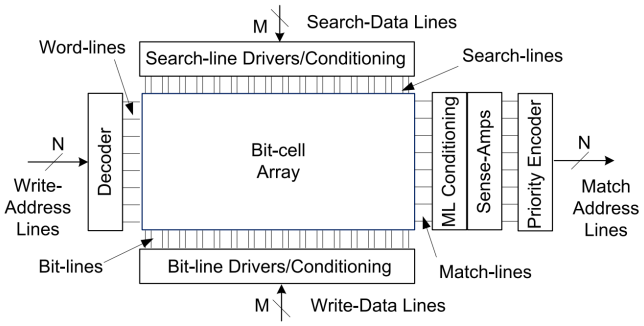

Fig. 1. Block Diagram

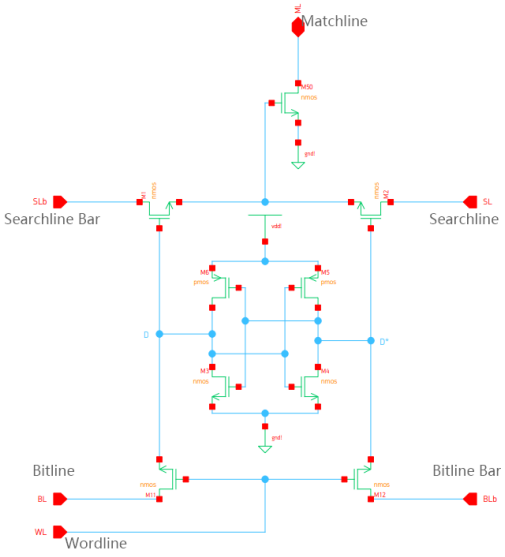

Fig. 2. BitCell Schematic

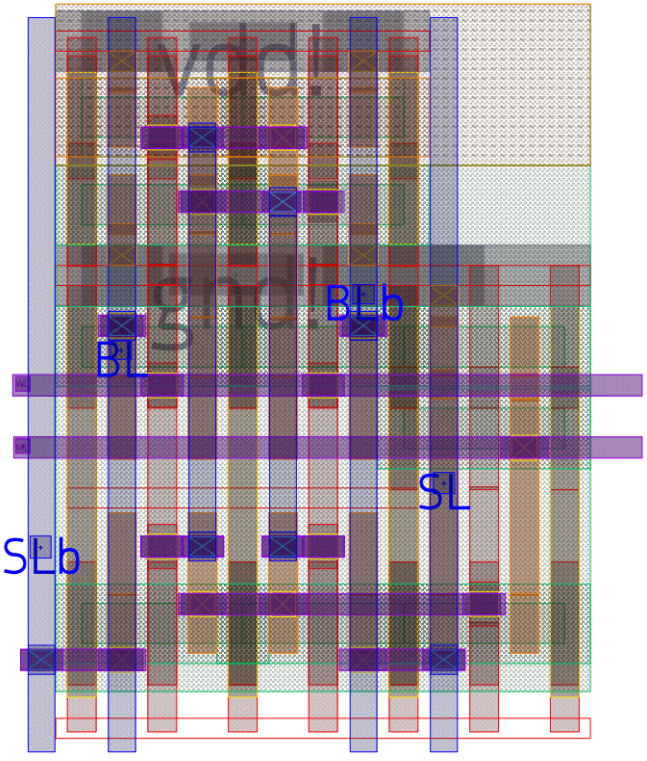

Fig. 3. BitCell Layout

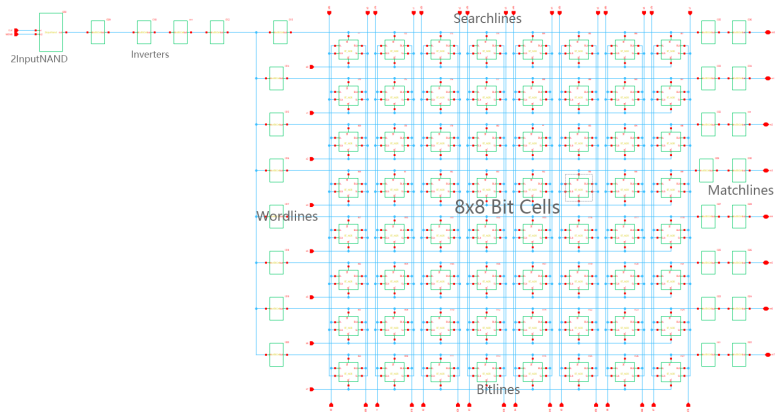

Fig. 4. CAM BitCell

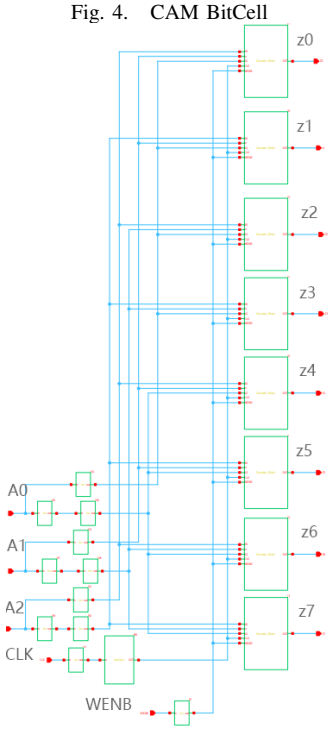

Fig. 5. Decoder Schematic

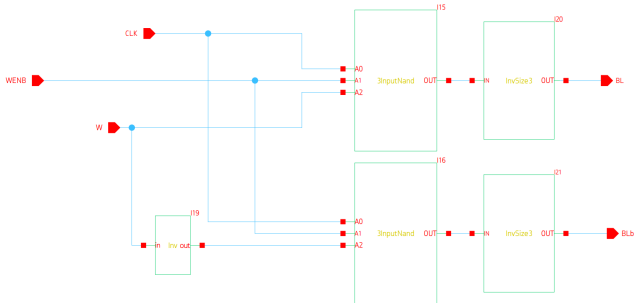

Fig. 6. Driver Cell

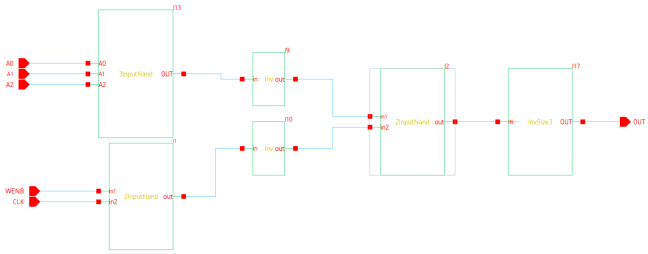

Fig. 7. Decoder Block

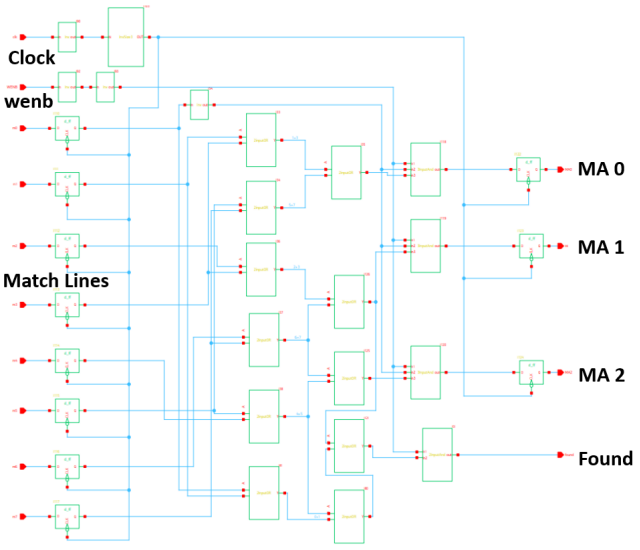

Fig. 8. Encoder Schematic

TABLE I
DESIGN STATISTICS

Parameter	Value
Maximum Clock Frequency	10 GHz
Minimum Clock Period	100 ps
Supply Voltage (Active)	0.8 V
Supply Voltage (Standby)	0.8V
Total Energy	3.027 pJ
Area (Bounding Box)	33.9110 μm^2
Number of Transistors	1606
Transistor Density	47.36 transistors per μm^2
Estimated Design Time	130 hrs

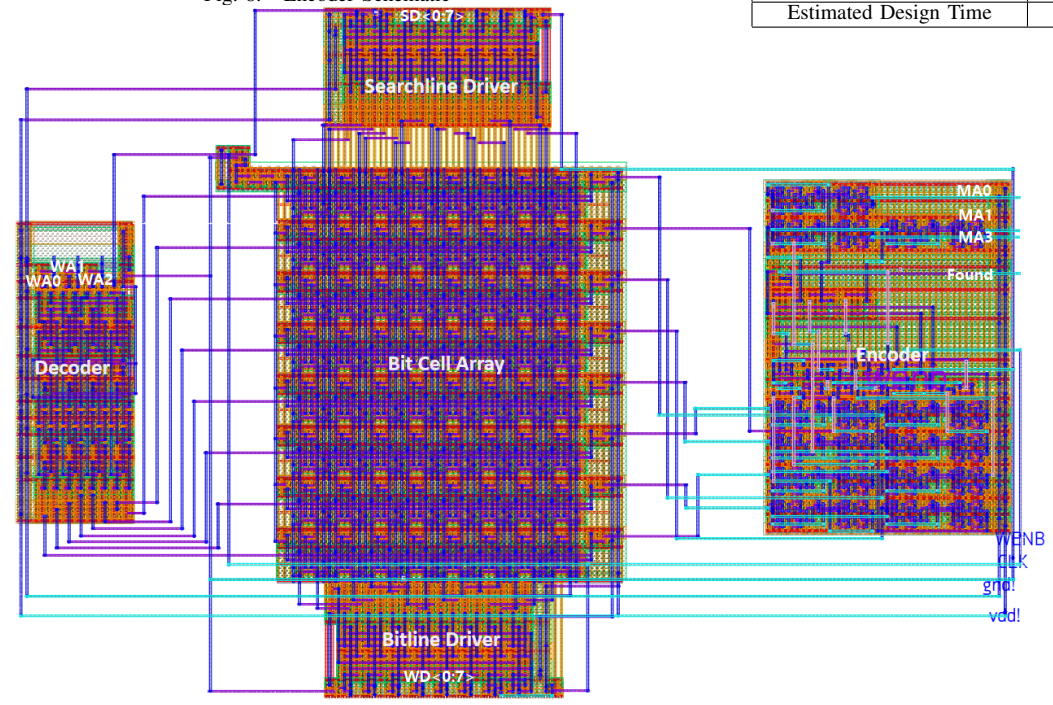

Fig. 9. Layout of the Synchronous CAM

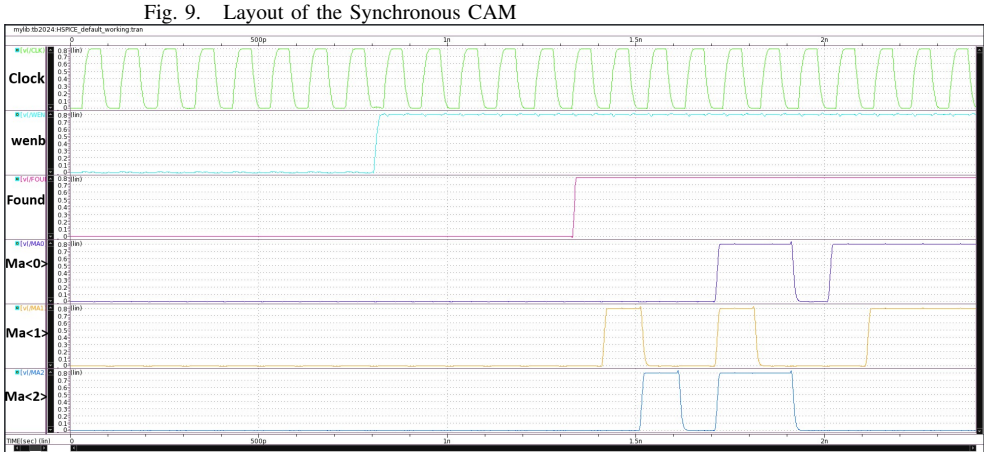

Fig. 10. Output Waveform Indicating Correct Operation