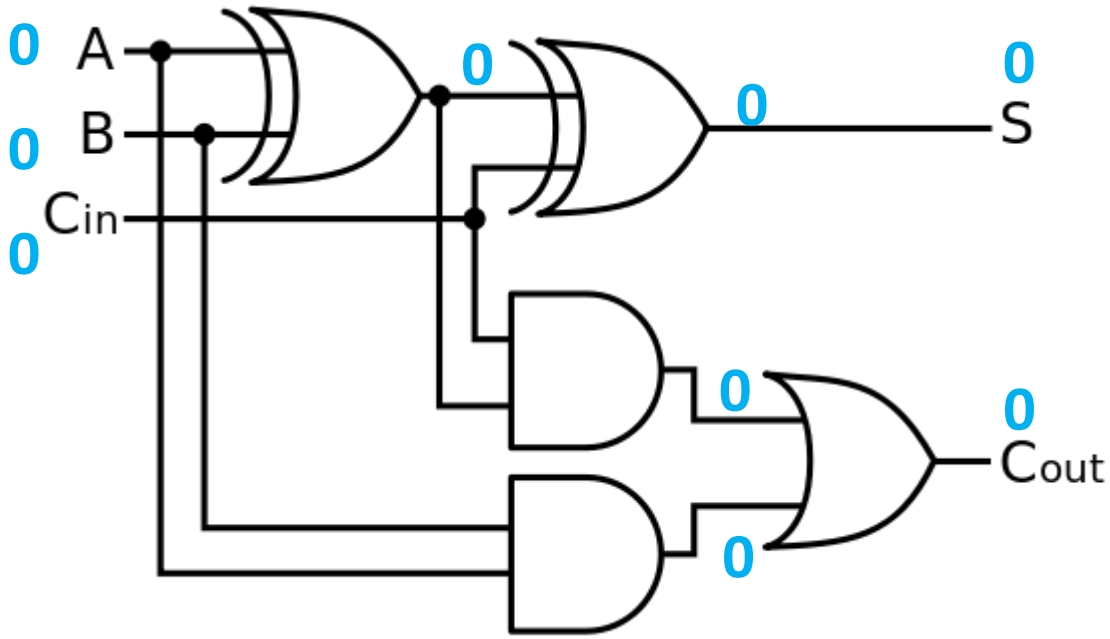
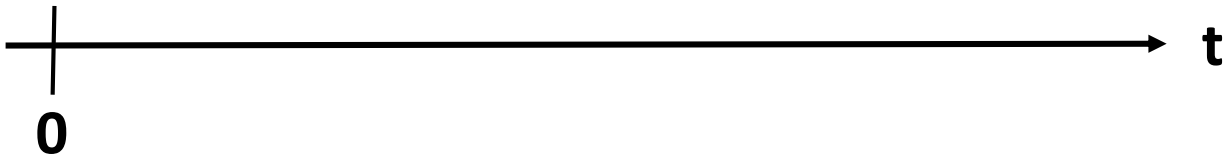
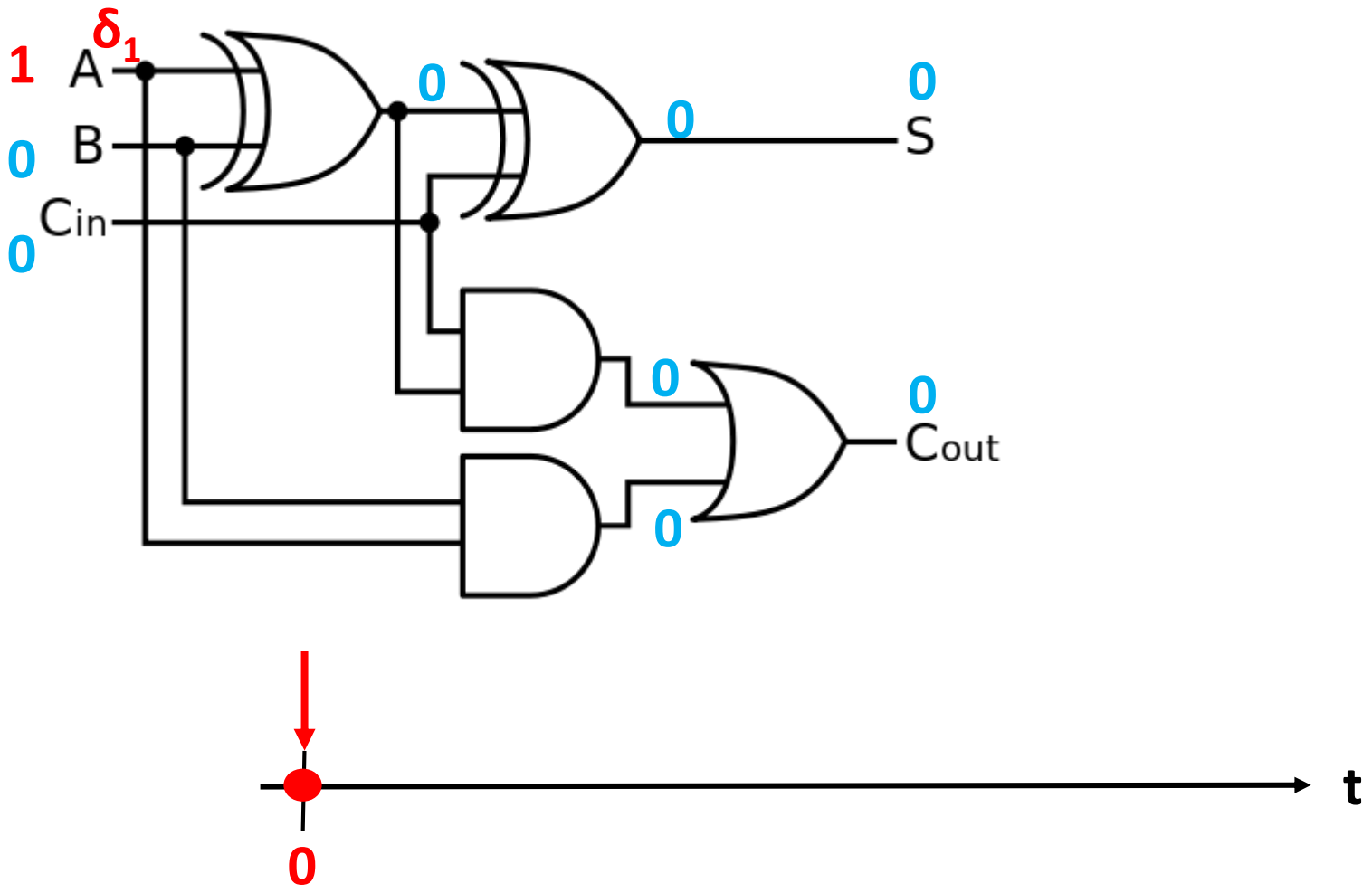
Example of gate-level RTL Delta Cycle



Event
None

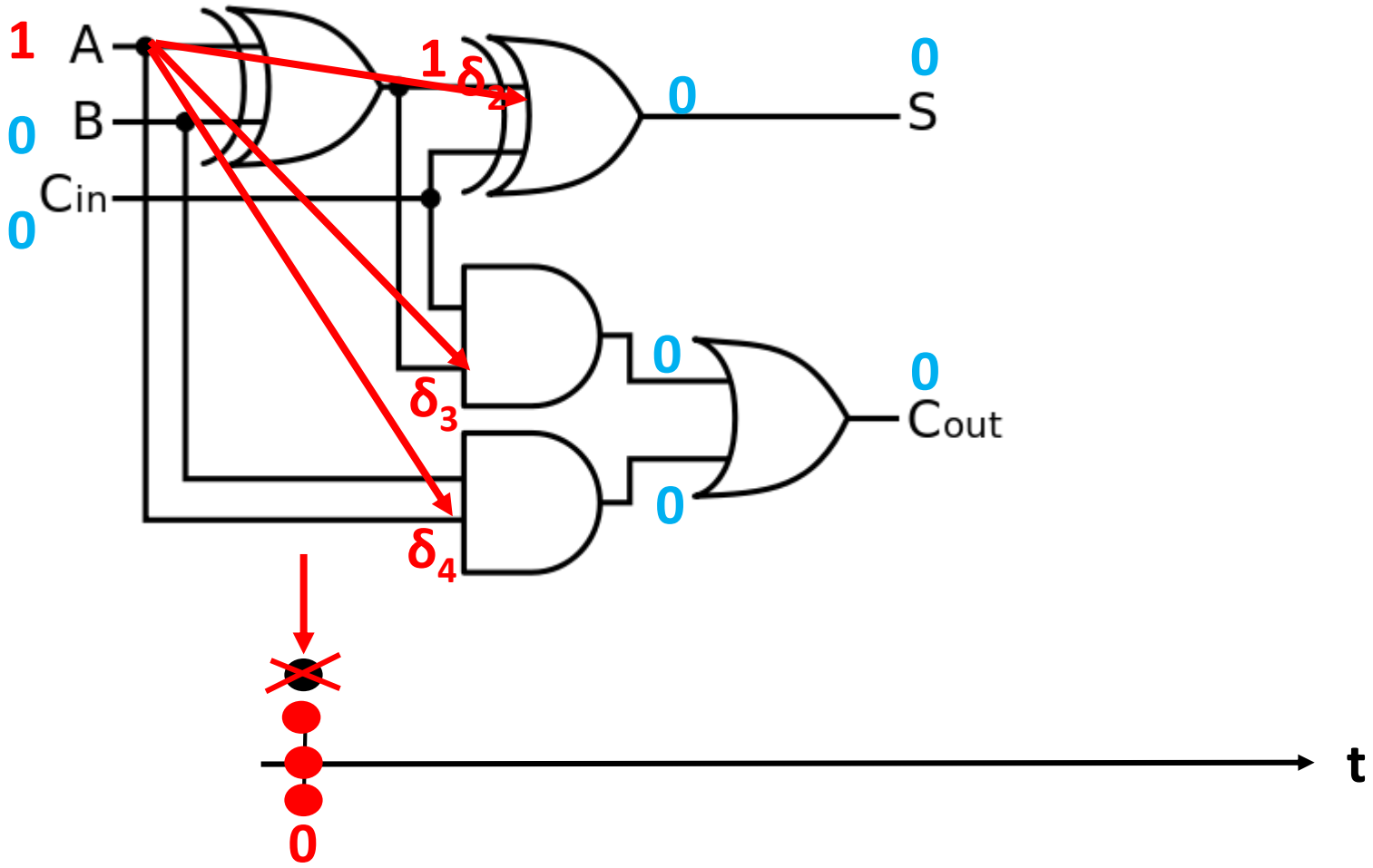


Input change at t=0: first delta event



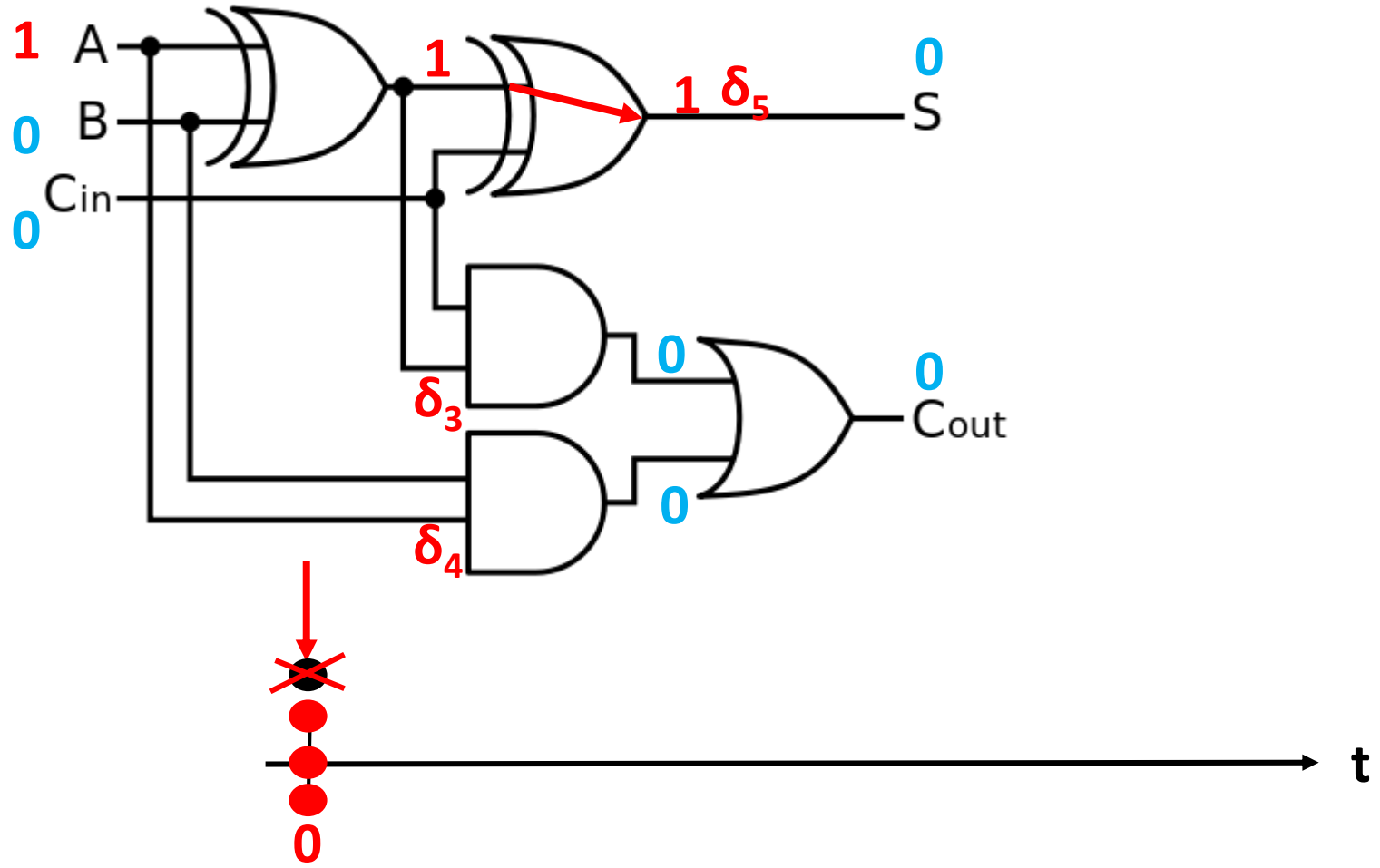
Event	Time
δ_1	0

Processing δ_1: propagation



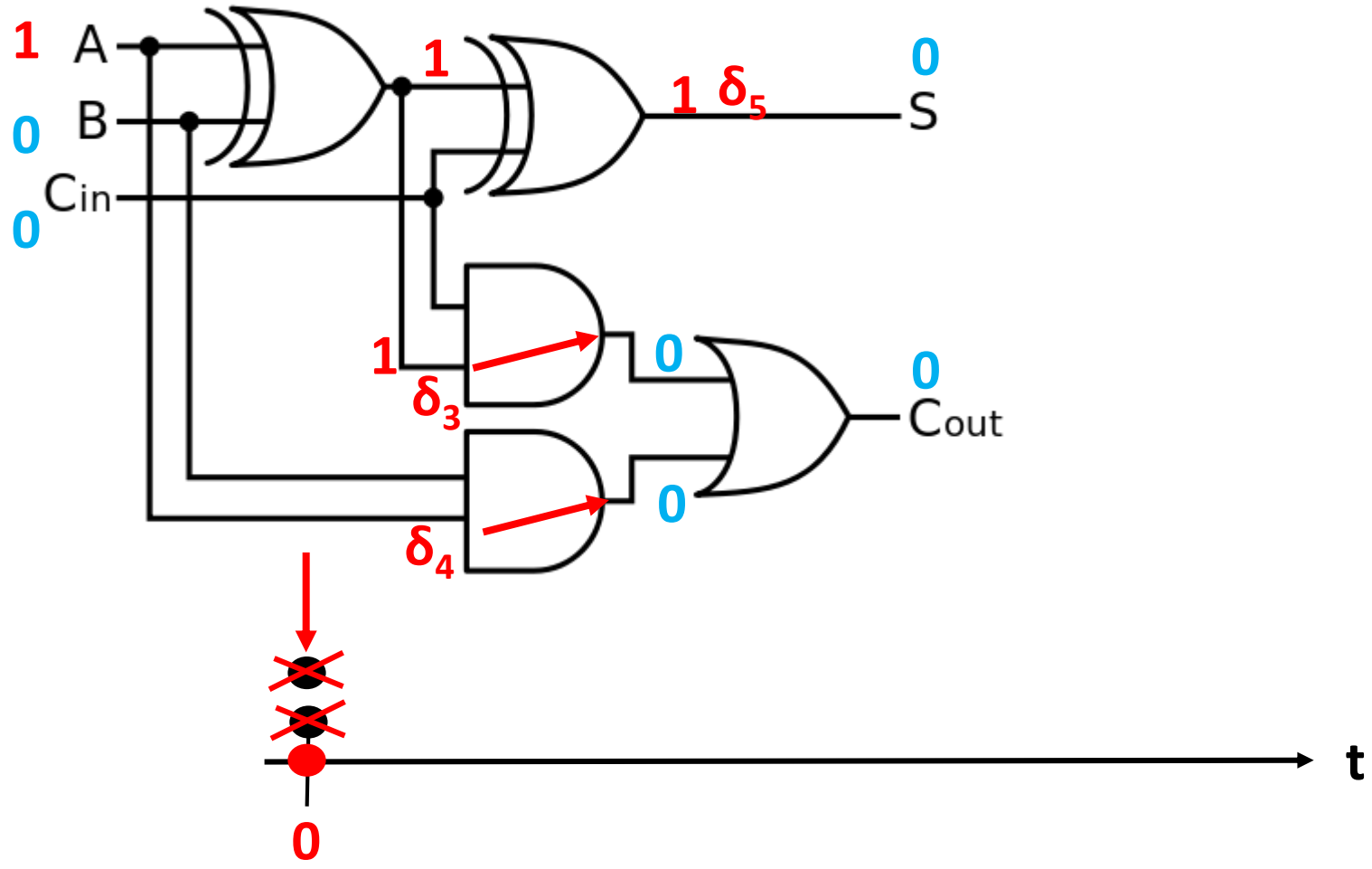
Event	Time
δ_2	0
δ_3	0
δ_4	0

Processing δ2: propagation



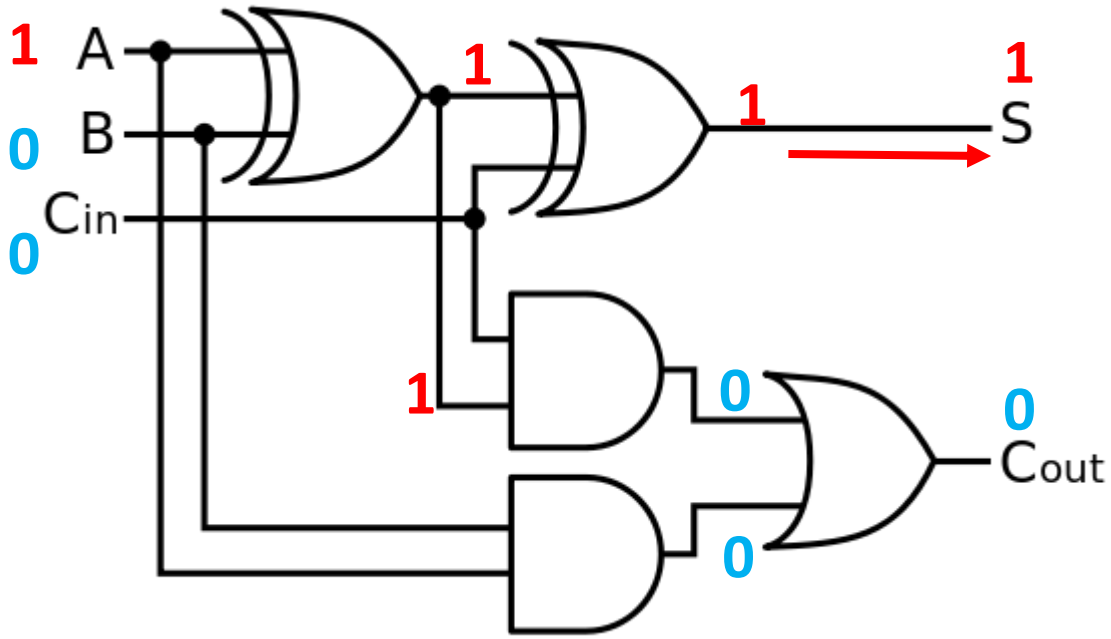
Event	Time
δ_3	0
δ_4	0
δ_5	0

Processing δ3: absorption

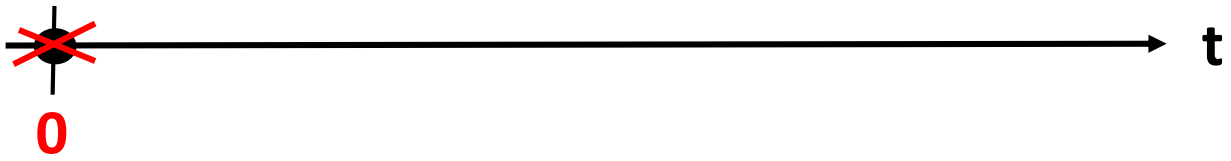


Event	Time
δ_5	0

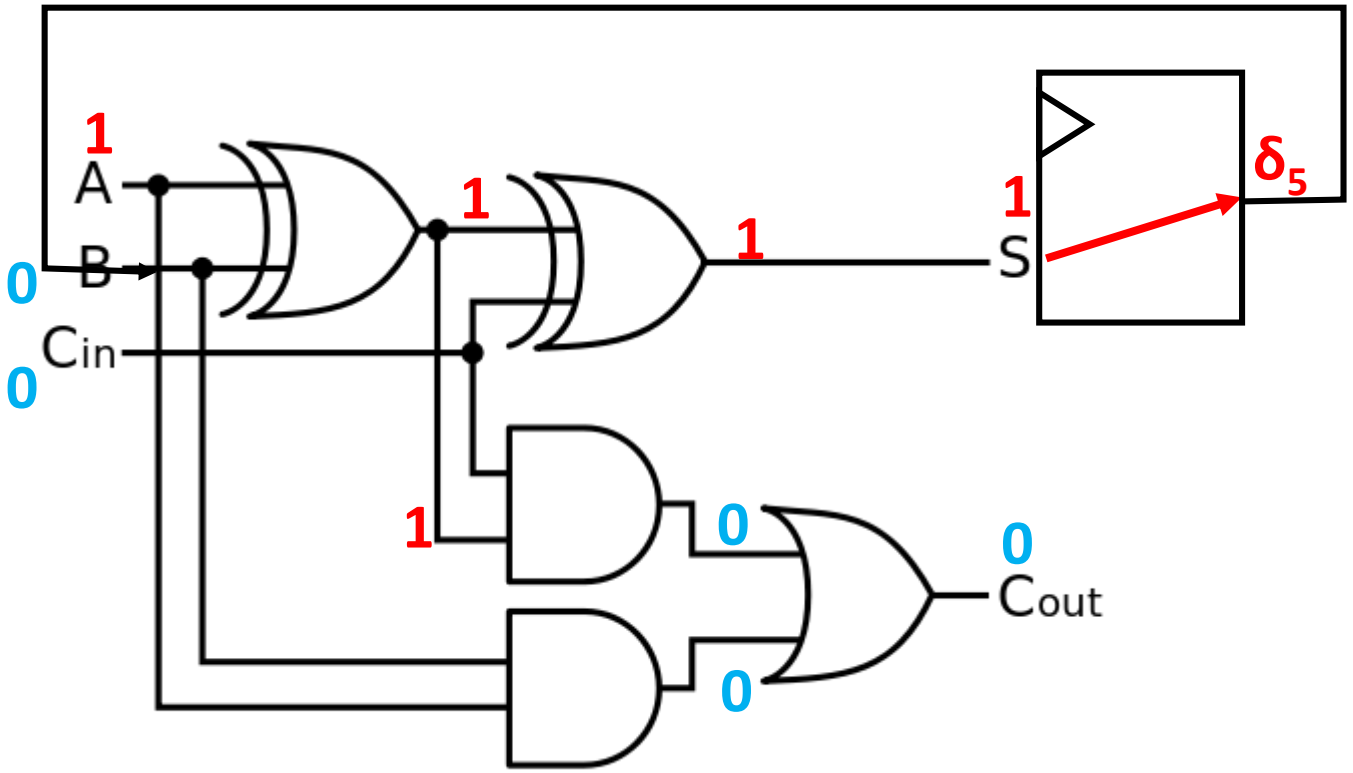
Processing δ4: end of simulation



Event	Time

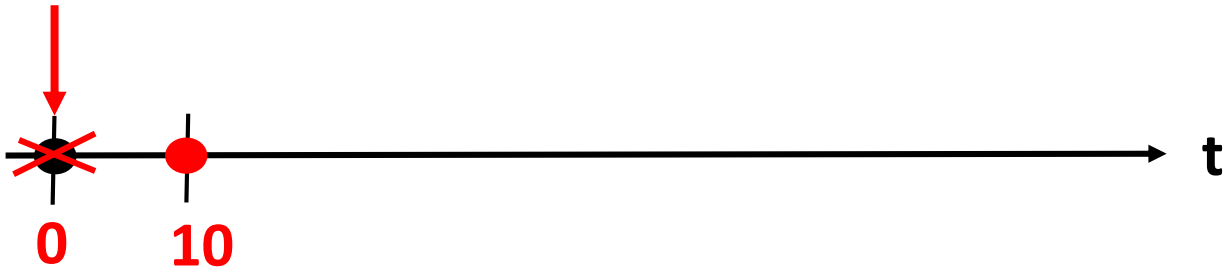


Flip-Flop: propagation in time

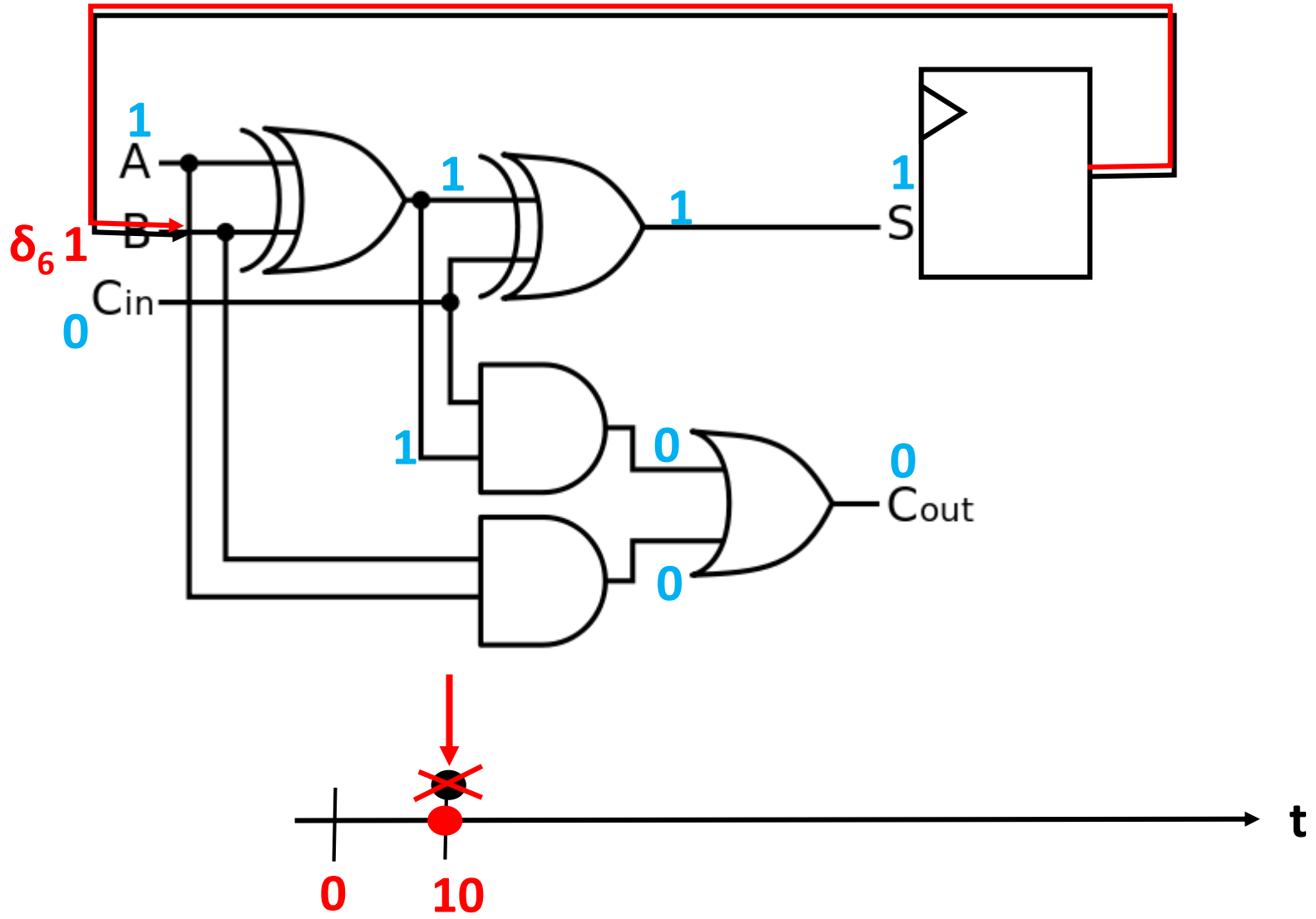


Event	Time
δ_5	10ns

Clk period

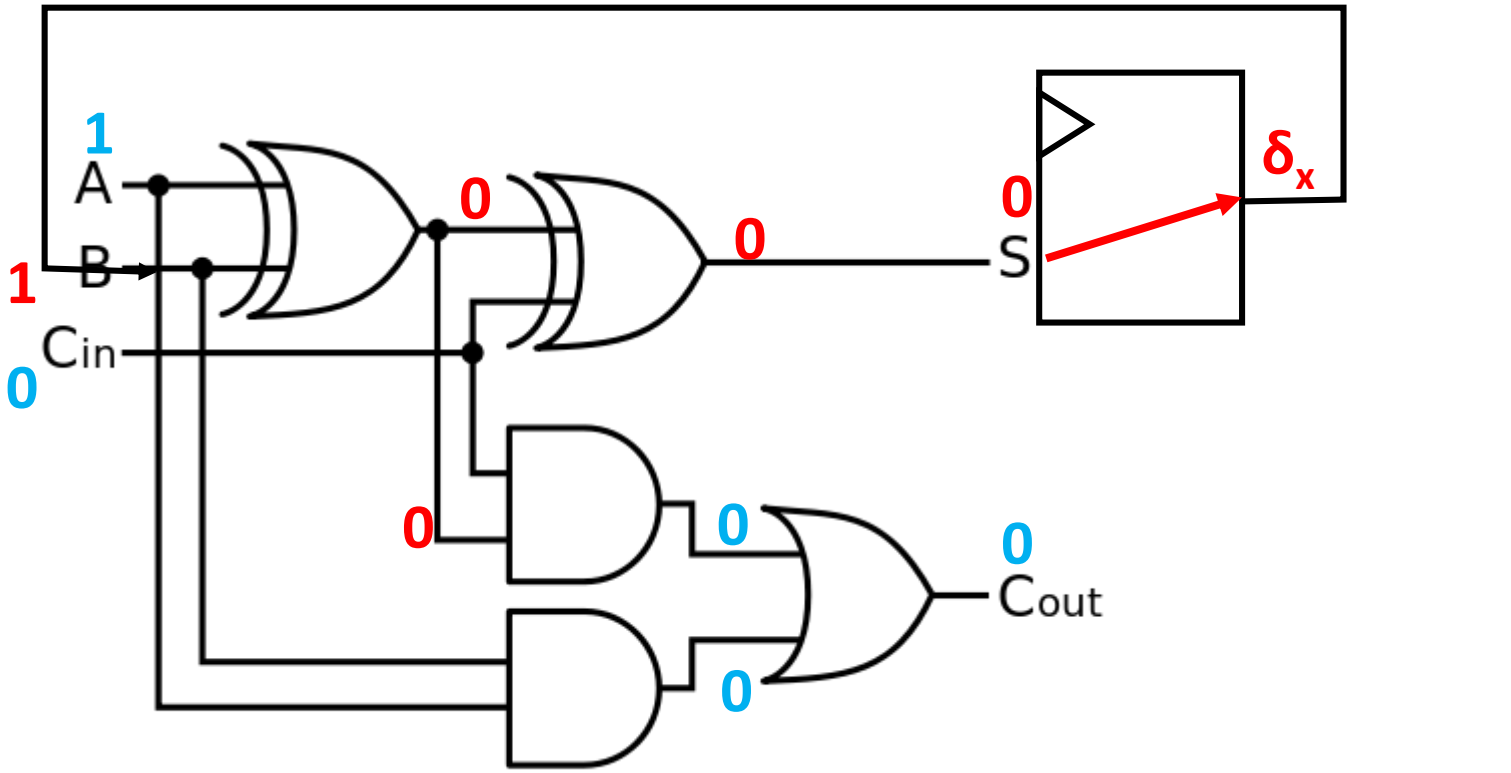


Flip-Flop: propagation in time



Event	Time
δ6	10ns

…after δ propagation at time 10…



Event	Time
δx	20ns

VHDL Delta Cycle

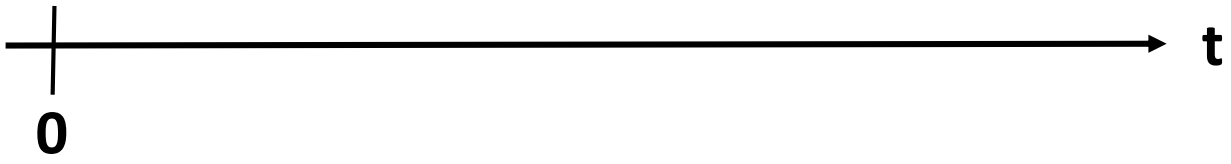
0 A·
0 B·
0 Cin·

```
Signal A_int, B_int, C_int,
result :
  std_logic_vector(1 downto 0);
Begin;
A_int <= '0'&A;
B_int <= '0'&A;
C_int <= '0'&A;

result <= A_int+ B_int+ C_int;
S <= result(0);
Cout<= result(1);
end ;
```

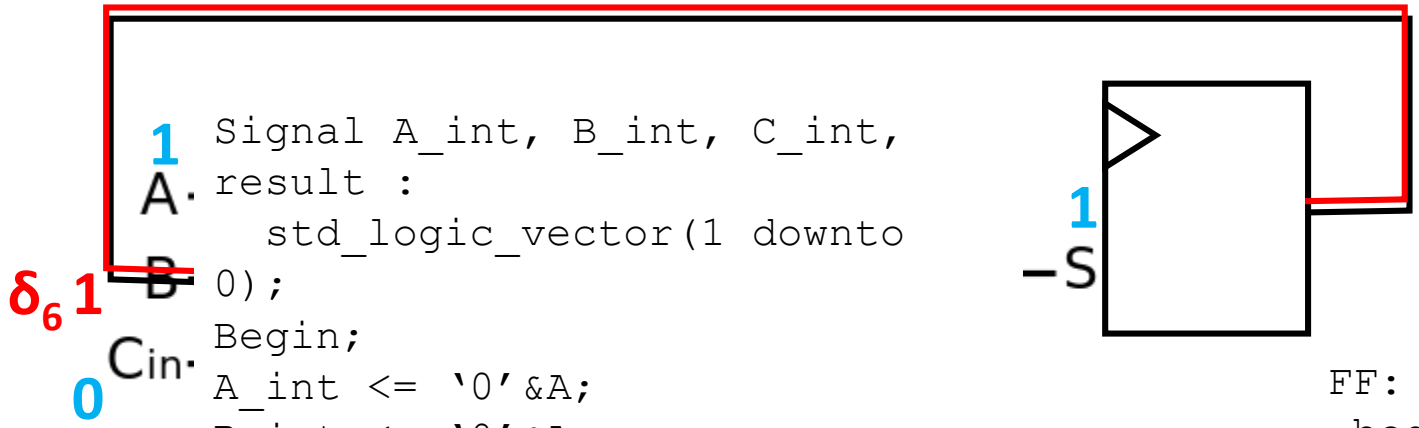
0 -S

0 -Cout

Event
None



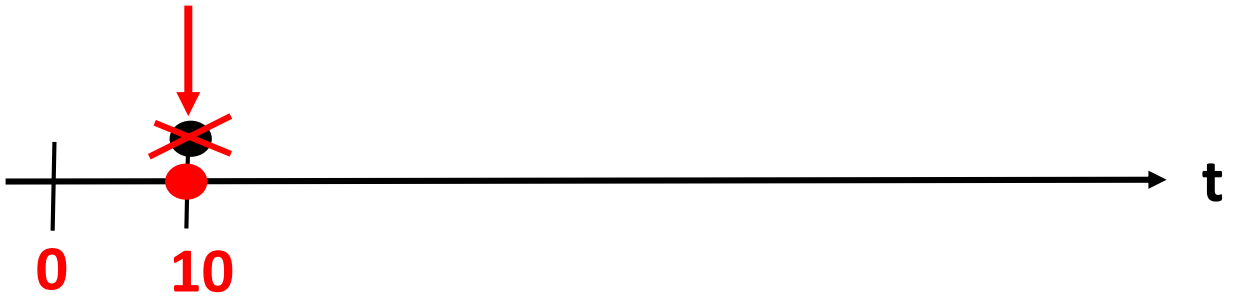
VHDL FF: propagation in time



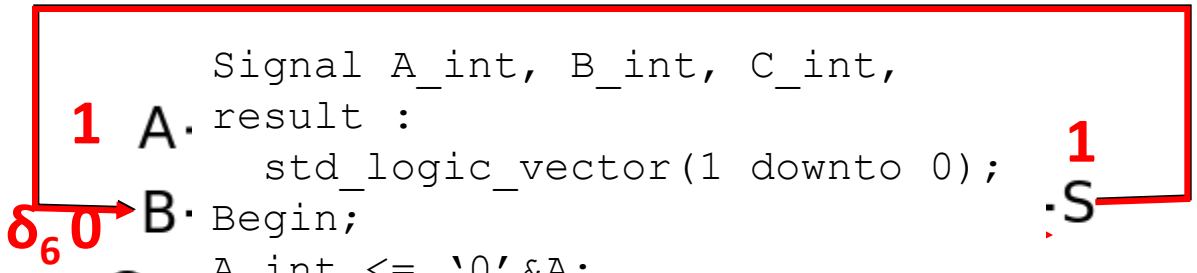

```
Signal A_int, B_int, C_int,
result :
  std_logic_vector(1 downto
0);
Begin;
A_int <= '0'&A;
B_int <= '0'&A;
C_int <= '0'&A;

result <= A_int+ B_int+ C_int;
S <= result(0);
Cout<= result(1);
end ;
```

Event	Time
δ6	10ns

```
FF: process (clk)
 begin
  if (clk'event) and clk=1
 then
  B <= S
 end if;
 End;
```



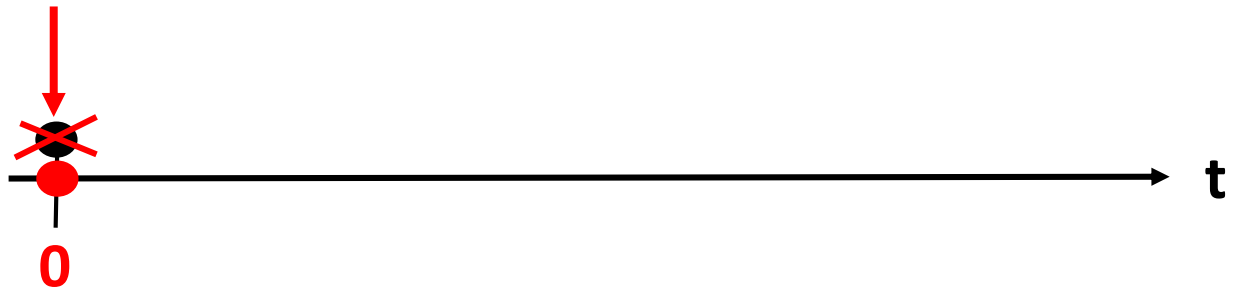
Watch out for combinatorial loops!




```
Signal A_int, B_int, C_int,
result :
  std_logic_vector(1 downto 0);
Begin;
A_int <= '0'&A;
B_int <= '0'&A;
C_int <= '0'&A;

result <= A_int+ B_int+ C_int;
S <= result(0);
Cout<= result(1);
B_int <= result(0);
end ;
```

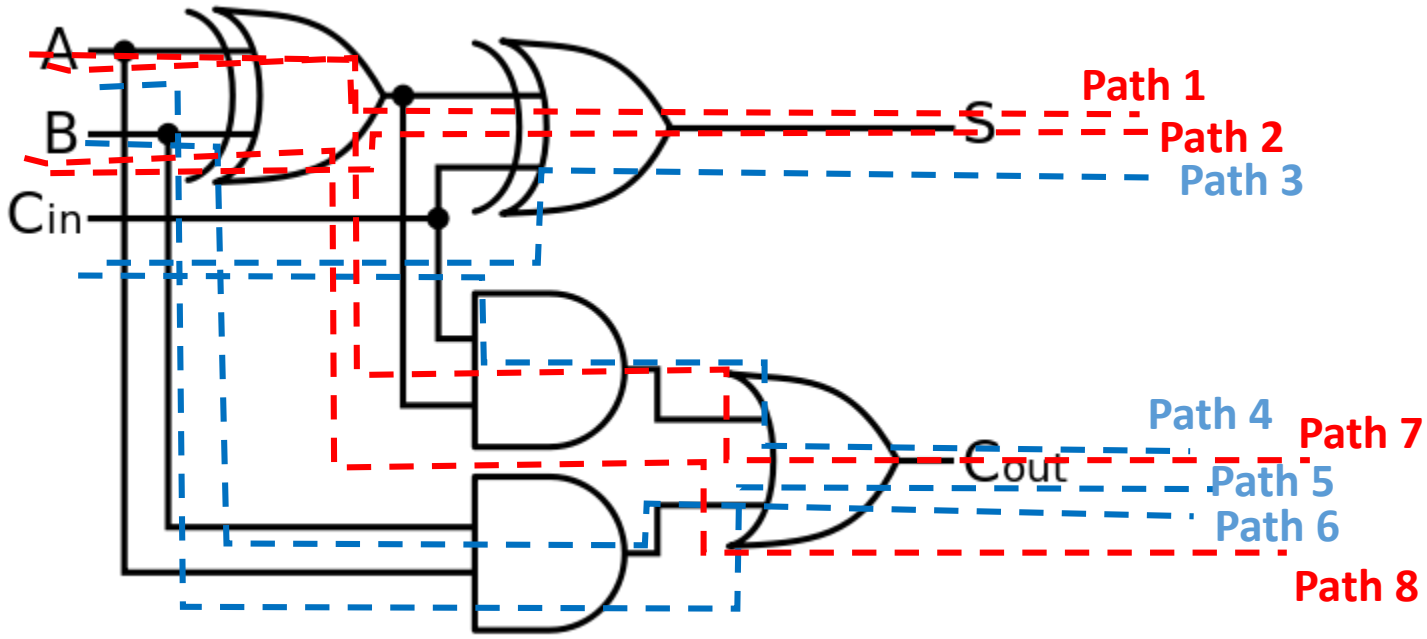

Event	Time
δ_6	0ns

Time did not change: infinite loop!



Static Timing Analysys: gate transversal

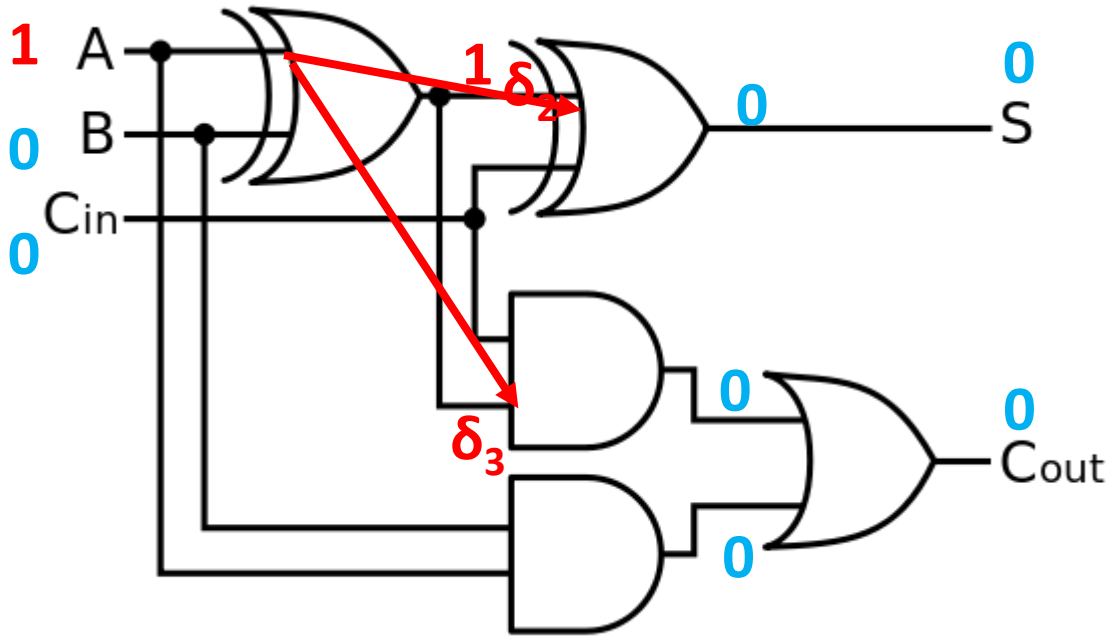
Base cells: Xor: 4ns, AND: 2ns, OR: 2 ns;



Path #	Delay
1	8ns
2	8ns
3	4ns
4	4ns
5	4ns
6	4ns
7	8ns
8	8ns

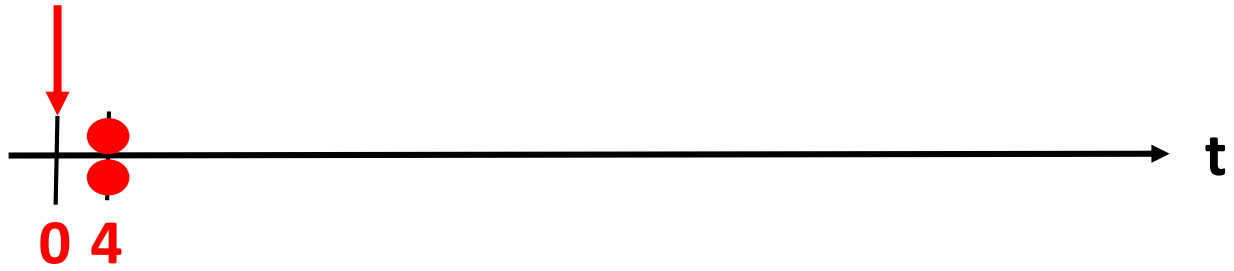
Critical Path 8ns => F_{MAX}=125 Mhz

Post synthesis: gate delay

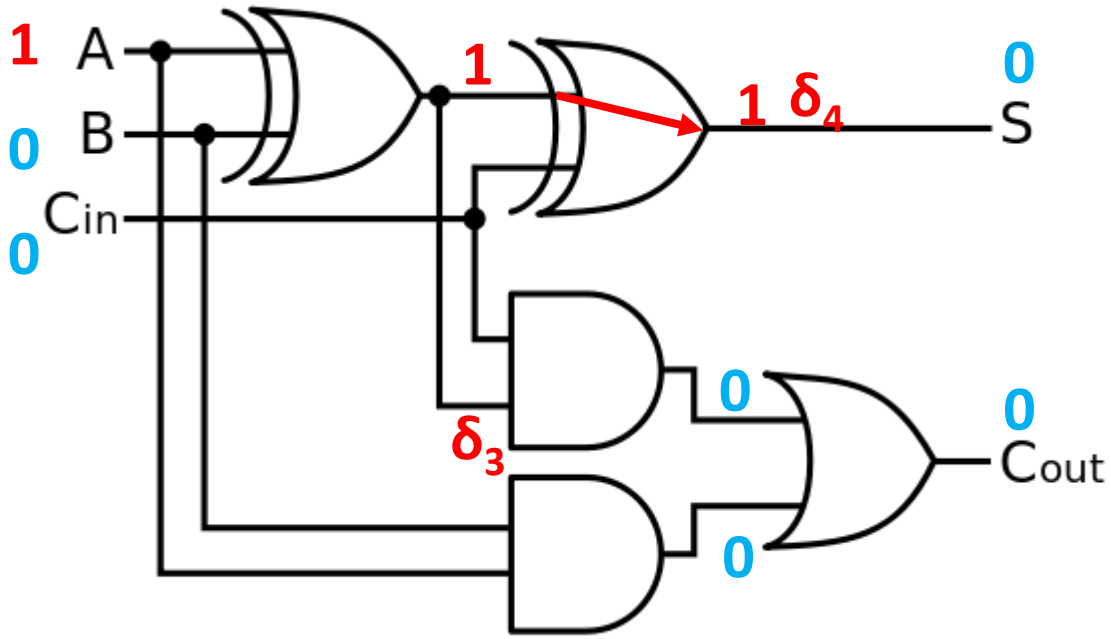


Event	Time
δ_2	4
δ_3	4

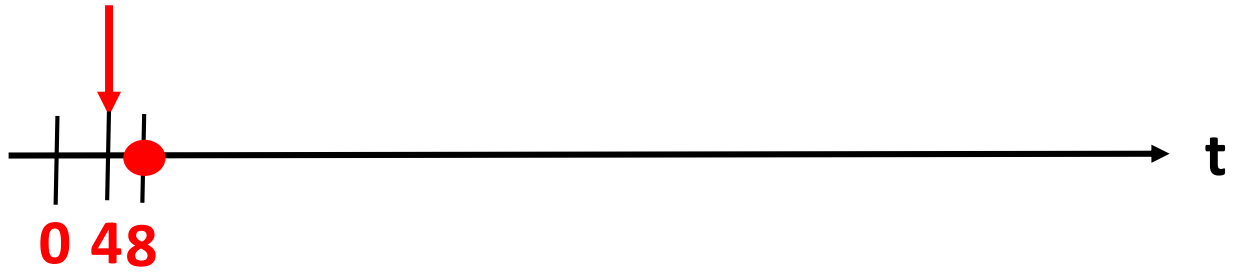
Gate delays from synthesis : Standard Delay Format (SDF) file



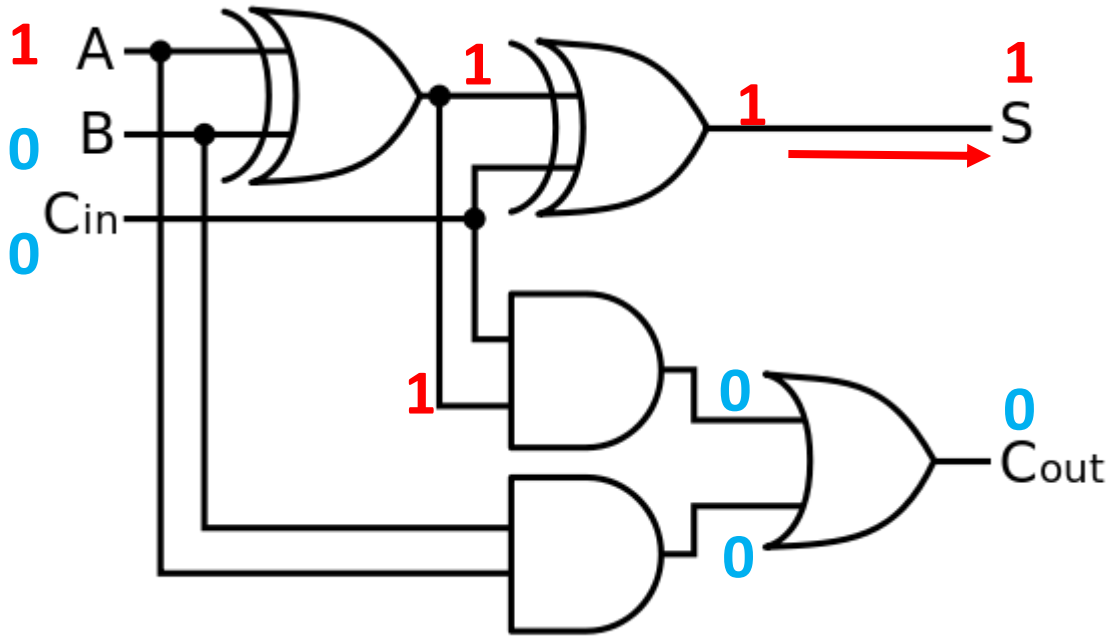
Processing δ2: propagation



Event	Time
δ_3	4
δ_4	8



End of timed simulation



Event	Time

Three times steps instead of one!