CSCI 540 Homework 3
Due by: 11:59PM on May 1st. 2024 (Wednesday)

Instruction:

- Provide your name and CWID on top in the first page of your submission
- Show your work (at least 50% penalty otherwise)
- Submit a single PDF document containing all your answers to the associated folder under Assignments (at least 50% penalty otherwise)
- Make sure that you submitted the intended one. It is recommended that you download what has been uploaded and double-check if the correct document has been submitted.
- You can submit as many times as you want, but the last submission will only be graded. If the last submission is made after the deadline, there should be a late submission penalty.
- Plagiarism: Any violation causes a zero score for the assignment and may result in a failing grade (Do not copy and paste anything from this document to your document submitted)
- Hand-written answers (including showing work) will not be accepted and graded.
- No extension/resubmission request will be accepted.

Problem 1. Packed Decimal (25 pt., 5 pt. each)

Show the decimal values for each of the packed decimal numbers (a-c) and the packed decimal format in binary for decimal numbers (d-e).

a. 0000 0111 0011 0110

b. 0101 0110 0000 0011

c. 1101 0100 0010 0010

d. 354

e. -820

Problem 2. Addressing Modes (25 pt., 5 pt. each)

Given the following memory values and a one-address machine with an accumulator, what values do the following instructions load into the accumulator?

- Word 20 contains 40
- Word 30 contains 50
- Word 40 contains 30
- Word 50 contains 60

a. LOAD IMMEDIATE 20

b. LOAD DIRECT 20

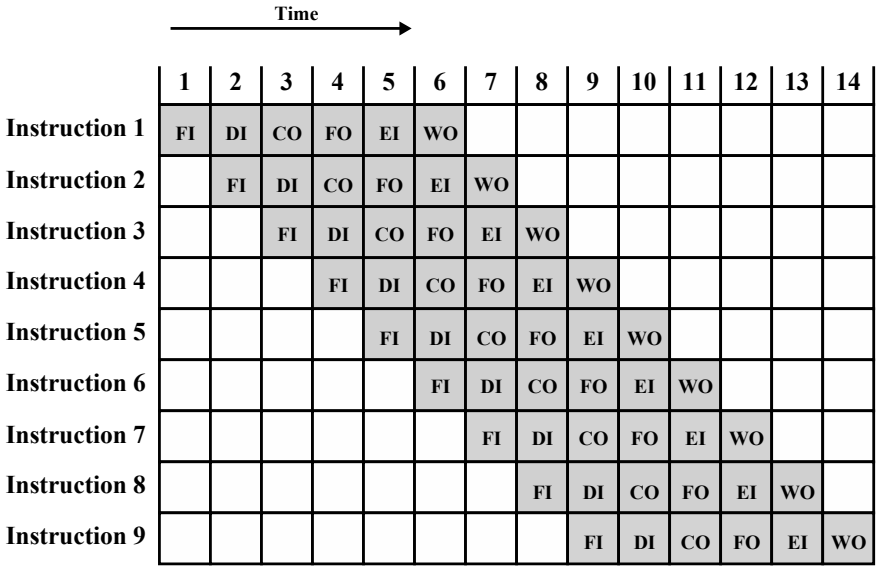
c. LOAD INDIRECT 20

d. LOAD DIRECT 30

e. LOAD INDIRECT 30

Problem 3. Pipelining (20 pt.)

Refer to the following timing diagram in Fig. 16.10 in the textbook, showing instruction pipeline operation for 9 instructions under the assumption of six stages.



Assume a pipeline with four stages: fetch instruction (FI), decode instruction and calculate addresses (DA), fetch operand (FO), and execute (EX). Complete the following timing diagram (similar to the diagram above) for a sequence of 7 instructions, in which the third instruction is a branch to instruction 15 that is taken and in which there are no data dependencies.

	1	2	3	4	5	6	7	8	9	10
I1										
I2										
I3										
I4										
I5										
I6										
I15										