

VIETNAM NATIONAL UNIVERSITY HO CHI MINH CITY  
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY  
FACULTY OF COMPUTER SCIENCE AND ENGINEERING



Course name h

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Report type h

Report title h

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HO CHI MINH CITY, NOVEMBER 2025





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# 1 Report of lab 1

In lab 1, there are 10 problems to be solved. In each problem, we need to solve it first by hand and then verify the result by using simulation tools. In this report, we will use PSpice for TI to verify our results.

## 1.1 Exercise 1

Given the following circuit. Calculate the value of the voltage  $v_o$  and the current  $i$ . Then, simulate the circuit to check it out.

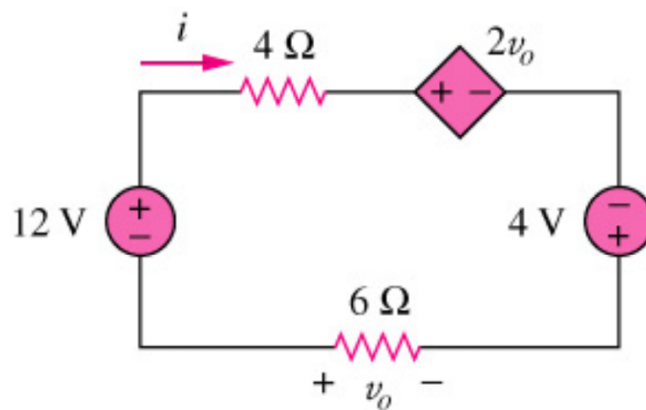


Figure 1.1: Find the voltage and the current in the given circuit using KVL

### 1.1.1 Calculation

**Notes:** Explanations, formulas, and equations are expected rather than only results.

According to the KVL (Kirchhoff's Voltage Law), we have the equations of the loops as follows:

$$12 - 0 = 4i + 2v_o - 4 + 6i \quad (1.1)$$

According to the Ohm's Law, we have:

$$i = \frac{-v_o}{6} \quad (1.2)$$

From (1) and (2), we have:

$$12 = 4 \left( \frac{-v_o}{6} \right) + 2v_o - 4 + 6 \left( \frac{-v_o}{6} \right) \Rightarrow v_o = 48(V)$$

By substituting  $v_o = 48$  into (2), we have:  $i = \frac{-48}{6} = -8(A)$

### 1.1.2 simulation

After redrawing the circuit in PSpice for TI, and run then simulation, we have the results as follows:

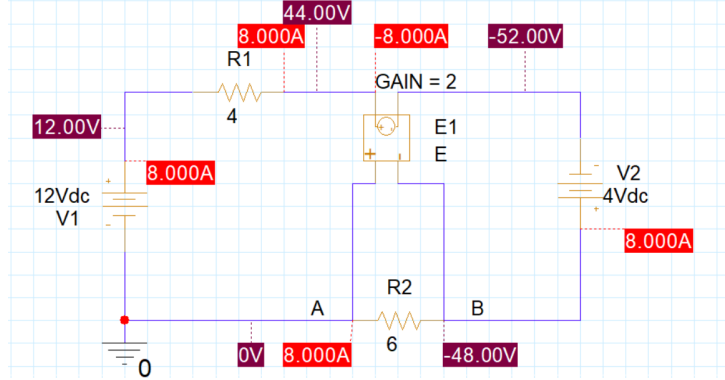


Figure 1.2: Simulation result of the circuit in Figure 1.1

Let  $A$  and  $B$  be the nodes across the voltage source  $v_0$ . From the simulation result in Figure 1.2, we have:

$$\begin{cases} v_0 = V_A - V_B = 48(V) \\ i = I = -8(A) \end{cases}$$

Even though the current  $i$  has a negative value, it is still correct because the direction of the current in the simulation is opposite to the assumed direction in the calculation.

**Conclusion:** The result of PSpice simulation matches the result of the calculation. Therefore, the calculation is correct.

## 1.2 Exercise 2

Given the following circuit, students rearrange the circuit to clarify its serial and/or parallel topology. Then, apply the knowledge you've learned to find the equivalent resistance value between two circuit terminals A and F. Finally, perform the simulation to check if the current through the whole circuit is correctly calculated.

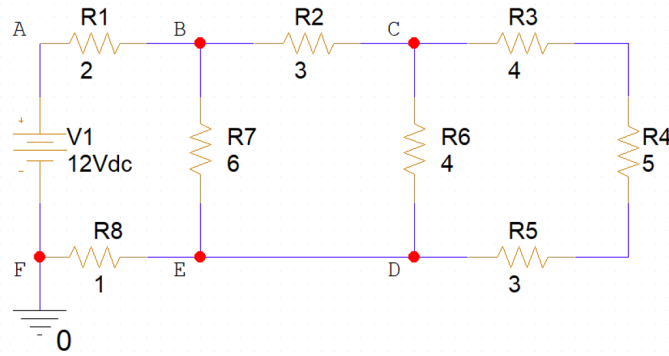


Figure 1.3: Find the equivalent resistance between terminals A and F

### 1.2.1 Rearrange the circuit

By extending wire between nodes B and E, we have the following rearranged circuit:

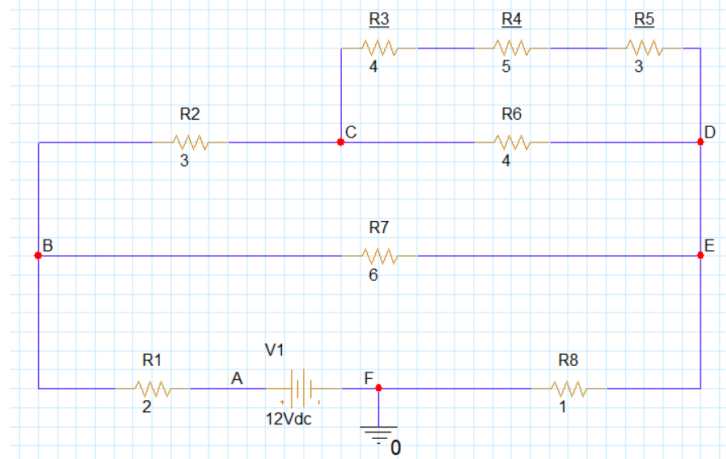


Figure 1.4: Rearranged circuit

### 1.2.2 Calculation

**Convention:** The equivalent resistance between the two terminals A and B of a circuit segment containing only R1, R2, R3, and R4 may be named  $R_{AB\_1234}$ .

Belong to the rearranged circuit, we have:  $R_6 \parallel (R_3 + R_4 + R_5)$ . Thus, we calculate the equivalent resistance  $R_{CD\_3456}$  as follows:

$$R_{CD\_3456} = \frac{1}{\frac{1}{R_6} + \frac{1}{R_3 + R_4 + R_5}} = \frac{1}{\frac{1}{4} + \frac{1}{4 + 5 + 3}} = 3(\Omega)$$

Next, looking at the circuit between  $B$  and  $E$ , we have:  $R7 \parallel (R2 + R_{CD\_3456})$ . Thus, we calculate the equivalent resistance  $R_{BE}$  as follows:

$$R_{BE} = \frac{1}{\frac{1}{R_7} + \frac{1}{R_2 + R_{CD\_3456}}} = \frac{1}{\frac{1}{6} + \frac{1}{3+3}} = \frac{1}{\frac{1}{2} + \frac{1}{6}} = 3(\Omega)$$

Now move to  $A$  and  $F$ , we have:  $R1 + R_{BE} + R8$ . Thus, we calculate the equivalent resistance  $R_{AF}$  as follows:

$$R_{AF} = R_1 + R_{BE} + R_8 = 1 + 3 + 2 = 6(\Omega)$$

By applying Ohm's law, we can find the current  $I_{AB}$  through the whole circuit:

$$I_{AB} = I = \frac{U}{R_{AF}} = \frac{12}{6} = 2(A)$$

### 1.2.3 Simulation

To verify the calculation above, we did perform the simulation twice: first, for original circuit; second, for rearranged circuit. The results are as follows:

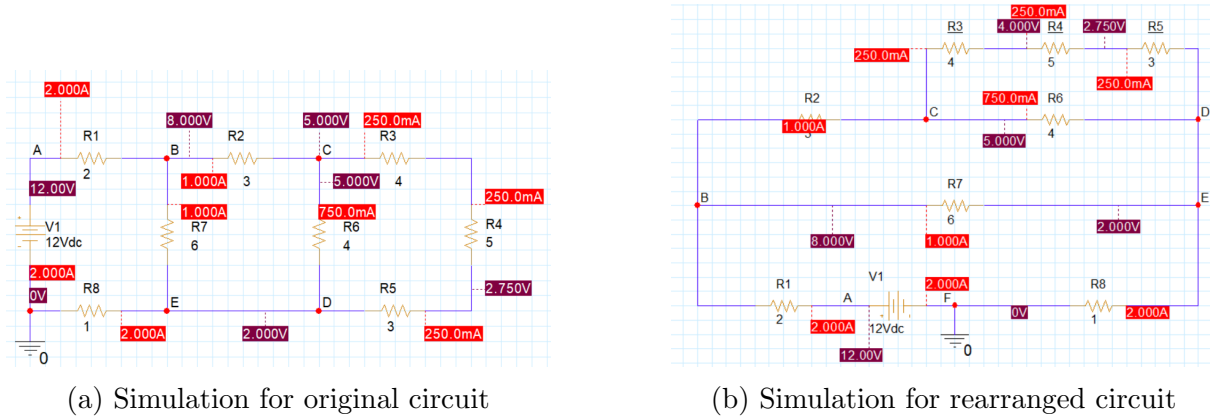


Figure 1.5: Simulation results

As shown, the value of current  $I$  and voltage  $V$  between corresponding terminals in both simulations are the same. Thus, our calculation and rearrangement are correct.



### 1.3 Exercise 3

Given the following circuit, students rearrange the circuit to clarify its serial and/or parallel topology. Next, apply the knowledge you've learned to find the equivalent resistance value between two circuit terminals A and F, the voltage values at A, B, C, D, and E. Finally, perform the simulation to check your calculation.

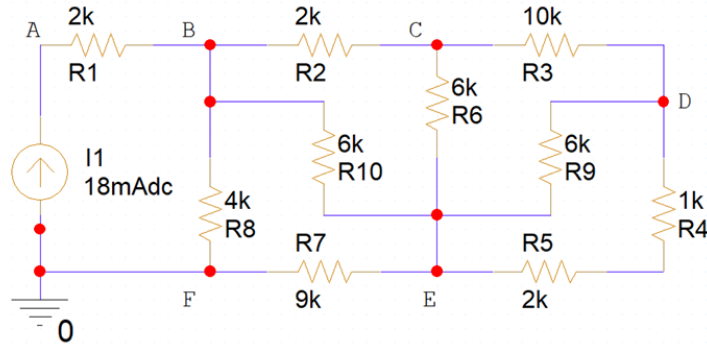


Figure 1.6: Find the whole-circuit equivalent resistance and the voltages at A, B, C, D, and E

#### 1.3.1 Rearrange the circuit

By drawing a wire with current source I1, A, B, C, D, and E, we can clarify the circuit topology. As follows:

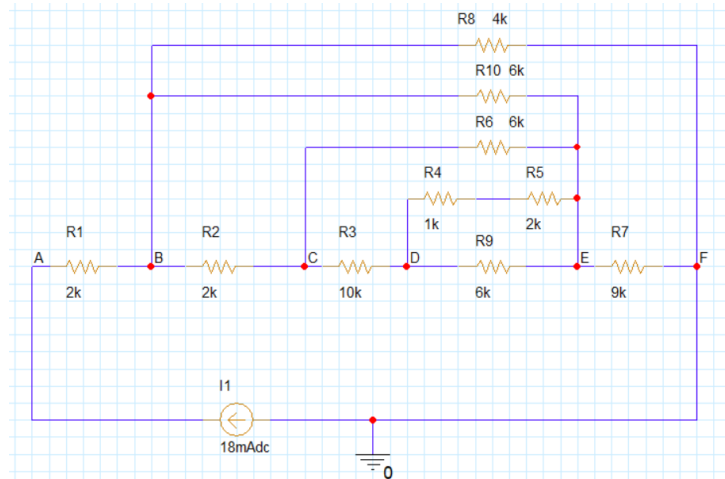


Figure 1.7: Rearranged circuit

#### 1.3.2 Calculation

As the rearranged circuit showed in Figure 1.7, we can calculate the equivalent resistance  $R_{AF}$  by the following steps: First, we calculate  $R_{DE}$ . Because  $R9 \parallel (R4 + R5)$ , we have:

$$R_{DE} = \frac{1}{\frac{1}{R_9} + \frac{1}{R_4 + R_5}} = \frac{1}{\frac{1}{6} + \frac{1}{1+2}} = 2(k\Omega)$$

Next, we calculate  $R_{CE}$ . Because  $R_6 \parallel (R_3 + R_{DE})$ , we have:

$$R_{CE} = \frac{1}{\frac{1}{R_6} + \frac{1}{R_3 + R_{DE}}} = \frac{1}{\frac{1}{6} + \frac{1}{10+2}} = 4(k\Omega)$$

Now, we calculate  $R_{BE}$ . Because  $R_{10} \parallel (R_2 + R_{CE})$ , we have:

$$R_{BE} = \frac{1}{\frac{1}{R_{10}} + \frac{1}{R_2 + R_{CE}}} = \frac{1}{\frac{1}{6} + \frac{1}{2+4}} = 3(k\Omega)$$

We then calculate  $R_{BF}$ . Because  $R_8 \parallel (R_7 + R_{BE})$ , we have:

$$R_{BF} = \frac{1}{\frac{1}{R_8} + \frac{1}{R_7 + R_{BE}}} = \frac{1}{\frac{1}{4} + \frac{1}{3+9}} = 3(k\Omega)$$

Finally, we calculate  $R_{AF}$ . Because  $R_1 + R_{BF}$ , we have:

$$R_{AF} = R_1 + R_{BF} = 2 + 3 = 5(k\Omega)$$

By applying Ohm's law, we can find the voltage value between terminals A and F:

$$V_{AF} = V = I \times R_{AF} = 18 \times 5 = 90(V)$$

We have voltages at nodes A, B, C, D, and E as follows:

$$\begin{cases} V_A - V_F = V_{AF} = 90 \Rightarrow V_A = 90 + V_F = 90 + 0 = 90(V) \\ V_{BF} = I \times R_{BF} = 18 \times 3 = 54(V) \Rightarrow V_B = V_F + V_{BF} = 0 + 54 = 54(V) \end{cases}$$

By applying the voltage divider rule, we have:

$$V_{EF} = V_{BF} \times \frac{R_7}{R_{BE} + R_7} = 54 \times \frac{9}{3+9} = 40.5(V) \Rightarrow V_E = V_F + V_{EF} = 0 + 40.5 = 40.5(V)$$

$$\begin{aligned} V_{CE} &= V_{BE} \times \frac{R_{CE}}{R_{CE} + R_{DE}} = (V_B - V_E) \times \frac{R_{CE}}{R_{CE} + R_{DE}} = (54 - 40.5) \times \frac{4}{4+2} = 9(V) \\ \Rightarrow V_C &= V_E + V_{CE} = 40.5 + 9 = 49.5(V) \end{aligned}$$

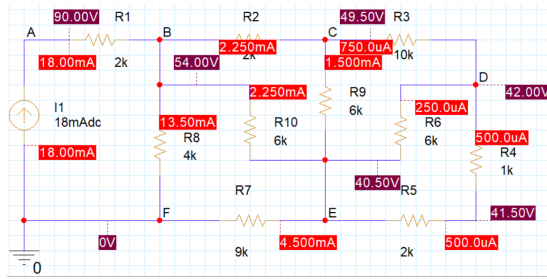
$$\begin{aligned} V_{DE} &= V_{CE} \times \frac{R_{DE}}{R_{DE} + R_3} = (V_C - V_E) \times \frac{R_{DE}}{R_{DE} + R_3} = (49.5 - 40.5) \times \frac{2}{2+10} = 1.5(V) \\ \Rightarrow V_D &= V_E + V_{DE} = 40.5 + 1.5 = 42(V) \end{aligned}$$

**Conclusion:** After rearranging the circuit and calculating step-by-step, we have:

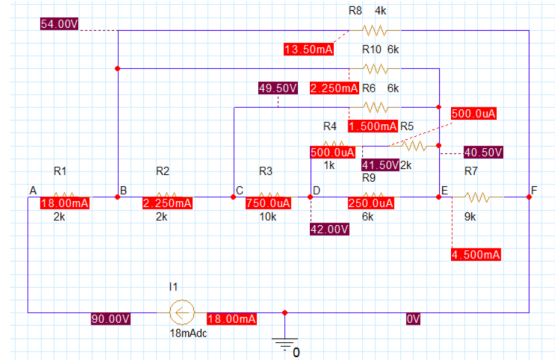
$$\begin{cases} R_{AF} = 5(k\Omega) \\ V_A = 90(V), V_B = 54(V), V_C = 49.5(V), V_D = 42(V), V_E = 40.5(V) \end{cases}$$

### 1.3.3 Simulation

To verify the calculation above, we did perform the simulation twice: first, for original circuit; second, for rearranged circuit. The results are as follows:



(a) Simulation for original circuit



(b) Simulation for rearranged circuit

Figure 1.8: Simulation results

From the simulation results in Figure 1.8, we can see that the equivalent resistance  $R_{AF}$  and voltages at nodes A, B, C, D, and E are the same for both original and rearranged circuits. The simulation results confirm our calculations are correct.

## 1.4 Exercise 4

Given the following circuit, find  $I_1$ ,  $I_2$ ,  $I_3$ ,  $V_a$ , and  $V_b$ . Present your calculation steps and check them out by performing the simulation.

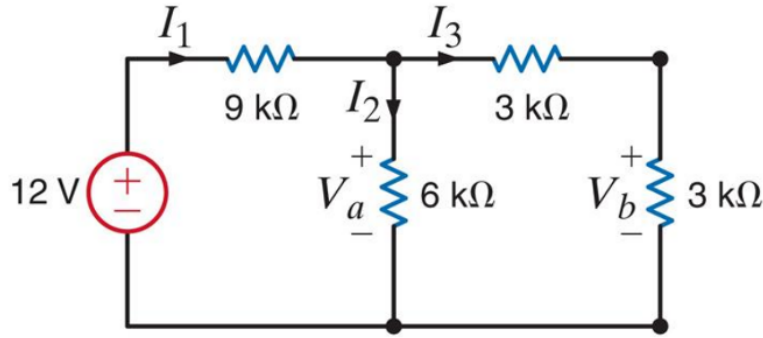


Figure 1.9: Find  $I_1$ ,  $I_2$ ,  $I_3$ ,  $V_a$ , and  $V_b$

### 1.4.1 Calculation

The whole circuit equivalent resistance:

$$R_{eq} = 9 + \frac{1}{\frac{1}{6} + \frac{1}{3+3}} = 9 + \frac{1}{\frac{1}{6} + \frac{1}{6}} = 12(\Omega)$$

By applying Ohm's law, we can find the total current  $I_1$ :

$$I_1 = \frac{V}{R_{eq}} = \frac{12}{12} = 1(mA)$$

By the current division rule, we can find  $I_2$  and  $I_3$ :

$$I_2 = I_1 \times \frac{6}{6 + 3 + 3} = 1 \times \frac{6}{12} = 0.5(mA)$$

$$I_3 = I_1 \times \frac{3 + 3}{6 + 3 + 3} = 1 \times \frac{6}{12} = 0.5(mA)$$

By applying Ohm's law, we can find  $V_a$  and  $V_b$ :

$$V_a = I_2 \times 6 = 0.5 \times 6 = 3(V)$$

$$V_b = I_3 \times 3 = 0.5 \times 3 = 1.5(V)$$

### 1.4.2 Simulation

By performing the simulation in PSpice for TI, we have the following results:

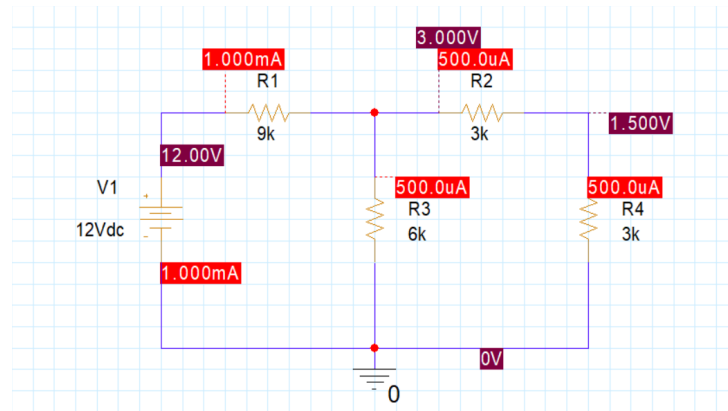


Figure 1.10: Simulation results of Exercise 4

As shown in Figure 1.10, the simulation results match our calculation.

## 1.5 Exercise 5

Given the network as shown below

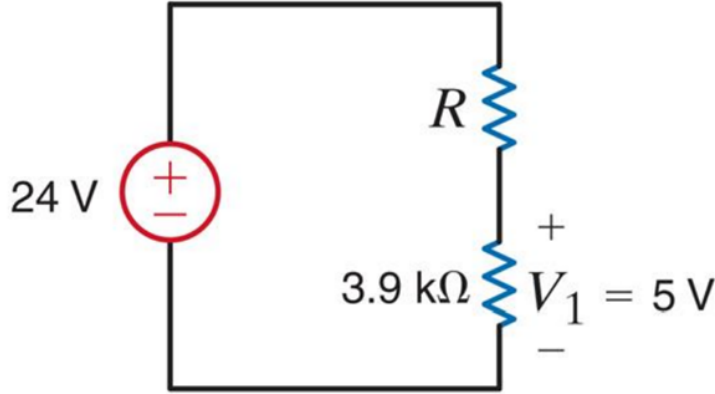


Figure 1.11: Select resistor  $R$  from the standard resistors list and do the following requirements

- a. Find the required value for the resistor. By applying Ohm's law for  $3.9k\Omega$  resistor, we have:

$$I = I_1 = \frac{5}{3.9} = 1.282(mA)$$

Then by applying Ohm's law for resistor  $R$ , we have:

$$R = \frac{V}{I} = \frac{24 - 5}{1.282} = 14.821(k\Omega)$$

- b. Use Table 2.1 in the lecture slide to select a standard 10% tolerance resistor for  $R$ .  $R$  in the circuit may be a single resistor or a combination of resistors as long as these resistors meet the standard values and are available in the market. From the standard resistor list with 10% tolerance, we can select  $15k\Omega$  resistor for  $R$ .
- c. Using the resistor selected in (b), determine the voltage across the  $3.9 k\Omega$  resistor. By applying Ohm's law for resistor the whole circuit, we have:

$$I = \frac{V}{R_{eq}} = \frac{24}{3.9 + 15} = 1.270(mA)$$

Then by applying Ohm's law for  $3.9k\Omega$  resistor, we have:

$$V_1 = I \times 3.9 = 1.270 \times 3.9 = 4.95(V)$$

- d. Calculate the percent error in the voltage  $V_1$  if the standard resistor selected in (b) is used. The percent error in the voltage  $V_1$  is calculated as follows:

$$\text{Percent error} = \left| \frac{V_{1,calculated} - V_{1,selected}}{V_{1,calculated}} \right| \times 100\% = \left| \frac{5 - 4.95}{5} \right| \times 100\% = 1\%$$



- e. Determine the power rating for this standard component. The power rating for the  $15k\Omega$  resistor is calculated as follows:

$$P = I^2 \times R = (1.270 \times 10^{-3})^2 \times 15 \times 10^3 = 0.024(W)$$

Therefore, a standard resistor with a power rating of at least  $0.025W$  should be selected.

## 2 Report of lab 2

### 2.1 Half-wave Rectifier

In this exercise, an alternating source is used to generate a half-wave rectifier output using a diode. The schematic of the simulation is given below.

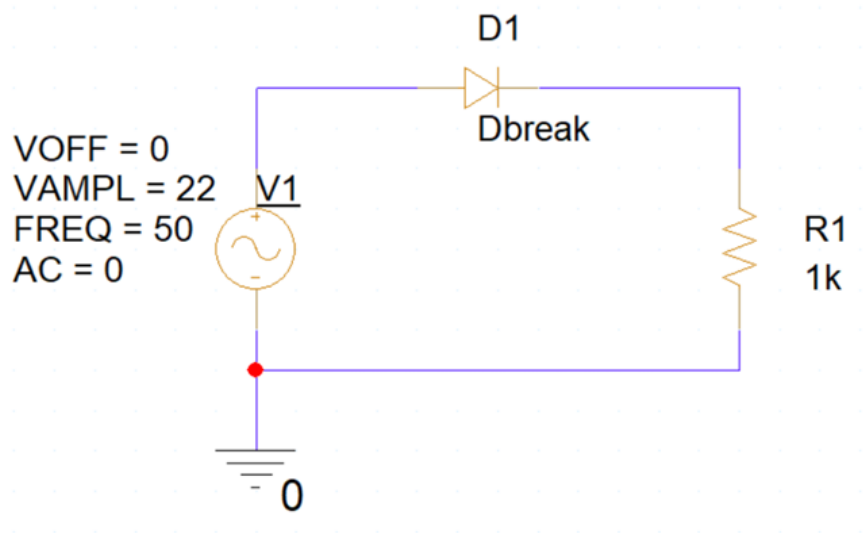


Figure 2.1: Half-wave Rectifier with Voltage Sin Source

#### 2.1.1 Theory calculations

**Approximation:** Diodes have  $V_f = 0.78V$

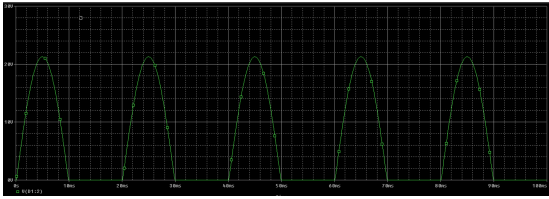
- Minimum Value of  $V_{R1} = 0$  (Because during negative half cycle, diode is off).
- Maximum Value of  $V_{R1} = V_{\sin Max} - V_f = 22 - 0.78 = 21.22V$
- Duration (millisecond) for a cycle of  $V_{R1} = T_{cycle} = \frac{1}{FREQ} = \frac{1}{50} = 0.02s = 20ms$

#### 2.1.2 PSpice simulation

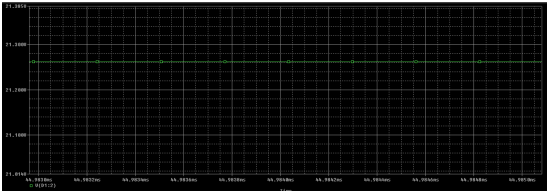
- Minimum Value of  $V_{R1} \approx -6.399018344997e - 28V \approx 0V$ .
- Maximum Value of  $V_{R1} \approx 2.125892105879e + 01V \approx 21.26V$ .
- Duration (millisecond) for a cycle of  $V_{R1} = 20ms$ .

The following images show the simulation results for the half-wave rectifier circuit and highest Voltage value.





(a) Half-wave Rectifier Output Voltage



(b) Maximum Voltage Measurement

Figure 2.2: Half-wave Rectifier Simulation Results

Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	431.232u		
	X Values	44.966m	44.979m	-12.095u	Y1 - Y1(Cursor1) Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(D1:2)	21.263	21.262	431.232u	0.000	0.000	21.263	21.262

Figure 2.3: Min and max values tracking on the wave-form

## 2.2 Full-wave Rectifier

The following circuit is known as a full-wave bridge diode rectifier. Given that the transformer has the ratio  $N1/N2 = 10$ . Write the voltage difference equation  $V_{AB}$  and  $V_{CD}$ . After that, perform a time-domain (transient) analysis to check the equation you've written.

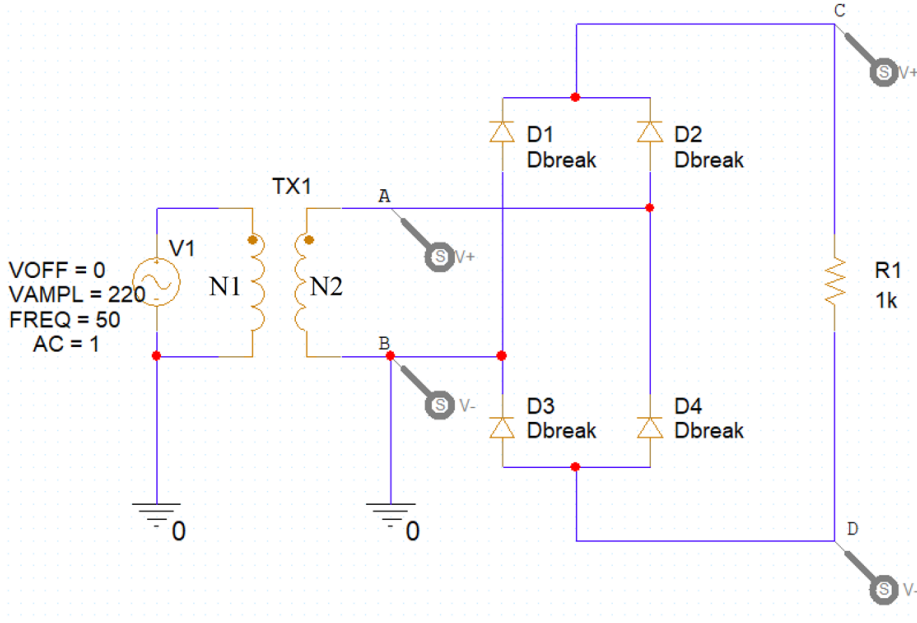


Figure 2.4: Full-wave bridge rectifier

### 2.2.1 Theory calculation

**Approximation:** Diodes have  $V_f = 0.7V$

$$V_{AB} = V_{\sin} \times \frac{N1}{N2} = 220 \cos(100\pi t) \times \frac{1}{10} = 22 \cos(100\pi t) (V)$$

During both half cycles, two diodes are conducting in series.

$$V_{CD} = \min(0, V_{AB} - 2V_f) = \min(22 \cos(100\pi t) - 1.4, 0)$$

### 2.2.2 Simulation

The sinusoidal waveform of the voltage difference  $V_{AB}$  has the period

$$T = \frac{1}{FREQ} = \frac{1}{50} = 0.02s = 20ms.$$

If we want to perform the transient analysis in 10 periods of the waveform  $V_{AB}$ , the required time would be:

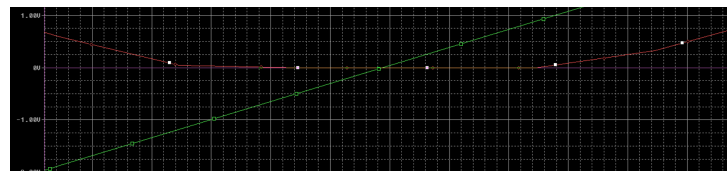
$$T_{total} = 10 \times T = 10 \times 0.02s = 0.2s.$$

$$\Delta t = \frac{T}{10} = \frac{0.02s}{10} = 0.002s = 2ms.$$

The screenshot shows an oscilloscope display with two waveforms,  $V(A,B)$  (red) and  $V(C,D)$  (green), plotted against time. The time scale is 2 ns/div. A probe cursor is positioned at 20.391 ns, highlighting a specific point on the  $V(C,D)$  waveform. Below the waveform, a table displays various measurement parameters for the selected cursor.

Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	21.573			
1 Values	154.812	0.000	148.520		Y1: Y1(Cursor1)	Y2: Y2(Cursor2)	Max Y	Min Y	Avg Y
Cursor 1,2	V(A,B)	21.878	0.000	21.878	0.000	0.000	21.878	0.000	10.939
	V(C,D)	20.391	597.221p	20.391	-1.4065	597.221p	20.391	597.221p	10.110

From the simulation result, we can see that  $V_{CD}$  or the red trace is always smaller than  $V_{AB}$  or the green trace, due to voltage drops across the conducting diodes. Also, when  $|V_{AB}| \leq 1.2(V)$ ,  $V_{CD}$  becomes zero because all diodes are off.



From the simulation result, we can verify that our theoretical calculations for  $V_{AB}$  and  $V_{CD}$  are nearly the same as the simulation results, except for some minor differences due to the idealized assumptions made in the theoretical calculations.

## 2.3 Zener Diodes as Regulators

The Zener diode has a well-defined reverse-breakdown voltage, at which it starts conducting current, and continues operating continuously in the reverse-bias mode without getting damaged. Additionally, the voltage drop across the diode remains constant over a wide range of voltages, a feature that makes Zener diodes suitable for use in voltage regulation.

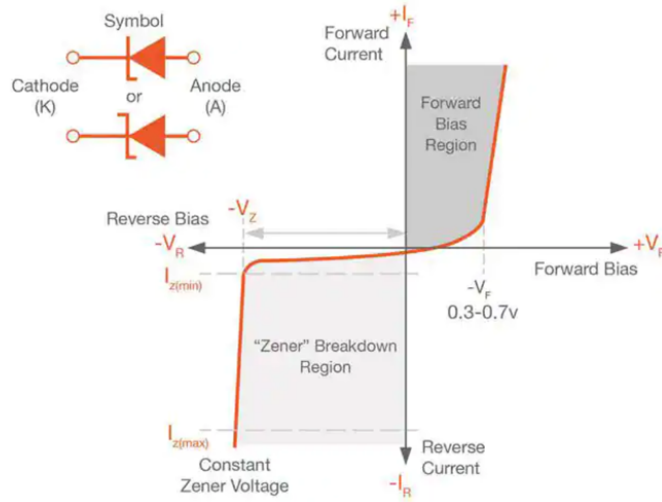


Figure 2.7: Electrical characteristic of Zener diode<sup>[6]</sup>

In this exercise, a Zener diode is used to design a voltage regular circuit. The schematic in this exercise is given following Figure 2.7.

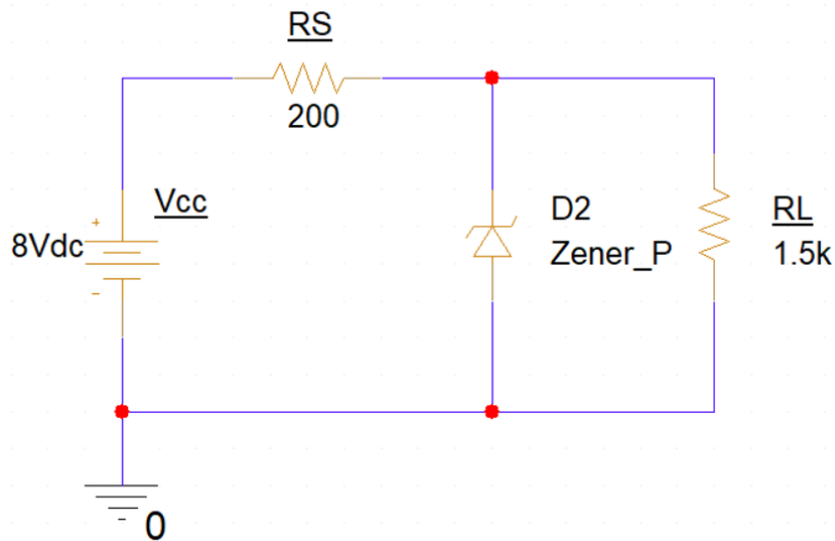


Figure 2.8: Voltage regulator using Zener diode<sup>[6]</sup>

The Zener component in the circuit can be found in the Favourites list by searching the keyword Zener. The full name of the component used in the circuit above is **Zenner\_P**

- **Zener Diode (parameterized)**. The default Zener voltage of this component is  $V_Z = 5V$ . However, this value can be changed in the properties of the component (right click and select Edit Properties) for other simulations. Theory calculation

- $I_L = \frac{V_Z}{R_L}$  (Ohm's Law).
- $I_S = \frac{V_{CC} - V_Z}{R_S}$  (KVL and Ohm's Law).
- $I_Z = I_S - I_L$  (KCL).
- $P_{RS} = I_S^2 \times R_S$ .
- $P_Z = I_Z \times V_Z$ .

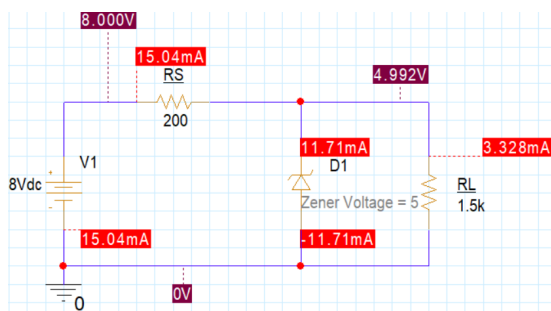
Then, perform the calculation for the Zener diode voltage regulator with two different input voltage, including 8V and 12V power supply. Finally, run the simulations in PSpice (in Bias Point simulation profile) to confirm with the theory calculation.

The results are summarized in the table below.

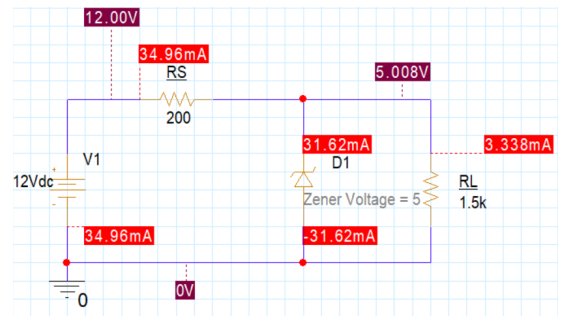
	Theory Calculation						PSpice Simulation					
	$I_S$	$I_L$	$I_Z$	$V_L$	$P_{RS}$	$P_Z$	$I_S$	$I_L$	$I_Z$	$V_L$	$P_{RS}$	$P_Z$
Vcc = 8V	15	3.33	11.67	5	0.045	0.06	15.04	3.33	11.71	5	0.05	0.06
Vcc = 12V	35	3.33	31.67	5	0.245	0.16	34.96	3.33	31.62	5	0.25	0.16

Table 2.1: Comparison between theoretical and PSpice simulation results for Zener regulator circuit

The following images show the PSpice simulation results for both input voltages.



(a) PSpice simulation result for Vcc = 8V



(b) PSpice simulation result for Vcc = 12V

Figure 2.9: PSpice simulation results for Zener regulator circuit at different input voltages

## 2.4 AC/DC Power Circuit Application

In this exercise, we are building step by step an AC to DC voltage source transformation circuit. Students perform a time-domain simulation and write out comments and explanations for each step.

- **Step 1:** The rectified voltage without any filtering or being regulated.

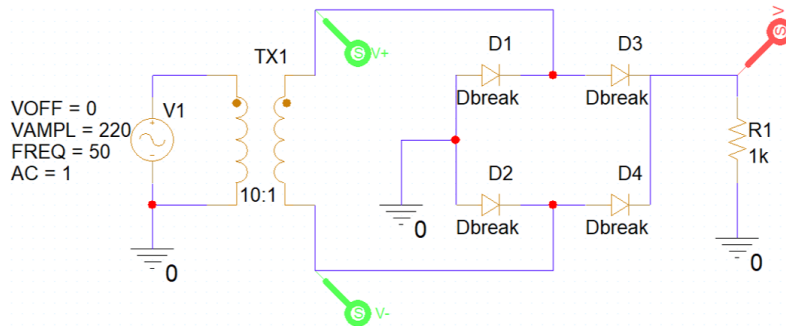


Figure 2.10: The rectified voltage without any filtering or being regulated

**Comments:** The simulation result is similar to the exercise 7 because the two circuit are thee same.

- **Step 2:** Rectified voltage regulated with a  $10\mu\text{F}$  capacitor

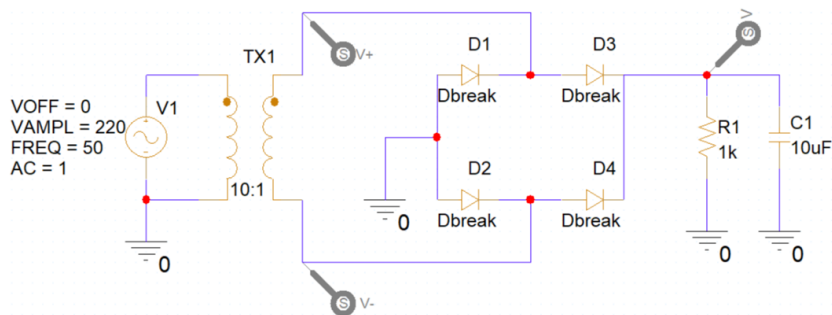
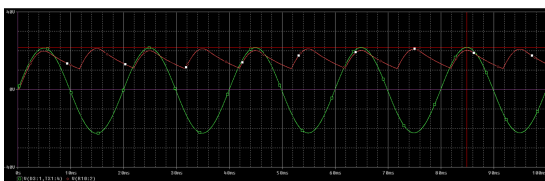


Figure 2.11: The rectified voltage regulated with a  $10\mu\text{F}$  capacitor

**Simulation result:**



(a) Waveform of the output voltage

Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	21.689			
	X Values	84.903m	0.000	84.903m	Y1 - Y1(Cursor1) Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y	
CURSOR 1:2	V(D3:1,TX1:4)	21.689	0.000	21.689	0.000	0.000	21.689	0.000	10.845
	V(R1:2)	20.216	2.3245f	20.216	-1.4718	2.3245f	20.216	2.3245f	10.109

(b) Max value of the output voltage

Figure 2.12: Simulation results of Step 1

**Comments:** The output voltage waveform is better when compared to step 1. However, there are still ripples on the output voltage. This is the role of the capacitor, which helps to smooth the output voltage. The maximum voltage between differential markers is around 21.6V, which is close to the expected value of  $V_{max} = 22V$ . In addition, the maximum output voltage is around 20.2V, which is exactly 1.2V drops from 2 diodes in series.

- **Step 3:** Replace the 10 $\mu$ F capacitor with a 680 $\mu$ F one and re-run the simulation, recognize the change in the result and explain.

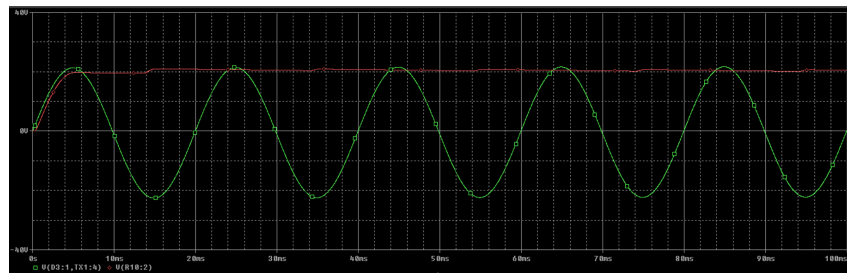


Figure 2.13: The rectified voltage regulated with a 680 $\mu$ F capacitor

**Comments:** The output voltage waveform is much better when compared to step 2. The ripples on the output voltage are significantly reduced. This is because the larger capacitor can store more charge, which helps to smooth out the voltage fluctuations. The maximum voltage between differential markers is around 21.7V, which is closer to the expected value of  $V_{max} = 22V$ . And the output voltage is around 20.4V.

- **Step 4:** Add a zener diode as in Figure 2.14 with the zener voltage properties set to 22 volts then simulate the circuit and comment or explain the result.

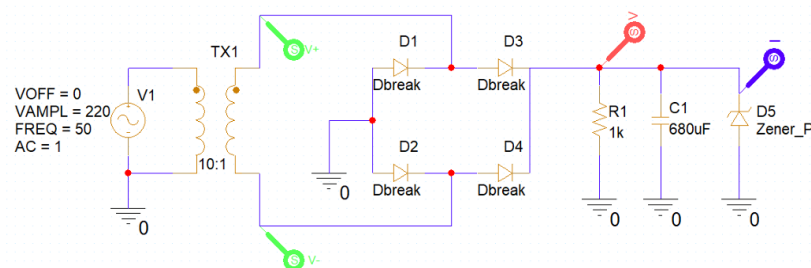


Figure 2.14: Rectified voltage regulated with a capacitor and a zener diode

**Simulation result:**

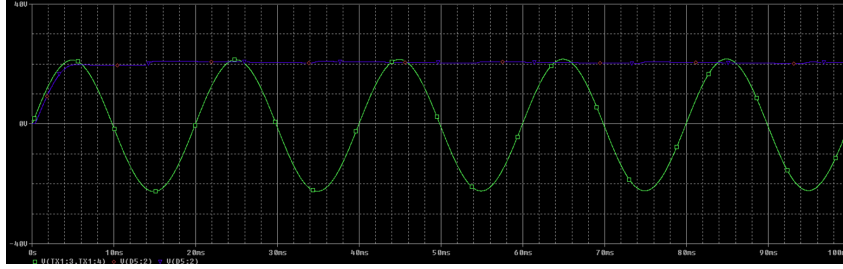


Figure 2.15: The output voltage with a zener diode added

**Comments:** The zener diode helps to regulate output voltage to  $V_{zener}$  if the output voltage exceed  $V_{zener} = 22V$ ; However, as the highest output voltage cap at around  $20.4V$ , according to the simulation result in step 3, the zener diode does not change anything in the output voltage waveform.

- **Step 5:** Change the zener voltage properties of the zener diode to 20 volts and then re-run the simulation. Comment and explain any changes in the result. **Simulation result:**

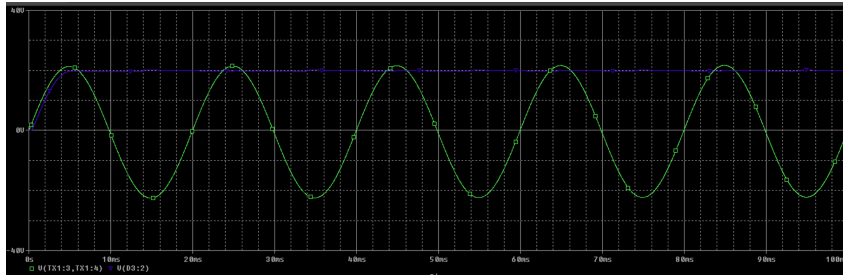


Figure 2.16: The output voltage with a zener diode of  $V_{zener} = 20V$  added

**Comments:** As explain in step 4, now because the output voltage exceed  $V_{zener} = 20V$ , the zener diode starts to conduct in reverse bias and regulate the output voltage to around  $20V$ . This can be seen in the simulation result where the output voltage waveform is clamped at around  $20V$ .



## 2.5 Exercise 8: AC/DC Power Circuit Application With LM2596\_5P0\_TRANS

Figure 2.17 describes an incomplete Texas Instrument LM2596-5.0 Switching Power Supply circuit. It lacks a Zener diode voltage regulator and an inductor reducing the voltage variation. At first, let perform a time-domain (transient) simulation with this incomplete circuit and figure out the problem with the output voltage (the voltage marker at R1).

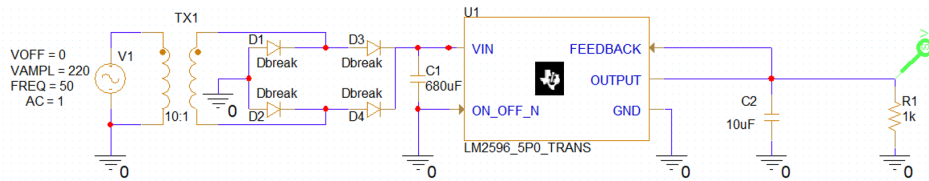
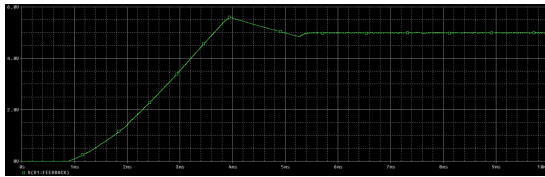
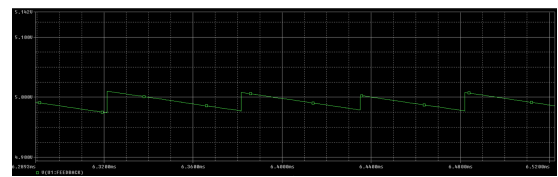


Figure 2.17: Incomplete switching power supply circuit

### *Simulation results:*



(a) Output voltage waveform

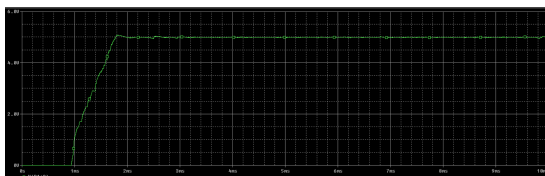


(b) Output voltage zoomed-in waveform

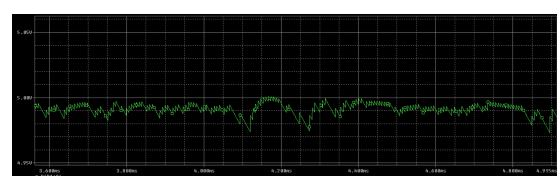
Figure 2.18: Output voltage waveforms of the incomplete circuit

**Comment and explanation:** From the simulation results in Figure 2.18, we can see that in the 2.18a, the output voltage rise from 0V to about 5.75V and then drop to about 5.0V and become stable after that. However, if we zoom closer, the wave form is not a straight line. This phenomenon happens because we are not using Zener diode and inductor regulator.

Next, add an inductor 33μH to the circuit as shown in Figure 2.17 then re-run the simulation and explain any improvements.



(a) Output voltage waveform with inductor



(b) Output voltage zoomed-in waveform with inductor

Figure 2.19: Output voltage waveforms with inductor added

**Simulation results:** From the new simulation results in Figure 2.19, we can see that the voltage just rise to approximately  $5V$  and become stable, but not exceed  $5V$  as before. Also, the zoomed-in waveform of voltage is softer and smoother than before. This is the effect of the inductor added to the circuit, which helps reduce voltage variation.

Continue, add a  $5V$  Zener diode to the circuit as shown in Figure 1.36, change the capacitor to  $220\mu F$ , add a current marker to the Zener diode, re-run the simulation and explain the role of the Zener diode in the circuit.

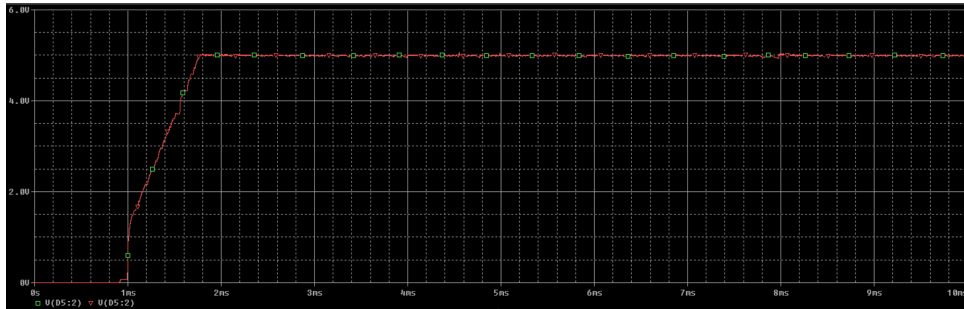


Figure 2.20: Complete switching power supply circuit with Zener diode and inductor

**Simulation results:** From the new simulation results in Figure 2.20, the waveform is similar but it is more straight and stable. Also, the Zener help to protect the circuit from spike and over voltage.

## References

- [1] Donald E. Knuth. Literate programming. *The Computer Journal*, 27(2):97–111, 1984.
- [2] Donald E. Knuth. *The T<sub>E</sub>X Book*. Addison-Wesley Professional, 1986.
- [3] Leslie Lamport. *L<sup>A</sup>T<sub>E</sub>X: a Document Preparation System*. Addison Wesley, Massachusetts, 2 edition, 1994.
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- [5] Frank Mittelbach, Michel Gossens, Johannes Braams, David Carlisle, and Chris Rowley. *The L<sup>A</sup>T<sub>E</sub>X Companion*. Addison-Wesley Professional, 2 edition, 2004.
- [6] Le Trong Nhan. *CO2104 Fall 2025 Lab 02*. Ho Chi Minh University of Technology - VNUHCM, 2025.