TCC805x Hardware

Application Note for Choosing Pull-up and down Resistor at Input Port

Rev. 1.00 [G]
2024-08-09

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1 INTRODUCTION

This document is a guideline for determining which resistor to use: a pull-up or pull-down resistor, as well as the appropriate pull-up and pull-down resistances for the Input GPIO ports. When selecting the pull-up or pull-down resistance, if you do not consider the initial configuration at the RESET state and the leakage current through the input port, you may not get the expected logic value.

2 INITIAL CONFIGURATION AT RESET STATE FOR GPIOS

In TCC805x, the initial GPIO setting can be configured as disabling both the input and output in the RESET state. In this configuration state, the GPIO consumes less leakage current. Therefore, you can freely set the port considering only the port condition of the device regardless of whether the initial configuration at the RESET state is input pull-down or input pull-up. This chapter describes three types of GPIO settings. You can change these GPIO settings after RESET release.

Table 2.1 Initial Value for GPIOs of TCC805x

GPIO	TCC805x			
	OE	IE	PE	PS
GPIO_A[28:0]	0	1	1	0
GPIO_A[31:29]	0	0	1	0
GPIO_B[28:0]	0	0	1	0
GPIO_C[29:0]	0	0	1	0
GPIO_E[19:0]	0	0	1	0
GPIO_G[10:0]	0	0	1	0
GPIO_H[11:0]	0	0	1	0
GPIO_K[18:13], GPIO_K[10:0]	0	0	0	0
GPIO_K[11]	1	0	0	0
GPIO_K[12]	0	1	0	0
GPIO_MA[28:0]	0	1	1	0
GPIO_MA[29]	0	0	1	0
GPIO_MB[31:0]	0	0	1	0
GPIO_MC[29:0]	0	0	1	0
GPIO_MD[17:0]	0	0	1	0
GPIO_SD0[14:10]	0	0	1	0
GPIO_SD0[9:0]	0	0	0	0
GPIO_SD1[10]	0	0	1	0
GPIO_SD1[9:0]	0	0	0	0
GPIO_SD2[9:0]	0	0	0	0

- OE: Output enable (1: enable, 0: disable)
- IE: Input enable (1: enable, 0: disable)
- PE: Pull enable (1: enable, 0: disable)
- PS: Pull select (1: Pull-up, 0: Pull-down)

2.1 Type 1

The initial configuration at the RESET state for GPIO_SD0[9:0], GPIO_SD1[9:0], GPIO_SD2[9:0], and all GPIO_K (except GPIO_K[12:11]):

- Input, output disable
- Internal pull-up/down disable
- OE=0, IE=0, PE=0, PS=0
  - OE=0: Output disable
  - IE=0: Input disable
  - PE=0: Pull disable
  - PS=0: Pull-down select (Pull-down is not applied because PE=0)
  - Initial configuration at the RESET state for GPIO_K[11] is Output High.

To select the value of the external pull-up or pull-down resistor, refer to Chapter 3.

Note: A GPIO_K[11] port cannot be used as a general GPIO. This port can be used only as an indicator pin to indicate specific status.

2.1.1 Precautions for Type 1 Port

This chapter describes the precautions for the type 1 port based on the port status of the device connected to the port.
When disabling the input and output, there is no internal leakage of the GPIO.

If the port of any device connected to Type 1 port is in the input state, the port requires pull-up or pull-down resistor to prevent floating state of the device's port.
If the port of any device connected to Type 1 port is in the output state, the device must control the logic state of the output port not to be in unknown state.

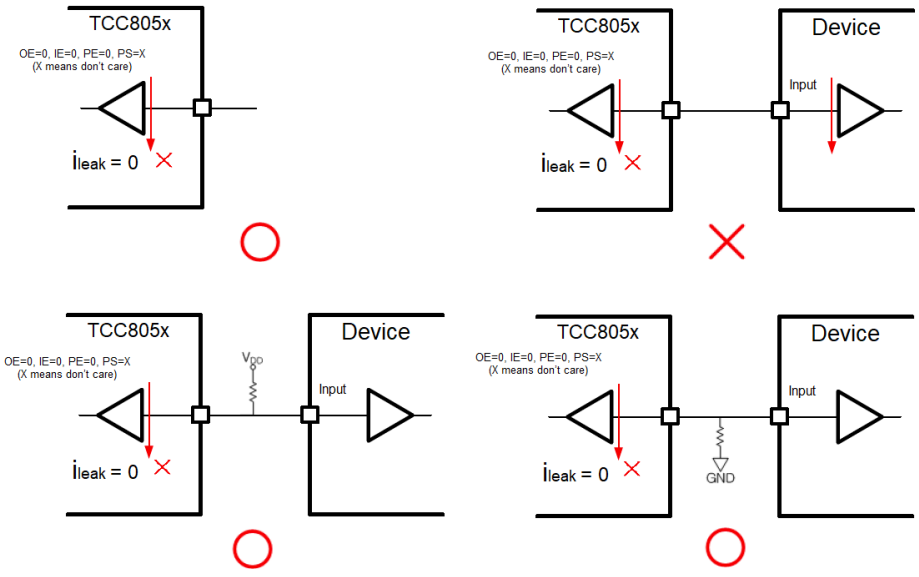

Figure 2.1 Cases that Device Port is Input State at RESET State

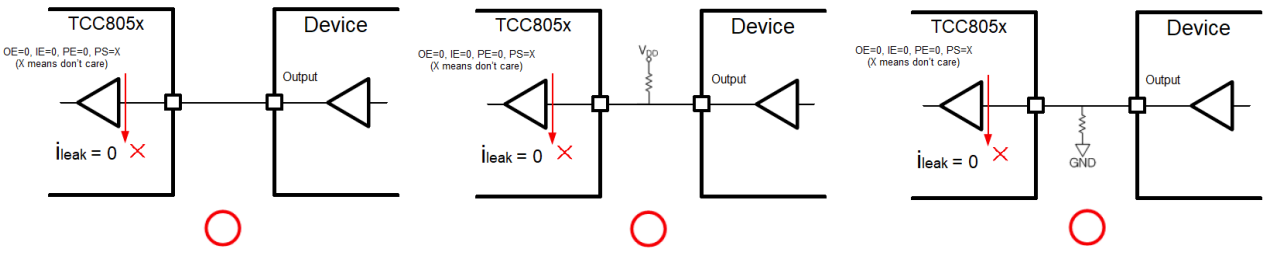

Figure 2.2 Cases that Device Port is Output State at RESET State

2.2 Type 2

The initial configuration at the RESET state for GPIO_B/C/E/G/H/MB/MC/MD, GPIO_SD0[14:10], GPIO_SD1[10], GPIO_A[31:29], GPIO_MA[29]:

- Input, output disable
- Internal pull-down enable
- OE=0, IE=0, PE=1, PS=0
  - OE=0: Output disable
  - IE=0: Input disable
  - PE=1: Pull enable
  - PS=0: Pull-down select

2.2.1 Open State or External Pull-down State at Type 2 Port

These cases are normal.

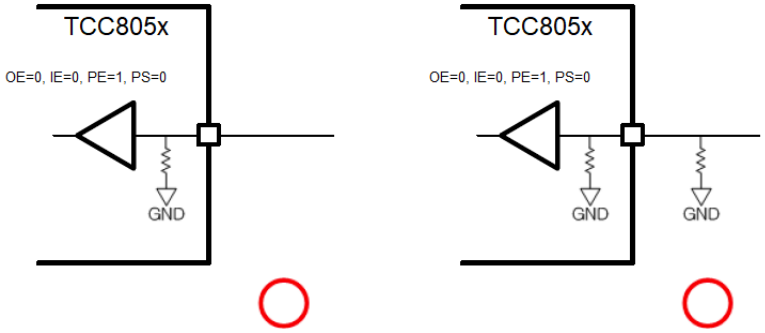

Figure 2.3 Case of Open or External Pull-down State at RESET State

2.2.2 External Pull-up State at Type 2 Port

If divided voltage is between VIH and VIL, the voltage may cause a leakage current.
Therefore, the pull-up resistance should be used so that the divided voltage becomes higher than VIH.
It is recommended to use a pull-up resistor of 4.7K or less for 3.3V I/O and 2.4K or less for 1.8V I/O for this case.

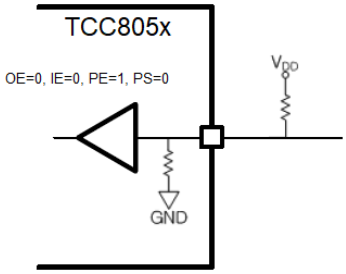

Figure 2.4 Case of Internal Pull-down and External Pull-up State at RESET State

Table 2.2 Internal Resistance of Pull-up/Pull-down for GPIO SD0

Parameter	MIN	TYP	MAX
	DVDD=1.95V T_J = -40 ℃ Process = Fast	DVDD = 1.8V T_J = 25 ℃ Process = Typical	DVDD = 1.65V T_J = 125 ℃ Process = Slow
Pull-up	19 kΩ	44 kΩ	86 kΩ
Pull-down	20 kΩ	40 kΩ	73 kΩ

Table 2.3 Internal Resistance of Pull-up/Pull-down for General & Alive I/O

Parameter	MIN	TYP	MAX
	DVDD = 3.6V T_J = -40 ℃ Process = Fast	DVDD = 3.3V T_J = 25 ℃ Process = Typical	DVDD = 3.0V T_J = 125 ℃ Process = Slow
Pull-up	15 kΩ	25 kΩ	83 kΩ
Pull-down	20 kΩ	36 kΩ	75 kΩ

Table 2.4 Internal Resistance of Pull-up/Pull-down for General & Alive I/O

Parameter	MIN	TYP	MAX
	DVDD = 1.95V T_J = -40 ℃ Process = Fast	DVDD = 1.8V T_J = 25 ℃ Process = Typical	DVDD = 1.65V T_J = 125 ℃ Process = Slow
Pull-up	11 kΩ	21 kΩ	49 kΩ
Pull-down	12 kΩ	21 kΩ	73 kΩ

2.3 Type 3

The initial configuration at the RESET state for GPIO_A[28:0] and GPIO_MA[28:0]:

- Input enable, output disable
- Internal pull-down enable
- OE=0, IE=1, PE=1, PS=0
  - OE=0: Output disable
  - IE=1: Input enable
  - PE=1: Pull enable
  - PS=0: Pull-down select

2.3.1 Open State or External Pull-down State at Type 3 Port

These cases are normal.

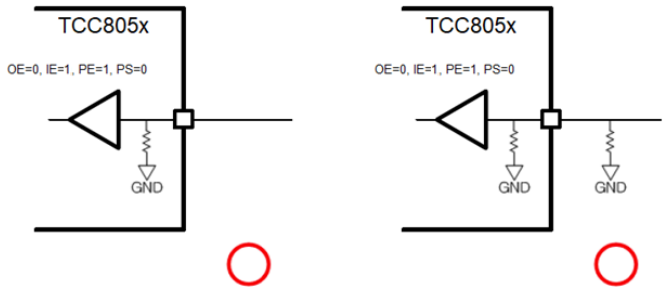

Figure 2.5 Case of Open or External Pull-down State at RESET State

2.3.2 External Pull-up State at Type 3 Port

If the divided voltage is between VIH and VIL, the voltage can cause a leakage current.
Therefore, the pull-up resistance should be used so that the divided voltage becomes higher than VIH.
It is recommended to use a pull-up resistor of 4.7K or less for 3.3V I/O and 2.4K or less for 1.8V I/O for this case.
Refer to Table 2.2, Table 2.3, and Table 2.4 for the internal resistance of pull-up and pull-down for each GPIO.

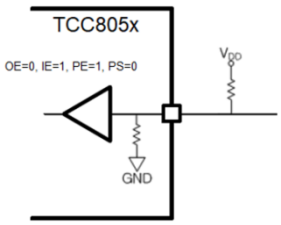

Figure 2.6 Case of Internal Pull-down and External Pull-up State when RESET State

2.4 Type 4

The initial configuration at the RESET state for GPIO_K[12]:

- Input enable, output disable
- Internal pull-up/down disable
- OE=0, IE=1, PE=0, PS=0
  - OE=0: Output disable
  - IE=1: Input enable
  - PE=0: Pull disable
  - PS=0: Pull-down select (Pull-down is not applied because of PE=0)

A GPIO_K[12] port cannot be used as a general GPIO because this port is used only as a dedicated pin for STR_MODE.
The STR_MODE pin requires an external pull-down resistor.
For pull-down resistance, a value of 23K or less is recommended.
To select the value of external pull-down resistor, refer to Chapter 3.

2.4.1 Precautions for Type 4 Port

If the port of any device connected to Type 4 port is in input state, the port requires pull-up or pull-down resistor to prevent floating state of the device's port. However, GPIO_K[12] is a dedicated pin for STR_MODE and the STR_MODE pin requires pull-down resistor, so only the pull-down resistor should be applied to GPIO_K[12].

If the port of any device connected to type 4 port is in the output state, the device must control the logic state of the output port not to be in unknown state. However, it is recommended to apply a pull-down resistor to STR_MODE regardless of the following cases.

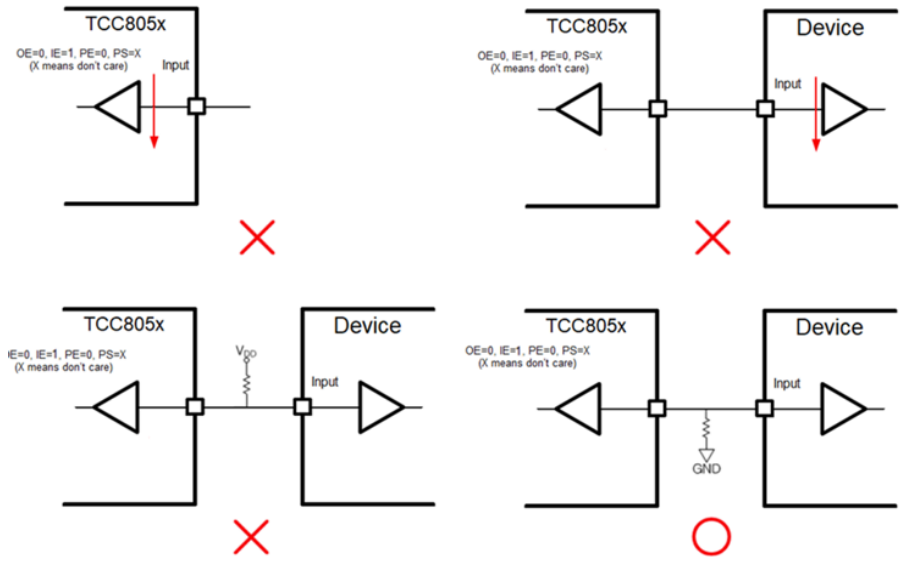

Figure 2.7 Cases that Device Port is Input State at RESET State

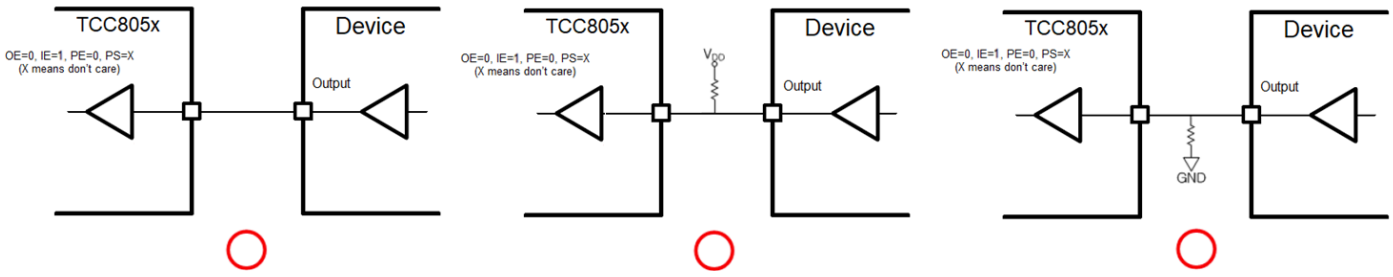

Figure 2.8 Cases that Device Port is Output State at RESET State

3 GENERAL INPUT PORT STRUCTURE

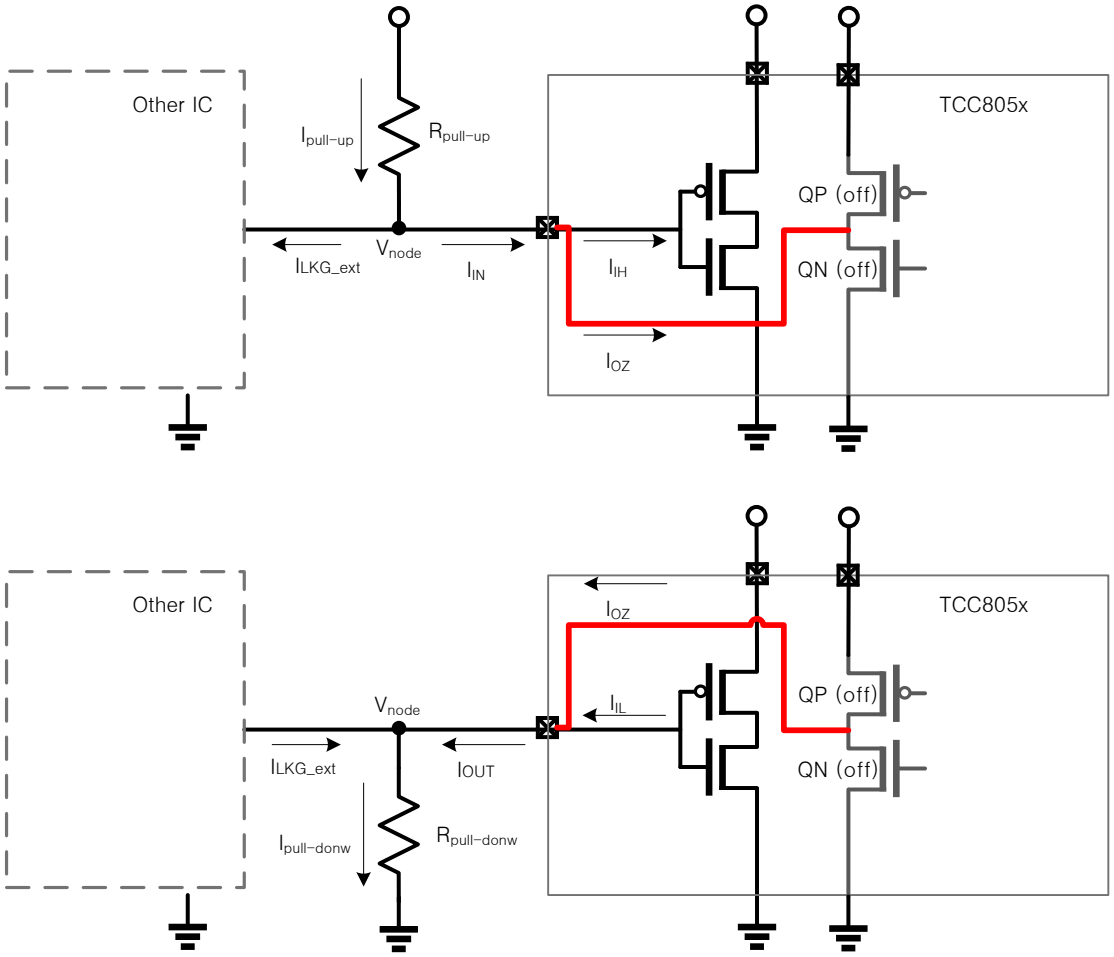

Figure 3.1 Typical Input with External Pull-up and Pull-down Circuitry

3.1 Calculating Pull-up & down Resistance Range at Input Port

In order for the input port to be pulled high by the pull-up resistor, the output driver (Q) of the external IC is turned off and the logic high is driven by the pull-up resistor. There is some leakage current (I_{LKG_ext}) even though the output driver (Q) is off.

In general, the current flow through the pull-up resistor is calculated as the sum of the leakage current (I_{LKG_ext}) of the external IC, the high level input current (I_{IH}) of the TCC805x, and the tri-state output leakage current (I_{OZ}). However, I_{IH} and I_{IL} in the "*TCC805x Chip Specification*" are included with I_{OZ}.

$$I_{pull-up} = I_{LKG\_ext} + I_{OZ} + I_{IH}$$

Thus, the maximum pull-up resistance is derived as follows:

$$R_{pull-up,max} = \frac{V_{out} - V_{IH}}{I_{pull-up}}$$

Conversely, the maximum pull-down resistance is derived as follows:

$$R_{pull-down,max} = \frac{V_{IL}}{I_{pull-down}}$$

Table 3.1, Table 3.2, and Table 3.3 show I_{IH}, I_{IL}, and GPIO voltage range of TCC805x.

Table 3.1 DC Electrical Specification for General I/O

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
3.3V Tol and Non-Tol I/O						
High Level Input Voltage for Schmitt trigger operation	V_{IH}	CMOS/Schmitt trigger Interface	0.7 * V_{DDIO}		V_{DDIO}+0.3	V
Low Level Input Voltage for CMOS or Schmitt trigger operation	V_{IL}	CMOS/Schmitt trigger Interface	-0.3		0.3 * V_{DDIO}	V
Input Hysteresis for Schmitt Trigger Operation	V_H		0.08 * V_{DDIO}			V
High Level Input Current	I_{IH}	Non-Tol cell VIN = V_{DDIO} Pull-down disabled Power On	-12		12	µA
		Fail-safe cell VIN = V_{DDIO} Pull-down disabled Power ON	-12		12	µA
		Fail-safe cell VIN = V_{DDIO} Pull-down disabled Power Off & SNS = 0	-18		18	µA
		VIN = V_{DDIO} Pull-down enabled	25		200	µA
Low Level Input Current	I_{IL}	Non-Tol or Fail-safe VIN = VSS Pull-up disabled	-18		18	µA
		VIN = VSS Pull-up enabled	-25		-200	µA

Table 3.2 DC Electrical Specification for Alive I/O (GPIO_K, PCTL0, PCTL1)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Non-Tol I/O						
Tolerant External Voltage	V_{TOL}	V_{DDIO} Power Off and On			3.6	V
High Level Input Voltage	V_{IH}	CMOS Interface	0.7 * V_{DDIO}		V_{DDIO}+0.3	V
Low Level Input Voltage	V_{IL}	CMOS Interface	-0.3		0.3 * V_{DDIO}	V
Hysteresis Voltage	ΔV		0.08 * V_{DDIO}			V
High Level Input Current	I_{IH}	Input Buffer for Non-Tol cell VIN = V_{DDIO} VDDIO Power On	-12		12	µA
		Input Buffer for Fail-safe cell VIN = V_{DDIO} V_{DDIO} Power On	-12		12	µA
		Input Buffer for Fail-safe cell VIN = V_{DDIO} V_{DDIO} Power Off and SNS = 0	-18		18	µA
		Input Buffer with pull-down VIN = V_{DDIO}	25		200	µA
Low Level Input Current	I_{IL}	Input Buffer for Non-Tol or Fail-safe VIN = VSS	-18		18	µA
		Input Buffer with pull-up VIN = VSS	-25		-200	µA

Table 3.3 DC Electrical Specification for GPIO_SD0

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
1.8V Tol and Non-Tol I/O						
Tolerant External Voltage	V_{TOL}	High voltage tolerant function is not supported				V
High Level Input Voltage	V_{IH}	CMOS/Schmitt Interface	0.65 * V_{DDIO}		V_{DDIO}	V
Low Level Input Voltage	V_{IL}	CMOS/Schmitt Interface	VSS		0.35*V_{DDIO}	V
Hysteresis Voltage	ΔV		0.1			V
High Level Input Current	I_{IH}	Input buffer VIN = VDD, VDD Power On	-12		12	μA
Low Level Input Current	I_{IL}	Input Buffer VIN = VSS, VDD Power On	-12		12	μA

Note: I_{IH} and I_{IL} include I_{OZ}.

Table 3.4 I/O Power Information

Group	MIN	TYP	MAX	Description
PWRGPIOx_33D	1.65 3.00	1.80 3.30	1.95 3.60	GPIOx Group I/O Power x: A, B, C, E, G, H, MA, MB, MC, MD, SD1, SD2, K, SYS
PWRGPIOSD0_18D	1.65	1.80	1.95	GPIO SD0 Group I/O Power

Calculate the **pull-up resistance** by applying the V_{IH}, V_{IL} of I/O voltage and the worst value of I_{IL}, and I_{IH} for **General I/O and Alive I/O** of TCC805x.

- V_{IH}: 0.7 * V_{DDIO} = 0.7 * 3.3 = 2.31V
- V_{IH}: 0.7 * V_{DDIO} = 0.7 * 1.8 = 1.26V
- Worst I_{IH}: 18 μA
- Assumed Values
  - I_{LKG_ext}: 5 μA

Note: I_{LKG_ext} is assumed to be 5 μA to calculate the resistance, and the I_{LKG_ext} is different depending on the actual specification of external IC. The calculated resistance depends on I_{LKG_ext}.

$$I_{pull-up} = Worst\ I_{IH} + I_{LKG\_ext} = 18 + 5 = 23\ \text{uA}$$

$$R_{pull-up,max} = \frac{(3.3 - 2.31)V}{23\ uA} = \frac{0.99\ V}{23\ uA} = 43K\Omega$$

$$R_{pull-up,max} = \frac{(1.8 - 1.26)V}{23\ uA} = \frac{0.54\ V}{23\ uA} = 23K\Omega$$

Calculate the **pull-up resistance** by applying the V_{IH}, V_{IL} of I/O voltage and the worst value of I_{IL}, I_{IH} for **GPIO SD0** of TCC805x.

- V_{IH}: 0.65 * V_{DDIO} = 0.65 * 1.8 = 1.17V
- Worst I_{IH}: About 12 μA
- Assumed Values
  - I_{LKG_ext}: 5 μA

Note: I_{LKG_ext} is assumed to be 5 μA to calculate the resistance, and the I_{LKG_ext} is different according to the actual external IC specification. The calculated resistance depends on I_{LKG_ext}.

$$I_{pull-up} = Worst\ I_{IH} + I_{LKG\_ext} = 12 + 5 = 17\ \text{uA}$$

$$R_{pull-up,max} = \frac{(1.8 - 1.17)V}{17\ uA} = \frac{0.63\ V}{17\ uA} = 37K\Omega$$

As above, calculate the **pull-down resistance** for **General I/O and Alive I/O** of TCC805x.

- V_{IL}: 0.3 * V_{DDIO} = 0.3 * 3.3 = 0.99V
- V_{IL}: 0.3 * V_{DDIO} = 0.3 * 1.8 = 0.54V
- Worst I_{IL}: 18 μA
- Assumed Values
  - I_{LKG_ext}: 5 μA

Note: I_{LKG_ext} is assumed to be 5 μA to calculate the resistance, and the I_{LKG_ext} is different depending on the actual specification of external IC. The calculated resistance depends on I_{LKG_ext}.

$$I_{pull-down} = Worst\ I_{IL} + I_{LKG\_ext} = 18 + 5 = 23\ \text{uA}$$

$$R_{pull-down,max} = \frac{(0.99)V}{23\ uA} = \frac{0.99\ V}{23\ uA} = 43\text{K}\Omega$$

$$R_{pull-down,max} = \frac{(0.54)V}{23\ uA} = \frac{0.54\ V}{23\ uA} = 23K\Omega$$

As above, calculate the **pull-down resistance** for **GPIO SD0** of TCC805x.

- V_{IL}: 0.35 * V_{DDIO} = 0.35 * 1.8 = 0.63V
- Worst I_{IL}: 12 μA
- Assumed Values
  - I_{LKG_ext}: 5 μA

Note: I_{LKG_ext} is assumed to be 5 μA to calculate the resistance, and the I_{LKG_ext} is different depending on the actual specification of external IC. The calculated resistance depends on I_{LKG_ext}.

$$I_{pull-down} = Worst\ I_{IL} + I_{LKG\_ext} = 12 + 5 = 17\ \text{uA}$$

$$R_{pull-down,max} = \frac{(0.63)V}{17\ uA} = \frac{0.63\ V}{17\ uA} = 37K\Omega$$

3.2 Recommended $R_{pull-up}$, $R_{pull-down}$, and R_{max} Value

In an operating environment, there may be various variations such as voltage drop, temperature, and PCB condition.
Therefore, choose a value considering margins.

If the pull-up resistance is too high, a voltage drop will occur and a logic value below V_{IH} can be input.
Conversely, in case of the pull-down resistance, a logic value higher than V_{IL} can be input if the leakage current does not sink to ground. This causes the TCC805x not to recognize the logic value normally.
Also, inexplicit voltage level by pull-up and pull-down resistors can cause the leakage current.
Therefore, you must select the appropriate value when determining the pull-up and down resistance.

4 CONCLUSION

When considering a pull-up or pull-down resistor for the GPIOs of input state, a pull-up resistor of 4.7K or less for 3.3V I/O and 2.4K or less for 1.8V I/O is recommended as described in Chapter 2.2.2 and Chapter 2.3.2 (External pull-up at Type 2 port and Type 3 port). In other cases, you can determine the value of resistor by referring to Chapter 3.

5 REFERENCES

[1] Contact Telechips for more details: sales@telechips.com
[2] TCC805x_CS_Design_Change_Related_To_Hardware_Board_Design

Note: Reference documents can be provided whenever available, depending on the terms of a contract. If the reference documents are unavailable, the contents directly related to your development can be guided.

6 REVISION HISTORY

Rev. 1.00: 2024-08-09

- Changed
  - Title changed from "TCC805x ~~Common~~ Hardware-Application Note for Choosing Pull-up and down Resistor at Input Port"

Rev. 0.02: 2021-04-19

- Updated
  - Chapter 2.1: added **Note** about GPIO_K[11]
  - Chapter 2.1.1: Description
  - Chapter 2.4: added description about STR_MODE
  - Chapter 2.4.1:
    - added description about STR_MODE
    - Figure 2.7
  - Chapter 3.1: Table 3.1, Table 3.2, Table 3.3

Rev. 0.01: 2020-09-09

- Preliminary version release

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