Lab 8 - Finite State Machines

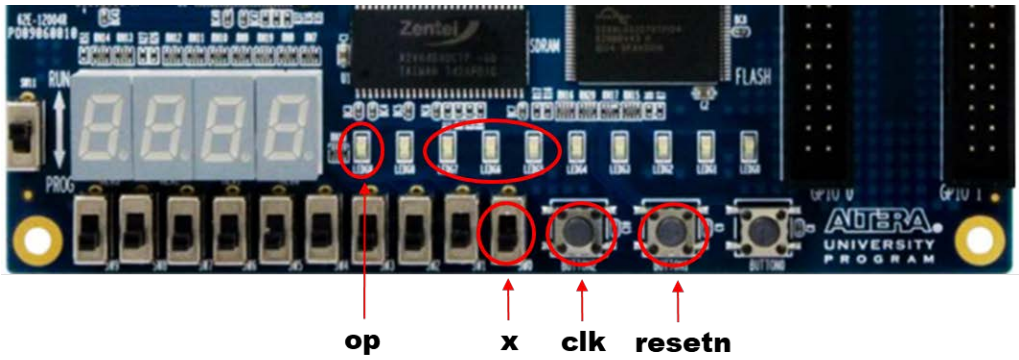
The purpose of this lab is to exercise finite state machines.

Lab 8.1:

Design a sequence detector(I).

With reference to the sequence detector specified on page 11 of lab8_instruction, Write VHDL code for it and assign pins on DE0 as follows.

- Use switch SW0 as input **x**, LEDG9 as the output **op**, and LEDG7-5 to represent **present state**.
- Use Button1 as an active-low asynchronous reset, Button2 as a clock input.



Lab 8.2:

Design a sequence detector(II).

We wish to implement a finite state machine (FSM) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s or four consecutive 0s. There is an input w and an output z. Whenever w = 1 or w = 0 for four consecutive clock pulses, the value of z has to be 1; otherwise, z = 0. Overlapping sequences are allowed, so that if w = 1 for five consecutive clock pulses the output z will be equal to 1 after the fourth and fifth pulses. Figure 1 illustrates the required relationship between w and z.

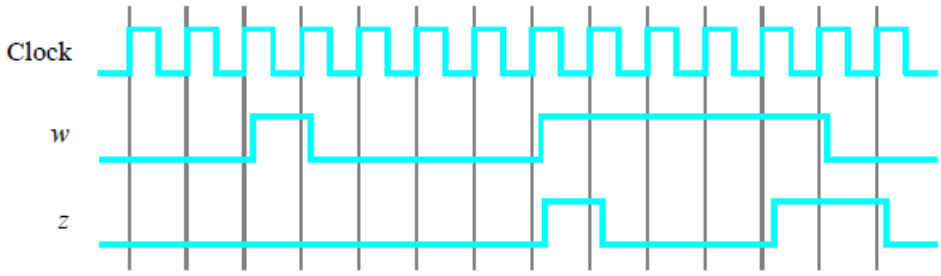
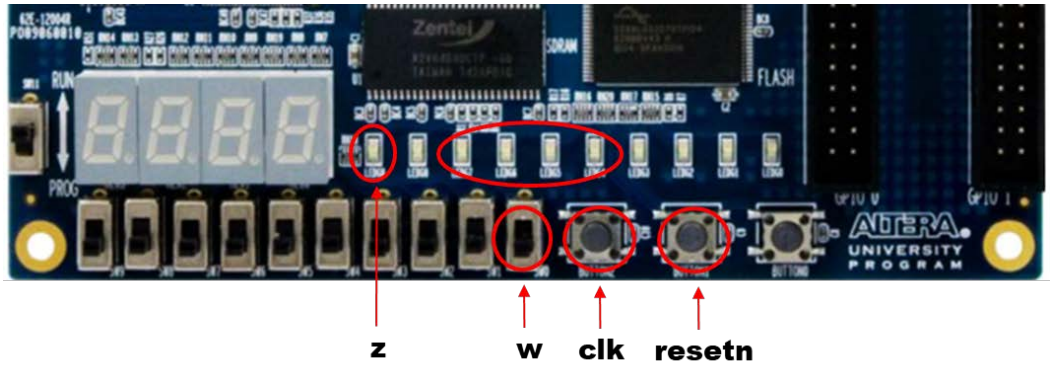


Figure 1: Required timing for the output z.

Design and implement your circuit on the DE0 board as follows

- Use switch SW0 as input **w**, LEDG9 as the output **z**, and LEDG7-4 to represent **present state**.
- Use Button1 as an active-low asynchronous reset, Button2 as a clock input.



Lab-report:

Submit a lab report on **ilearn** by 11:00pm the day before of next lab. (The lab report must be a **PDF** file.) Your Lab report should include the following items:

1) VHDL design and simulation for the sequence detector(I).

2) VHDL design and simulation for the sequence detector(II).