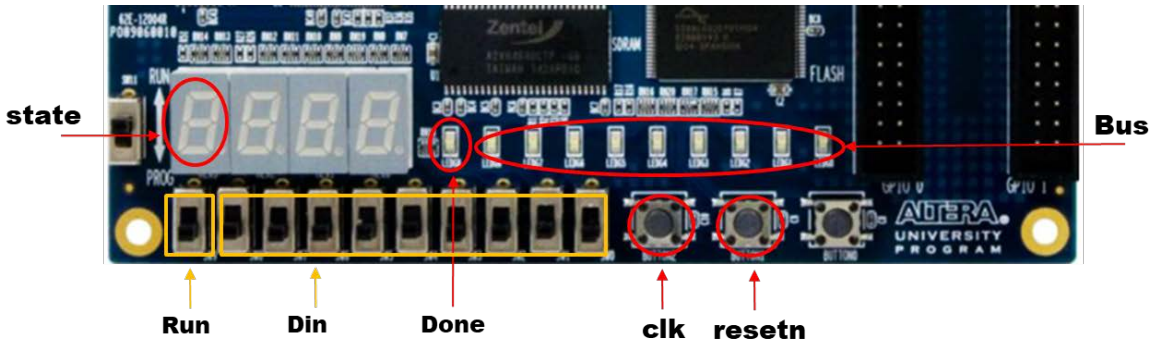
Lab 13- A 9-bit processor

Lab 13.1:

FPGA prototyping a simple 9-bit processor.

With reference to material in “a simple processor(I).pdf”, prototype the processor as follows.

- Create a Quartus II project which will be used for implementation of the circuit on the Altera DE0 board. This project should consist of a top-level entity that contains the appropriate input and output ports for the Altera board. Instantiate your processor in this top-level entity.
- Use switches SW_{8-0} to drive the DIN input port of the processor and use switch SW_9 to drive the Run input.
- Use Button1 as an active-low asynchronous reset, Button2 as a clock input.
- Connect the processor bus wires to $LEDG_{8-0}$ and connect the Done signal to $LEDG_9$.
- Indicate the current state on Hex3, i.e. 0 ~ 3.
- Test the functionality of your design by toggling the switches and observing the LEDs. Since the processor’s clock input is controlled by a push button switch, it is easy to step through the execution of instructions and observe the behavior of the circuit.



Lab 13.2:

FPGA prototyping an enhanced 9-bit processor

With reference to material in “cpu_project.pdf”, prototype the processor. The DE0 setting is the same as Lab13-1.

Lab-report:

Submit a lab report on **ilearn** by 11:00pm the day before of next lab. (The lab report must be a **PDF** file.) Your Lab report should include the following items for the enhanced 9-bit processor:

1) VHDL code.

2) An architecture diagram, i.e., p.21 in lecture09.

2) A table shows the control signals asserted in each instruction/time step, i.e., p.25 in lecture09.

2) Observations and comments.