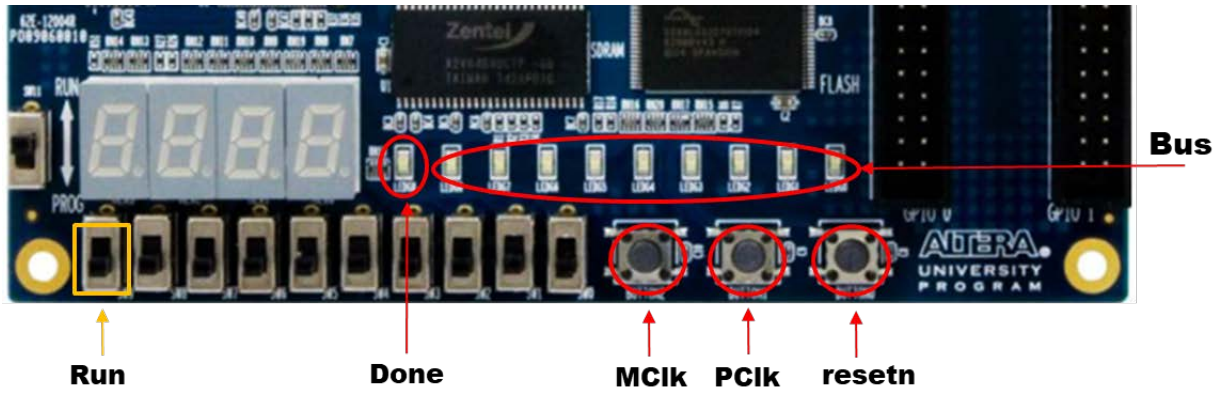
Lab 14- A simple 9-bit processor (II)

Lab 14.1:

FPGA prototyping a processor (II).

With reference to material in lab14_a simple processor(II).pdf, prototype the processor as follows.

- Create a Quartus II project which will be used for implementation of the circuit on the Altera DE0 board. This project should consist of a top-level entity that contains the appropriate input and output ports for the Altera board. Instantiate your processor in this top-level entity.
- Use switch SW_9 to drive the Run input.
- Use Button0 as an active-low asynchronous reset, Button1 for PClock, and Button2 for MClock.
- Connect the processor bus wires to $LEDG_{8-0}$ and connect the Done signal to $LEDG_9$.
- Indicate the current state on Hex3, i.e. 0 ~ 3.
- Test the functionality of your design by toggling the switches and observing the LEDs. Since the processor's clock input is controlled by a push button switch, it is easy to step through the execution of instructions and observe the behavior of the circuit.



Lab-report:

Submit a lab report on **ilearn** by 11:00pm the day before of next lab. (The lab report must be a **PDF** file.)

Your Lab report should include the following items:

1) VHDL design for Lab14.1

3) Observations and comments.