

Lab 6- Sequential Circuits (I): Using VHDL

The goal of this lab is to design basic sequential circuits using VHDL PROCESS statements.

Lab 6.1:

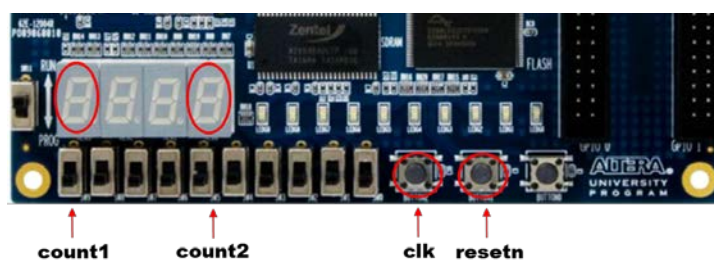
Counters with SIGNAL and VARIABLE

Write a VHDL code that implements a regular 0-to-9 binary counter. A suggested skeleton of the code is presented below. Counter 1 employs a signal, while counter 2 uses a variable.

- Use Button1 as an active-low asynchronous reset, and Button2 as a manual clock input.
- The counts are shown on two 7-segment displays, respectively.
- Does the suggested code implement counters with the same counting range? If not, modify it, and explain the reason in your lab-report.

```
ARCHITECTURE dual_counter OF counter IS
    SIGNAL temp1: INTEGER RANGE 0 TO 10;
BEGIN
    -----counter 1: with signal:-----
    PROCESS(clk)
    BEGIN
        IF (clk'EVENT AND clk='1') THEN
            temp1 <= temp1 + 1;
            IF (temp1=10) THEN
                temp1 <= 0;
            END IF;
        END IF;
        count1 <= temp1;
    END PROCESS;

    -----counter 2: with variable:-----
    PROCESS(clk)
        VARIABLE temp2: INTEGER RANGE 0 TO 10;
    BEGIN
        IF (clk'EVENT AND clk='1') THEN
            temp2 := temp2 + 1;
            IF (temp2=10) THEN
                temp2 := 0;
            END IF;
        END IF;
        count2 <= temp2;
    END PROCESS;
END dual_counter;
```

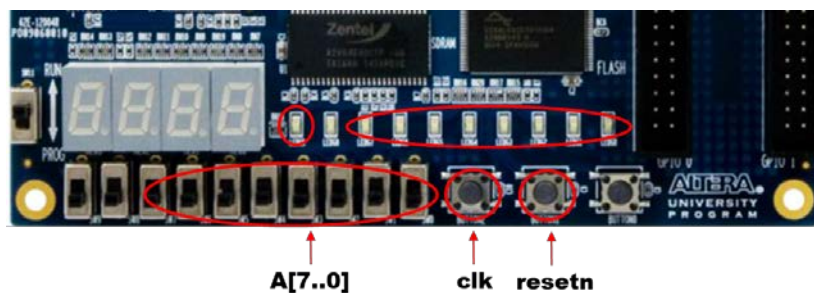
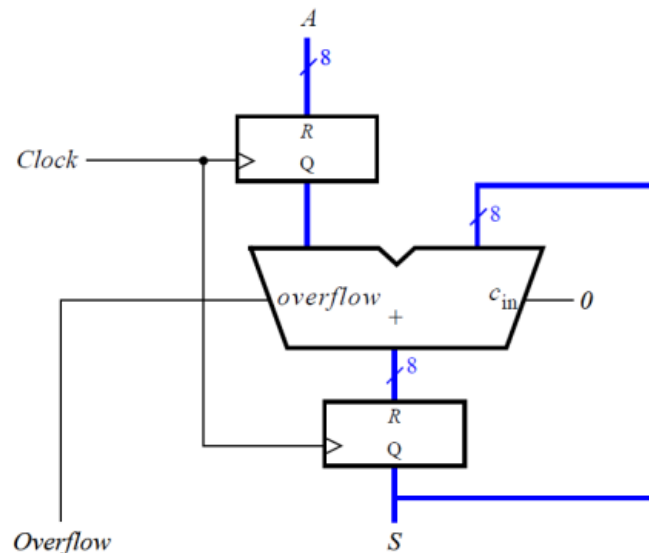


Lab 6.2:

Design a signed 8-bit accumulator:

The block diagram of the signed 8-bit accumulator is seen below.

- Use Button1 as an active-low asynchronous reset, and Button2 as a manual clock input.
- Connect input A to switches SW₇₋₀.
- The sum output **S** would be displayed on green LEDG₇₋₀ lights and the overflow would be displayed on the green LEDG₉ light.



Lab-report:

Submit a lab report on **ilearn** by 11:59pm the day before of next lab. (The lab report must be a **PDF** file.) Your Lab report should include the following items:

- 1) VHDL code and discussion for Lab 6.1.
- 2) VHDL code for Lab 6.2.