MS-7B00 Ver:1.1

CPU:
AMD AM4

System Chipset:
Promontory B350
(Performance gaming)

Main Memory:
DDR IV * 4 MAX:64 GB

VRM
RT8894A 4+2

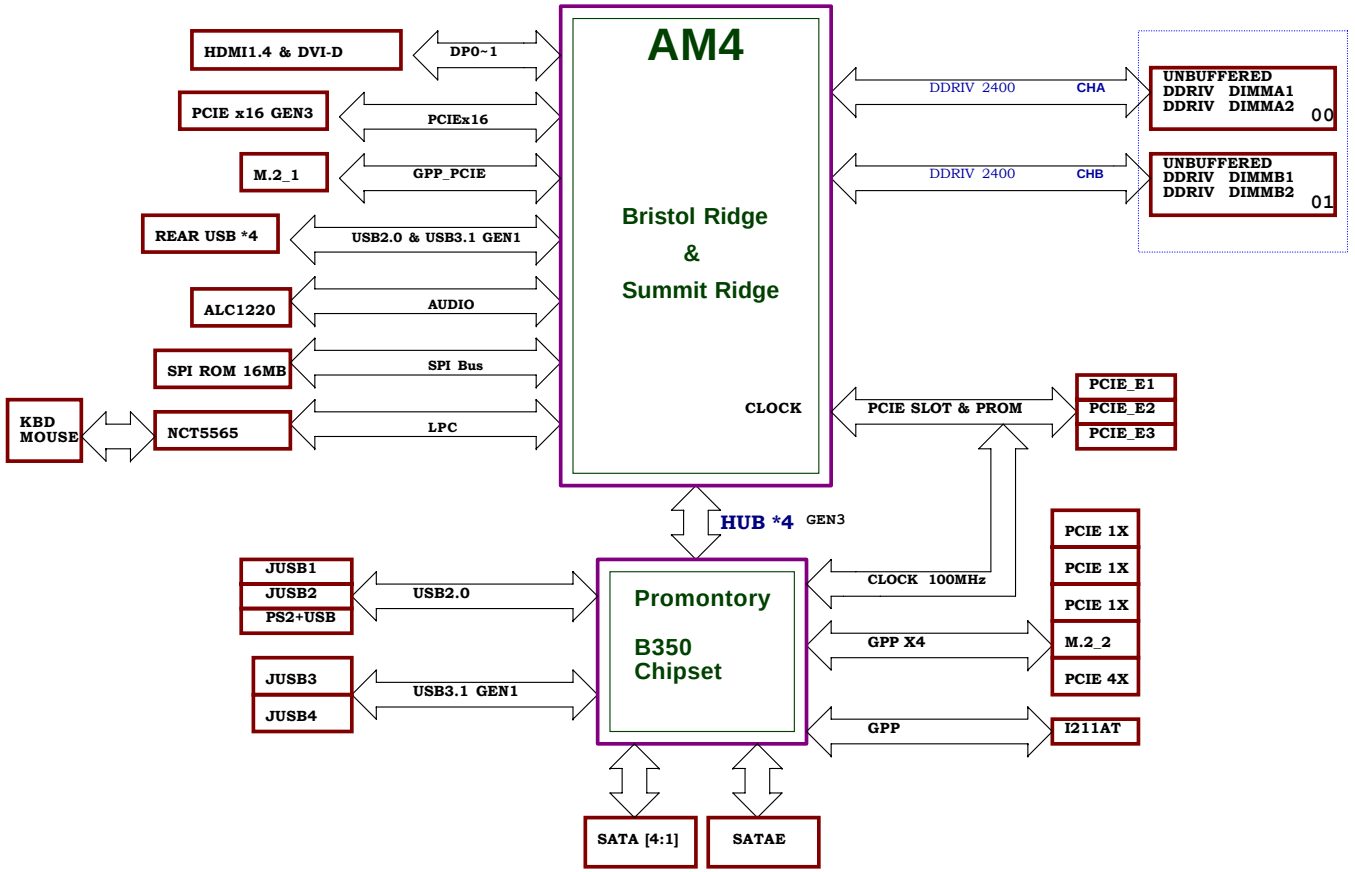
On Board Chipset:
LPC Super I/O --NCT6795D
LAN I211AT
Azalia CODEC - Realtek ALC1220
ASM2142 USB3.1 Gen2
ASM1061 (B350 only)

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X8 Slot * 1

From FCH
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
PCI Express X4 Slot * 1

OCP IC:
UP6273

FUSION BLOCK DIAGRAM



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	MS-7B00	
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AMD AM4

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20 SIO NCT5565	
21 CPU/SYS FAN Control TYPE K	
22 LAN-RTL8111H	
23 / 24 Audio ALC887	
25 USB Rear PS2+USB2.0	
26 USB Rear LAN+USB3.1 GEN1	
27 USB Front Side	
28 SATA Connector	
29 DVI Connector	
30 DP to VGA ITE6516	
31 ACPI uPI-5VDIMM&3VSB	
32 PM-NB681-1.05V/GS7133-2.5V	
33 DDR PWR VPP25/VTT-MP2143	
34 DDR Power-RT8231AGQW	
35 CPU Power 1P8V-MP2147	

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MS-7B00

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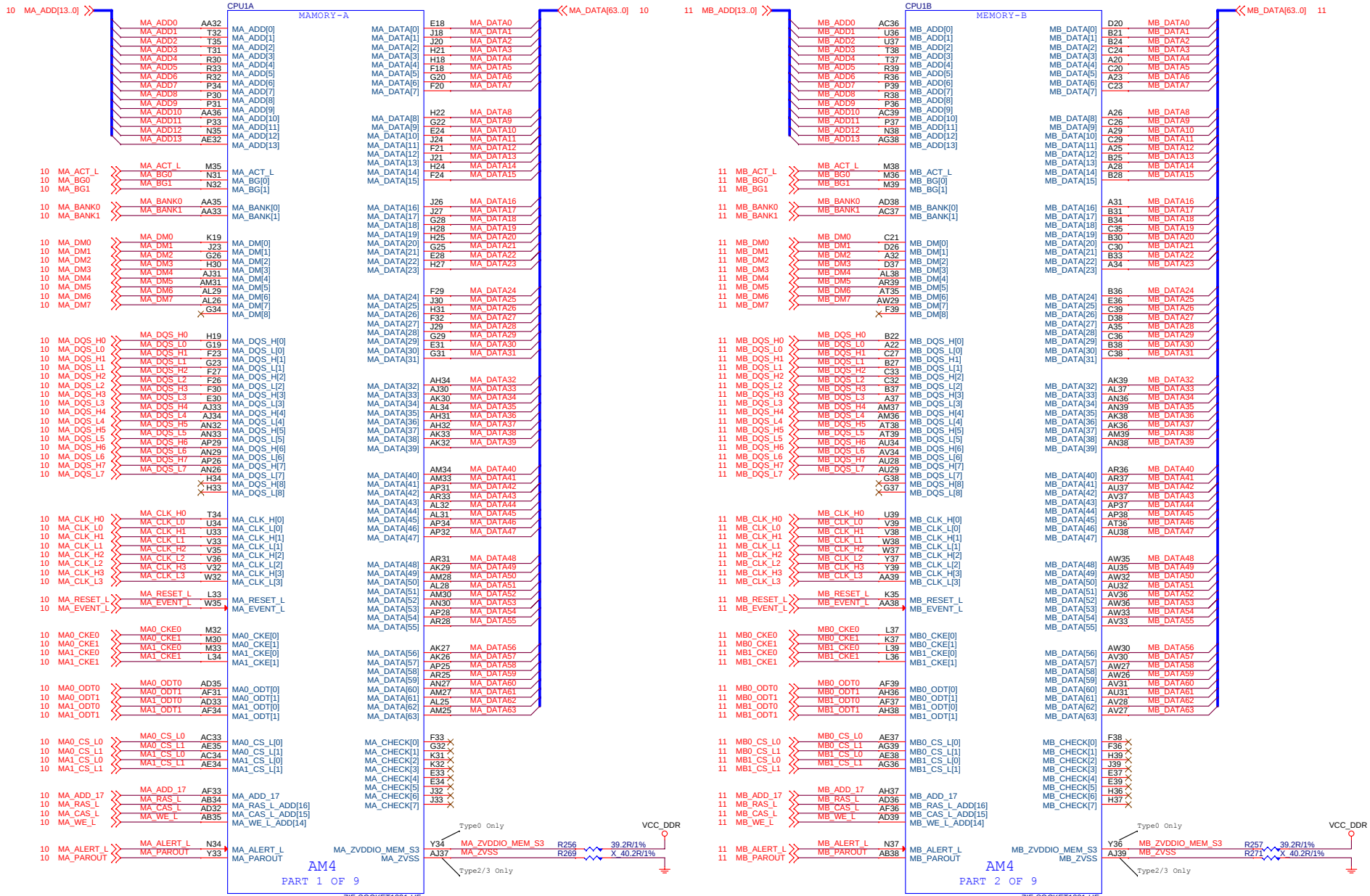

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MS-7B00	
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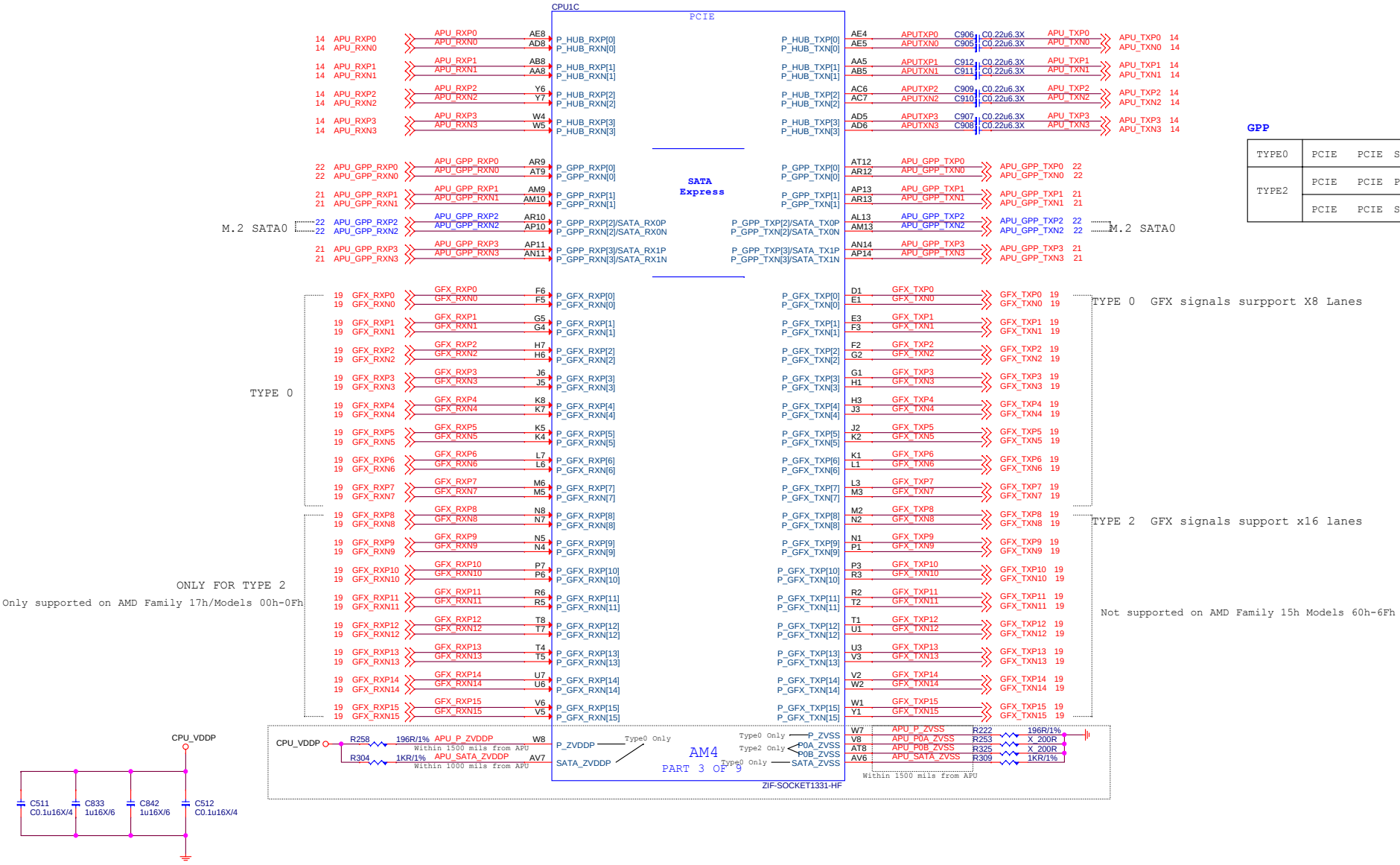

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MS-7B00			
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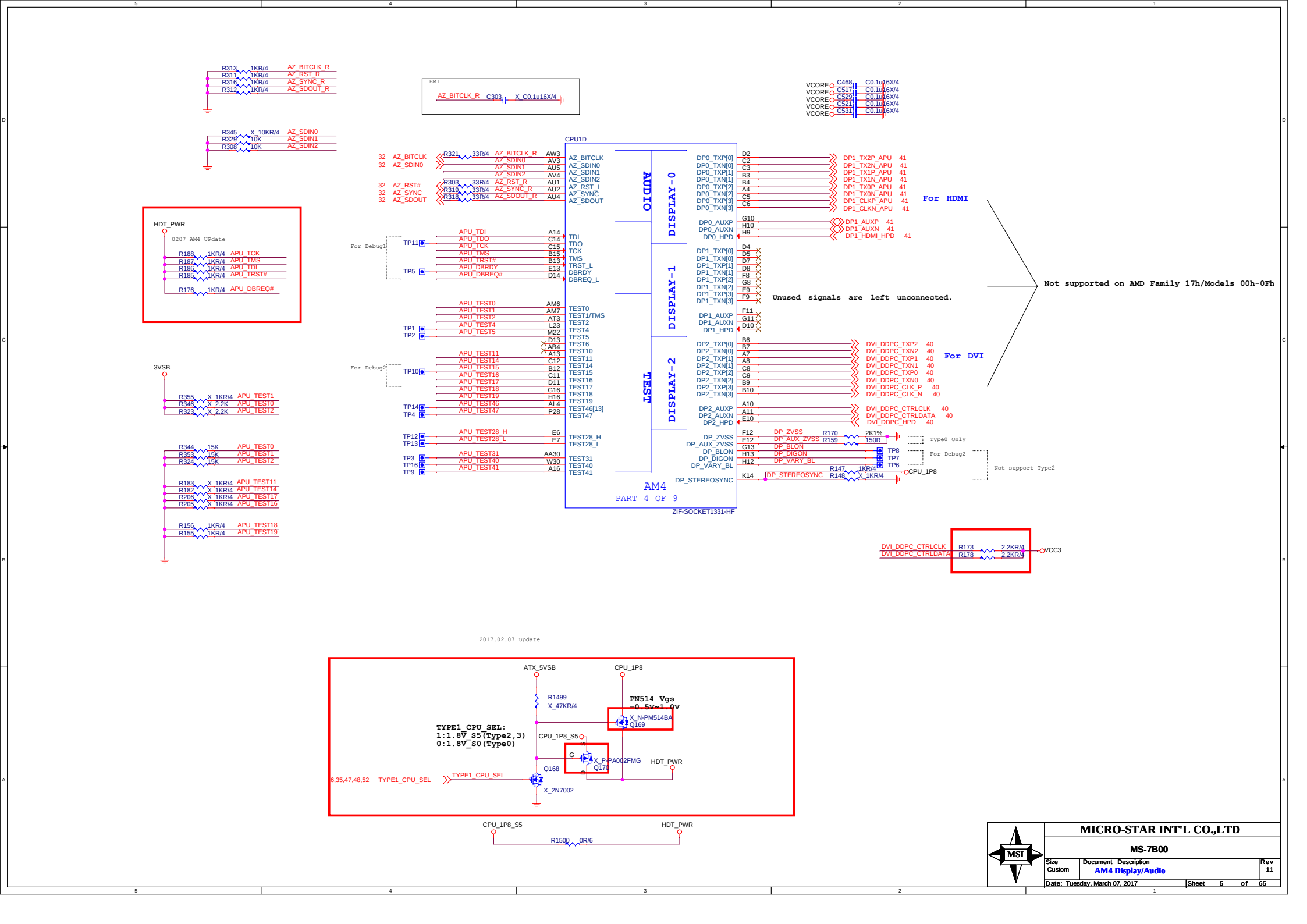
R313 1KR/4 AZ_BITCLK_R
R311 1KR/4 AZ_RST_R
R316 1KR/4 AZ_SYNC_R
R312 1KR/4 AZ_SDOUT_R
R345 X_10KR/4 AZ_SDIN0
R329 10K AZ_SDIN1
R308 10K AZ_SDIN2
EMI
AZ_BITCLK_R C303 X_C0.1u16X/4
VCORE C468 C0.1u16X/4
VCORE C517 C0.1u16X/4
VCORE C529 C0.1u16X/4
VCORE C521 C0.1u16X/4
VCORE C531 C0.1u16X/4
HDT_PWR
0207 AM4 UPdate
R188 1KR/4 APU_TCK
R187 1KR/4 APU_TMS
R186 1KR/4 APU_TDI
R185 1KR/4 APU_TRST#
R176 1KR/4 APU_DBREQ#
3VSB
R355 X_1KR/4 APU_TEST1
R346 X_2.2K APU_TEST0
R323 X_2.2K APU_TEST2
R344 15K APU_TEST0
R353 15K APU_TEST1
R324 15K APU_TEST2
R183 X_1KR/4 APU_TEST11
R182 X_1KR/4 APU_TEST14
R206 X_1KR/4 APU_TEST17
R205 X_1KR/4 APU_TEST16
R156 1KR/4 APU_TEST18
R155 1KR/4 APU_TEST19
CPU1D
AUDIO
DISPLAY-0
DISPLAY-1
DISPLAY-2
TEST
32 AZ_BITCLK
32 AZ_SDIN0
32 AZ_RST#
32 AZ_SYNC
32 AZ_SDOUT
R321 33R/4 AZ_BITCLK_R
AZ_SDIN0
AZ_SDIN1
AZ_SDIN2
R303 33R/4 AZ_RST_R
R319 33R/4 AZ_SYNC_R
R318 33R/4 AZ_SDOUT_R
AZ_BITCLK AW3
AZ_SDIN0 AV3
AZ_SDIN1 AU5
AZ_SDIN2 AV4
AZ_RST_L AU1
AZ_SYNC AU2
AZ_SDOUT AU4
For Debug1
TP11
TP5
APU_TDI A14
APU_TDO C14
APU_TCK C15
APU_TMS B15
APU_TRST# B13
APU_DBRDY E13
APU_DBREQ# D14
TDI
TDO
TCK
TMS
TRST_L
DBRDY
DBREQ_L
TP1
TP2
APU_TEST0 AM6
APU_TEST1 AM7
APU_TEST2 AT3
APU_TEST4 L23
APU_TEST5 M22
D13
AB4
A13
TEST0
TEST1/TMS
TEST2
TEST4
TEST5
TEST6
TEST10
TEST11
TEST14
TEST15
TEST16
TEST17
TEST18
TEST19
For Debug2
TP10
TP14
TP4
APU_TEST11
APU_TEST14
APU_TEST15
APU_TEST16
APU_TEST17
APU_TEST18
APU_TEST19
APU_TEST46 AL4
APU_TEST47 P28
TEST46[13]
TEST47
TP12
TP13
APU_TEST28_H E6
APU_TEST28_L E7
TEST28_H
TEST28_L
TP3
TP16
TP9
APU_TEST31 AA30
APU_TEST40 W30
APU_TEST41 A16
TEST31
TEST40
TEST41
AM4
PART 4 OF 9
ZIF-SOCKET1331-HF
DP0_TXP[0] D2
DP0_TXN[0] C2
DP0_TXP[1] C3
DP0_TXN[1] B3
DP0_TXP[2] B4
DP0_TXN[2] A4
DP0_TXP[3] C5
DP0_TXN[3] C6
DP1_TX2P_APU 41
DP1_TX2N_APU 41
DP1_TX1P_APU 41
DP1_TX1N_APU 41
DP1_TX0P_APU 41
DP1_TX0N_APU 41
DP1_CLKP_APU 41
DP1_CLKN_APU 41
For HDMI
DP0_AUXP G10
DP0_AUXN H10
DP0_HPD H9
DP1_AUXP 41
DP1_AUXN 41
DP1_HDMI_HPD 41
DP1_TXP[0] D4
DP1_TXN[0] D5
DP1_TXP[1] D7
DP1_TXN[1] D8
DP1_TXP[2] F8
DP1_TXN[2] G8
DP1_TXP[3] E9
DP1_TXN[3] F9
Unused signals are left unconnected.
DP1_AUXP F11
DP1_AUXN G11
DP1_HPD D10
Not supported on AMD Family 17h/Models 00h-0Fh
DP2_TXP[0] B6
DP2_TXN[0] B7
DP2_TXP[1] A7
DP2_TXN[1] A8
DP2_TXP[2] C8
DP2_TXN[2] C9
DP2_TXP[3] B9
DP2_TXN[3] B10
DVI_DDPC_TXP2 40
DVI_DDPC_TXN2 40
DVI_DDPC_TXP1 40
DVI_DDPC_TXN1 40
DVI_DDPC_TXP0 40
DVI_DDPC_TXN0 40
DVI_DDPC_CLK_P 40
DVI_DDPC_CLK_N 40
For DVI
DP2_AUXP A10
DP2_AUXN A11
DP2_HPD E10
DVI_DDPC_CTRLCLK 40
DVI_DDPC_CTRLDATA 40
DVI_DDPC_HPD 40
DP_ZVSS F12
DP_AUX_ZVSS E12
DP_BLON G13
DP_DIGON H13
DP_VARY_BL H12
DP_STEREOSYNC K14
R170 2K1%
R159 150R
Type0 Only
TP8
TP7
TP6
For Debug2
Not support Type2
R147 1KR/4
R148 X_1KR/4
CPU_1P8
DVI_DDPC_CTRLCLK R173 2.2KR/4
DVI_DDPC_CTRLDATA R178 2.2KR/4
VCC3
2017.02.07 update
ATX_5VSB
CPU_1P8
R1499 X_47KR/4
PN514 Vgs =0.5V~1.0V
X_N-PM514BA
Q169
TYPE1_CPU_SEL:
1:1.8V_S5(Type2,3)
0:1.8V_S0(Type0)
CPU_1P8_S5
G
X_P-PA002FMG
Q170
HDT_PWR
6,35,47,48,52 TYPE1_CPU_SEL
TYPE1_CPU_SEL
Q168
X_2N7002
CPU_1P8_S5
HDT_PWR
R1500 0R/6
MSI
MICRO-STAR INT'L CO.,LTD
MS-7B00
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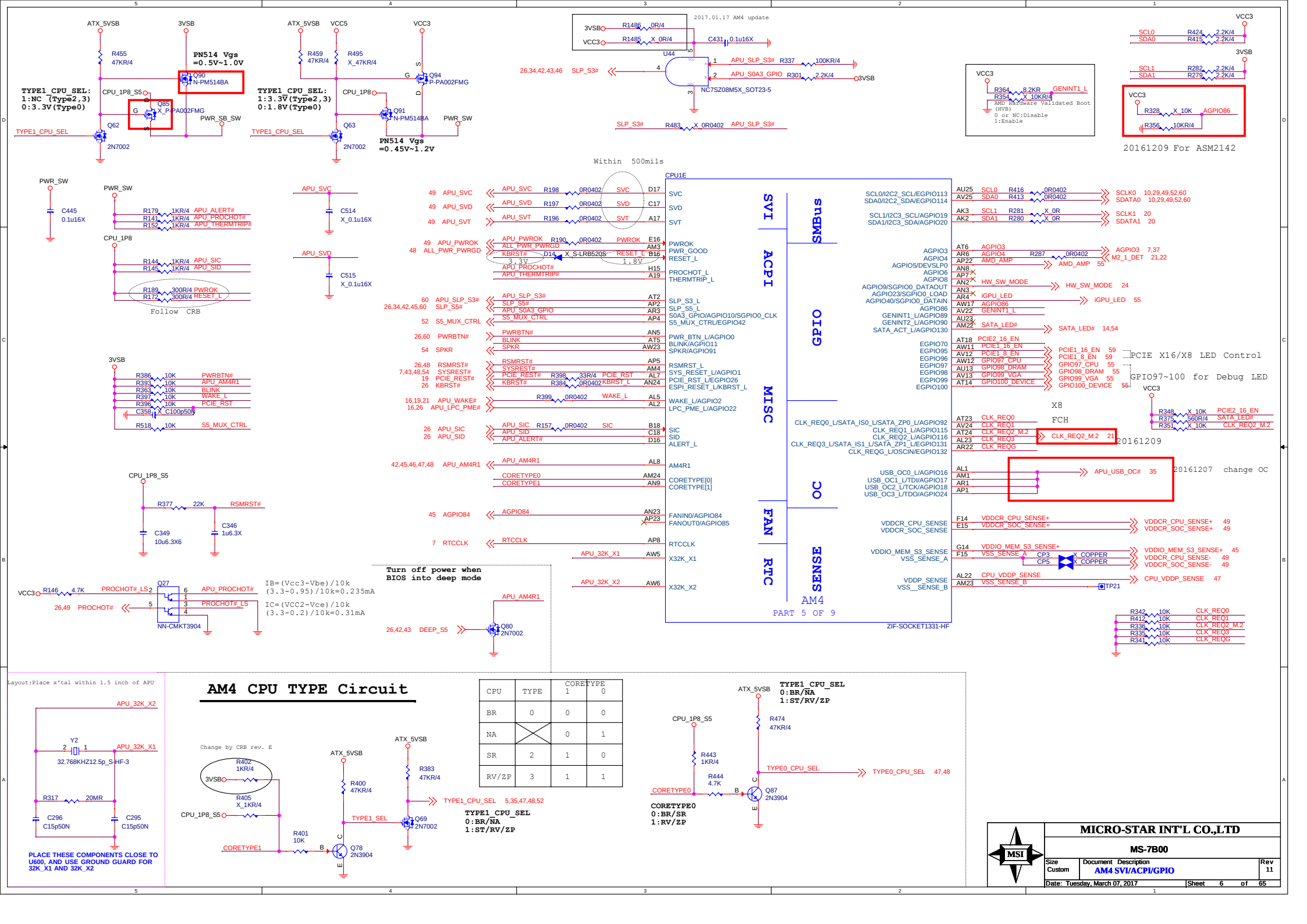
ATX_5VSB
3VSB
R455 47KR/4
PN514 Vgs =0.5V~1.0V
Q90 N-PM514BA
TYPE1_CPU_SEL: 1:NC (Type2,3) 0:3.3V(Type0)
CPU_1P8_S5
Q85 X_P-PA002FMG
PWR_SB_SW
TYPE1_CPU_SEL
Q62 2N7002
ATX_5VSB
VCC5
VCC3
R459 47KR/4
R495 X_47KR/4
Q94 P-PA002FMG
TYPE1_CPU_SEL: 1:3.3V(Type2,3) 0:1.8V(Type0)
CPU_1P8
Q91 N-PM514BA
PWR_SW
TYPE1_CPU_SEL
Q63 2N7002
PN514 Vgs =0.45V~1.2V
2017.01.17 AM4 update
3VSB
R1486 0R/4
VCC3
R1485 X_0R/4
C431 0.1u16X
U44
26,34,42,43,46 SLP_S3#
APU_SLP_S3# R337 100KR/4
APU_S0A3_GPIO R301 2.2K/4
3VSB
NC7SZ08M5X_SOT23-5
SLP_S3# R483 X_0R0402 APU_SLP_S3#
VCC3
R364 8.2KR GENINT1_L
R354 X_10KR/4
AMD Hardware Validated Boot (HVB)
0 or NC:Disable
1:Enable
SCL0 R424 2.2K/4
SDA0 R415 2.2K/4
3VSB
SCL1 R282 2.2K/4
SDA1 R279 2.2K/4
VCC3
R328 X_10K AGPIO86
R356 10KR/4
20161209 For ASM2142
Within 500mils
PWR_SW
C445 0.1u16X
PWR_SW
R179 1KR/4 APU_ALERT#
R141 1KR/4 APU_PROCHOT#
R152 1KR/4 APU_THERMTRIP#
CPU_1P8
R144 1KR/4 APU_SIC
R145 1KR/4 APU_SID
R189 300R/4 PWROK
R172 300R/4 RESET_L
Follow CRB
APU_SVC
C514 X_0.1u16X
APU_SVD
C515 X_0.1u16X
CPU1E
49 APU_SVC
APU_SVC R198 0R0402 SVC
D17 SVC
49 APU_SVD
APU_SVD R197 0R0402 SVD
C17 SVD
49 APU_SVT
APU_SVT R196 0R0402 SVT
A17 SVT
SVI
49 APU_PWROK
ALL_PWR_PWRGD
48 ALL_PWR_PWRGD
APU_PWROK R190 0R0402 PWROK
E16 PWROK
AM3 PWR_GOOD
KBRST# D14 X_S-LRB520S RESET_L B16
3.3V 1.8V
APU_PROCHOT# H15
APU_THERMTRIP# A19
PROCHOT_L
THERMTRIP_L
ACPI
60 APU_SLP_S3#
26,34,42,45,60 SLP_S5#
APU_SLP_S3# AT2
SLP_S5# AP2
APU_S0A3_GPIO AR3
S5_MUX_CTRL AP4
SLP_S3_L
SLP_S5_L
S0A3_GPIO/AGPIO10/SGPIO0_CLK
S5_MUX_CTRL/EGPIO42
52 S5_MUX_CTRL
26,60 PWRBTN#
BLINK AT5
54 SPKR
SPKR AW23
PWR_BTN_L/AGPIO0
BLINK/AGPIO11
SPKR/AGPIO91
GPIO
3VSB
R386 10K PWRBTN#
R393 10K APU_AM4R1
R363 10K BLINK
R397 10K WAKE_L
R396 10K PCIE_RST
C358 X_C100p50N
R518 10K S5_MUX_CTRL
26,48 RSMRST#
7,43,48,54 SYSRST#
19 PCIE_RST#
26 KBRST#
RSMRST# AP5
SYSRST# AM4
PCIE_RST# R398 33R/4 PCIE_RST AL7
KBRST# R384 0R0402 KBRST_L AN24
RSMRST_L
SYS_RESET_L/AGPIO1
PCIE_RST_L/EGPIO26
ESPI_RESET_L/KBRST_L
16,19,21 APU_WAKE#
16,26 APU_LPC_PME#
R399 0R0402 WAKE_L AL5
AL2
WAKE_L/AGPIO2
LPC_PME_L/AGPIO22
MISC
26 APU_SIC
26 APU_SID
APU_SIC R157 0R0402 SIC
APU_SID B18
APU_ALERT# C18
D16
SIC
SID
ALERT_L
CPU_1P8_S5
R377 22K RSMRST#
C349 10u6.3X6
C346 1u6.3X
42,45,46,47,48 APU_AM4R1
APU_AM4R1 AL8
AM4R1
CORETYPE0 AM24
CORETYPE1 AN9
CORETYPE[0]
CORETYPE[1]
45 AGPIO84
AGPIO84 AN23
AP23
FANIN0/AGPIO84
FANOUT0/AGPIO85
FAN
7 RTCCLK
RTCCLK AP8
RTCCLK
APU_32K_X1 AW5
X32K_X1
APU_32K_X2 AW6
X32K_X2
RTC
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92
CLK_REQ1_L/AGPIO115
CLK_REQ2_L/AGPIO116
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131
CLK_REQG_L/OSCIN/EGPIO132
USB_OC0_L/AGPIO16
USB_OC1_L/TDI/AGPIO17
USB_OC2_L/TCK/AGPIO18
USB_OC3_L/TDO/AGPIO24
OC
VDDCR_CPU_SENSE
VDDCR_SOC_SENSE
VDDIO_MEM_S3_SENSE
VSS_SENSE_A
VDDP_SENSE
VSS_SENSE_B
SENSE
AM4
PART 5 OF 9
ZIF-SOCKET1331-HF
SMBus
GPIO
SCL0/I2C2_SCL/EGPIO113
SDA0/I2C2_SDA/EGPIO114
SCL1/I2C3_SCL/AGPIO19
SDA1/I2C3_SDA/AGPIO20
AGPIO3
AGPIO4
AGPIO5/DEVSLP0
AGPIO6
AGPIO8
AGPIO9/SGPIO0_DATAOUT
AGPIO23/SGPIO0_LOAD
AGPIO40/SGPIO0_DATAIN
AGPIO86
GENINT1_L/AGPIO89
GENINT2_L/AGPIO90
SATA_ACT_L/AGPIO130
EGPIO70
EGPIO95
EGPIO96
EGPIO97
EGPIO98
EGPIO99
EGPIO100
AU25 SCL0 R416 0R0402 SCLK0 10,29,49,52,60
AV25 SDA0 R413 0R0402 SDATA0 10,29,49,52,60
AK3 SCL1 R281 X_0R SCLK1 20
AK2 SDA1 R280 X_0R SDATA1 20
AT6 AGPIO3
AR6 AGPIO4 R287 0R0402 AGPIO3 7,37
AP22 AMD_AMP AMD_AMP 55
M2_1_DET 21,22
AN8
AP7
AN2 HW_SW_MODE HW_SW_MODE 24
AN3
AR4 iGPU_LED iGPU_LED 55
AW17 AGPIO86
AV22 GENINT1_L
AU23
AM22 SATA_LED# SATA_LED# 14,54
AT18 PCIE2_16_EN
AW11 PCIE1_16_EN PCIE1_16_EN 59
AV12 PCIE1_8_EN PCIE1_8_EN 59
AW12 GPIO97_CPU GPIO97_CPU 55
AU13 GPIO98_DRAM GPIO98_DRAM 55
AV13 GPIO99_VGA GPIO99_VGA 55
AT14 GPIO100_DEVICE GPIO100_DEVICE 55
PCIE X16/X8 LED Control
GPIO97~100 for Debug LED
X8
FCH
AT23 CLK_REQ0
AV24 CLK_REQ1
AT24 CLK_REQ2_M.2
AL23 CLK_REQ3
AR22 CLK_REQG
CLK_REQ2_M.2 21
20161209
VCC3
R348 X_10K PCIE2_16_EN
R375 560R/4 SATA_LED#
R351 X_10K CLK_REQ2_M.2
AL1
AM1
AR1
AP1
APU_USB_OC# 35
20161207 change OC
F14 VDDCR_CPU_SENSE+
E15 VDDCR_SOC_SENSE+
VDDCR_CPU_SENSE+ 49
VDDCR_SOC_SENSE+ 49
G14 VDDIO_MEM_S3_SENSE+
F15 VSS_SENSE_A
CP3 X_COPPER
CP5 X_COPPER
VDDIO_MEM_S3_SENSE+ 45
VDDCR_CPU_SENSE- 49
VDDCR_SOC_SENSE- 49
AL22 CPU_VDDP_SENSE
AM23 VSS_SENSE_B
TP21
CPU_VDDP_SENSE 47
R342 10K CLK_REQ0
R412 10K CLK_REQ1
R336 10K CLK_REQ2_M.2
R335 10K CLK_REQ3
R341 10K CLK_REQG
VCC3
R146 4.7K PROCHOT#_LS
Q27 NN-CMKT3904
APU_PROCHOT#
26,49 PROCHOT#
PROCHOT#_LS
IB=(Vcc3-Vbe)/10k (3.3-0.95)/10k=0.235mA
IC=(VCC2-Vce)/10k (3.3-0.2)/10k=0.31mA
Turn off power when BIOS into deep mode
APU_AM4R1
26,42,43 DEEP_S5
Q80 2N7002
Layout:Place x'tal within 1.5 inch of APU
APU_32K_X2
Y2
32.768KHZ12.5p_S-HF-3
APU_32K_X1
R317 20MR
C296 C15p50N
C295 C15p50N
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
AM4 CPU TYPE Circuit
Change by CRB rev. E
3VSB
R402 1KR/4
R405 X_1KR/4
CPU_1P8_S5
CORETYPE1
R401 10K
Q78 2N3904
ATX_5VSB
R400 47KR/4
TYPE1_SEL
Q69 2N7002
ATX_5VSB
R383 47KR/4
TYPE1_CPU_SEL 5,35,47,48,52
TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP
CPU TYPE CORETYPE 1 0
BR 0 0 0
NA X 0 1
SR 2 1 0
RV/ZP 3 1 1
ATX_5VSB
TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP
CPU_1P8_S5
R474 47KR/4
R443 1KR/4
R444 4.7K
CORETYPE0
Q87 2N3904
TYPE0_CPU_SEL
TYPE0_CPU_SEL 47,48
CORETYPE0
0:BR/SR
1:RV/ZP
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Size Custom
Document Description AM4 SVI/ACPI/GPIO
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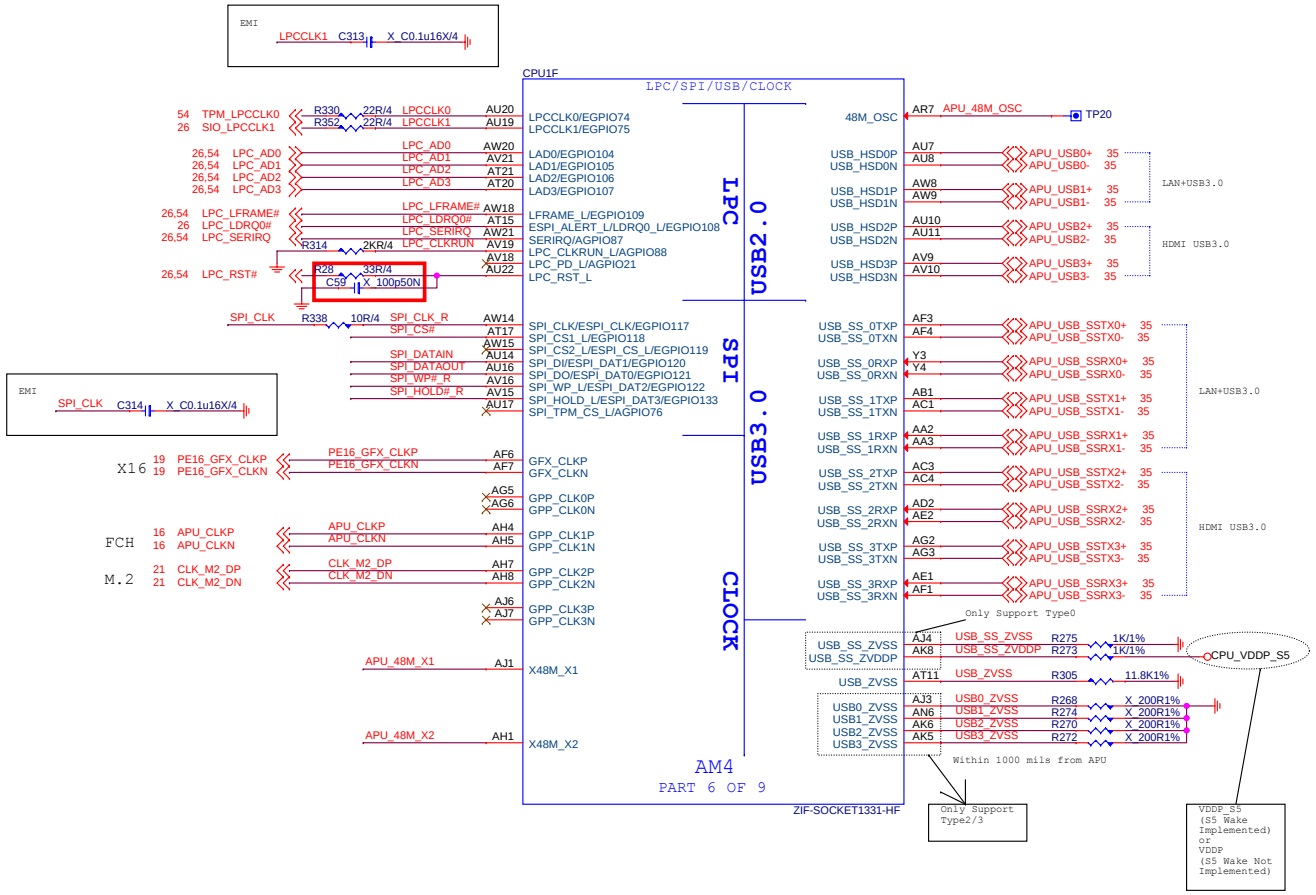
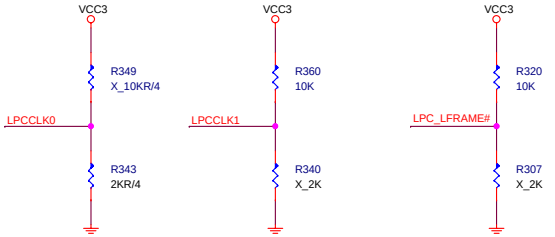
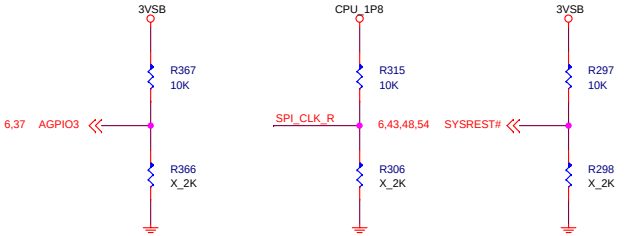


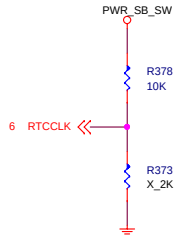
Strapping Options



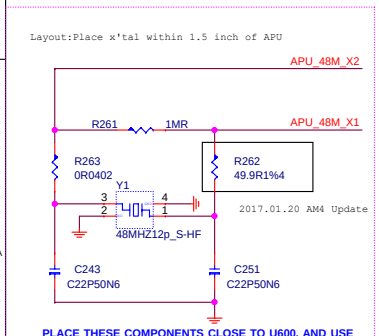
	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM



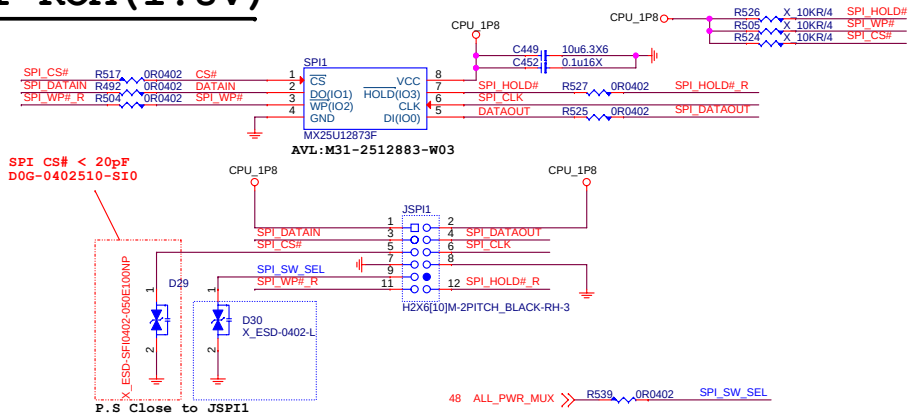
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board



SPI ROM(1.8V)



MICRO-STAR INT'L CO.,LTD	
MS-7B00	
Size: Custom	Document Description: AM4 LPC/SPI/USB/CLK/STRAP
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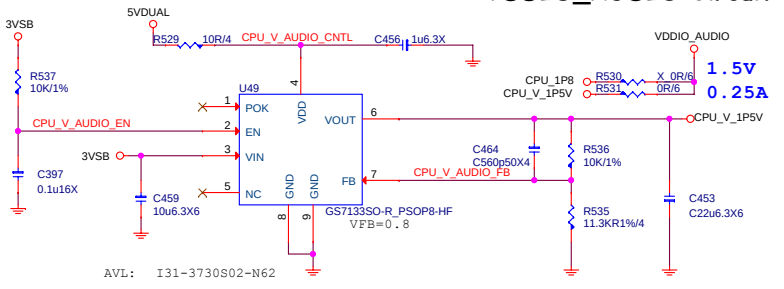
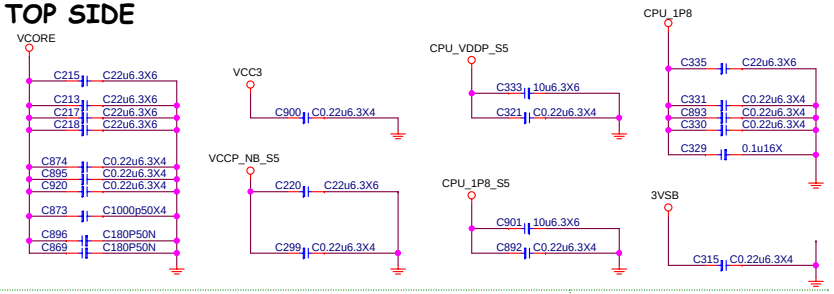
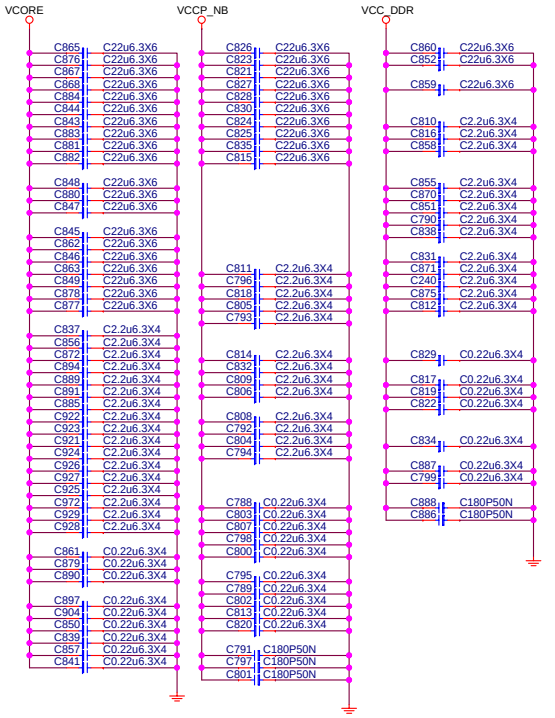
VDDIO_AUDIO Circuit



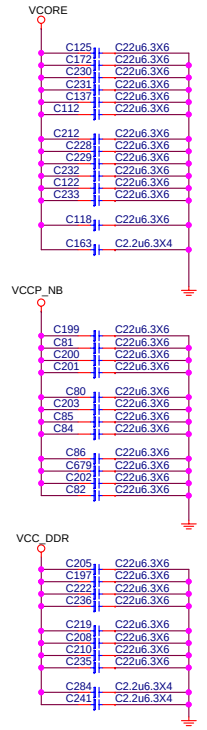
TOP SIDE

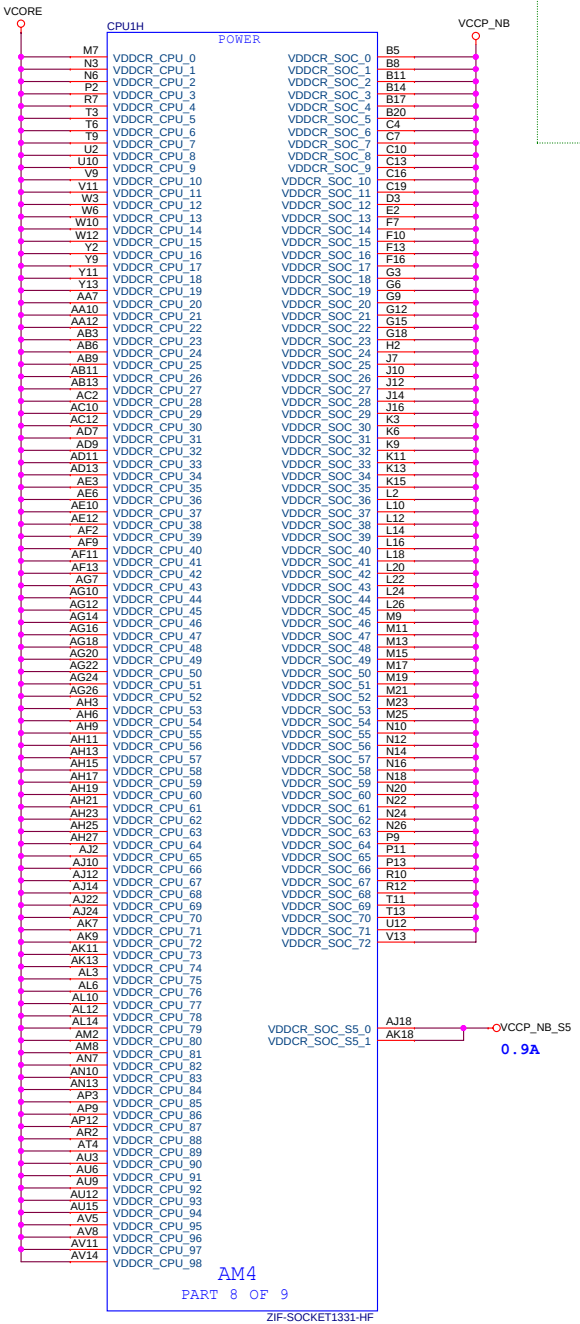


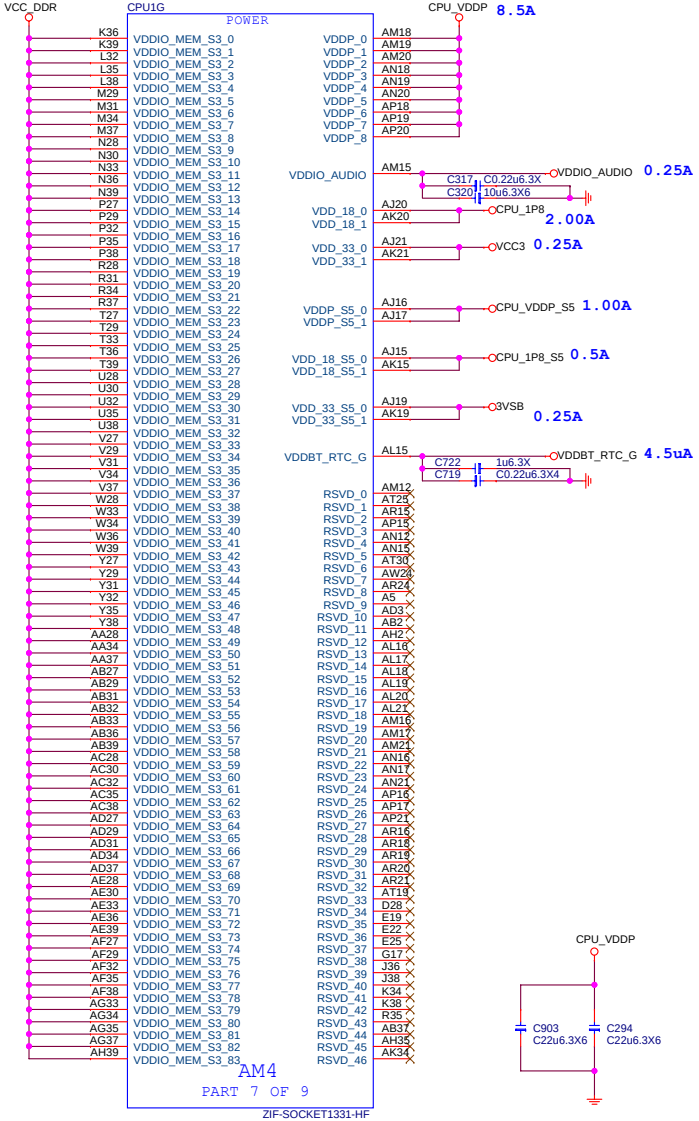
BOTTOM SIDE



TOP CAVITY







MICRO-STAR INT'L CO.,LTD	
MS-7B00	
Size: Custom	Document Description: AM4 Power/RTC Power
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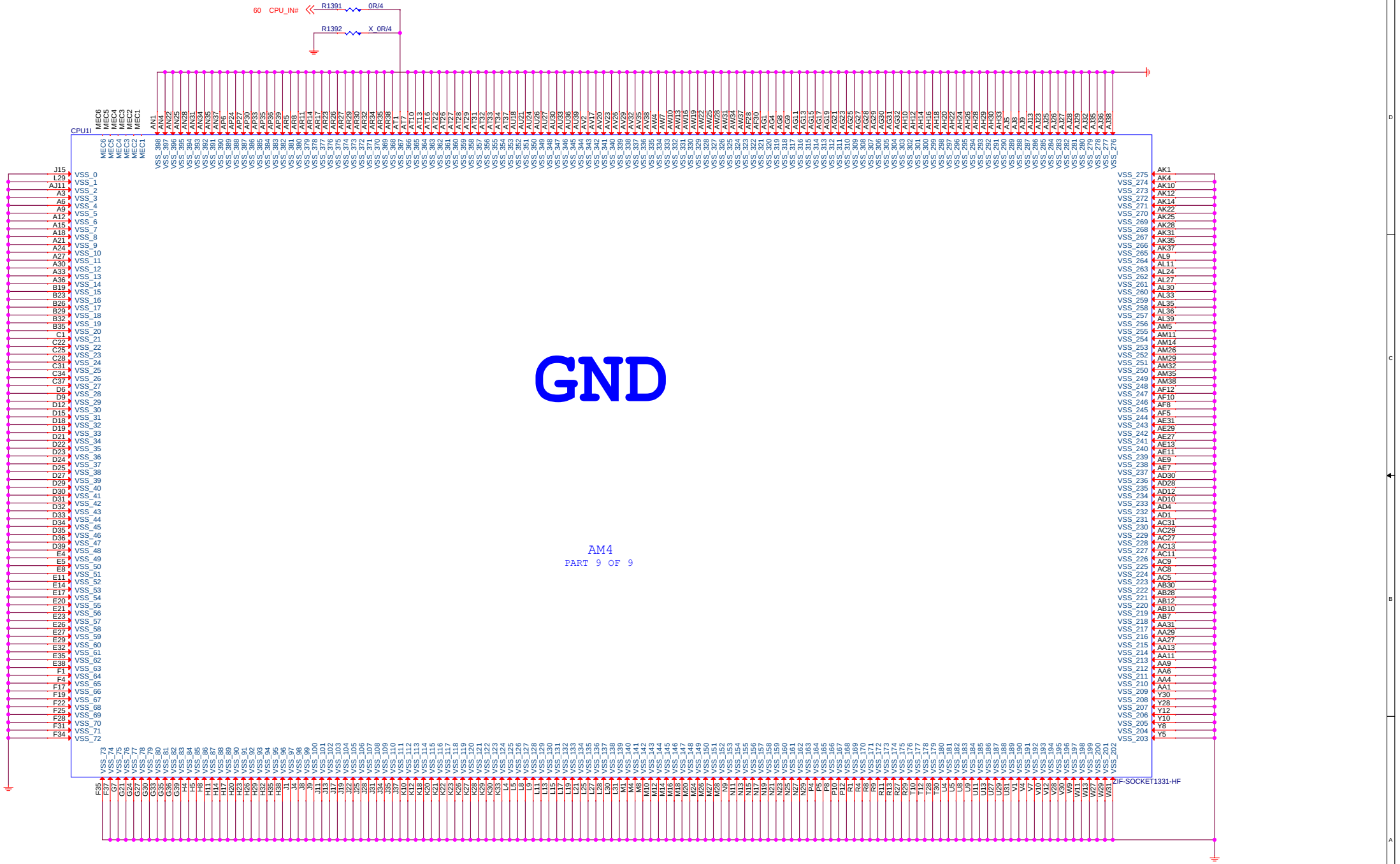

MICRO-STAR INT'L CO.,LTD		
MS-7B00		
Size: Custom	Document Description: AM4 GND	Rev: 11
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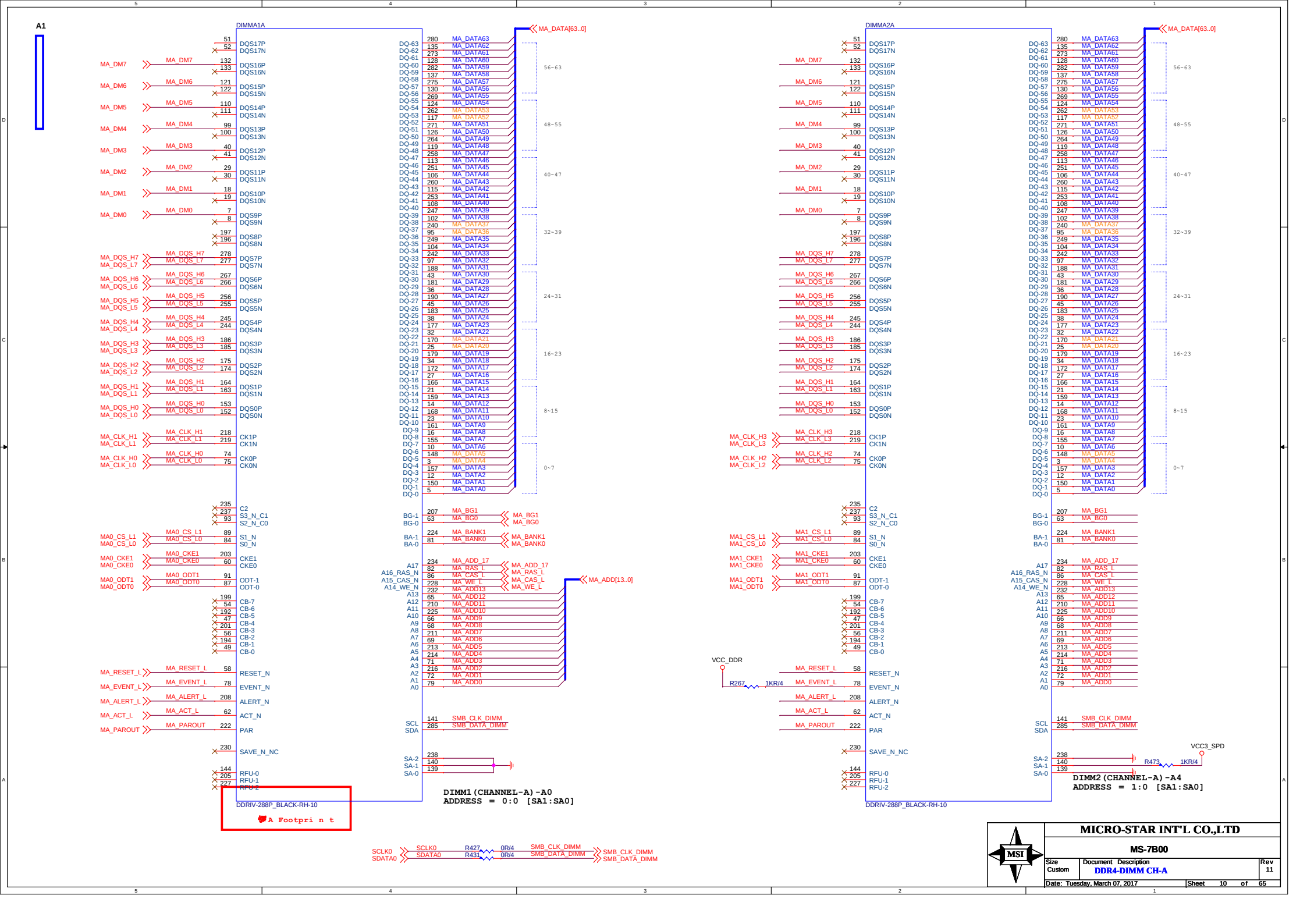
A1
DIMMA1A
DDRIV-288P_BLACK-RH-10
DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]
DIMMA2A
DDRIV-288P_BLACK-RH-10
DIMM2(CHANNEL-A)-A4
ADDRESS = 1:0 [SA1:SA0]
MA_DATA[63..0]
MA_ADD[13..0]
VCC_DDR
R267 1KR/4
VCC3_SPD
R473 1KR/4
SCLK0
SDATA0
R427 0R/4
R431 0R/4
SMB_CLK_DIMM
SMB_DATA_DIMM
MICRO-STAR INT'L CO.,LTD
MS-7B00
Size Custom
Document Description DDR4-DIMM CH-A
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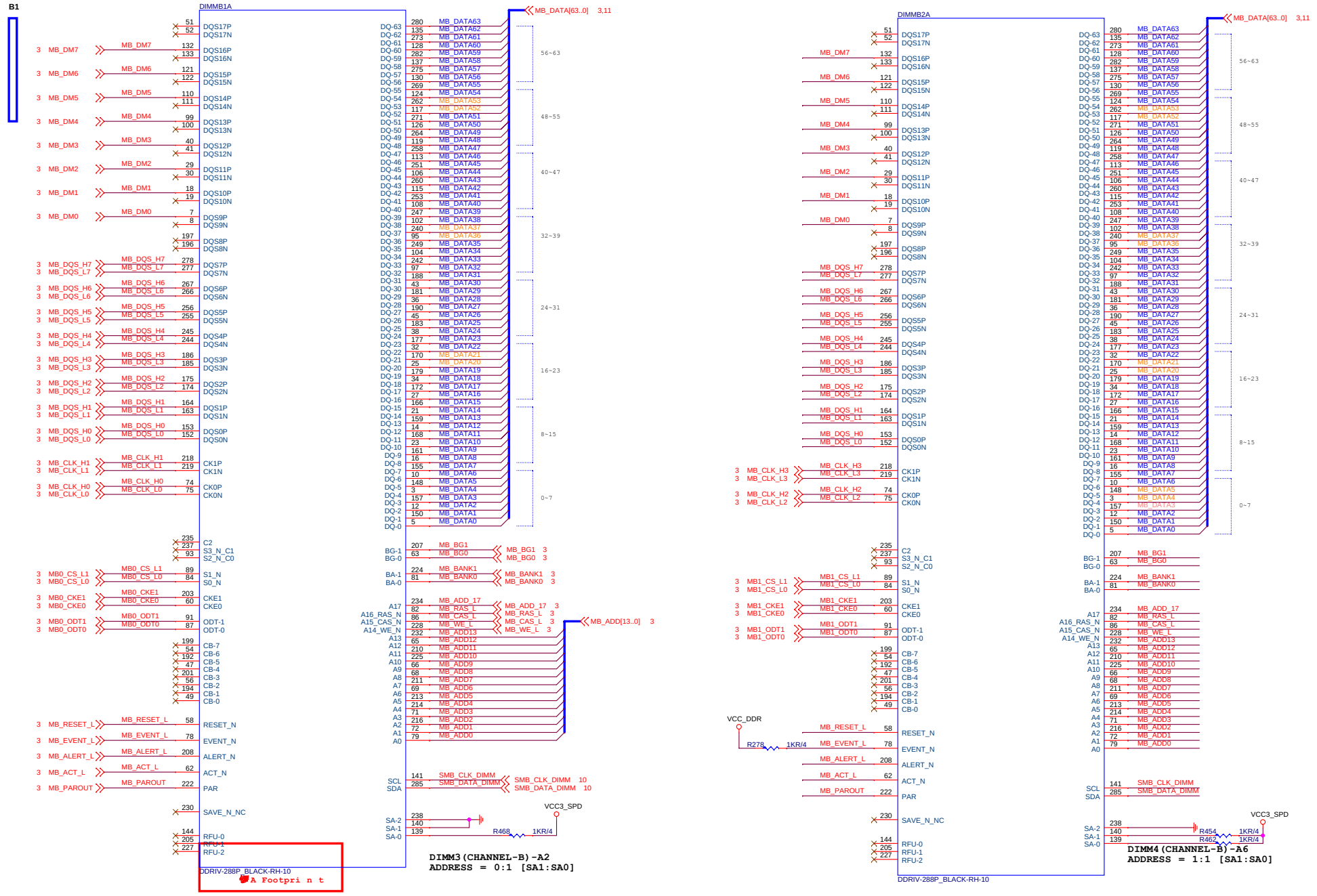
B1
DIMMB1A
MB_DATA[63..0] 3,11
MB_DM7
MB_DM6
MB_DM5
MB_DM4
MB_DM3
MB_DM2
MB_DM1
MB_DM0
MB_DQS_H7
MB_DQS_L7
MB_DQS_H6
MB_DQS_L6
MB_DQS_H5
MB_DQS_L5
MB_DQS_H4
MB_DQS_L4
MB_DQS_H3
MB_DQS_L3
MB_DQS_H2
MB_DQS_L2
MB_DQS_H1
MB_DQS_L1
MB_DQS_H0
MB_DQS_L0
MB_CLK_H1
MB_CLK_L1
MB_CLK_H0
MB_CLK_L0
MB0_CS_L1
MB0_CS_L0
MB0_CKE1
MB0_CKE0
MB0_ODT1
MB0_ODT0
MB_RESET_L
MB_EVENT_L
MB_ALERT_L
MB_ACT_L
MB_PAROUT
MB_BG1
MB_BG0
MB_BANK1
MB_BANK0
MB_ADD_17
MB_RAS_L
MB_CAS_L
MB_WE_L
MB_ADD[13..0] 3
SMB_CLK_DIMM
SMB_DATA_DIMM
SMB_CLK_DIMM 10
SMB_DATA_DIMM 10
VCC3_SPD
R468 1KR/4
DDRIV-288P_BLACK-RH-10
A Footpri n t
DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]
DIMMB2A
VCC_DDR
R278 1KR/4
DDRIV-288P_BLACK-RH-10
R454 1KR/4
R462 1KR/4
DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]
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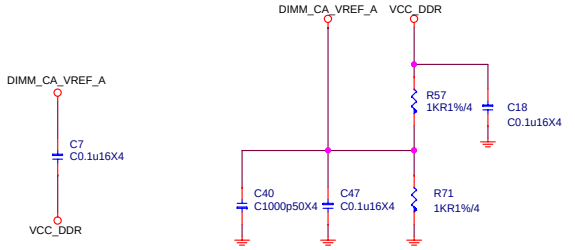
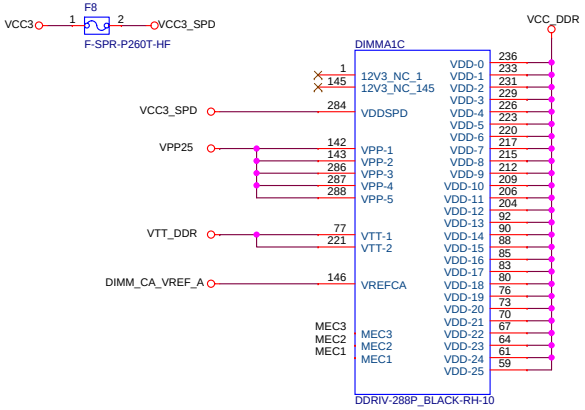
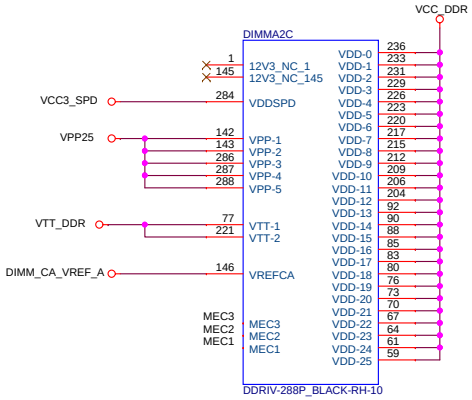
DDR VREF

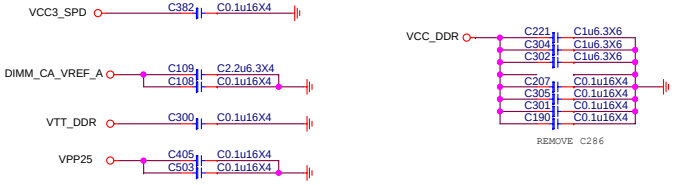
(place resistors close to DIMMs)

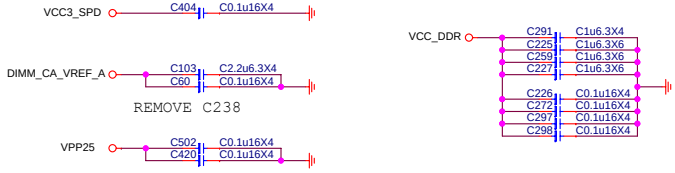


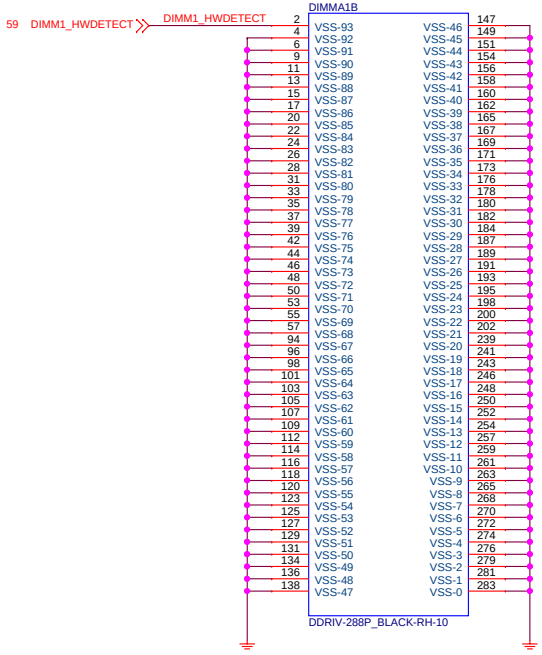
DIMM SLOT PN BY SPEC

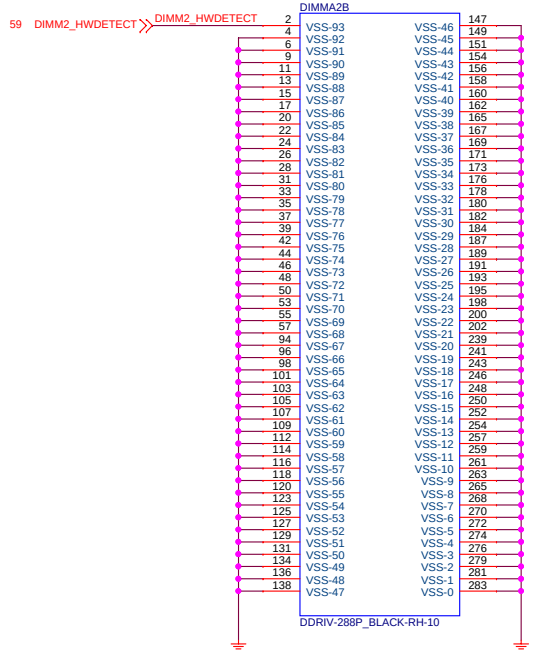












MICRO-STAR INT'L CO.,LTD	
MS-7B00	
Size: Custom	Document Description: DDR4-POWER/GND-1
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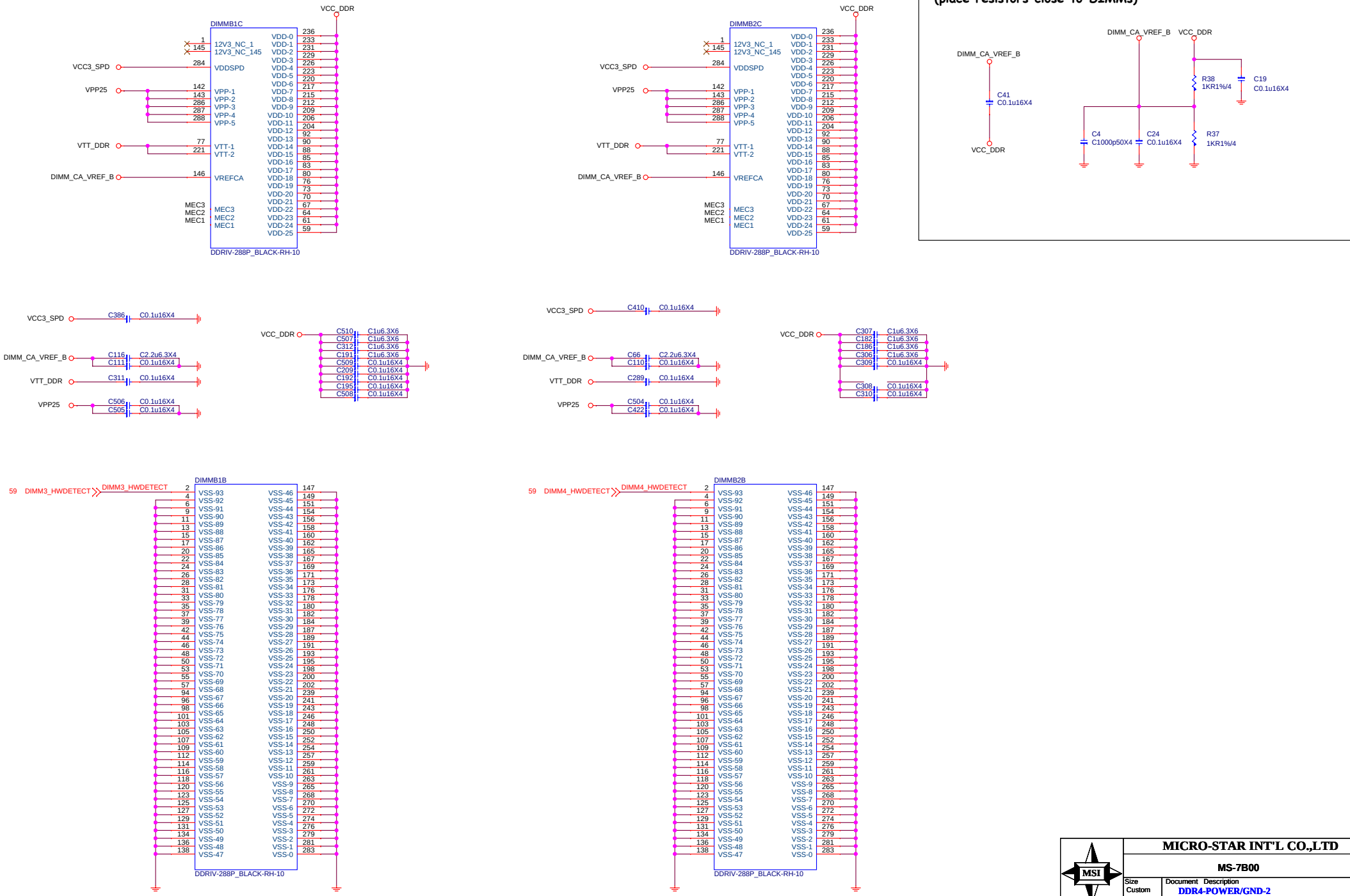
DDR VREF
(place resistors close to DIMMs)
DIMM_CA_VREF_B
C41
C0.1u16X4
VCC_DDR
DIMM_CA_VREF_B
VCC_DDR
R38
1KR1%/4
C19
C0.1u16X4
C4
C1000p50X4
C24
C0.1u16X4
R37
1KR1%/4
DIMMB1C
DIMMB2C
VCC_DDR
VCC3_SPD
VPP25
VTT_DDR
DIMM_CA_VREF_B
MEC3
MEC2
MEC1
12V3_NC_1
12V3_NC_145
VDDSPD
VPP-1
VPP-2
VPP-3
VPP-4
VPP-5
VTT-1
VTT-2
VREFCA
VDD-0
VDD-1
VDD-2
VDD-3
VDD-4
VDD-5
VDD-6
VDD-7
VDD-8
VDD-9
VDD-10
VDD-11
VDD-12
VDD-13
VDD-14
VDD-15
VDD-16
VDD-17
VDD-18
VDD-19
VDD-20
VDD-21
VDD-22
VDD-23
VDD-24
VDD-25
DDRIV-288P_BLACK-RH-10
VCC3_SPD
C386
C0.1u16X4
DIMM_CA_VREF_B
C116
C2.2u6.3X4
C111
C0.1u16X4
VTT_DDR
C311
C0.1u16X4
VPP25
C506
C505
C0.1u16X4
VCC_DDR
C510
C507
C312
C191
C509
C209
C192
C195
C508
C1u6.3X6
C0.1u16X4
VCC3_SPD
C410
C0.1u16X4
DIMM_CA_VREF_B
C66
C110
C2.2u6.3X4
C0.1u16X4
VTT_DDR
C289
C0.1u16X4
VPP25
C504
C422
C0.1u16X4
VCC_DDR
C307
C182
C186
C306
C309
C308
C310
C1u6.3X6
C0.1u16X4
59
DIMM3_HWDETECT
DIMMB1B
DDRIV-288P_BLACK-RH-10
59
DIMM4_HWDETECT
DIMMB2B
DDRIV-288P_BLACK-RH-10
MICRO-STAR INT'L CO.,LTD
MS-7B00
Size
Custom
Document Description
DDR4-POWER/GND-2
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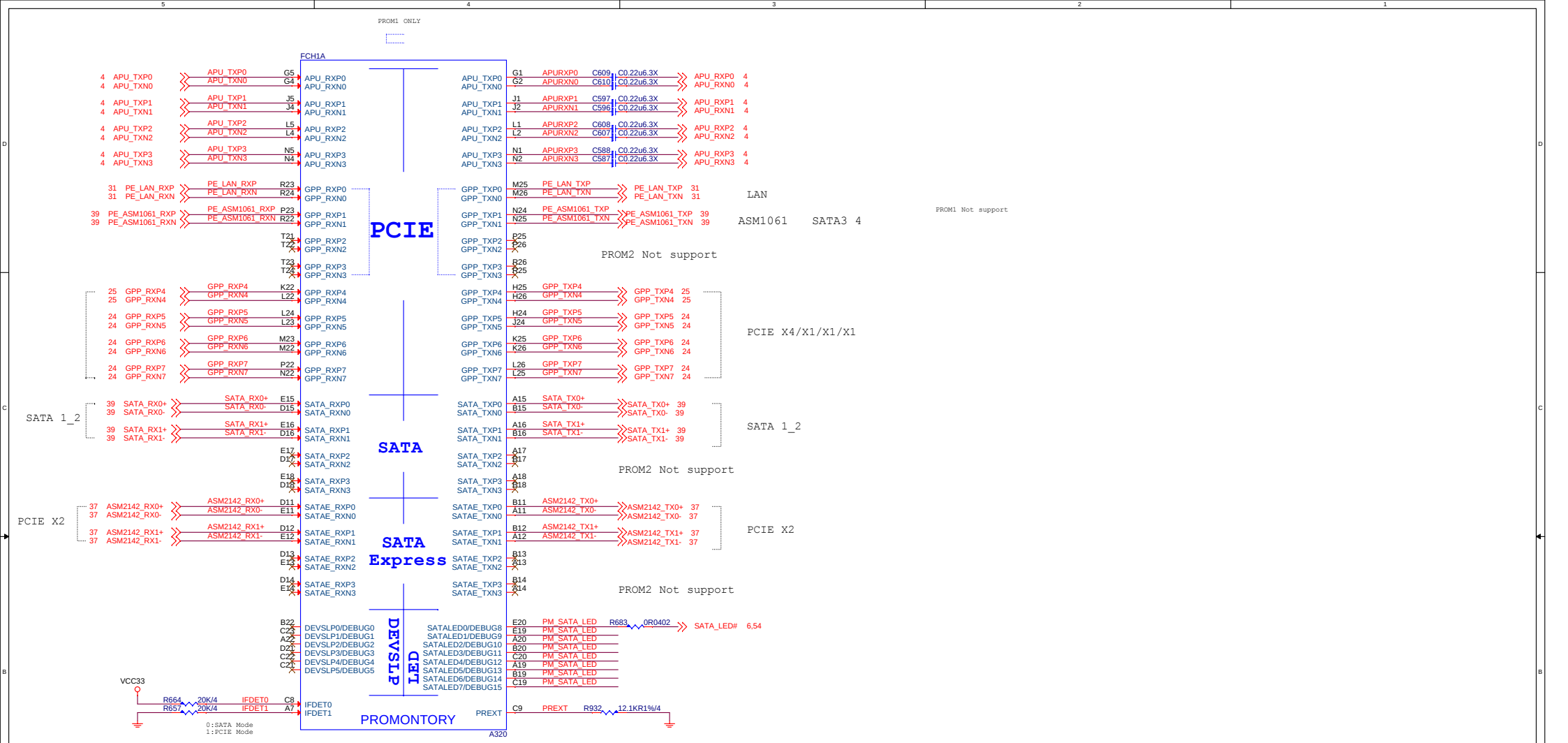

MICRO-STAR INT'L CO.,LTD	
MS-7B00	
Size: Custom	Document Description: Promontory-PCIE/SATA/SATAE
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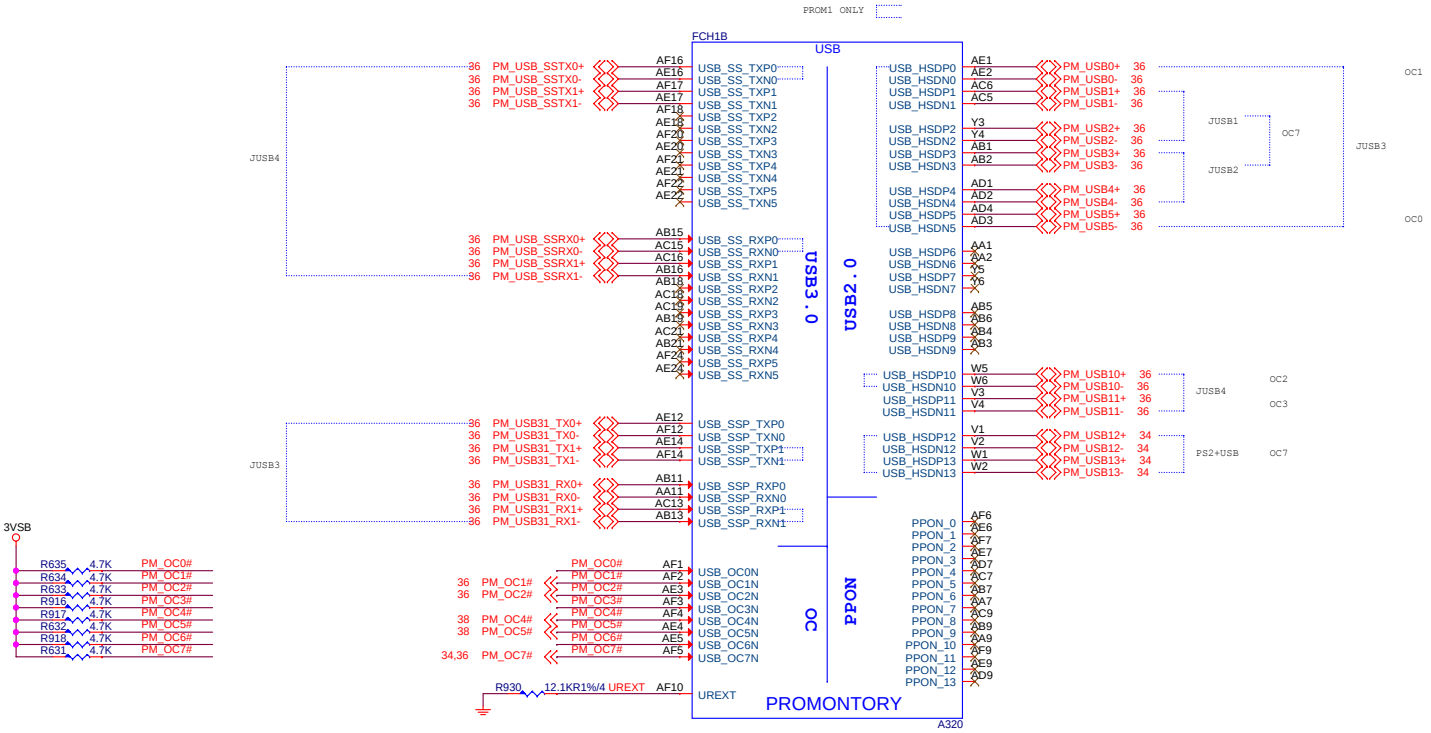

MICRO-STAR INT'L CO.,LTD	
MS-7B00	
Size: Custom	Document Description: Promontory-USB/OC
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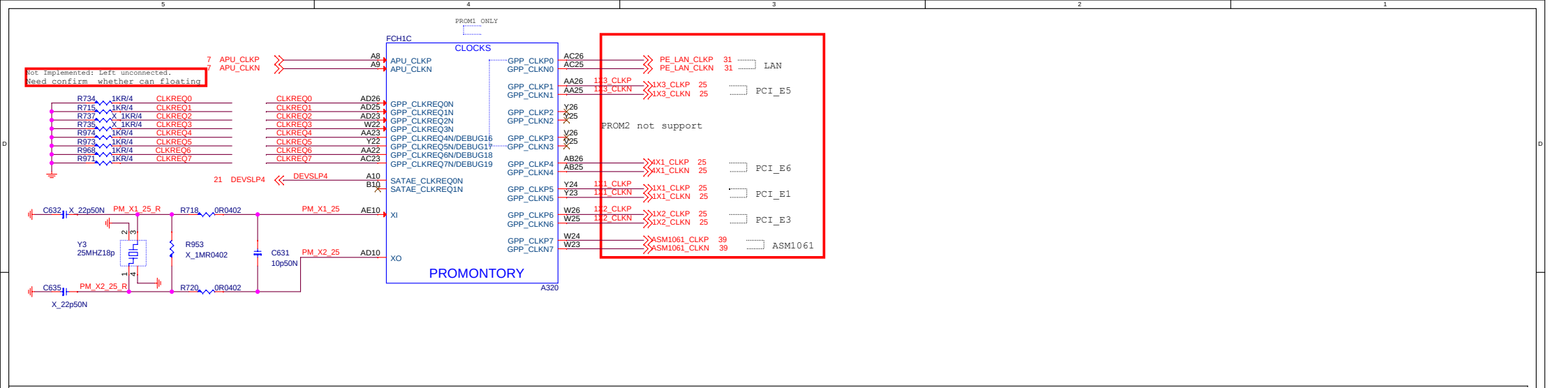
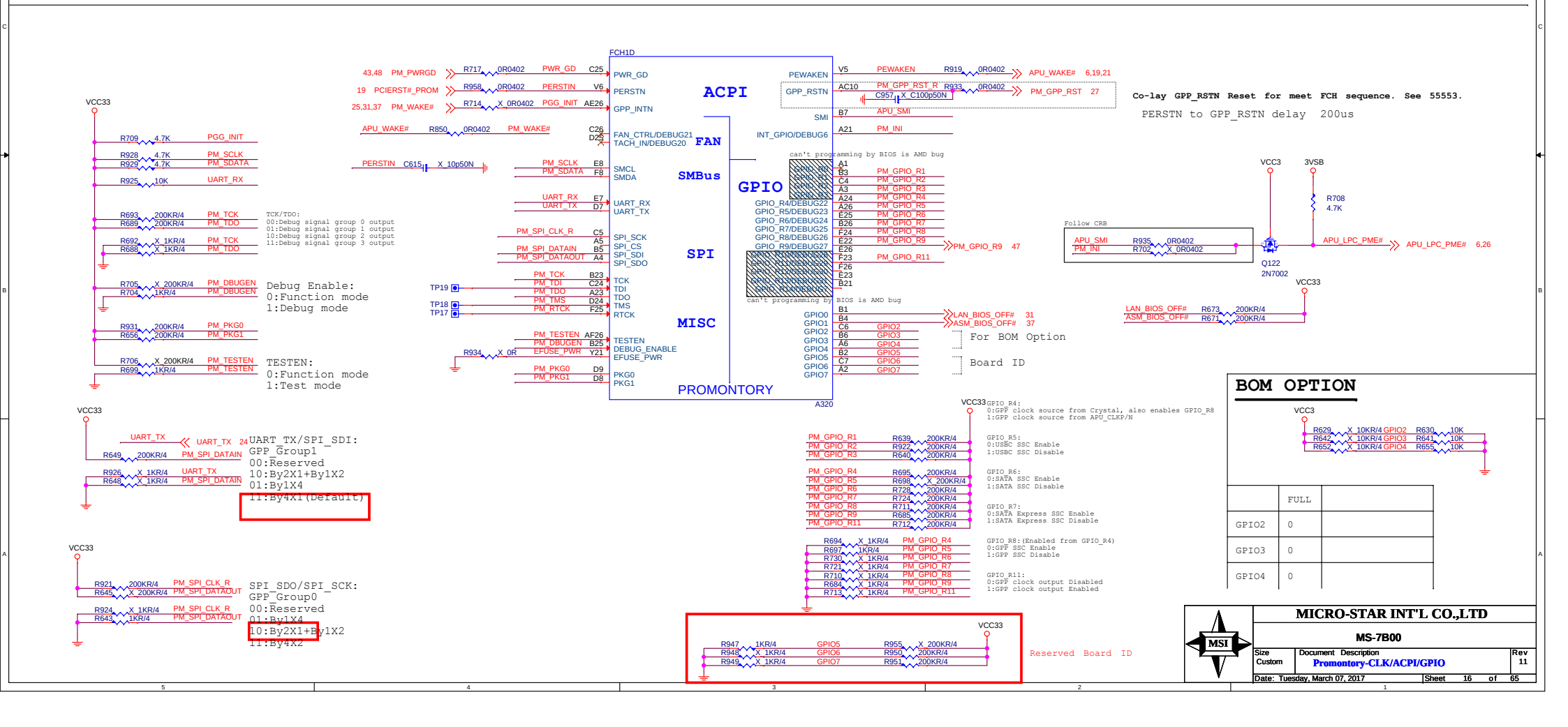

PROM1 ONLY
FCH1C
CLOCKS
Not Implemented: Left unconnected.
Need confirm whether can floating
APU_CLKP
APU_CLKN
GPP_CLKP0
GPP_CLKN0
GPP_CLKP1
GPP_CLKN1
GPP_CLKP2
GPP_CLKN2
GPP_CLKP3
GPP_CLKN3
GPP_CLKP4
GPP_CLKN4
GPP_CLKP5
GPP_CLKN5
GPP_CLKP6
GPP_CLKN6
GPP_CLKP7
GPP_CLKN7
PE_LAN_CLKP
PE_LAN_CLKN
LAN
1X3_CLKP
1X3_CLKN
PCI_E5
PROM2 not support
1X1_CLKP
1X1_CLKN
PCI_E6
PCI_E1
1X2_CLKP
1X2_CLKN
PCI_E3
ASM1061_CLKP
ASM1061_CLKN
ASM1061
CLKREQ0
CLKREQ1
CLKREQ2
CLKREQ3
CLKREQ4
CLKREQ5
CLKREQ6
CLKREQ7
GPP_CLKREQ0N
GPP_CLKREQ1N
GPP_CLKREQ2N
GPP_CLKREQ3N
GPP_CLKREQ4N/DEBUG16
GPP_CLKREQ5N/DEBUG17
GPP_CLKREQ6N/DEBUG18
GPP_CLKREQ7N/DEBUG19
DEVSLP4
SATAE_CLKREQ0N
SATAE_CLKREQ1N
C632 X_22p50N
C635 X_22p50N
PM_X1_25_R
PM_X2_25_R
R718 0R0402
R720 0R0402
Y3 25MHZ18p
R953 X_1MR0402
C631 10p50N
PM_X1_25
PM_X2_25
XI
XO
PROMONTORY
A320


FCH1D
ACPI
FAN
SMBus
GPIO
SPI
MISC
PROMONTORY
A320
PWR_GD
PERSTN
GPP_INTN
FAN_CTRL/DEBUG21
TACH_IN/DEBUG20
SMCL
SMDA
UART_RX
UART_TX
SPI_SCK
SPI_CS
SPI_SDI
SPI_SDO
TCK
TDI
TDO
TMS
RTCK
TESTEN
DEBUG_ENABLE
EFUSE_PWR
PKG0
PKG1
PEWAKEN
GPP_RSTN
SMI
INT_GPIO/DEBUG6
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
can't programming by BIOS is AMD bug
PM_PWRGD
PCIERST#_PROM
PM_WAKE#
APU_WAKE#
PERSTN
PM_SCLK
PM_SDATA
PM_SPI_CLK_R
PM_SPI_DATAIN
PM_SPI_DATAOUT
PM_TCK
PM_TDI
PM_TDO
PM_TMS
PM_RTCK
PM_TESTEN
PM_DBUGEN
EFUSE_PWR
PM_PKG0
PM_PKG1
PM_GPIO_R1
PM_GPIO_R2
PM_GPIO_R3
PM_GPIO_R4
PM_GPIO_R5
PM_GPIO_R6
PM_GPIO_R7
PM_GPIO_R8
PM_GPIO_R9
PM_GPIO_R11
LAN_BIOS_OFF#
ASM_BIOS_OFF#
For BOM Option
Board ID
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
PERSTN to GPP_RSTN delay 200us
Follow CRB
Q122
2N7002
TCK/TDO:
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output
Debug Enable:
0:Function mode
1:Debug mode
TESTEN:
0:Function mode
1:Test mode
UART_TX/SPI_SDI:
GPP_Group1
00:Reserved
10:By2X1+By1X2
01:By1X4
11:By4X1(Default)
SPI_SDO/SPI_SCK:
GPP_Group0
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X2
GPIO_R4:
0:GPP clock source from Crystal, also enables GPIO_R8
1:GPP clock source from APU_CLKP/N
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable
GPIO_R7:
0:SATA Express SSC Enable
1:SATA Express SSC Disable
GPIO_R8:(Enabled from GPIO_R4)
0:GPP SSC Enable
1:GPP SSC Disable
GPIO_R11:
0:GPP clock output Disabled
1:GPP clock output Enabled
Reserved Board ID
BOM OPTION
FULL
GPIO2 0
GPIO3 0
GPIO4 0
MICRO-STAR INT'L CO.,LTD
MS-7B00
Size Custom
Document Description Promontory-CLK/ACPI/GPIO
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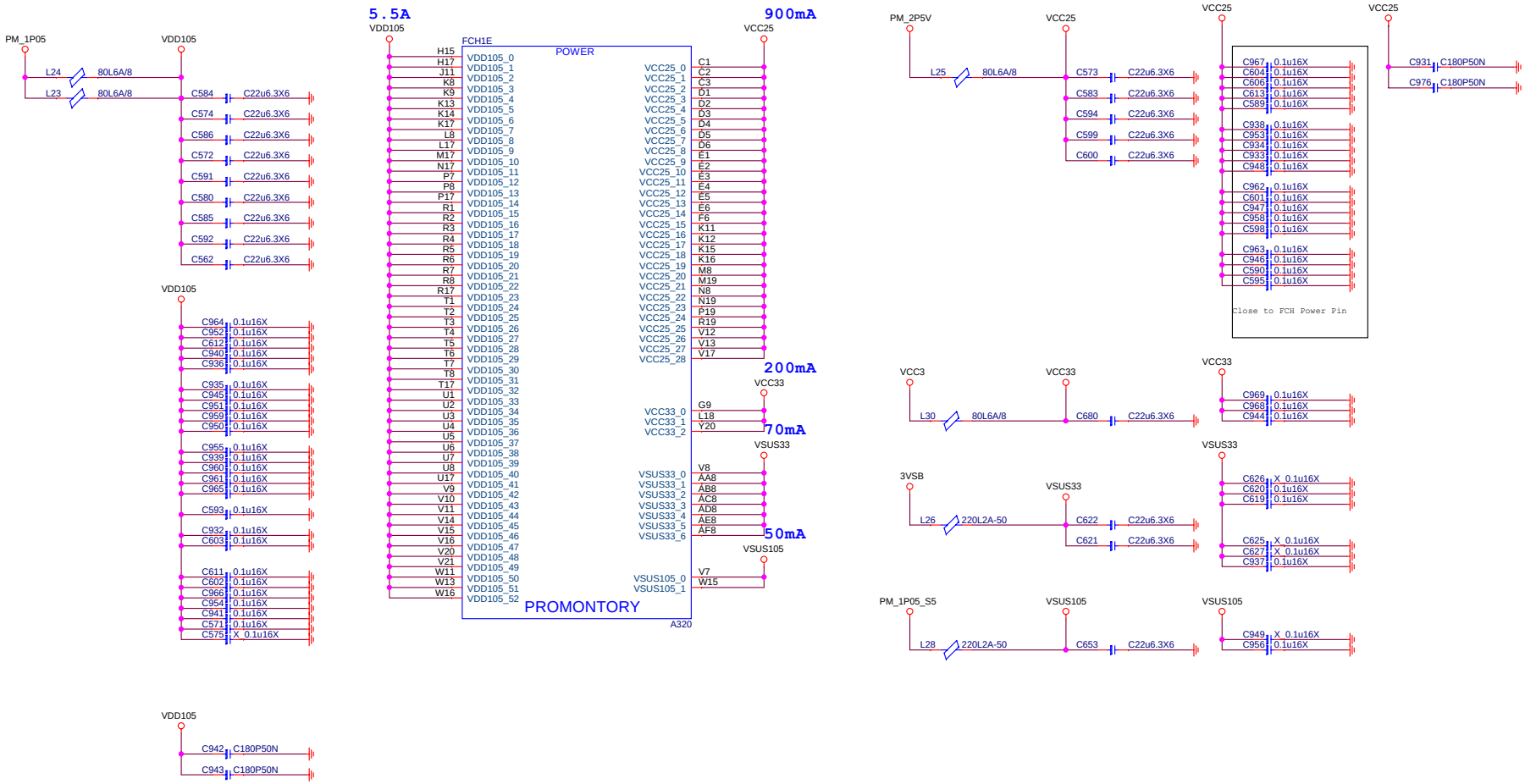

MICRO-STAR INT'L CO.,LTD		
MS-7B00		
Size: Custom	Document Description: Promontory-Power	Rev: 11
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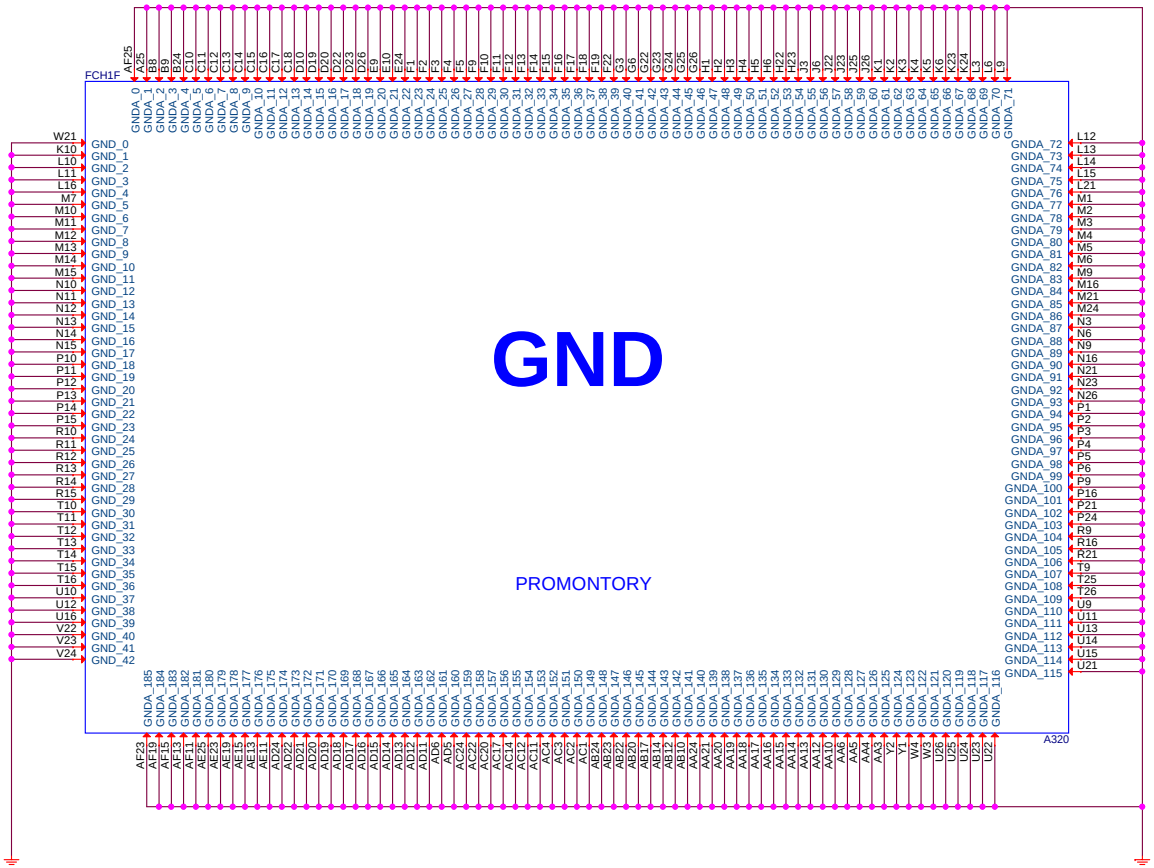

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MS-7B00	
Size: Custom	Document Description: Promontory-GND
Rev: 11	
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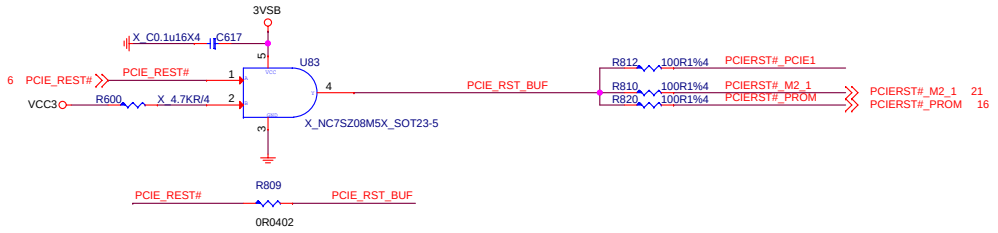
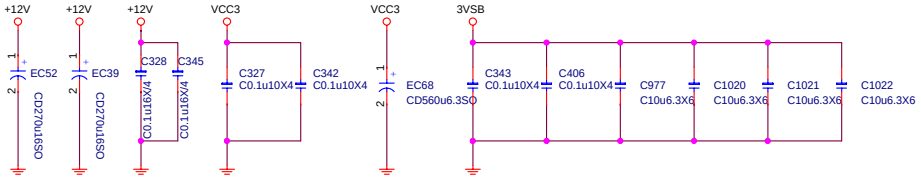
PCI EXPRESS x16 Slot

3.3V 3.0A
12V 5.5A





MICRO-STAR INT'L CO.,LTD			
MS-7B00			
Size: Custom	Document Description: PCIE X16 SLOT		Rev: 11
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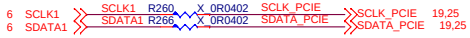
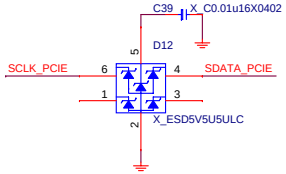
SMBus separate circuit

SMB_SEL
GPIO Default High





PCIE Lanes control circuit

	PCIE_CNTL	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0

PCI EXPRESS Switch

For PCIE2 & PCIE4

MICRO-STAR INT'L CO.,LTD

MS-7B00

Size	Document Description	Rev
Custom	PCIE Switch	11

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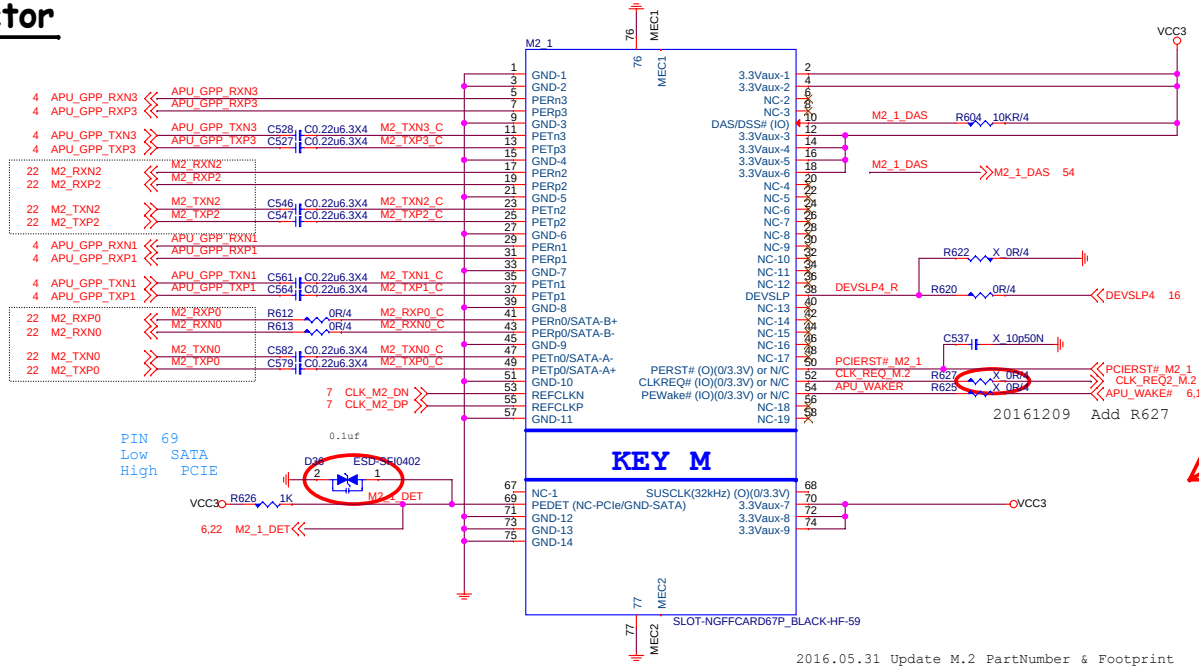
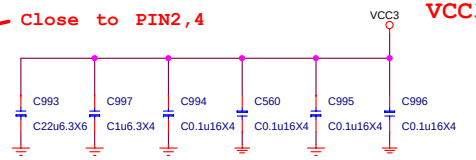
M.2 Connector

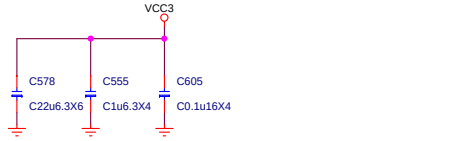


Close to PIN2,4

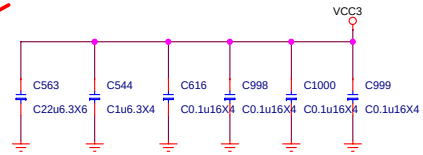


VCC3 2.5A

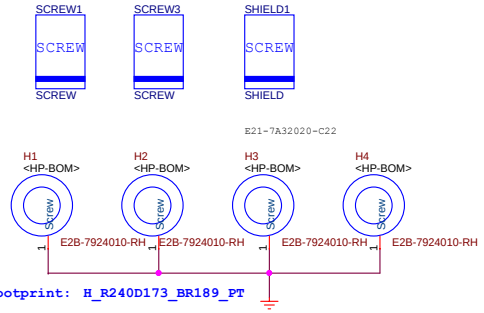
Close to PIN12, 14, 16, 18



Close to PIN70, 72, 74



2016.05.31 Update M.2 PartNumber & Footprint
ON1-7A58001-L06
SLOT_NGFFCARD67_31



Footprint: H_R240D173_BR189_PT

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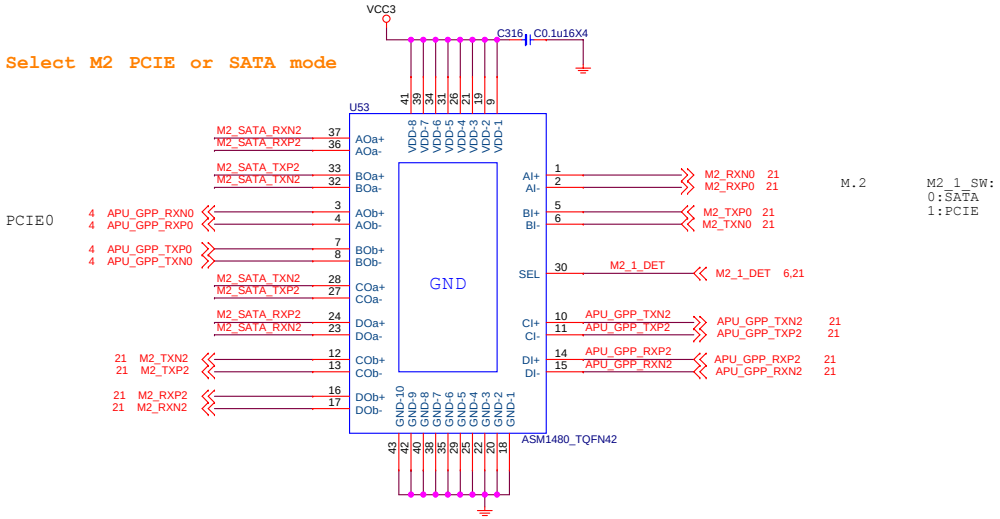
Select M2 PCIE or SATA mode



GPP	0	1	2	3
TYPE0	PCIE	PCIE	SATA	SATA
TYPE2	PCIE	PCIE	PCIE	PCIE
	PCIE	PCIE	SATA	SATA

MICRO-STAR INT'L CO.,LTD

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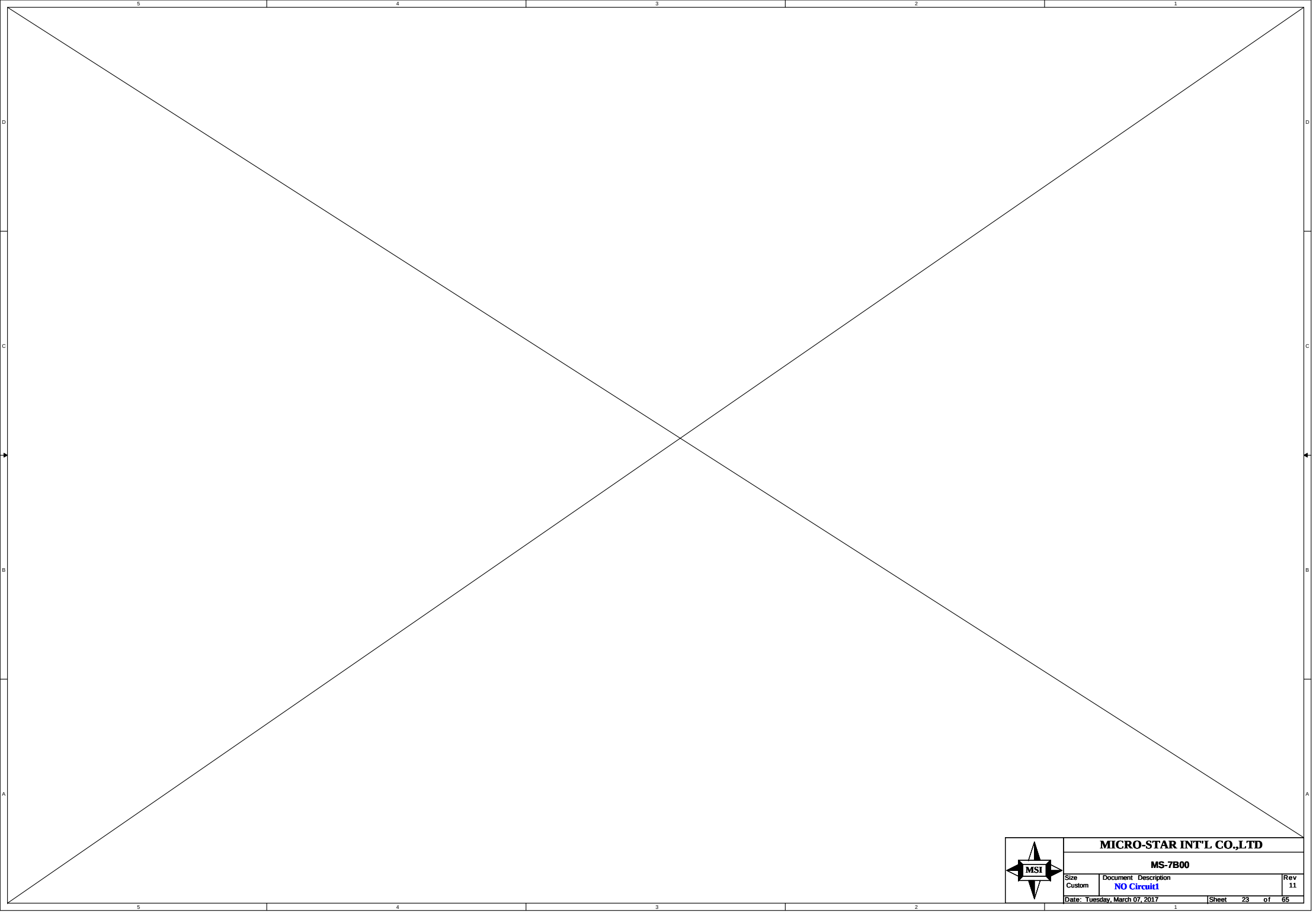

MICRO-STAR INT'L CO.,LTD

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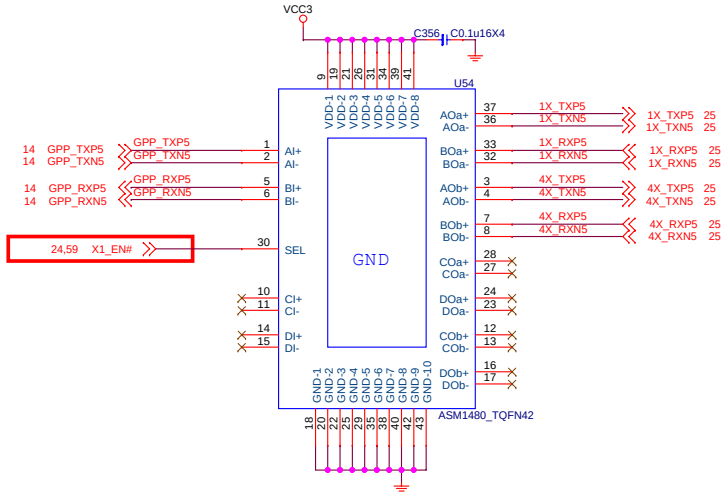

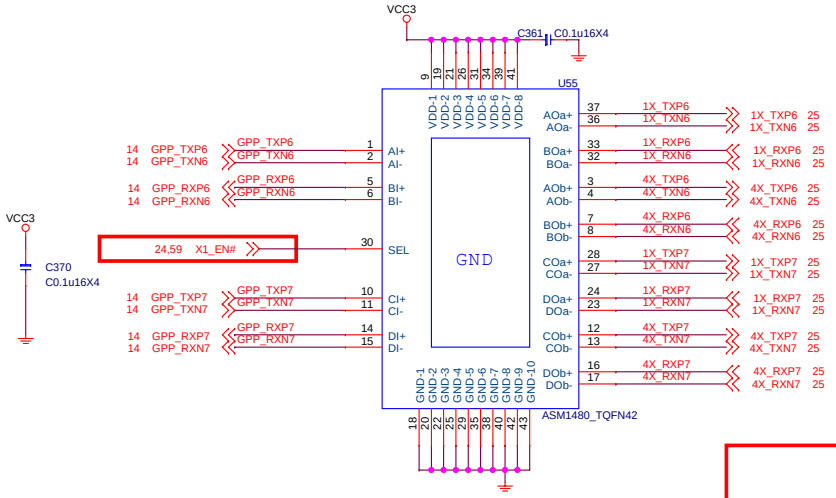

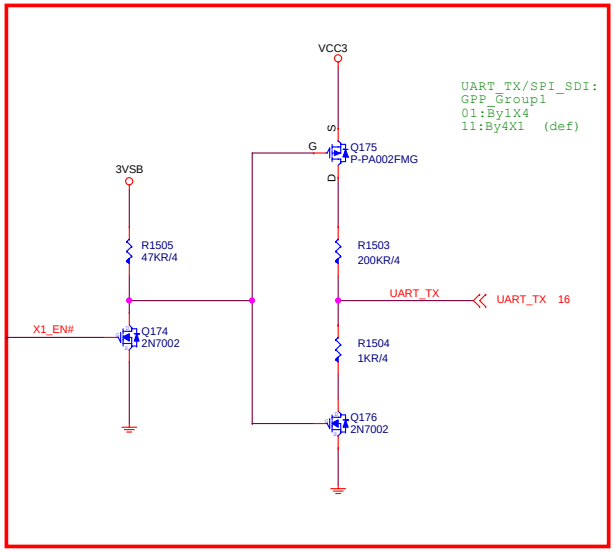

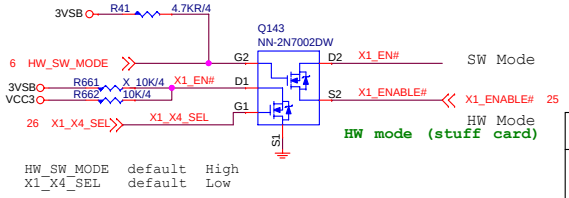

	HW_SW_MODE	X1_X4_SEL	X1_ENABLE#	X1_EN#	UART_TX	
HW MODE	1	0	1	1	H	X4
	1	0	0	0	L	X1
SW MODE	0	1	X	0	L	X1
	0	1	X	1	H	X4

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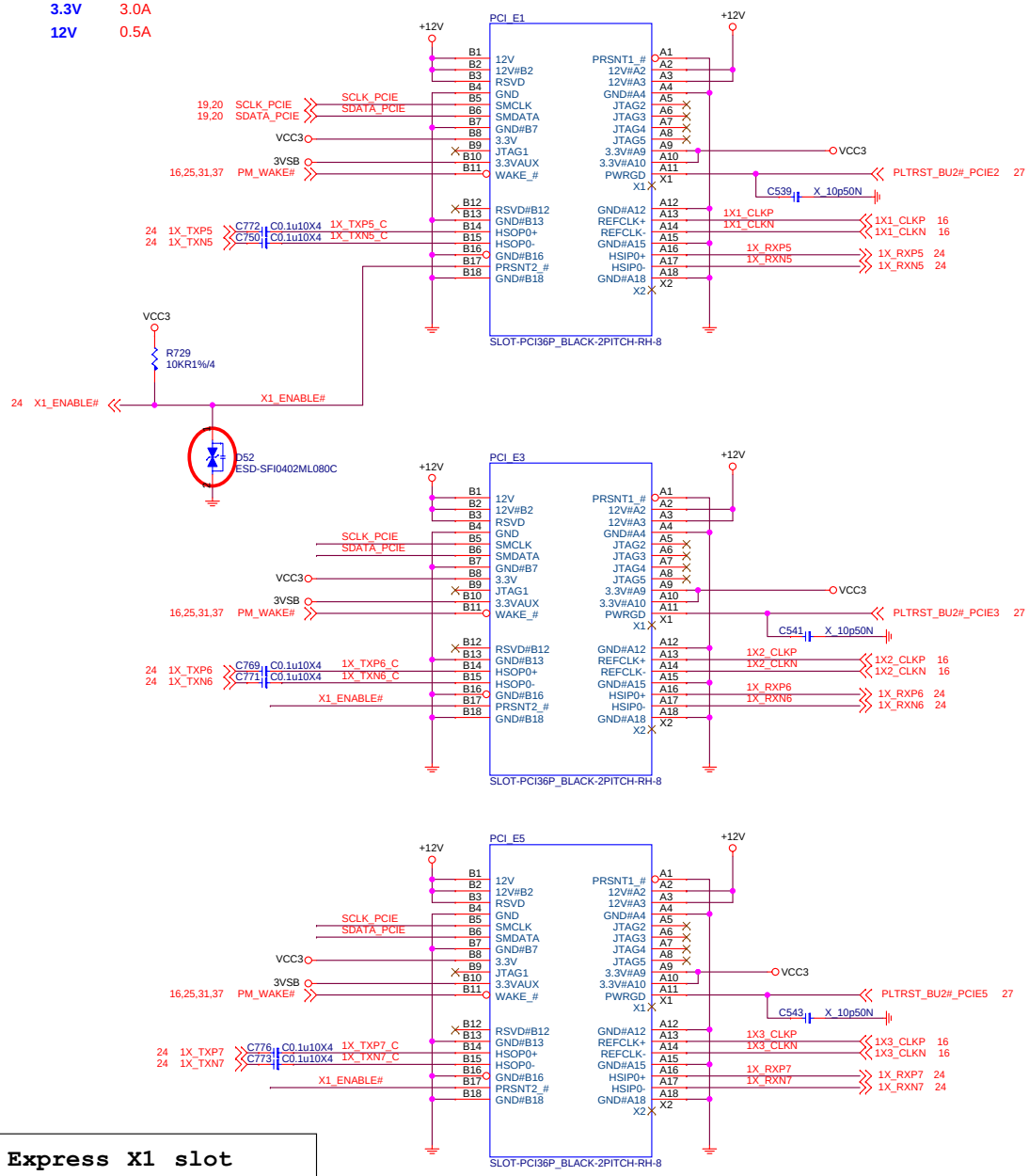
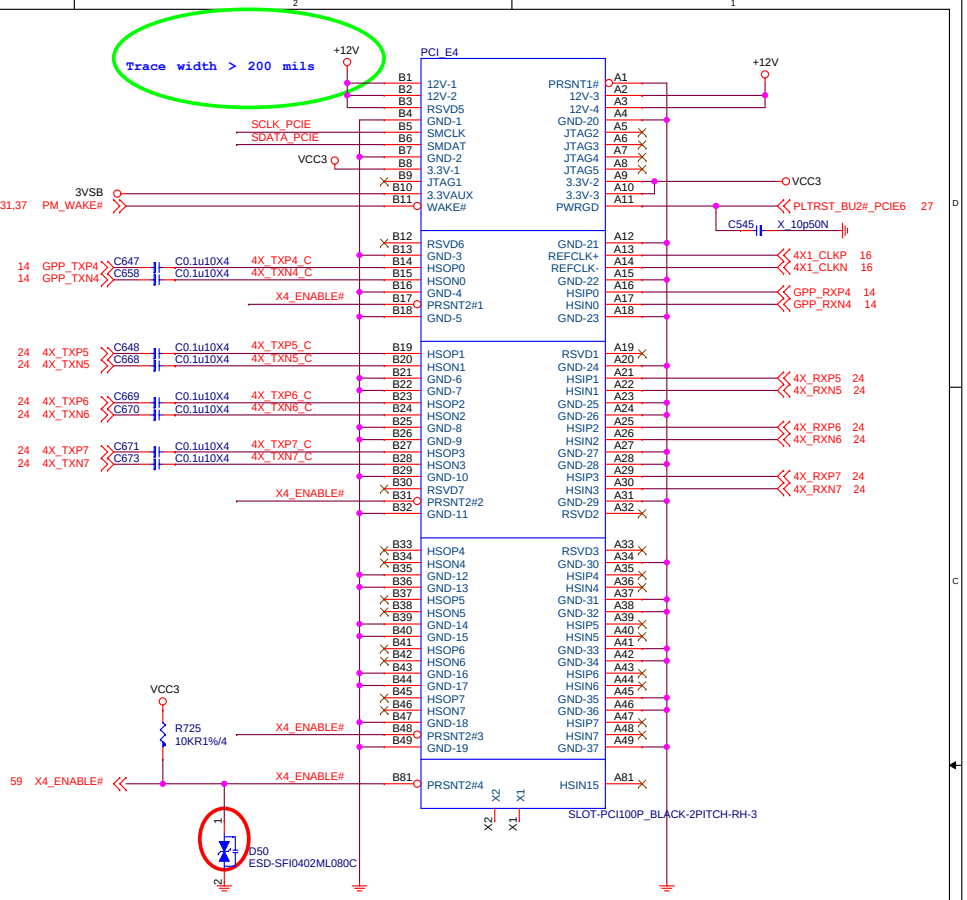
PCIEX1 12V 0.5A
3.3V weak 375mA

3.3V	3.0A
12V	0.5A





PCI Express X1 slot	
+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

MICRO-STAR INT'L CO.,LTD

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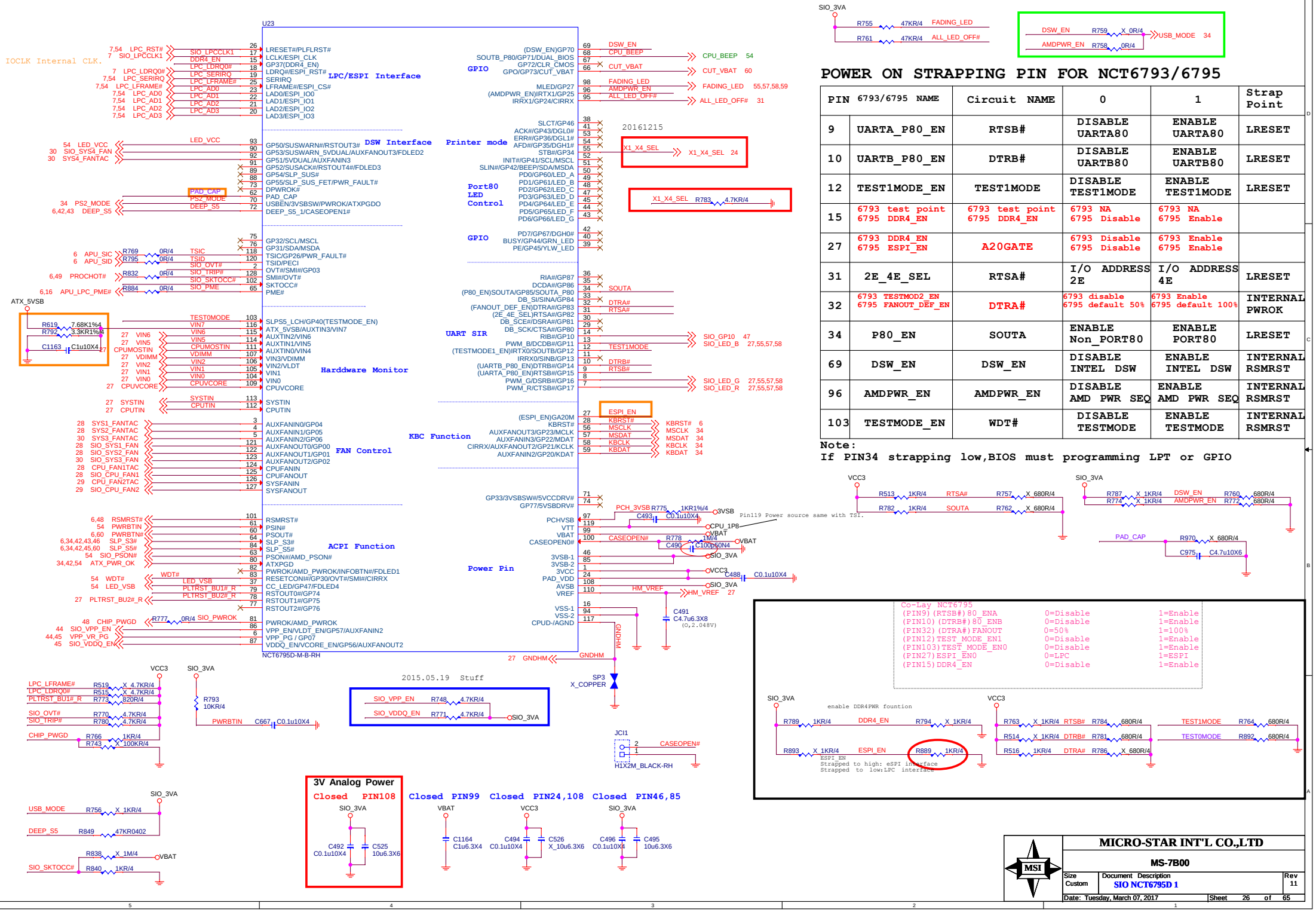

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

Co-Lay NCT6795

(PIN9)(RTSB#)80_ENA	0=Disable	1=Enable
(PIN10)(DTRB#)80_ENB	0=Disable	1=Enable
(PIN32)(DTRA#)FANOUT	0=50%	1=100%
(PIN12)TEST_MODE_EN1	0=Disable	1=Enable
(PIN103)TEST_MODE_EN0	0=Disable	1=Enable
(PIN27)ESPI_EN0	0=LPC	1=ESPI
(PIN15)DDR4_EN	0=Disable	1=Enable

enable DDR4PWR fountion

ESPI_EN
Strapped to high: eSPI interface
Strapped to low:LPC interface

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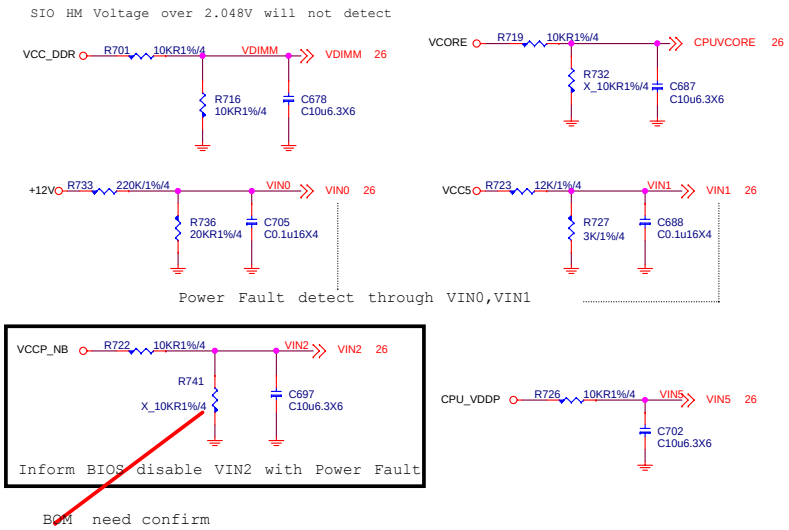
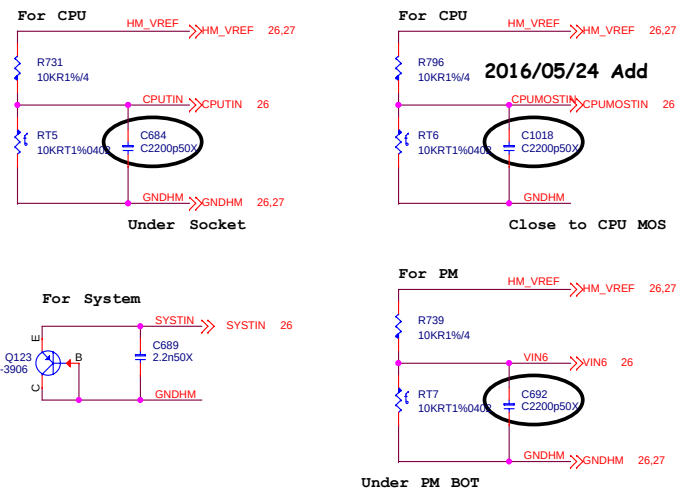
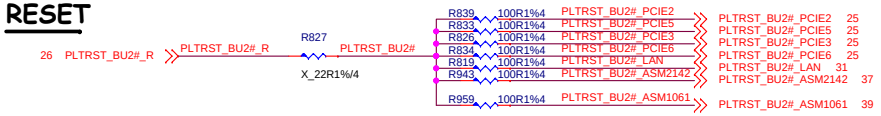
HW Monitor - Voltage



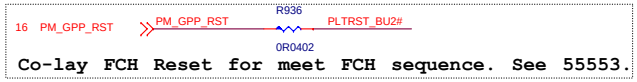
TEMP SENSOR



RESET



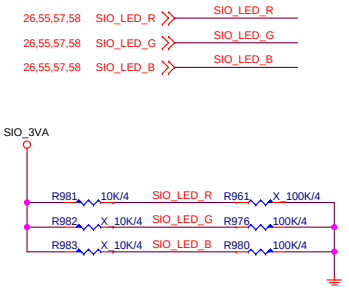
need test signal rise time/fall time



Co-lay FCH Reset for meet FCH sequence. See 55553.

20161211 LED default Red

RGB LED defult setting



Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

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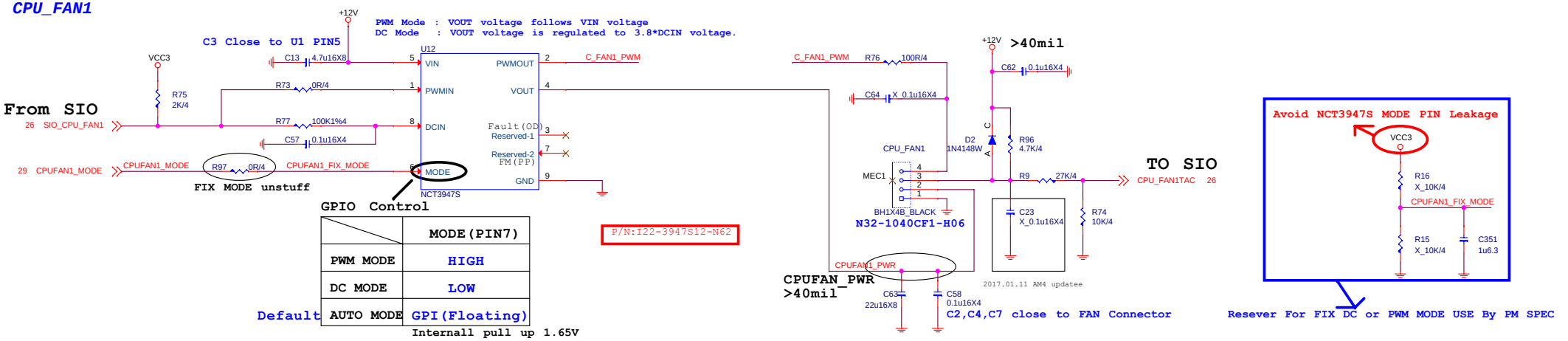
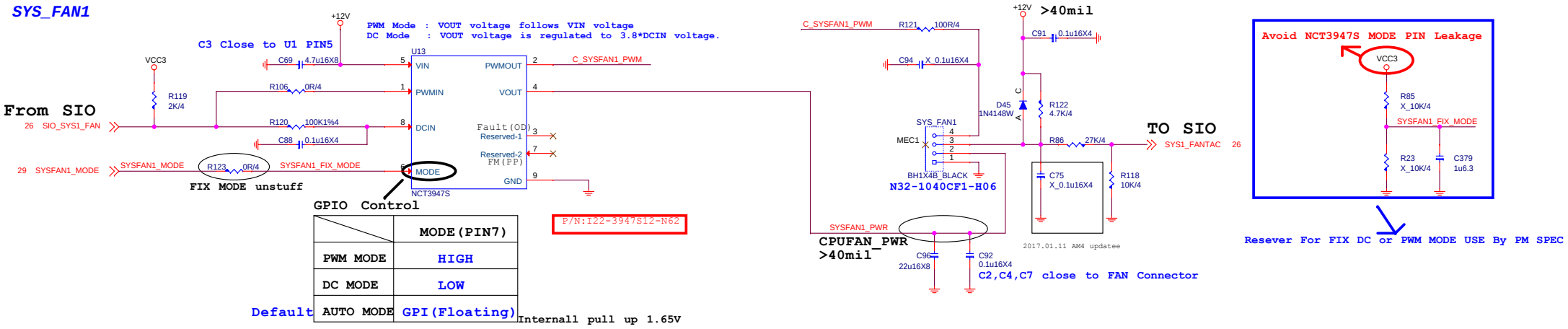
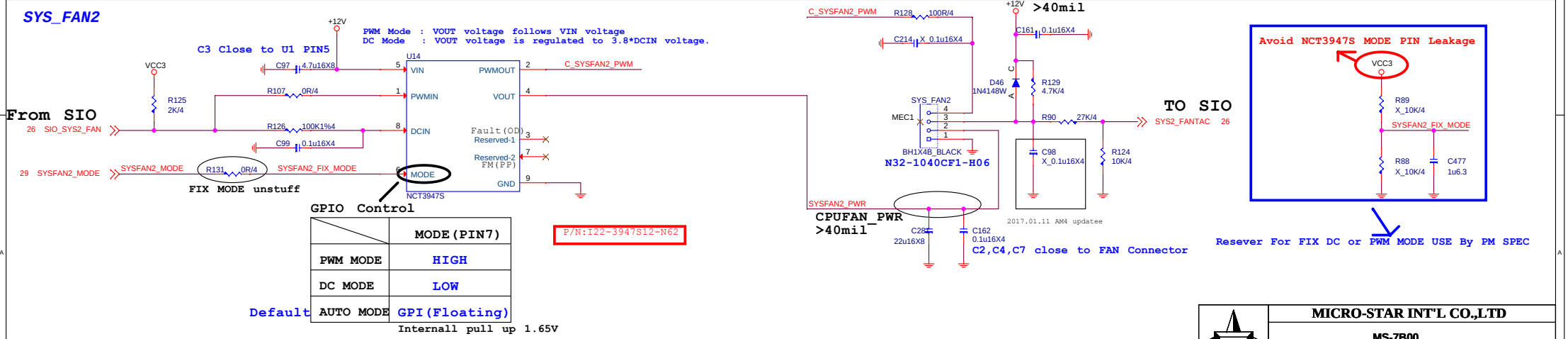
CPU_FAN1



SYS_FAN1



SYS_FAN2



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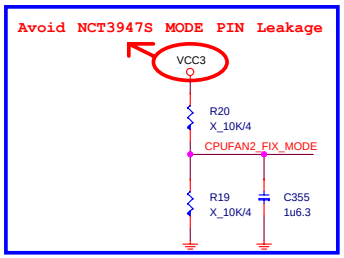
PUMP_FAN1

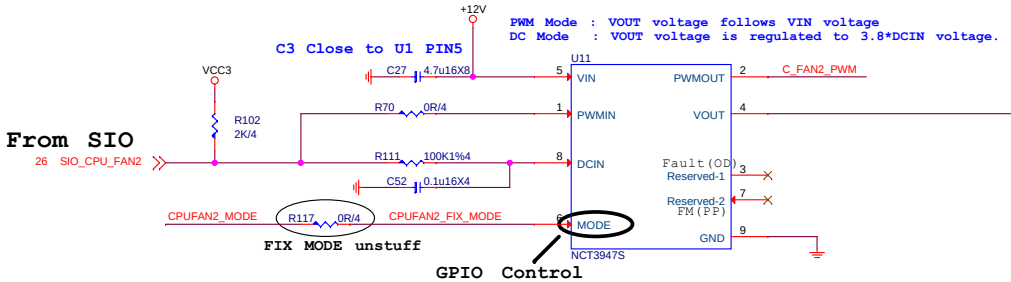
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO パBS ち传 PW M/DC M O D E

2A



Resever For FIX DC or PWM MODE USE By PM SPEC

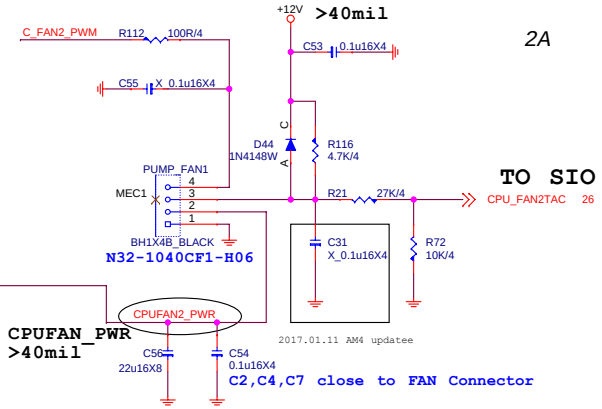


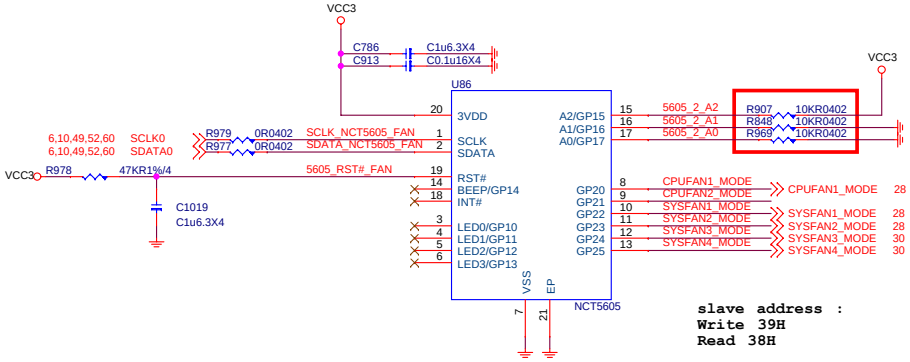
GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

P/N:I22-3947S12-N62





1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

NCT5605Y SMBus™ Address is:

0	0	1	1	A2	A1	A0	R/W

R/W: 0 Read 38H; 1 Write 39H

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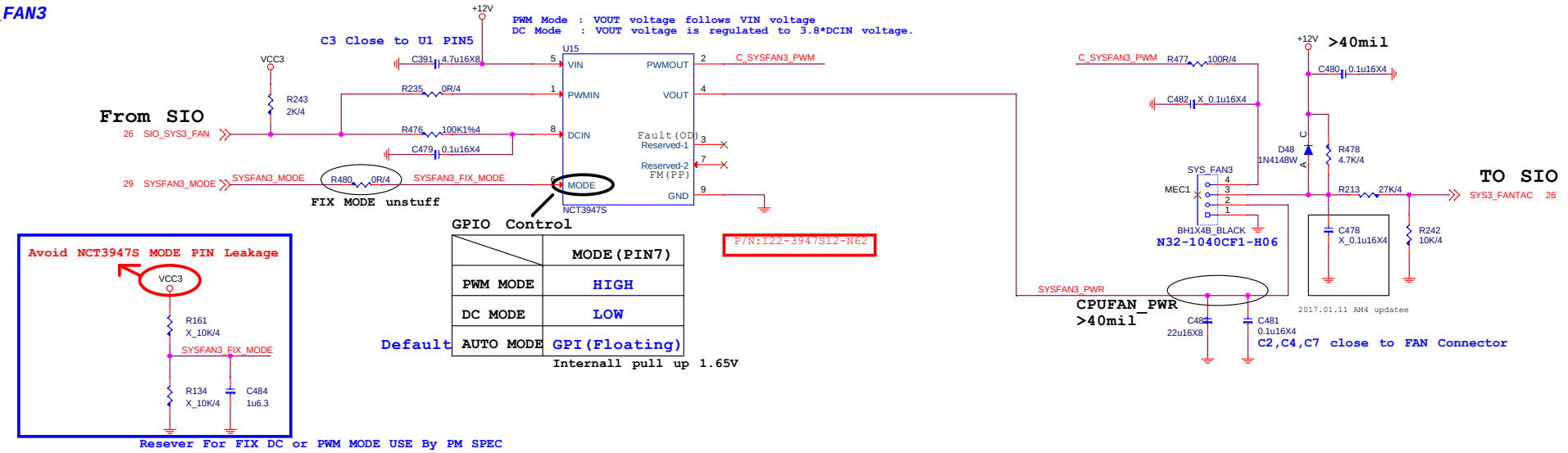
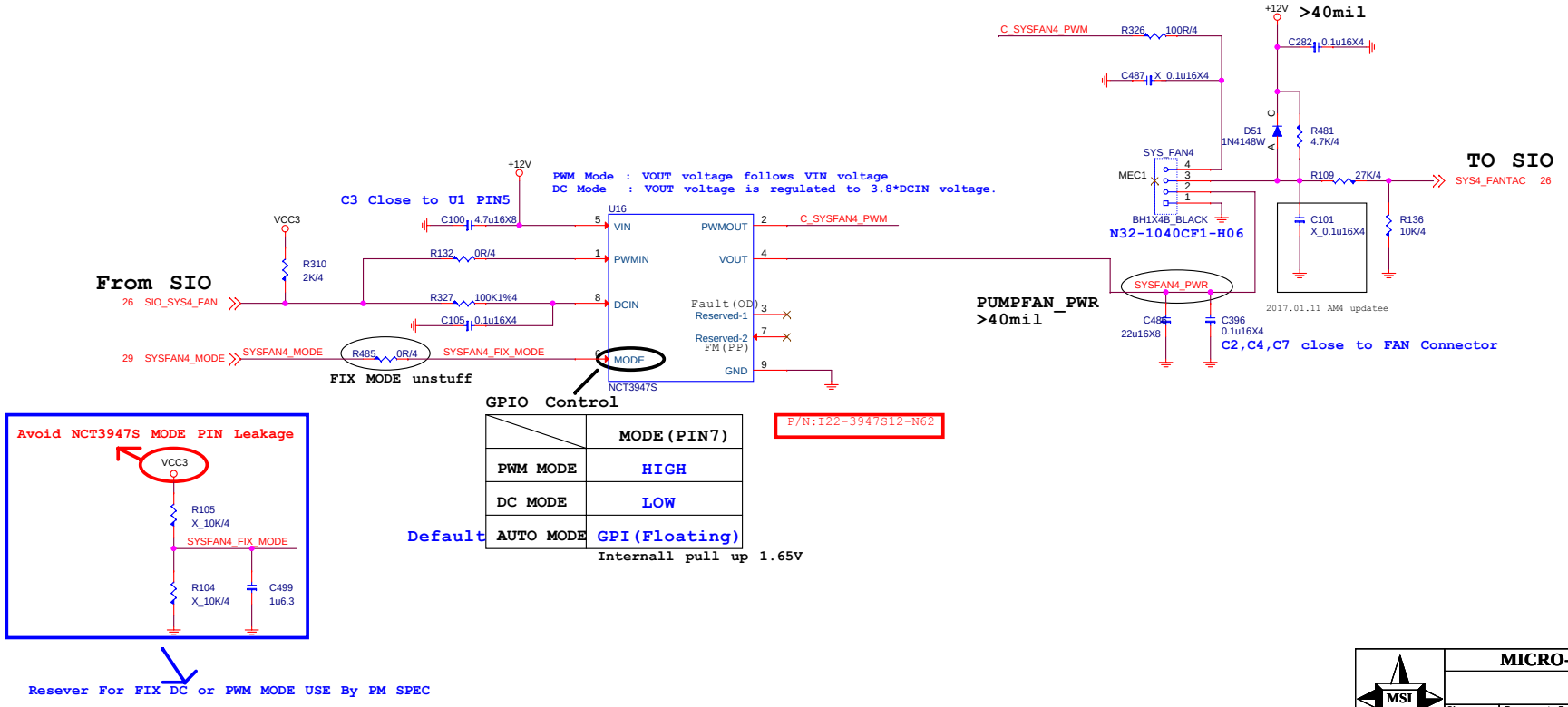
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO パB9 ち伝 PW M/DC M O D E

SYS_FAN3



SYS_FAN4



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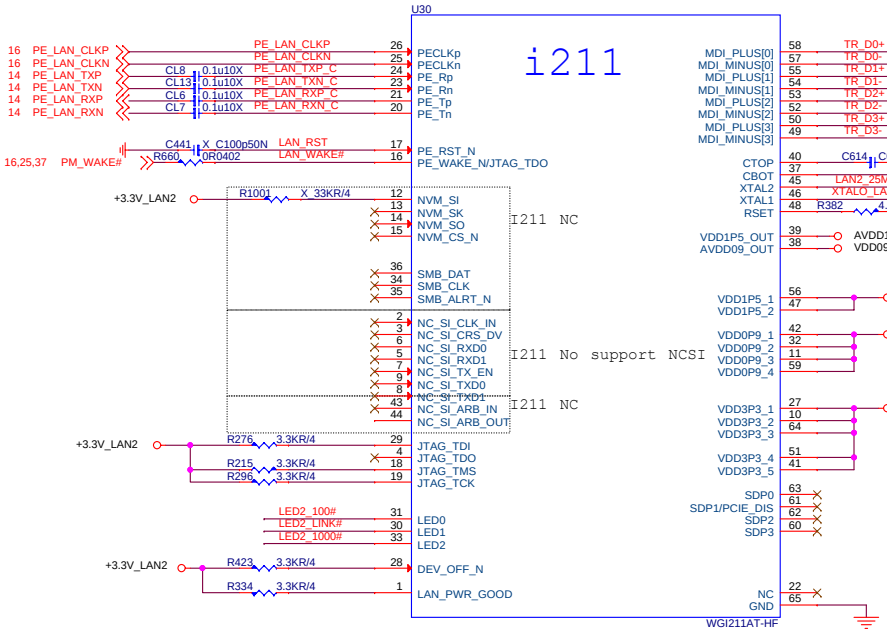
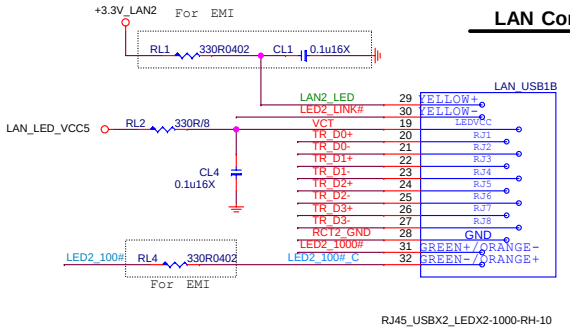
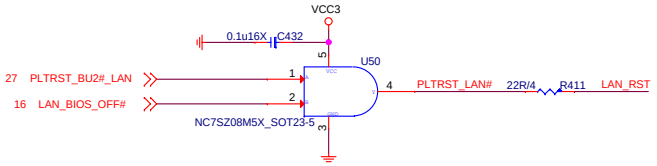
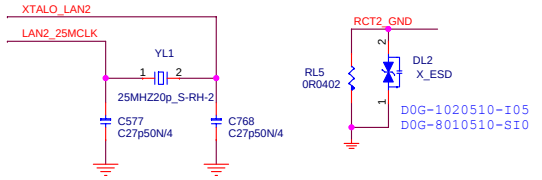
LAN2-- I211AT

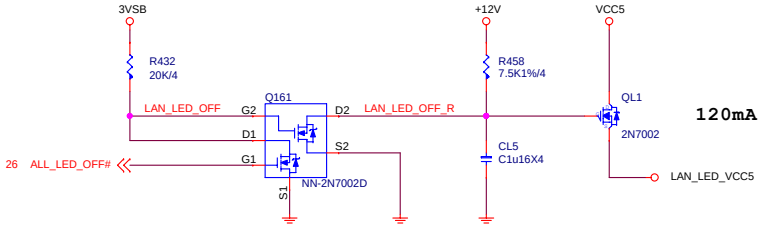


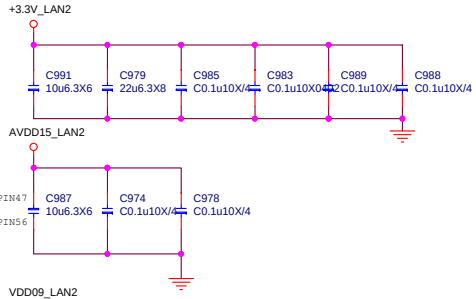
LAN Connector

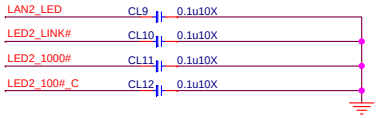


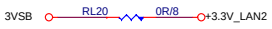


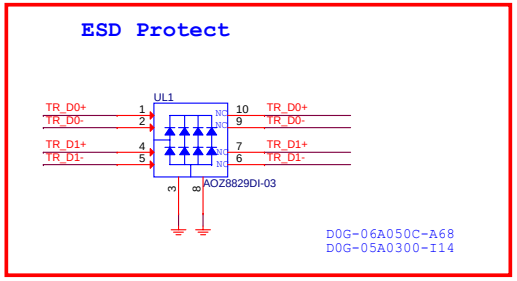












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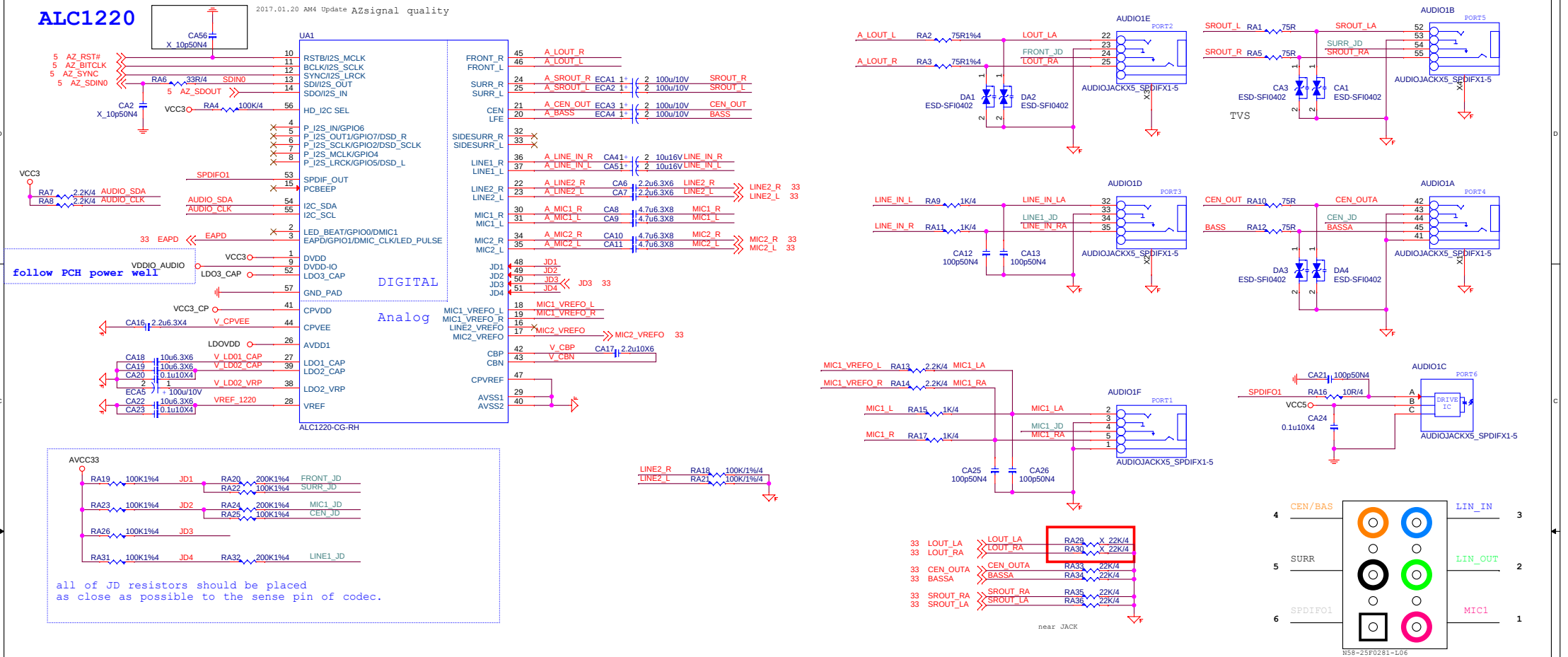
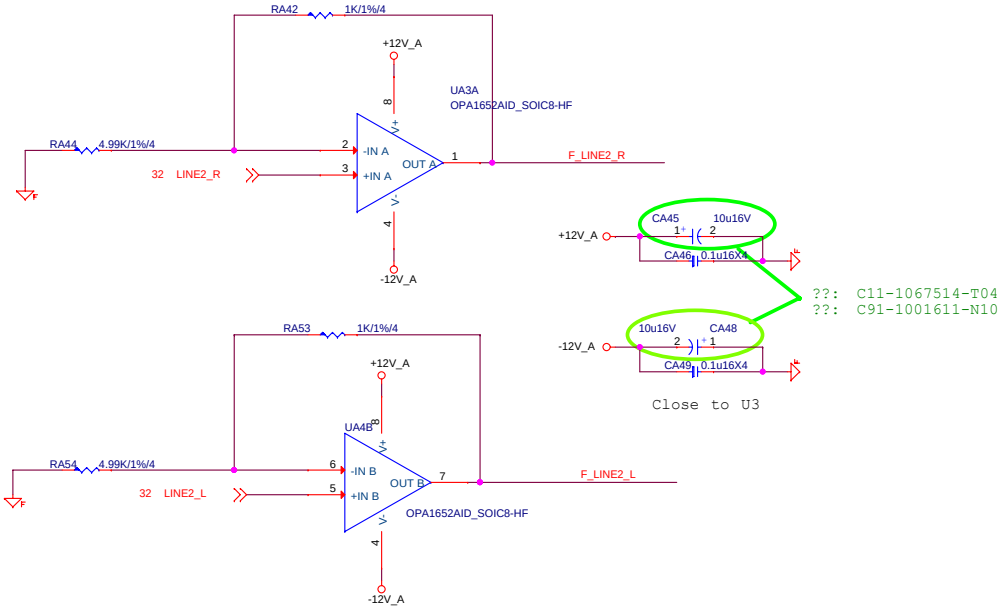
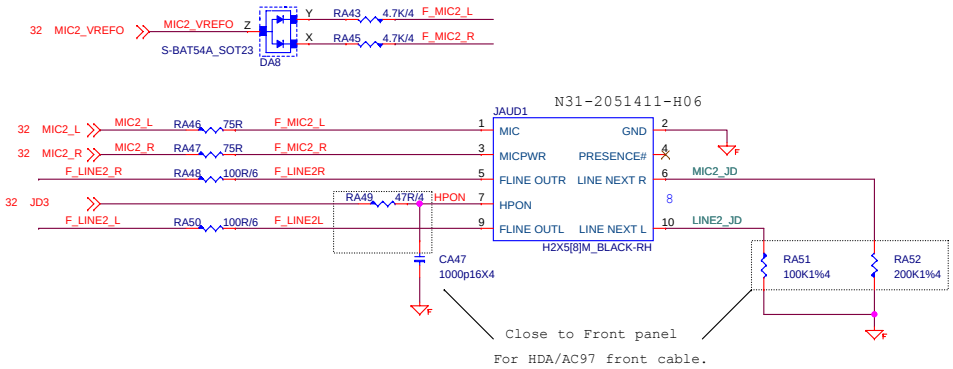
ALC1220

2017.01.20 AM4 Update AZsignal quality



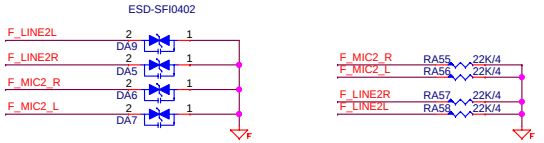




Close to Jack

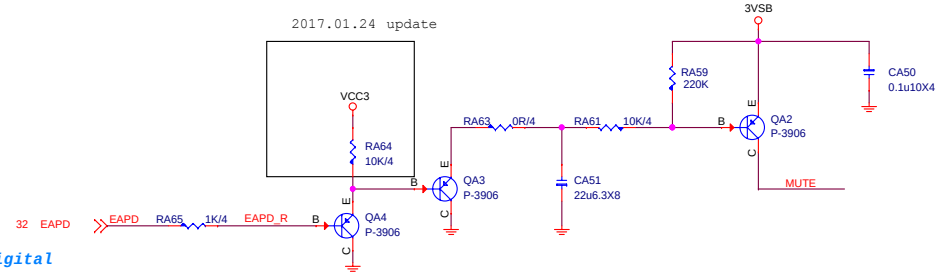
ESD protect

D0G-2950500-SI0
D0G-3010510-I05



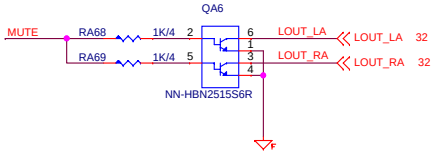
Rear Line OUT De-POP circuit

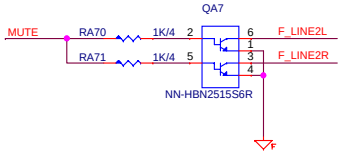
(De-pop circuit for Rear Line out & Front Headphone out)

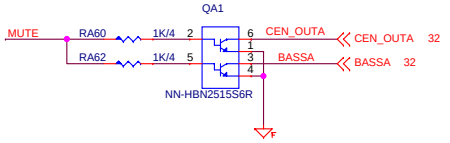


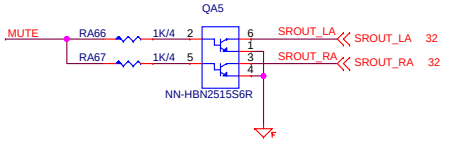
Digital

Analog









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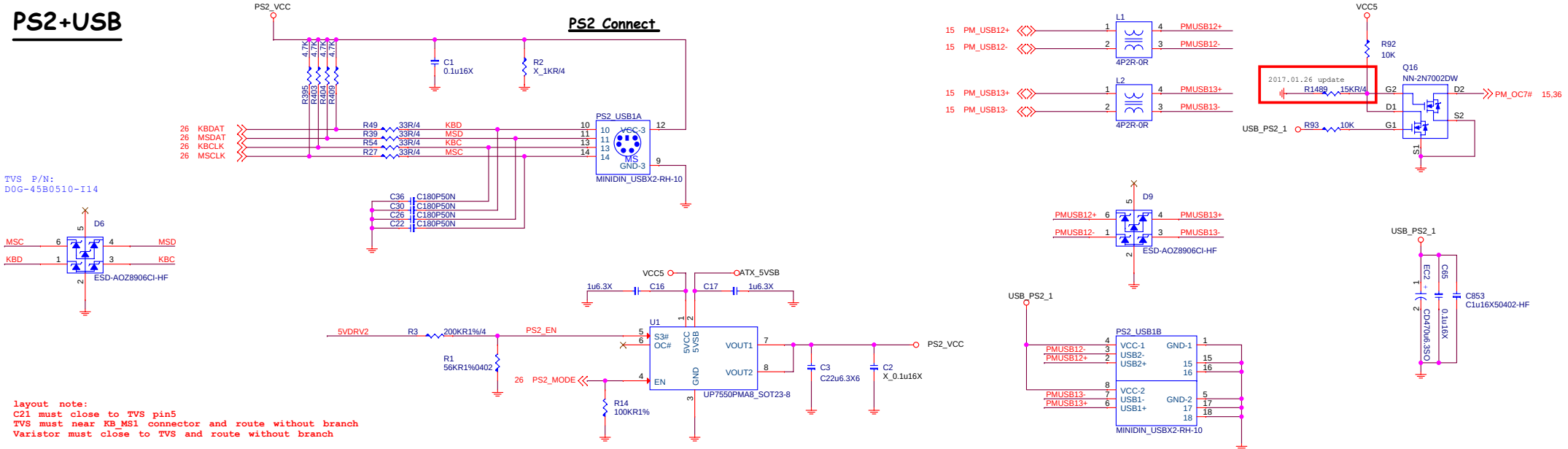
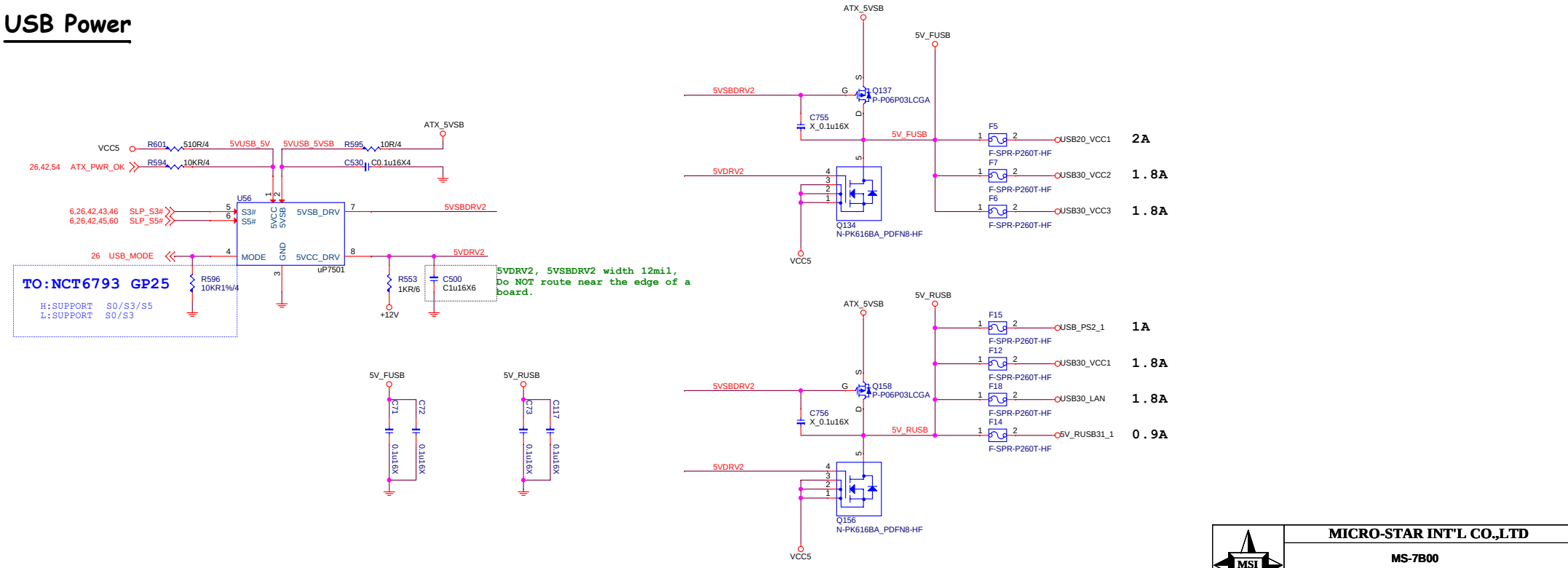
PS2+USB



USB Power



MSI

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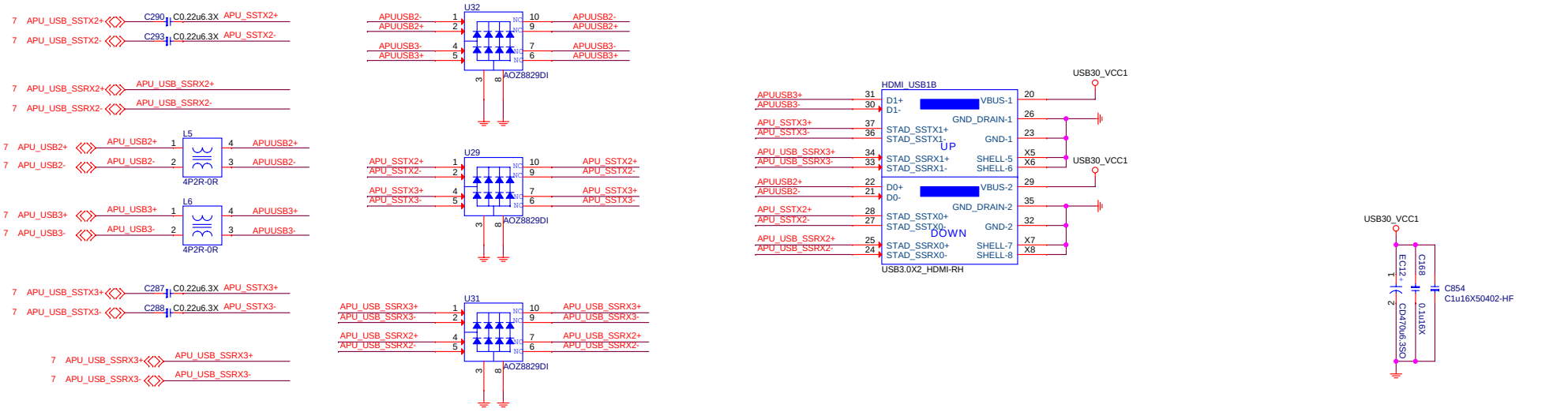
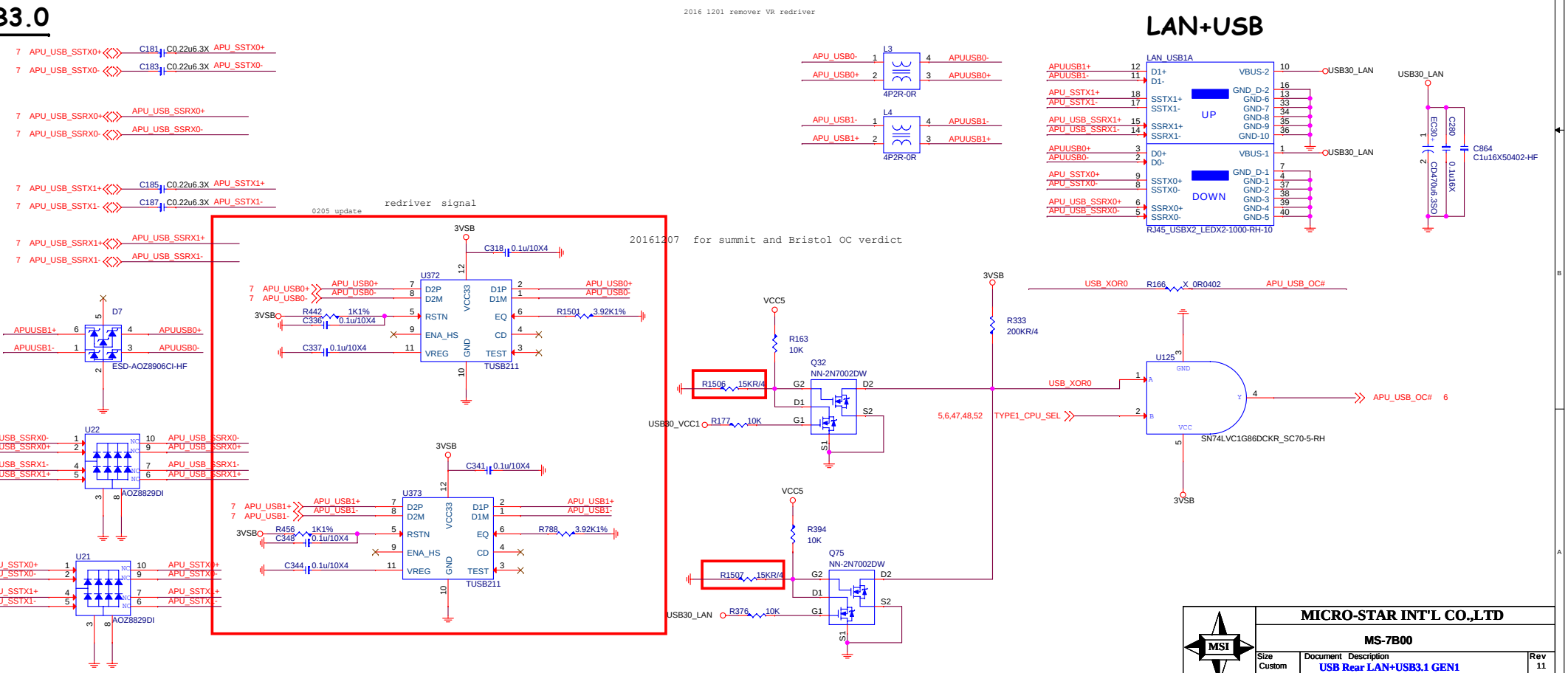
USB 3.0



USB3.0

2016 1201 remover VR redriver



LAN+USB

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MS-7B00	
Size: Custom	Document Description: USB Rear LAN+USB3.1 GEN1
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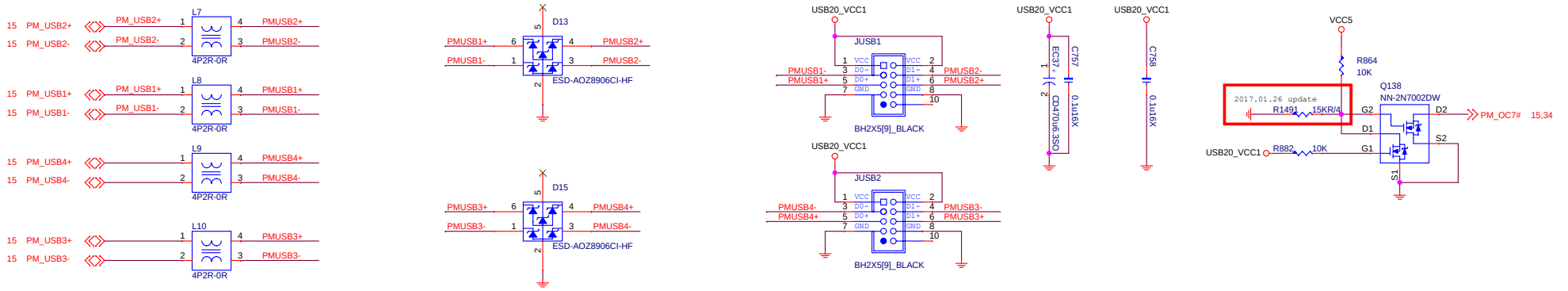
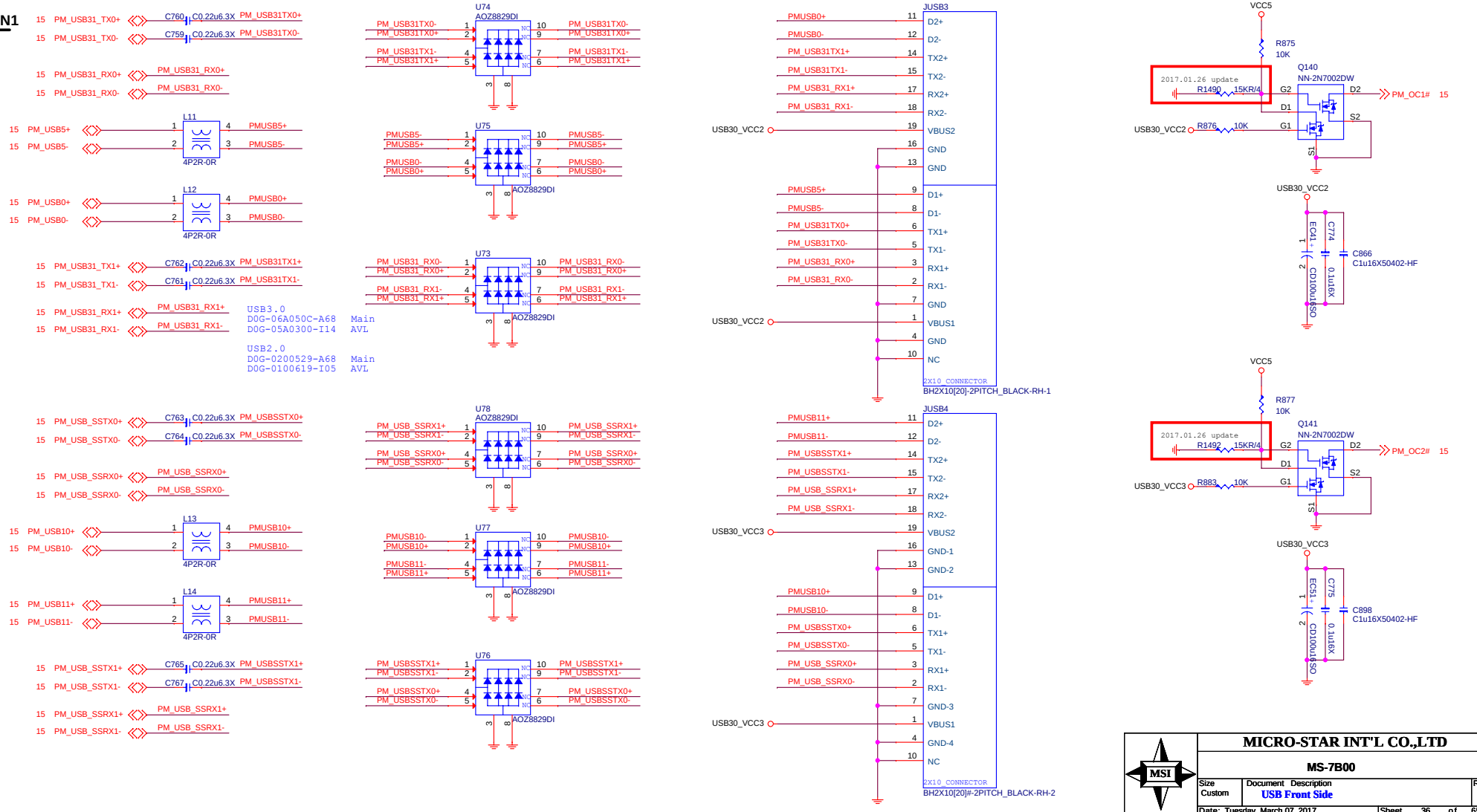
Front USB2.0



Front USB3.1 GEN1



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Minimum gap should be greater of >15mil with other signal.

Chip to Connector <1.5 inch.

Power Consumption

	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP

CLK Rule (Follow SB PDG)

PCIE Rule (Follow SB PDG)

USB HS (90Ohm-Diff)

USB SS (80Ohm-Diff)

USB HS (90Ohm-Diff)

USB SS (80Ohm-Diff)

PPON_X Internal Pull-up to VCC3

OCI_X Internal Pull-up to SUS

RX/TX Internal Pull-up

SRIS mode

SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

ASM1142 RU29 stuff RU28 unstuff
ASM2142 RU29 unstuff RU28 stuff

ASM1142 RU14 stuff RU16 unstuff
ASM2142 RU14 unstuff RU16 stuff

X0/XI (95hm-Diff,Spacing 30mil)
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8

YU1
D04-0901200-F07
D04-0901100-T16

P/N:B02-021421C-AD0

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

ASM2142 UU8 stuff RU6 unstuff
ASM1142 UU8 unstuff RU6 stuff

Reset control for ASM2142 only.

ASM1142 1.2 VCC Power

SN:L01-0107118-M26

ASM1142 RU3/RU4 100K/93.12K 1.24V
ASM2142 RU1/RU2 196K/261K 1.05V

ASM1142 1.2 VSB Power

ASM1142 RU31 18K 1.24V
ASM2142 RU31 31.6K 1.05V

EEPROM

ASM1142 UU3 M31-2551222-M24(512K bit)
ASM2142 UU3 M31-25L1022-M24(1M bit)

ASM1142/ASM1042 unstuff
ASM2142 stuff

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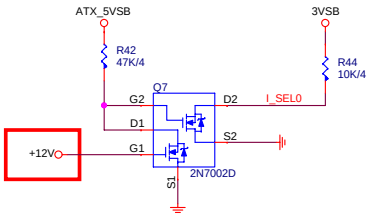
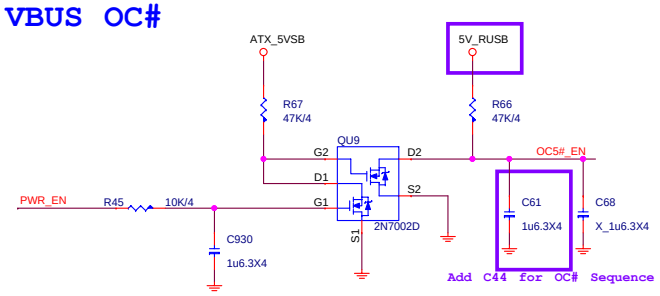
Current Mode

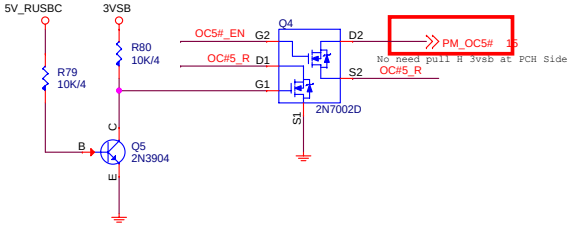


I_SEL0 : I_SEL1		
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

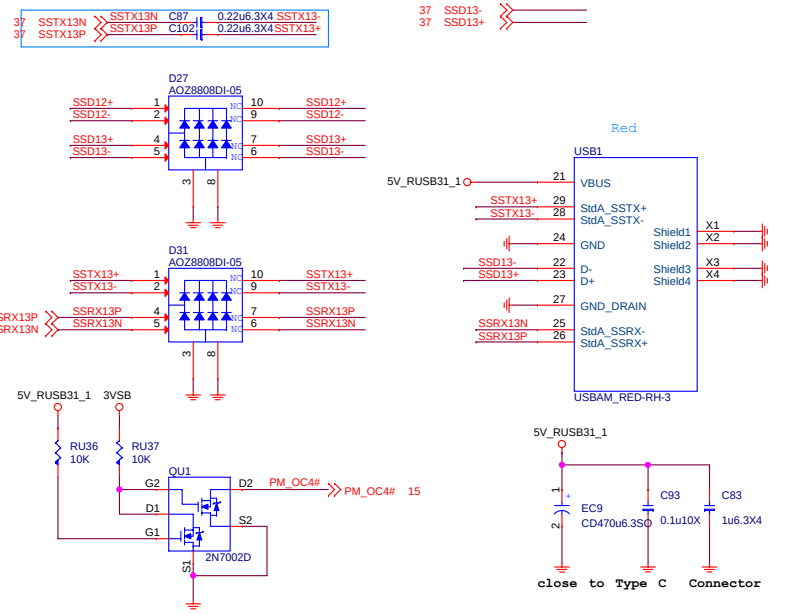
1.5A under S3 mode
3A under S0 mode

VBUS OC#

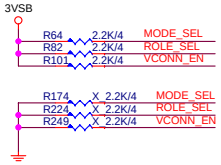




TYPE-A



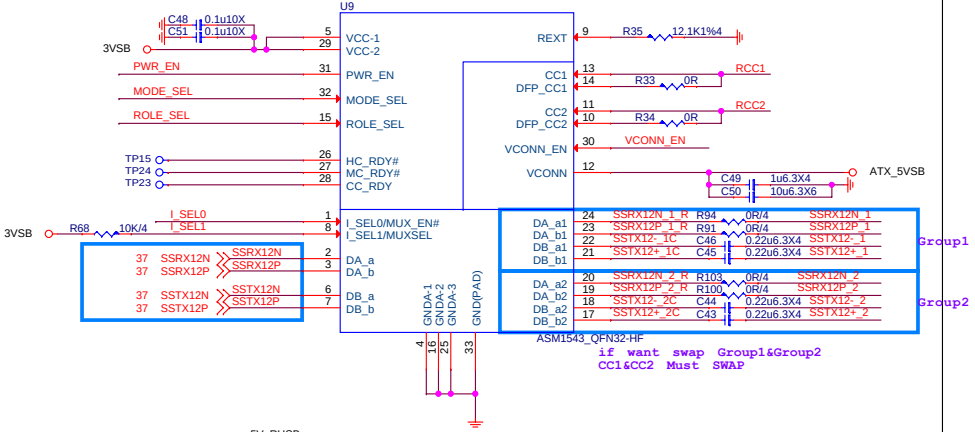
USB Type-C MUX with Configuration Channel (CC)

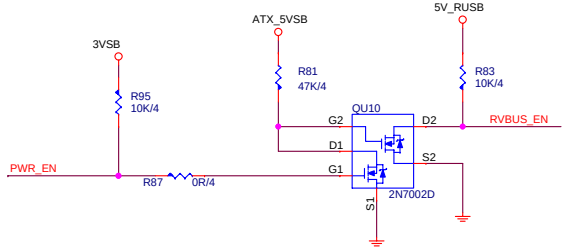


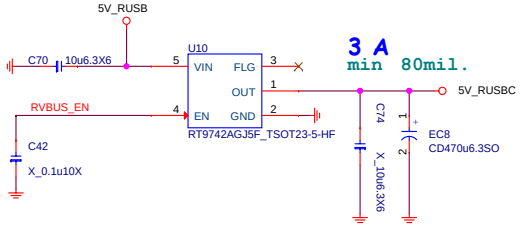
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

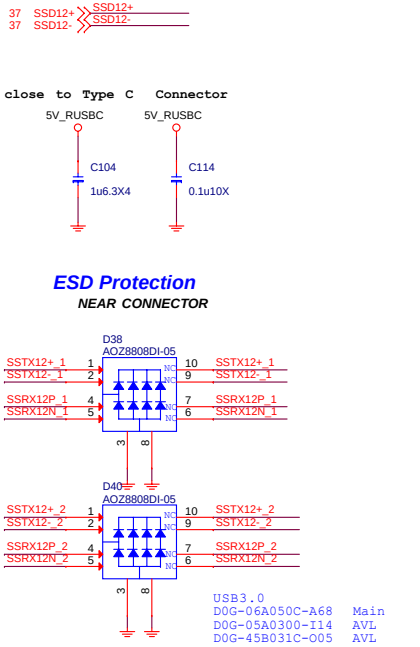
VCONN_EN	
1	enable
0	disable

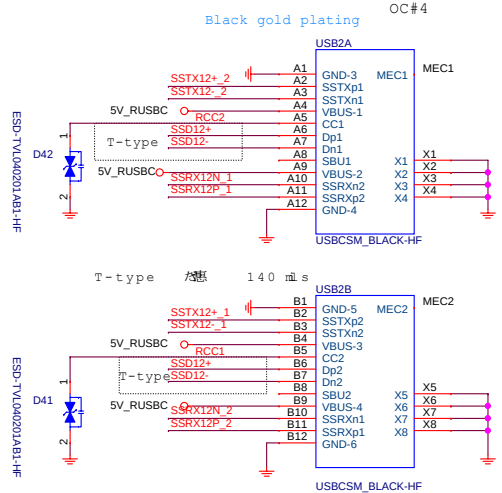






TYPE-C





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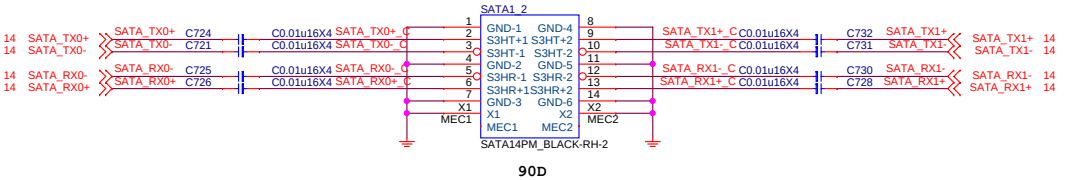
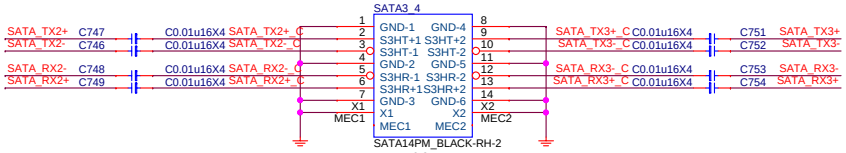
SATA Connector

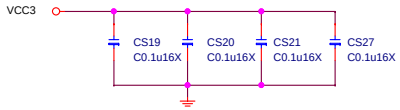
1.2V delay from 3.3V 90% > 0ms

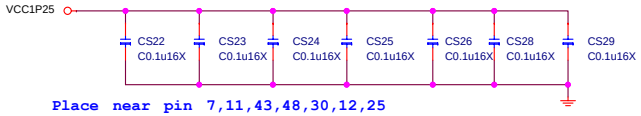
ASM1061 POWER Consumption

	3.3V	1.25V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47

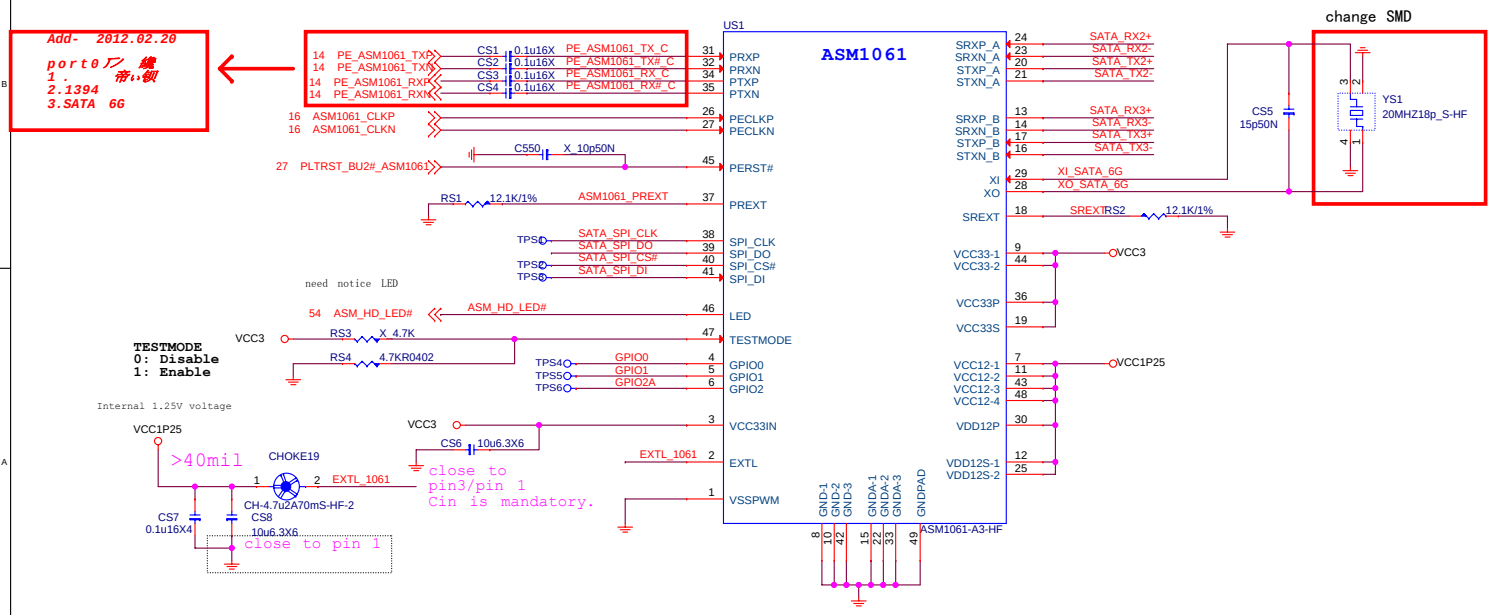




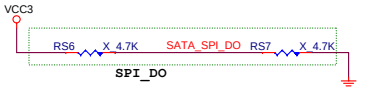




ASM1061 SATA6G



3.0



Add- 2011.3.18

SATA_SPI_DO don't need pull up (integrated pull-up) or pull down for Asmedia recommendation.
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.

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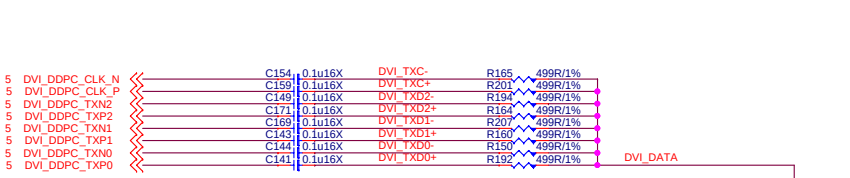
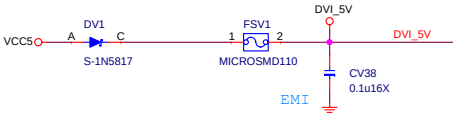
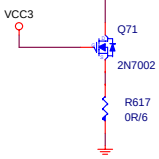
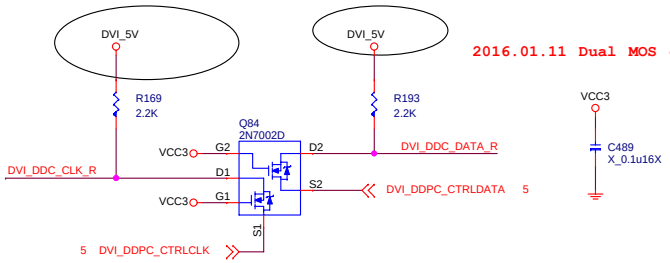
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

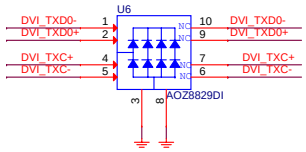


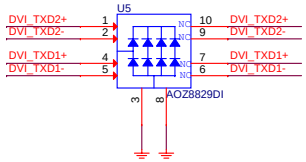


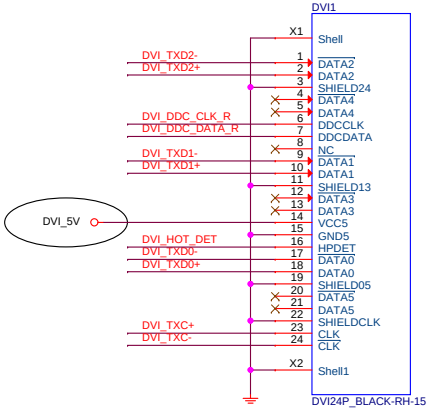


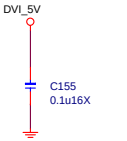


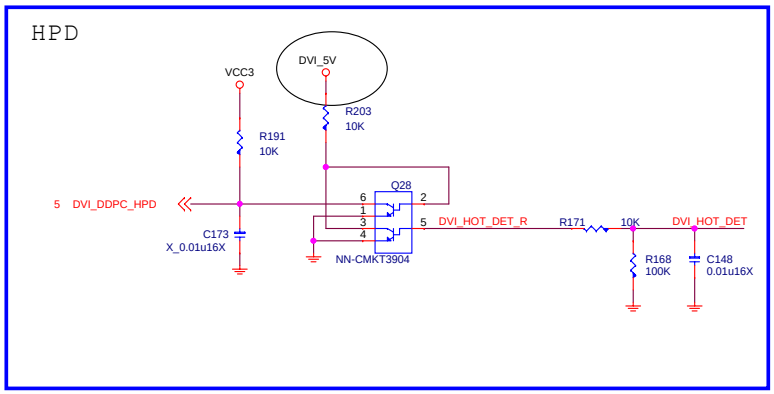
2016.01.11 Dual MOS change to single MOS,reduce CM noise by EMI Suggestion

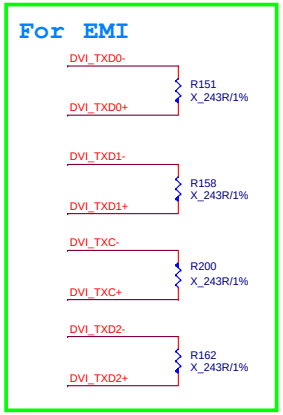


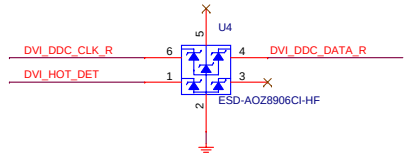


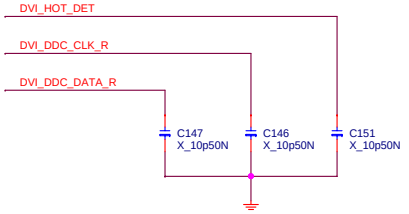












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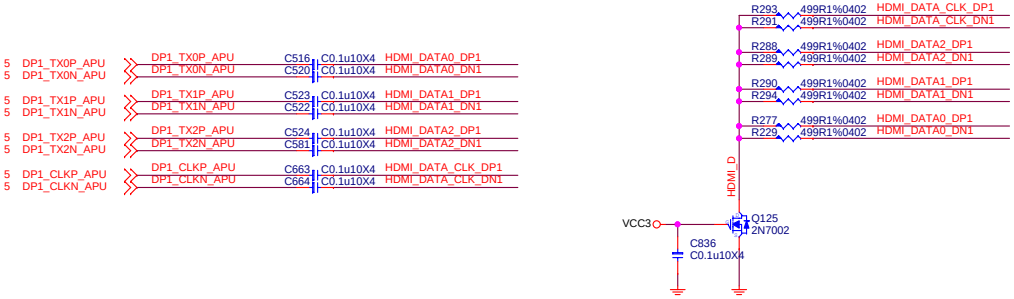
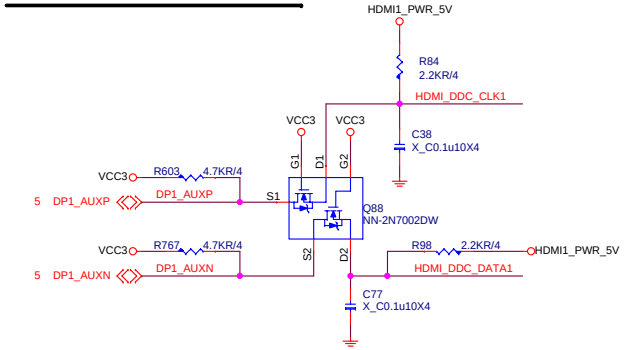
HDMI CONNECTOR

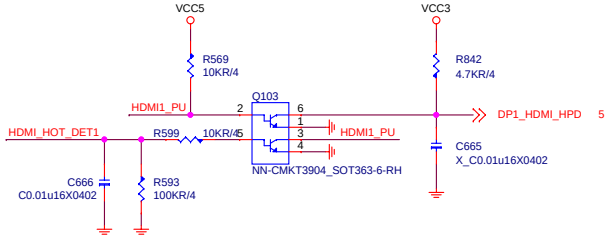
For HDMI 1.4



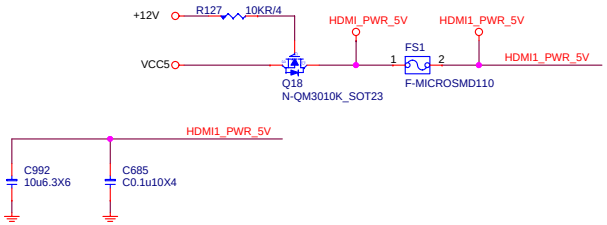
AUX Level Shifter



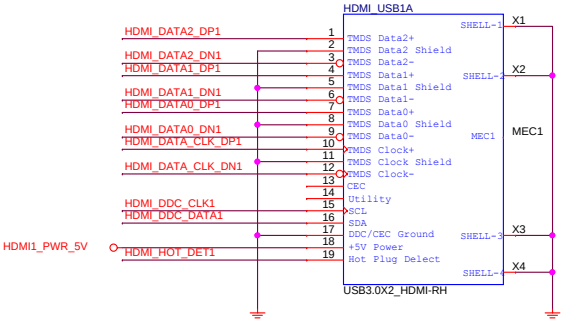
HPD Circuit



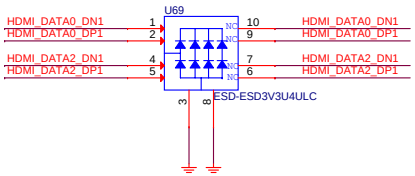
Connector Power

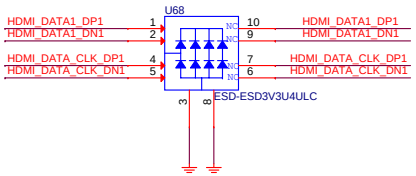


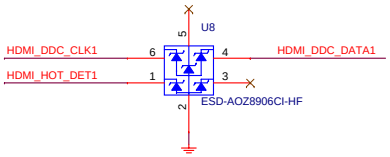
Connector

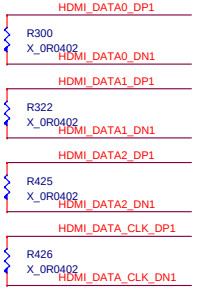


For EMI









MICRO-STAR INT'L CO.,LTD

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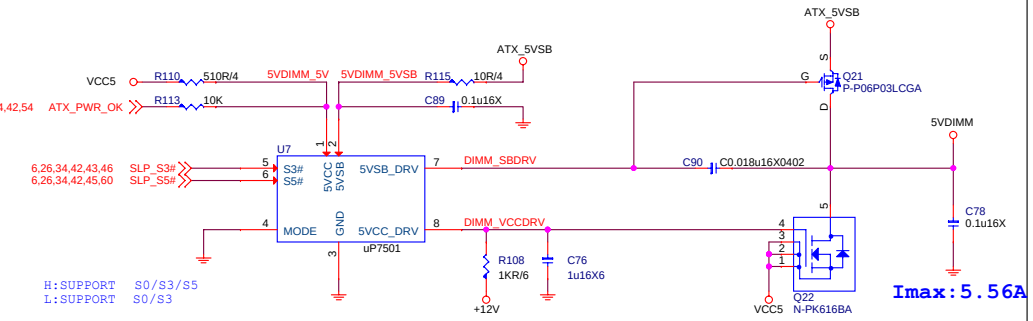
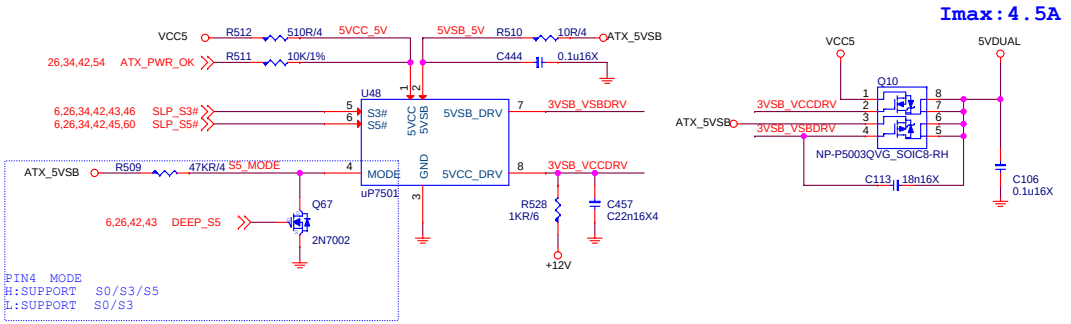
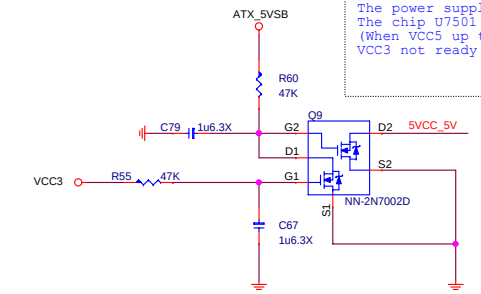
5VDIMM FOR DDR



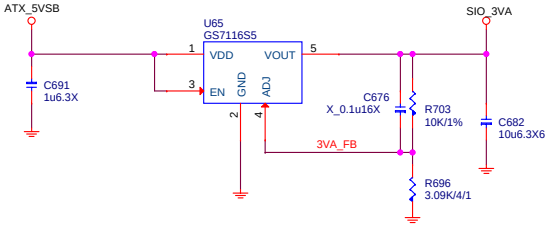
5VDUAL For 3VSB CPU 1.8V VDDP



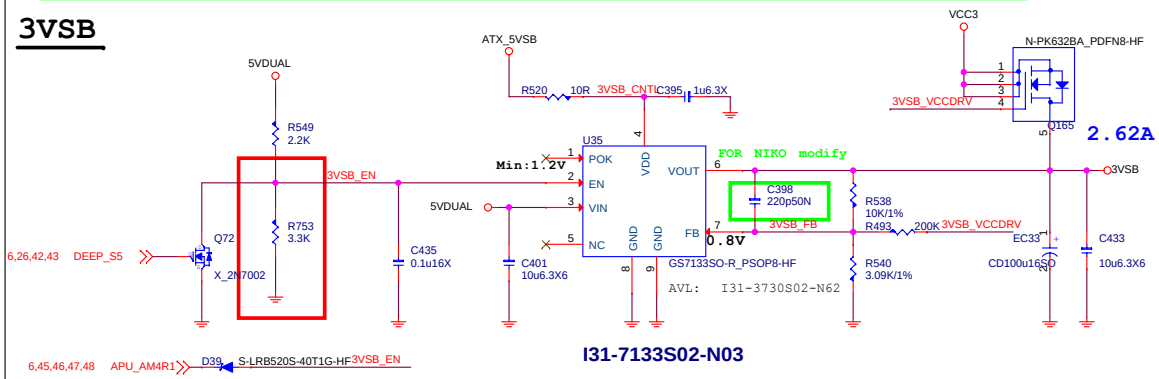
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

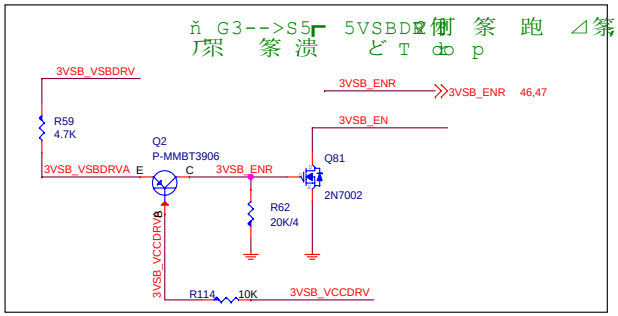


SIO_3VA



3VSB





MICRO-STAR INT'L CO.,LTD		
MS-7B00		
Size: Custom	Document Description: ACPI uPI-5VDIMM&3VSB	Rev: 11
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FOR Promontory 1.05V_S0

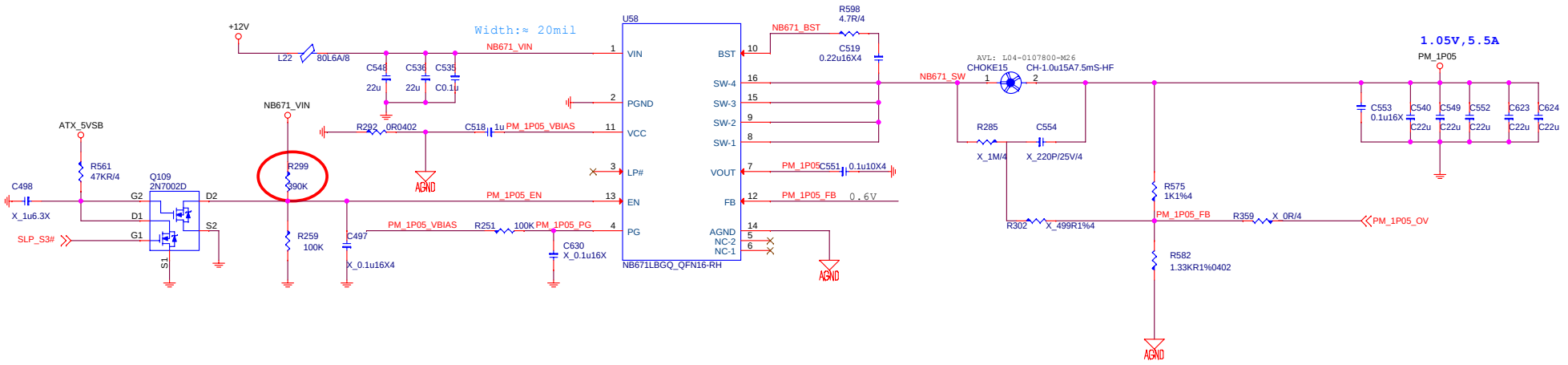
support 0V=>NB685
not support 0V=> NB681

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH<L<1.1664u H

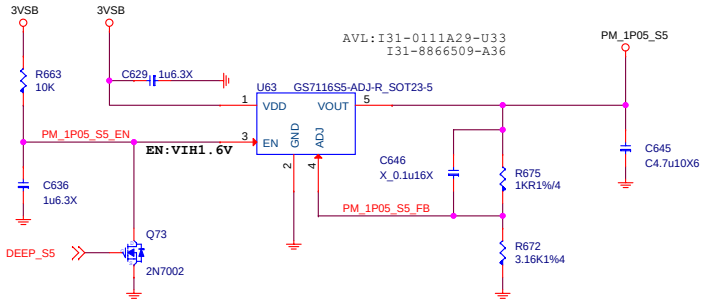
1.05V
S0:5.5A
S5:0.05A

F:500K



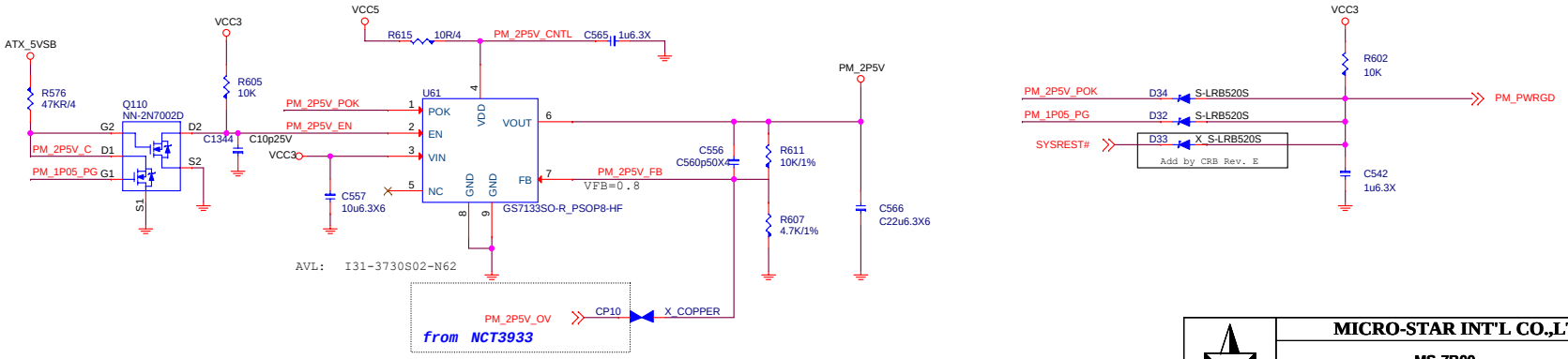
FOR Promontory 1.05V_S5

0.05A



Promontory-2.5V

2.5V; 900mA



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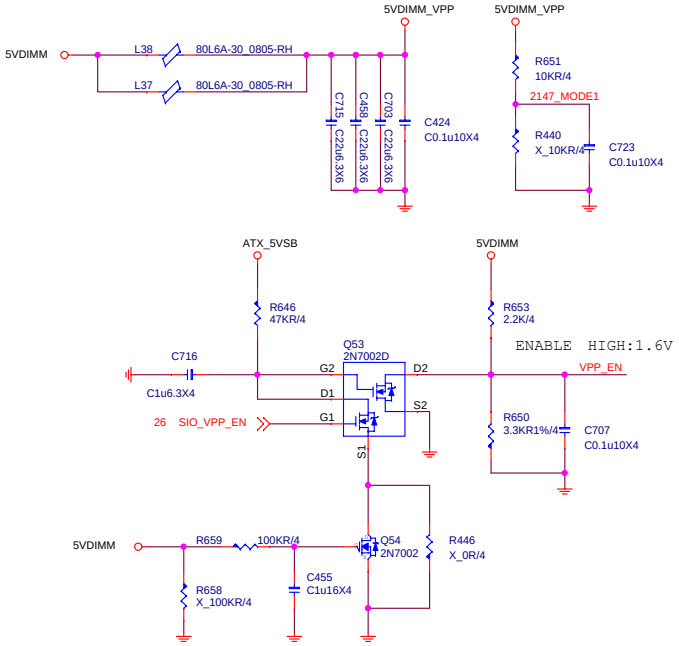
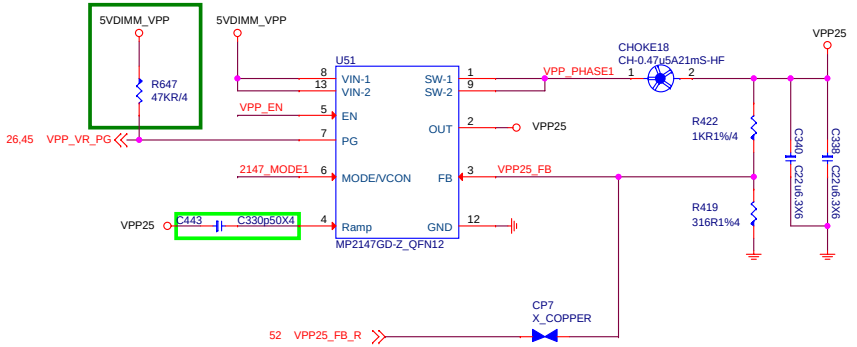
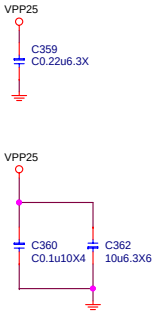
4DIMM :2.24A FOR DDR VPP2.5V

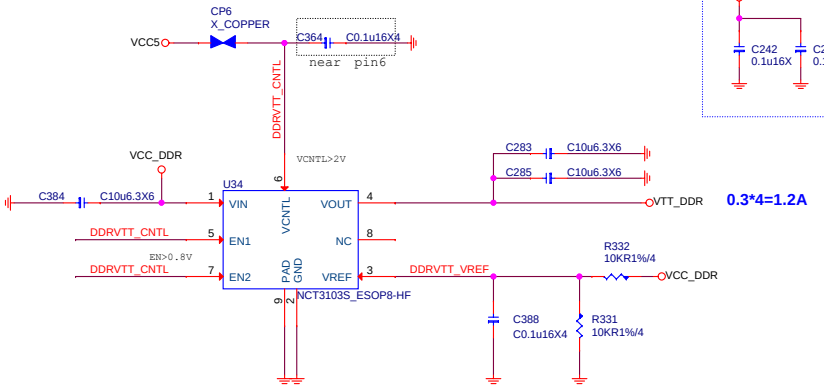


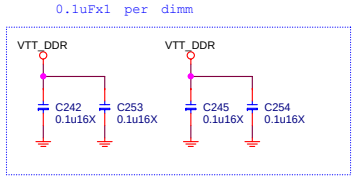


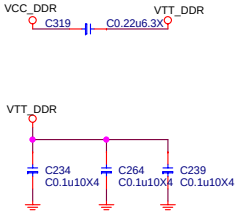


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .







MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7B00	
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DDR4_1.2V 15.5A+9.5A+1.2A=26.2A

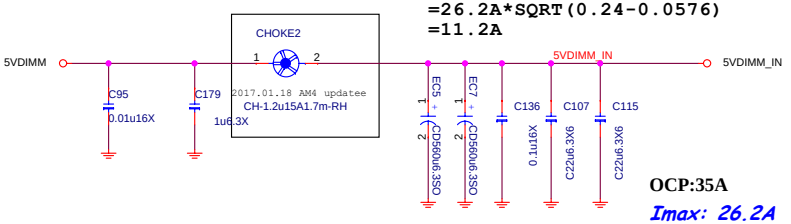
15.5A FOR CPU

9.5A FOR 2DIMM

1.2A FOR DDR VTT

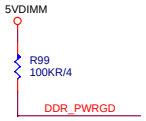
VID	Reference Voltage (V)
H	0.675
L	0.75

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=26.2A*SQRT(0.24-0.0576)
=11.2A



OCP:35A

Imax: 26.2A



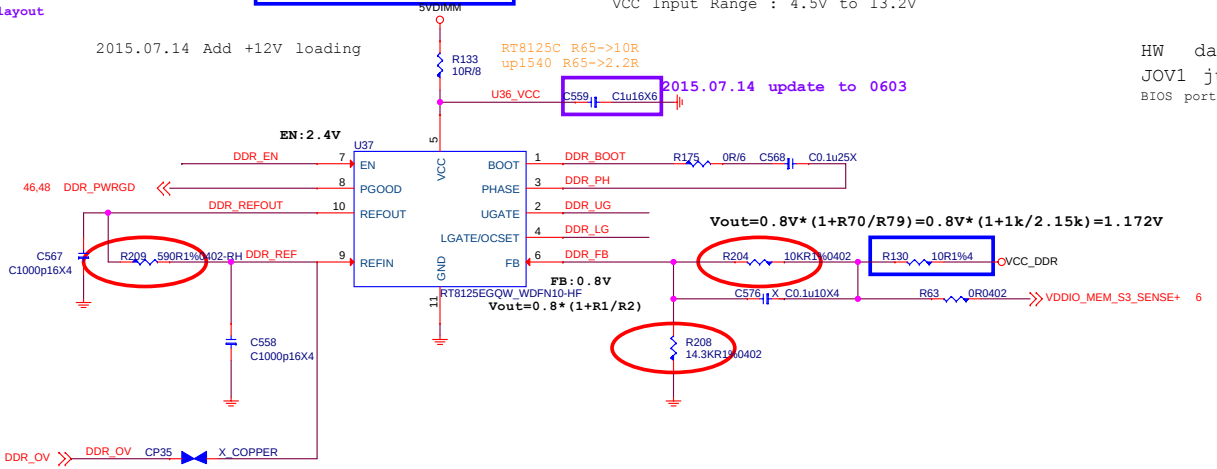
Pull up change by layout

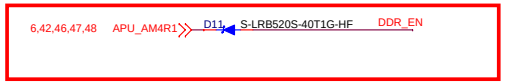
20151230 Update

uP1504 & RT8125
VCC Input Range : 4.5V to 13.2V

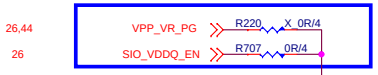
2015.07.14 Add +12V loading

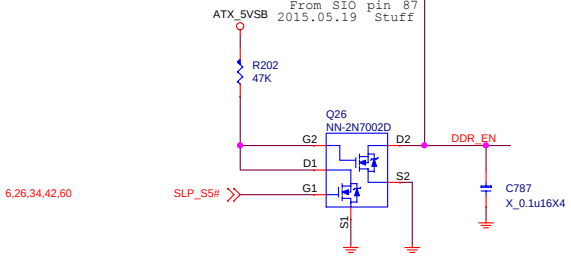
HW dafault 1.36V
JOV1 jump 1.4V
BIOS porting SPD voltage

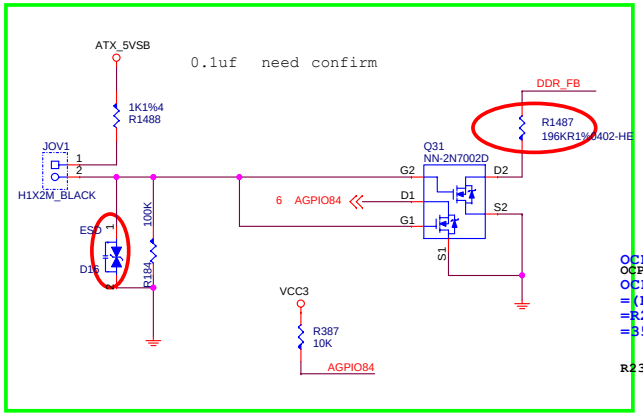




20170228 remove Q26

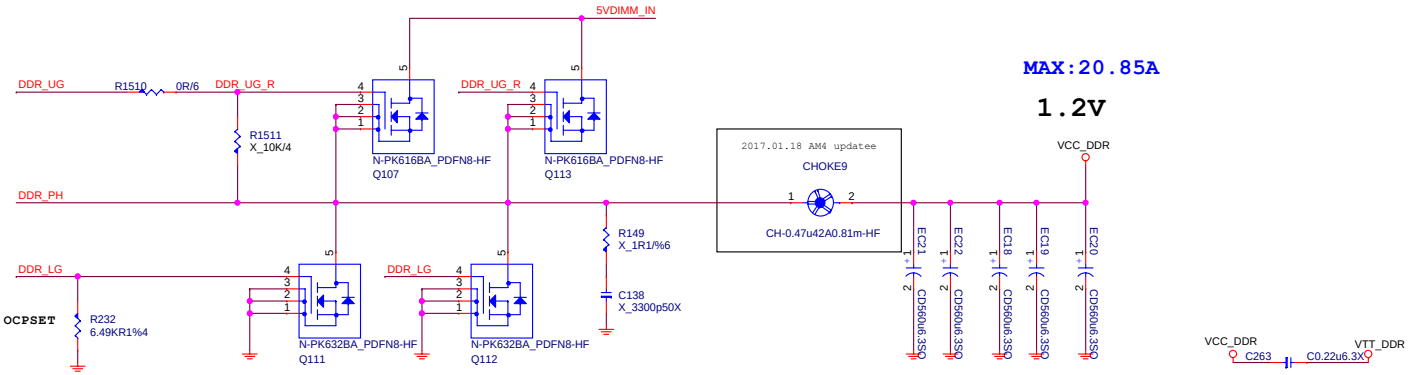






OCP=35A
OCPSET:min 5Kohm
OCP
=(R232*10uA)/Rdson
=R232*10uA)/3.3m/2
=35A

R232=5.775k



MAX:20.85A

1.2V

MICRO-STAR INT'L CO.,LTD

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FOR CPU 1.8V S5

0.5A

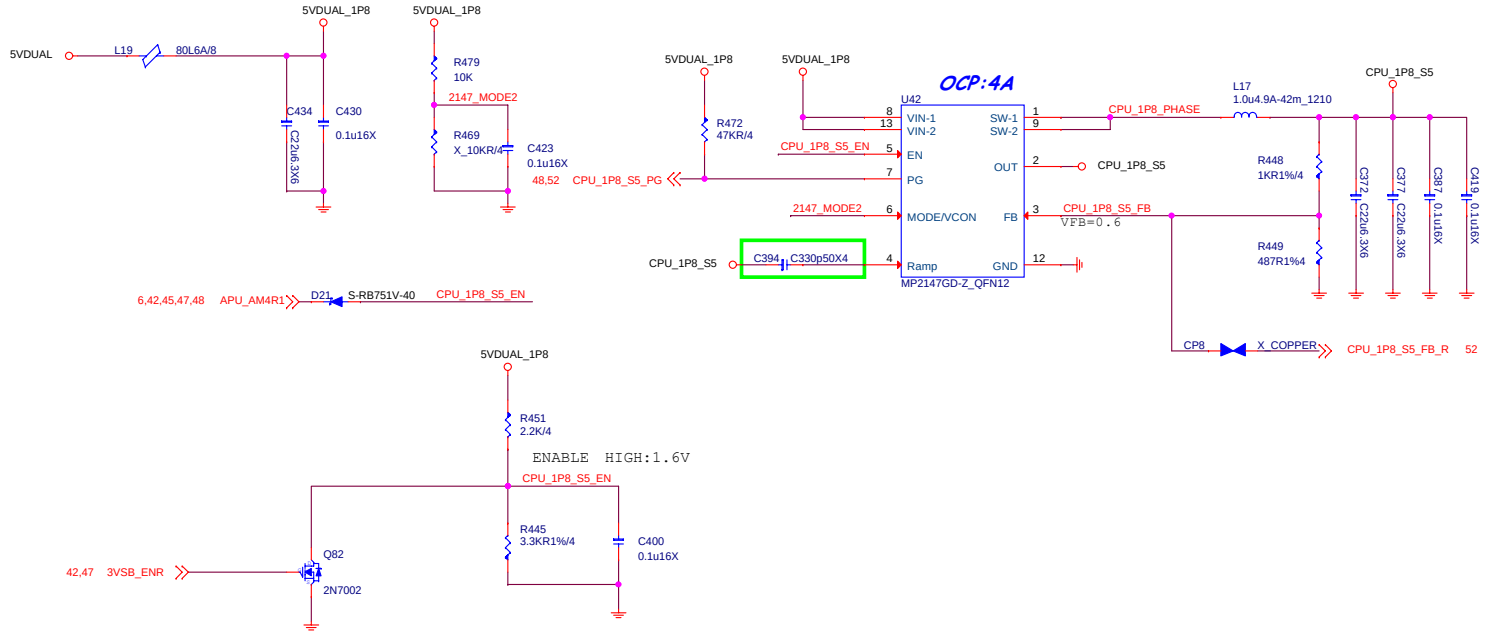
FOR VCCP_SOC_S5

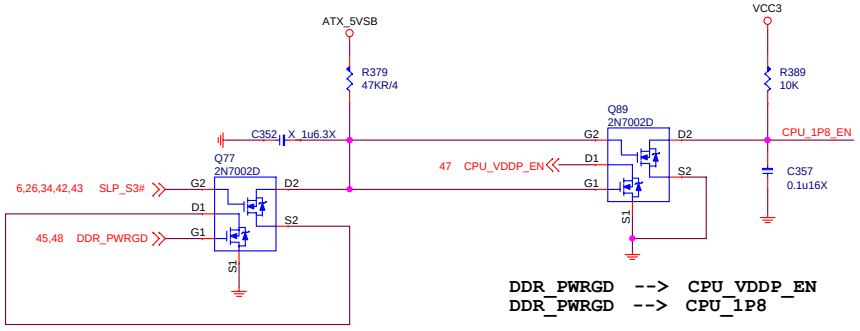
0.9A

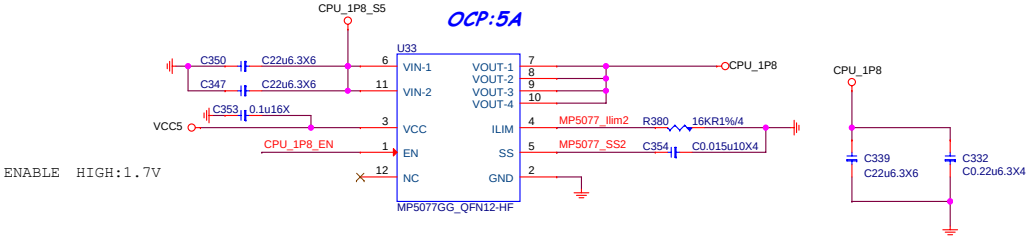
FOR CPU 1.8V S0

2.0A

0.5A + 2.0A + 0.9A =3.4A







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	MS-7B00	
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CPU_VDDP_S0

1.05V/0.9
S0:8.5A

by layout

+12V

R406 100K1%4 EN:VIH1.6V

CPU_VDDP_EN

R418 33K/1%

C389 0.1u16X

VCC5

R437 10K

48 CPU_VDDP_PG

6,42,45,46,47,48 APU_AM4R1

D20 S-LRB520S

CPU_VDDP_EN

EN:VIH1.6V
EN pin Maximum:6.5V

U41

R494 10R/8

U6_VCC C429 C1u16X6

EN PGOOD REFOUT REFIN VCC GND BOOT PHASE UGATE LGATE/OCSET FB

CPU_VDDP_BOOT1 R484 0R/6 C440 0.1u16X25

CPU_VDDP_PH1

CPU_VDDP_UG1

CPU_VDDP_LG1

CPU_VDDP_FB

RT8125EGQW_WDFN10-HF

CPU_VDDP_REFOUT

C426 C1000p50X4

R453 768R1%4

CPU_VDDP_REFIN

C374 C1000p50X4

R463 4.53KR1%4

0.8V
0.684V

FB:0.8V

CPU_VDDP

R420 10R1%0402

R438 1KR1%/4

CPU_VDDP_SENSE_R R421 0R/4 CPU_VDDP_SENSE 6

C399 X_0.1u16X

R450 3.16K/1%

AM4_CPU_SEL
0:Type 0/1 1.05V
1:Type 2/3 0.9V

Q86 NN-2N7002DW

5,6,35,47,48,52 TYPE1_CPU_SEL

16 PM_GPIO_R9

52 CPU_VDDP_OV

CP25 X_COPPER

PM_GPIO_R9
1:Type 0/1 1.05V
0:Type 2/3 0.9V

2017.01.18 AM4 updatee

3VSB

1K1%4 R339

JOV2 H1X2M_BLACK

26 SIO_GP10

Q149 2N7002

R212 2.26KR1%0402

ESD D57 R185 100K

0.1uf need confirm

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 8.5*0.2823
= 2.4A

TYPE0_CPU_SEL:
1:TYPE 0
0:TYPE 2

CPU_VDDP_EN:
0:TYPE 2
1:TYPE 0

Q92 NN-2N7002DW

6,48 TYPE0_CPU_SEL

VDDP_SEL

5,6,35,47,48,52 TYPE1_CPU_SEL

CPU_VDDP_EN CPU_VDDP_EN 46

TYPE1_CPU_SEL:
0:TYPE 0
1:TYPE 2

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

12VCC_IN

CHOKE14 CH-0.47u5A21mS-HF

+12V

C461 C1u16X6 C460 22u16X8 EC11 CD270u16SO C446 0.1u16X

CPU_VDDP_UG1 R508 0R/6 CPU_VDDP_UG1_R

R500 X_10KR/4

N-PK616BA_PDFN8-HF Q97

CPU_VDDP_PH1

CPU_VDDP_LG1

OCP=12A

OCPSET:min 5Kohm

OCP
=(R475*10uA)/Rdson
=(5.1k*10uA)/3.3m
=15.45A

R475 5.1K/1%/4

N-PK632BA_PDFN8-HF Q96

R482 X_2.2R/8

snubber

C437 X_C3300p50X4

CHOKE13 1.0u15A7.5mS-HF

CPU_VDDP

C334 1u6.3X C425 C22u6.3X6 EC31 CD560u6.3SO EC32 CD560u6.3SO

OCP=12A
1.05V,8.5A

CPU_VDDP_S5

VDDP_S5 1.05V/0.9
S5:1A

3VSB 3VSB 5VDUAL

L20 80L6A/8

R501 X_10KR/4 R502 10K

C439 C22u6.3X6

U45 MP2143DJ

VDDP_VSB_VIN VDDP_VSB_EN VDDP_VSB_PG

48 VDDP_VSB_PG

Internal Pull-Up 500K

VDDP_VSB_PHASE

L18 1.0u5.5A-35_1210-HF

CPU_VDDP_S5

R489 1KR1%/4

R488 2KR1%/4

C412 C22u6.3X6 C421 C22u6.3X6 C427 C0.22u6.3X4

VDDP_VSB_FB

6,42,45,46,47,48 APU_AM4R1

D28 S-LRB520S

VDDP_VSB_EN

C390 X_0.1u16X

42,46 3VSB_ENR

Q98 2N7002

ATX_5VSB

R490 47KR/4

Q95 NN-2N7002DW

C436 0.1u16X

5,6,35,47,48,52 TYPE1_CPU_SEL

AM4_CPU_SEL
0:Type 0/1
1:Type 2/3

R464 3.83KR1%4

R488///R464=1.3139K, Vout=1.056V
R488=8.06K, Vout=0.9V

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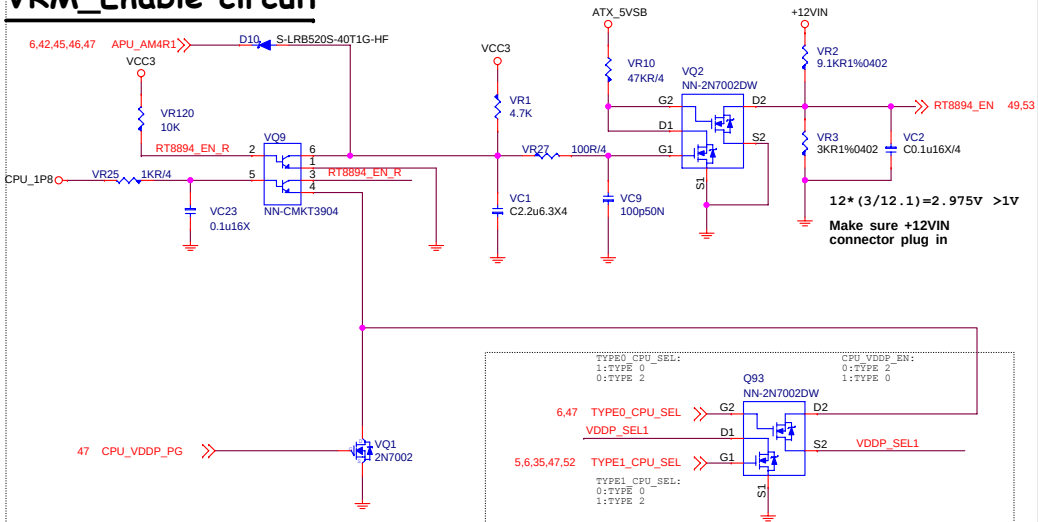
VRM_Enable circuit

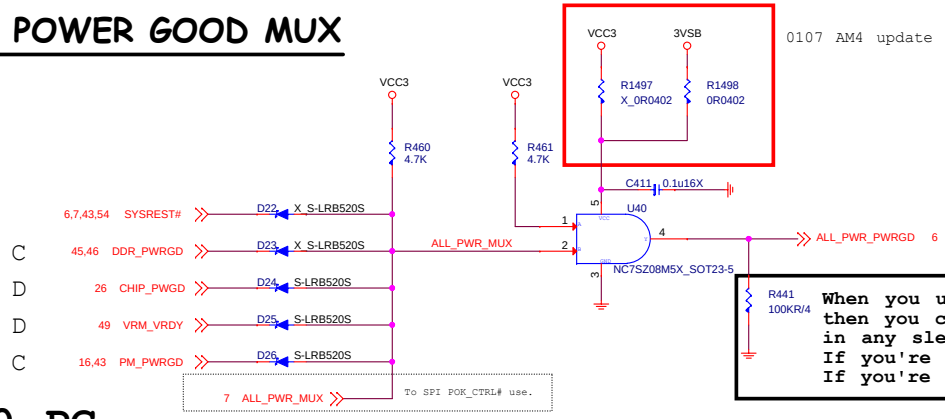


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

0107 AM4 update

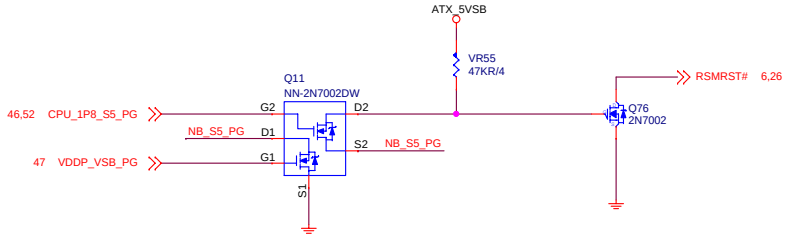


R441 100KR/4

When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



MICRO-STAR INT'L CO.,LTD		
MS-7B00		
Size: Custom	Document Description: CPU Power Connector/PWRGD	Rev: 11
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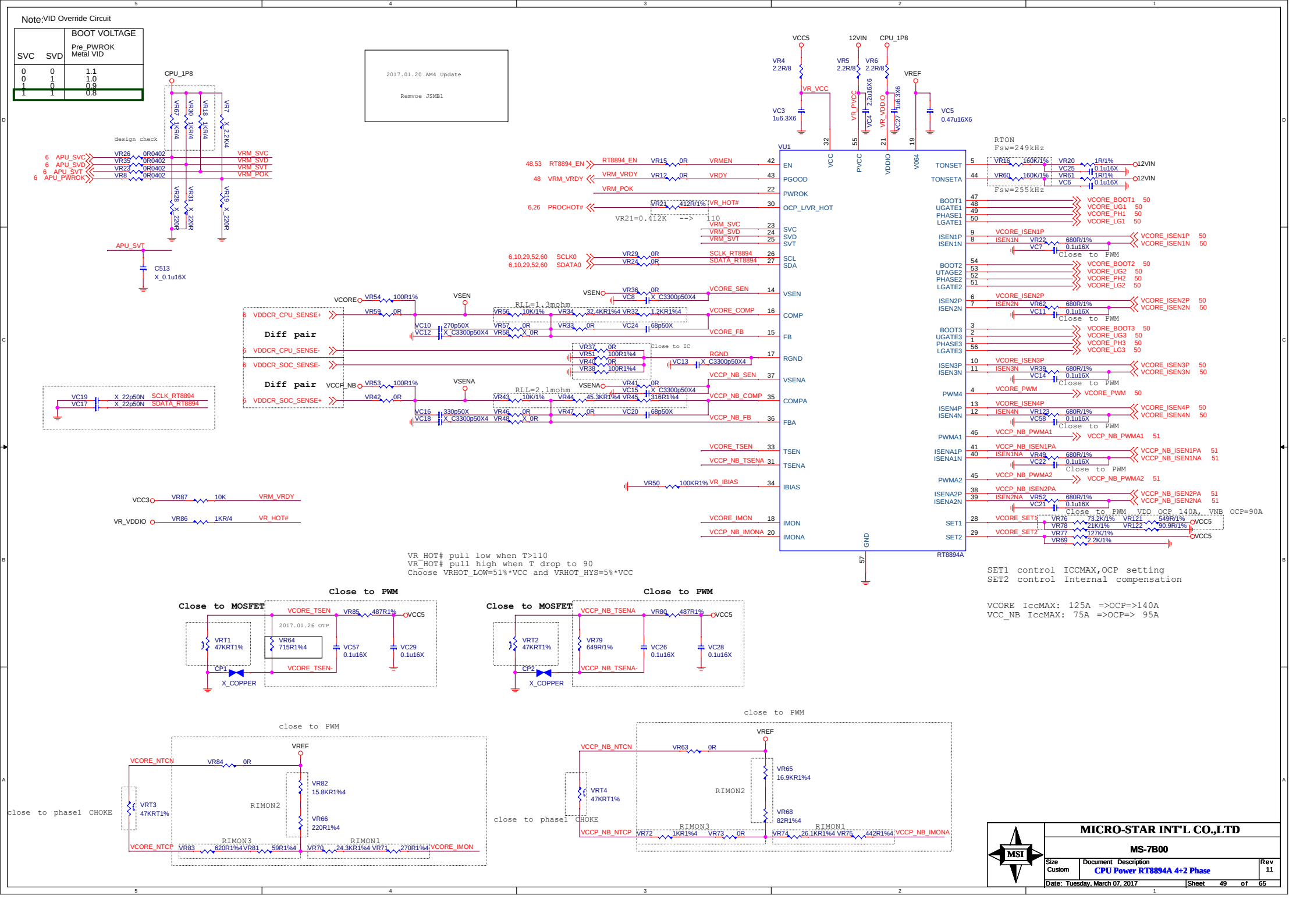
Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

2017.01.20 AM4 Update

Remvoe JSMB1



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU Power RT8894A 4+2 Phase	11

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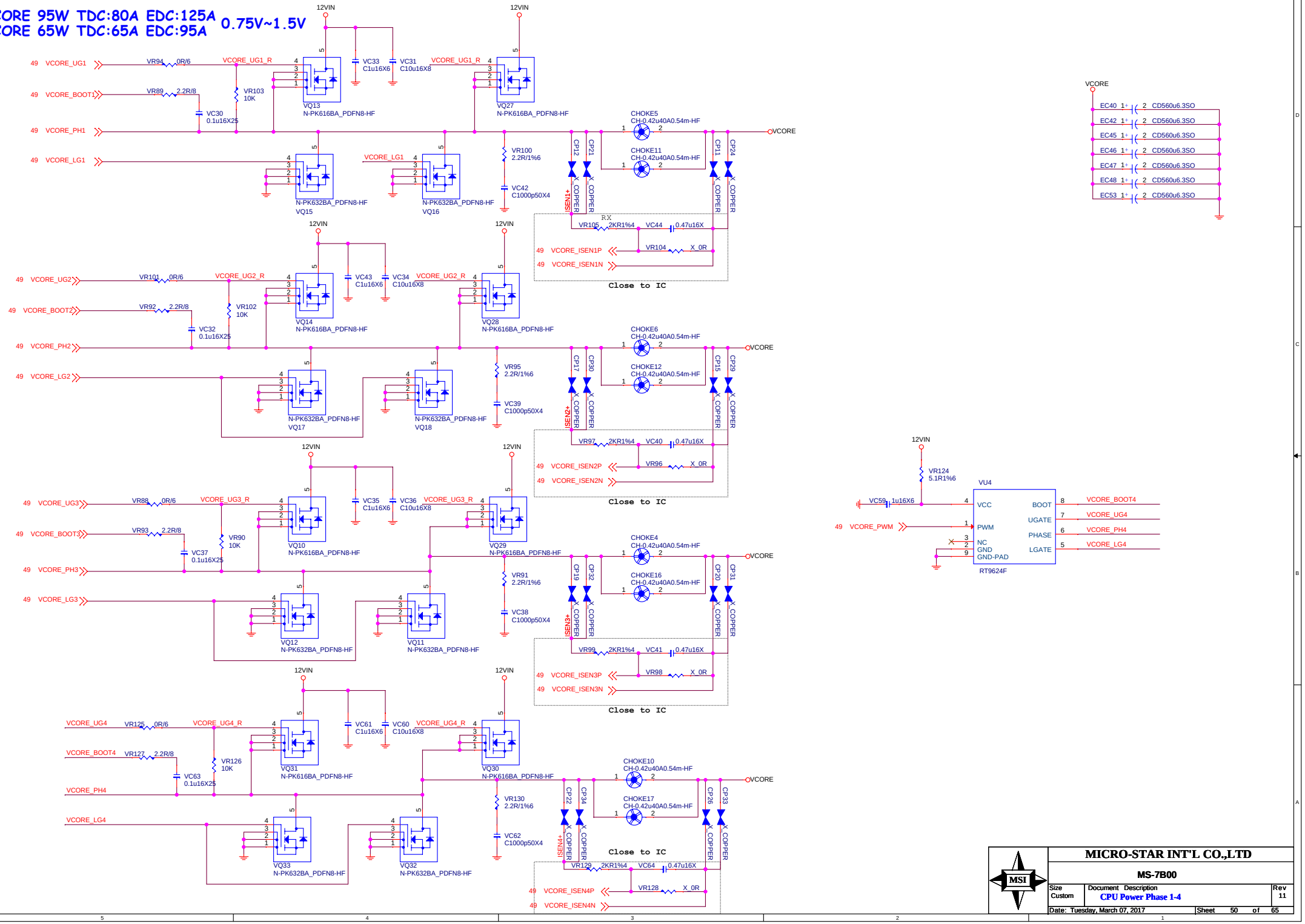
VCORE 95W TDC:80A EDC:125A 0.75V~1.5V
VCORE 65W TDC:65A EDC:95A



MICRO-STAR INT'L CO.,LTD	
MS-7B00	
Size: Custom	Document Description: CPU Power Phase 1-4
Rev: 11	
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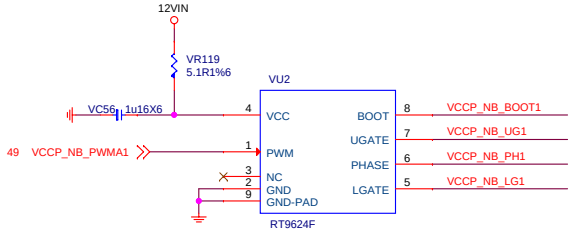
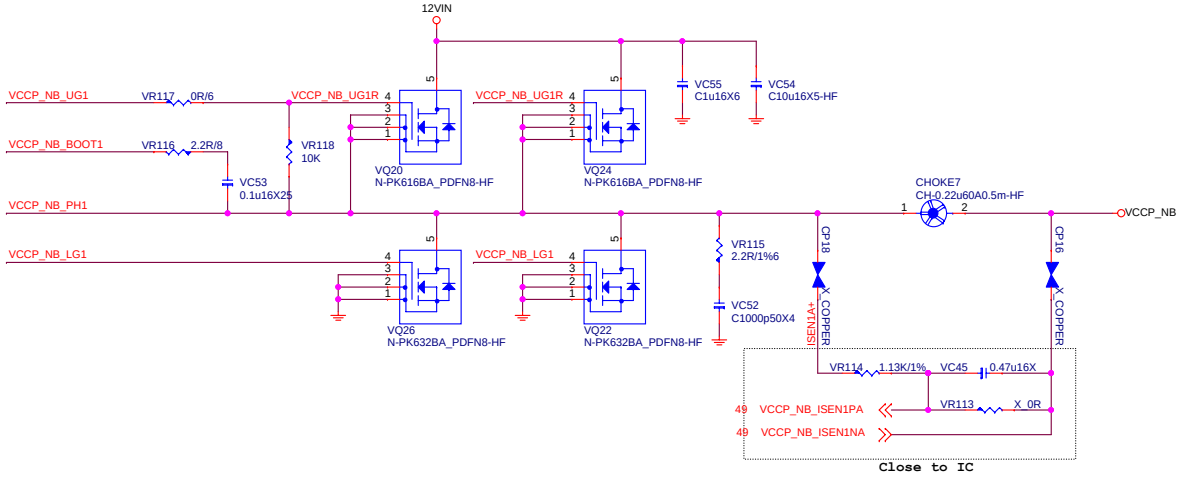
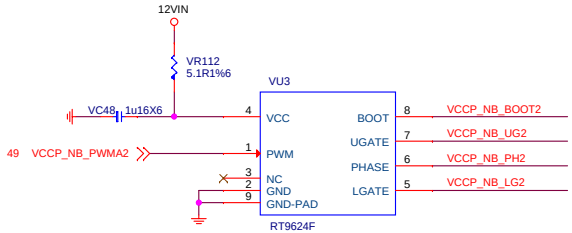
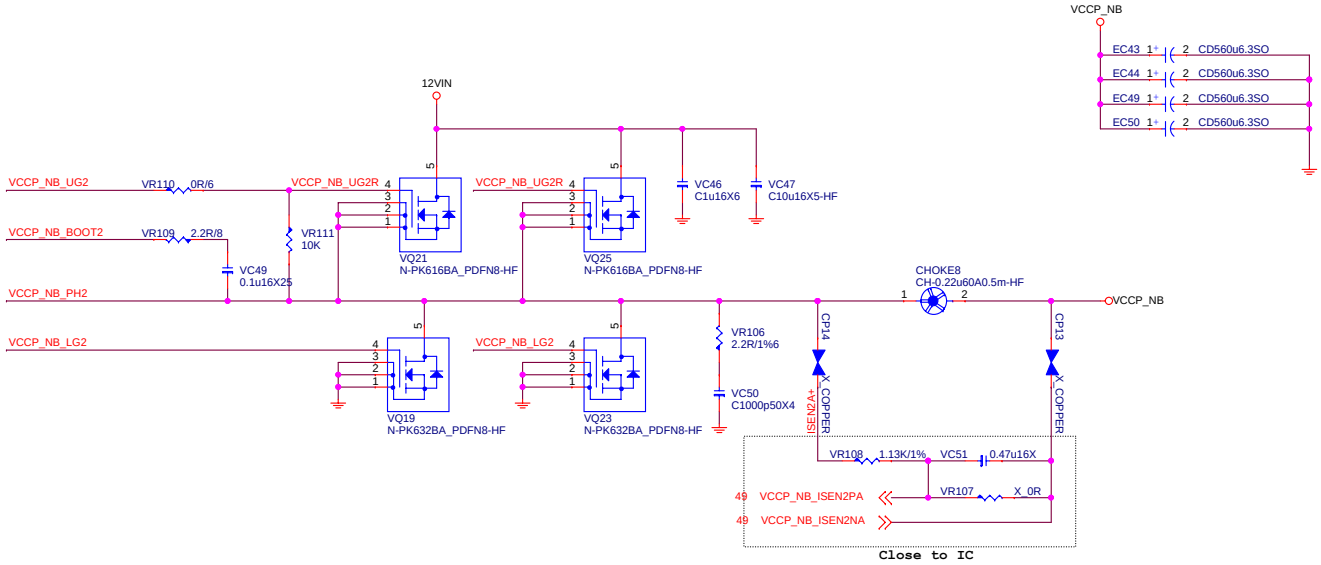
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

0.75V~1..2V









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FOR VCCP_SOC_s5
0.9A

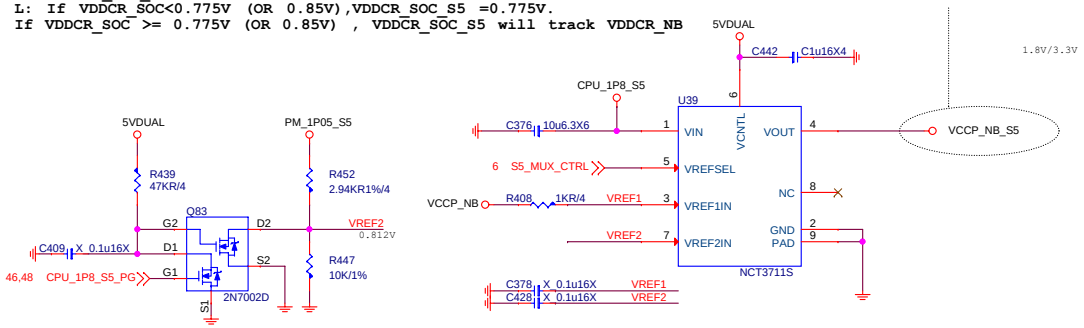
TYPE0 Only

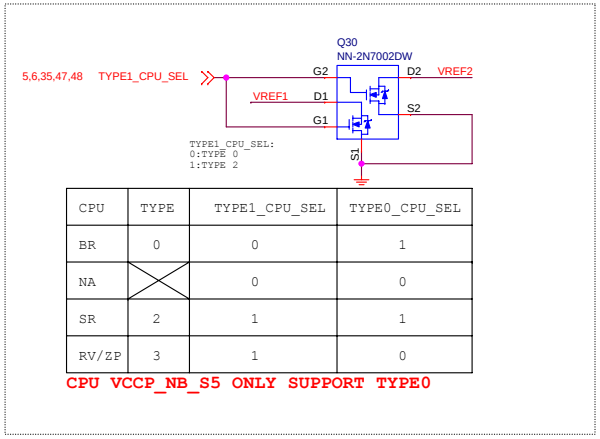
S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)

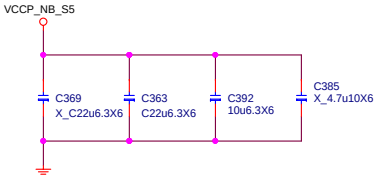
Bristol Ridge TYPE0



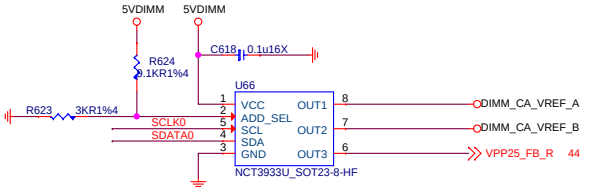


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0



0x28:RH=9.1K,RL=3K

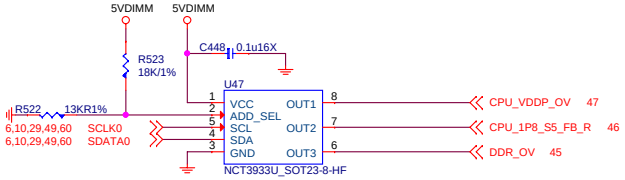


Over Voltage Control IC

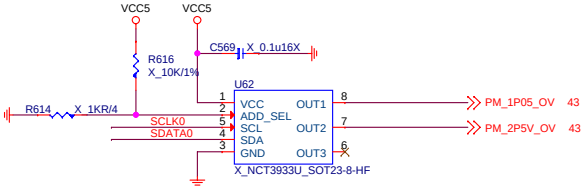
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

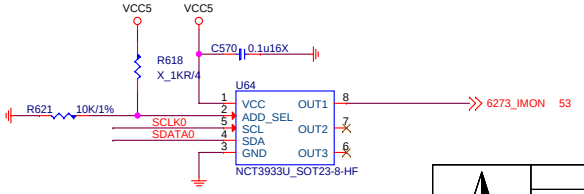
0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN



0x2A:RH=OPEN,RL=10K



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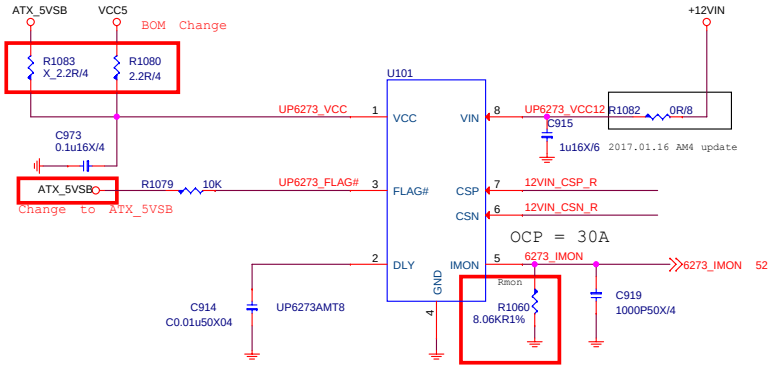
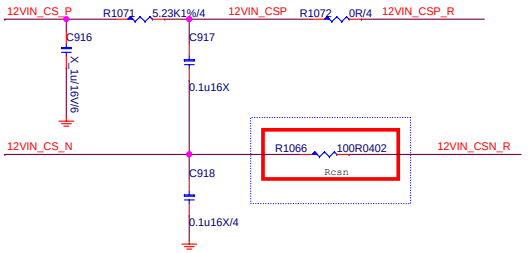
uP6273 CURRENT SENSE

VCORE EDC MAC 125A

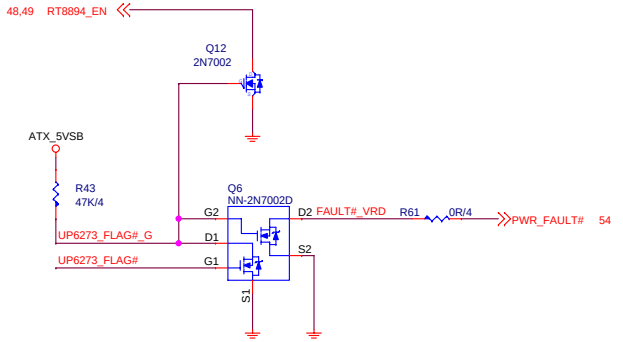
NB EDC MAX75A



Vmon = 1.2V髖ocp
Vmon=(Iin x Rdc / Rcsn) x Rmon
1.2V=30 x 0.5m /100 x Rmon
Rmon=8K



Imon= 10uA = Vin 2A (NCT3933隔軛橛
Iin x Rdc /Rcsn = Imon
2A x 0.5m / Rcsn = 10uA
Rcsn=100 ohm

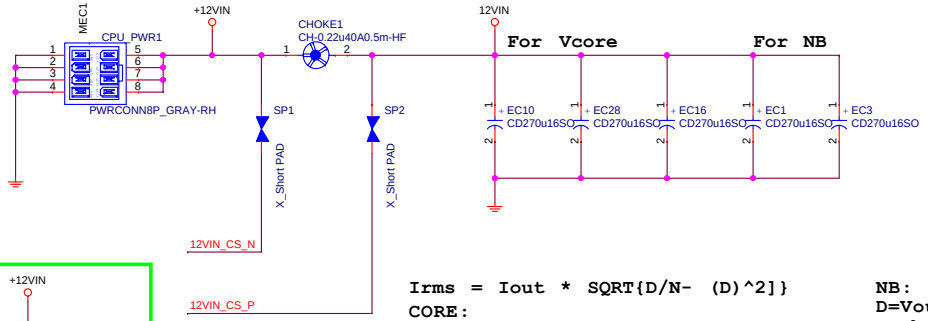


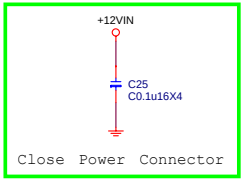
CPU POWER CONNECTOR

uP6273 CURRENT SENSE

VCORE EDC MAC 125A

NB EDC MAX75A





Irms = Iout * SQRT{D/N- (D)^2]}
CORE:
D=Vout/Vin=1.5/12=0.125
N=Phase number=4
=125A*SQRT(0.03125-0.015625)
=15.625A

Iout = 80A,Irms=10A

NB:
D=Vout/Vin=1.2/12=0.1
N=Phase number=2
=75A*SQRT(0.05-0.01)
=15A

Iout = 50A,Irms=10A

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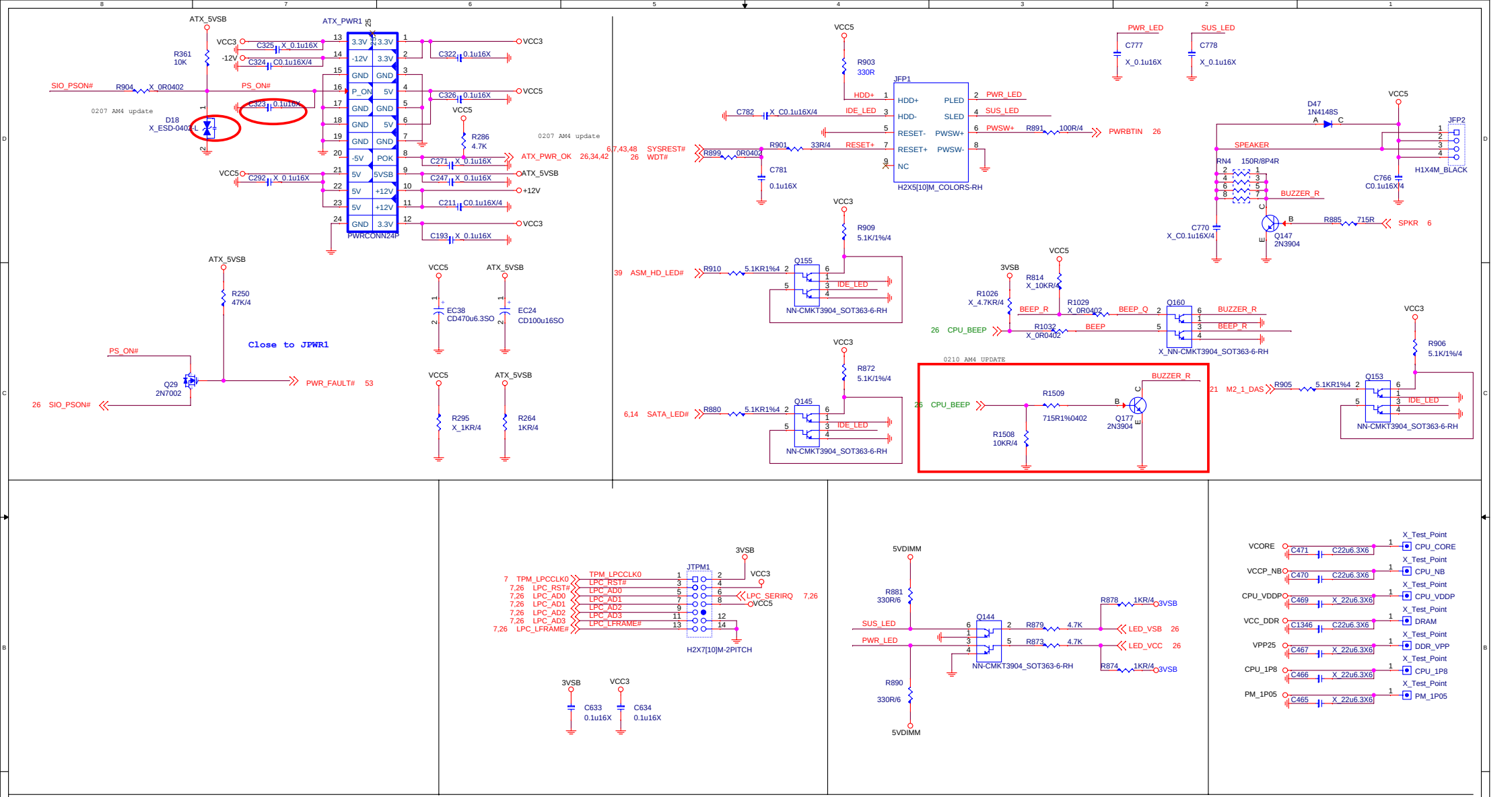

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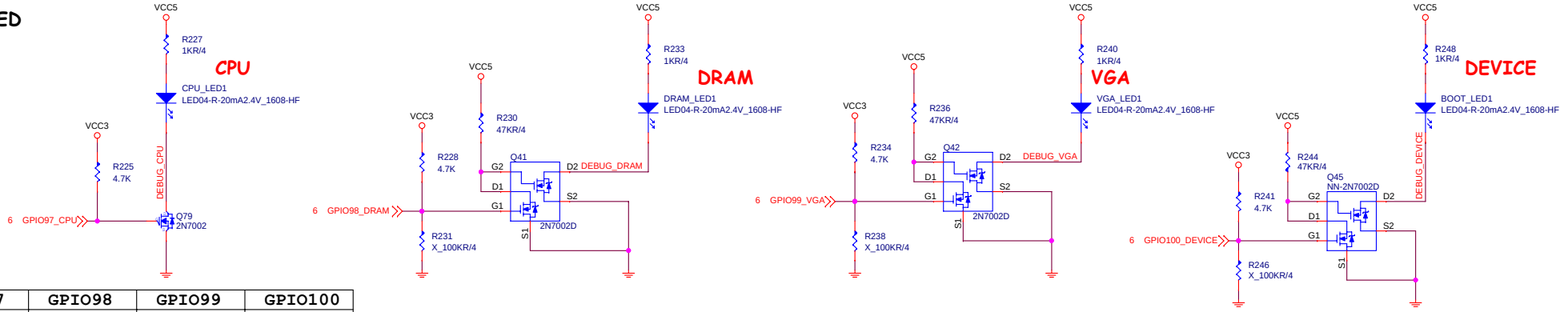
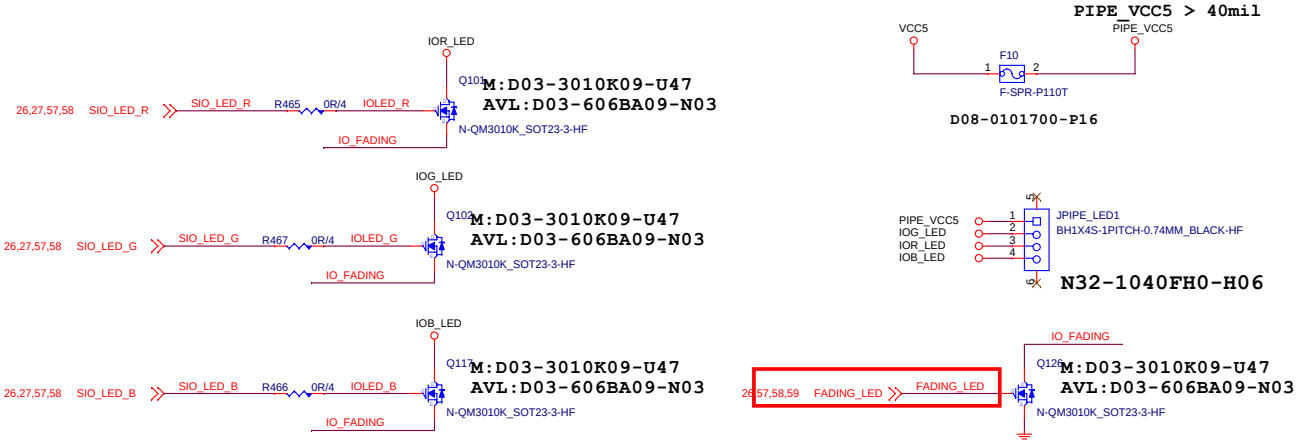
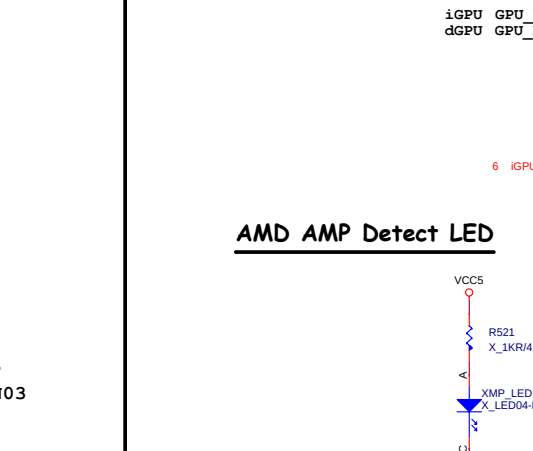
EZ Debug LED



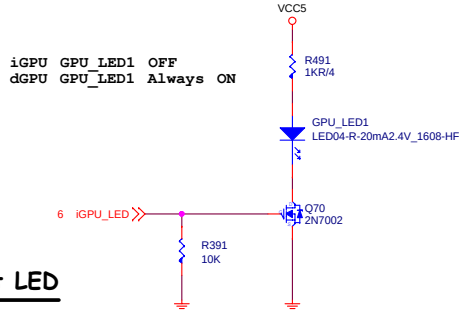
LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
獰	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

IO Cover RGB LED

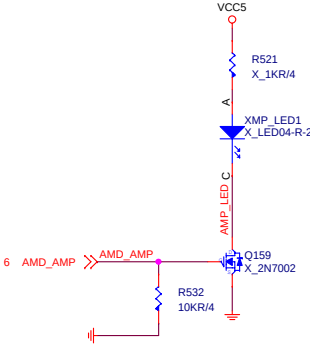




AM4 APU Detect LED Circuit



AMD AMP Detect LED



LED	x16	x8	x4
PCIE2	Red	White	White

LED \ GPIO	EGPIO95	EGPIO96
獰	GPO PO HIGH	GPO PO HIGH
防	GPI (default LOW)	GPI (default LOW)

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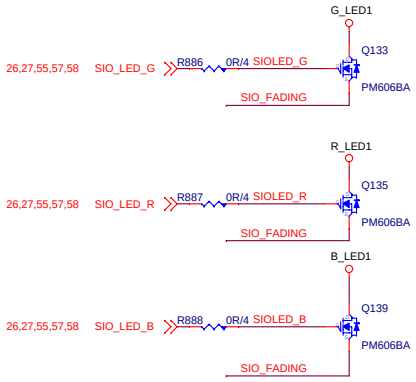
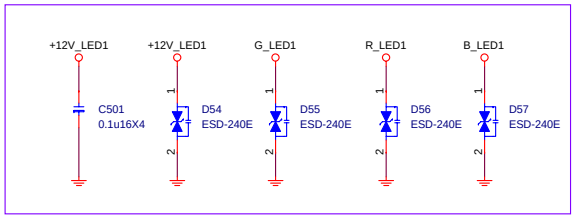
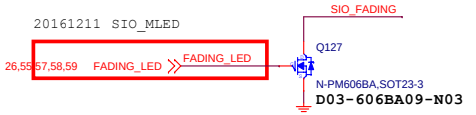
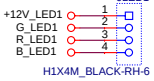
LED STRIPLINE(LEFT)



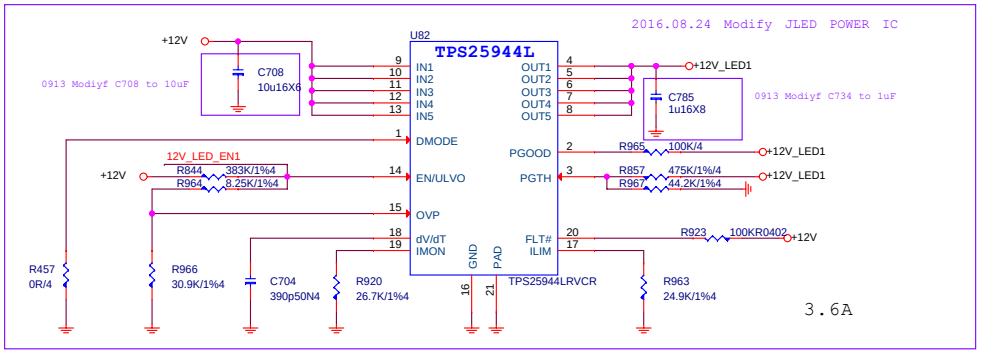
2016.08.24 Add,Close to JLED1





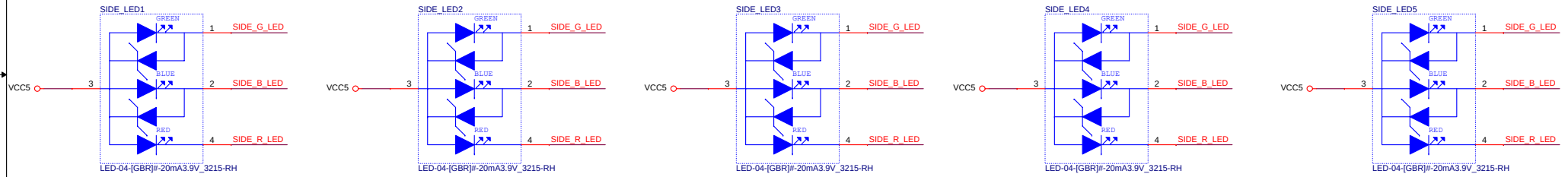


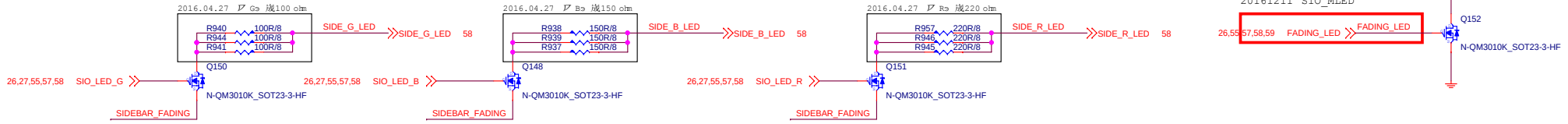
2016.08.24 Modify JLED POWER IC



钡LE 繈 兵 （ RG B ）
---- PCB ゅ琰 (JLED1)
---- も 爹 **繈** や穿 夹非 505 **R** GB LED 繈兵 (1 **■**繈兵黑 块 篆琛 综 成 3 蚌 （12 ヱ 疯），
繈戕 ぞへ沈 7A20 嘈**鑾**

BOARD SIDE LED





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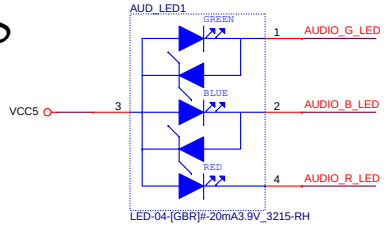
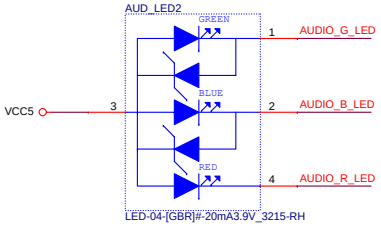
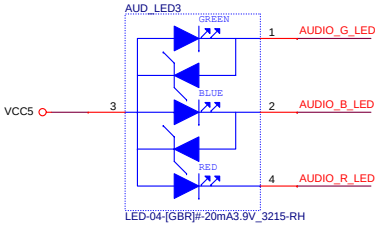
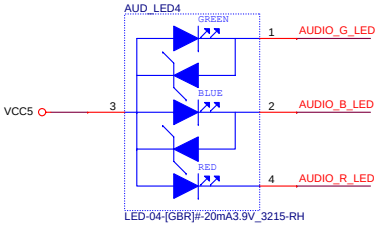
AUDIO_MOAT LED

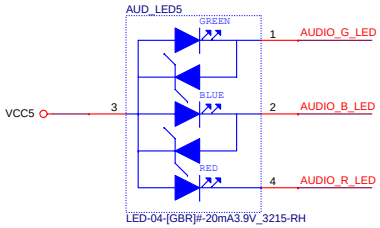
LEFT

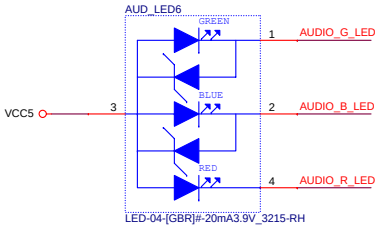


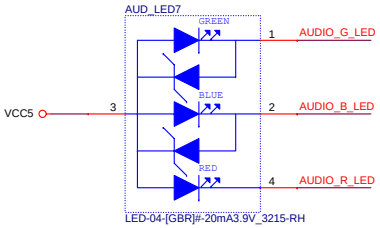


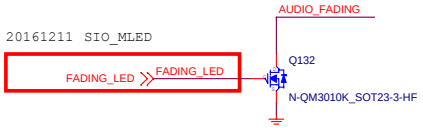


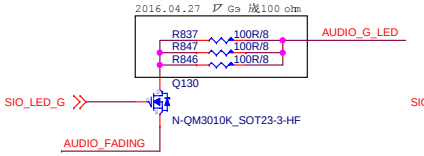


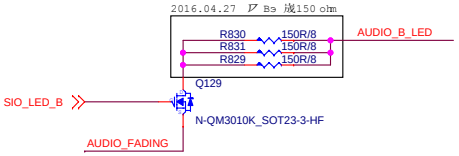


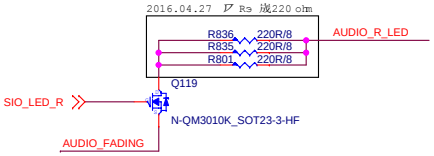




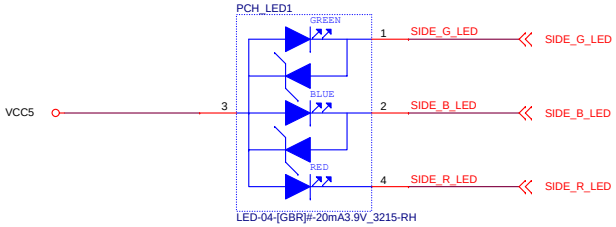


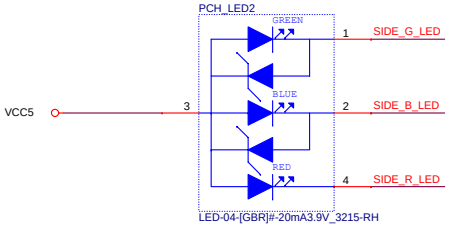


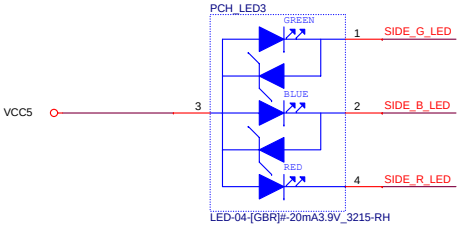


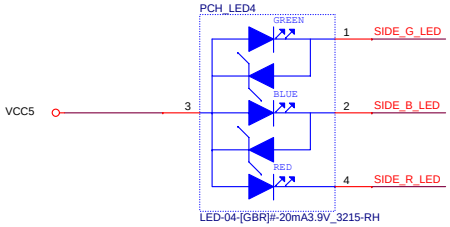


PCH LED









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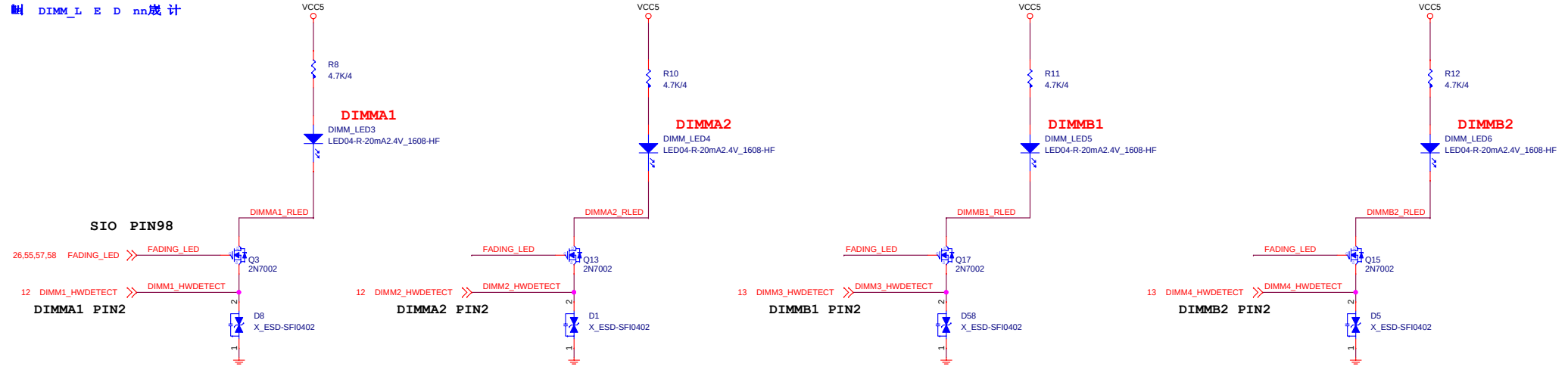
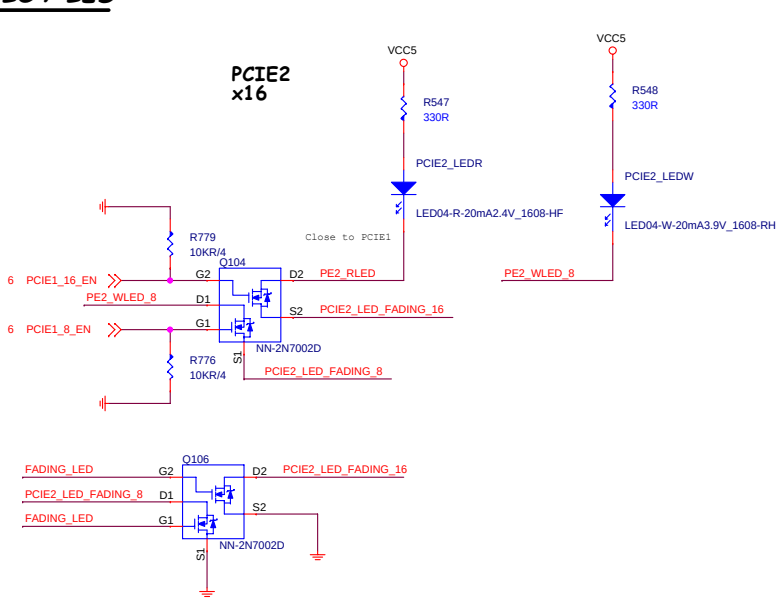
DIMM_SLOT

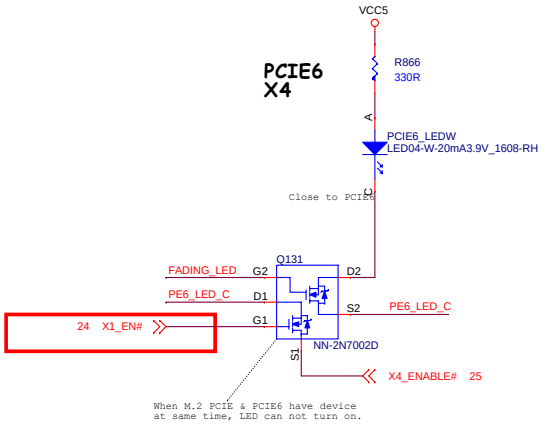
翎 : D0C-040S500-E07

LED 圖 DIMM_L E D nn歲 计



PCIE SLOT LED





	x16	x8	x4
PCIE1	Red	X	X
PCIE4	X	White	X
PCIE6	X	X	White

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Size	Document Description	Rev
Custom	LED DIMM/PCIE	11

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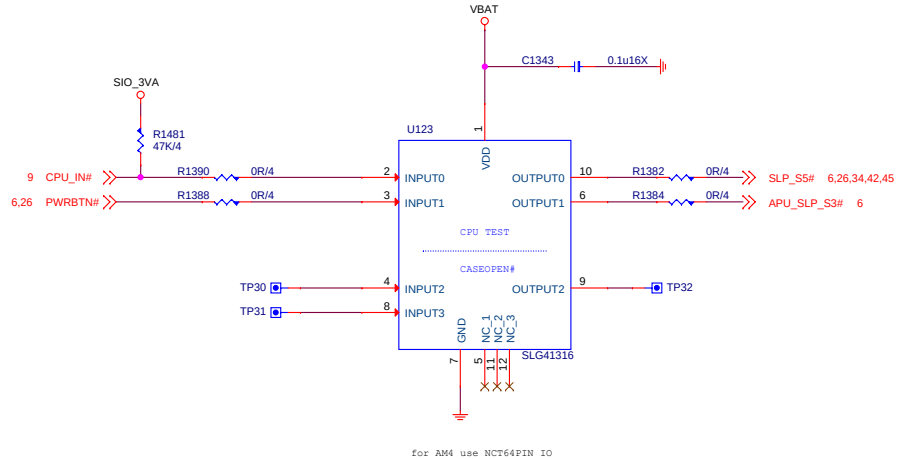
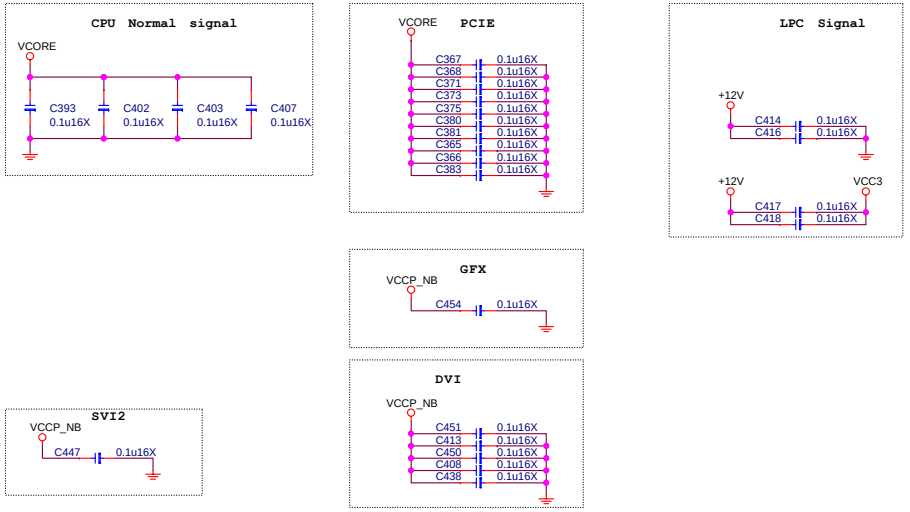
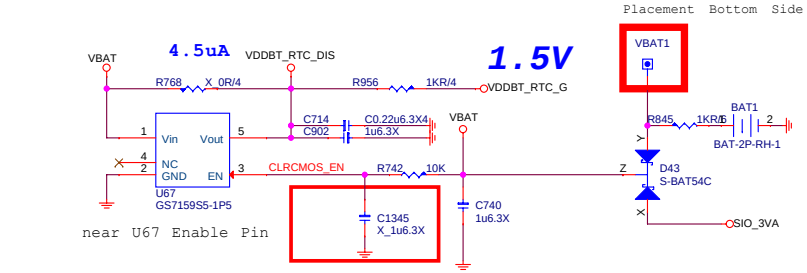
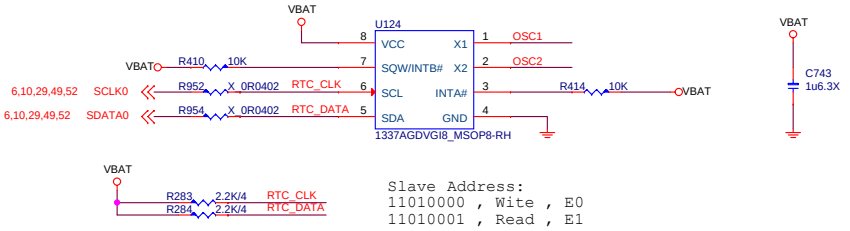


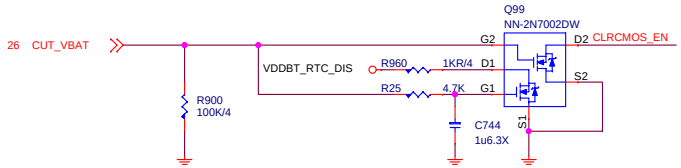
Moat Cap



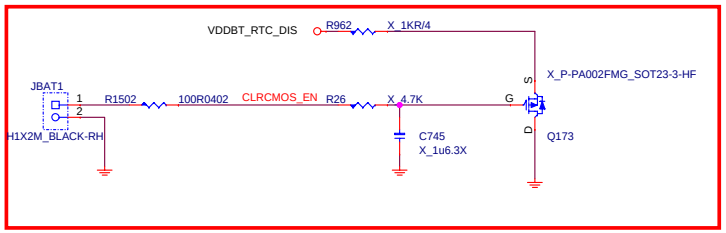
RTC & Clear CMOS Circuit



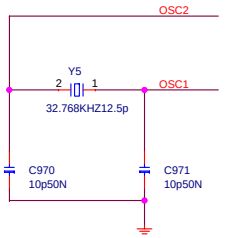


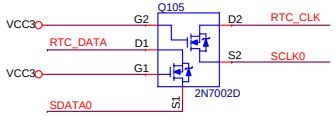


0207 update



0107 AM4 update





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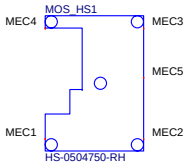
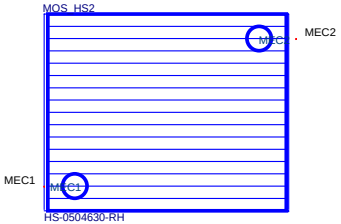
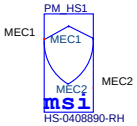
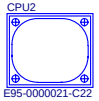
HEAT SINK





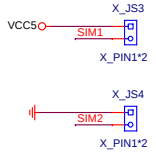


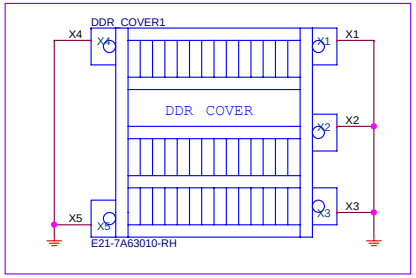
CPU Socket



RETENTION MODULE

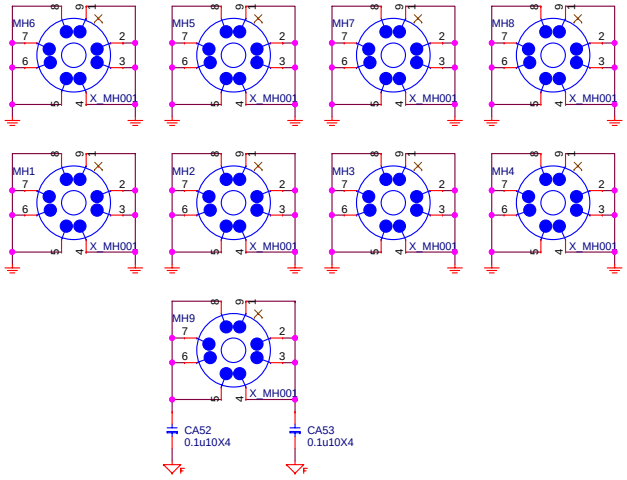
Simulation





0901 Modify DDR_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND for tiancai

Optics Orientation Holes



MANUAL PART

UEFI1
G51-M1SPXXA-A09

MKT1
G51-M1SPK97-Q13

VIRTUAL1
G51-M1SPK31-Q13

VIRTUAL2
G51-M1SPK31-Q13

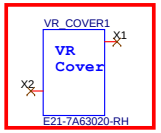
VIRTUAL3
G51-M1SPK31-Q13

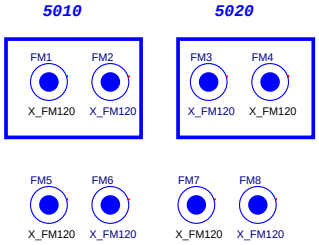
VIRTUAL4
G51-M1SPK31-Q13

VIRTUAL5
Y02-MA00401-XSP

PD0-07B0011-G37
PD0-07B0011-E48

VR Cover





OPT	Configure	BOM	Function
			XXXX

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