# Lab8

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## **Q1**

Prove that you have replaced the kernel

#### Before replacement

```
The programs included with the Debian GNU/Linux system are free software; the exact distribution terms for each program are described in the individual files in /usr/share/doc/*/copyright.

Debian GNU/Linux comes with ABSOLUTELY NO WARRANTY, to the extent permitted by applicable law.

SSH is enabled and the default password for the 'pi' user has not been changed. This is a security risk - please login as the 'pi' user and type 'passwd' to set a new password.

5.4.51-u7+

**Processpuerrypi:** § uname -r
```

#### After replacement

Prove that you have built the nailgun module with new headers

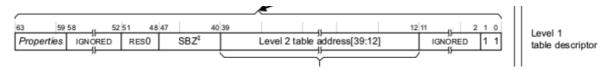
### We complie the nailgun module successfully

The Nailgun Attack works.

```
[ 4.838067] systemdill: /etc/system/system/tean/leverd.service:8: PIDFile= references path below legacy discordingly.
[ 5.140238] randon: systemd: uninitialized urandon read (16 bytes read)
[ 5.180212] randon: systemd: uninitialized urandon read (16 bytes read)
[ 5.19048] systemdill: Listening on udev Control Socket.
[ 5.225742] randon: systemd: uninitialized urandon read (16 bytes read)
[ 5.243442] systemdill: Listening on Journal Socket (/dev/log).
[ 5.284186] systemdill: Condition check resulted in Journal Audit Socket being skipped.
[ 5.304136] systemdill: Set up autonount Arbitrary Executable File Fornats File System Autonount Point.
[ 6.213902] EXT4-fs (nachlbQp2): re-mounted. Opts: (null)
[ 6.372883] systemd-journaldil06]: Received request to flush runtime journal from PID 1
[ 9.283459] randon: crug init done
[ 9.283459] randon: 7 urandon warning(s) missed due to ratelimiting
[ 9.612706] uart-plo11 37201000 serial: no DMA platform data
[ 10.201186] Adding 102396k swap on /var/swap. Priority:-2 extents:1 across:102396k SSFS
[ 341.810509] nailgun: loading out-of-tree module taints kernel.
[ 341.811080] Step 1: Unlock debug and cross trigger registers
[ 341.811080] Step 2: Emable halting debug
[ 341.811093] Step 3: Halt the target processor
[ 341.811093] Step 4: Noit the target processor
[ 341.811093] Step 5: Save context
[ 341.811109] Step 6: Switch to EL3
[ 341.811109] Step 6: Switch to EL3
[ 341.811109] Step 7: Read SCB
[ 341.811113] Step 7: Read SCB
[ 341.811130] Step 7: Read SCB
[ 341.811131] Step 7: Read SCB
[ 341.811132] Step 9: Send restart request to the target processor
[ 341.811131] Step 7: Read SCB
[ 341.811132] Step 9: Send restart request to the target processor
[ 341.811136] All done The value of SCB is 0x00000131
[ pi@raspberrypi - All Scales - All
```

# Q3 & Q4

The translation table base address is VTTBR: 0x32000000



As the picture above shows, size of a descriptor is  $2^3$  B.

According to structure of IPA, I know followings:



- 1. The number of entries for each page table:
  - $\circ \ \ \text{level-1 page table:} \ 2^{31-30+1} = 2^2 \\$
  - $\circ \ \ \text{level-2 page table:} \ 2^{29-21+1} = 2^9 \\$
  - $\circ \;\;$  level-3 page table:  $2^{20-12+1}=2^9$
- 2. Space (B) needed to store each level page table:
  - o level-1 page table

Since 
$$2^3 imes 2^2 = 2^5 < 4KB$$
, it needs  $4KB = 2^{12}B$ 

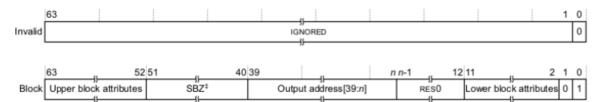
o level-2 and level-3 page table

$$2^3 \times 2^9 = 2^{12}B$$

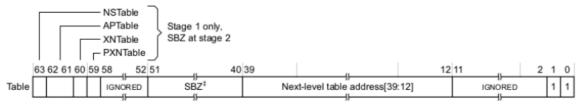
## Design

### **Descriptor's value**

1. For level-1 & level-2 descriptor:



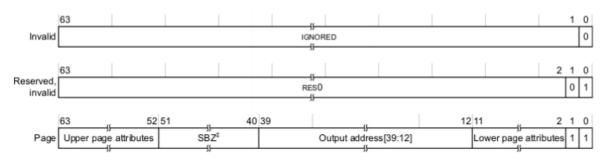
For the level 1 descriptor, n is 30. For the level 2 descriptor, n is 21.



The level 1 descriptor returns the address of the level 2 table. The level 2 descriptor returns the address of the level 3 table.

## For simplicity, if it is

- invalid: value is 0
- $\bullet$  block: only care about output address , value is output address <<30+1 for level 1 and output address <<21+1 for level 2
- ullet table: only care about next-level table address, value is next-level table base address <<12+3
- 2. For level-3 descriptor:



## For simplicity, if it is

- invalid: value is 0
- ullet page: only care about output address , value is output address << 12+3

#### Address range of each page table

1. Level-1 Page Table: [  $0x3200\ 0000\ ,\ 0x3200\ 0000\ +\ 2^{12})$  =

[0x32000000, 0x32001000)

Base of level-1 page is VTTBR.

2. Level-2 Page Table: [ 0x3200 1000 , 0x3200 1000 +  $2^2 \times 2^{12}$ ) =

[0x32001000, 0x32005000)

Base of level-2 page is 0x3200 1000, called BA2.

3. Level-3 Page Table:

Theoretically, the range should be <code>[0x3200 5000, 0x3200 5000 +  $2^2 \times 2^9 \times 2^{12}$ ) = <code>[0x3200 1000, 0x3280 5000)</code> but <code>0x3280 5000 > 0x321f ffff</code> (upper bound of the reserved space). Therefore, actual range is</code>

Base of level-3 page is 0x0x3200 5000, called BA3.

## Q3

What I know:

- VTTBR: 0x3200 0000
- input IPA: 0x40030614 = 0b0100 0000 0000 0011 0000 0110 0001 0100
  - Level-1 Page Table Number: IPA[31:30] = 0b01
  - Level-2 Page Table Number: IPA[29:21] = 0b0
  - Level-3 Page Table Number: IPA[20:12] = 0b0011 0000
  - offset (4kb): IPA[11:0] = 0b0110 0001 0100
- output PA (PA== IPA): 0x40030614 = 0x40030 << 12 + 0x614

According to my design,

- 1. level 1:
  - o address of descriptor:

concat(VTTBR[39:5], IPA[31:30], 0b000) = 0x3200 0008

value of descriptor:

it points to the second (index is IPA[31:30]==1) level-2 table, so address of the table is  $A2=(\mathrm{BA2}+1\times2^{12})=0\mathrm{x}3200~2000$ 

$$A2[39:12] << 12 + 3 = 0x3200\ 2003$$

2.

- 2. level 2 (base 0x3200 1000):
  - address of descriptor:concat(A2[39:12], IPA[29:21], 0b000) = 0x3200 2000
  - o value of descriptor:

it points to the first (index is IPA[29:21]==0) level-3 table, so address of the table is  $A3=(\mathrm{BA3}+0\times2^{12})=0\mathrm{x}3200~5000$ 

$$A3[39:12] << 12 + 3 = 0x32005003$$

- 3. level 3 (base 0x3200 5000):
  - address of descriptor:

concat(A3[39:12], IPA[20:12], 0b000) = 0x3200 5180

value of descriptor:

it points to output address PA, so the value is

## **Q4**

#### What I know:

- VTTBR: 0x3200 0000
- input IPA: 0x41912614 = 0b0100 0001 1001 0001 0010 0110 0001 0100
  - Level-1 Page Table Number: IPA[31:30] = 0b01
  - Level-2 Page Table Number: IPA[29:21] = 0b1100
  - Level-3 Page Table Number: IPA[20:12] = 0b1 0001 0010
  - offset (4kb): IPA[11:0] = 0b0110 0001 0100
- output PA (PA== IPA): 0x41912614 = 0x41912 << 12 + 0x614

### According to my design,

- 1. level 1:
  - address of descriptor:

concat(VTTBR[39:5], IPA[31:30], 0b000) = 0x3200 0008

value of descriptor:

it points to the second (index is IPA[31:30]==1) level-2 table, so address of the table is  $A2=(\mathrm{BA2}+1\times2^{12})=0\mathrm{x}3200~2000$ 

$$A2[39:12] << 12 + 3 = 0x3200\ 2003$$

- 2. level 2 (base 0x3200 1000):
  - address of descriptor:

value of descriptor:

it points to the 12th (index is IPA[29:21]==12) level-3 table, so address of the table is  $A3=({
m BA}3+12\times 2^{12})=0{
m x}3201\ 1000$ 

$$A3[39:12] << 12 + 3 = 0x32011003$$

- 3. level 3 (base 0x3200 5000):
  - address of descriptor:

$$concat(A3[39:12], IPA[20:12], 0b000) = 0x3201 1890$$

value of descriptor:

it points to output address PA, so the value is

$$PA[39:12] << 12 + 3 = 0x4191 2003$$