WK2124

SPI Interface
Four-channel Universal Asynchronous transceiver
Lead-free Package

1. Product Overview

WK2124 is a SPI™ bus interface to 4-channel UART device. It realizes SPI bridging/extending to four enhancements UART.

The extended sub-channel UART has the following features:

- Each slave channel UART baud rate, word length, parity format can be set independently. And can offer the communication rates up to 2Mbps.
- Each slave channel can be set independently in the IRDA infrared communications.
- Each slave channel is equipped with 256-level FIFO in sending and receiving, can be programmed according to user requirements and has timeout interrupt function.

WK2124 comes in SSOP20L green lead-free package and can operate in a wide operating voltage range of 2.5 ~ 5.0V. and with automatic sleep / wake function.

[Note]: SPI™ is registered trademark of MOTOROLA Company.

2. Basic Characteristics

2.1 General Features

- Low-power design, can configure the automatic sleep, automatic wake-up mode(uS level wake-up)
- L hardware transceiver cache， supporting 256 FIFO
- Wide operating voltage, 2.5V ~ 5.0V
- Configuration register and control word、 operater simply
- Industrial products
- High-speed CMOS process, the port rates up to 2Mbps@5V, 1.5Mbps@3.3V and 1Mbps@2.5V.
- Come in SSOP20 Lead-free green packaging .

2.2 Sub-channel UART Characteristics

- Slave channel UART can be configurated independently, speed, flexibility:
  Full-duplex, on / off by software;
  The baud rate can be set independently, and port rates up to 2Mbps.
  Character formats including data length, stop digit, parity mode can be set independently.
  status query function
  Supporting the software reset of single sub-serial port ..
- FIFO function:
  Independent 256-level sending FIFO, and the FIFO trigger point is programmable.
  Independent 256-level receiving FIFO, and the FIFO trigger point is programmable.

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Software FIFO enables and empties.

FIFO status and counter output.

- Error detection:

  Support parity error, framing error, overrun error, and Line-Break error .

  Support start bit error detection

- Built-in IRDA infrared transceiver and decoder, SIR standard, the rates up to 115.2K bit/s
- Interrupt features:
  Receiving FIFO timeout interruption
  Support Line-Break error interruption

2.3 SPI Interface Features

- 10Mbit/s maximum speed
- Support SPI slave mode only
- SPI mode 0
- Up to 256 bytes receive and send continuously

3. Applications

- Multi-serial Server/Multi-port serial Card
- IRS-485 Control in Industrial/Automation Site
- Wireless data transmission through 2G/3G/4G
- Vehicle Information Platform/ GPS
- Remote automatic meter reading (AMR) systems
- POS / tax control POS / financial machinery
- DSP / Embedded Systems

4. Order Information

Table 4.1 WK2124 Order Information

Product Type	Package	Explanation
WK2124-ISSG	SSOP20 Lead-free package	General industrial grade; industrial temperature range -40℃～+85℃

5. Principle Block Diagram

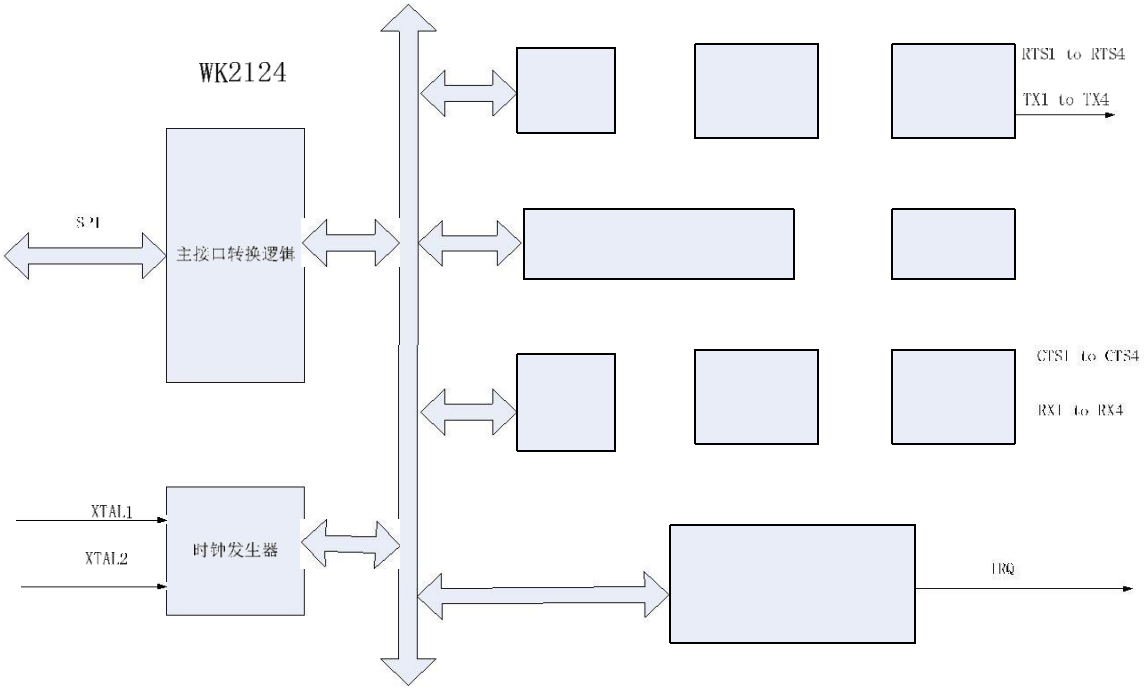
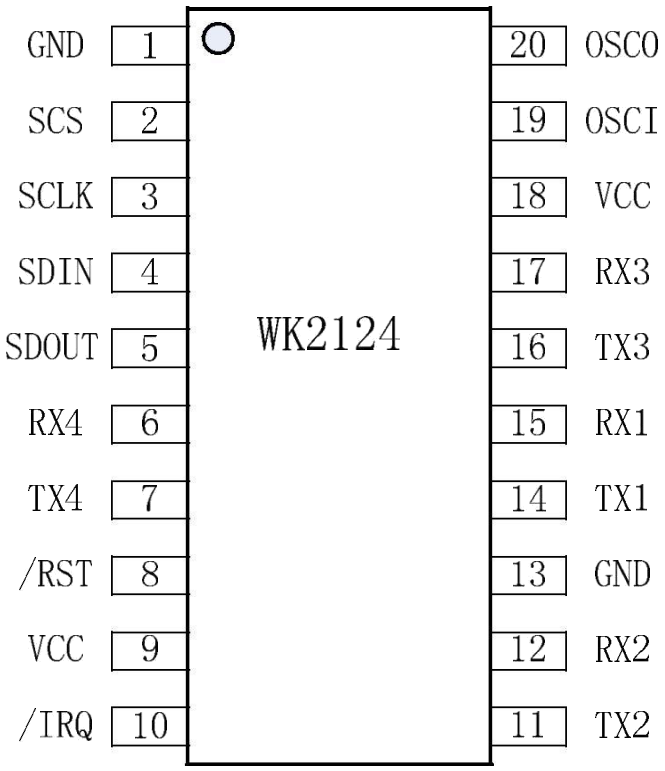


Figure 5.1 WK2124 Block Diagram

6. Package Pins

6.1 Figure Package



6.2 Pin Description

Table 6.2 WK2124 Pin Description

Symbol	Pin	Type	Function Description
GND	1,13	-	land
SCS	2	I/O	When the main interface is SPI, for SCS (SPI chip selection SSEL) functional pin: low level effective
SCLK	3	I/O	When the main interface is SPI, it is SCLK (SPI clock input) functional pin.
SDIN	4	I/O	When the main interface is SPI, it is a MOSI functional pin.
SDOUT	5	I/O	When the main interface is SPI, it is MISO functional pin
RX1 RX2 RX3 RX4	15 12 17 6	I	Sub-channel serial data input. RX inputs the serial data of UART to the corresponding pins of WK2124.
TX1 TX2 TX3 TX4	14 11 16 7	O	Sub-channel serial data output. TX outputs serial data to the device pins connected to it.
RST	8	I	Hardware reset pin, low level reset is effective
VCC	9,18	-	Power supply 2.5V~5.0V working voltage
IRQ	10	O	Output signal interruption, low level effective. External pull-up resistance is recommended. Typical value is 5.1K.
OSCI	19	I	Crystal vibration input. Note: 1 M resistor in parallel with crystal oscillator is required.
OSCO	20	O	Crystal oscillator output

7. Register Description

7.1 Register List

WK2124's register address is numbered by 6-bit address, ranging from 000000 to 111111. It is divided into global register and sub-serial register.

There are 4 global registers. The address arrangement is shown in Table 7.1.1:
Table 7.1 Global Register Lists

Addr[5:0]	Name	Type	Function Description
000000	GENA	R/W	Global Control Register
000001	GRST	R/W	Global Sub-serial Reset Register
010000	GIER	R/W	Global Interrupt Register
010001	GIFR	R	Global Interrupt Flag Register

There are 16 sub-serial port registers , arranged in C1C0 REG [3:0], The two high bits are the sub-serial port channel numbers, and the four low bits are register address, shown in Table 7.1.2

Table 7.1.2 Sub-serial Control Register

Register address [3:0]	Name	Type	Function description	
(C1,C0) 0011	SPAGE	R/W	Sub-serial port page control register	
(C1,C0) 0100	SCR	R/W	Sub-serial port control register	SPAGE0
(C1,C0) 0101	LCR	R/W	Sub-serial port configuration register	SPAGE0
(C1,C0) 0110	FCR	R/W	Sub-serial port FIFO control register	SPAGE0
(C1,C0) 0111	SIER	R/W	Sub-serial Interrupt Enabling Register	SPAGE0
(C1,C0) 1000	SIFR	R/W	Sub-serial interrupt flag register	SPAGE0
(C1,C0) 1001	TFCNT	R	FIFO Count Register Send by Sub-serial Port	SPAGE0
(C1,C0) 1010	RFCNT	R	Sub-serial Receiving FIFO Count Register	SPAGE0
(C1,C0) 1011	FSR	R	Sub-serial FIFO Status Register	SPAGE0
(C1,C0) 1100	LSR	R	Sub-serial Receive Status Register	SPAGE0
(C1,C0) 1101	FDAT	R/W	Sub-serial FIFO Data Register	SPAGE0
(C1,C0) 0100	BAUD1	R/W	Suberial Port Baud Rate Configuration Register High Bytes	SPAGE1
(C1,C0) 0101	BAUD0	R/W	Sub-serial Port Baud Rate Configuration Register Low Byte	SPAGE1
(C1,C0) 0110	PRES	R/W	Sub-serial Port Baud Rate Configuration Register Decimal Part	SPAGE1
(C1,C0) 0111	RFTL	R/W	Sub-serial Receiving FIFO Interrupt Trigger Configuration Register	SPAGE1
(C1,C0) 1000	TFTL	R/W	FIFO Interrupt Trigger Configuration Register Send by Sub-serial Port	SPAGE1

C1, C0: sub-channel number, 00-11: corresponding to sub-serial port 1 to port 4, respectively

7.2 Register Description

7.2.1 GENA Global Control Register: (000000)

Bit	Rst	Function Description	Type
Bit7	0	RSV (reserved bit)	R
Bit6	0	RSV (reserved bit)	R
Bit5	1	RSV (reserved bit)	R
Bit4	1	RSV (reserved bit)	R
Bit3	0	UT4EN ,sub-serial 4 clock enable bit (Shut down the sub-serial clock for lower power consumption) 0: Disenabled 1: Enable	W/R
Bit2	0	UT3EN ,sub-serial 3 clock enable bit (Shut down the sub-serial clock for lower power consumption) 0: Disenabled 1: Enable	W/R
Bit1	0	UT2EN, sub-serial 2 clock enable bit (Shut down the sub-serial clock for lower power consumption) 0: Disenabled 1: Enable	W/R
Bit0	0	UT1EN, sub-serial 1 clock enable bit (Shut down the sub-serial clock for lower power consumption)	W/R

		0: Disenabled 1: Enable	

7.2.2 GRST Global Sub-serial Reset Register: (000001)

Bit	Rst	Function Description	Type
Bit7	0	UT4SLEEP Sub-serial Port 4 Hibernation Status Bit (Reduce power consumption, automatic wake-up) 0: Not dormant 1: dormant	R
Bit6	0	UT3SLEEP Sub-serial Port 3 Hibernation Status Bit (Reduce power consumption, automatic wake-up) 0: Not dormant 1: dormant	R
Bit5	0	UT2SLEEP Sub-serial Port 2 Hibernation Status Bit (Reduce power consumption, automatic wake-up) 0: Not dormant 1: dormant	R
Bit4	0	UT1SLEEP Sub-serial Port 1 Hibernation Status Bit (Reduce power consumption, automatic wake-up) 0: Not dormant 1: dormant	R
Bit3	0	UT4RST Sub-serial Port 4 Soft Reset Control Bit (The bit writes 1 to reset and automatically sets 0 after completion) 0: Unreset Sub-serial 4 1: Reset Sub-serial Port 4	W1/R0
Bit2	0	UT3RST Sub-serial Port 3 Soft Reset Control Bit (The bit writes 1 to reset and automatically sets 0 after completion) 0: Unreset Sub-serial Port 3 1: Reset Sub-serial Port 3	W1/R0
Bit1	0	UT2RST Sub-serial Port 2 Soft Reset Control Bit (The bit writes 1 to reset and automatically sets 0 after completion) 0: Unreset Sub-serial 2 1: Reset Sub-serial Port 2	W1/R0
Bit0	0	UT1RST Sub-serial Port 1 Soft Reset Control Bit (The bit writes 1 to reset and automatically sets 0 after completion) 0: Unreset Sub-serial Port 1 1: Reset Sub-serial Port 1	W1/R0

7.2.3 GIER Global Interrupt Register: (010000)

Bit	Rst	Function Description	Type
Bit7--5	000	RSV (reserved bit)	R
Bit4	0	RSV (reserved bit)	W/R
Bit3	0	UT4IE sub-serial port 4 interrupt enable control bit 0: Disenabled 1: Enable	W/R
Bit2	0	UT3IE sub-serial port 3 interrupt enable control bit 0: Disenabled 1: Enable	W/R
Bit1	0	UT2IE sub-serial 2 interrupt enable control bit 0: Disenabled 1: Enable	W/R
Bit0	0	UT1IE sub-serial port 1 interrupt enable control bit 0: Disenabled 1: Enable	W/R

7.2.4 GIFR Global Interrupt Flag Register: (010001)

Bit	Rst	Function Description	Type
Bit7--4	000	RSV (reserved bit)	R
Bit3	0	UT4INT sub-serial port 4 interrupt flag bit 0: Not interrupt 1: Interrupt	R
Bit2	0	UT3INT sub-serial port 3 interrupt flag bit 0: Not interrupt 1: Interrupt	R
Bit1	0	UT2INT sub-serial 2 interrupt flag bit 0: Not interrupt 1: Interrupt	R
Bit0	0	UT1INT sub-serial 1 interrupt flag bit 0: Not interrupt 1: Interrupt	R

7.2.5 SPAGE sub-serial page control register: (0011)

Bit	Rst	Function Description	Type
Bit7--1	000000	RSV (reserved bit)	R
Bit0	0	PAGE sub-serial page control bit (sub-serial registers are distributed on PAGE0 and PAGE1, switching between different pages, controlled by this register)	W/R

7.2.6 SCR sub-serial control register: (PAGE0: 0100)

Bit	Rst	Function Description	Type
Bit7--3	000	RSV (reserved bit)	W/R
Bit2	0	SLEEPEN sub-serial sleep enable bit 0: Disenabled 1: Enable	W/R
Bit1	0	TXEN sub-serial transmit enable bit 0: Disenabled 1: Enable	W/R
Bit0	0	RXEN sub-serial receive enable bit 0: Disenabled 1: Enable	W/R

7.2.7 LCR sub-serial configuration register: (PAGE0: 0101)

Bit	Rst	Function Description	Type
Bit7--6	00	RSV (reserved bit)	W/R
Bit5	0	BREAK Sub-serial Line-Break Output Control Bit 0: Normal output 1: Line-Break output (TX forced output 0)	W/R
Bit4	0	IREN sub-serial infrared enable bit 0: Normal mode 1: Infrared mode	W/R
Bit3	0	PAEN sub-serial check enable bit 0: Not parity bit(8-bit data) 1:There is a check digit(9-bit data)	W/R
Bit2--1	0	PAM1—0 sub-serial check mode selection bit When PAEN=1 sub-serial port verification is enabled: 00: check 01: odd check 10: even check 11: check	W/R
Bit0	0	STPL sub-serial stop bit length control bit 0:1bit 1:2bits	W/R

7.2.8 FCR sub-serial FIFO control register: (PAGE0: 0110)

Bit	Rst	Function Description	Type
Bit7--6	00	TFTRIG[1:0]: sub-serial transmit FIFO contact setting bit When TFTL[7:0]=0: 00: 8 byte 01: 16 byte 10: 24 byte 11: 30 byte	W/R
Bit5--4	00	RFTRIG[1:0]: sub-serial receive FIFO contact setting bit When RFTL[7:0]=0: 00: 8 byte 01: 16 byte 10: 24 byte 11: 28 byte	W/R
Bit3	0	TFEN sub-portal transmit FIFO enable bit 0: Disenable 1: Enable	W/R
Bit2	0	RFEN sub-serial receive FIFO enable bit 0: Disenable 1: Enable	W/R
Bit1	0	TFRST sub-serial port sends FIFO reset bit(This bit is written with 1 reset and is automatically set to 0 after completion) 0: Reset is not enabled 1: Reset FIFO	W1/R0
Bit0	0	RFRST sub-port receiving FIFO reset bit(This bit is written with 1 reset and is automatically set to 0 after completion) 0: Reset is not enabled 1: Reset FIFO	W1/R0

7.2.9 SIER sub-serial interrupt enable register: (PAGE0: 0111)

Bit	Rst	Function Description	Type
Bit7	0	FERR_IEN receive FIFO error interrupt enable bit 0: Forbid receiving FIFO data error interrupt 1: Enable receive FIFO data error interrupt	W/R
Bit6	0	RSV (reserved bit)	W/R
Bit5	0	RSV (reserved bit)	W/R
Bit4	0	RSV (reserved bit)	W/R
Bit3	0	TFEMPTY_IEN transmit FIFO empty interrupt enable bit 0: Forbid transmit FIFO empty interrupt 1: Enable transmit FIFO empty interrupt	W/R
Bit2	0	TFTRIG_IEN transmit FIFO trigger interrupt enable 0: Forbid transmit FIFO contact interrupt 1: Enable transmit FIFO contact interrupt	W/R
Bit1	0	RXOVT_IEN receive FIFO timeout interrupt enable bit 0: Forbid receive FIFO timeout interrupt 1: Enable receive FIFO timeout interrupt	W/R
Bit0	0	RFTRIG_IEN receive FIFO contact interrupt enable bit 0: Forbid receiver FIFO contact interrupt 1: Enable receive FIFO contact interrupt	W/R

7.2.10 SIFR Sub-serial Interrupt Flag Register: (PAGE0: 1000)

Bit	Rst	Function Description	Type
Bit7	0	FERR_INT: receive FIFO data error interrupt flag 0: Not receive FIFO data error interrupt 1: Receive FIFO data error interrupt	W/R
Bit6	0	RSV (reserved bit)	W/R
Bit5	0	RSV (reserved bit)	W/R
Bit4	0	RSV (reserved bit)	W/R
Bit3	0	TFEMPTY_INT: transmit FIFO empty interrupt flag 0: Not transmit FIFO empty interrupt 1: Transmit FIFO empty interrupt	W/R
Bit2		TFTRIG_INT: transmit FIFO trigger interrupt flag 0: Not transmit FIFO trigger interrupt 1: Transmit FIFO trigger interrupt	W/R
Bit1		RXOVT_INT: receive FIFO overtime interrupt flag 0: Not transmit FIFO overtime interrupt 1: Transmit FIFO overtime interrupt	W/R
Bit0	0	RFTRIG_INT: receive FIFO trigger interrupt flag 0: Not transmit FIFO trigger interrupt 1: Transmit FIFO trigger interrupt	W/R

7.2.11 TFCNT Sub-serial Transmit FIFO Count Register: (PAGE0: 1001)

Bit	Rst	Function Description	Type
Bit7 -- 0	00000000	Number of Data in FIFO Send by Sub-serial Port	R

7.2.12 RFCNT Sub-serial Receive FIFO Count Register: (PAGE0: 1010)

Bit	Rst	Function Description	Type
Bit7 -- 0	00000000	Number of Data in Sub-serial Receiving FIFO	R

7.2.13 FSR Sub-serial FIFO Status Register: (PAGE0: 1011)

Bit	Rst	Function Description	Type
Bit7	0	Data Overflow Error Location in RFOE Sub-serial Port Receiving FIFO 0: No OE error 1: OE error	R
Bit6	0	Line-Break Error in RFBI Sub-serial Port Receiving FIFO Data 0: No Line-Break error 1: Line-Break error (Rx signal has been zero state, including check bits and stop bits)	W/R
Bit5	0	RFFE Sub-serial Port Receives Data Frame Error Markers in FIFO 0: No FE error 1: FE error	W/R
Bit4	0	Data Check Error Marker in RFPE Sub-serial Receiving FIFO 0: No PE error 1: PE error	W/R
Bit3	0	RDAT Sub-serial Port Receives FIFO Null Flag Bit 0: Sub-serial Receiving FIFO Empty 1: Sub-serial receiving FIFO is not empty	W/R
Bit2	0	TDAT Sub-serial Port Sends FIFO Null Flag Bit 0: Sub-serial port sends FIFO empty 1: Sub-serial port sending FIFO is not empty	W/R
Bit1	0	TFULL Sub-serial Port Sends FIFO Full Flag Bit 0: Sub-serial sending FIFO is not full 1: Sub-serial port sends FIFO full	W/R
Bit0	0	TBUSY Sub-serial Port Sends TX Busy Flag Bit 0: Sub-serial port sends TX empty 1: Sub-serial port sends TX busy	W/R

7.2.14 LSR Sub-serial Receive Status Register: (PAGE0: 1100)

Bit	Rst	Function Description	Type
Bit7 – 4	0	RSV (reserved)	
Bit3	0	OE sub-serial port receives the currently read byte overflow error flag bit in FIFO 0: No OE error 1: OE error	R
Bit2	0	BI Sub-serial Receives Line-Break Error Markers in FIFO 0: No Line-Break Error 1: Line-Break Error (Rx signal has been zero state, including check bits and stop bits)	R
Bit1	0	FE sub-serial port receives the error flag bit of byte frame currently read in FIFO 0: No FE error 1: FE error	R
Bit0	0	PE sub-serial port receives the current read byte check error flag bit in FIFO 0: No PE error 1: PE error	R

7.2.15 FDAT Sub-serial FIFO Data Register: (PAGE0: 1101)

Bit	Rst	Function Description	Type
Bit7--0	00000000	Write operation: Write the data of FIFO to the sub-serial port Read Operation: Read out Sub-serial Port to Receive FIFO Data	W/R

7.2.16 BAUD1 Sub-serial Baud Rate Configuration Register High Byte: (PAGE1: 0100)

Bit	Rst	Function Description	Type
Bit7--0	00000000	BAUD[15:8]: Sub-serial Port Baud Rate Configuration Register High Bytes	W/R

7.2.17 BAUD0 Sub-serial Baud Rate Configuration Register Low Byte: (PAGE1: 0101)

Bit	Rst	Function Description	Type
Bit7--0	00000000	BAUD[7:0]: Sub-serial Port Baud Rate Configuration Register Low Byte	W/R

7.2.18 PRES Sub-serial Baud Rate Configuration Register Fractional Part: (PAGE1: 0110)

Bit	Rst	Function Description	Type
Bit7--4	0000	RSV	R
Bit3--0	0000	PRES[3:0]	W/R

7.2.19 RFTL Sub-serial Receive FIFO Trigger Interrupt Register: (PAGE1: 0111)

Bit	Rst	Function Description	Type
Bit7--0	00000000	Receiving FIFO Contact Control	W/R

7.2.20 TFTL Sub-serial Transmit FIFO Trigger Interrupt Register: (PAGE1: 1000)

Bit	Rst	Function Description	Type
Bit7--0	00000000	Send FIFO Contact Control	W/R

8. Global Function Description

8.1 Reset

WK2124 is low level reset.

The reset value of each register is listed in Table 7.2

During reset and after reset, all sub-serial ports are in the state of prohibition of receiving and receiving. When the sub-serial port is in the networking mode, this feature makes the sub-node of the sub-serial port not interfere with other nodes during power-on and reset.

Software reset can be achieved independently by each sub-serial port.

8.2 Clock Selection

WK2124 can choose to use chip oscillator clock as the clock source. Note: The starting resistance of 1M in parallel with the crystal oscillator is required. Follow as figure 8.2.

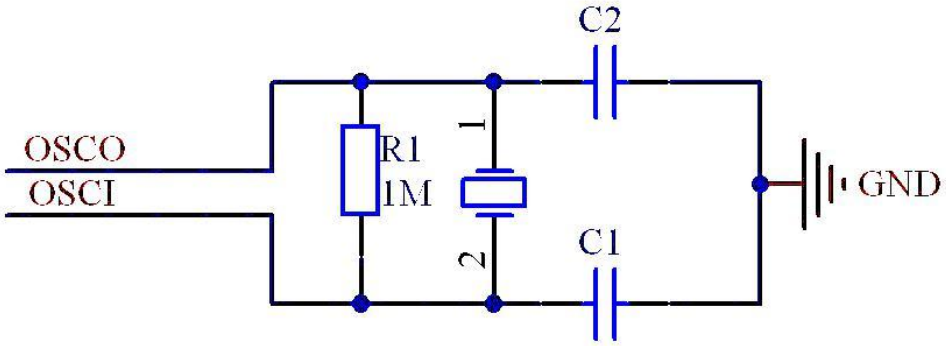


Figure 8.2 WK2124 Clock Circuit

8.3 Interrupt Control

WK2124 has two levels of interrupt: sub-serial interrupt and global interrupt. When the IRQ pin indicates an interrupt, the current interrupt type can be determined by reading the global interrupt register GIFR, and then the corresponding interrupt state register can be read to determine the current interrupt source.

The interrupt structure of WK2124 is shown in the following figure:

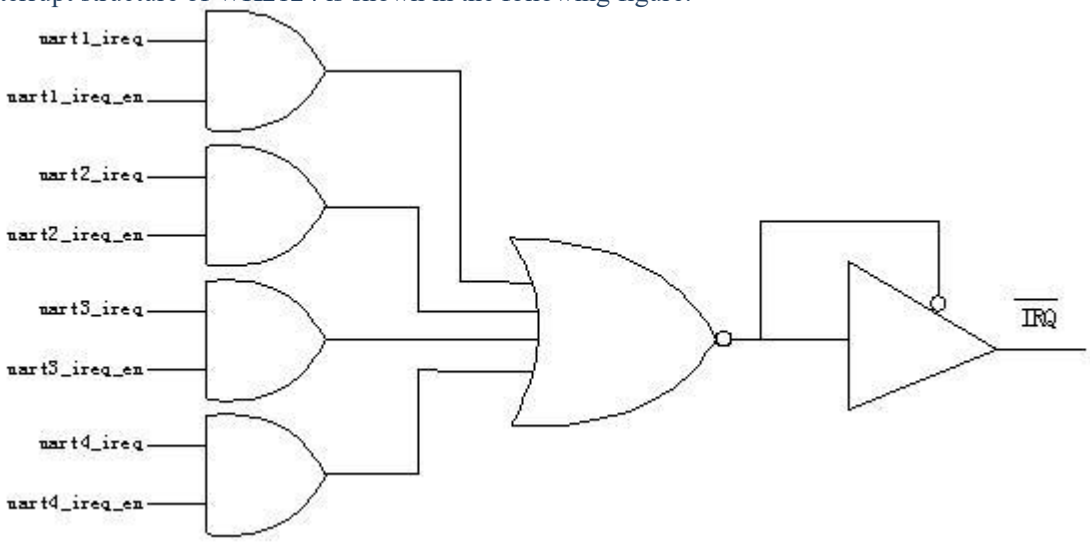


Figure 8.3 WK2124 Interrupt Structure Diagram

Each sub-serial port of WK2124 has its own interrupt system, including FIFO data error interrupt, sending FIFO vacancy interrupt, sending FIFO trigger interrupt, receiving FIFO timeout interrupt and receiving FIFO trigger interrupt

Any interrupt is enabled, a corresponding interrupt will occur if condition is satisfied.

8.3.1 FIFO Data Error Interrupt

FIFO data error interruption indicates that there is one or more data errors in receiving FIFO. The conditions include OE (Data Overflow Error), FE (Data Frame Error), PE (Parity Check Error), BE (Line-Break Error).

If an error data is in receiving FIFO, the interrupt disappears when the FSR register is read, and the interrupt can also be cleared by clearing the error data.

8.3.2 Transmitting FIFO Vacancy Interrupt

When no data is in sending FIFO, the interrupt is generated. The interrupt is cleared when the number of data is more than the set point of the sending FIFO.

8.3.3 Transmitting FIFO Trigger Interrupt

When the number of data in sending FIFO is less than the set trigger point of sending FIFO, the interrupt is generated.. On the contrary, the number is greater than or equal to the set trigger point, the interrupt is cleared.

8.3.4 Receiving FIFO time-out interrupt

When the number of data in the receiving FIFO is less than the set point and no data in the 4 bytes of RX pin, the interrupt is generated. The interrupt disappears when the data in the receiving FIFO is read away or RX continue to receive data.

8.3.5 Receiving FIFO Trigger Interrupt

When the number of data in receiving FIFO is more or equal to the set trigger point of sending FIFO, the interrupt occurs. On the contrary, the interrupt is be cleared.

8.4 Infrared Mode Operation

WK2124 main and sub - serial ports can be set to infrared communication mode. When the UART is set to IRDA mode, it can communicate with devices that conform to the standard of SIR infrared protocol, or directly apply to optical isolation communication.

In IRDA mode, a data cycle is shorted to an ordinary UART data 3/16, pulse less than 1/16 potter cycle will be ignored as an interference .

8.4.1 Infrared Receiver Operation

The time-sequence of infrared data reception and normal UART data reception is shown in figure 8.4.1:

IRX is infrared data signal.RX is the decoded signal through the infrared data. The decoded data has a BIT (16xCLOCK) delay with the data on the IRX. In receiving mode, different from the normal UART, RX samples once in the middle of the pulse (distinct from sampling three times to the normal UART), and the IRDA decoder decodes the 3/16 baud period pulse on the IRX into data 0. Continuous low level decoding is data 1.

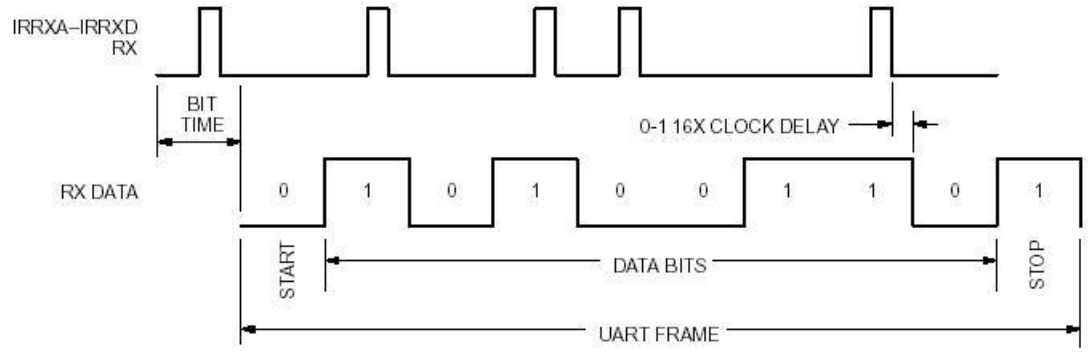


Figure 8.4.1 Infrared Receiver Timing

8.4.2 Infrared Transmission Operation

The time-sequence of infrared data transmission and normal UART data transmission is shown in figure 8.4.2: TX is data transmission time-sequence of normal UART .RTX is the infrared transmission time-sequence. When sending data 0, the infrared encoder will gerenrate a 3/16 bit-wide pulse which sending through the TX. When sending data 0, keep the low level unchanged.

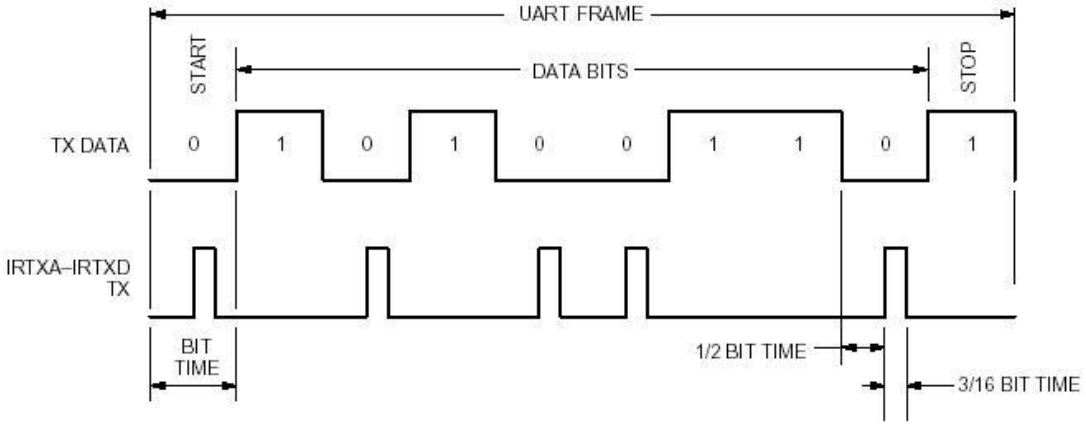


Figure 8.4.2 Infrared Transmission Timing

8.5 Programmable Baud Rate Generator

Both main and sub serial ports adopt the same independent programmable baud rate generator. The generator generates the frequency division coefficient of the 16X system clock, whose rate can be set by software.

8.5.1 The table between common Baud Rate and Crystal Vibration Contrast

The following table shows how to set the serial port baud rate under different system clock frequencies:

Table 8.5.1

BAUD BAUD[15-0]	PRES	BAUD RATE Fosc= 1.8432MHz	BAUD RATE Fosc= 3.6864MHz	BAUD RATE Fosc= 7.3728MHz	BAUD RATE Fosc= 11.0592MHz	BAUD RATE Fosc= 14.7456MHz
0X0002	0X00	38400	76800	153600	230400	307200
0X0005	0X00	19200	38400	78600	115200	153600
0X000b	0X00	9600	19200	38400	57600	76800
0X0017	0X00	4800	9600	19200	28800	38400
0X002f	0X00	2400	4800	9600	14400	19200
0X005f	0X00	1200	2400	4800	7200	9600
0X00bf	0X00	600	1200	2400	3600	4800
0X017f	0X00	300	600	1200	1800	2400
0X0000	0X00	115200	230400	460800	691200	912600
0X0001	0X00	57600	115200	230400	345600	460800
0X0003	0X00	28800	57600	115200	172800	230400
0X0007	0X00	14400	28800	57600	86400	115200

0X000f	0X00	7200	14400	28800	43200	57600
0X001f	0X00	3600	7200	14400	21600	28800
0X003f	0X00	1800	3600	7200	10800	14400
0X007f	0X00	900	1800	3600	5400	7200

8.5.2 Baud Rate Calculation under any Crystal

The formula: fs / (baud*16) = Reg

Note: fs is the system clock. baud is the one should be set, Reg is result(usually accurate to two decimal places)

The integer part of Reg is subtracted by one and then converted into hexadecimal writing {BAUD1, BAUA0}; if there is a decimal part, the first decimal part is written to PRES. If no, just write the integer part to {BAUD1, BAUA0} and PRES to 0.

Example 1: fs = 11.0592MHz, baud = 115200. Reg=6. Then the data to fill in the register are: BAUD1 = 0X00; BAUD0 = 0X05; PRES = 0X00.

Example 2: fs = 12MHz, baud = 115200. Reg=6.51(accurate to two decimal places). Then the data to fill in the register are: BAUD1=0X00;BAUD0=0X05; PRES=0X05.

8.5.3 high baud rate calculation

BAUD BAUD[15-0]	PRES	BAUD RATE Fosc= 8MHz	BAUD RATE Fosc= 16MHz	BAUD RATE Fosc= 24MHz	BAUD RATE Fosc= 32MHz
0X0000	0X00	500K	1M	1.5M	2M
0X0001	0X00	250K	500K	750K	1M
0X0003	0X00	125K	250K	375K	500K

8.6 Data format setting

8.6.1 validation mode

WK2124 can provide compulsory checking, computational checking and non-checking data formats, which are set by LCR (Sub-serial Configuration Register):

Compulsory Check Mode

WK2124 supports strong 1 、 strong 0 and user- specified check mode. In this mode, the validation settings only affect data transmission, and data reception ignores parity

Computational Check Mode

WK2124 supports 1-check, 0-check, odd-check and even-check modes. In this mode, parity checking is performed for both received and transmitted data.

8.6.2 Data length

WK2124 supports 1 or 2-bit stop mode, and the sub-serial port is set by LCR.STPL.

8.7 Dormancy and automatic arousal

WK2124 supports sleep and Automatic wake-up mode, and each sub-serial port can be set to sleep independently.

Dormancy condition: 1、SCR SLEEPEN=1

2、Receive FIFO and send FIFO empty.

3、No data reception on RX and no data transmission on TX

4. There is no interrupt in the sub-serial port.

When the above conditions are satisfied and remain the state continuing 4 bytes time, slave UART goes to sleep automatically. Subserial clock is automatically closed to reduce power consumption. At this time, whether the slave UART into sleep state determined by reading GRST.

In dormant state, one of the following conditions is satisfied. The sub-serial ports can automatically wake up. At this time, we can judge whether the sub-serial ports are awakened by reading GRST.

Wake-up conditions: 1、Start receiving data on RX.

2、Send FIFO Write Data to Sub-serial Port.

8.8 FIFO trigger point Setting

WK2124 supports setting different **trigger point** for each sub-serial port、receiving FIFO and sending FIFO. There are two ways to set up **trigger point**:

1. Fixed **trigger point**: Set up **trigger point** through the fixed-programme through the TFTRIG[1:0] and RFTRIG[1:0] bits in the FCR register2.
2. Unfixed **trigger point**: Set up any trigger point by setting the registers TFTL and RFTL (note: the priority of this method is higher than fixed trigger point, that is, when TFTL/RFTL is not 0, the value of interrupt **trigger point** is equal to the one in TFTL/RFTL.and while the TFTRIG[1:0]/RFTRIG[1:0] configuration in FCR is invalid).

The specific configuration is shown in tables 8.8.1 and 8.8.2.

Send interrupt contact configuration table 8.8.1

TFTL[7:0]	FCR[7:6] TFTRIG[1:0]		Value of sending interrupt **trigger point**
= =0	0	0	8
= =0	0	1	16
= =0	1	0	24
= =0	1	1	30
! =0	X	X	TFTL

Receiving interrupt contact configuration table 8.8.2

RFTL[7:0]	FCR[5:4] RFTRIG[1:0]		Value of receiving interrupt **trigger point**
= =0	0	0	8
= =0	0	1	16
= =0	1	0	24
= =0	1	1	28
! =0	X	X	RFTL

9. SPI Interface Mode Operation

9.1 SPI Connect With Host

The SPI interface includes the following four signals as showed in Figure 9.1:

MISO: SPI outputs data from devices.

MOSI: SPI inputs data from devices.

SCLK: SPI serial clock.

SSEL: SPI Chip Selection (Subordinate Selection).

The connection between WK2124 and the host is shown in Figure 9.1.1.

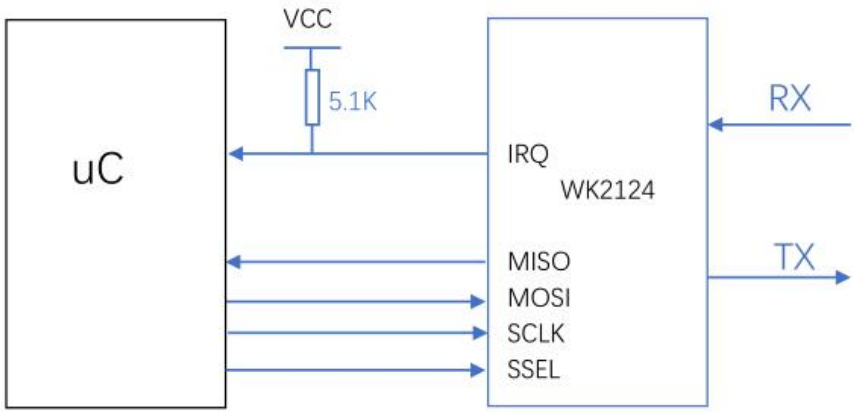


Figure 9.1 The Connection Diagram of SPI and Host

9.2 SPI interface operation sequence

WK2124 works in SPI synchronous serial communication slave mode, support SPI mode 0 standard. to achieve the communication between host and WK2124, it needs to set CPOL=0(SPI clock polarity selection bit) and CPHA=0(SPI clock phase selection bit) on the host.

The operation time- sequence of WK2124 SPI interface is as follow:

The operation time- sequence of writing register is as shown in Figure 9.2.1 First ,write a command byte (Command Byte), then write the corresponding data byte, the register address of the data byte increases automatically.

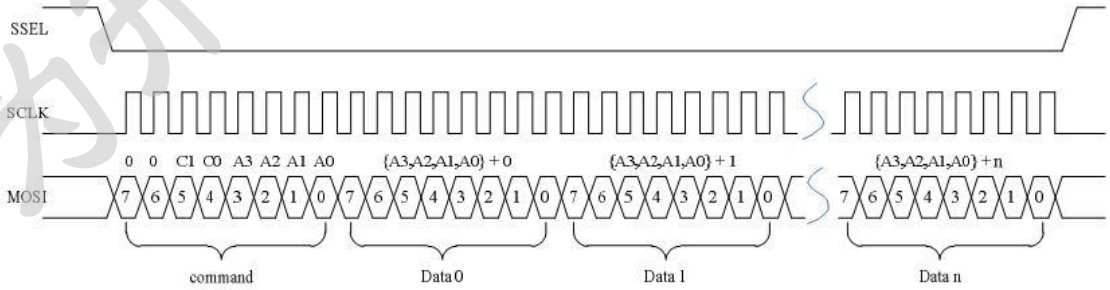


Figure 9.2.1 SPI writes the register sequence diagram

The operation time- sequence of reading register is shown in Figure 9.2.2: First ,write a command byte (Command Byte), and then return the corresponding data byte on the chip MISO line. Register addresses returning data bytes are increased automatically.

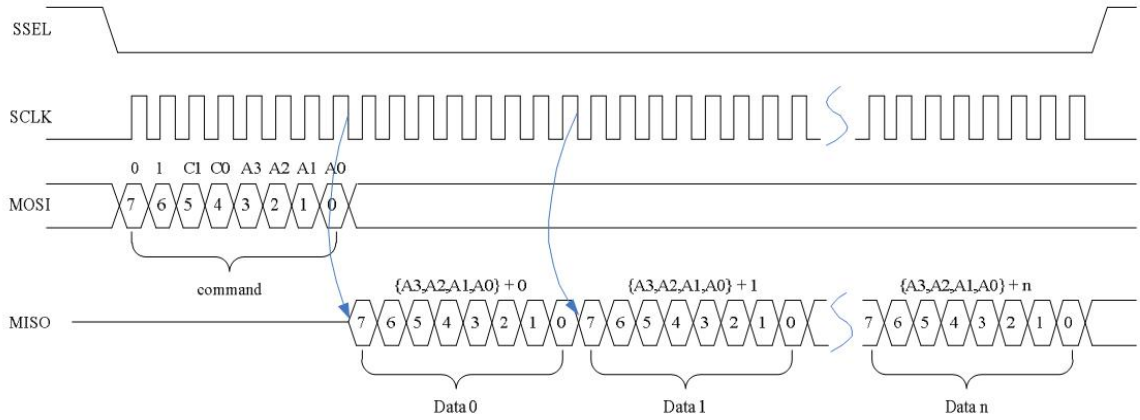


Figure 9.2.2 SPI Read Register Timing Diagram

The operation time- sequence of Writing FIFO is shown in Figure 9.2.3: First, write a command byte (Command Byte), then write the corresponding data byte. FIFO Address increased automatically.

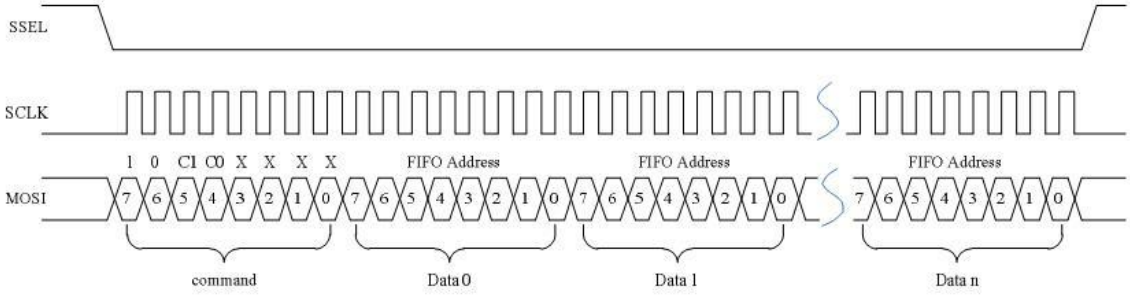


Figure 9.2.3 SPI Write FIFO Timing Diagram

The operation time- sequence of reading FIFO is shown in Figure 9.2.4: Write a command byte (Command Byte) first, and then return the corresponding data byte on the chip MISO line. FIFO Address increased automatically.

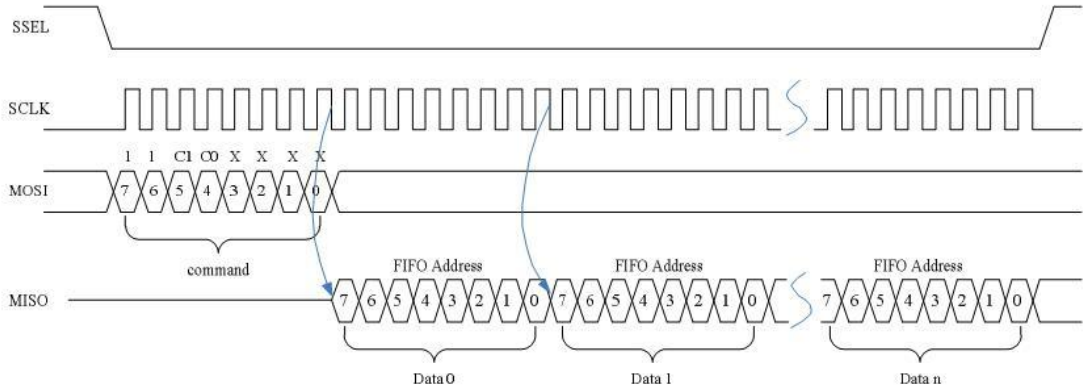


Figure 9.2.4 SPI Read FIFO Timing Diagram

9.3 SPI Bus Communication Protocol Description

9.3.1 SPI Write Register

SPI	Control byte CMD								Data byte DB (write N data bytes, register address is automatically increased)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	0	0	C1	C0	A3	A2	A1	A0	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t
MISO	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ

9.3.2 SPI Read Register

SPI	Control byte CMD								Data byte DB (read N data bytes, register address is automatically increased)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	0	1	C1	C0	A3	A2	A1	A0	X	X	X	X	X	X	X	X
MISO	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t

9.3.3 SPI Write FIFO

SPI	Control byte CMD								Data byte DB (Write N data bytes to FIFO of {C1 C0}, FIFO address increases automatically)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	1	0	C1	C0	X	X	X	X	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t
MISO	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ

9.3.4 SPI Read FIFO

SPI	Control byte CMD								Data byte DB (read N data bytes from FIFO of {C1 C0} and FIFO address increases automatically)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	1	1	C1	C0	X	X	X	X	X	X	X	X	X	X	X	X
MISO	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t

Explain:

1. C1 C0: Sub-serial Channel Number 00-11 corresponds to Sub-serial Port 1 to Sub-serial Port 4.
2. A3-A0: Sub-serial Register Address
3. D7t... D0t: 8-bit data byte

10. Sub-serial Operation Description

10.1 Sub-serial Enable/Disable

WK2124 allows independent enabled or prohibition of each sub-serial channel.
Sub-serial channels that are not used can be prohibited in use.
Sub-serial Channel can receive and send data only in enabled state

10.2 Receive and Transmit FIFO Control

WK2124 provides a separate 256-level FIFO for receiving and sending FIFO. (Sub-serial FIFO control register) set.

10.2.1 Transmit FIFO Trigger Point Operation

WK2124 provide independent programmable transmit FIFO trigger point setting for each channel to generate a corresponding transmit FIFO trigger point interrupt.

When the transmit FIFO trigger point interrupt is enabled, the corresponding interrupt is generated when the number of data in the transmit FIFO is less than the set trigger point.

10.2.2 Receive FIFO Trigger Point Operation

WK2124 provide independent programmable receive FIFO trigger point setting for each channel to generate a corresponding receive FIFO trigger interruption.

When receiving FIFO trigger interruption enabled, the corresponding interruption occurs when the number of data in receiving FIFO is greater than or equal to the set trigger point.

10.2.3 Transmit FIFO Enable/Disable

After reset, the transmit FIFO is disabled. If you want to write data to the transmit FIFO, you need to enable the transmit FIFO first.

Whether the data in the transmit FIFO is transmitted depends on whether the corresponding sub-channel UART is enabled. Once the corresponding sub-channel UART is enabled, the data in the transmit FIFO will be sent immediately. Otherwise, the data in the transmit FIFO will not be transmitted until the corresponding sub-channel is enabled.

10.2.4 Receive FIFO Enable/Disable

After reset, the receive FIFO is disabled. If you want to receive sub-serial data, you need to enable the corresponding sub-serial channel and its receive FIFO first. The received data can be written to the receive FIFO memory only after the corresponding UART and receive FIFO are enabled.

If the sub-serial channel is enabled and the receive FIFO is disabled, the sub-serial can receive data,but the data is not written to the receive FIFO and is ignored.

10.2.5 Transmit FIFO Empty

When the TFRST is set to 1 in the FCR, the data in the FIFO will be cleared and the FIFO counter and pointer will be cleared.

When the TFRST bit is set to 1, it will be automatically cleared by hardware after a clock.

10.2.6 Receive FIFO Empty

When receiving FIFO clearance (RFRST) in FCR is set to 1, the data in receiving FIFO in this Sub-channel will be cleared, and the receiving FIFO counter and pointer will be cleared.

When the RFRST bit is set to 1, it will be automatically cleared by hardware after a clock.

10.2.7 Send FIFO Counter

WK2124 uses an 8-bit register to reflect the number of data currently sent in FIFO. When a byte of data is written to send FIFO, the sending FIFO counter automatically adds 1; when a sending FIFO data is sent, the sending FIFO counter automatically subtracts 1.

Note: When sending FIFO counter 255 (11111111111), if another data is written, the counter becomes 0 (00000000). When the FIFO counter is sent to 1 (00000001), after sending a data, the counter is also changed to 0 (00000000). Therefore, when the sending FIFO counter is 0, it indicates that the sending FIFO is full or empty. In this case, it is necessary to combine the relevant state bits in the sub-serial port state register (FSR) to judge.

10.2.8 Receive FIFO Counter

WK2124 uses an 8-bit register to reflect the current number of data received in FIFO: when a byte of data is written to receive FIFO, the receiving FIFO counter automatically adds 1; when a receiving FIFO data is read, the receiving FIFO counter automatically subtracts 1

Note: When receiving FIFO counter 255 (11111111111), if another data is received, the counter becomes 0 (00000000). When the receiving FIFO counter is 1 (00000001), after reading a data, the counter also changes to 0 (00000000). Therefore, when the receiving FIFO counter is zero, it indicates that the receiving FIFO is full or empty. In this case, it is necessary to combine the relevant state bits in the sub-serial port state register (FSR) to judge.

11. Parameter Index

11.1 Static Parameter of WK2124

Unless otherwise specified, it satisfies: VCC=(2.5V±0.2V) or (3.3V±0.3V) or (5V); -40℃ ~ +85℃.

Symbol	Description	Condition	VCC=2.5V		VCC=3.0V		VCC=5.0V		Unit
			Min	Max	Min	Max	Min	Max	
power supply									
VCC	voltage		2.3	2.7	3.0	3.6	4.5	5.0	V
ICC	Working current	3.6864MHz crystal oscillator without load	0.8	2	1	2	2	3	mA
ICCSL	Dormancy current		150	-	200	-	460	-	uA
Input logic signal									
VIH	Input high level		1.8	5.0	2.0	5.0	3.6	5.0	V
VIL	Input low level		-	0.6	-	0.9	-	1.1	V
IIL	Input leakage current	VI=5.0 or 0V	-	±10	-	±10	-	±10	uA
CI	Input capacitance		-	5	-	5	-	5	pF
Output logic signal									
VOH	Output high level	IOH=3mA	1.9	–	2.4	–	4.5	–	V
VOL	Output low level	IOL=-3mA	-	0.4	-	0.4	0	0.4	V
IOL	Output leakage current		-	±10	-	±10	-	±10	uA
Co	Output capacitance		-	5	-	5	-	5	pF

11.2 Dynamic Parameter of WK2124

Symbol	Description	Condition	VCC=2.5V		VCC=3.0V		VCC=5.0V		Unit
			Min	Max	Min	Max	Min	Max	
FOSI	Crystal frequency		-	16	-	24	-	32	MHz

11.3 Limit Parameter of WK2124

Symbol	Description	Condition	Min	Max	Unit
VCC	voltage		-0.5	5	V
VI	input voltage		-0.5	+5.5	V
VO	output voltage		-0.5	+5.5	V
PTOL	total power consumption		-	300	mW
TO	operating temperature		-40	+85	℃
TSTG	storage temperature		-65	+150	℃

11. Package Information

WK2124 in SSOP20 lead-free green package

size / Label	Min（mm）	Max（mm）	size / Label	Min（mm）	Max（mm）
A	7.15	7.25	C3	0.152	
A1	0.30TYP		C4	0.172	
A2	0.65TYP		H	0.05	0.25
A3	0.525TYP		θ	12° TYP4	
B	5.25	5.35	θ1	12° TYP4	
B1	7.65	7.95	θ2	10° TYP	
B2	0.60	0.80	θ3	0° ～ 8°	
C	1.45	1.55	R	0.20TYP	
C1	1.65	1.85	R1	0.15TYP	
C2	0.674				

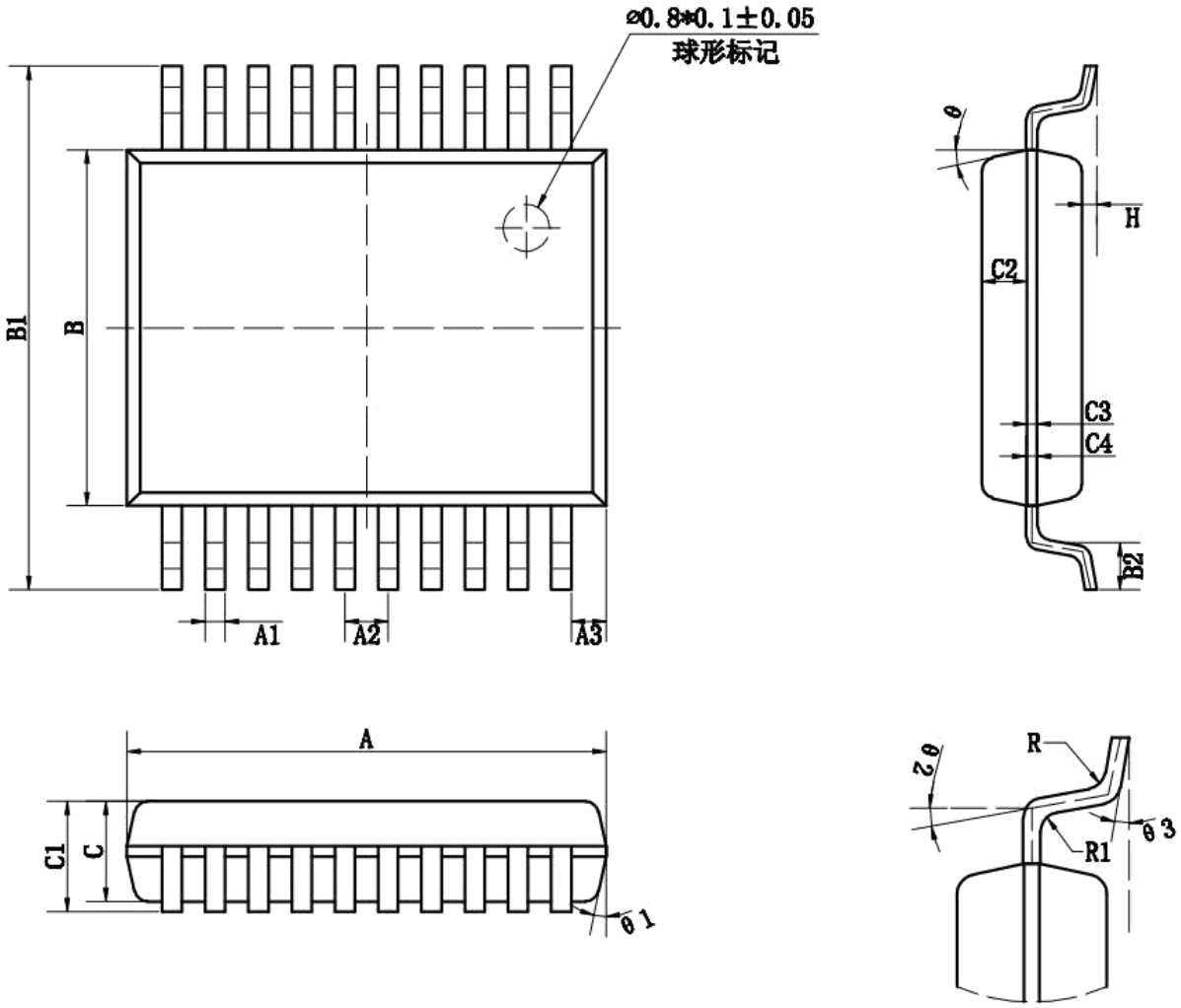


Figure 12.1 SSOP20 Package Information

13. Welding Process

WK2124 uses green environmental protection materials and pure tin plating for pins. It is recommended to use reflow soldering process with peak temperature less than 260 C and conforming to lead-free standard for soldering.

All SMD welding processes are sensitive to humidity (humidity level and conditions are shown in the package). Drying treatment is recommended before welding.

When manual welding is used, the pins of two diagonal lines should be fixed first and then the other pins should be welded. Welding temperature is 300 C, the contact time between soldering iron and pin is controlled within 10 seconds.

14. Special Statement

This product is not designed for the life support system, aerospace system design, the application of this product in the field of all consequences ,WEIKAI Microelectronics no responsibility will be assumed.

WEIKAI microelectronics, reserve the right to modify the performance, function and parameters of the product is reserved. For formal mass-produced products,modifications made will be notified to the user by announcement.

15. Version History

Previous versions of V1.0 were internal versions that were not officially disclosed.

version	Date of publication	Modify content
V1.0	2014.11	Create a file
V1.1	2017.09	Packaging information

16. Contact Information

Please visit our website to get our latest contact information: www.wkmic.com.