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EXPERIMENT 2. PROGRAMMING BOTH MYRIO CPU AND FPGA

LABORATORY REPORT

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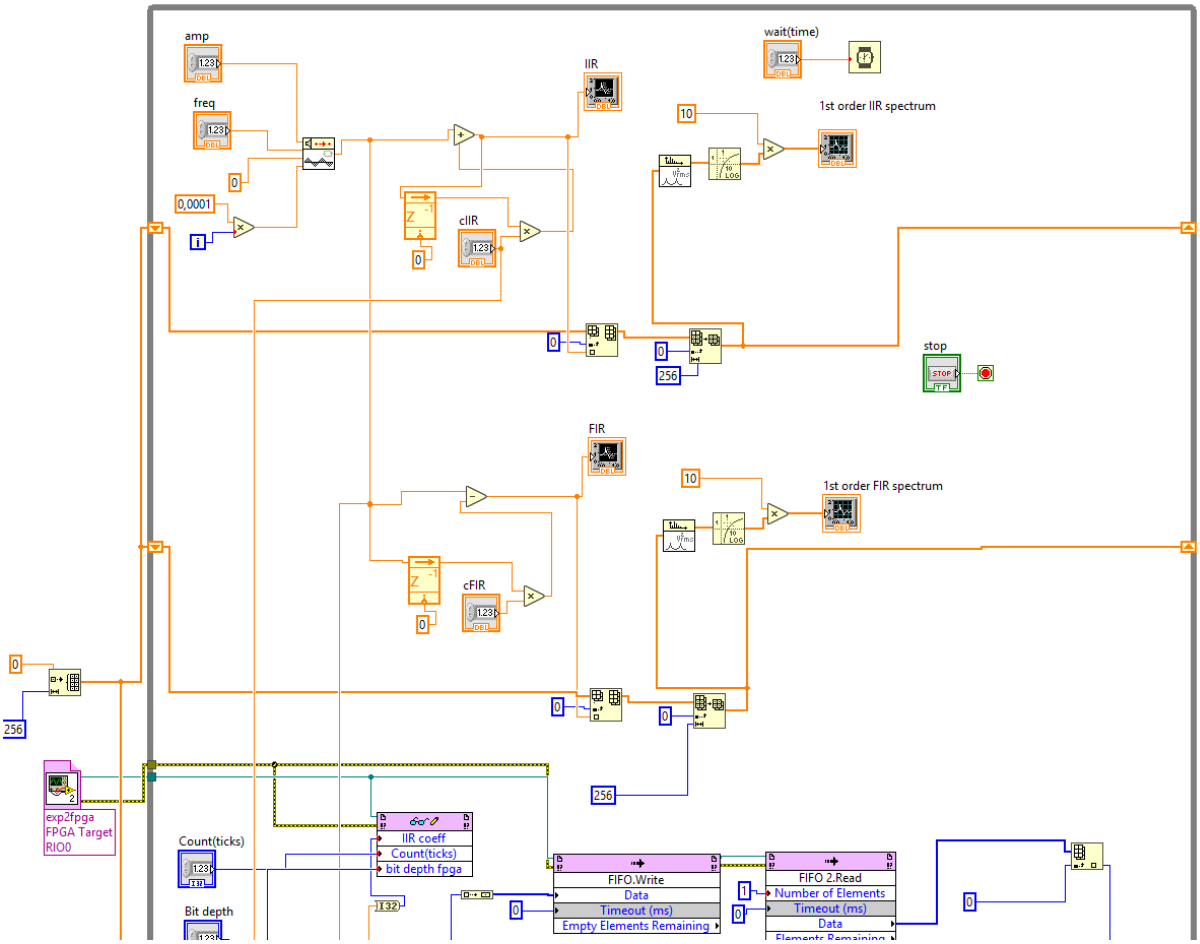
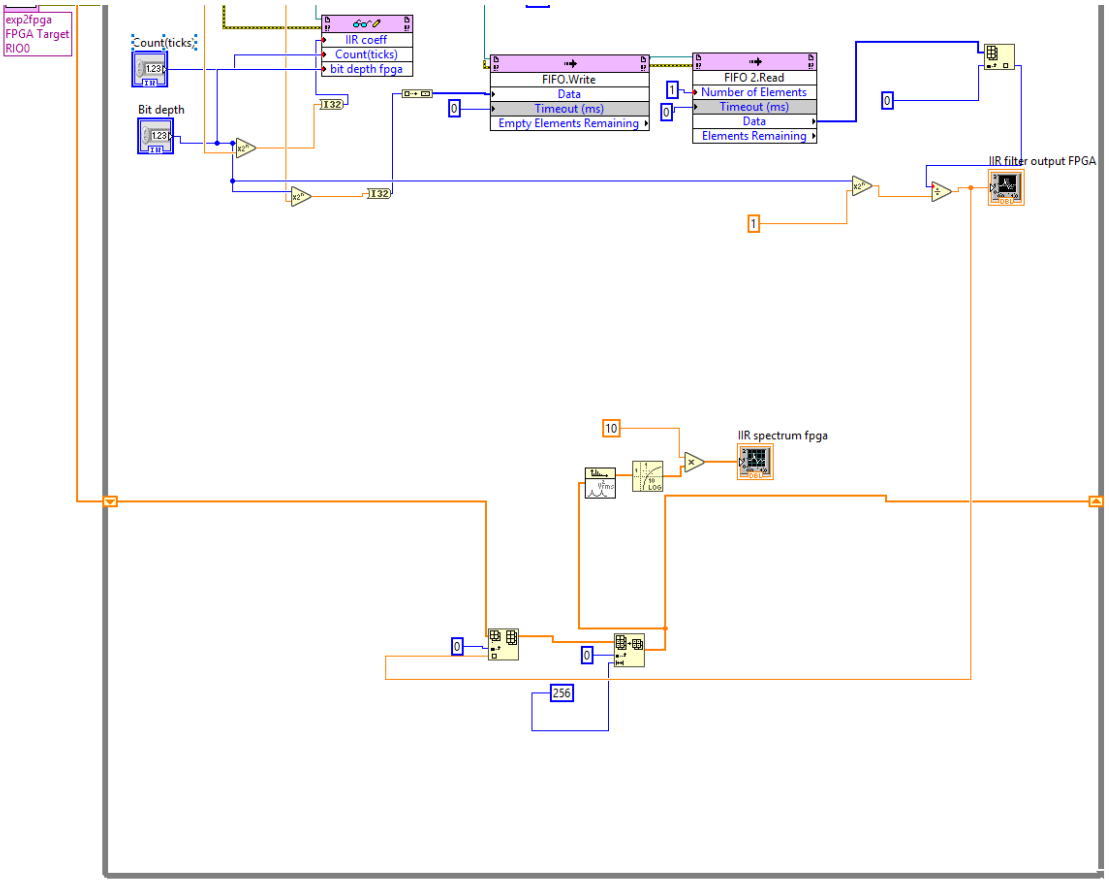
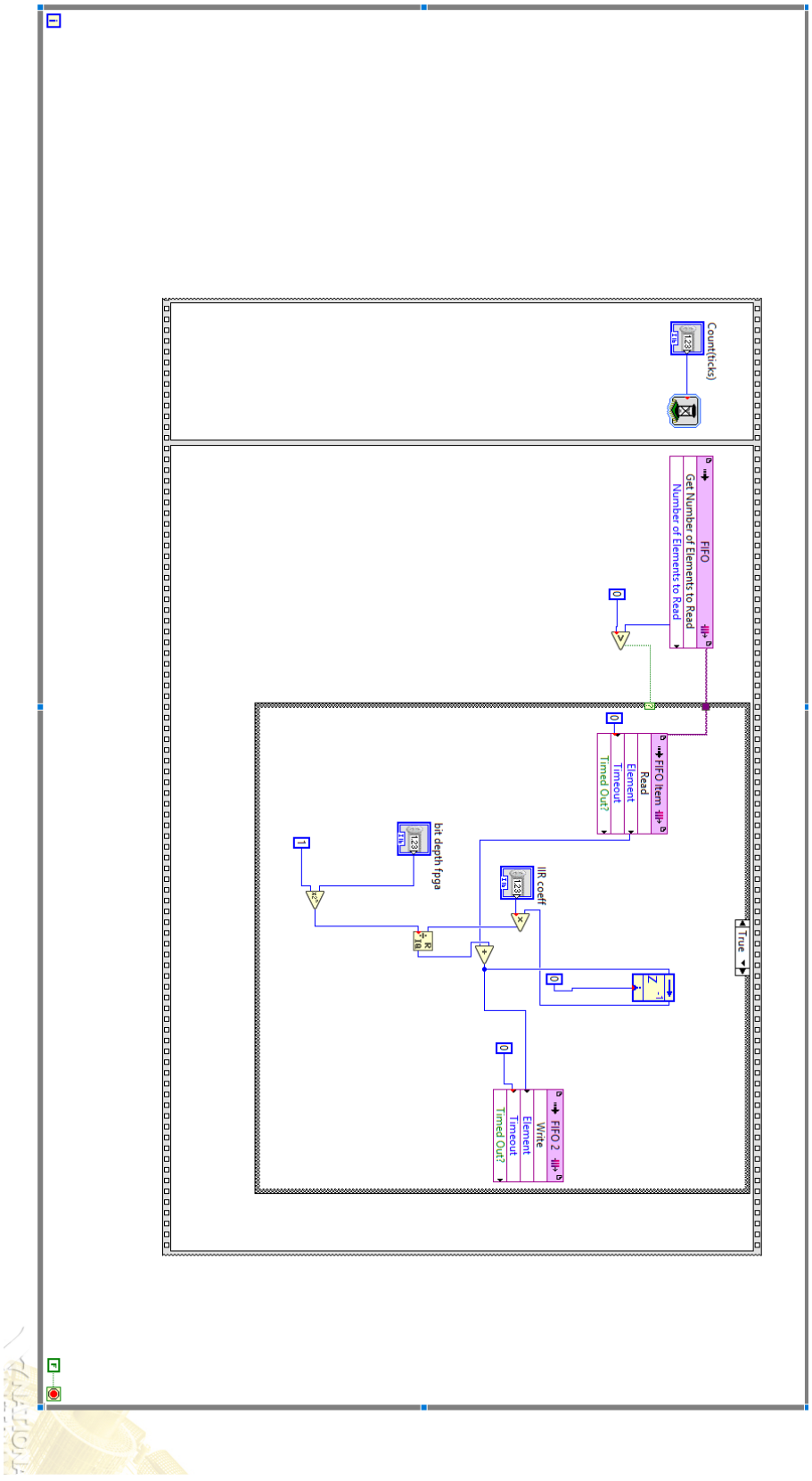
- Place the screenshot of the final version of **block diagram** of **Run_from_myRIO.vi** (myRIO CPU VI) to the space below. Please note that the details should be **clearly visible**. You can use ***Snipping Tool***.



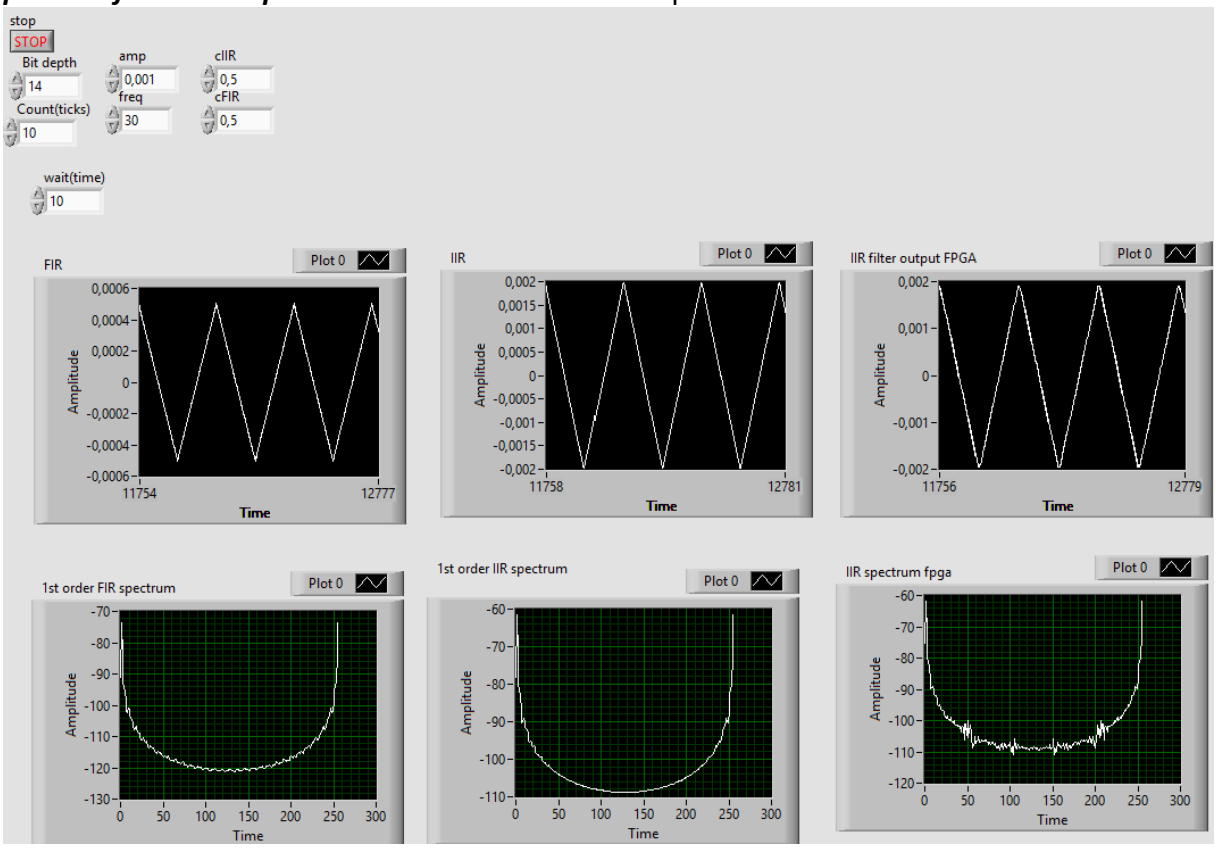

exp2fpga
FPGA Target
RIO0
Count(ticks)
Bit depth
IIR coeff
Count(ticks)
bit depth fpga
FIFO.Write
Data
Timeout (ms)
Empty Elements Remaining
FIFO 2.Read
Number of Elements
Timeout (ms)
Data
Elements Remaining
IIR filter output FPGA
IIR spectrum fpga
10
256

- Place the screenshot of the final version of **block diagram** of **FPGA VI** to the space below. Please note that the details should be **clearly visible**.

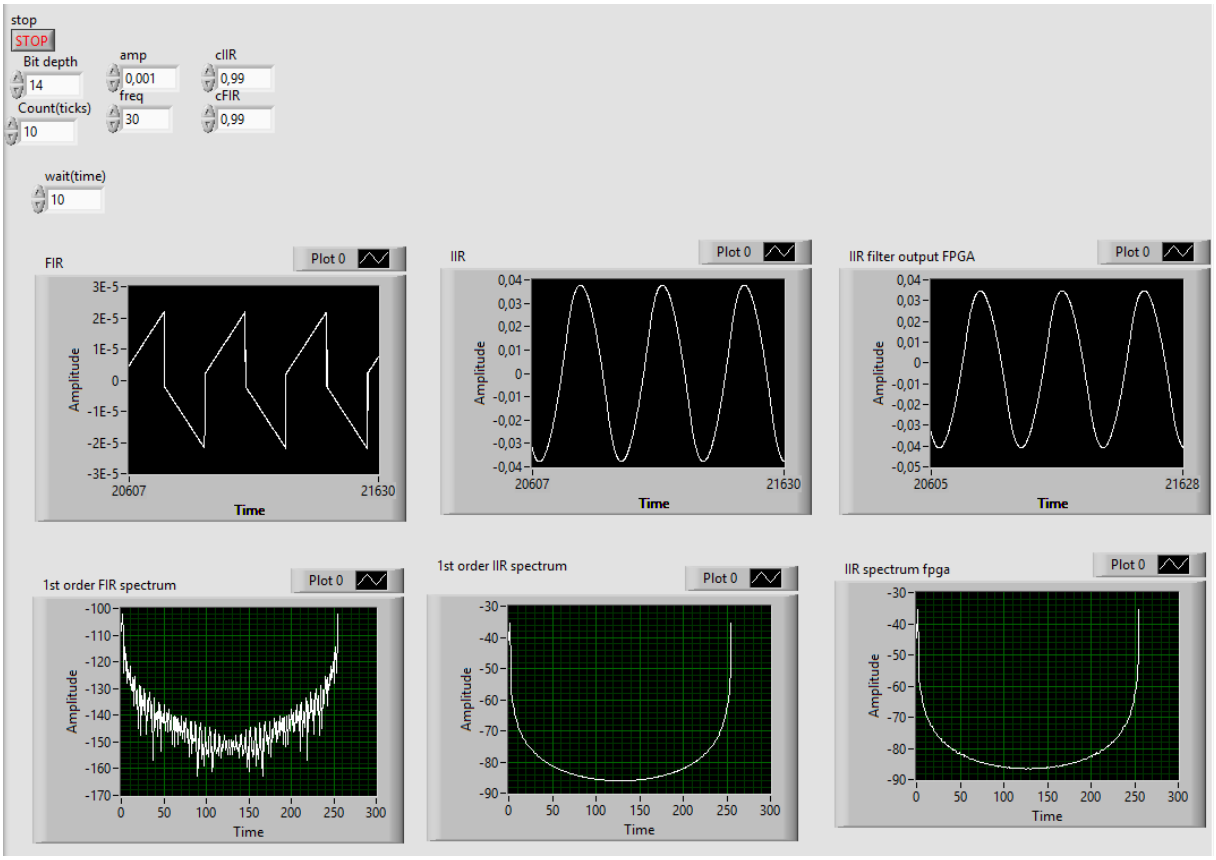


iii) Set ***amplitude*** and ***frequency*** of Triangular waveform as ***0,001*** and ***30***, respectively. Set ***wait(ms)*** and ***Count(Ticks)*** as ***10***.

iv) Choose the ***IIR and FIR filter coefficients*** as ***0.5*** and ***Bit Depth*** as ***14***. ***Note*** and ***plot the filtered outputs*** for both ***CPU*** and ***FPGA*** implementations.



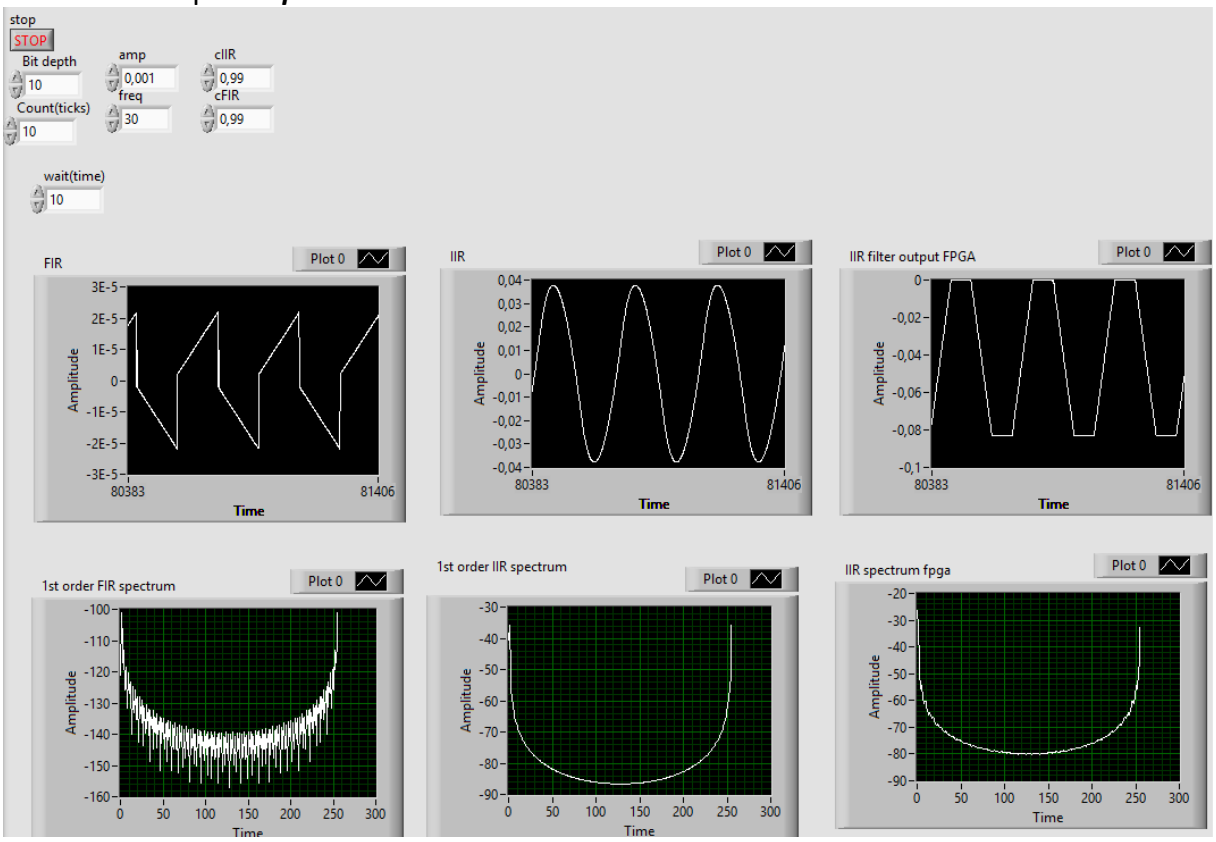
v) Change ***filter coefficients*** as ***0.99***. ***Note the changes*** in ***myRIO CPU and FPGA*** implementations. ***Plot*** the results. ***Comment*** on the results. What happens to ***FIR filter output***? Does it ***change significantly***?



The order is 1 in both filters. When we increase the coefficient, it does not let the high frequencies pass and even sharp low pass occurs. Therefore, something close to pure sine occurs in IIR cases.

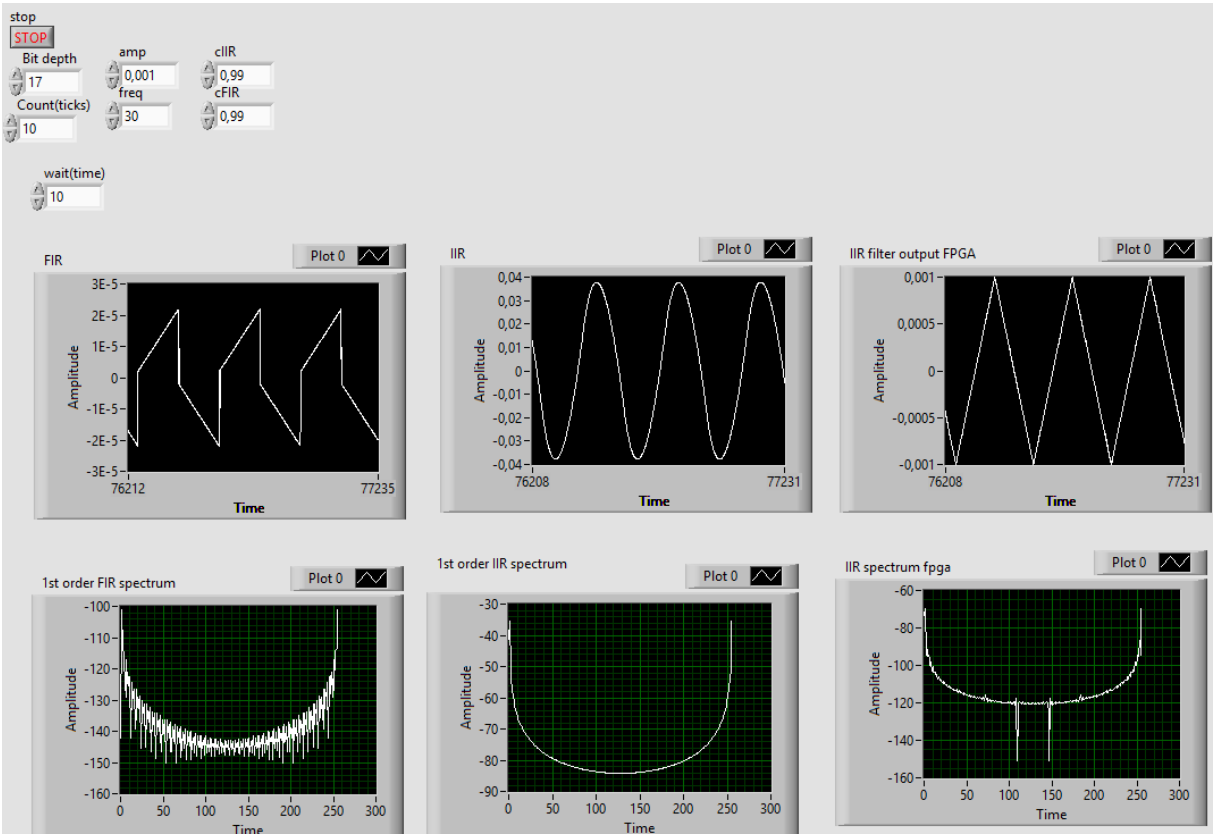
In the FIR case there is no feedback therefore low order is not enough to show low pass characteristic. When it is considered in time domain, it erases the previous values since the coefficient is high.

vi) ***Decrease Bit Depth*** one by one from ***14*** to ***10***. ***Note the changes*** in the ***FPGA*** output. ***Explain*** them.



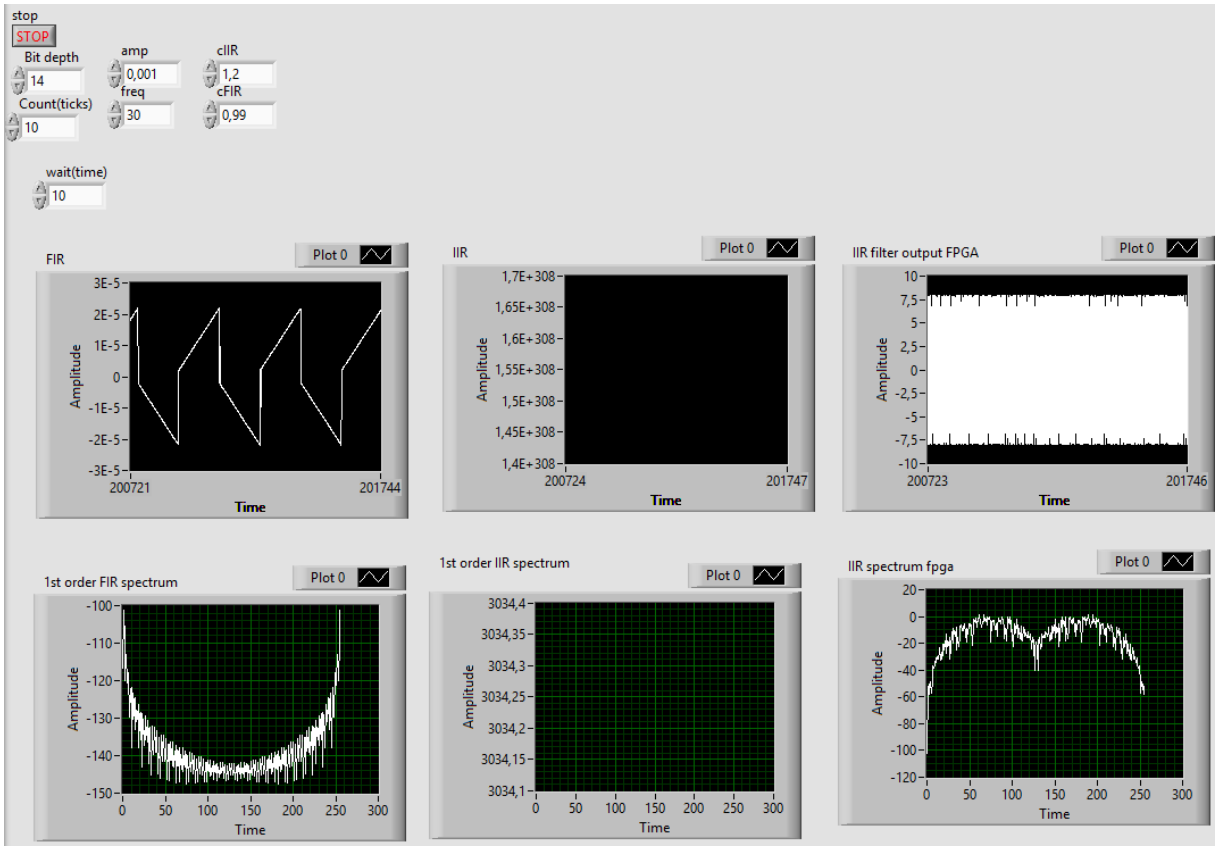
Since the useful bits are decreased, during quantization we cannot see all the details. The bits are not enough to show details. Therefore, we see saturation due to bad resolution.

vii) Now, ***increase Bit Depth*** from ***14*** to ***17*** one by one and ***note the changes***. ***Why*** do we observe such a response for the ***FPGA implementation*** which is ***different than the CPU implementation*** in myRIO?



When we use 17 instead of 10, we scale the values with 2(17). However, the allowable bit is less than 17, therefore overflow occurs and we actually use same useful bits due to FPGA's capabilities. While using FPGA with this configuration the upper bound will not affect the result.

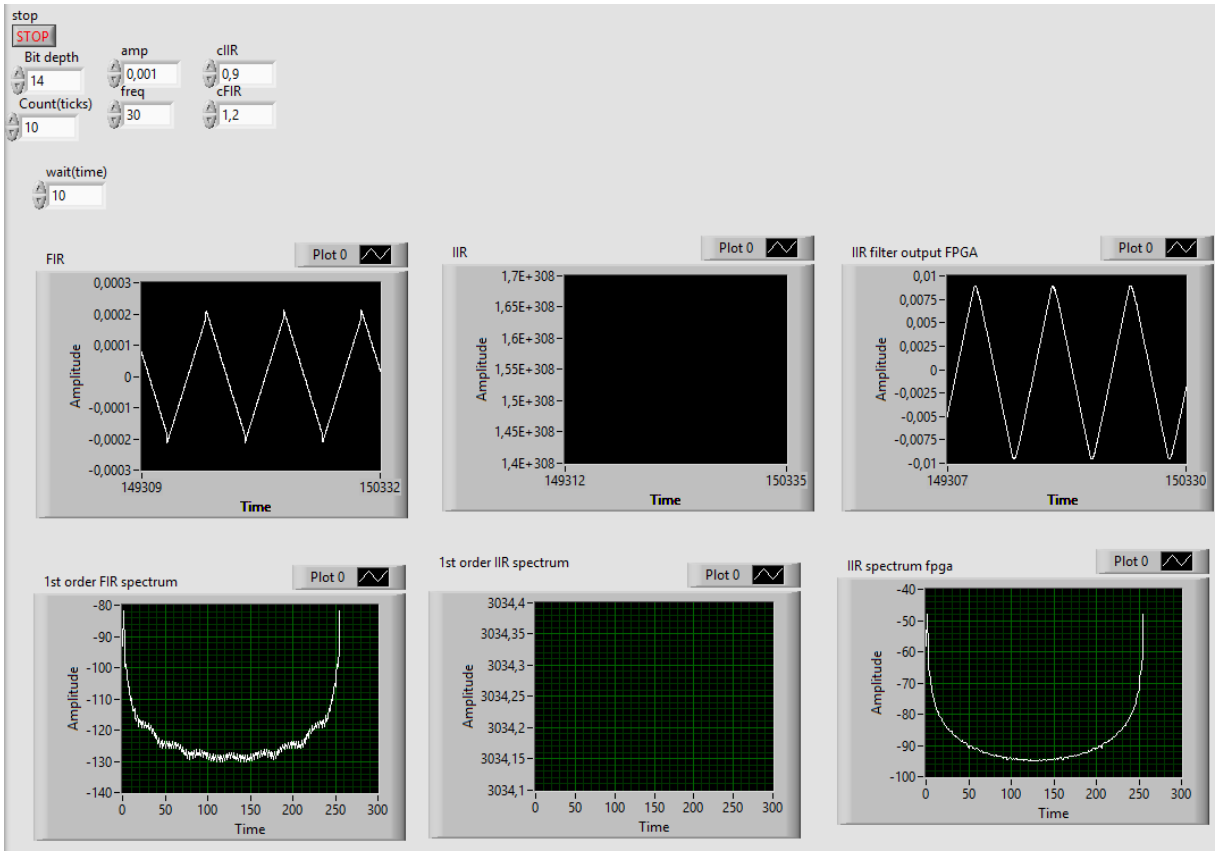
viii) Change the ***IIR filter coefficient*** to ***1.2***. ***Why*** do we observe such a response for both of the implementations in myRIO?



For IIR(CPU case), the poles are moved to out of unit circle. Therefore, IIR filter is not stable anymore.

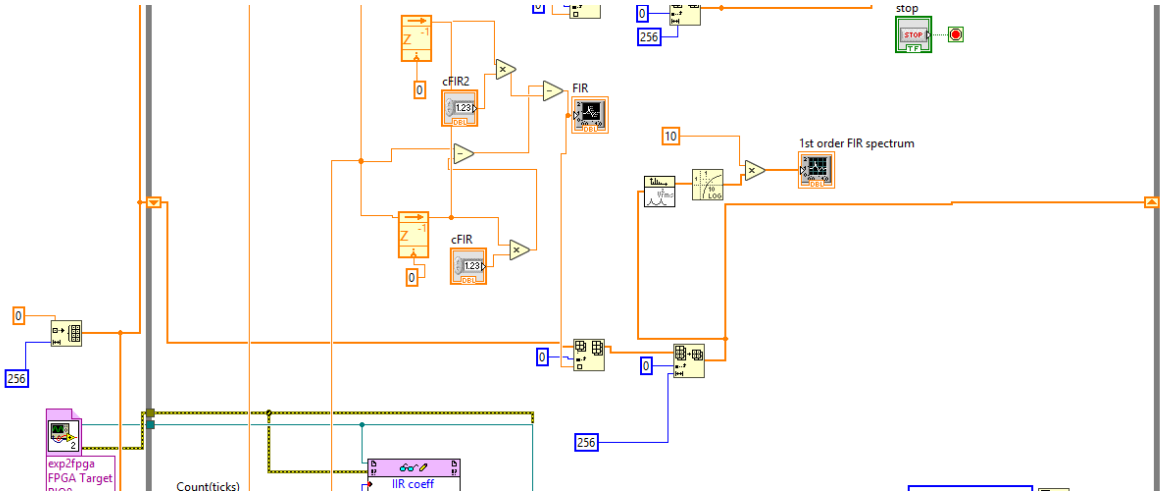
For FPGA IIR case it tries to jump between high values whereas it can only show between -8 and 8. Therefore it jumps quickly between -8 and 8, in other words it is also unstable.

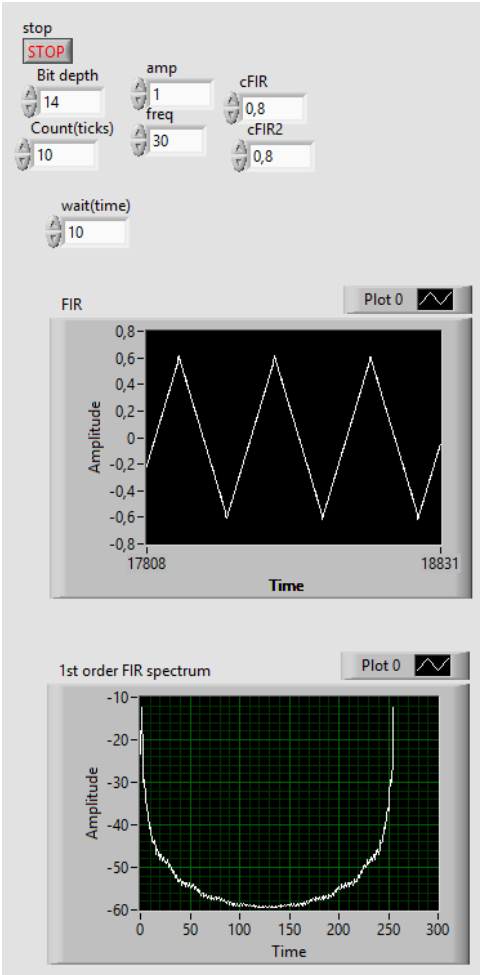
ix) Change the ***FIR filter coefficient*** as ***1.2***. ***Why don't we see a similar change for the FIR filter***?



In the FIR(CPU case) the poles are at 0 anyways. Therefore, it is still stable but the gain becomes low. Therefore, the signal can pass less but it is stable.

BONUS





Additional order is implemented. After that better power spectrum is observed since the order is increased. However there is not a significant change in time plot.