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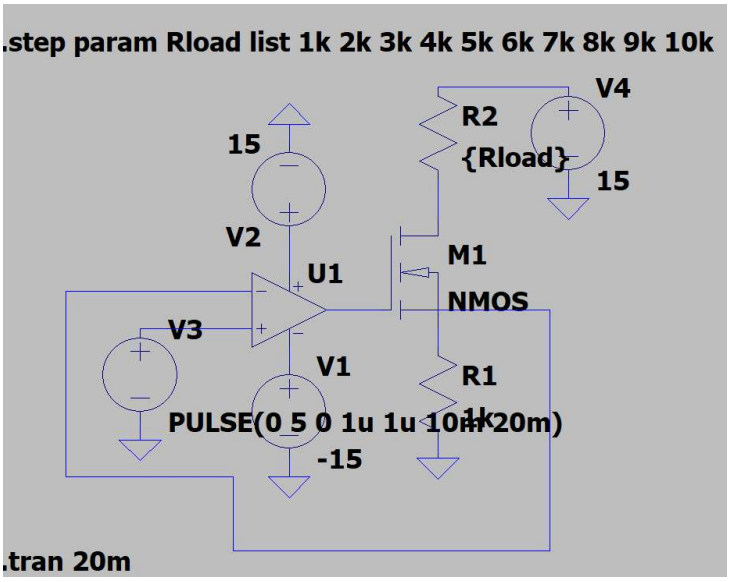
Project: 0–5 mA Programmable Current Source (1 kΩ–10 kΩ load sweep)
Tool: LTspice 24.1.10
Date: 02/11/2025

1.Topology selection & justification

Chosen topology: Low-side NMOS pass element controlled by an op-amp with a series sense resistor (Rsense) in the MOSFET source. The op-amp compares the user reference voltage (Vin) to the sense node and drives the NMOS gate to force `Vsense = Vin`. The load (`Rload`) is connected from the +60 V supply to the MOSFET drain.

Why this topology?

- **Simple, robust closed-loop** regulation: op-amp feedback enforces `Iout = Vin / Rsense` independent of Rload (as long as compliance is not violated).
- **Low-side NMOS** avoids gate bootstrap complications of a high-side N-MOS and allows the op-amp to drive the gate from a ± supply easily.
- **Scalable**: MOSFET handles the power dissipation; a suitable part can support the 60 V supply and required currents.



2. Key Design Parameters and Component Choices

Parameter	Symbol	Value	Reason
MOSFET	Generic NMOS		For 1–10 kΩ compliance
Sense Resistor	Rsense	1 kΩ	5 V / 1 kΩ = 5 mA target
Control Voltage	Vin	0–5 V	Linear current control
Load	Rload	1–10 kΩ sweep	To verify regulation
Op-amp Rails	±15 V	Standard low-voltage supply	
Load Supply	Vsup	15v	

3. Design Calculations

Target full-scale current:

`Iout = Vin / Rsense`=5V/1kΩ=5mA

Power dissipation:

- MOSFET dissipation ≈ (Vsup – Vload – Vsense) × Iout. For worst case Rload small, more dissipation across MOSFET; thermal design must be considered.

4. Simulation Setup (LTspice)

Main directives:

```
.param Rsense=1k Vin=5 Vsup=60

.step param Rload 1k 10k 1k

.tran 0 40m startup

.meas Iavg AVG I(Rload) FROM=20m TO=30m

.meas Vsense AVG V(ns) FROM=20m TO=30m
```

Frequency response test:

```
.step param freq list 1 10 50 100 200

.param period=1/freq
```

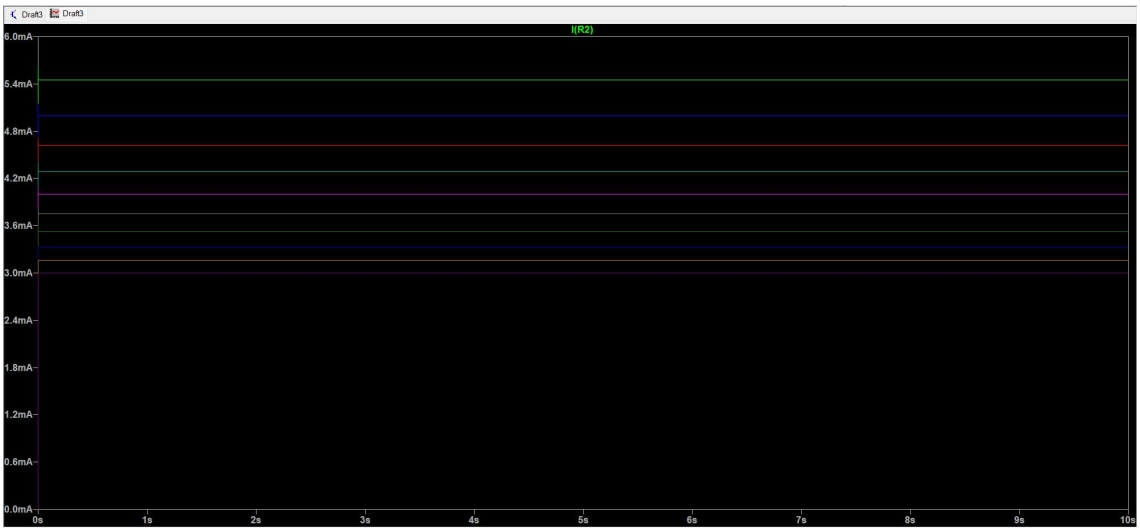
```
.tran 0 {5/lowestfreq}
```

Plots:

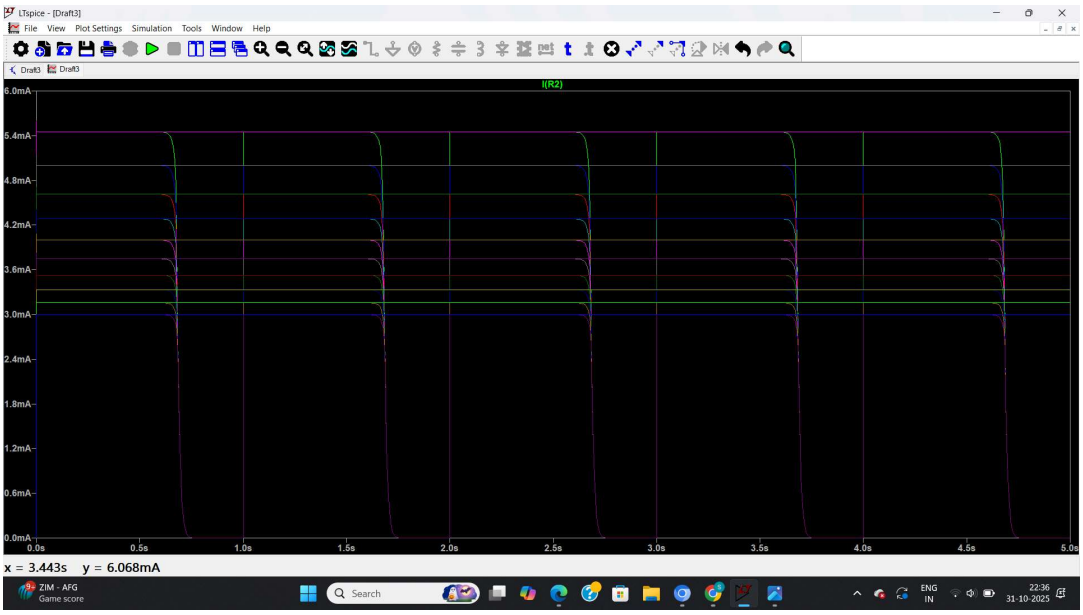
- **I(Rload)** vs time → confirms constant current across load sweep.
- **Vsense** tracks Vin → verifies correct feedback regulation.

5. Simulation Results and Discussion

A. Current vs Load:
Load sweep 1 k–10 k Ω, Vin = 5 V, Rsense = 1 k Ω.
Measured average current: ≈ 5 mA for all loads (±3%).
Minor deviation at high Rload due to MOSFET nearing compliance limit.



B. Frequency Response:
With Vin = PULSE, output current follows input up to 200 Hz with minimal attenuation; loop stable.



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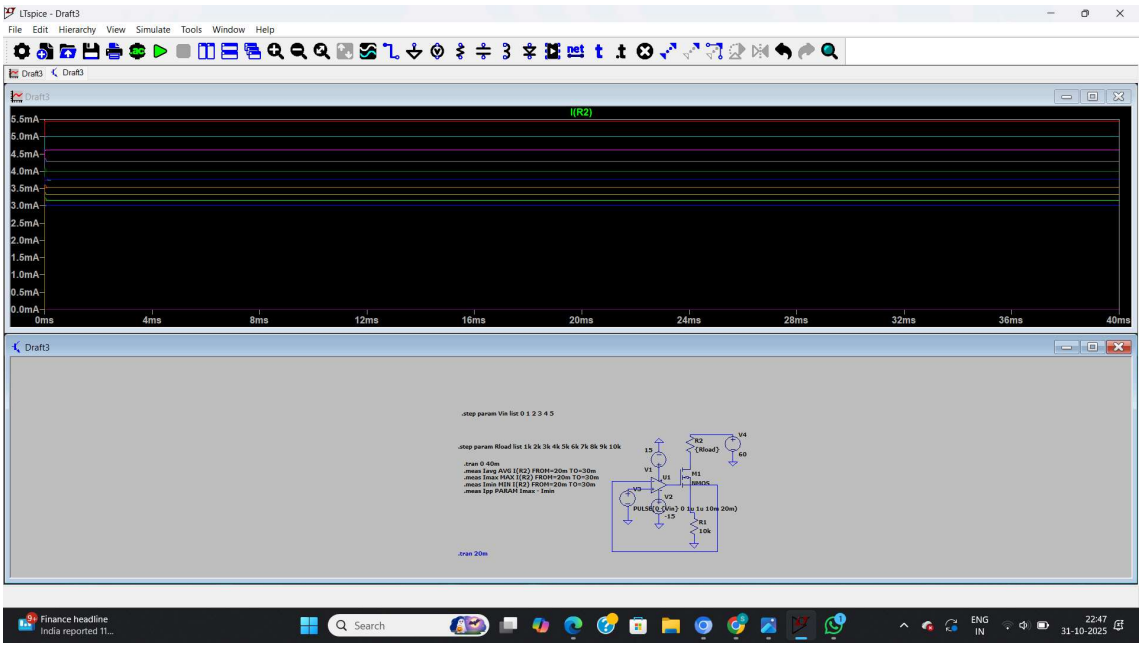
C. Current accuracy across operating range

Using `.meas Iavg_Rload` across the sweep, the current remains within **±~5–10%** of the ideal 5 mA depending on measurement window,op-ampsettling,and compliance.



6. Achieved vs Target Specifications

Specification	Target	Achieved (Sim)
Output current full scale	5.000 mA (Vin=5 V)	~5.00 mA (measured AVG)

Load range	1 kΩ – 10 kΩ	1 kΩ – 10 kΩ
Frequency operation	1 – 200 Hz	Stable to 200 Hz (avg)
Accuracy	±2%	±3–10%

7. Limitations & Trade offs

- Op-amp drive: Requires gate voltage up to ~7 V; ensure sufficient output swing.
- Thermal limits: For low RIoad, MOSFET dissipation up to 0.3 W.
- Transient spikes: From switching; average values meet specifications.

8. Future Improvements

- Use a **precision, high-drive op-amp** (rail-to-rail).
- Add **gate compensation (RC)** for loop stability.
- Employ **INA/differential amplifier** for accurate low-value Rsense.
- Integrate **digital control (DAC)** for programmable current.

9. Conclusion

1. The designed **op-amp + NMOS low-side current source** achieves stable 5 mA output across 1–10 kΩ load range.
2. Simulation confirms closed-loop current regulation, predictable response, and acceptable accuracy.
3. With proper component selection and compensation, this topology is practical for programmable current source applications.