High Density Single Port SRAM RVT-HVT-RVT Compiler
CLN40G 40nm Process
256 Rows Per Bank, 0.299um^2 Bit Cell
512 Words X 64 Bits, Mux 16 Instance

Overview

The Synchronous Single-Port Ram is optimized for speed and density. The memory is designed to take full advantage of the TSMC 40nm CLN40G CMOS process.

The storage array is composed of six-transistor bit cells with fully static circuitry. The SRAM operates at a voltage of 0.9V to 0.9V and a junction temperature range of 25.0°C to 25.0°C.

Instance Settings

Parameter	Setting
Instance Name	sram_sp_512x64
Process	CLN40G
Words	512
Bits	64
Mux	16
Write Mask	off
Extra Margin Adjustment	on
Redundancy	off
Soft Error Repair	none
BIST Muxes	on
Output Drive	6
Power Routing Type	otc
Top Metal	M5-M9
Frequency	100 MHz
Power Gating	off
Retention	on
Back Biasing	off
Weak Bit Test	off
Read Disturb Test	off
Pipeline	off
Write-thru	on

Description

The single-port synchronous RAM is a fully static memory with write enable (WEN), chip enable (CEN), address (A), data in (D) and data out (Q) pins. The RAM is self-timed and consumes the minimum amount of power for read or write operations.

All synchronous inputs are latched on the rising-edge of the clock signal. When CEN is low and WEN is high the memory will read. When CEN and WEN are both low the word on the D will be written to the memory.It will appear at the outputs (write-thru).

When CEN is high the memory is deselected and forced into a low-power standby mode. Stored data is fully retained but memory access is disabled for data read or data write, the existing data outputs continue to drive their previous values.

Description (cont)

The Self timing overrride STOV allows you to adjust the latching of output in posedge or negedge of the clock.

The Extra Margin Adjustment EMA ,Sense amp Extra margin adjustment EMAS and Write Extra margin adjustment EMAW allows you to adjust the width of the self timing pulse.

BIST muxes with test inputs, test enable (TEN) and test outputs are connected to each input.

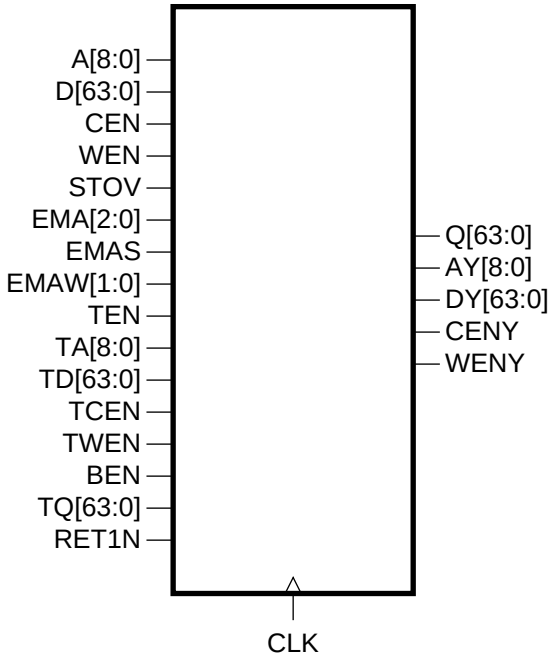
Memory normal mode is enabled (RET1N=1). In this mode the core and periphery power are both connected to the chip level power grid either through power rings or through Artigrid

Refer to the users manual for a more detailed description of memory operation.

Physical Dimensions

Area Type	Width (μm)	Height (μm)	Area (μm^2)
Core	891.03	62.98	56117.1

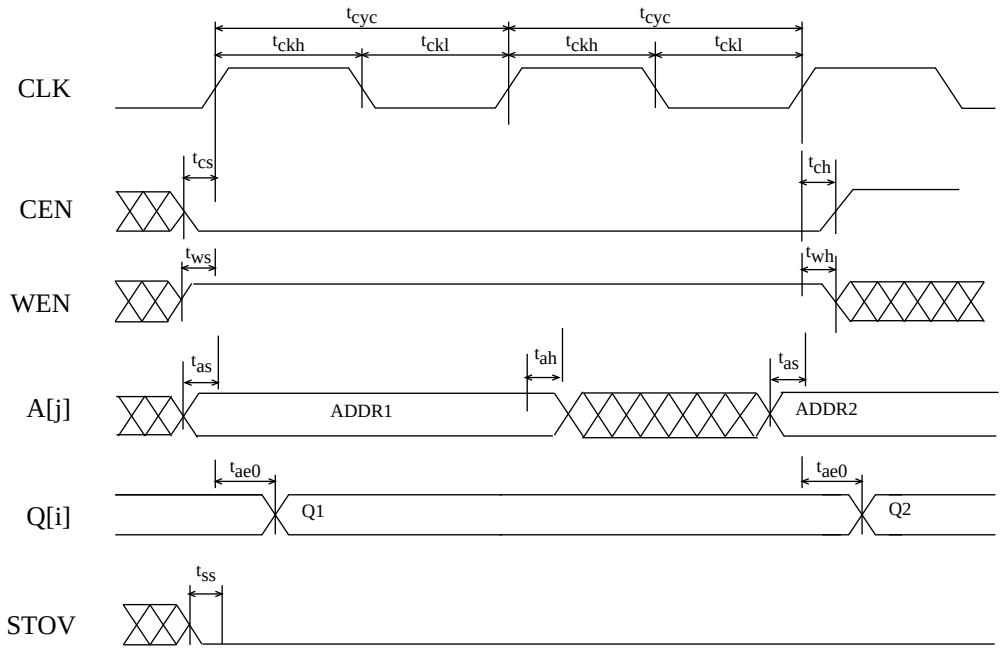
Symbol



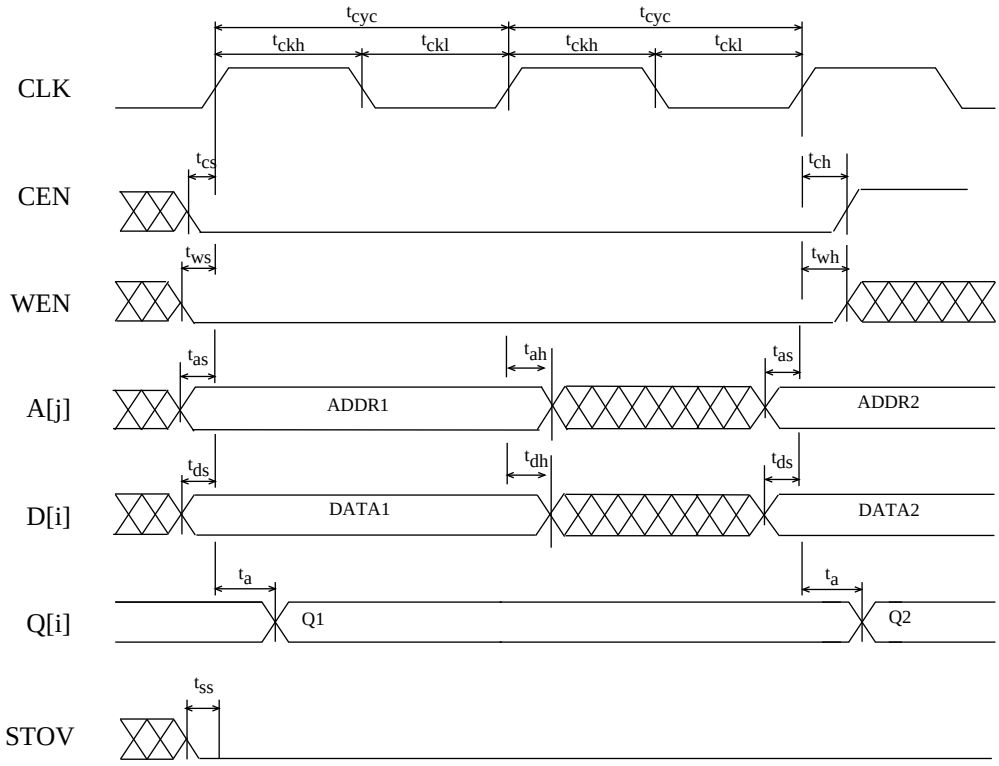
Pin Description

Pin	Description
A[8:0]	Address (A[0] = LSB)
D[63:0]	Data Input (D[0] = LSB)
CLK	Clock
CEN	Chip Enable (active low)
WEN	Write Enable (active low)
Q[63:0]	Data Output (Q[0] = LSB)
EMA[2:0]	Extra Margin Adjustment (EMA[0] = LSB)
EMAS	Sense amp Extra Margin Adjustment (EMAS)
EMAW[1:0]	Write Extra Margin Adjustment (EMAW[0] = LSB)
TEN	Test Mode Enable (active low)
TA[8:0]	Address Test Input (TA[0] = LSB)
AY[8:0]	Address Mux Output (AY[0] = LSB)
TD[63:0]	Data Test Input (TD[0] = LSB)
DY[63:0]	Data Mux Output (DY[0] = LSB)
TCEN	Chip Enable Test Input (active low)
CENY	Chip Enable Mux Output
TWEN	Write Enable Test Input (active low)
WENY	Write Enable Mux Output
BEN	Bypass Mode Enable (active low)
TQ[63:0]	Test mux Q Input (TQ[0] = LSB)
RET1N	Retention Input (active low)
STOV	Self timing override

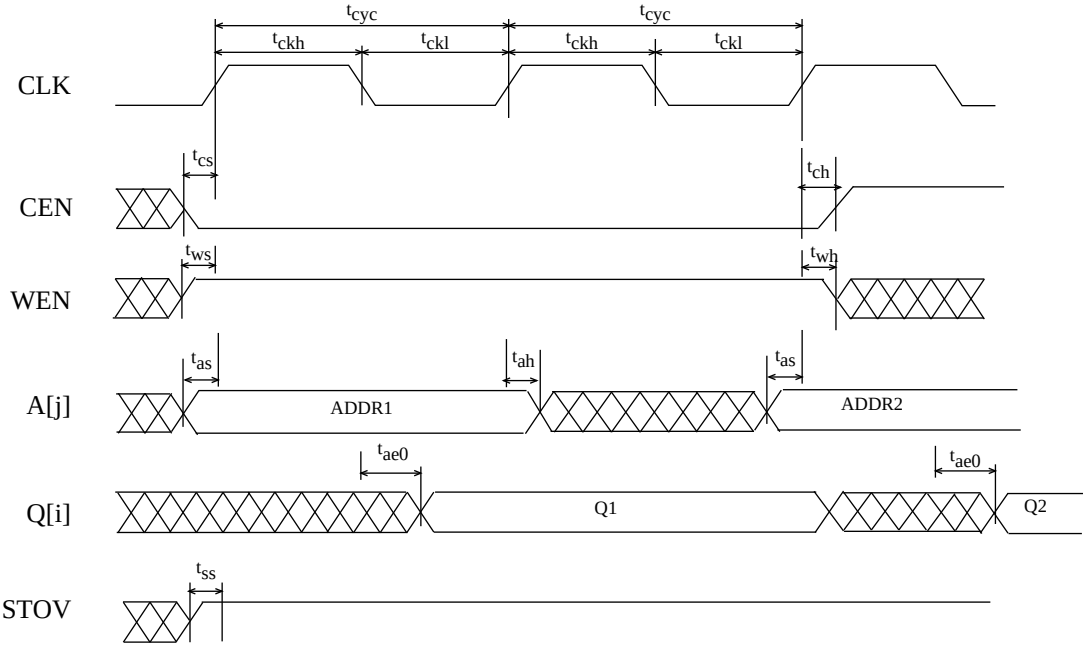
Read Cycle Timing stov=0



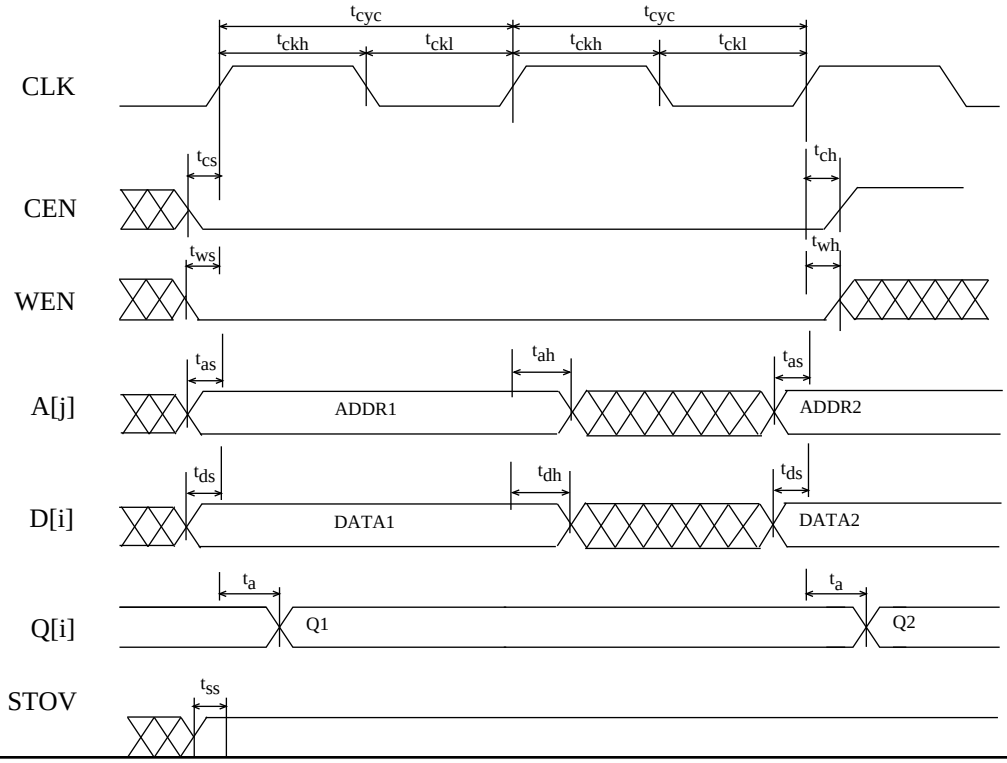
Write Cycle Timing stov=0



Read Cycle Timing stov=1



Write Cycle Timing stov=1



Timing (units = ns)

The timing tables shows delay values measured from the input threshold to the output threshold.
The timing and power values are measured at input slew of 0.1ns on clock pin, 0.1ns on signal pins and output load 0.05pF.

Pin	Symbol	Typical Process 0.9V, 25°C	
		Min	Max
Read Cycle	t_{cyce0}	0.778	
Write Cycle	$t_{cyce0ew0}$	0.778	
Read Access[1,2]	t_{ae0}		0.661
Write-Thru Access[1,2]	t_a		0.568
Clock high	t_{ckh}	0.081	
Clock low	t_{ckl}	0.083	
Clock rise slew	t_{ckr}		0.545
CENY load factor[3]	$K_{cenyload}$		0.841
AY load factor[3]	K_{ayload}		0.841
DY load factor[3]	K_{dyload}		0.814
WENY load factor[3]	$K_{wenyload}$		0.841
Q load factor[3]	K_{qload}		0.315
A setup	t_{as}	0.196	
A hold	t_{ah}	0.160	
D setup	t_{ds}	0.028	

Timing continued (units = ns)

Pin	Symbol	Typical Process 0.9V, 25°C	
		Min	Max
D hold	t_{dh}	0.138	
CEN setup	t_{cs}	0.127	
CEN hold	t_{ch}	0.166	
WEN setup	t_{ws}	0.108	
WEN hold	t_{wh}	0.160	
STOV setup	t_{ss}	0.781	
STOV hold	t_{sh}	0.778	
RET1N setup	t_{ret1ns}	1.482	
RET1N hold	t_{ret1nh}	0.778	
RET1N fall to TCEN rise hold	t_{ret1n_tcenh}	0.778	
TCEN fall to RET1N rise hold	t_{tcen_ret1nh}	1.309	
RET1N fall to CEN rise hold	t_{ret1n_cenh}	0.778	
CEN fall to RET1N rise hold	t_{cen_ret1nh}	1.309	

[1]Output delays and a load dependency (Kload) which is used to calculate:*TotalDelay = FixedDelay + (Kload x Cload).*
[2]Access time is defined as the longest possible delay to valid output for the typical and slow corners, and the shortest possible delay for the fast corners.
[3]The output load factor units are ns/pF.

Cycle and Access Timing for Different Values of Extra Margin Adjustment (units = ns)

Pin	Symbol	Typical Process 0.9V, 25°C	
		Min	Max
Read Cycle EMA=0	t_{cyce0}	0.778	
Read Cycle EMA=1	t_{cyce1}	0.836	
Read Cycle EMA=2	t_{cyce2}	0.858	
Read Cycle EMA=3	t_{cyce3}	0.880	
Read Cycle EMA=4	t_{cyce4}	0.915	
Read Cycle EMA=5	t_{cyce5}	0.980	
Read Cycle EMA=6	t_{cyce6}	1.043	
Read Cycle EMA=7	t_{cyce7}	1.108	
Write Cycle EMA=0 EMAW=0	$t_{cyce0ew0}$	0.778	
Write Cycle EMA=0 EMAW=1	$t_{cyce0ew1}$	0.795	

Cycle and Access Timing for Different Values of Extra Margin Adjustment continued (units = ns)

Pin	Symbol	Typical Process 0.9V, 25°C	
		Min	Max
Write Cycle EMA=0 EMAW=2	$t_{cyce0ew2}$	0.831	
Write Cycle EMA=0 EMAW=3	$t_{cyce0ew3}$	0.894	
Write Cycle EMA=1 EMAW=0	$t_{cyce1ew0}$	0.836	
Write Cycle EMA=1 EMAW=1	$t_{cyce1ew1}$	0.853	
Write Cycle EMA=1 EMAW=2	$t_{cyce1ew2}$	0.889	
Write Cycle EMA=1 EMAW=3	$t_{cyce1ew3}$	0.952	
Write Cycle EMA=2 EMAW=0	$t_{cyce2ew0}$	0.858	
Write Cycle EMA=2 EMAW=1	$t_{cyce2ew1}$	0.875	
Write Cycle EMA=2 EMAW=2	$t_{cyce2ew2}$	0.911	
Write Cycle EMA=2 EMAW=3	$t_{cyce2ew3}$	0.974	
Write Cycle EMA=3 EMAW=0	$t_{cyce3ew0}$	0.880	
Write Cycle EMA=3 EMAW=1	$t_{cyce3ew1}$	0.897	
Write Cycle EMA=3 EMAW=2	$t_{cyce3ew2}$	0.934	
Write Cycle EMA=3 EMAW=3	$t_{cyce3ew3}$	0.996	
Write Cycle EMA=4 EMAW=0	$t_{cyce4ew0}$	0.915	
Write Cycle EMA=4 EMAW=1	$t_{cyce4ew1}$	0.932	
Write Cycle EMA=4 EMAW=2	$t_{cyce4ew2}$	0.968	
Write Cycle EMA=4 EMAW=3	$t_{cyce4ew3}$	1.031	
Write Cycle EMA=5 EMAW=0	$t_{cyce5ew0}$	0.980	
Write Cycle EMA=5 EMAW=1	$t_{cyce5ew1}$	0.997	

Cycle and Access Timing for Different Values of Extra Margin Adjustment continued (units = ns)

Pin	Symbol	Typical Process 0.9V, 25°C	
		Min	Max
Write Cycle EMA=5 EMAW=2	$t_{cyce5ew2}$	1.034	
Write Cycle EMA=5 EMAW=3	$t_{cyce5ew3}$	1.096	
Write Cycle EMA=6 EMAW=0	$t_{cyce6ew0}$	1.043	
Write Cycle EMA=6 EMAW=1	$t_{cyce6ew1}$	1.060	
Write Cycle EMA=6 EMAW=2	$t_{cyce6ew2}$	1.096	
Write Cycle EMA=6 EMAW=3	$t_{cyce6ew3}$	1.159	
Write Cycle EMA=7 EMAW=0	$t_{cyce7ew0}$	1.108	
Write Cycle EMA=7 EMAW=1	$t_{cyce7ew1}$	1.125	
Write Cycle EMA=7 EMAW=2	$t_{cyce7ew2}$	1.162	
Write Cycle EMA=7 EMAW=3	$t_{cyce7ew3}$	1.225	
Read Access EMA=0	t_{ae0}		0.661
Read Access EMA=1	t_{ae1}		0.718
Read Access EMA=2	t_{ae2}		0.741
Read Access EMA=3	t_{ae3}		0.763
Read Access EMA=4	t_{ae4}		0.797
Read Access EMA=5	t_{ae5}		0.863
Read Access EMA=6	t_{ae6}		0.926
Read Access EMA=7	t_{ae7}		0.991
Write-Thru Access	t_a		0.568
EMA setup	t_{emas}	0.781	
EMA hold	t_{emah}	0.778	
EMAS setup	t_{emass}	0.781	
EMAS hold	t_{emash}	0.778	
EMAW setup	t_{emaws}	0.781	
EMAW hold	t_{emawh}	0.778	

**Illegal setting of EMA for this corner.

BIST Mux Timing (units = ns)

Pin	Symbol	Typical Process 0.9V, 25°C	
		Min	Max
CENY load	K_{ceny}		0.841
WENY load	K_{weny}		0.841
AY load	K_{ay}		0.841
DY load	K_{dy}		0.814
TEN rise to CENY delay	$t_{tenceny}$		0.341
TEN fall to CENY delay	$t_{tenceny}$		0.392
CEN to CENY delay	$t_{cenceny}$		0.141
TCEN to CENY delay	$t_{tcenceny}$		0.179
TEN rise to WENY delay	$t_{tenweny}$		0.341
TEN fall to WENY delay	$t_{tenweny}$		0.392
WEN to WENY delay	$t_{wenweny}$		0.142
TWEN to WENY delay	$t_{twenweny}$		0.174
TEN rise to AY delay	t_{tenay}		0.342
TEN fall to AY delay	t_{tenay}		0.398
A to AY delay	t_{aay}		0.145
TA to AY delay	t_{taay}		0.180
TEN rise to DY delay	t_{tendy}		0.400
TEN fall to DY delay	t_{tendy}		0.404
D to DY delay	t_{ddy}		0.161
TD to DY delay	t_{tddy}		0.169
BEN rise to Q delay	t_{benq}		0.330
BEN fall to Q delay	t_{benq}		0.353
TQ to Q delay	t_{tqq}		0.181
TEN setup	t_{tens}	0.437	
TEN hold	t_{tenh}	0.000	
TCEN setup	t_{tcens}	0.145	
TCEN hold	t_{tcenh}	0.141	
TWEN setup	t_{twens}	0.136	
TWEN hold	t_{twenh}	0.142	

BIST Mux Timing (units = ns)

Pin	Symbol	Typical Process 0.9V, 25°C	
		Min	Max
TA setup	t_{tas}	0.221	
TA hold	t_{tah}	0.142	
TD setup	t_{tds}	0.036	
TD hold	t_{tdh}	0.131	

Pin Capacitance (units = fF)

Pin	Typical Process 0.9V, 25°C
A	4.662
D	5.443
CLK	14.212
CEN	4.324
WEN	4.188
EMA	6.611
EMAW	6.400
EMAS	6.022
TEN	7.695
TA	4.139
TD	4.678
TCEN	3.667
TWEN	3.991
BEN	17.214
TQ	5.512
RET1N	34.672
STOV	6.631

Power (current units = mA)

Pin	Typical Process 0.9V, 25°C
core AC Curr (EMA=0)[1,4]	0.051178
peri AC Curr (EMA=0)[1,4]	3.455545
core AC Curr (EMA=1)[1,4]	0.050942
peri AC Curr (EMA=1)[1,4]	3.442584
core AC Curr (EMA=2)[1,4]	0.050942
peri AC Curr (EMA=2)[1,4]	3.533976
core AC Curr (EMA=3)[1,4]	0.051734
peri AC Curr (EMA=3)[1,4]	3.518885
core AC Curr (EMA=4)[1,4]	0.051551

Power continued (current units = mA)

Pin	Typical Process 0.9V, 25°C
peri AC Curr (EMA=4)[1,4]	3.61168
core AC Curr (EMA=5)[1,4]	0.052073
peri AC Curr (EMA=5)[1,4]	3.715061
core AC Curr (EMA=6)[1,4]	0.051904
peri AC Curr (EMA=6)[1,4]	3.865033
core AC Curr (EMA=7)[1,4]	0.052541
peri AC Curr (EMA=7)[1,4]	3.936113
core Read AC Curr (EMA=0)[1,4]	0.058721
peri Read AC Curr (EMA=0)[1,4]	3.701611
core Read AC Curr (EMA=1)[1,4]	0.0584
peri Read AC Curr (EMA=1)[1,4]	3.825374
core Read AC Curr (EMA=2)[1,4]	0.05827
peri Read AC Curr (EMA=2)[1,4]	3.886265
core Read AC Curr (EMA=3)[1,4]	0.059228
peri Read AC Curr (EMA=3)[1,4]	3.914283
core Read AC Curr (EMA=4)[1,4]	0.058861
peri Read AC Curr (EMA=4)[1,4]	4.005032
core Read AC Curr (EMA=5)[1,4]	0.059604
peri Read AC Curr (EMA=5)[1,4]	4.133725
core Read AC Curr (EMA=6)[1,4]	0.059521
peri Read AC Curr (EMA=6)[1,4]	4.310262
core Read AC Curr (EMA=7)[1,4]	0.060396
peri Read AC Curr (EMA=7)[1,4]	4.427514
core Write AC Curr (EMA=0)[1,4]	0.043634
peri Write AC Curr (EMA=0)[1,4]	3.209479
core Write AC Curr (EMA=1)[1,4]	0.043484
peri Write AC Curr (EMA=1)[1,4]	3.059795
core Write AC Curr (EMA=2)[1,4]	0.043614
peri Write AC Curr (EMA=2)[1,4]	3.181686
core Write AC Curr (EMA=3)[1,4]	0.04424
peri Write AC Curr (EMA=3)[1,4]	3.123487
core Write AC Curr (EMA=4)[1,4]	0.044241
peri Write AC Curr (EMA=4)[1,4]	3.218329
core Write AC Curr (EMA=5)[1,4]	0.044542
peri Write AC Curr (EMA=5)[1,4]	3.296397
core Write AC Curr (EMA=6)[1,4]	0.044287
peri Write AC Curr (EMA=6)[1,4]	3.419804
core Write AC Curr (EMA=7)[1,4]	0.044685
peri Write AC Curr (EMA=7)[1,4]	3.444712
core Peak Curr	4.237288
peri Peak Curr	188.715393
core Deselected Curr[2,4]	0.000e+00

Power continued (current units = mA)

Pin	Typical Process 0.9V, 25°C
peri Deselected Curr[2,4]	0.446588
core Standby Curr	0.096559
peri Standby Curr	0.210716
core Retention Standby Curr	0.096711
peri Retention Standby Curr	0.017714

** Illegal setting of EMA for this corner.

1 The AC current value assumes 50% read and write operations, where all addresses and 50% of input and output pins switch at the user defined frequency of 100MHz. It is assumed that EMA and BIST pins do not switch.

2 The deselected current assumes the memory is deselected, all addresses switch, and 50% of input pins switch at the user defined frequency of 100MHz. The logic switching component of deselected power becomes negligbly small if the input pins are held stable by externally controlling these signals with chip select. It is assumed that EMA and BIST pins do not switch.

3 The standby current value is independent of frequency and assumes all inputs and outputs are stable.

4 The leakage current component is not included in this value.

Clock Noise Limit

Symbol	Typical Process 0.9V, 25°C	
	Pulse Width	Voltage
CLK	10.000ns	0.392V

The clock noise limit is the maximum voltage allowed (for the indicated pulse width) that does not cause an unintentional memory cycle or other memory failure.

Supply Noise Limit (units = V)

Pin	Typical Process 0.9V, 25°C
Power	0.090
Ground	0.090

The power and ground noise limit is the maximum supply voltage transition that is allowed without causing a memory failure.