

# Team05 Lab3 Report

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## 一、層級架構

- src (left) & Altpll generate by Qsys (right)

```
AudDSP.sv
audplayer.sv
AudRecorder.sv
I2cInitializer.sv
test_audPlay.sv
test_AudRecorder.sv
test_dsp.sv
test_I2C.sv
Top.sv

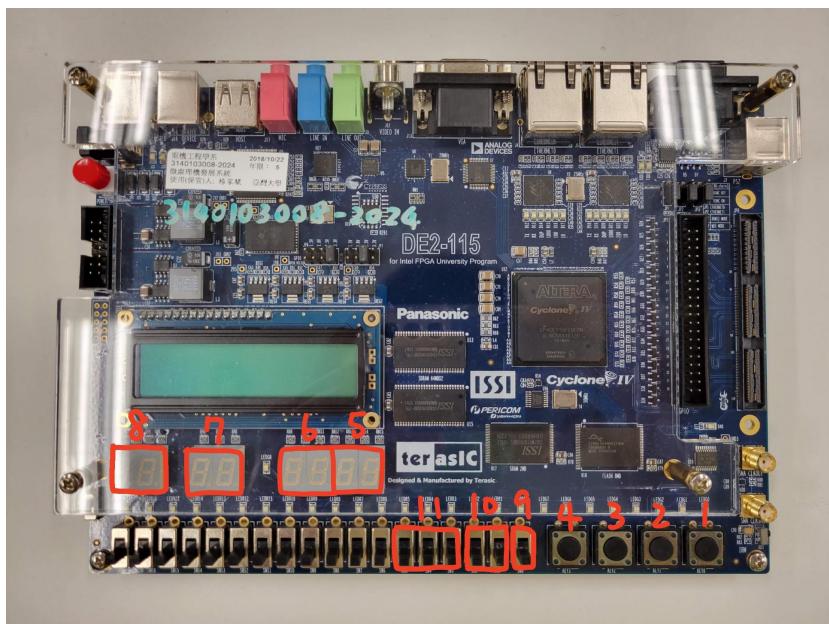
DE2_115
    DE2_115.qsf
    DE2_115.sdc
    DE2_115.sv
    DE2_115.sv.bak
    Debounce.sv
    SevenHexDecoder.sv

Altpll.bsf
Altpll.cmp
Altpll.html
Altpll.xml
Altpll_bb.v
Altpll_generation.rpt
Altpll_inst.v
Altpll_inst.vhd

synthesis
    Altpll.debuginfo
    Altpll.qip
    Altpll.v

submodules
    altera_reset_controller.sdc
    altera_reset_controller.v
    altera_reset_synchronizer.v
    Altpll_altpll_0.v
```

## 二、操作介紹

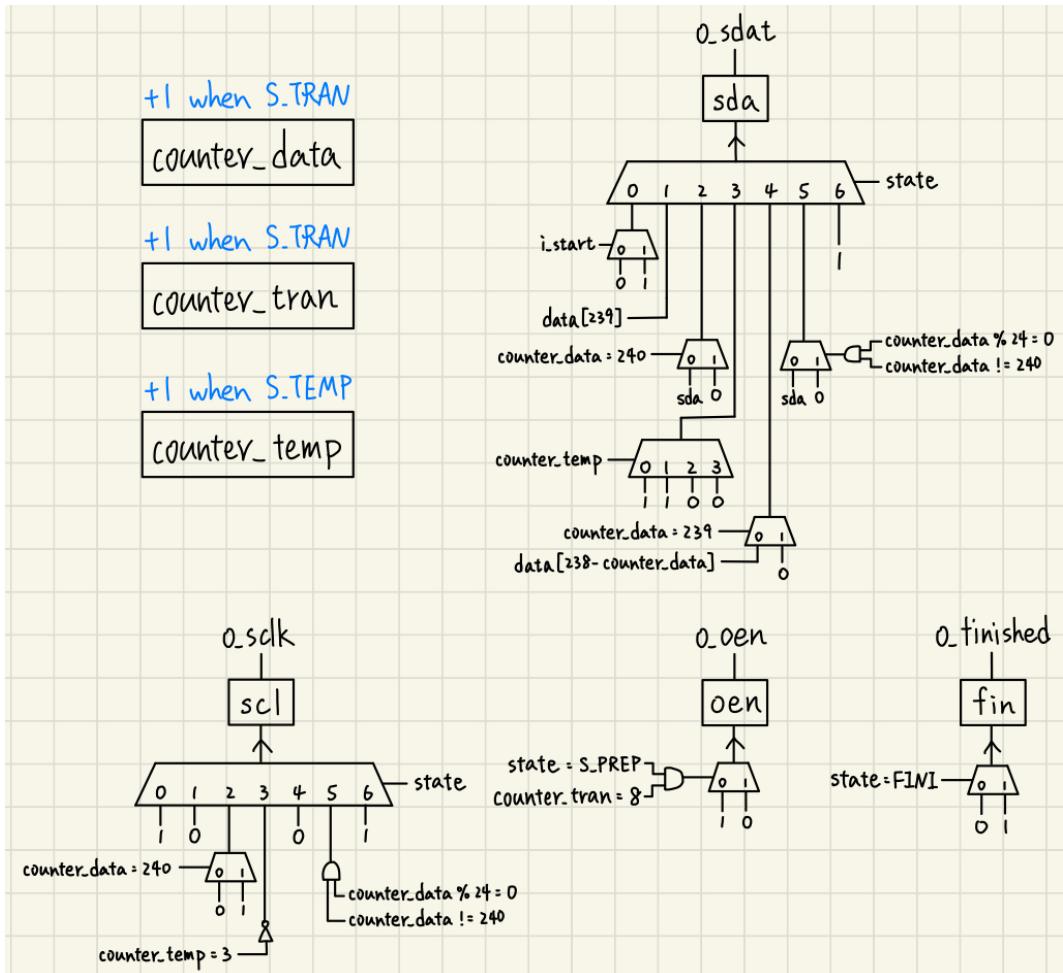
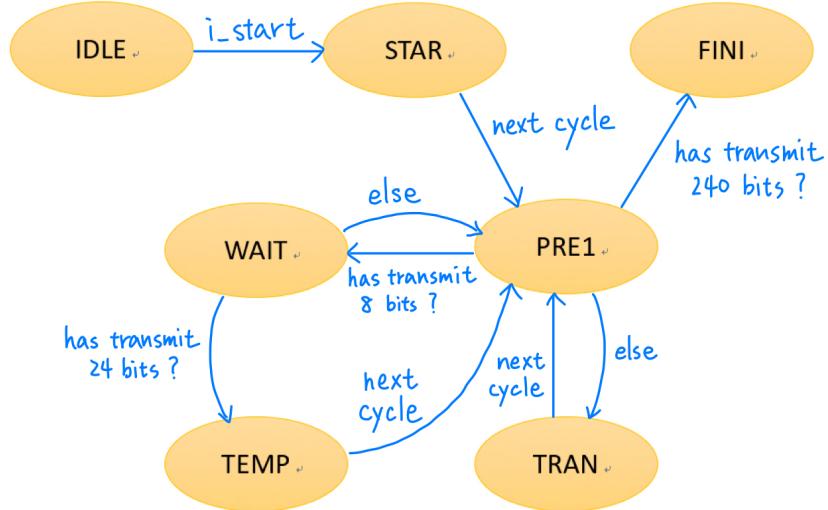


- 1: start button ; 2: pause button ; 3: stop button ; 4:reset button  
5: play time ; 6: record time ; 7: speed ; 8: state  
9: 0→record, 1→play  
10: 00→normal speed, 10→fast, 01→0'th slow, 11→1'st slow  
11: transfer to decimal (0~7)→speed (1~8)  
LED above switches: show amplitude of voice when playing

### 三、Finite State Machine & Block diagram

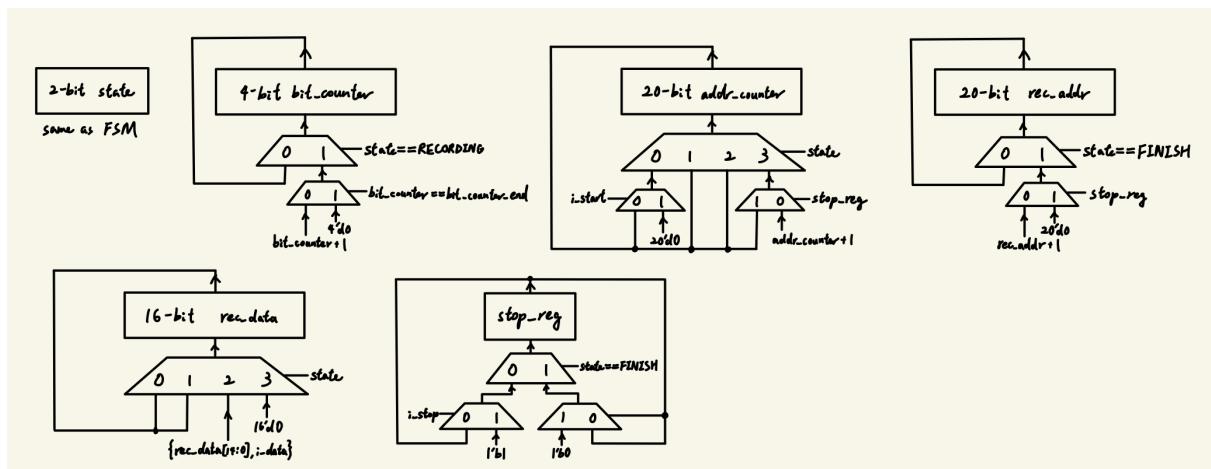
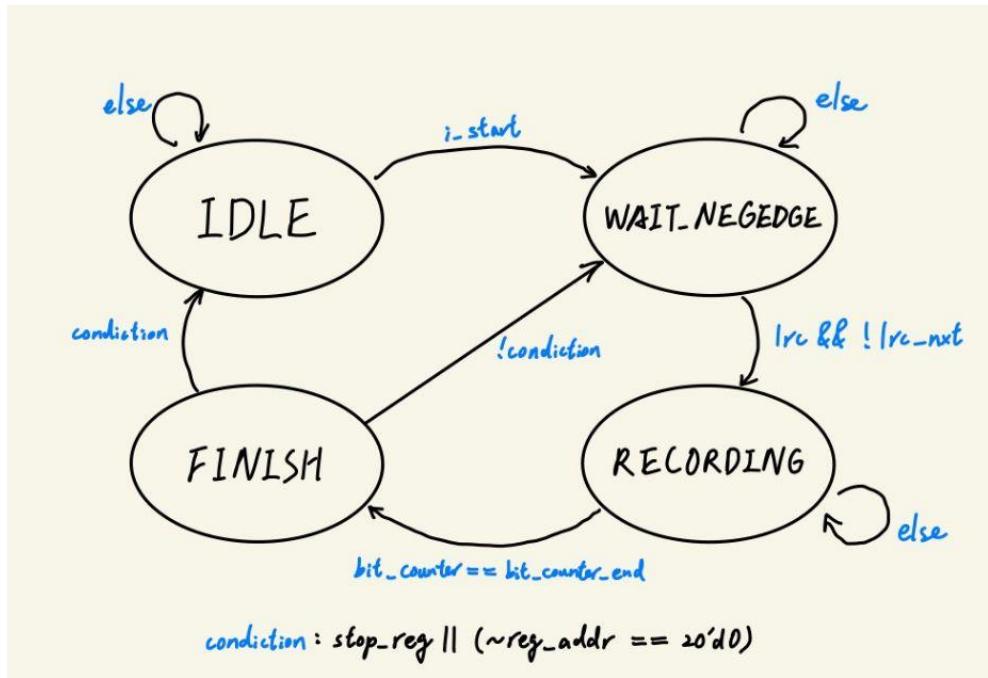
- I2C Initializer

- PRE1 : fetch next bit of data
- WAIT : pull o\_oen low to receive ack after 8'b transmitted
- TEMP : end & restart transmit after 24'b transmitted
- TRAN : pull o\_sclk high to transmit data



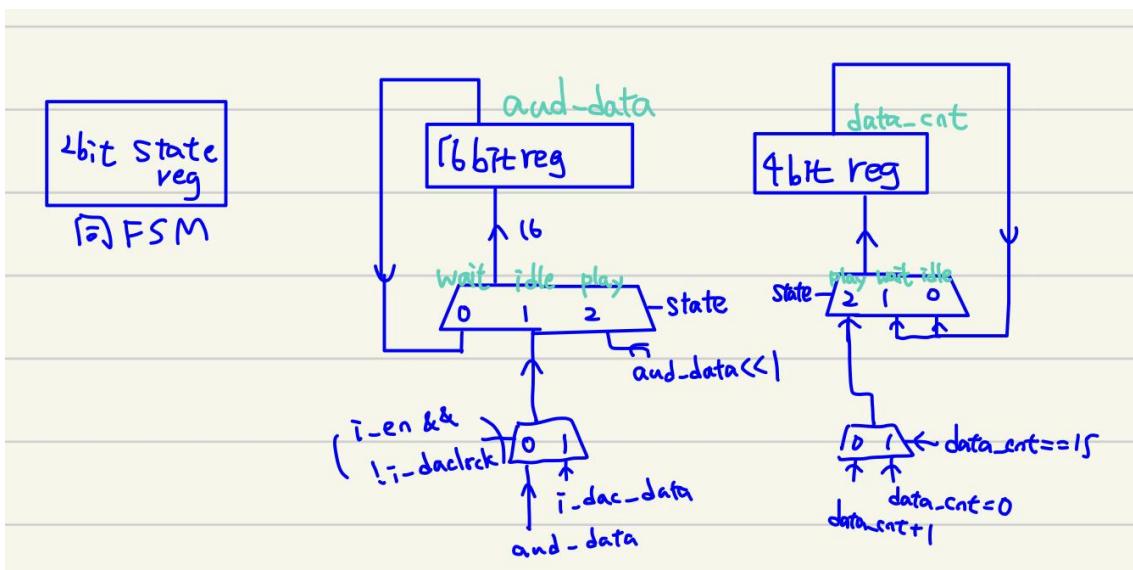
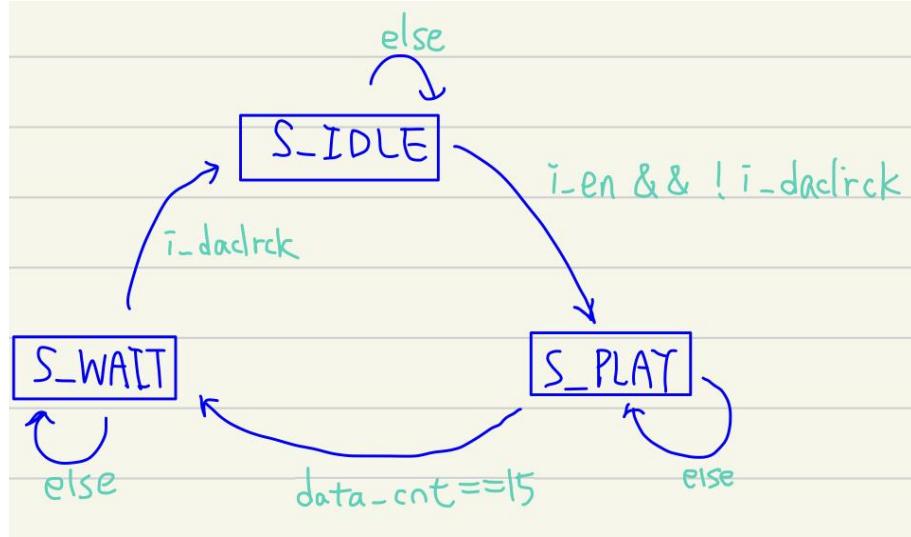
- AudRecorder

- RECORDING: start record 16 cycles when negedge i\_lrc
- WAIT\_NEGEDGE: hold data and wait next negedge i\_lrc
- FINISH: determine record next cycle or back to IDLE



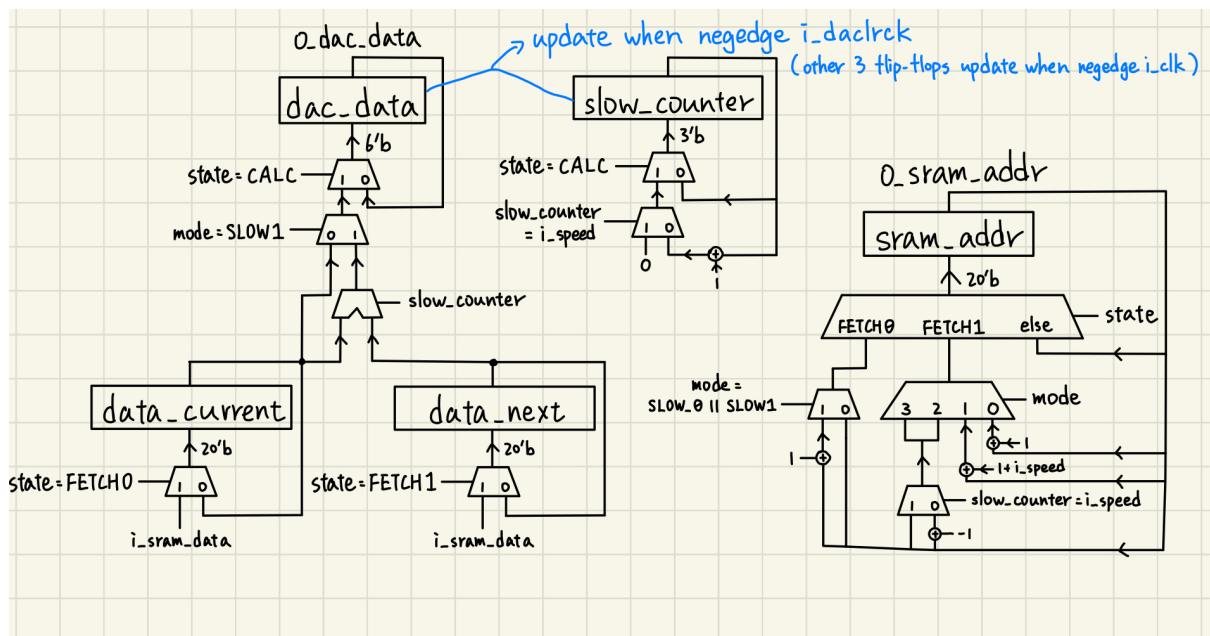
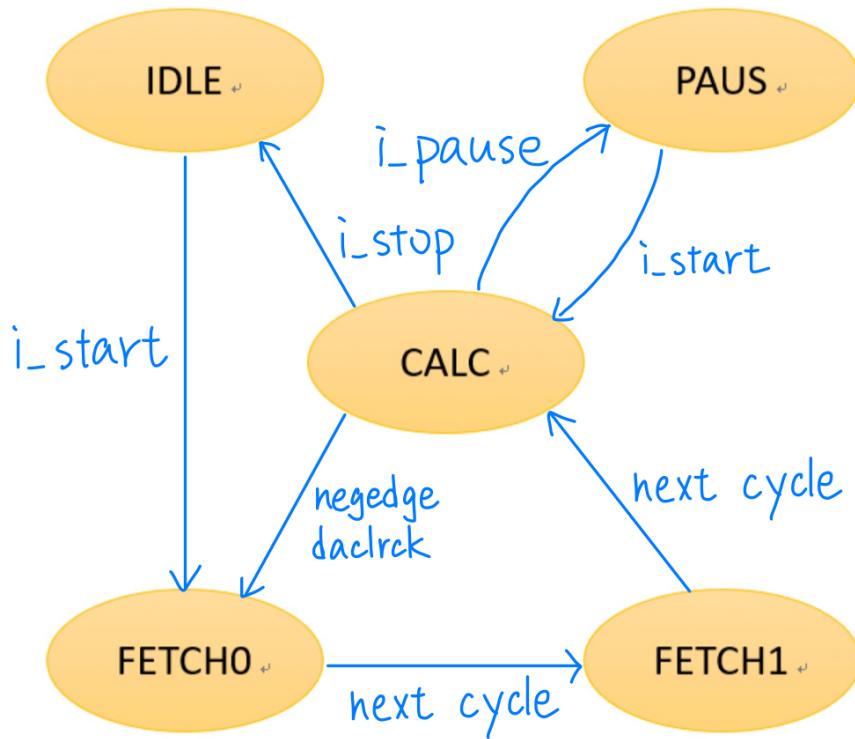
- AudPlayer

- S\_PLAY : transmit 16'b data when negedge i\_daclrck
- S\_WAIT : wait next negedge i\_daclrck



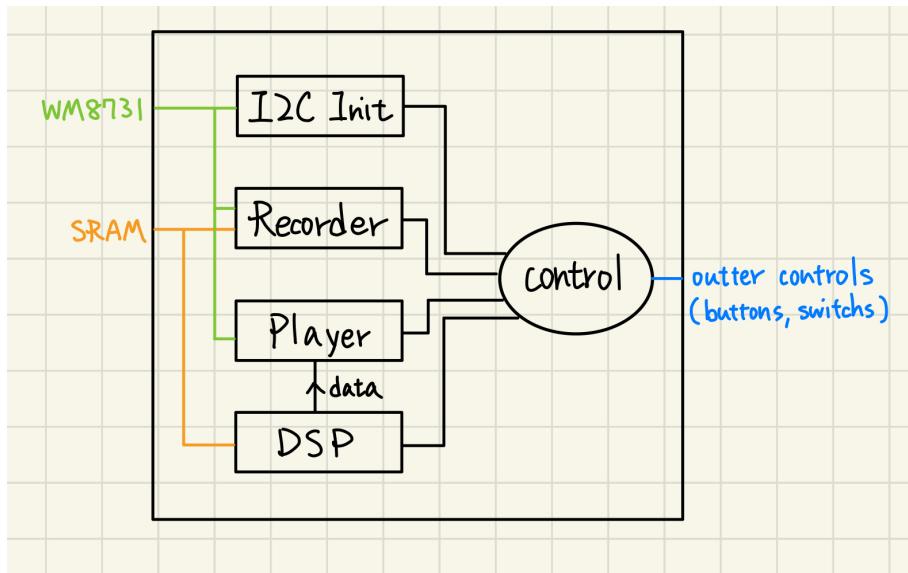
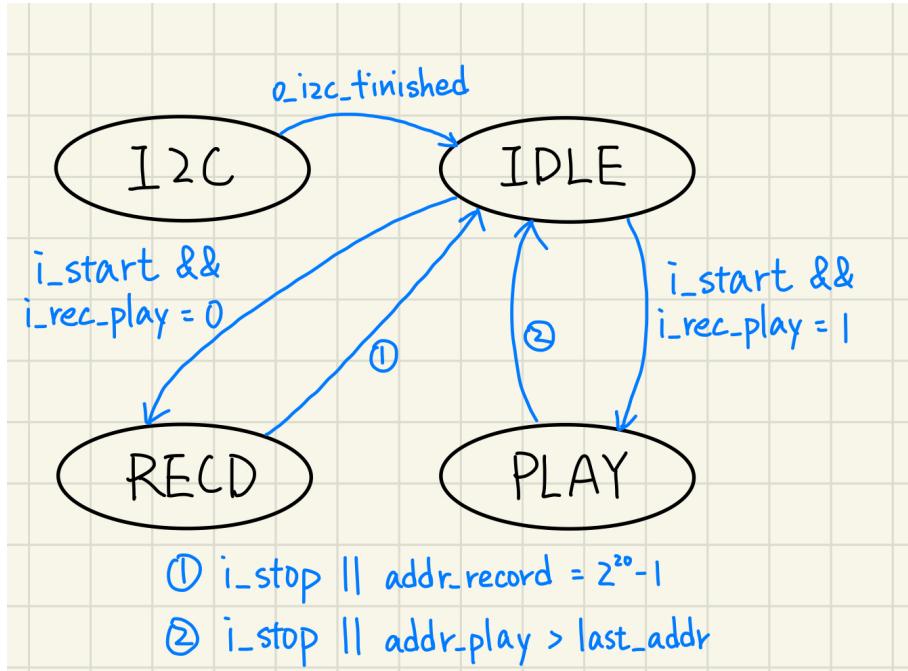
- AudDSP

- S\_FETCH0 : fetch current data
- S\_FETCH1 : fetch data\_next (for Interpolation) & update sram address
- S\_CALC : calculate o\_dac\_data according to speed
- S\_PAUS : hold data until i\_start



- Top

- I2C Initial after reset
- Using i\_rec\_play determine go to record or play



## 四、Fitter summary & Timing analyzer

Fitter Summary	
Fitter Status	Successful - Thu Apr 14 19:51:31 2022
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	1,000 / 114,480 ( < 1 % )
Total combinational functions	980 / 114,480 ( < 1 % )
Dedicated logic registers	214 / 114,480 ( < 1 % )
Total registers	214
Total pins	518 / 529 ( 98 % )
Total virtual pins	0
Total memory bits	0 / 3,981,312 ( 0 % )
Embedded Multiplier 9-bit elements	6 / 532 ( 1 % )
Total PLLs	1 / 4 ( 25 % )

### TimeQuest Timing Analyzer

- Summary
- Parallel Compilation
- SDC File List
- Clocks
  - > Slow 1200mV 85C Model
  - > Slow 1200mV OC Model
  - > Fast 1200mV OC Model
  - > Multicorner Timing Analysis S
  - > Multicorner Datasheet Report
  - > Advanced I/O Timing
  - > Clock Transfers
  - Report TCCS
  - Report RSKM
  - Unconstrained Paths
  - Messages

### Unconstrained Paths

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	2	2
3	Unconstrained Input Ports	29	29
4	Unconstrained Input Port Paths	601	601
5	Unconstrained Output Ports	98	98
6	Unconstrained Output Port Paths	494	494

### Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-7.860	-0.001	N/A	N/A	9.400
1	AUD_BCLK	-4.391	-0.001	N/A	N/A	40.655
2	CLOCK2_50	N/A	N/A	N/A	N/A	16.000
3	CLOCK3_50	N/A	N/A	N/A	N/A	16.000
4	CLOCK_50	N/A	N/A	N/A	N/A	9.400
5	pll0 altpll_0 sd1 pll7 clk[0]	-7.860	0.172	N/A	N/A	41.357
6	pll0 altpll_0 sd1 pll7 clk[1]	36.735	0.179	N/A	N/A	4999.755
2	Design-wide TNS	-543.832	-0.001	0.0	0.0	0.0
1	AUD_BCLK	-371.190	-0.001	N/A	N/A	0.000
2	CLOCK2_50	N/A	N/A	N/A	N/A	0.000
3	CLOCK3_50	N/A	N/A	N/A	N/A	0.000
4	CLOCK_50	N/A	N/A	N/A	N/A	0.000
5	pll0 altpll_0 sd1 pll7 clk[0]	-172.642	0.000	N/A	N/A	0.000
6	pll0 altpll_0 sd1 pll7 clk[1]	0.000	0.000	N/A	N/A	0.000

### Slow 1200mV 85C Model Setup Summary

	Clock	Slack	End Point TNS
1	pll0 altpll_0 sd1 pll7 clk[0]	-7.860	-172.642
2	AUD_BCLK	-4.391	-371.190
3	pll0 altpll_0 sd1 pll7 clk[1]	36.735	0.000

### Slow 1200mV OC Model Setup Summary

	Clock	Slack	End Point TNS
1	pll0 altpll_0 sd1 pll7 clk[0]	-7.226	-158.011
2	AUD_BCLK	-4.138	-349.949
3	pll0 altpll_0 sd1 pll7 clk[1]	37.147	0.000

### Fast 1200mV OC Model Setup Summary

	Clock	Slack	End Point TNS
1	pll0 altpll_0 sd1 pll7 clk[0]	-4.005	-88.469
2	AUD_BCLK	-1.779	-147.523
3	pll0 altpll_0 sd1 pll7 clk[1]	39.157	0.000

## 五、遇到的問題與解法

1. 一開始燒上去測試時發現i\_clk\_100k沒有東西，但是測試Atpll產生的12M跟100k兩個clk都是正確的，後來把Top中的i\_clk\_100k這個input port改名後就好了，猜測是原本的名字有那裡打錯或全形半形混用導致的。
2. 測試時發現WM8731沒有回傳i\_AUD\_BCLK，因此整個系統都無法運作。後來想說問題可能出在I2C Initializer上，就試試看把傳輸的指令從7條改成另一份投影片中的10條結果就好了。
3. 有時在更改一些control訊號後就會跑出一堆雜音，但完全不知其原由（例如把i\_start按鈕跟另一個訊號做AND來區隔要開始錄音還是開始播放就出現雜音），後來就只好先改回去，然後看能不能更動其他東西來做到一樣的功能。
4. 在demo前兩天（週三）的晚上某一次燒錄後就整組壞去，WM8731沒有回傳i\_AUD\_BCLK，但那次改動的只有AudRecorder中的一個control訊號，理論上不會讓整組不運作，用github reset到下午確定能使用但有小bug版本後燒錄也失敗。後來吃飯回來code都沒改再重燒幾次就好了。接著週四下午直接用前一天晚上確定成功的版本再燒一次又失敗，但這次學乖了，都不改code爆燒個20次後就成功了，之後不敢再重燒，直接讓板子不關電留到demo。
5. 嘗試使用板子上的LEDR來顯示目前聲音的振幅，但只有播音時會照我們期待的顯示，後來發現是因為我們的AudRecorder傳出來的data在寫入sram後的下一個cycle就會馬上歸零，所以理論上只要把data用另一個register記住直到下一個完整的data產生再更新就可以，但因為再demo前一天才想到這個解法，很害怕改了之後板子又一直燒失敗所以就沒有嘗試QQ。