Performance Analysis of a 4-bit Ripple Carry Adder (RCA) formed using Static CMOS, Transmission Gate, NMOS Pass Transistor Logic at gpdk 180nm Technology node.

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CHAPTER 1: INTRODUCTION

1.1 WHAT ARE ADDERS IN DIGITAL ELECTRONICS?

An adder is a circuit used in digital electronics that adds binary values. Similar to decimal addition but using base-2 integers, binary addition requires bit by bit joining of two binary numbers. Adders are essential components of digital circuits and are used in computers and other digital systems for arithmetic operations. A single bit full adder consists of two single bit half adders which is formed using XOR and AND gates to calculate Sum and Carry from the inputs provided.

1.2 ADDER TOPOLOGIES

There are various adder topologies or architectures, each with its own set of benefits and drawbacks in terms of speed, area, and power consumption. The most common adder topologies include the following architectures,

- Ripple Carry Adder (RCA)
- Carry Lookahead Adder (CLA)
- Carry Select Adder (CSLA)
- Carry Skip Adder (CSKA)

1.3 SIGNIFICANCE OF ADDERS

These adders are crucial components of a processor's arithmetic logic unit (ALU), where they perform operations like as adding numbers, incrementing counters, and conducting other arithmetic operations like comparison, subtraction, multiplication between operands. Adders are also important in applications such as digital signal processing and other digital communication systems.

CHAPTER 2: LITERATURE REVIEW

2.1 WHAT IS STATIC CMOS LOGIC?

Static CMOS (Complementary Metal-Oxide-Semiconductor) logic is a form of digital circuit design that implements logic operations using complementary pairs of p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs).

Here the NMOS and PMOS are used as a switch to implement logic expressed in the form Boolean expressions.

A certain rule is followed while evaluating the switch level structure of a particular logic available in its Boolean expression form where in all inputs to PMOS involved in AND operation are kept in parallel and for OR operation all inputs to PMOS involved are kept in series.

Similarly, all inputs to NMOS involved in AND operation are kept in series and for OR operation all inputs to NMOS are kept in parallel connection.

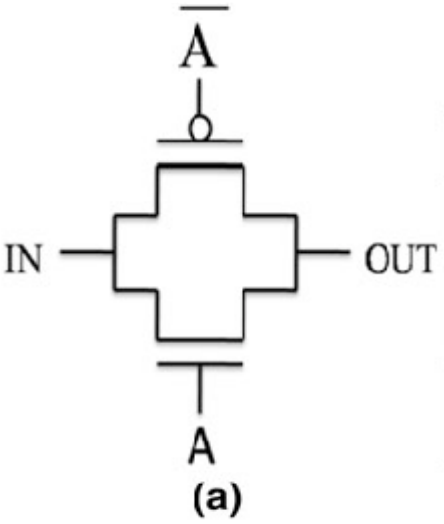
2.1.1 Key Characteristics of Static CMOS Logic

- **Rail-to-Rail Output Swing:** A rail-to-rail output swing is commonly provided by static CMOS circuitry, which allows the output voltage to fluctuate between ground and power supply voltages.
- **Complementary Pair:** N-type (NMOS) and p-type (PMOS) transistors are used in complementary pairs in static CMOS logic. There are two pull-up and pull-down networks (PMOS and NMOS) in every logic gate.
- **Minimal Power Consumption:** Static CMOS logic uses relatively minimal power while the inputs are not changing, as there is no direct current channel connecting the power supply to the ground. It is therefore appropriate for uses where power efficiency is crucial.

2.2 WHAT IS TRANSMISSION GATE LOGIC?

Transmission gate logic is a method for designing digital circuits that implements logic operations using transmission gates. They are electronic switches that allow signals to flow through by being selectively opened or closed.

The basic building block of transmission gate logic is the transmission gate itself, which consists of an n-type (NMOS) transistor and a p-type (PMOS) transistor connected in parallel. The control signal determines whether the transmission gate is in an open or closed state.



A	IN	OUT
H	H	H
H	L	L
L	X (don't care)	Z(high impedance)

(b)

Figure 1: Transmission Gate Logic

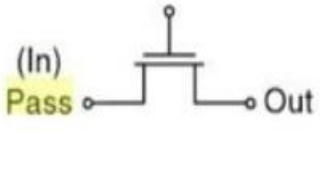
Logic (A) is given at the NMOS terminal and its complementary Logic (Abar) is given at the PMOS terminal. The gate conducts when signal Logic (A) goes high thereby making Logic (Abar) drive low which satisfies both NMOS and PMOS gate which makes the signal at Input (IN) to pass at the Output (OUT).

The major advantage of using Transmission Gates is that it significantly reduces the number of transistors used while designing a circuit compared to the traditional CMOS logic hence, in some cases may result in low power consumption.

2.3 WHAT IS NMOS PASS TRANSISTOR LOGIC?

NMOS pass transistor logic is a type of digital circuit design that uses NMOS transistors as pass transistors to implement logic functions.

Pass transistor logic is a subset of transmission gate logic, where transistors are used as electronic switches to allow or block the flow of signals. In NMOS pass transistor logic, only NMOS transistors are employed, and their conductivity is controlled to pass or block the signal.



Gate	Pass	Out
0	0	hi-Z
0	1	hi-Z
1	0	0
1	1	1

Figure 2: NMOS PTL Logic

When the control signal is high, the NMOS transistor is turned on, providing a low-resistance path between the source and drain terminals. The input signal (Pass) is effectively transmitted to the output terminal. When the control signal is low, the NMOS transistor is turned off, isolating the input signal (Pass) from the output.

Although, NMOS Pass Transistor Logic significantly reduces the Transistor count, even lesser than Transmission Gate Logic thereby reducing the area requirement but it may increase the power consumption as it provides a direct path between the supply voltage and the ground which might result in leakage currents. Also, unlike CMOS logic it doesn't provide full swing as NMOS passes weak Logic 1 (HIGH).

2.4 PREVIOUS WORK

Since, Adder forms the fundamental block of almost all circuits in a digital design, an extensive amount of research is done in order to reduce the propagation delays and power overhead starting from just a single bit full adder up to large adder chains.

In order to get familiar with the concepts and how different analysis needs to be carried out and to form a base for this project, several research papers have been studied.

One well-documented paper, "Low power 18T pass transistor logic ripple carry adder," compares a novel 18 transistor adder structure using pass transistor logic to the 28T conventional CMOS, 20T transmission gate (TGA), 16T transmission function (TFA), 14T hybrid, 24T hybrid pass logic with static CMOS, and 28T differential pass logic (DPL) full adders that were simulated using the same process technology. This comparison provides important insights into the proper methodology for the analysis.[1]

The study of various adder topologies and their comparison based on performance metrics, such as Area, Delay, and Power, was also the subject of a second work titled, “Area, Delay, and Power Comparison of Adder Topologies”, was referred.[2]

CHAPTER 3: METHODOLOGY

3.1 LOGIC GATES

Logic gates are fundamental building blocks in digital electronics, and they perform logical operations on binary inputs, producing a binary output based on predefined logic functions. Logic gates are used to build more complex digital design once their Boolean expression is known to the designer. The basic logic gates include AND, OR, NAND, NOR, XOR, XNOR, NOT.

Logic gates can be implemented using NMOS and PMOS transistors which is referred as Switch Level Design. Thus, they can be formed using Static CMOS, Transmission Gate and NMOS Pass Transistor Logic.

Following are the Switch Level Design of XOR, AND, OR gates used in the formation of an adder in all three logic schemes mentioned above.

$$(A \; XOR \; B = A.B' + A'.B)$$

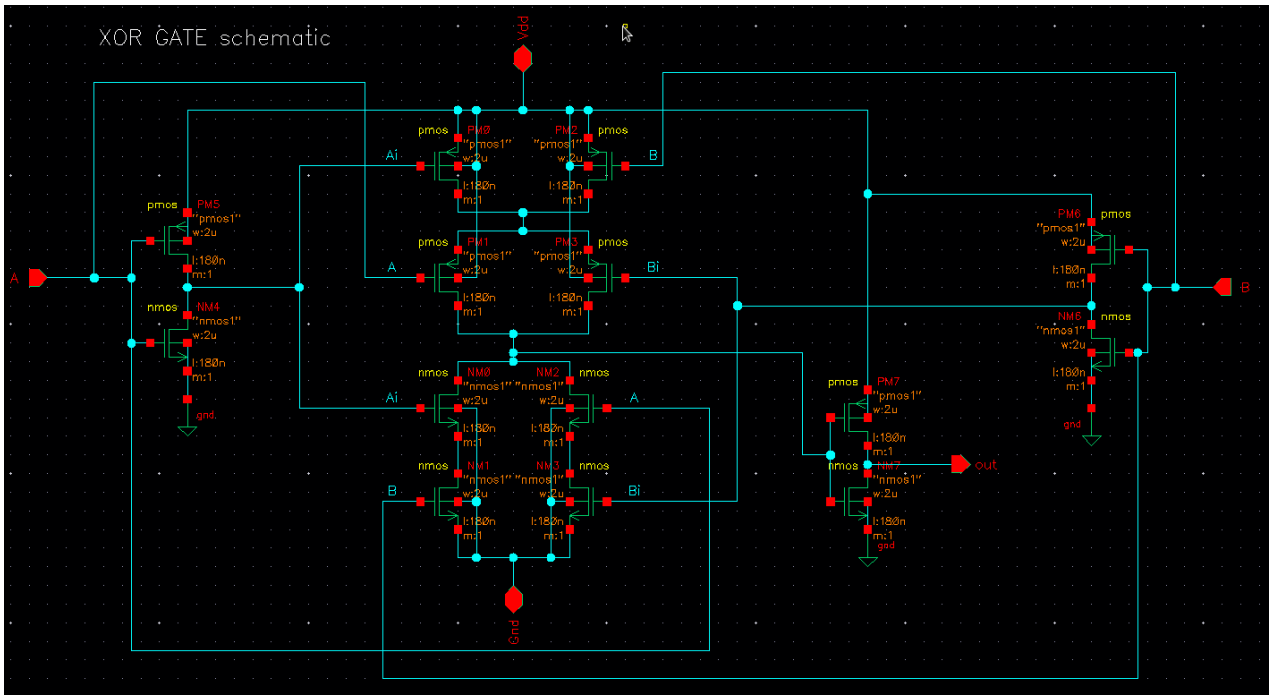


Figure 3: XOR Gate using CMOS logic

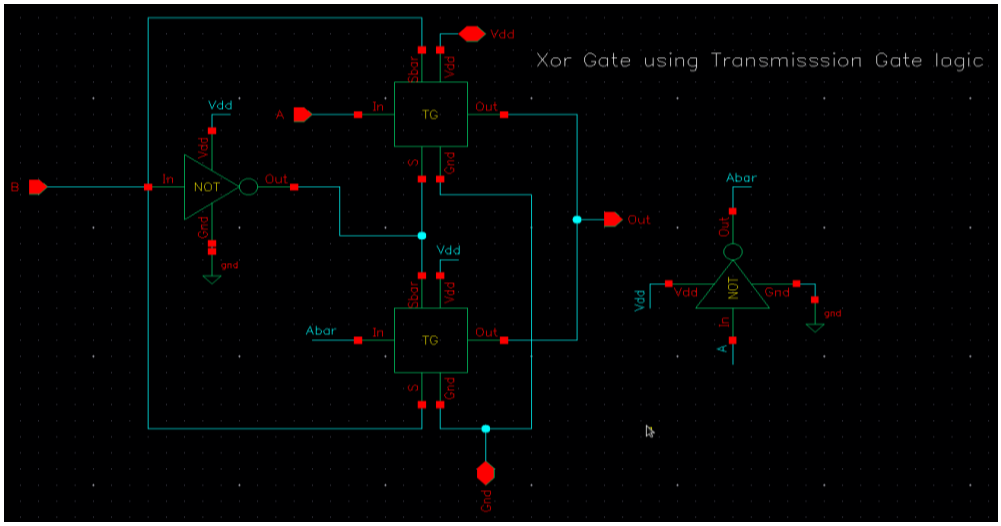


Figure 4: XOR Gate using TG Logic

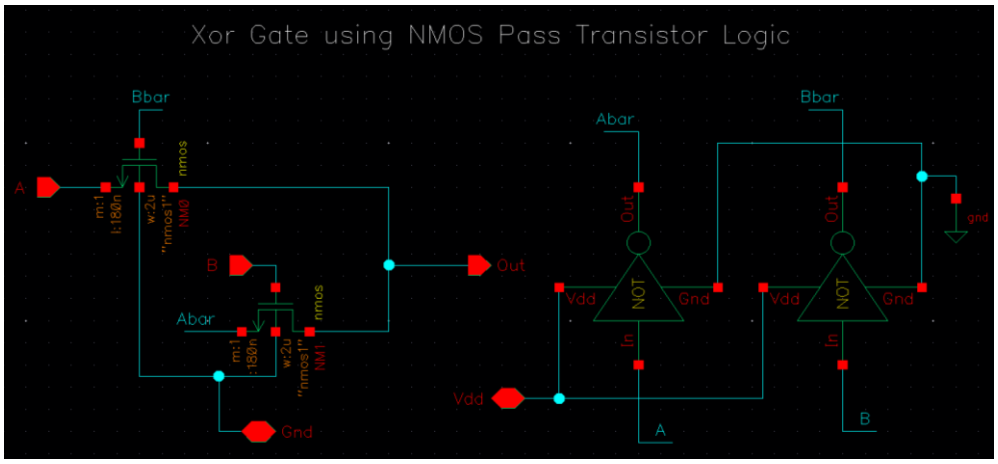


Figure 5: XOR Gate using NMOS PTL

(A AND B = A.B)

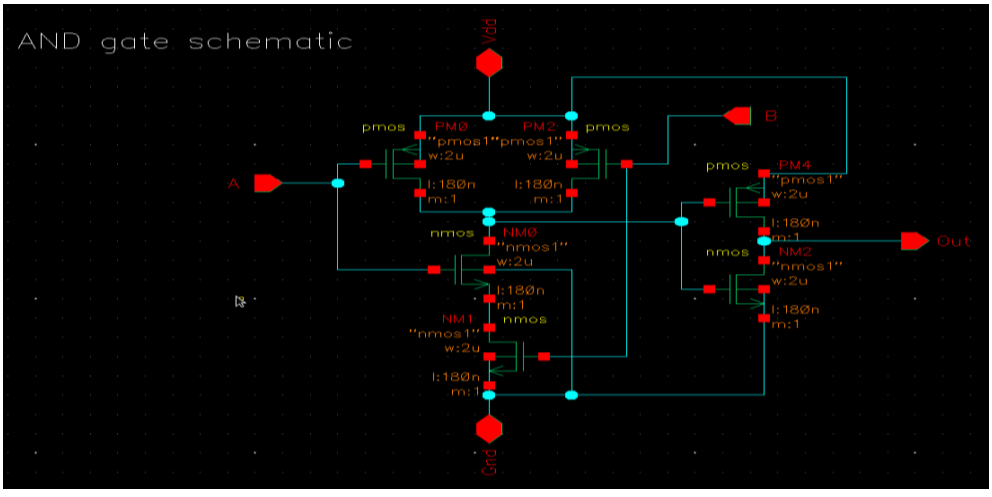


Figure 6: AND Gate using CMOS Logic

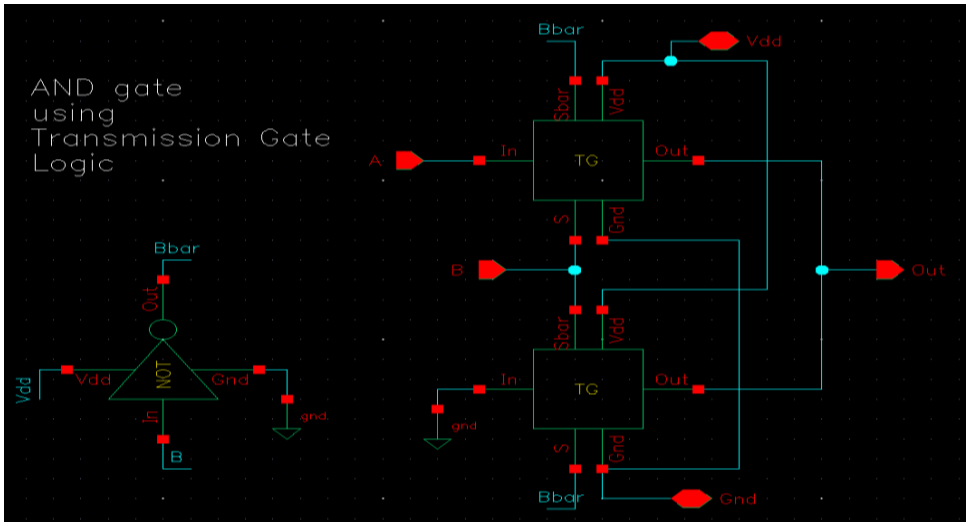


Figure 7: AND Gate using TG Logic

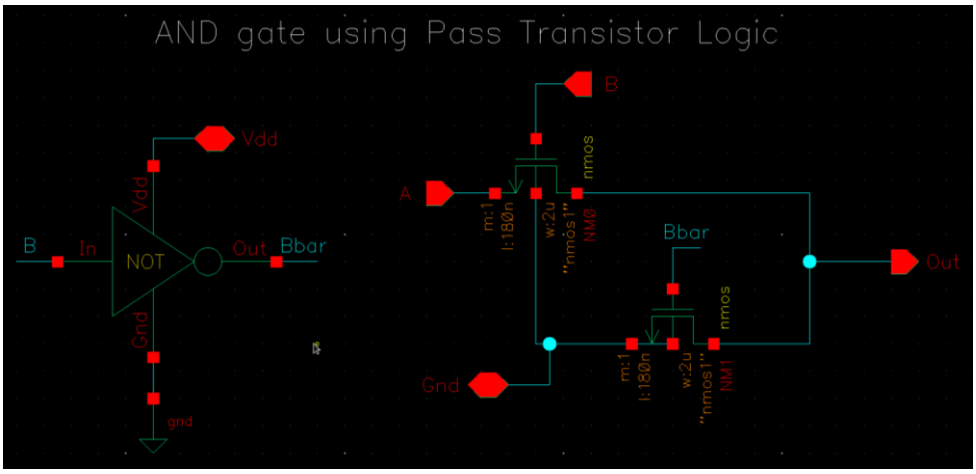


Figure 8: AND Gate using NMOS PTL

(A OR B = A+B)

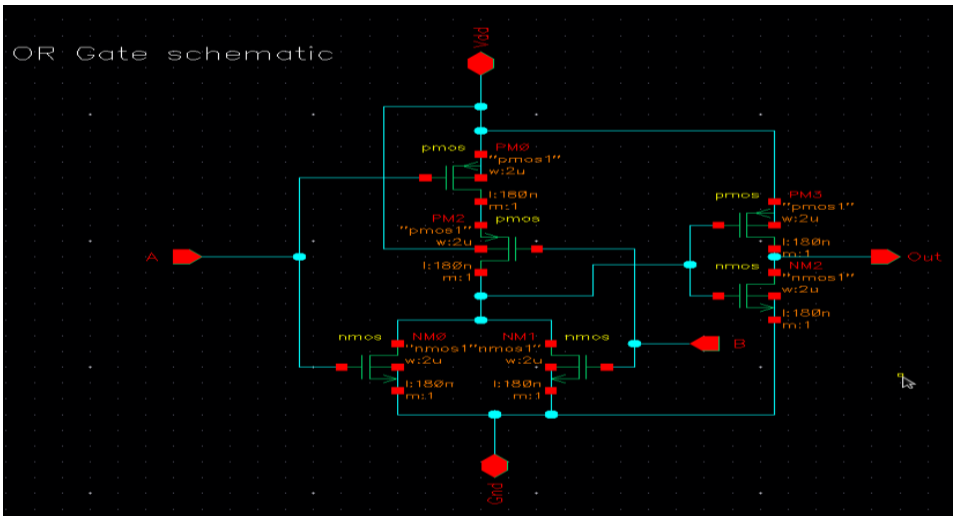


Figure 9: OR Gate using CMOS Logic

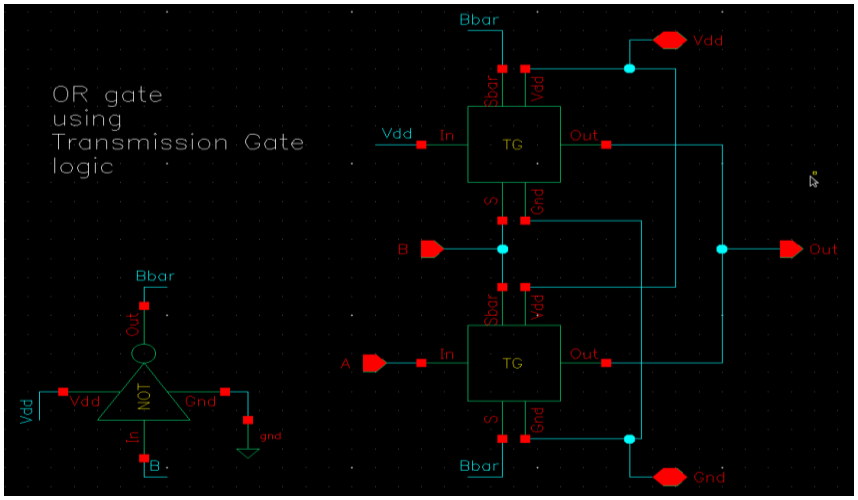


Figure 10: OR Gate using TG Logic

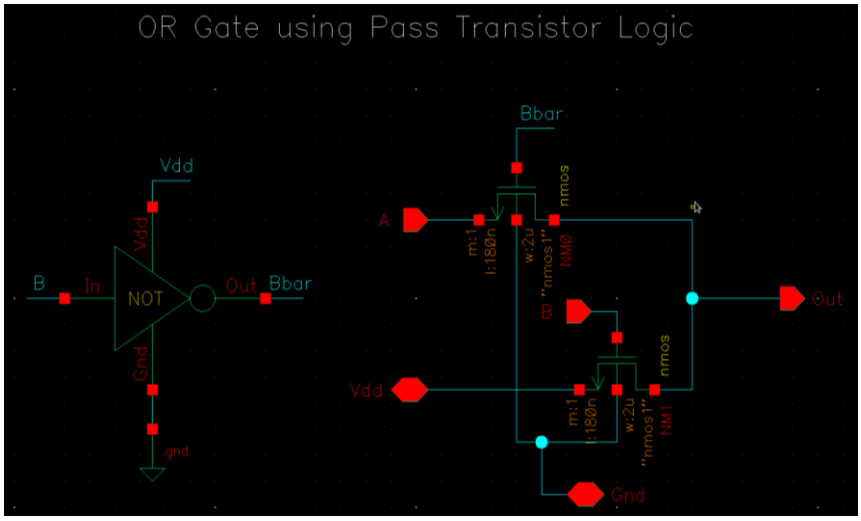


Figure 11: OR Gate using NMOS PTL

3.2 HALF ADDER

A half adder is a simple digital circuit used to add two binary numbers. It contains two outputs, namely Carry (C) and Sum (S), and two inputs, as A and B, denoting the two bits to be added. XOR and AND gates are two common logic gates that can be used to create the half adder.

Sum (S): $S = A \oplus B$ (XOR gate)

Carry (C): $C = A \cdot B$ (AND gate)

Figure 12: Boolean Expression for Sum and Carry of a Half Adder

Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 13: Truth Table of a Half Adder

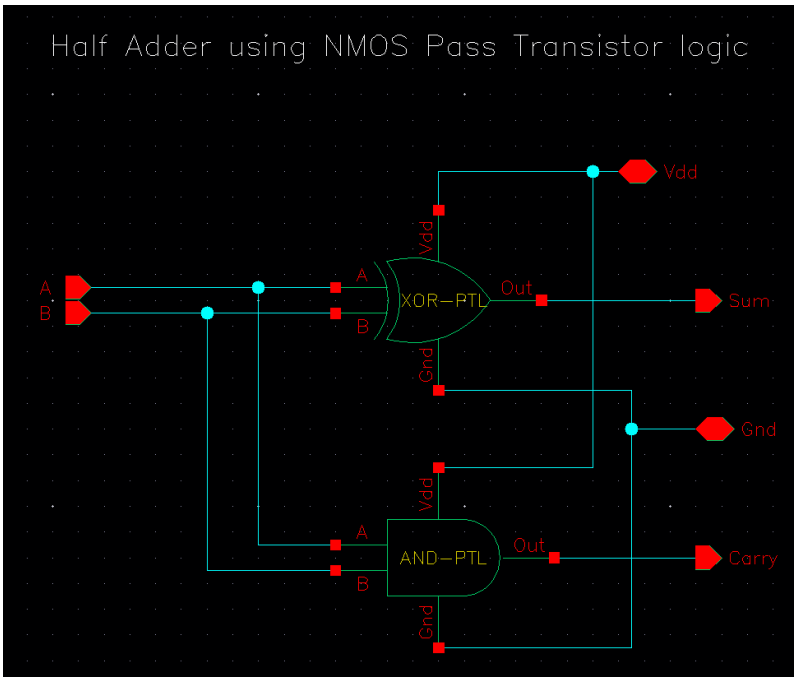


Figure 14: Half Adder Circuit Diagram

The above figure is the circuit diagram of a Half Adder formed using one XOR and one AND gate using PTL. The circuit remains same for Transmission Gate and CMOS Gate logic as well.

3.3 FULL ADDER

A 1-bit Full Adder is formed using two Half Adders cascaded in series with each other and an OR gate. It takes in three 1-bit inputs namely A, B, Cin and performs the binary addition to give Sum and Carry output (Cout) from these three bits.

$$S = A \oplus B \oplus C_{\text{in}}$$

Figure 15: Sum of a Full Adder

$$C_{\text{out}} = (A \cdot B) + (C_{\text{in}} \cdot (A \oplus B))$$

Figure 16: Carry of a Full Adder

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 17: Truth Table of a Full Adder

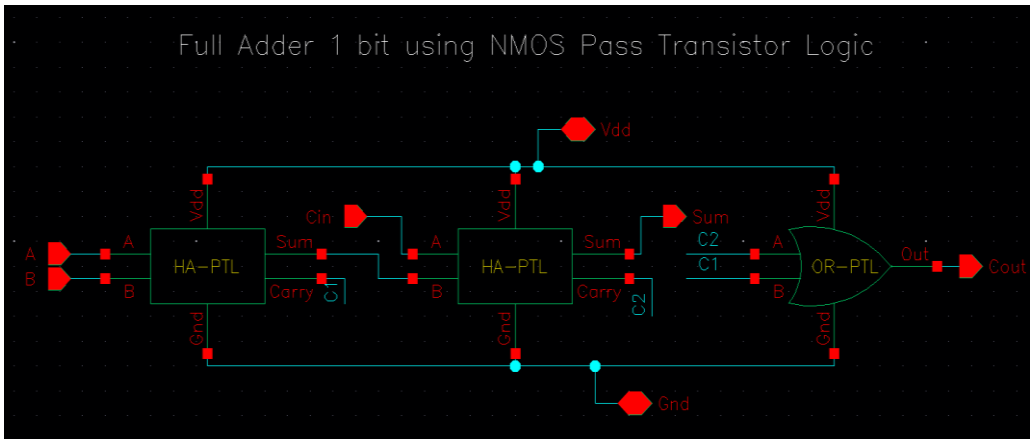


Figure 18: Block Diagram of a Full Adder

The above figure is the Block Diagram of a 1-bit Full Adder formed using two Half Adders and one OR gate using PTL. The circuit remains same for Transmission Gate and CMOS Gate logic as well.

3.4 4-BIT RIPPLE CARRY ADDER

A 4-bit Ripple Carry Adder (RCA) is formed using four 1-bit Full Adders cascaded in a series connection with the Carry out of one stage acting as Carry in to another stage.

A 4-bit Ripple Carry Adder (RCA) is used to calculate the binary addition of two 4bit binary numbers.

Since it is made using four 1-bit Full Adders, a 4-bit RCA has 8 inputs namely (A0 B0,……A3B3) and 4 Sum outputs namely (S0,…..S3) and a single Carry in as (Cin) to the adder at first stage and a single Carry out as (Cout) from the final stage in the adder chain.

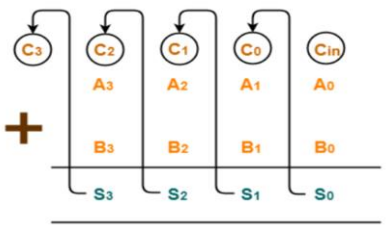


Figure 19: Adding two 4bit numbers

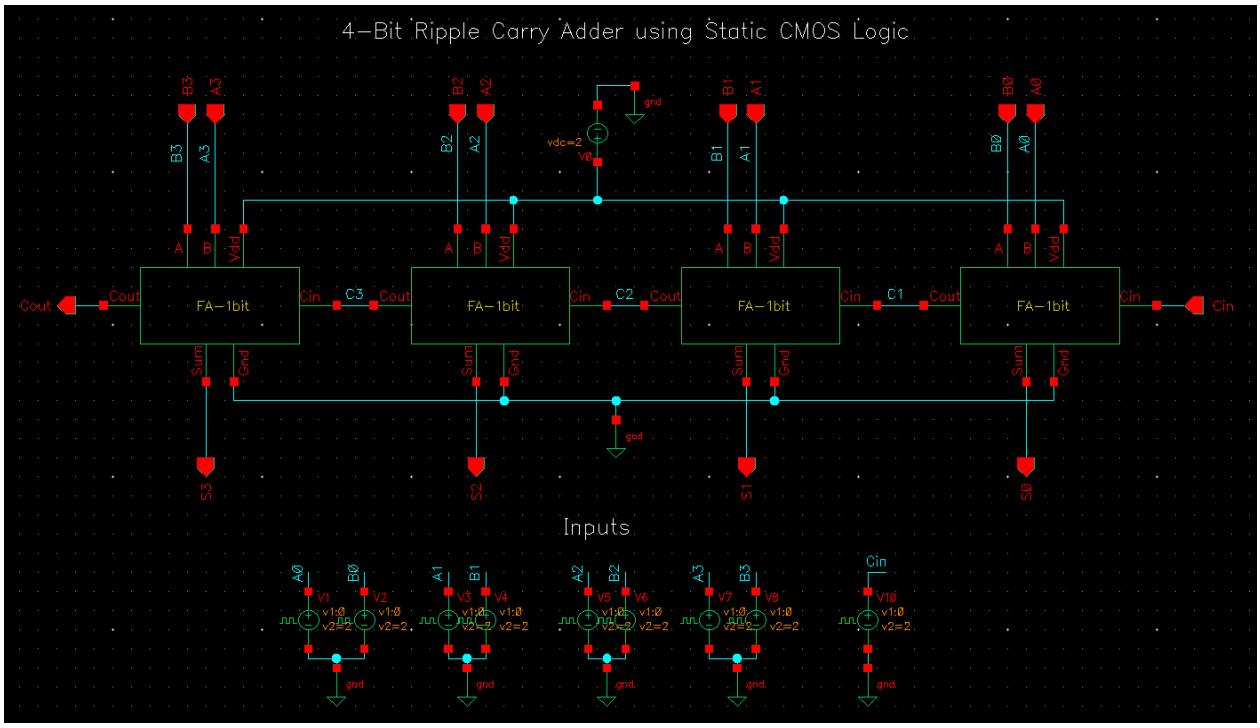


Figure 20: 4-bit RCA using Static CMOS Logic

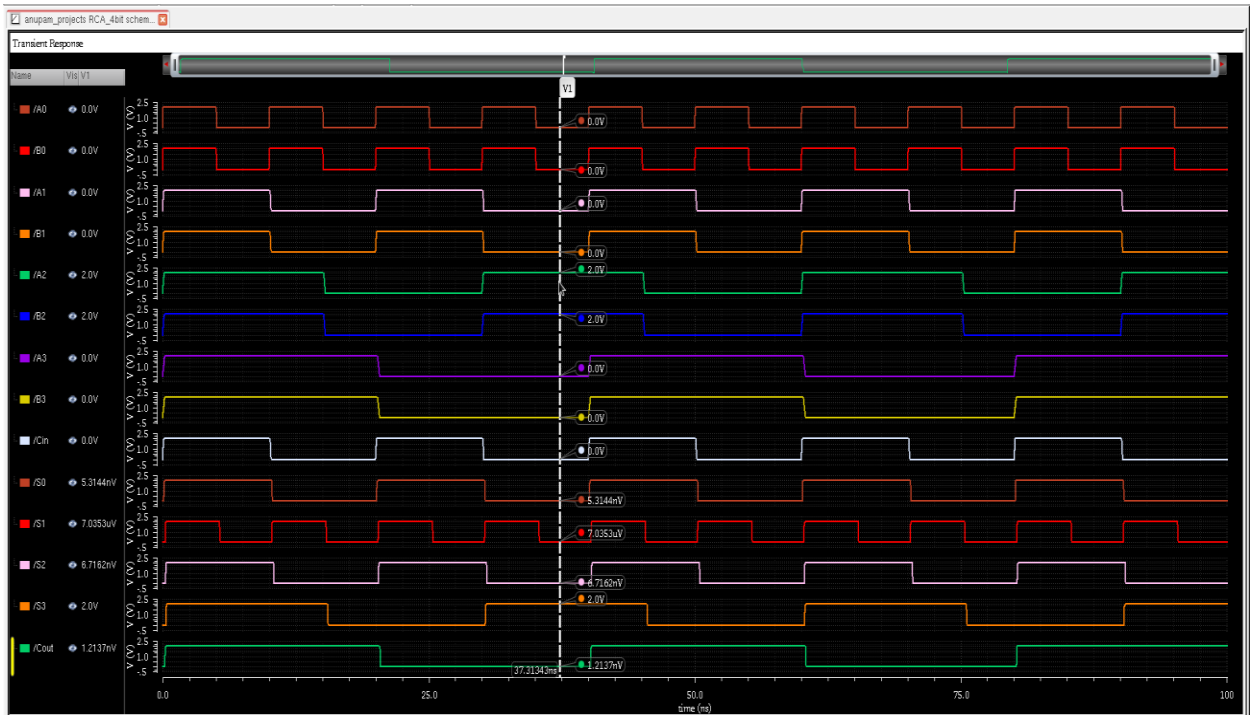


Figure 21: Waveform of 4-bit RCA using Static CMOS Logic

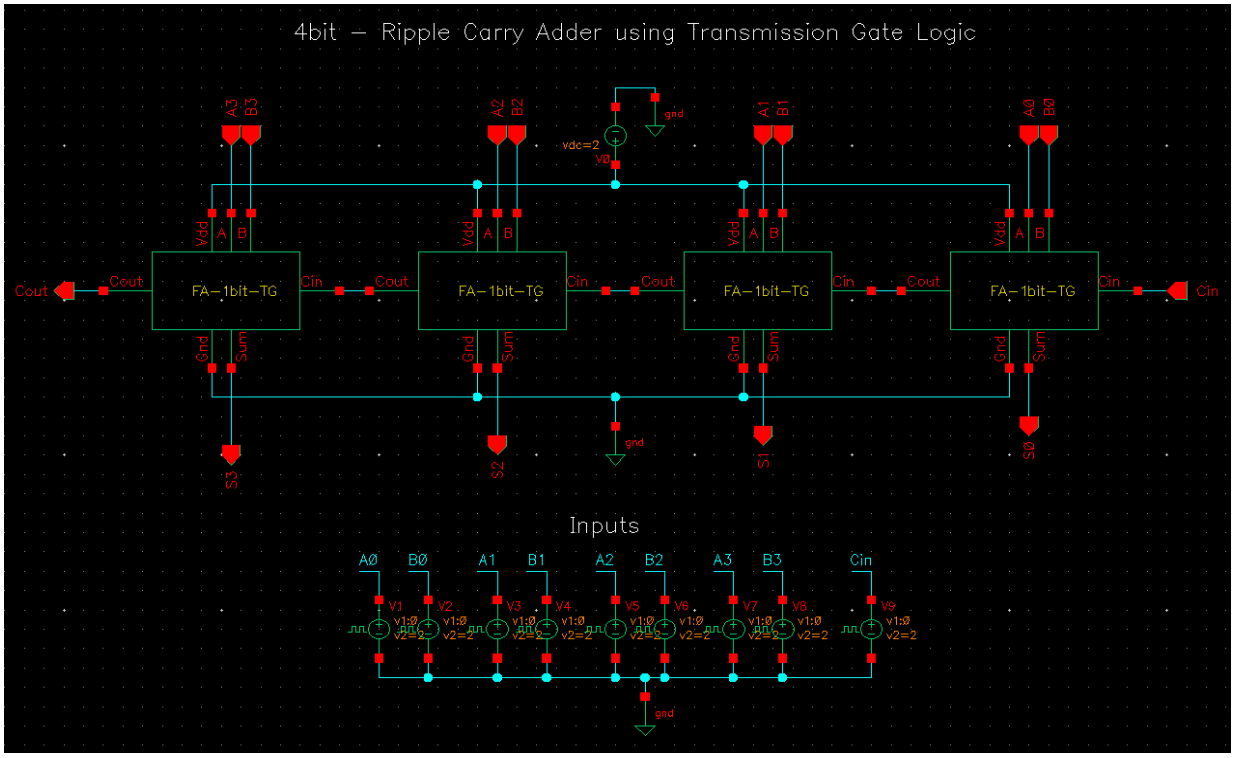


Figure 22: 4-bit RCA using TG Logic

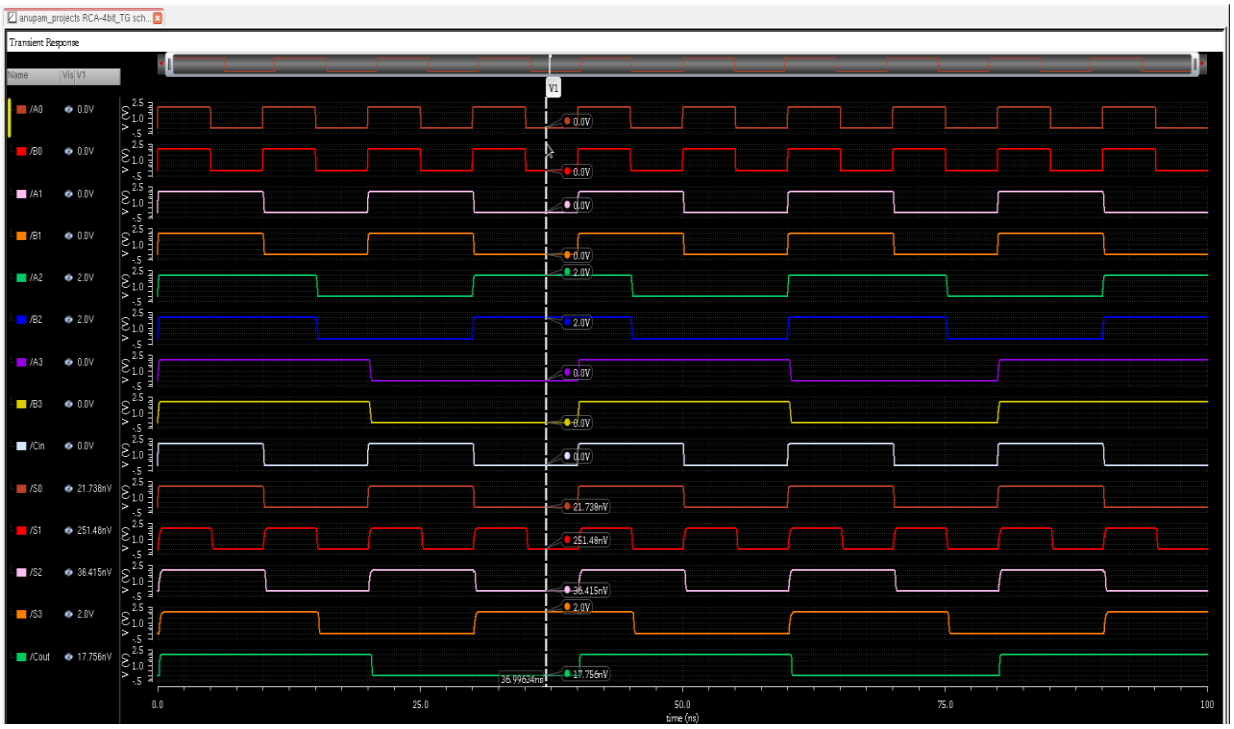


Figure 23: Waveform of 4-bit RCA using TG Logic

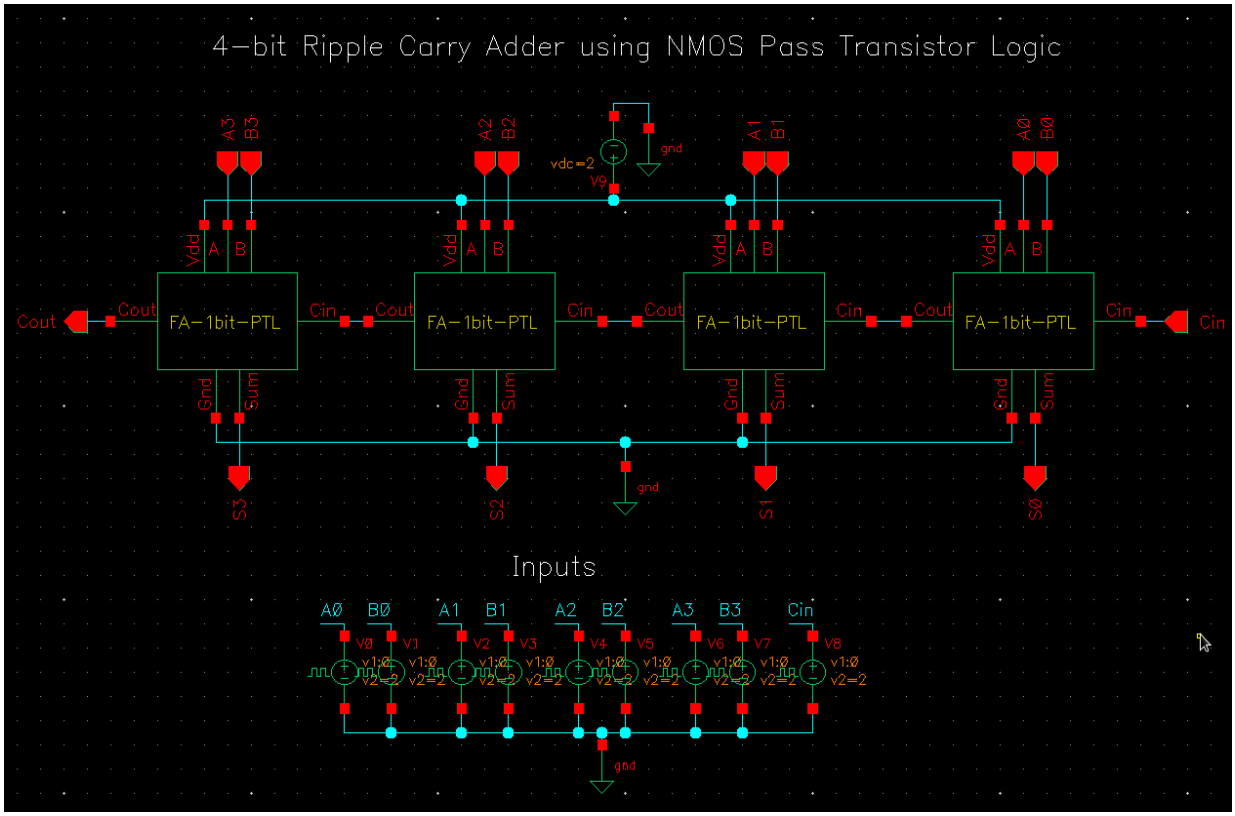


Figure 24: 4-bit RCA using NMOS PTL

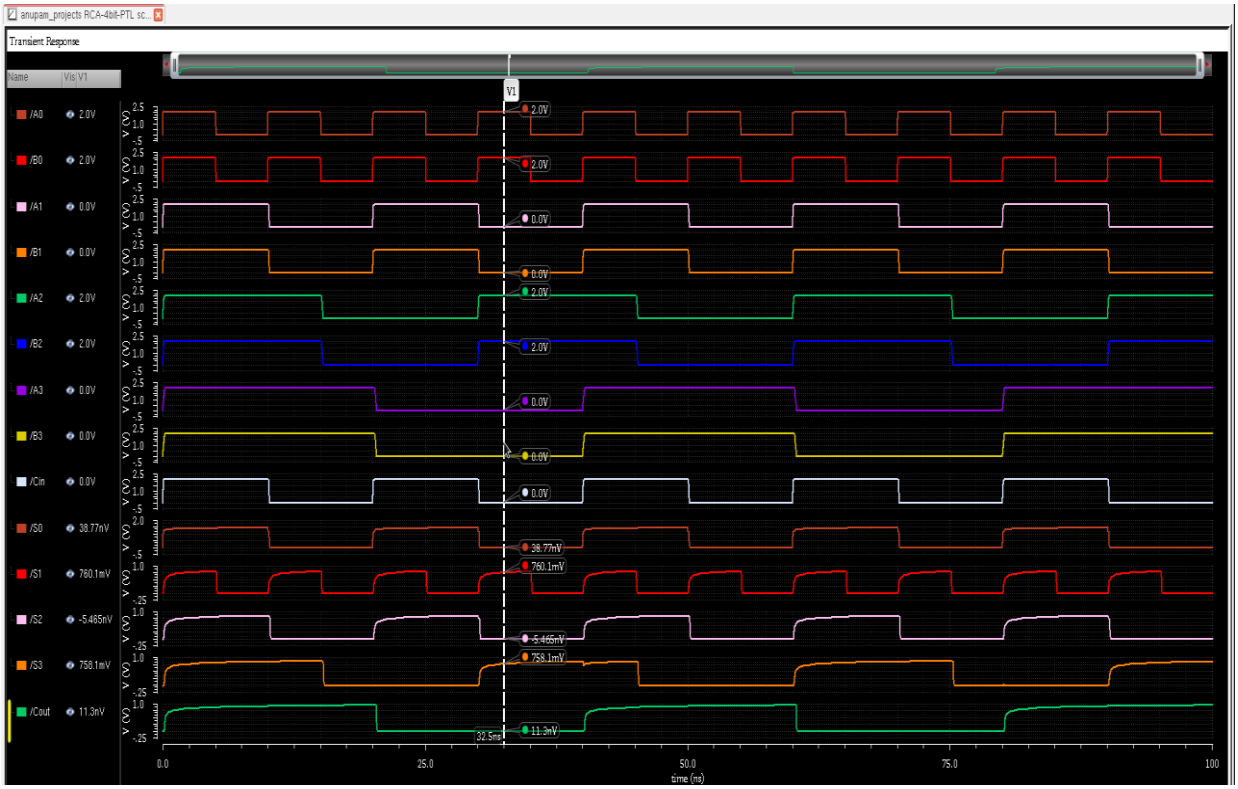


Figure 25: Waveform of 4-bit RCA using NMOS PTL

CHAPTER 4: RESULTS AND INFERENCES

4.1 TRANSISTOR COUNT

Upon analysis, following stats were obtained at gpdk 180nm technology node.

	TRANSISTOR COUNT
LOGIC	
Static CMOS	184
TG	136
NMOS PTL	96

Figure 26: Transistor Count

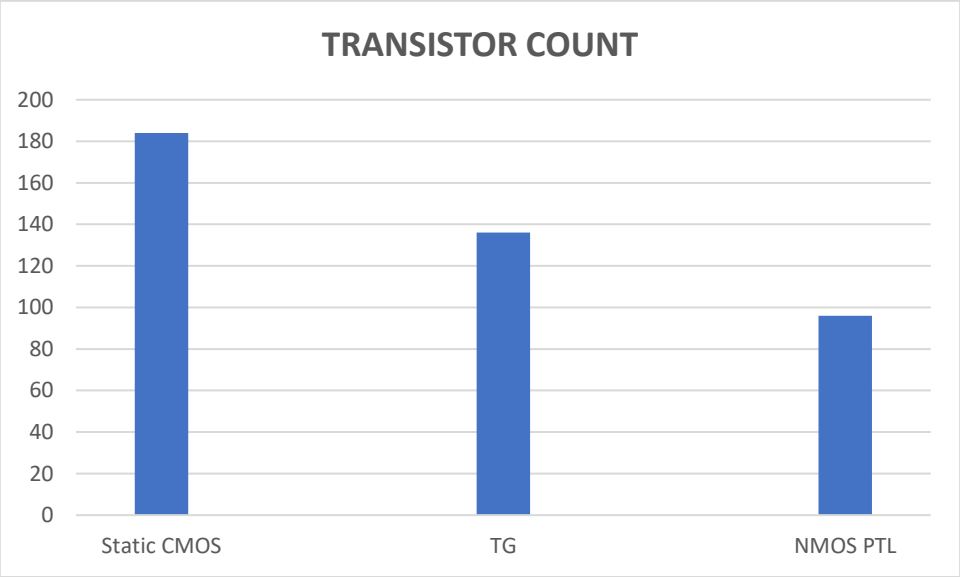


Figure 27: Graph for Transistor Count

- It's clearly evident from the above results that Static CMOS logic requires the greatest number of transistors to perform the same functionality of a 4-bit RCA as compared to Transmission Gate and NMOS Pass Transistor Logic, whereas NMOS PTL requires the least amount of transistor to perform the same functionality.

4.2 AVERAGE POWER CONSUMPTION

Upon analysis, following stats were obtained at gpdk 180nm technology node.

	AVERAGE POWER (in uW)		
	Voltage		
LOGIC	2V	4V	6V
Static CMOS	490.226	2406.71	7096.9
TG	312.665	1538.4	4492.9
NMOS PTL	574.382	4915.83	18951

Figure 28: Average Power Consumption (in uW)

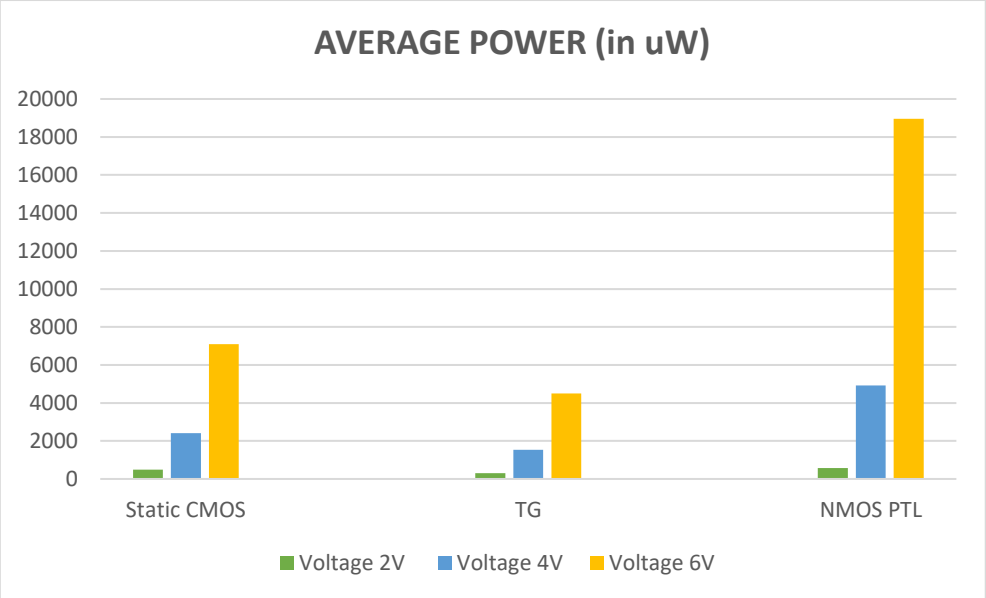


Figure 29: Graph of Average Power Consumption

- It's clearly evident from the above results that NMOS PTL consumes the greatest amount of Average Power to perform the same functionality of a 4-bit RCA as compared to Transmission Gate and Static CMOS Logic, whereas Transmission Gate Logic consumes the least amount of Average Power to perform the same functionality.

4.3 PROPAGATION DELAY

Upon analysis, following stats were obtained at gpdk 180nm technology node. Here to calculate the propagation delay of a 4-bit RCA, carry in from the first stage and carry out from the last stage was taken. To calculate Propagation Delay, average of Fall time delay (tpdf) and Rise time delay (tpdr) was taken.

	PROPAGATION DELAY (in ps)		
	Voltage		
LOGIC	2V	4V	6V
Static CMOS	631.917	589.078	577.454
TG	605.768	569.057	558.091
NMOS PTL	607.64	557.341	548.526

Figure 30: Propagation Delay (in ns)

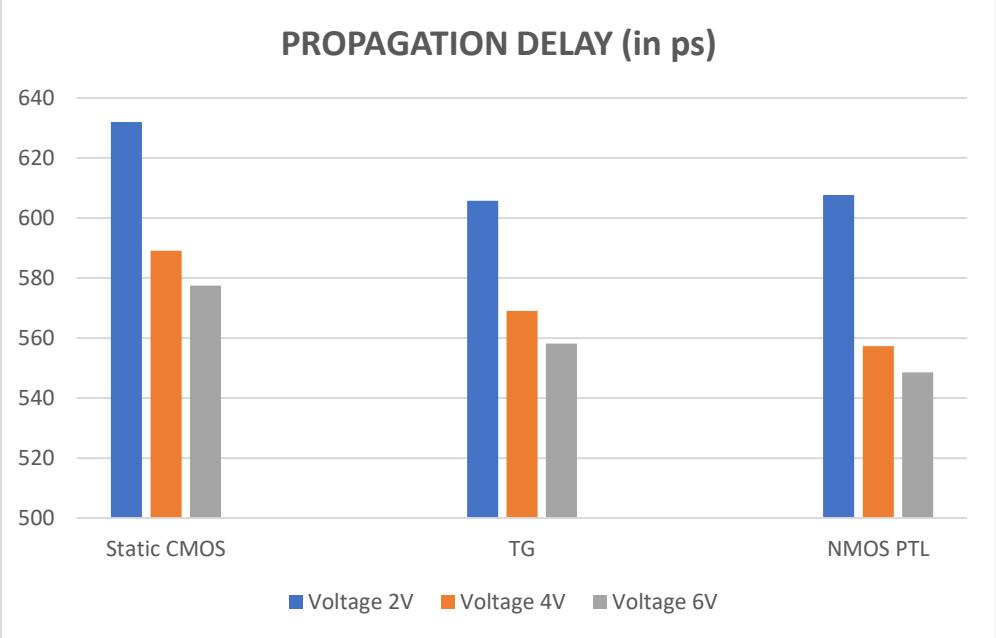


Figure 31: Graph for Propagation Delay

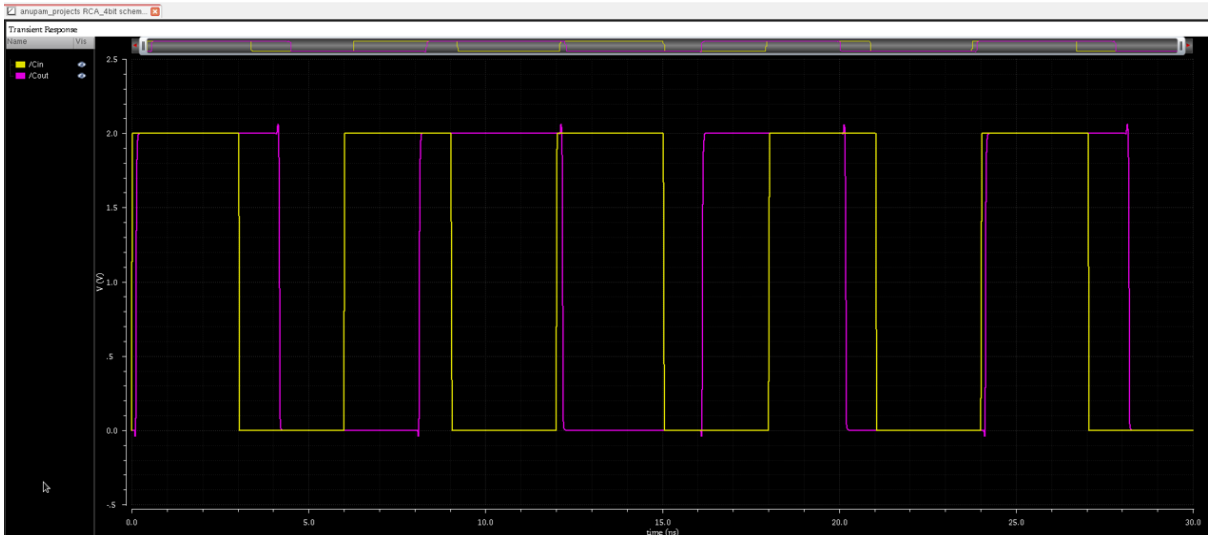


Figure 32: Propagation Dealy 4-bit RCA Static CMOS Logic

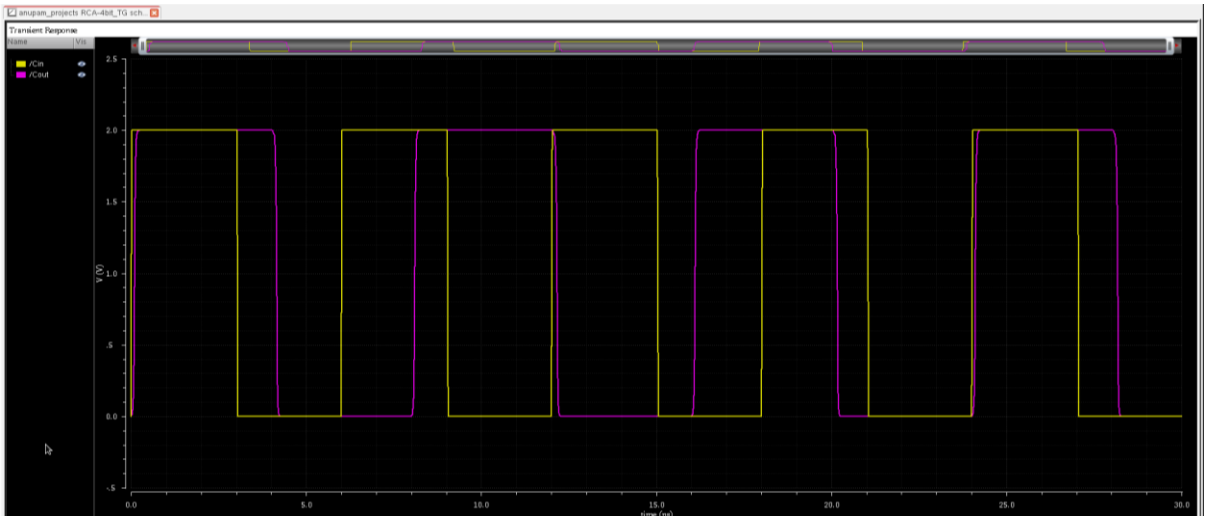


Figure 33: Propagation Dealy 4-bit RCA TG Logic

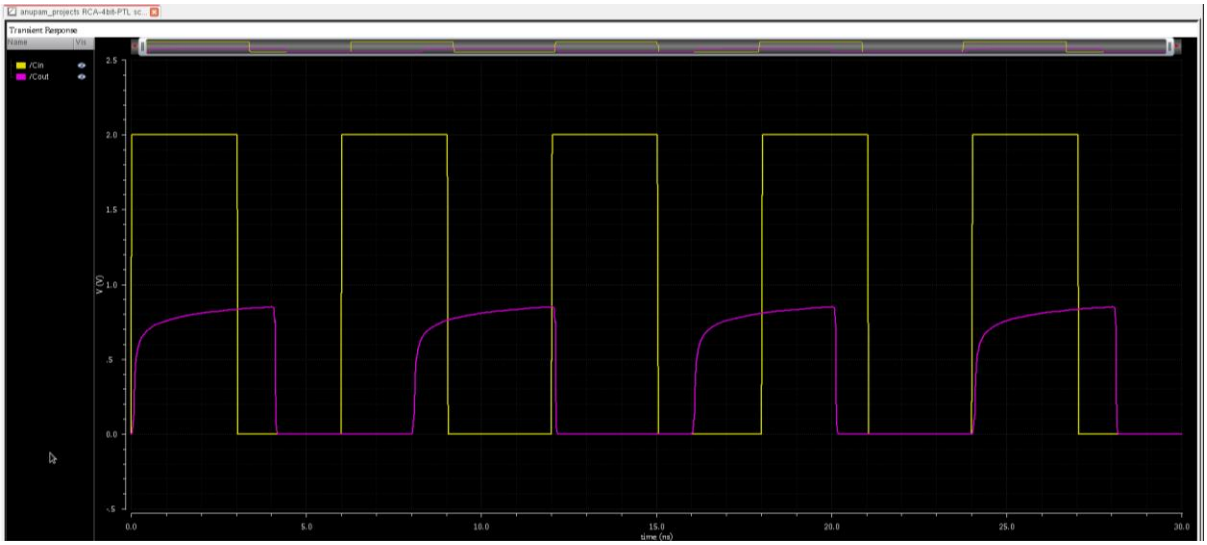


Figure 34: Propagation Dealy 4-bit RCA PTL

- It's clearly evident from the above results that NMOS PTL takes the least amount of Propagation Delay to produce the carry out of a 4-bit RCA as compared to Transmission Gate and Static CMOS Logic, whereas Static CMOS Logic takes the greatest amount of Propagation Delay to produce the carry out of a 4-bit RCA.

4.4 POWER DELAY PRODUCT (PDP)

Upon analysis, following stats were obtained at gpdk 180nm technology node.

	POWER DELAY PRODUCT (PDP) (in 10^-15 J)		
	Voltage		
LOGIC	2V	4V	6V
Static CMOS	309.7821432	1417.739913	4098.133293
TG	189.4024517	875.4372888	2507.447054
NMOS PTL	349.0174785	2739.793608	10395.11623

Figure 35: Power Delay Product (PDP) (in 10^-15 J)

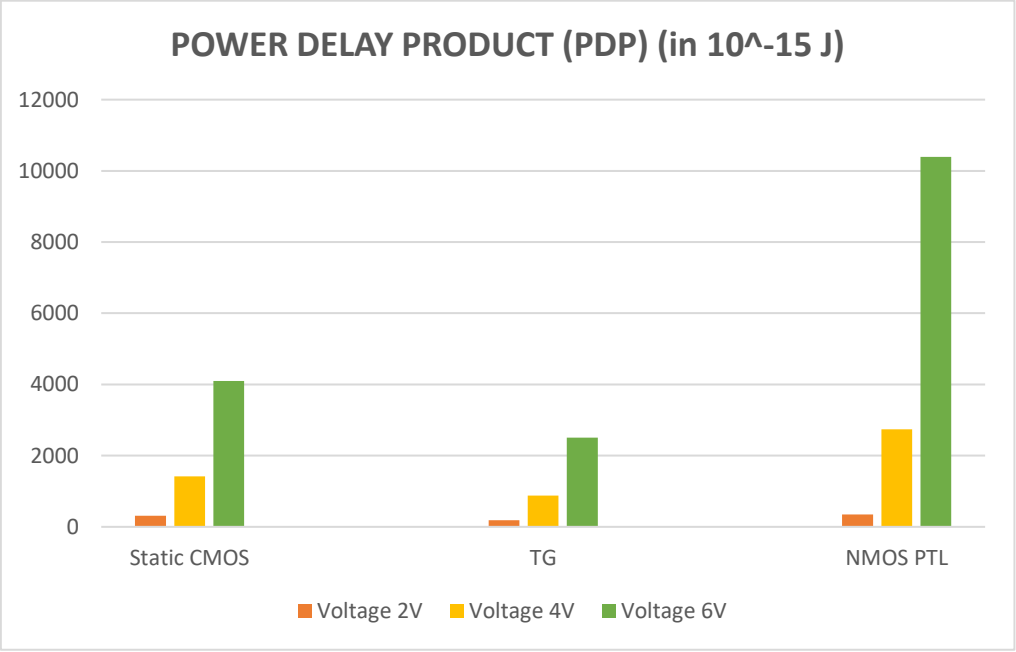


Figure 36: Graph for Power Delay Product

- It's clearly evident from the above results that NMOS PTL provides the greatest amount of Power Delay Product of a 4-bit RCA as compared to Transmission Gate and Static CMOS Logic, whereas Transmission Gate logic provides the least amount of Power Delay Product of a 4-bit RCA.

CHAPTER 5: CONCLUSION

The aim of this study was to compare a 4-bit Ripple Carry Adder made using different logic schemes namely, Static - Complementary Metal Oxide Semiconductor (Static-CMOS), Transmission Gate Logic, N - channel Metal Oxide Semiconductor - Pass Transistor Logic (NMOS - PTL) on the basis of common performance analysis parameters such as Transistor Count, Average Power consumption, Propagation Delay and Power Delay Product (PDP) In Cadence Virtuoso Design Environment on gpdk 180nm Technology node.

There were a fair share of advantages and disadvantages of choosing a particular logic scheme upon analysis of the results obtained during this study.

It all depends upon the designer's requirement to adopt a particular logic scheme for the design. If the design requires a stable and full rail – to – rail swing of the voltage levels then Static CMOS logic is the best choice but a trade-off in terms of Transistor Count, Average Power consumption and Propagation delay needs to be made as this logic scheme increases the overhead area which affects these parameters directly.

If the design requires the least Propagation Delay, less Transistor Count than NMOS PTL is the best choice but it may suffer through the problem of leakage currents as a direct path may form between the Vdd and ground which may lead to increased Average Power Consumption.

Also, the design may not provide full rail – to – rail swing of the voltage levels as NMOS passes weak logic 1 (HIGH) and gives a maximum of (Vdd-Vthn) at the output and therefore may require the use of level restoration circuits at various stages to again charge it to Vdd (logic HIGH).

In some cases, Transmission Gate logic comes handy as it has both the benefits of less Transistor Count compared to static CMOS logic and low Average Power Consumption compared to both Static CMOS logic and NMOS PTL but can have more Propagation Delay than NMOS PTL.

This study was performed on gpdk 180nm Technology node, further in future the same study can be performed on different technology nodes to analyse the performance of the 4-bit RCA.

CHAPTER 6: REFERENCES

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