



# TPS51206 2-A Peak Sink / Source DDR Termination Regulator With VTTREF Buffered Reference for DDR2, DDR3, DDR3L, and DDR4

## 1 Features

- Supply Input Voltage: Supports 3.3-V Rail and 5-V Rail
- VLDOIN Input Voltage Range: VTT+0.4 V to 3.5 V
- VTT Termination Regulator
  - Output Voltage Range: 0.5 V to 0.9 V
  - 2-A Peak Sink and Source Current
  - Requires Only 10-μF MLCC Output Capacitor
  - ±20 mV Accuracy
- VTTREF Buffered Reference
  - VDDQ/2 ± 1% Accuracy
  - 10-mA Sink and Source Current
- Supports High-Z in S3 and Soft-Stop in S4 and S5 with S3 and S5 Inputs
- Overtemperature Protection
- 10-Pin, 2 mm × 2 mm SON (DSQ) Package

## 2 Applications

- DDR2, DDR3, DDR3L, and DDR4 Memory Power Supplies
- SSTL\_18, SSTL\_15, SSTL\_135 and HSTL Termination

## 3 Description

The TPS51206 is a sink and source double data rate (DDR) termination regulator with VTTREF buffered reference output. It is specifically designed for low-input voltage, low-cost, low-external component count systems where space is a key consideration. The TPS51206 maintains fast transient response and only requires 1 × 10-μF of ceramic output capacitance. The TPS51206 supports a remote sensing function and all power requirements for DDR2, DDR3 and Low-Power DDR3 (DDR3L), and DDR4 VTT bus. The VTT current capability is ±2-A peak. The device supports all of the DDR power states, putting VTT to High-Z in S3 state (suspend to RAM) and discharging VTT and VTTREF in S4 or S5 state (suspend to disk).

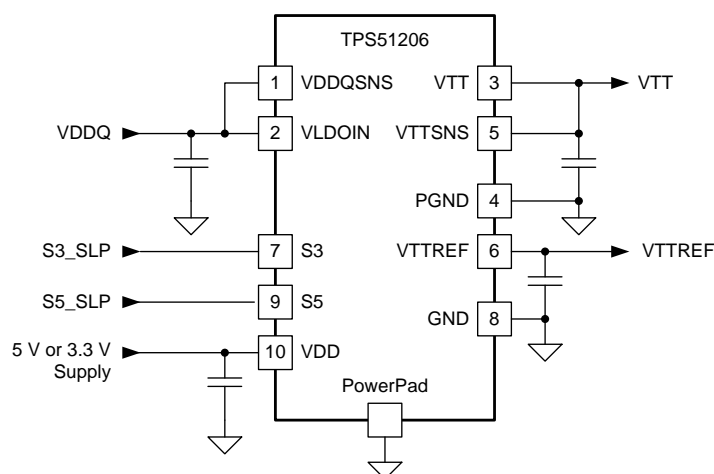
The TPS51206 is available in 10-pin, 2 × 2, SON (DSQ) PowerPAD™ package and specified from -40°C to 85°C.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS51206	WSO (10)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Simplified Application



Copyright © 2016, Texas Instruments Incorporated



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>12</b>
<b>2 Applications</b> .....	<b>1</b>	8.1 Application Information.....	12
<b>3 Description</b> .....	<b>1</b>	8.2 Typical Applications .....	12
<b>4 Revision History</b> .....	<b>2</b>	<b>9 Power Supply Recommendations</b> .....	<b>16</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Layout</b> .....	<b>16</b>
<b>6 Specifications</b> .....	<b>4</b>	10.1 Layout Guidelines .....	16
6.1 Absolute Maximum Ratings .....	4	10.2 Layout Example .....	17
6.2 ESD Ratings.....	4	10.3 Thermal Considerations .....	17
6.3 Recommended Operating Conditions.....	4	<b>11 Device and Documentation Support</b> .....	<b>18</b>
6.4 Thermal Information .....	4	11.1 Device Support.....	18
6.5 Electrical Characteristics.....	5	11.2 Receiving Notification of Documentation Updates .....	18
6.6 Typical Characteristics .....	6	11.3 Community Resources.....	18
<b>7 Detailed Description</b> .....	<b>10</b>	11.4 Trademarks .....	18
7.1 Overview .....	10	11.5 Electrostatic Discharge Caution.....	18
7.2 Functional Block Diagram .....	10	11.6 Glossary .....	18
7.3 Feature Description.....	10	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>18</b>
7.4 Device Functional Modes.....	11		

## 4 Revision History

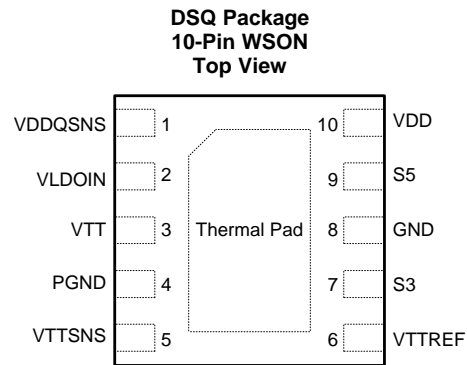
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (December 2014) to Revision C</b>	<b>Page</b>
• Added references to DDR4 compatibility .....	<b>1</b>
• Added <a href="#">Receiving Notification of Documentation Updates</a> section .....	<b>18</b>
• Added <a href="#">Community Resources</a> section .....	<b>18</b>

<b>Changes from Revision A (October 2013) to Revision B</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>

<b>Changes from Original (MAY 2011) to Revision A</b>	<b>Page</b>
• Added minimum and maximum values to the wake up condition of the VDD UVLO threshold voltage specification .....	<b>5</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	8	—	Signal ground
PGND	4	—	Power GND for VTT LDO
S3	7	I	S3 signal input
S5	9	I	S5 signal input
VDD	10	I	Device power supply input (3.3 V or 5 V)
VDDQSNS	1	I	VDDQ sense input, reference input for VTTREF
VLDOIN	2	I	Power supply input for VTT/ VTTREF
VTT	3	O	Power output for VTT LDO, need to connect 10-μF or greater MLCC for stability
VTTREF	6	O	VTTREF buffered reference output. Need to connect 0.22-μF or greater MLCC for stability
VTTSNS	5	I	VTT LDO voltage sense input
Thermal Pad		—	Solder to the ground plane for increased thermal performance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage <sup>(2)</sup>	VDD, S3, S5	−0.3	7	V
	VLDOIN, VTTSNS, VDDQSNS	−0.3	3.6	V
	PGND	−0.3	0.3	
Output voltage <sup>(2)</sup>	VTT, VTTREF	−0.3	3.6	
Junction temperature, T <sub>J</sub>			125	°C
Operating free-air temperature, T <sub>A</sub>		−55	150	°C
Storage temperature, T <sub>stg</sub>		−55	150	°C

- (1) Stresses beyond those listed under [Absolute Maximum Ratings](#)<sup>(1)</sup> may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal unless otherwise noted.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage	VDD	3.1		6.5	V
Input voltage range <sup>(1)</sup>	S3, S5	−0.1		6.5	V
	VLDOIN, VTTSNS, VDDQSNS	−0.1		3.5	
	PGND	−0.1		0.1	
Output voltage range <sup>(1)</sup>	VTT, VTTREF	−0.1		3.5	V
Operating free-air temperature, T <sub>A</sub>		−40		85	°C

- (1) All voltage values are with respect to the network ground terminal unless otherwise noted.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS51206	UNIT
		DSQ (WSN)	
		10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	70.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	46.3	
R <sub>θJB</sub>	Junction-to-board thermal resistance	33.8	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.9	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	33.5	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	16.3	

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

## 6.5 Electrical Characteristics

over operating free-air temperature range,  $V_{DD} = 5\text{ V}$ , VLDOIN is connected to VDDQSNS,  $V_{S3} = V_{S5} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
$I_{VDD(S0)}$	VDD supply current, in S0	$T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 5\text{ V}$ , $V_{VDDQSNS} = 1.8\text{ V}$		170		$\mu\text{A}$
$I_{VDD(S3)}$	VDD supply current, in S3	$T_A = 25^\circ\text{C}$ , No load, $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VDDQSNS} = 1.8\text{ V}$		80		$\mu\text{A}$
$I_{VDDSDN}$	VDD shutdown current, in S4 and S5	$T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 0\text{ V}$ , $V_{VDDQSNS} = 1.8\text{ V}$			1	$\mu\text{A}$
$I_{VLDOIN(S0)}$	VLDOIN supply current, in S0	$T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 5\text{ V}$ , $V_{LDION} = 1.8\text{ V}$			5	$\mu\text{A}$
$I_{VLDOIN(S3)}$	VLDOIN supply current, in S3	$T_A = 25^\circ\text{C}$ , No load, $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{LDION} = 1.8\text{ V}$			5	$\mu\text{A}$
$I_{VLDOINSDN}$	VLDOIN shutdown current, in S4 and S5	$T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 0\text{ V}$ , $V_{LDION} = 1.8\text{ V}$			5	$\mu\text{A}$
<b>VTTREF OUTPUT</b>						
$V_{VTTREF}$	Output voltage		$V_{VDDQSNS}/2$			V
$V_{VTTREFTOL}$	Output voltage tolerance to $V_{VDDQSNS}$	$ I_{VTTREF}  < 10\text{ mA}$ , $1.5\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}$	49%	50%	51%	
		$ I_{VTTREF}  < 10\text{ mA}$ , $1.2\text{ V} \leq V_{VDDQSNS} < 1.5\text{ V}$	48.75%		51.25%	
$I_{VTTREFSRC}$	Source current	$V_{VDDQSNS} = 1.8\text{ V}$ , $V_{VTTREF} = 0\text{ V}$	10			mA
$I_{VTTREFSNK}$	Sink current	$V_{VDDQSNS} = 0\text{ V}$ , $V_{VTTREF} = 1.8\text{ V}$	10			mA
$I_{VTTREFDIS}$	VTTREF Discharge current	$T_A = 25^\circ\text{C}$ , $V_{S3} = V_{S5} = 0\text{ V}$ , $V_{VTTREF} = 0.5\text{ V}$		1.3		mA
<b>VTT OUTPUT</b>						
$V_{VTT}$	Output voltage		$V_{VDDQSNS}/2$			V
$V_{VTTTOL}$	Output voltage tolerance to $V_{VDDQSNS}/2$	$ I_{VTT}  \leq 10\text{ mA}$ , $1.4\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}$	–20		20	mV
		$ I_{VTT}  < 1\text{ A}$ , $1.4\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}^{(1)}$	–30		30	
		$ I_{VTT}  < 2\text{ A}$ , $1.4\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}^{(1)}$	–40		40	
		$ I_{VTT}  \leq 10\text{ mA}$ , $1.2\text{ V} \leq V_{VDDQSNS} \leq 1.4\text{ V}$	–20		20	
		$ I_{VTT}  < 1\text{ A}$ , $1.2\text{ V} \leq V_{VDDQSNS} \leq 1.4\text{ V}^{(1)}$	–30		30	
		$ I_{VTT}  < 1.5\text{ A}$ , $1.2\text{ V} \leq V_{VDDQSNS} < 1.4\text{ V}^{(1)}$	–40		40	
$I_{VTTCLSRC}$	Source current limit	$V_{VDDQSNS} = 1.8\text{ V}$ , $V_{VTT} = V_{VTTNS} = 0.7\text{ V}$	2			A
$I_{VTTCLSNK}$	Sink current limit	$V_{VDDQSNS} = 1.8\text{ V}$ , $V_{VTT} = V_{VTTNS} = 1.1\text{ V}$	2			A
$I_{VTTLK}$	Leakage current	$T_A = 25^\circ\text{C}$ , $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VTT} = V_{VTTREF}$			5	$\mu\text{A}$
$I_{VTTNSBIAS}$	VTTNS input bias current	$V_{S3} = 5\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VTTNS} = V_{VTTREF}$	–0.1		0.1	$\mu\text{A}$
$I_{VTTNSLK}$	VTTNS leakage current	$V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VTTNS} = V_{VTTREF}$	–0.1		0.1	$\mu\text{A}$
$I_{VTTDIS}$	VTT Discharge current	$T_A = 25^\circ\text{C}$ , $V_{S3} = V_{S5} = V_{VDDQSNS} = 0\text{ V}$ , $V_{VTT} = 0.5\text{ V}$		7		mA
<b>VDDQ INPUT</b>						
$I_{VDDQSNS}$	VDDQSNS input current	$V_{VDDQSNS} = 1.8\text{ V}$		30		$\mu\text{A}$
<b>UVLO/LOGIC THRESHOLD</b>						
$V_{VDDUV}$	VDD UVLO threshold voltage	Wake up	2.67	2.90	3.00	V
		Hysteresis		0.2		
$V_{LL}$	S3 and S5 low-level voltage				0.5	V
$V_{LH}$	S3 and S5 high-level voltage		1.8			V
$V_{LHYS}$	S3 and S5 hysteresis voltage			0.3		V
$I_{LHLK}$	S3 and S5 input leak current		–1		1	$\mu\text{A}$
<b>OVER-TEMPERATURE PROTECTION</b>						
$T_{OTP}$	Over temperature protection	Shutdown temperature <sup>(1)</sup>		150		$^\circ\text{C}$
		Hysteresis <sup>(1)</sup>		10		

(1) Ensured by design. Not production tested.

## 6.6 Typical Characteristics

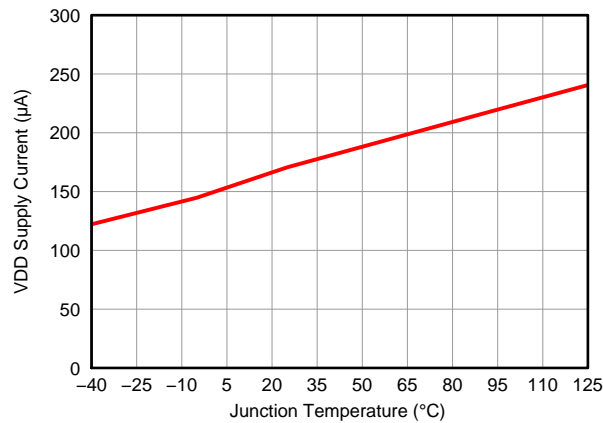


Figure 1. VDD Supply Current vs. Junction Temperature

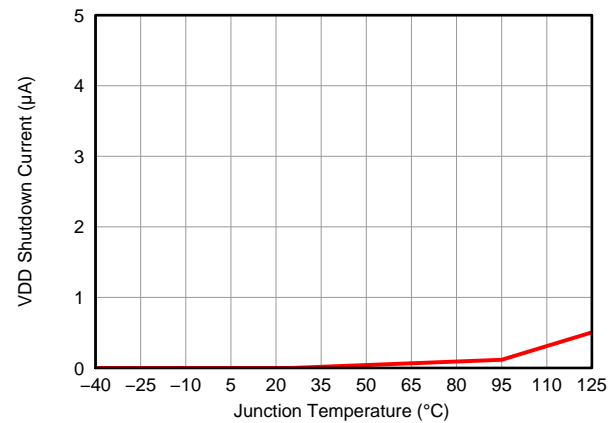


Figure 2. VDD Shutdown Current vs. Junction Temperature

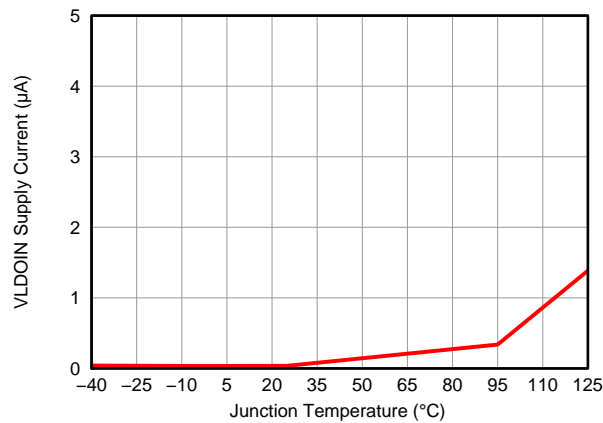


Figure 3. VLDOIN Supply Current vs. Junction Temperature

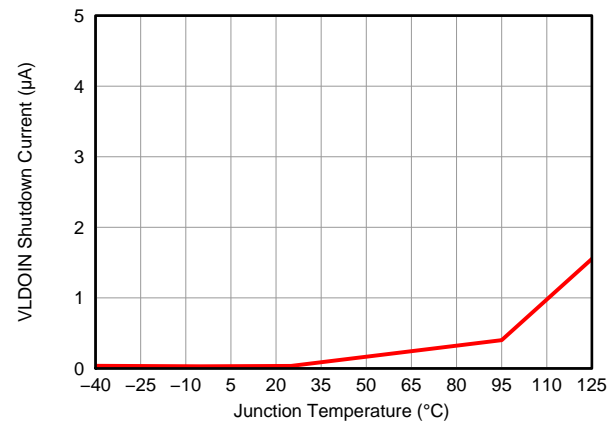


Figure 4. VLDOIN Shutdown Current vs. Junction Temperature

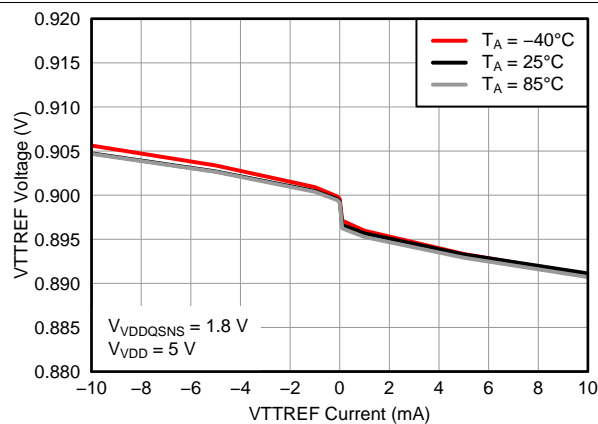


Figure 5. VTTREF Load Regulation (0.9 V)

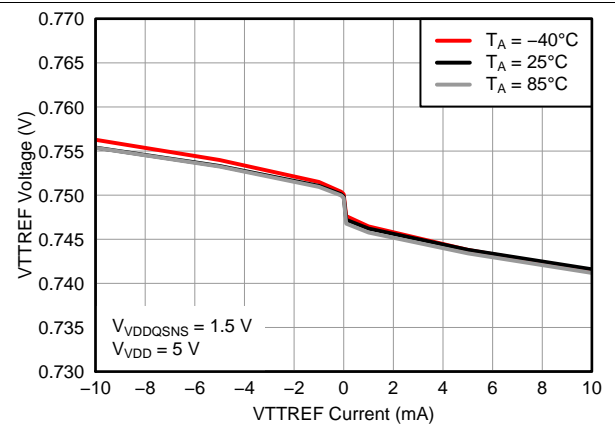
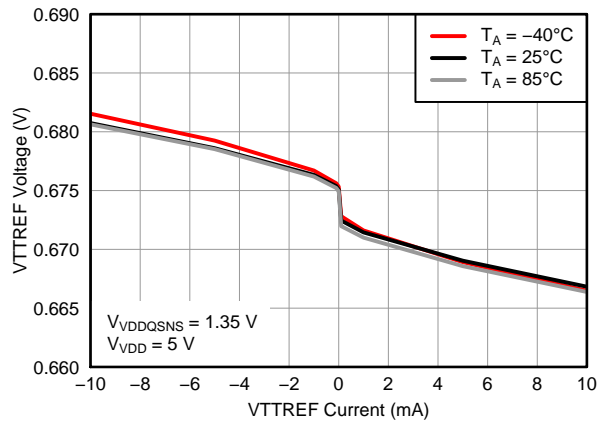
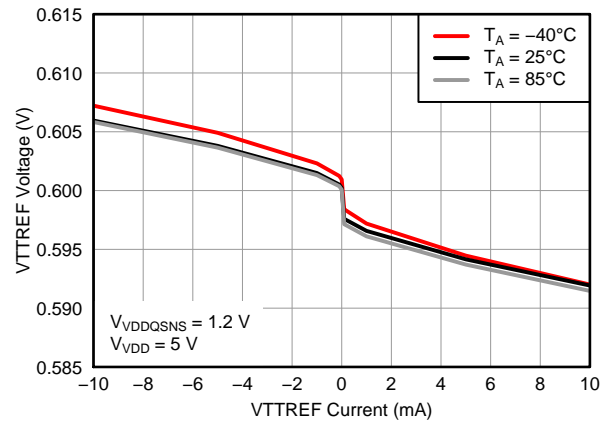


Figure 6. VTTREF Load Regulation (0.75 V)

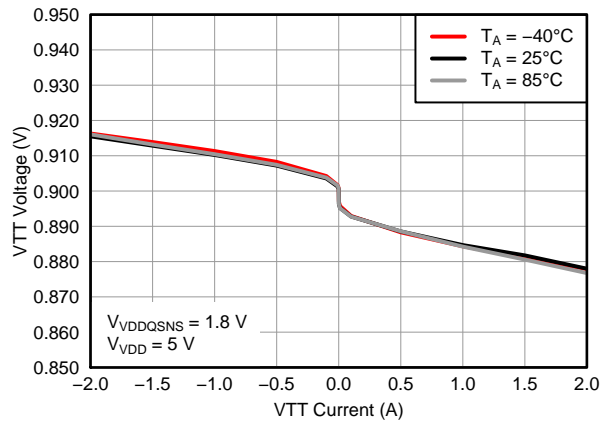
## Typical Characteristics (continued)



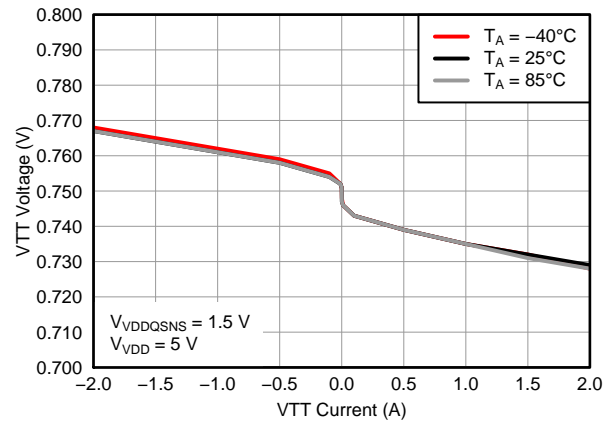
**Figure 7. VTTREF Load Regulation (0.675 V)**



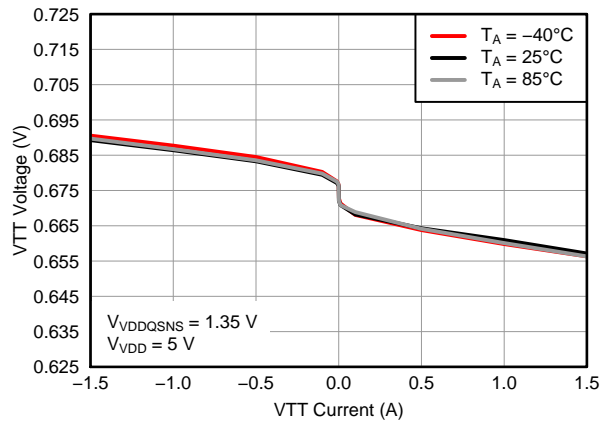
**Figure 8. VTTREF Load Regulation (0.6 V)**



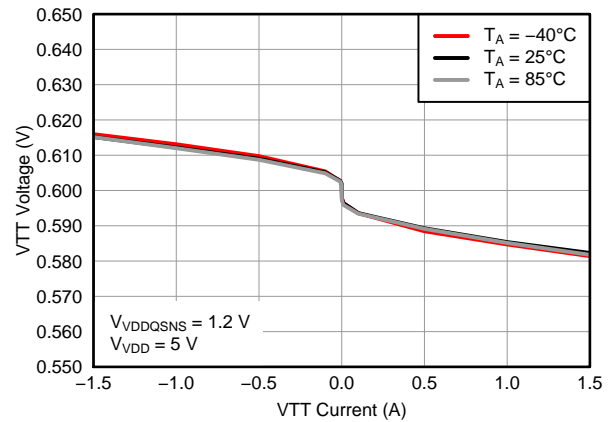
**Figure 9. VTT Load Regulation (0.9 V)**



**Figure 10. VTT Load Regulation (0.75 V)**



**Figure 11. VTT Load Regulation (0.675 V)**



**Figure 12. VTT Load Regulation (0.6 V)**

## Typical Characteristics (continued)

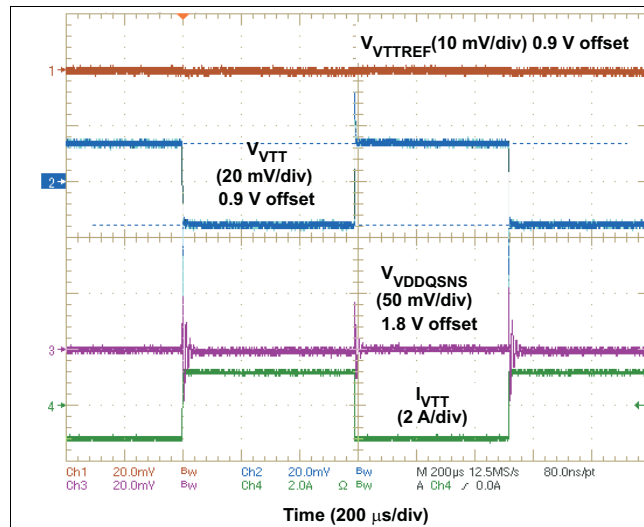


Figure 13. VTT Load Transient Response (0.9 V)

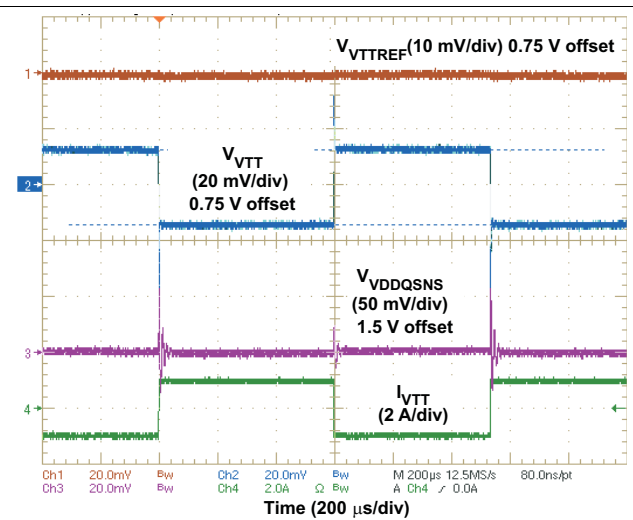


Figure 14. VTT Load Transient Response (0.75 V)

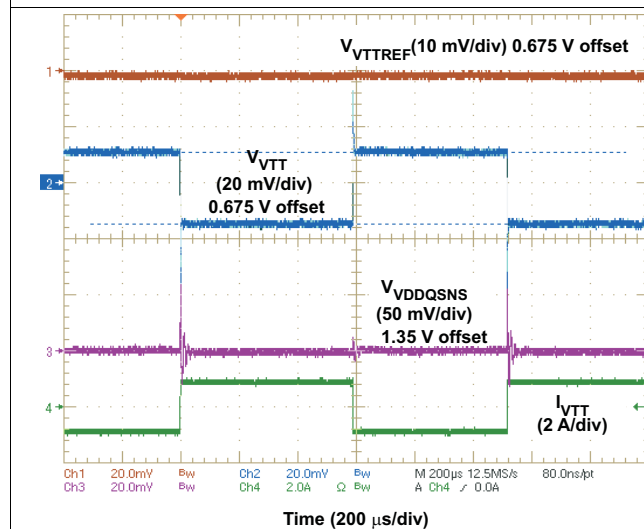


Figure 15. VTT Load Transient Response (0.675 V)

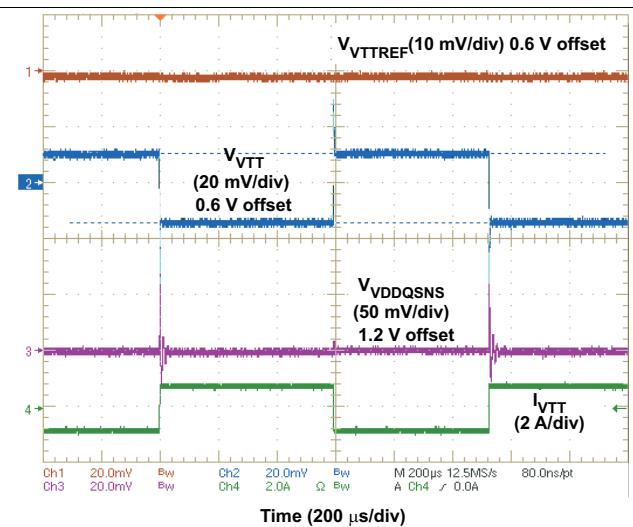


Figure 16. VTT Load Transient Response (0.6 V)

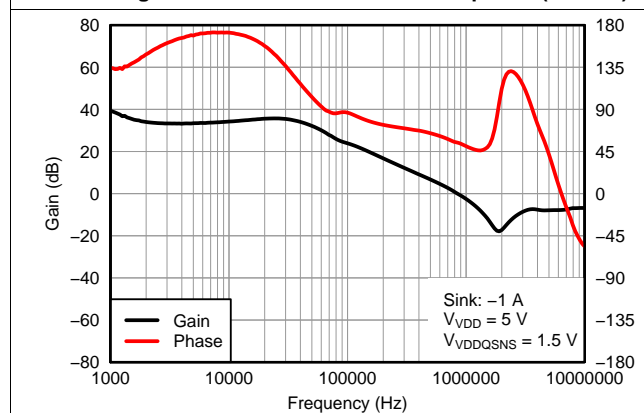


Figure 17. VTT (Sink: -1 A) Bode Plot (0.75 V)

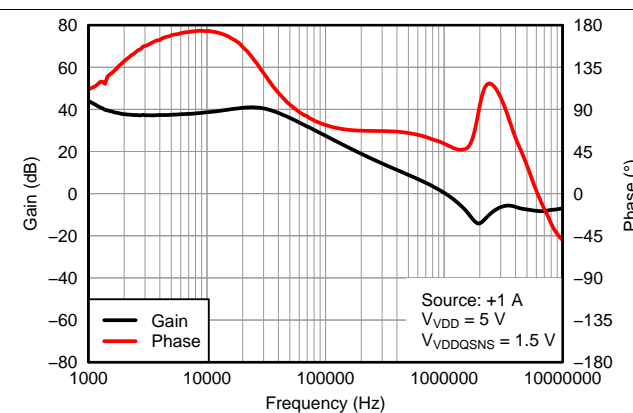
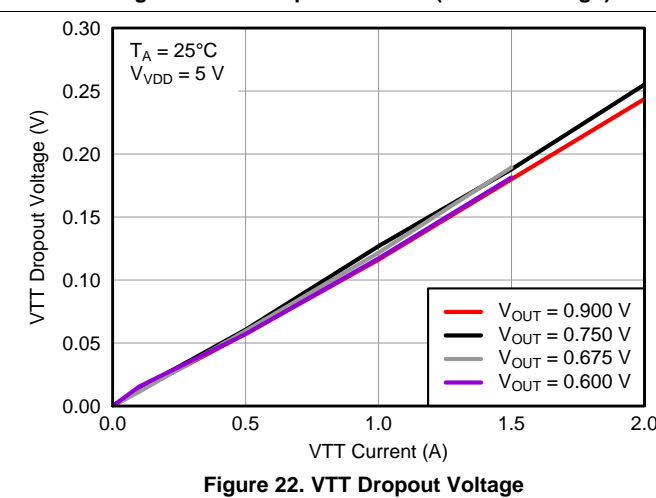
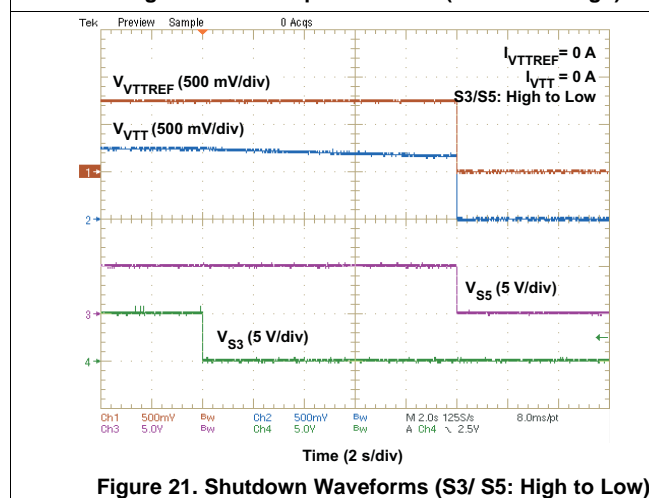
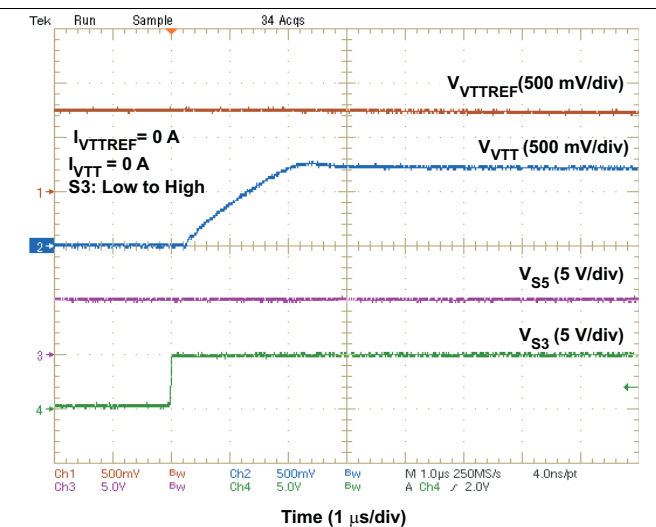
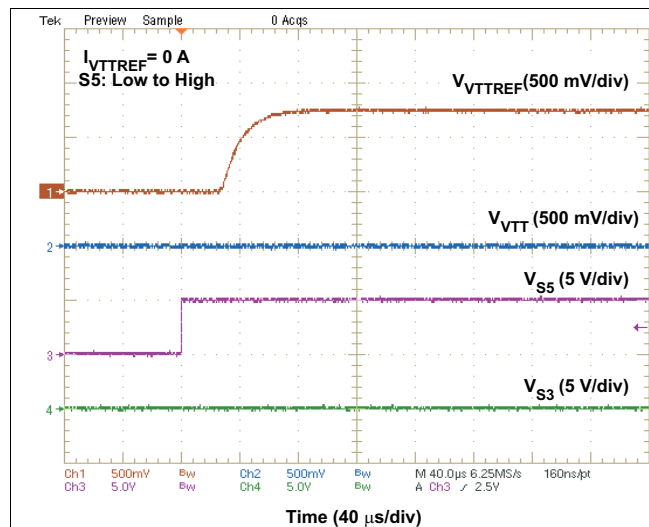


Figure 18. VTT (Source: +1 A) Bode Plot (0.75 V)



## Typical Characteristics (continued)

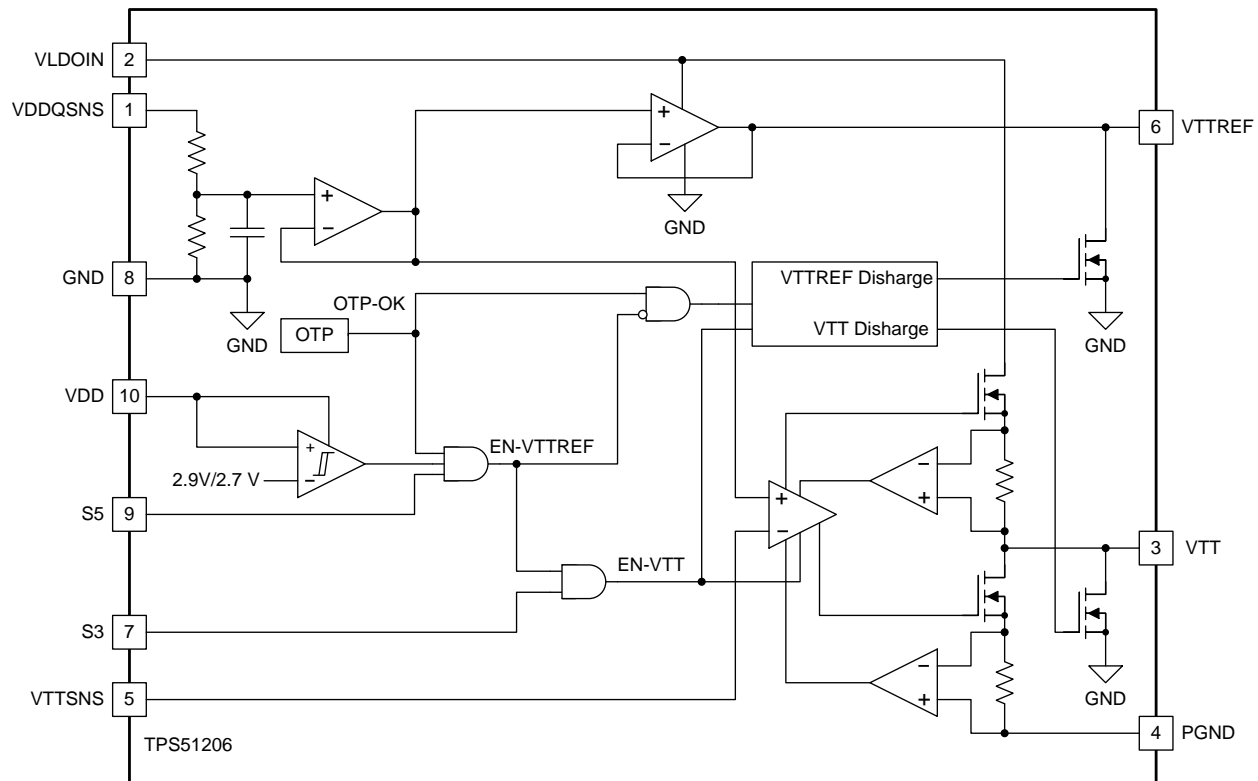


## 7 Detailed Description

## 7.1 Overview

The TPS51206 is a sink or source double data rate (DDR) termination regulator with VTTREF buffered reference output.

## 7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

### 7.3 Feature Description

### 7.3.1 VTT Sink and Source Regulator

The TPS51206 is a sink or source tracking termination regulator specifically designed for low input voltage, low cost, and low external component count systems where space is a key application parameter. The TPS51206 integrates a high-performance, low-dropout (LDO) linear regulator (VTT) that has ultimate fast response to track  $\frac{1}{2}$  VDDQSNS within 40 mV at all conditions, and its current capability is 2 A for both sink and source directions. A 10- $\mu$ F (or greater) ceramic capacitor(s) need to be attached close to the VTT terminal for stable operation. A grade of X5R or better is recommended. To achieve tight regulation with minimum effect of trace resistance, the remote sensing terminal, VTTSNS, should be connected to the positive terminal of the output capacitor(s) as a separate trace from the high current path from the VTT pin.

The device has a dedicated pin, VLDOIN, for VTT power supply to minimize the LDO power dissipation on user application. The minimum VLDOIN voltage is 0.4 V above the  $\frac{1}{2}$  VDDQSNS voltage.

### 7.3.2 VTTREF

The VTTREF pin includes 10 mA of sink or source current capability, and tracks  $\frac{1}{2}$  of VDDQSNS with  $\pm 1\%$  accuracy. A 0.22- $\mu$ F ceramic capacitor needs to be attached close to the VTTREF terminal for stable operation; X5R or better grade is recommended.

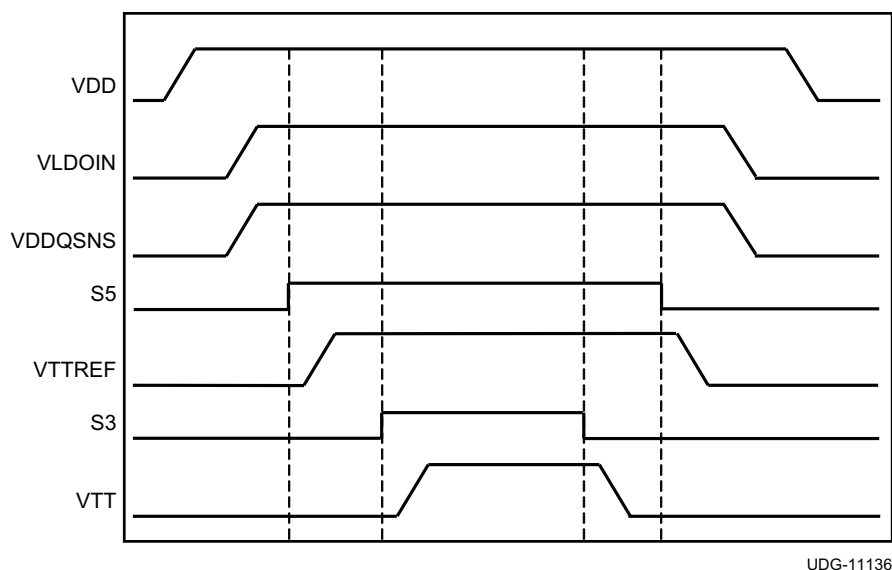
## Feature Description (continued)

### 7.3.3 VDD Undervoltage Lockout Protection

The TPS51206 input voltage (VDD) includes undervoltage lockout protection (UVLO). When the VDD pin voltage is lower than UVLO threshold voltage, VTT and VTTREF are shut off. This is non-latch protection.

### 7.3.4 Overtemperature Protection

This device features internal temperature monitoring. If the temperature exceeds the threshold value, VTT and VTTREF are shut off. This is a non-latch protection.



**Figure 23. Typical Timing Diagram**

## 7.4 Device Functional Modes

### 7.4.1 Power State Control

The TPS51206 has two input pins, S3 and S5, to provide simple control of the power state. [Table 1](#) describes S3 and S5 terminal logic state and corresponding state of VTTREF and VTT outputs. VTT is turn-off and placed to high impedance (High-Z) state in S3. The VTT output is floated and does not sink or source current in this state. When both S5 and S3 pins are LOW, the power state is set to S4 and S5. In S4 and S5 state, all the outputs are turn-off and discharged to GND.

**Table 1. S3 and S5 Control Table**

STATE	S3	S5	VTTREF	VTT
S0	HI	HI	ON	ON
S3	LO	HI	ON	OFF(High-Z)
S4 and S5	LO	LO	OFF(Discharge)	OFF(Discharge)

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

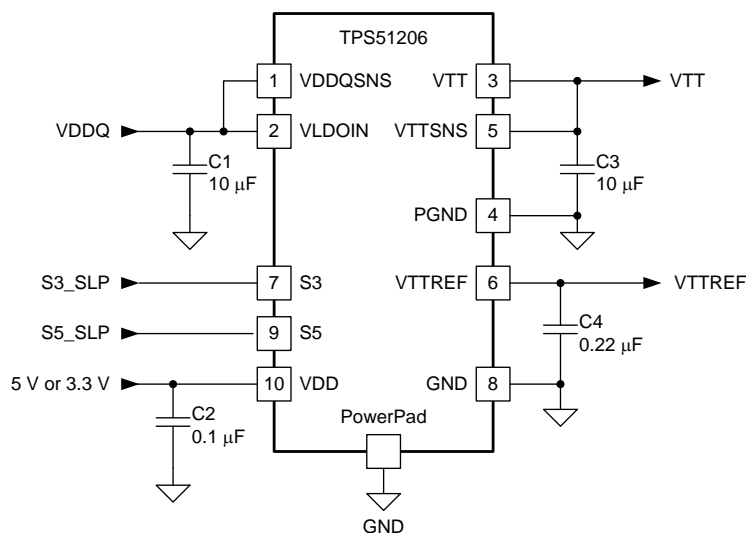
### 8.1 Application Information

The TPS51206 is typically used as a sink and source tracking termination regulator which converts a voltage from  $V_{TT}+0.4\text{ V}$  to 3.5 V

### 8.2 Typical Applications

#### 8.2.1 VLDOIN = VDDQ Configuration

Figure 24 shows an application diagram for a configuration where VLDOIN and VDDQ are connected.



Copyright © 2016, Texas Instruments Incorporated

**Figure 24. VLDOIN = VDDQ Configuration**

#### 8.2.1.1 Design Requirements

**Table 2. Design Parameters**

PARAMETER	EXAMPLE VALUE
Supply Voltage (VDD)	3.3 V or 5 V
VLDOIN = VDDQ	1.5 V
Output Current	±2 A

### 8.2.1.2 Detailed Design Procedure

Table 3. VLDOIN = VDDQ Configuration Components

REFERENCE DESIGNATOR	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C3	10 $\mu$ F, 6.3 V, X5R, 1608 (0603)	Taiyo Yuden	JMK107BJ106MA
C2	0.1 $\mu$ F, 6.3 V, X5R, 1005 (0402)	Taiyo Yuden	JWK105BJ104MP
C4	0.22 $\mu$ F, 6.3 V, X5R, 1005 (0402)	Taiyo Yuden	JMK105BJ224KV

#### 8.2.1.2.1 VDD Capacitor

Add a ceramic capacitor, with a value 0.1  $\mu$ F (or greater) and X5R grade (or better), placed close to the VDD terminal, to stabilize the bias supply voltage from any parasitic impedance from the power supply rail.

#### 8.2.1.2.2 VLDOIN Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10- $\mu$ F (or greater) and X5R grade (or better) ceramic capacitor to supply this transient charge.

#### 8.2.1.2.3 VTTREF Capacitor

Add a ceramic capacitor, with a value 0.22  $\mu$ F and X5R grade (or better), placed close to the VTTREF terminal for stable operation.

#### 8.2.1.2.4 VTT Capacitor

For stable operation, a 10- $\mu$ F (or greater) and X5R (or better) grade ceramic capacitor(s) need to be attached close to the VTT terminal. This capacitor is recommended to minimize any additional equivalent series resistance (ESR) and/or equivalent series inductance (ESL) of ground trace between the PGND terminal and the VTT capacitor(s).

#### 8.2.1.2.5 VTTSNS Connection

To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, the VTTSNS pin should be connected to the positive terminal of the VTT pin output capacitor(s) as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 m $\Omega$ . The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

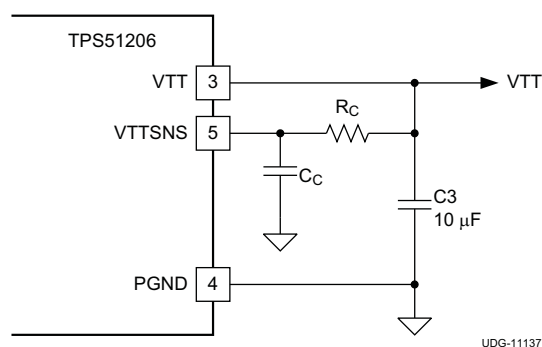
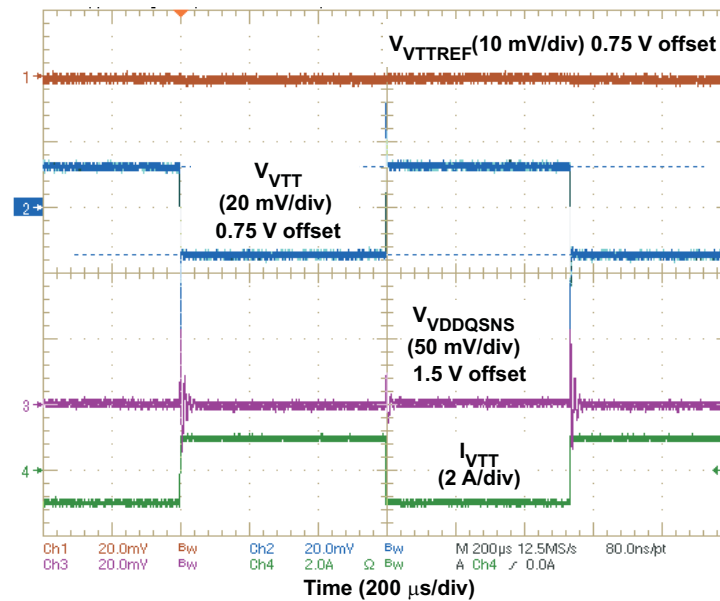


Figure 25. R-C Filter for VTTSNS

#### 8.2.1.2.6 VDDQSNS Connection

VDDQSNS is a reference input of the VTTREF and VTT. Trace should be routed away from noise-generating lines.

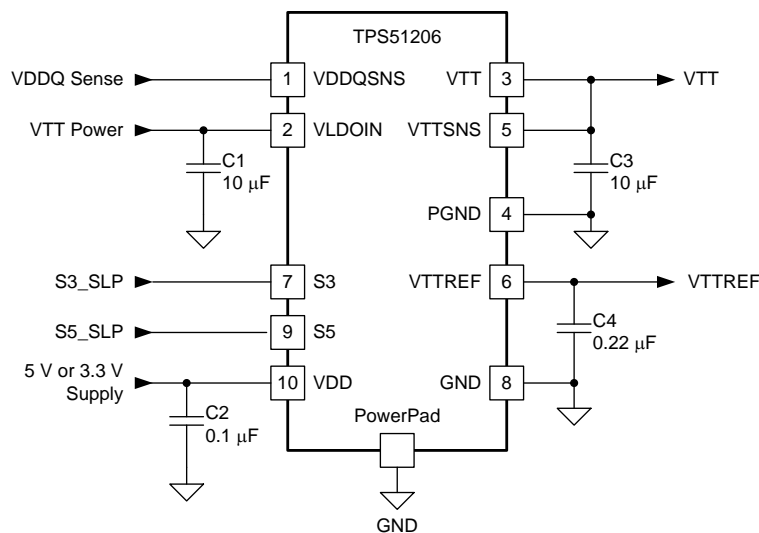
### 8.2.1.3 Application Curves



**Figure 26. VTT Load Transient Response (0.75 V)**

### 8.2.2 VLDOIN Separated from VDDQ Configuration

Figure 27 shows an application diagram for a configuration where VLDOIN and VDDQ are separated.



Copyright © 2016, Texas Instruments Incorporated

**Figure 27. VLDOIN Separated from VDDQ Configuration**

### 8.2.2.1 Design Requirements

**Table 4. Design Parameters**

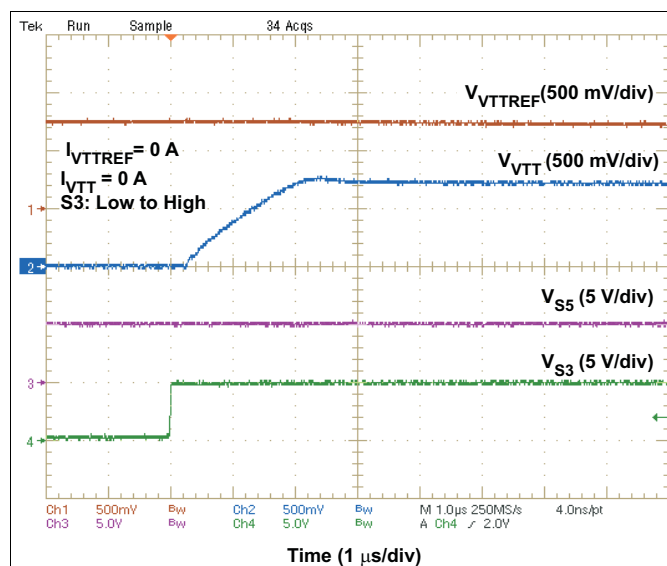
PARAMETER	EXAMPLE VALUE
Supply Voltage (VDD)	3.3 V or 5 V
VLDOIN = VDDQ	1.5 V
Output Current	±2 A

### 8.2.2.2 Detailed Design Procedure

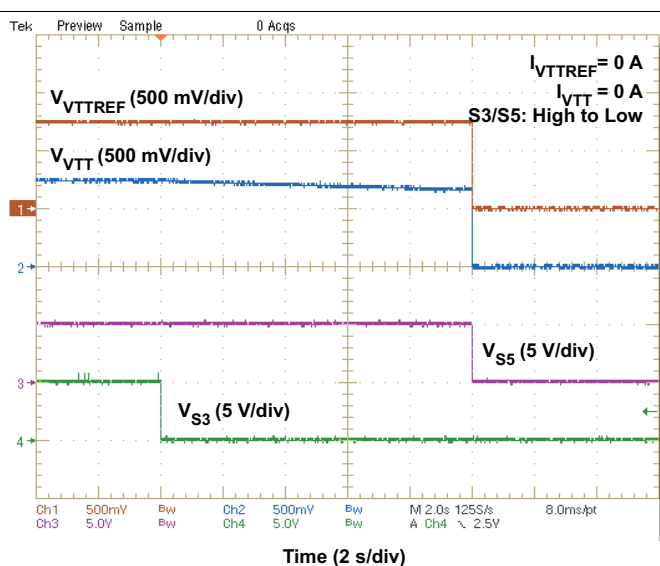
**Table 5. VLDOIN Separated from VDDQ Configuration Components**

REFERENCE DESIGNATOR	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C3	10 $\mu$ F, 6.3V, X5R, 1608 (0603)	Taiyo Yuden	JMK107BJ106MA
C2	0.1 $\mu$ F, 6.3V, X5R, 1005 (0402)	Taiyo Yuden	JWK105BJ104MP
C3	10 $\mu$ F, 6.3V, X5R, 1608 (0603)	Taiyo Yuden	JMK107BJ106MA
C4	0.22 $\mu$ F, 6.3V, X5R, 1005 (0402)	Taiyo Yuden	JMK105BJ224KV

### 8.2.2.3 Application Curves



**Figure 28. Start-Up Waveforms (S3: Low to High)**



**Figure 29. Shutdown Waveforms (S3 / S5: High to Low)**

## 9 Power Supply Recommendations

TPS51206 is designed for a sink / source double data rate (DDR) termination regulator with VTTREF buffered reference output. Supply input voltage (VDD) supports 3.3-V rail and 5-V rail; VLDOIN input voltage supports VTT+0.4 V to 3.5 V.

## 10 Layout

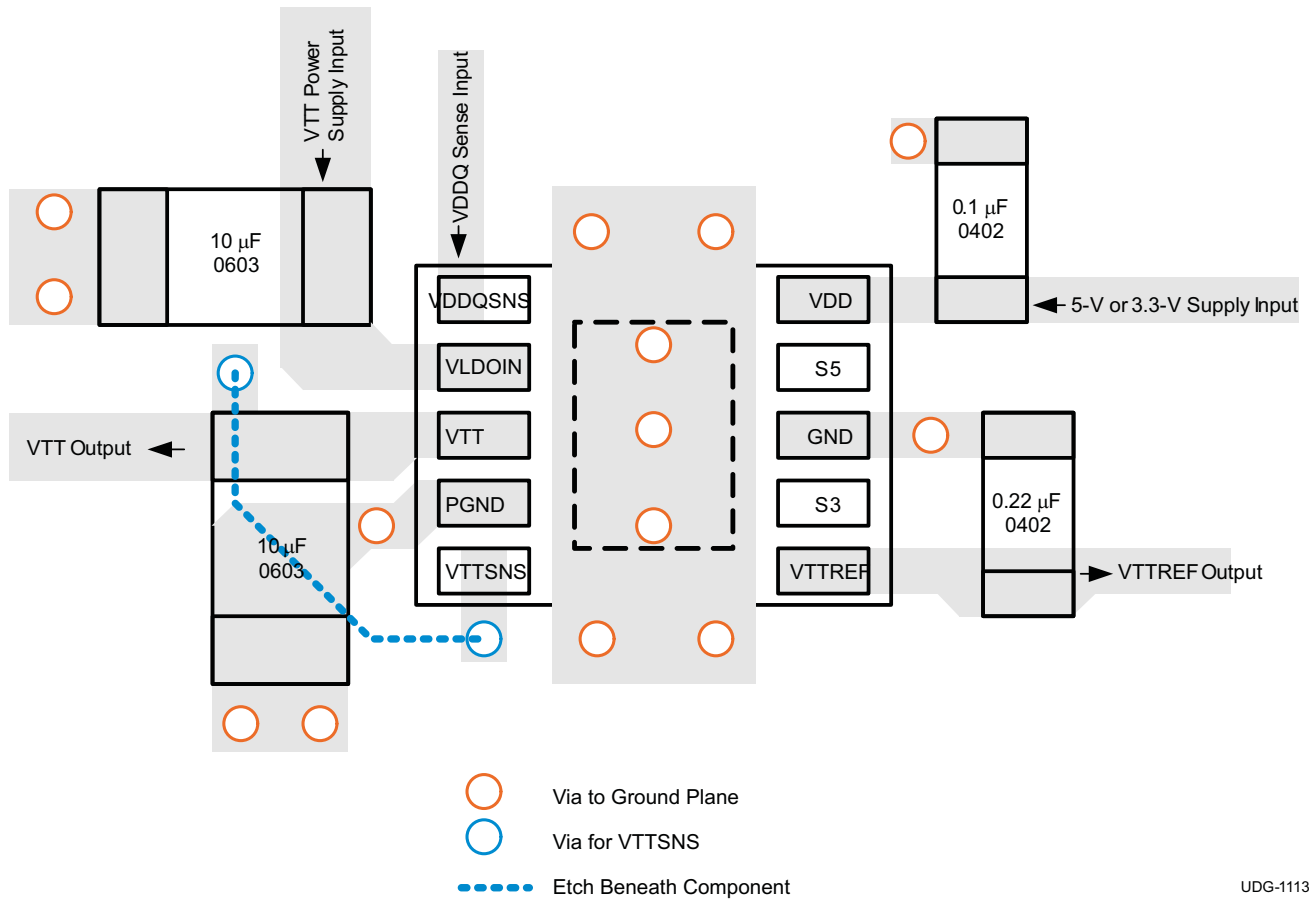
### 10.1 Layout Guidelines

Consider the following before beginning a TPS51206 layout design.

- The input bypass capacitor for VLDOIN should be placed as close as possible to the terminal with short and wide connections.
- The output capacitor for VTT should be placed close to the terminals (VTT and PGND) with short and wide connection in order to avoid additional ESR and/or ESL trace inductance.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current VTT power trace. In addition, VTTSNS trace should be routed away from high current trace, on the separate layer is recommended. This configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor(s) at that point. In addition, it is recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the VTT capacitor(s).
- The GND pin (and the negative node of the VTTREF output capacitor) and PGND pins (and the negative node of the VTT output capacitor) should be connected to the internal system ground planes (for better result, use at least two internal ground planes) with multiple vias. Use as many vias as possible to reduce the impedance between GND pin or PGND pin and the system ground plane.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package thermal pad. The wide traces of the component and the side copper connected to the thermal land pad help to dissipate heat. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder side ground plane(s) should also be used to help dissipation. Consult the [TPS51206-EVM User's Guide](#) for more detailed layout recommendations.



## 10.2 Layout Example



**Figure 30. PCB Layout Guideline**

UDG-11135

## 10.3 Thermal Considerations

Because the TPS51206 is a linear regulator, the VTT current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between  $V_{VLDOIN}$  and  $V_{VTT}$  times  $I_{VTT}$  (VTT current) current becomes the power dissipation as shown in Equation 1.

$$P_{DISS(src)} = (V_{VLDOIN} - V_{VTT}) \times I_{VTT(src)} \quad (1)$$

In this case, if the VLDOIN pin is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation can be calculated by Equation 2.

$$P_{DISS(snk)} = V_{VTT} \times I_{VTT(snk)} \quad (2)$$

Maximum power dissipation allowed by the package is calculated by Equation 3.

$$P_{PKG} = \frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}}$$

where

- $T_{J(max)}$  is 125°C
  - $T_{A(max)}$  is the maximum ambient temperature in the system
  - $\theta_{JA}$  is the thermal resistance from junction to ambient
- (3)

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

#### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 11.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51206DSQR	ACTIVE	WSO	DSQ	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1206	<a href="#">Samples</a>
TPS51206DSQT	ACTIVE	WSO	DSQ	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1206	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

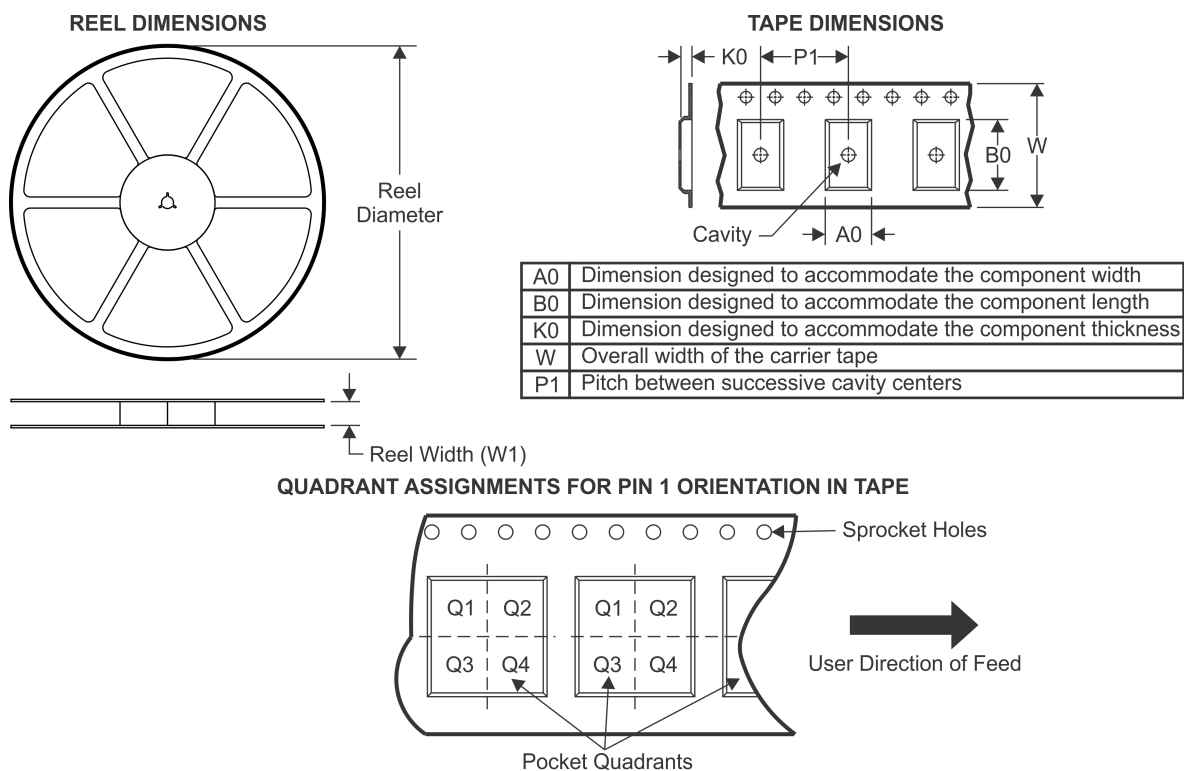
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51206DSQR	WSO	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51206DSQR	WSO	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51206DSQT	WSO	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51206DSQT	WSO	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS

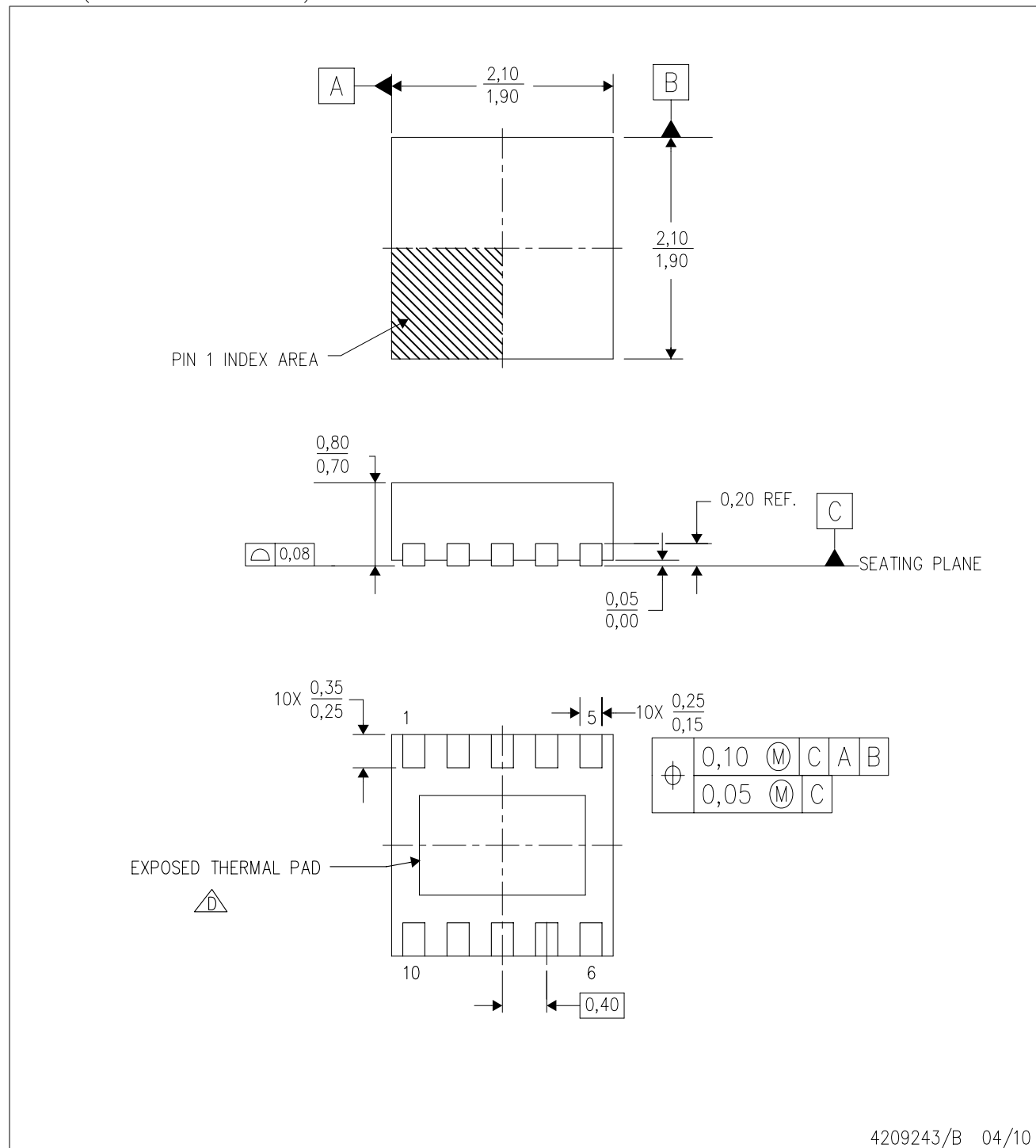


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51206DSQR	WSN	DSQ	10	3000	210.0	185.0	35.0
TPS51206DSQR	WSN	DSQ	10	3000	210.0	185.0	35.0
TPS51206DSQT	WSN	DSQ	10	250	210.0	185.0	35.0
TPS51206DSQT	WSN	DSQ	10	250	210.0	185.0	35.0

DSQ (S-PWSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4209243/B 04/10

## NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.



D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

DSQ (R-PWSON-N10)

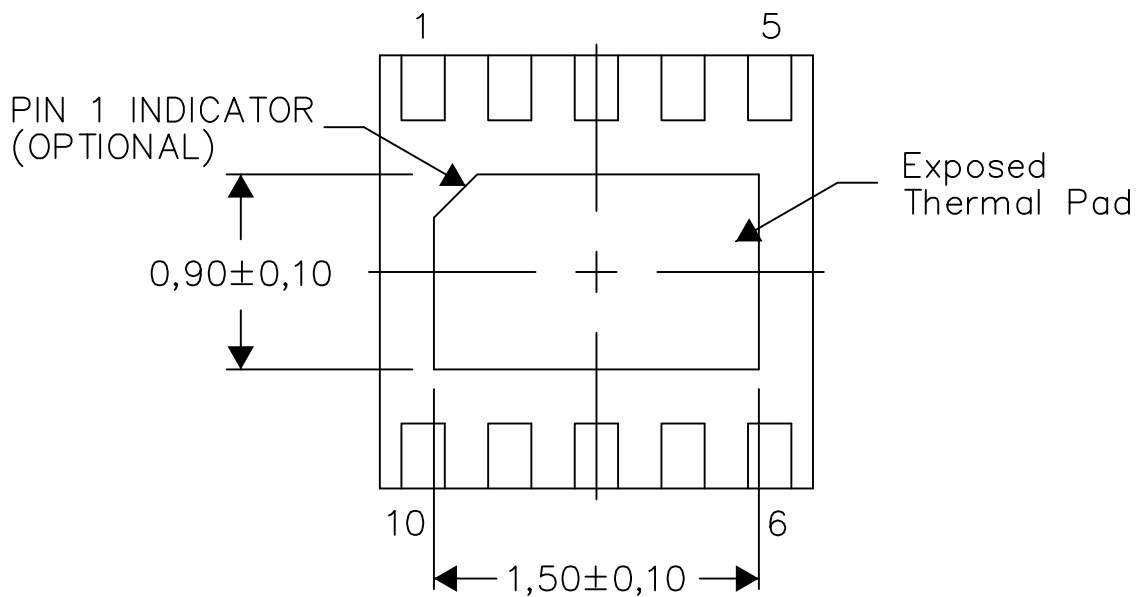
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

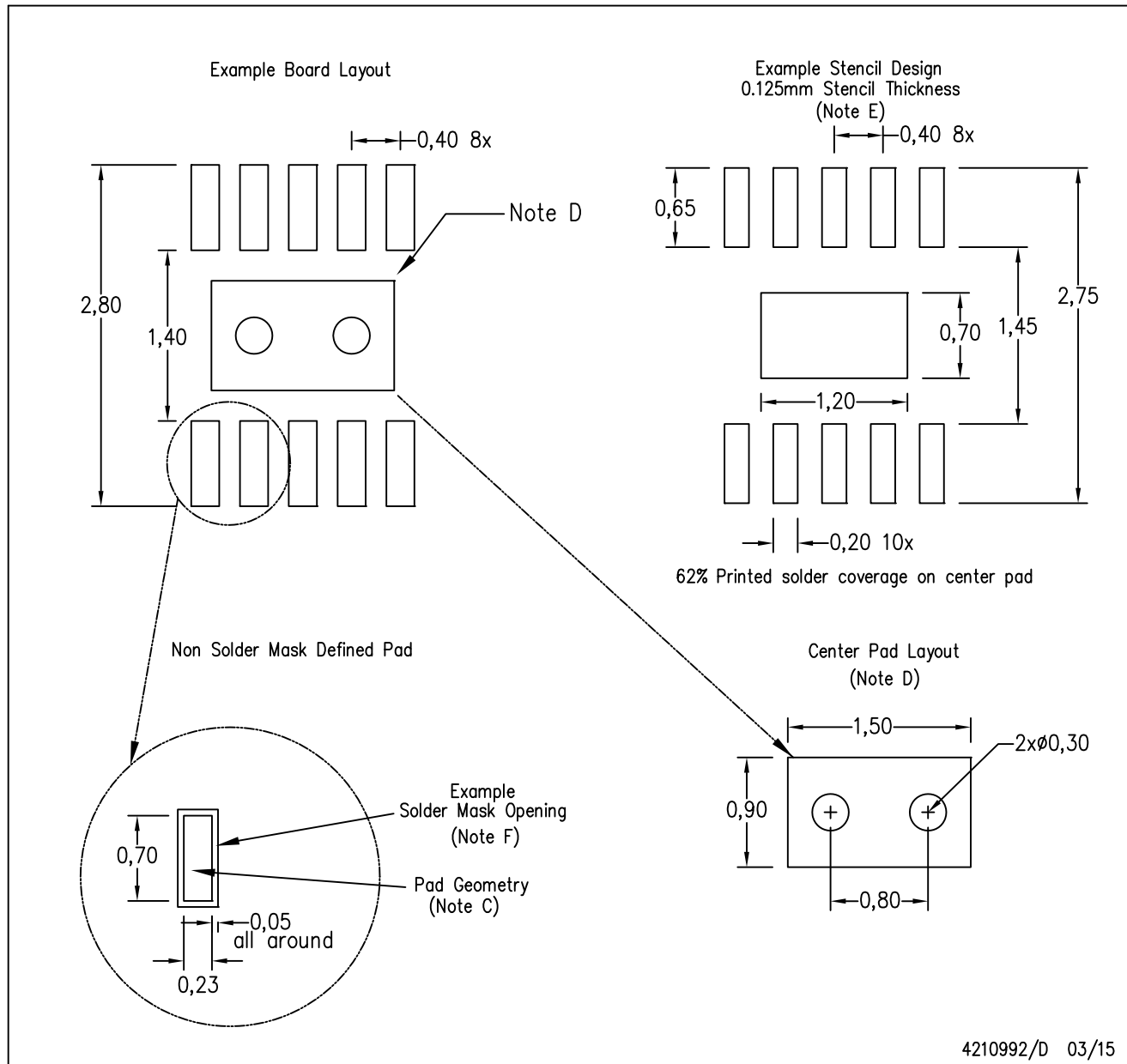
4210993/E 06/15

NOTES: A. All linear dimensions are in millimeters



DSQ (R-PWSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)