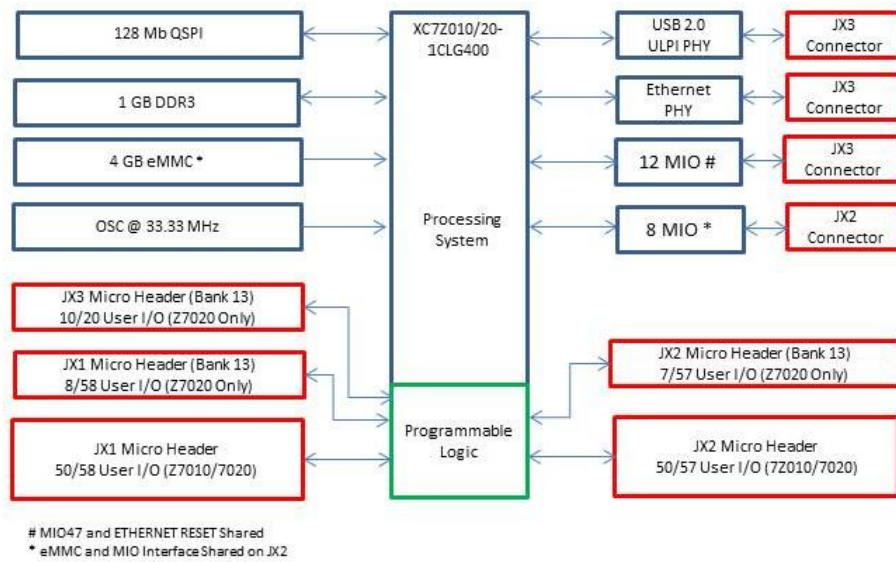


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## Zynq PS MIO - Bank 500

U11E  
Zynq 7010/7020 SOC CLG400

### BANK 500

PS\_MIO0\_500  
PS\_MIO1\_500  
PS\_MIO2\_500  
PS\_MIO3\_500  
PS\_MIO4\_500  
PS\_MIO5\_500  
PS\_MIO6\_500  
PS\_MIO7\_500  
PS\_MIO8\_500  
PS\_MIO9\_500  
PS\_MIO10\_500  
PS\_MIO11\_500  
PS\_MIO12\_500  
PS\_MIO13\_500  
PS\_MIO14\_500  
PS\_MIO15\_500

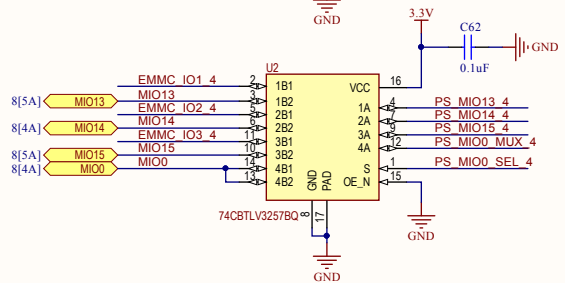
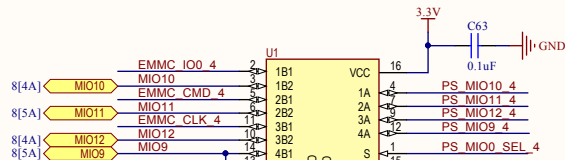
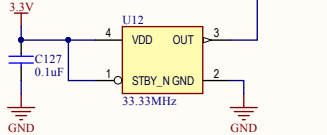
PS\_MIO0\_4  
QSPI\_1\_CS#\_4  
QSPI\_1\_DQ0\_4  
QSPI\_1\_DQ1\_4  
QSPI\_1\_DQ2\_4  
QSPI\_1\_DQ3\_4  
QSPI\_1\_CLK\_4  
PS\_MIO7  
PS\_MIO8\_4  
PS\_MIO9\_4  
PS\_MIO10\_4  
PS\_MIO11\_4  
PS\_MIO12\_4  
PS\_MIO13\_4  
PS\_MIO14\_4  
PS\_MIO15\_4

PS\_POR\_B\_500

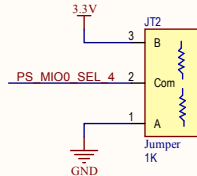
PS\_CLK\_500

PG\_MODULE 11[5B], 5[1C], 8[4A]

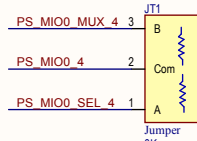
PS\_CLK\_4



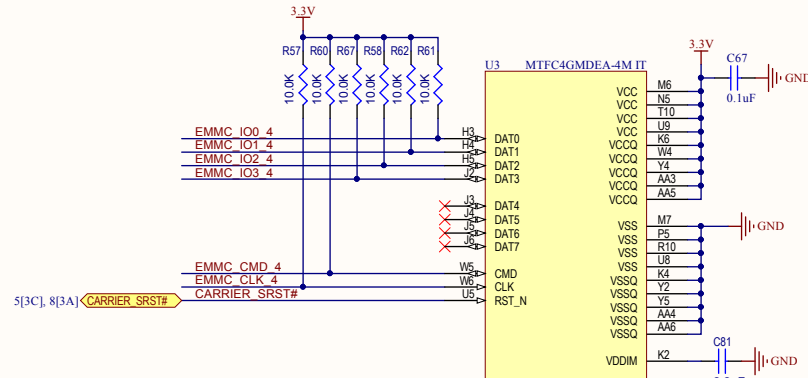
MUX SEL: Default - eMMC



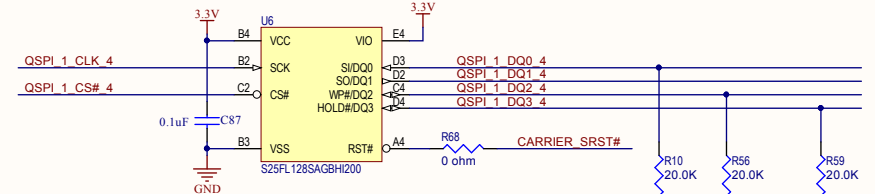
PMOD / MUX SEL: Default - MUX SEL



## Embedded eMMC: 2GB, 4GB, 8GB

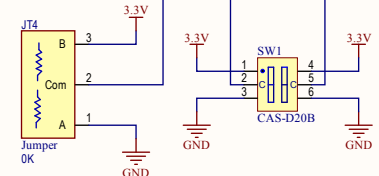


## QSPI



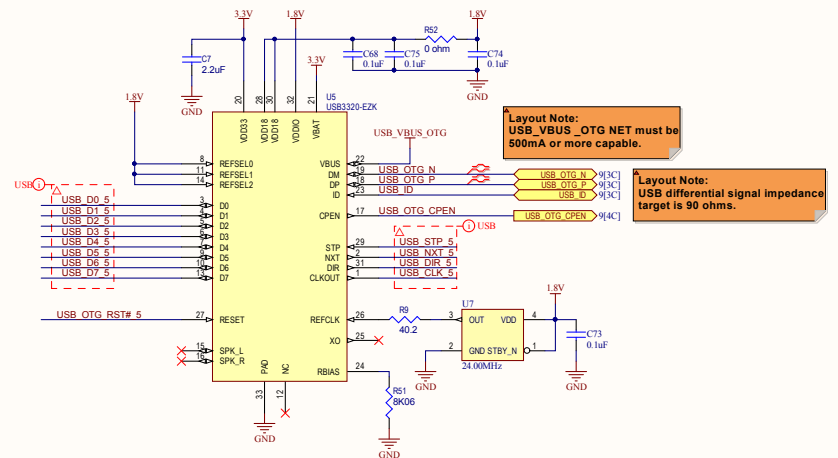
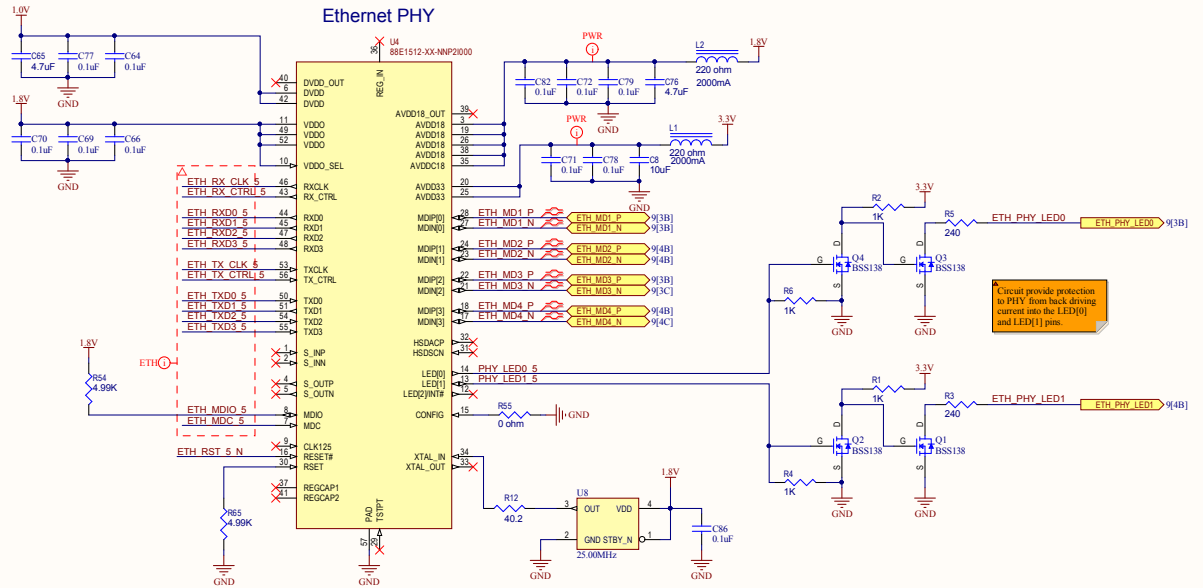
## Boot Mode Select

BOOT MODE	JT4	SW1 (1-3)	SW1 (4-6)
QSPI	X	LOW (2-3)	HIGH (4-5)
SD CARD	X	HIGH (1-2)	HIGH (4-5)
JTAG	X	LOW (2-3)	LOW (5-6)
IND JTAG	HIGH (2-3)	LOW (2-3)	LOW (5-6)
CASCADE JTAG	LOW (1-2)	LOW (2-3)	LOW (5-6)



CASCADE JTAG - DEFAULT MODE

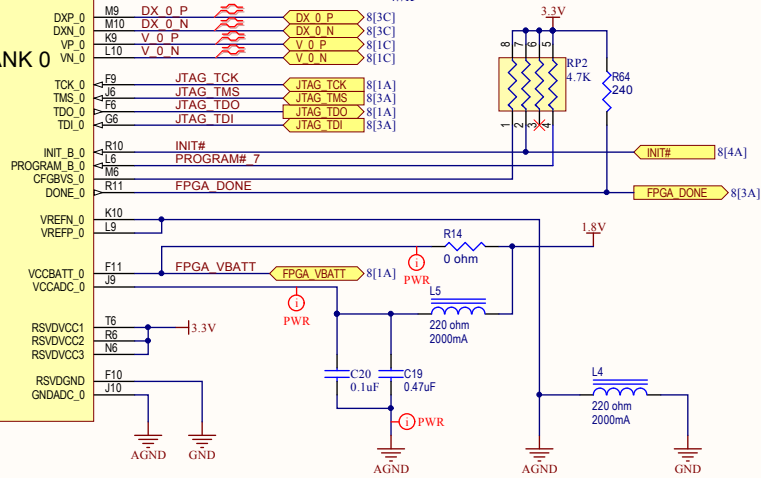
U11F  
Zynq 7010/7020 SOC CL.G400





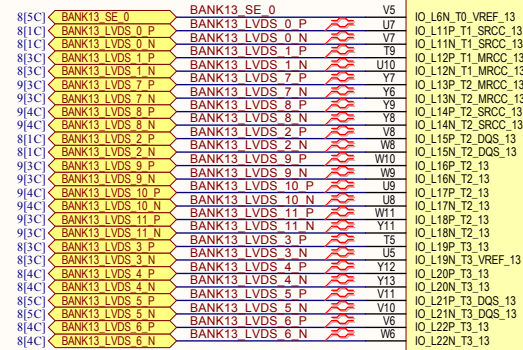
U11A  
Zynq 7010/7020 SOC CLG400

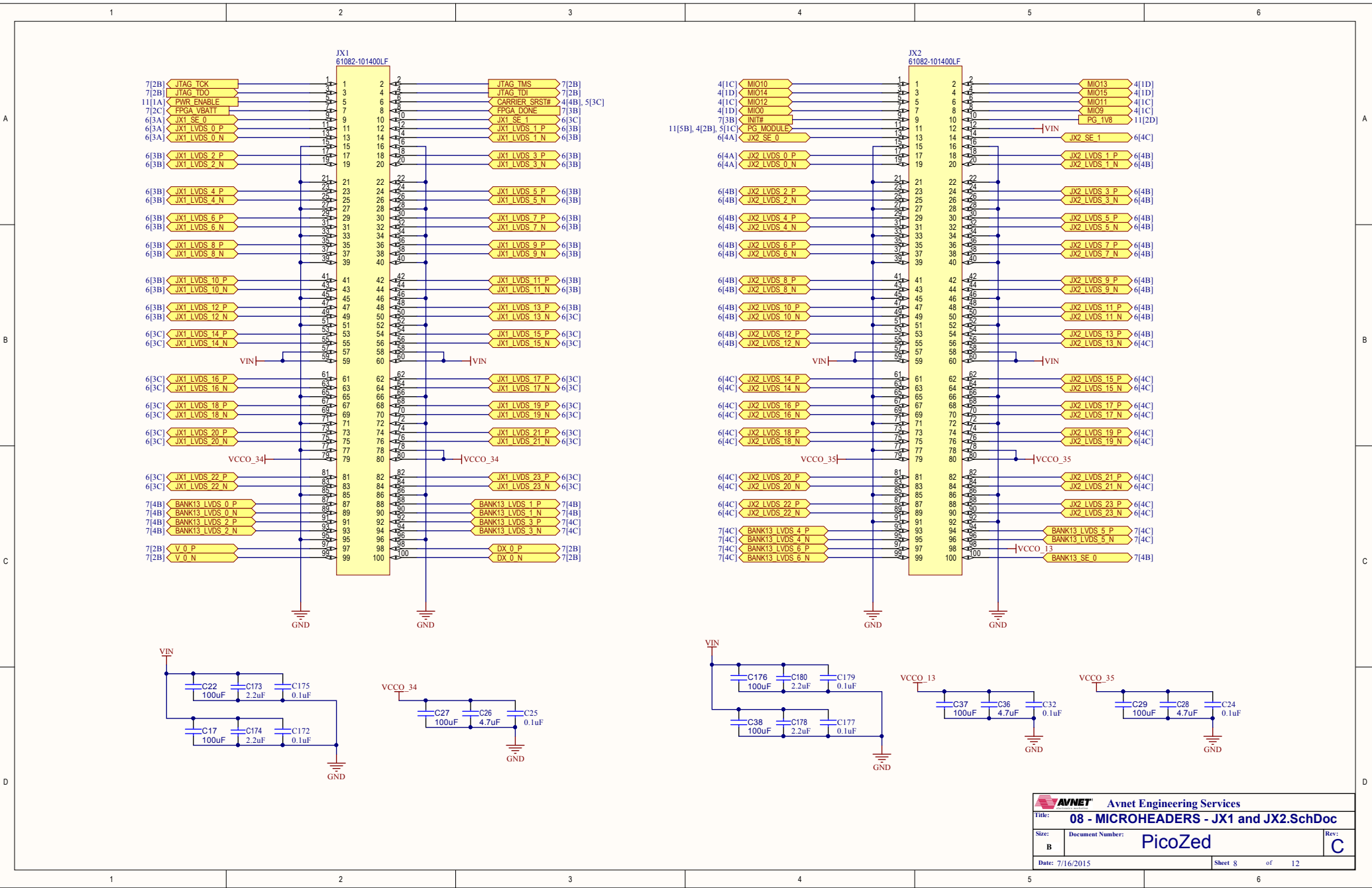
## BANK 0



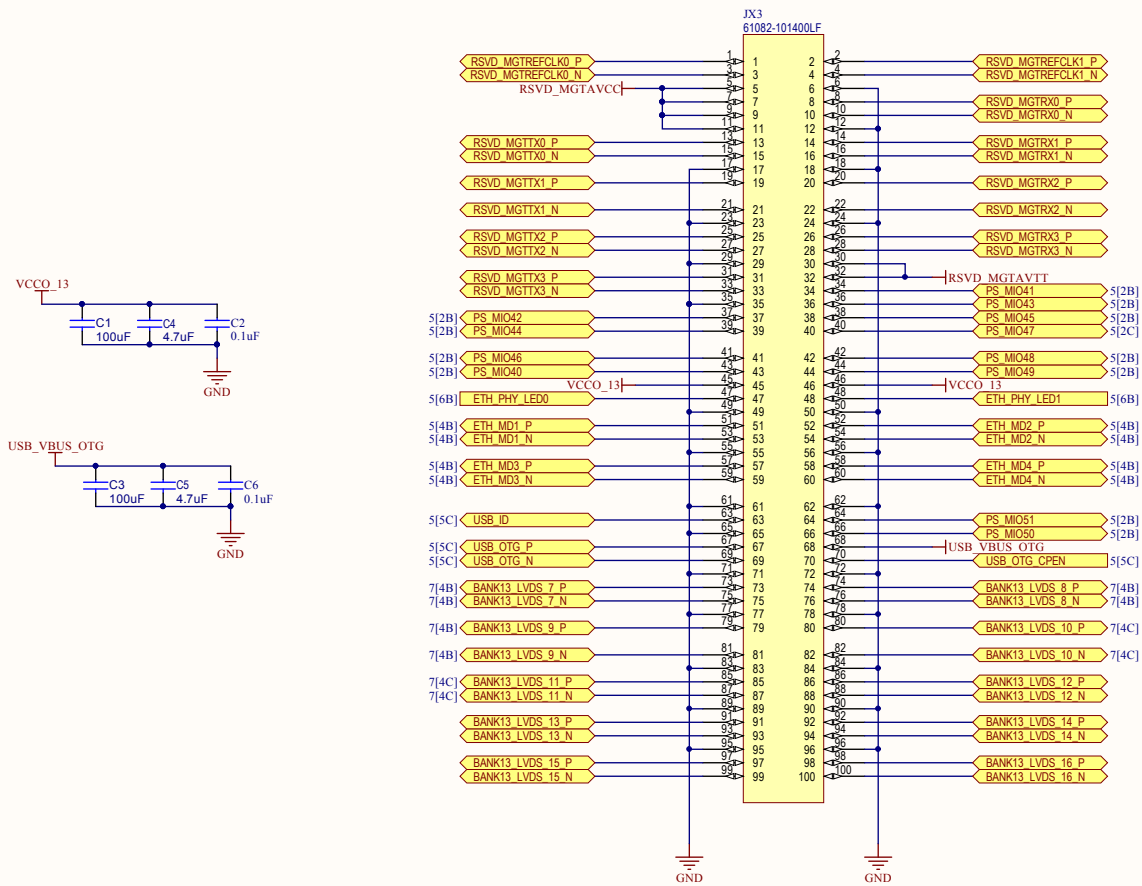
U11B  
Zynq 7010/7020 SOC CLG400

## BANK 13 (Z7020 Only)









\* All RSVD\_MGT\* signals are RESERVED for devices with MGTs.

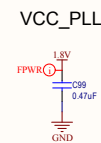
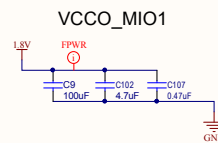
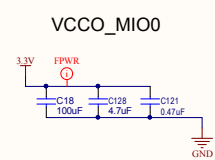
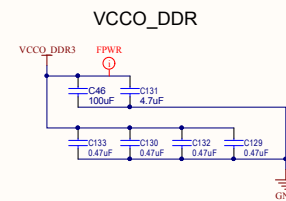
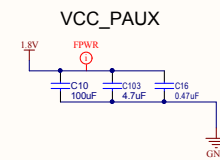
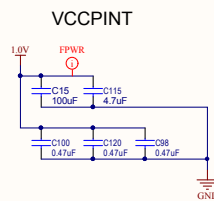
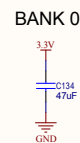
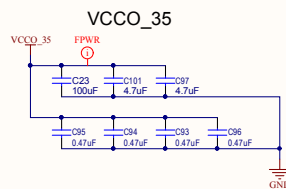
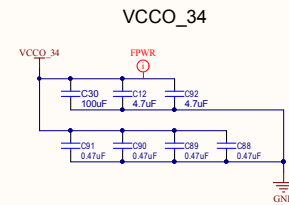
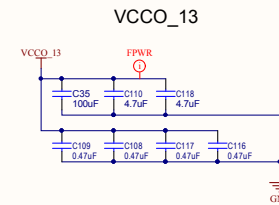
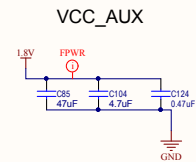
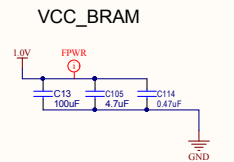
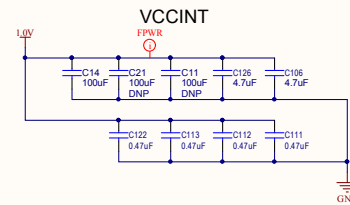
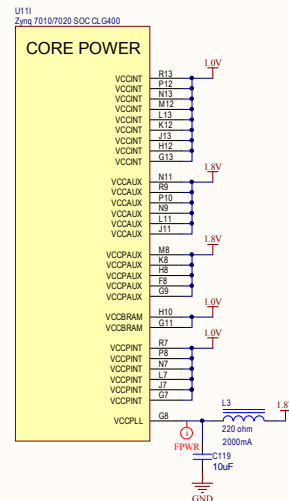
#### \* ZYNQ MIO POTENTIAL MAPPING OPTIONS:

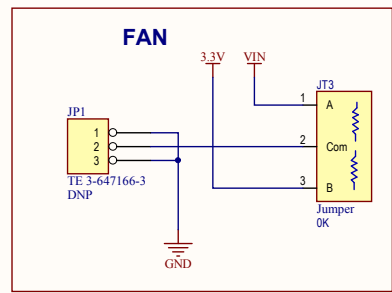
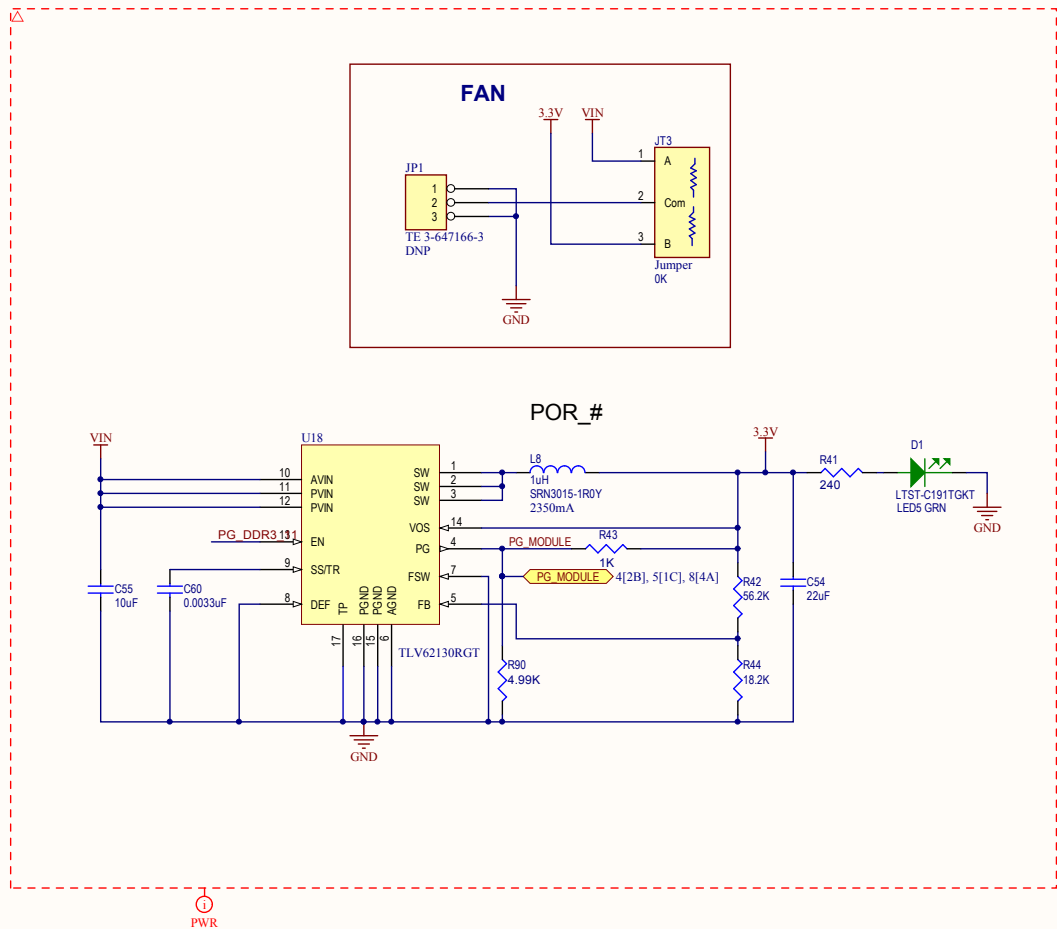
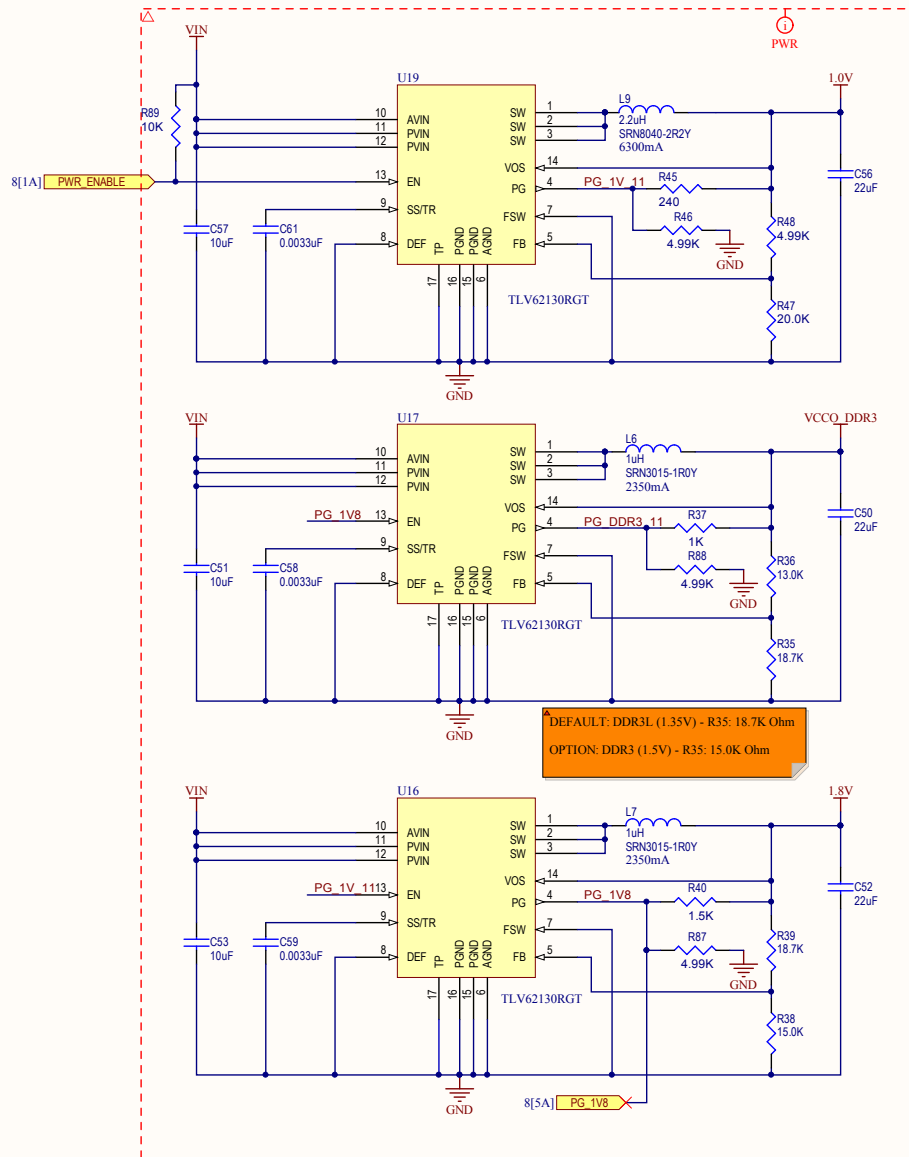
SDIO INTERFACE  
PS\_MIO40 - SD\_CLK through a 40.2-ohm RES  
PS\_MIO41 - SD\_CMD  
PS\_MIO42 - SD\_D0  
PS\_MIO43 - SD\_D1  
PS\_MIO44 - SD\_D2  
PS\_MIO45 - SD\_D3  
PS\_MIO46 - SD\_CD

UART INTERFACE  
PS\_MIO48 - UART\_RXD (Tie to the TXD pin of a UART)  
PS\_MIO49 - UART\_TXD (Tie to the RXD pin of a UART)

USB INTERFACE  
PS\_MIO40 - DATA  
PS\_MIO41 - DIR  
PS\_MIO42 - STP  
PS\_MIO43 - NXT  
PS\_MIO44 - DATA  
PS\_MIO45 - DATA  
PS\_MIO46 - DATA  
PS\_MIO47 - DATA  
PS\_MIO48 - CK  
PS\_MIO49 - DATA  
PS\_MIO50 - DATA

\* BANK13\_LVDS\_12\_P/N thru BANK13\_LVDS\_16\_P/N is reserved for larger density BANK13





Revision Notes:

- PicoZed Revision B1:
- 1) Multiplexed JX2 MIO signals with EMMC
  - 2) Removed Push Button Footprint
  - 3) Incorporated ETHERNET RESET circuit
  - 4) Added bulk cap to AVDD18
  - 5) Added GND Testpoints
- PicoZed Revision B2:
- 1) Updated BOOT MODE table
- PicoZed Revision C:
- 1) Updated Block Diagram
  - 2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
  - 3) Added RC time constant to ETHERNET RESET
  - 4) DDR3L / DDR3 Option Added
  - 5) Modified resistor divider value on PG\_1V8
  - 6) Changed DDR3 Termination Regulator VLDOIN from 1.8V to 3.3V
- PicoZed Revision C (Errata):
- 1) R71: Changed to 4.99K
  - 2) R182: Changed to 0.1uF

Mechanicals:

PCB  
Z7PZ-Z70x0-PCB-C

