

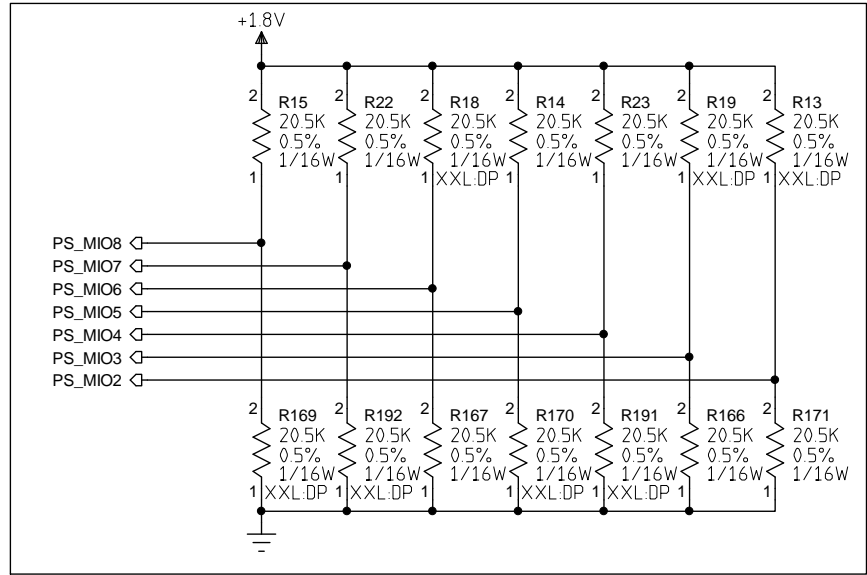


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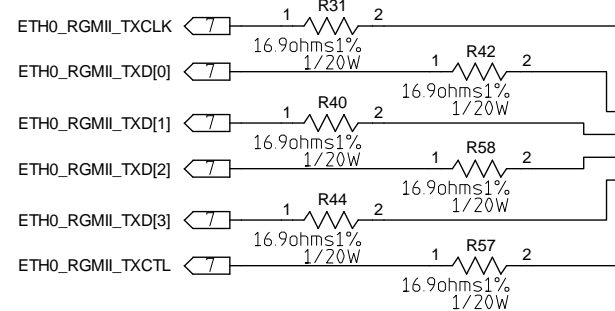
PS BOOTSTRAP
Ch. 30 of the TRM Details the Bootstrap Options
vmodel[0]=MIO[8:7] vmodel[0] indicates voltage on MIO_0 vmodel[1] indicates voltage on MIO_1 1=1.8V 0=2.5V/3.3V
model[4:0]=MIO[6:2] model[4] indicates PLL. 0=PLL Used (selected), 1=PLL Bypassed model[0] indicates JTAG mode. 0=cascaded(selected), 1=independent model[3:1] indicates boot mode. 000 Cascaded JTAG 001 NOR 010 NAND(8 bit) 011 Reserved 100 QSPI 101 Reserved 110 SD card boot <- selected 111 Reserved



SDIO Port Expander  
used for level translation

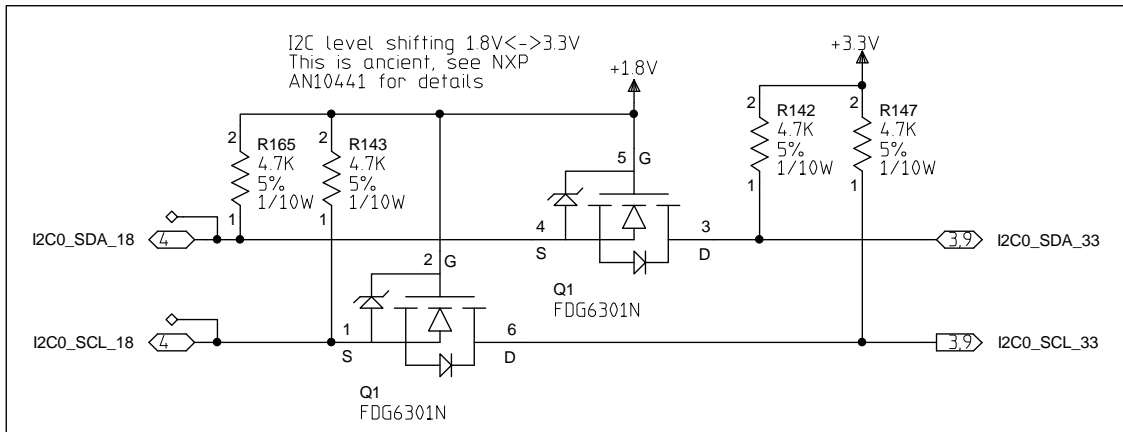
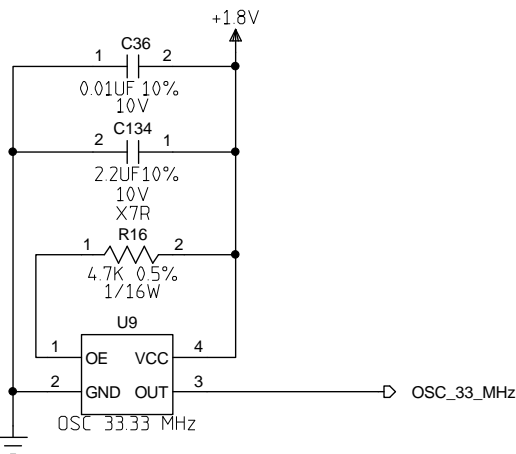
MIO[6:0] are used as configuration pins at boot time and should not be used for non-boot purposes.

MIOs 7/8 are output-only inputs read @ boot for MIO voltage select

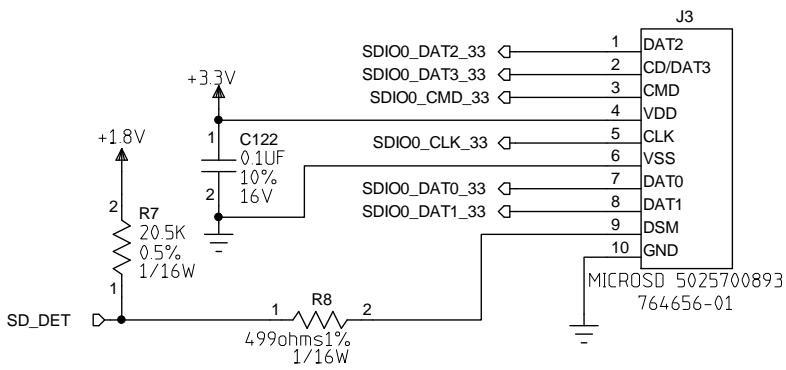


1/2 VccMIO1 for use with RGMII (UG865 p10)

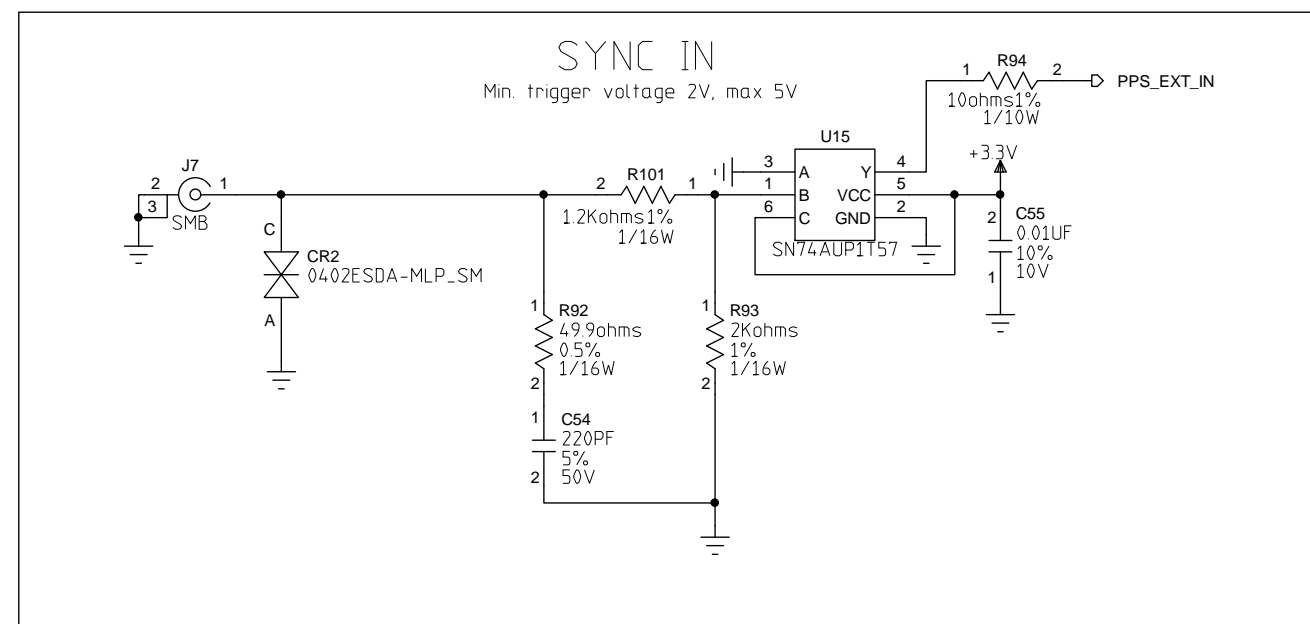
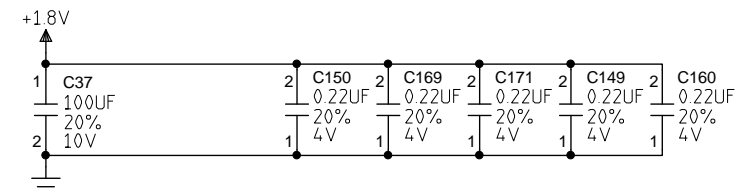
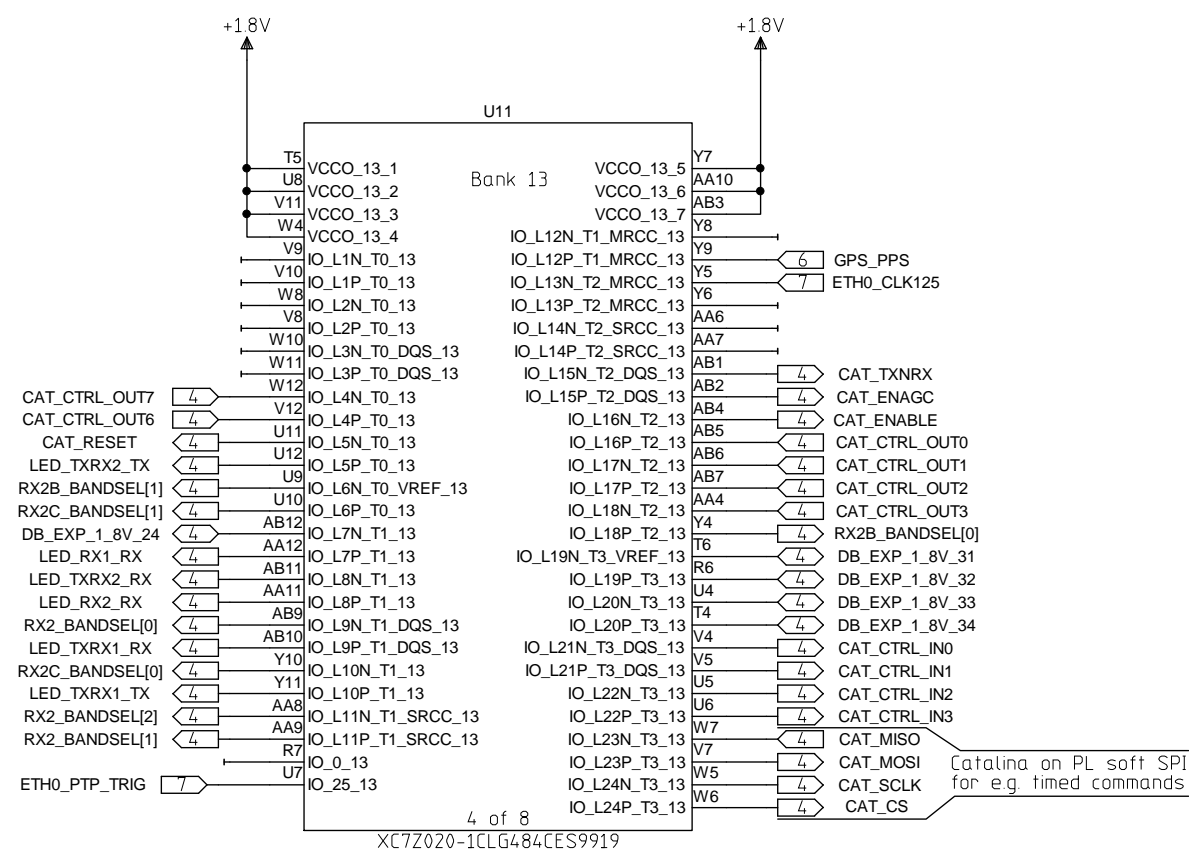
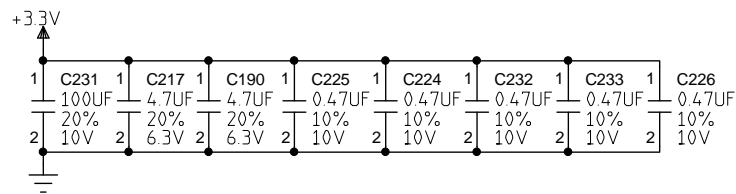
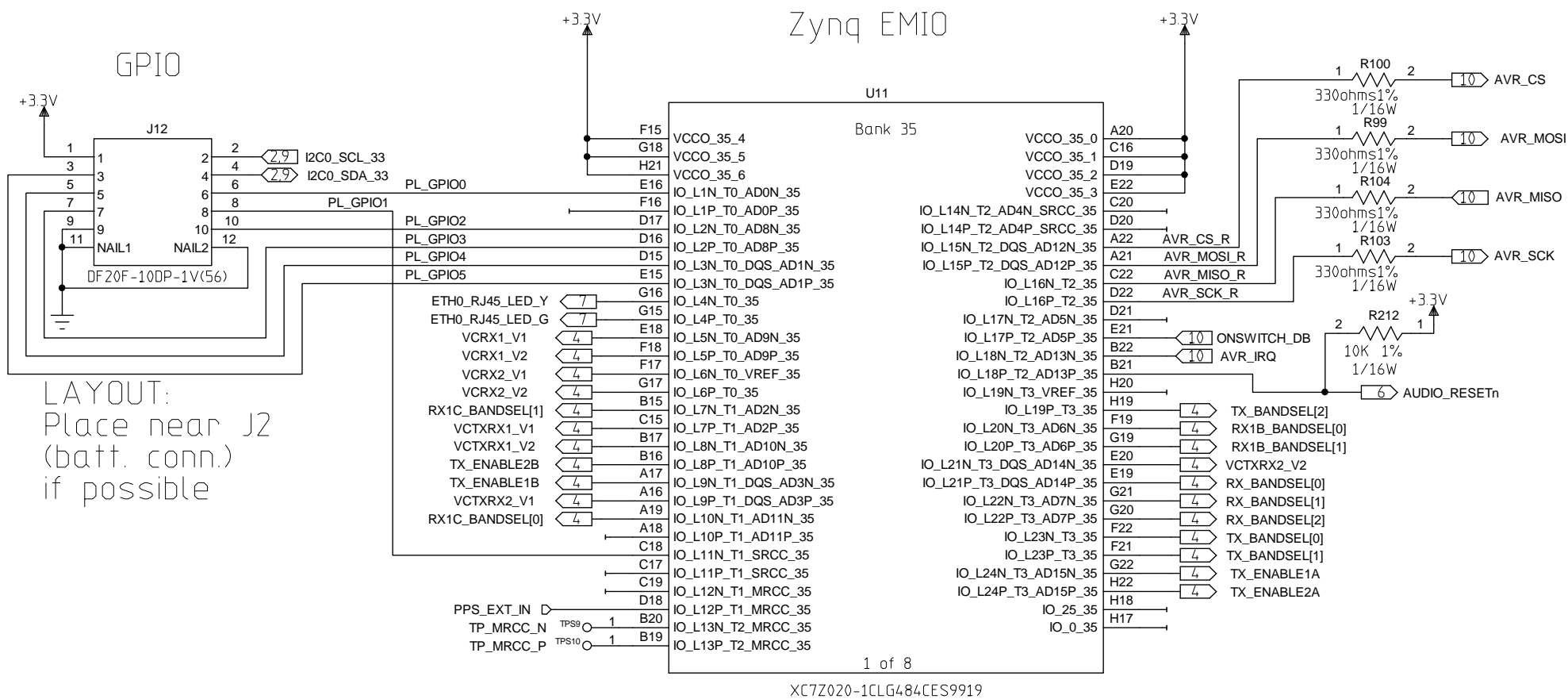
### PROCESSOR OSCILLATOR (33MHz)



### SDIO MicroSD slot



ZYNQ MIO				
E300				
SIZE	CODE IDENT NO.	DRAWING NO	REV	
C	7U296	154350D-01	1	
SCALE: NONE		SHEET 02 OF 13		



E300 EMIO BANK 35/BANK 13				
E300				
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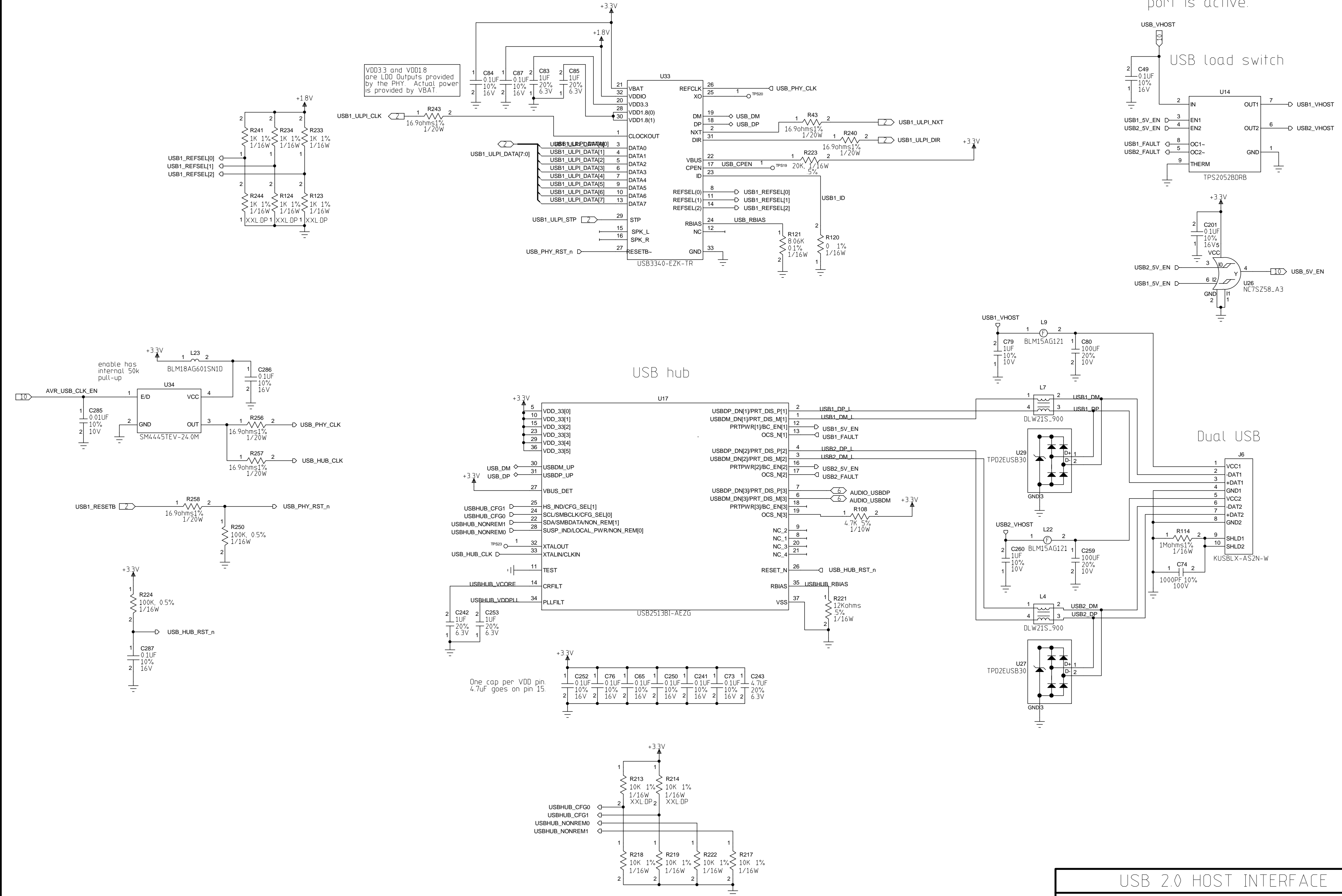
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154350D-01

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USB 2.0 HOST INTERFACE

E300

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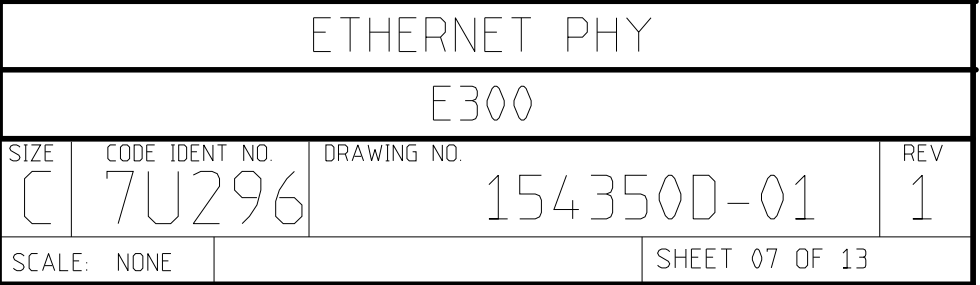
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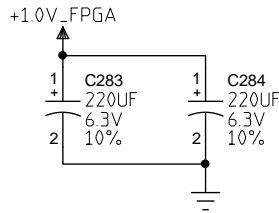
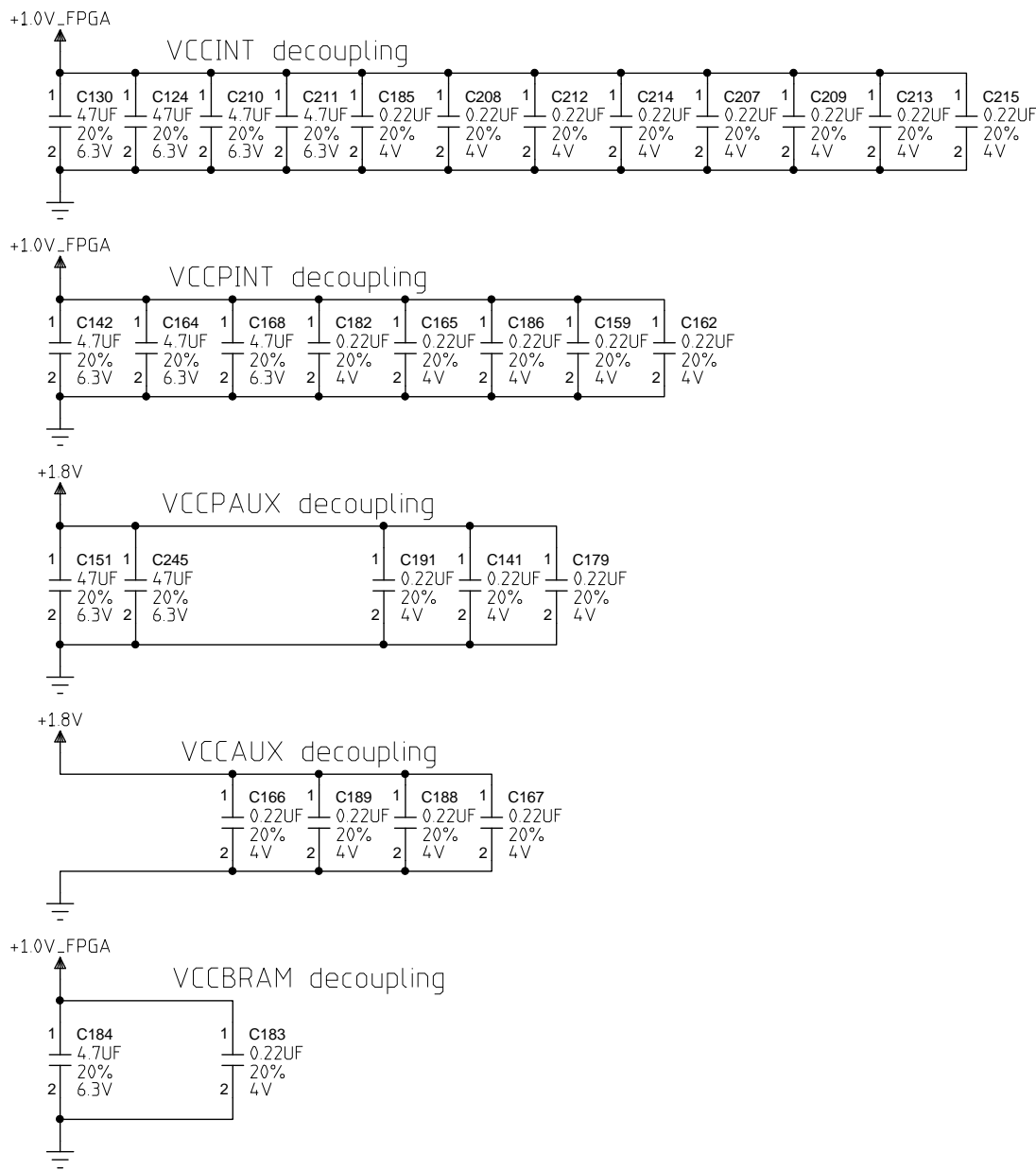
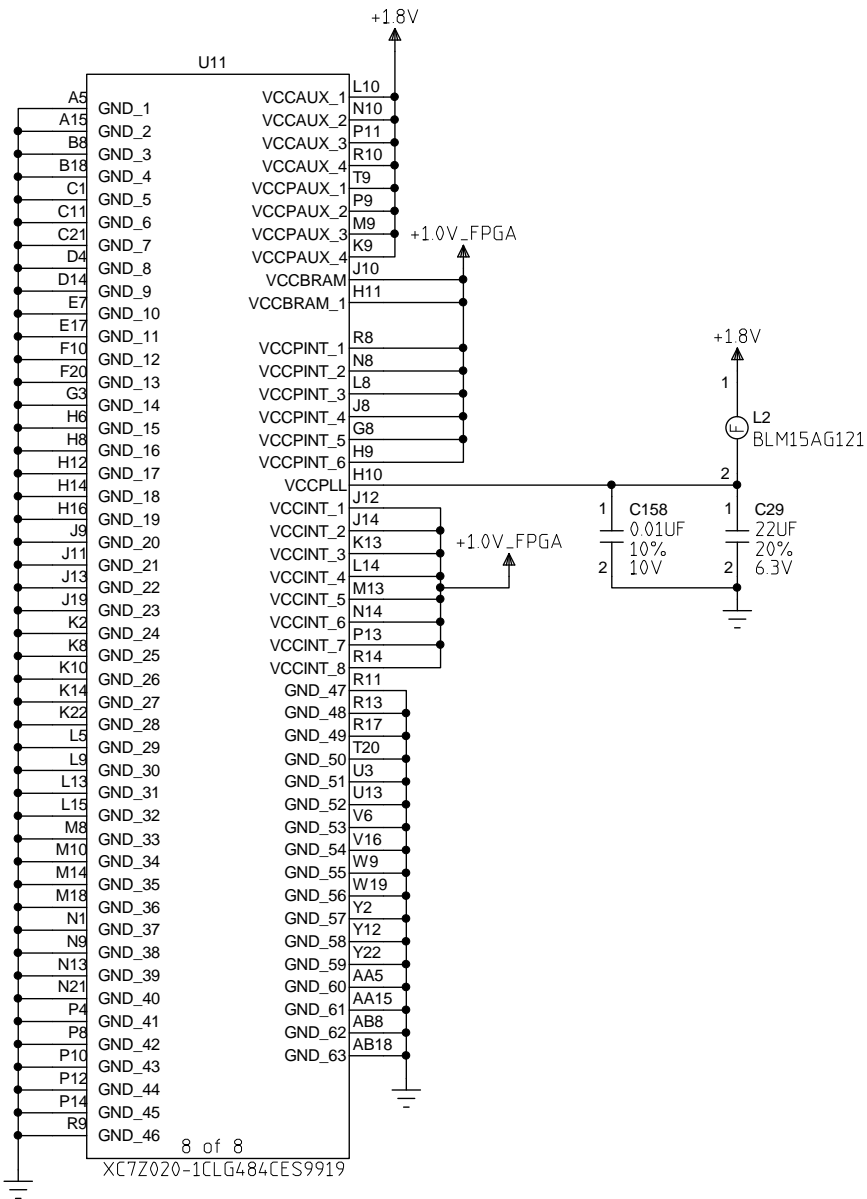
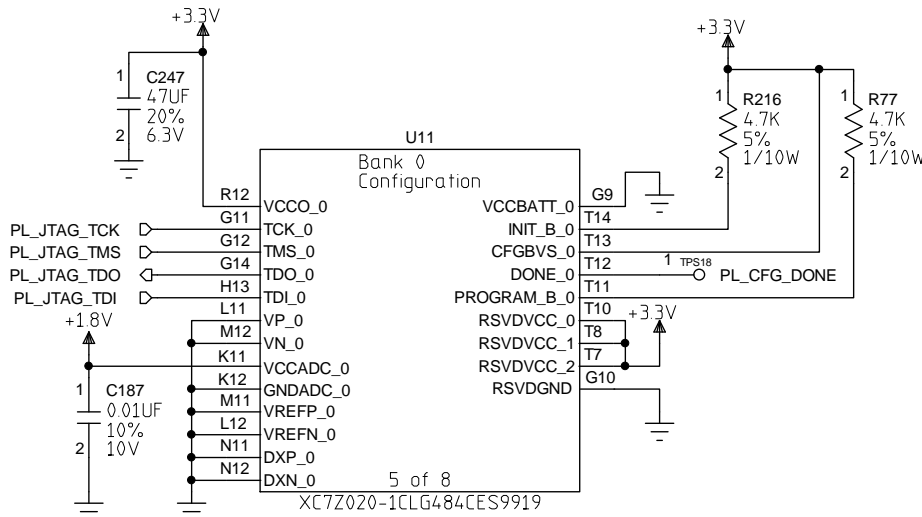
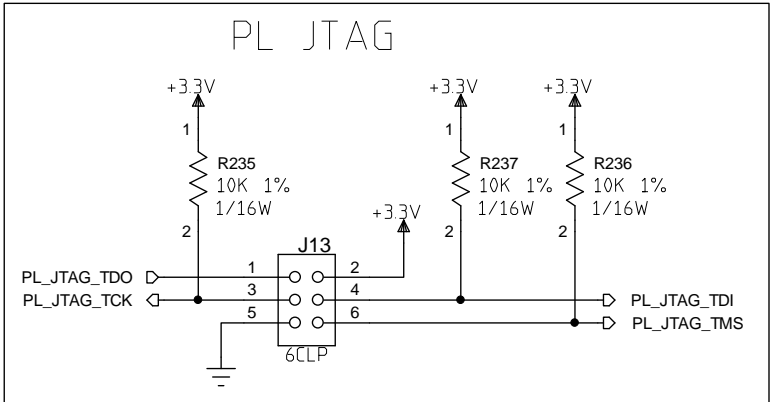
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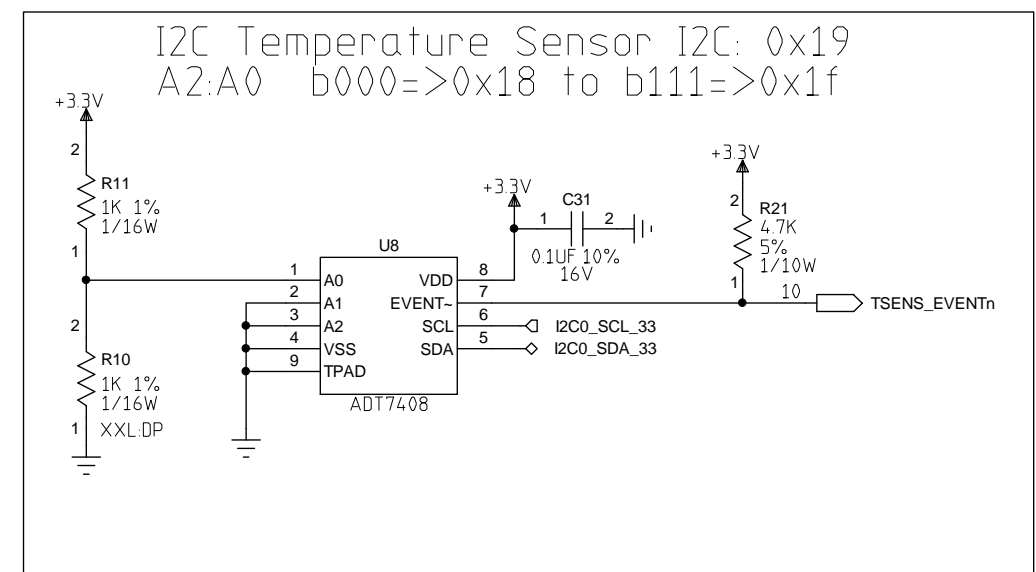


ZYNQ CONFIG AND POWER				
E300				
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I2C addresses:
AK8975 compass: 0x0C
MPU-9150: 0x69 (with AD0 tied high)
BMP085: 0x77
```

4

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3

2

1

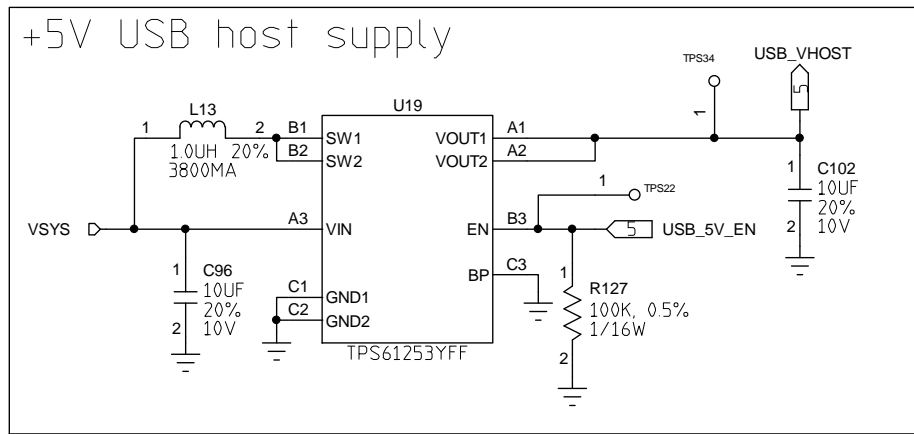
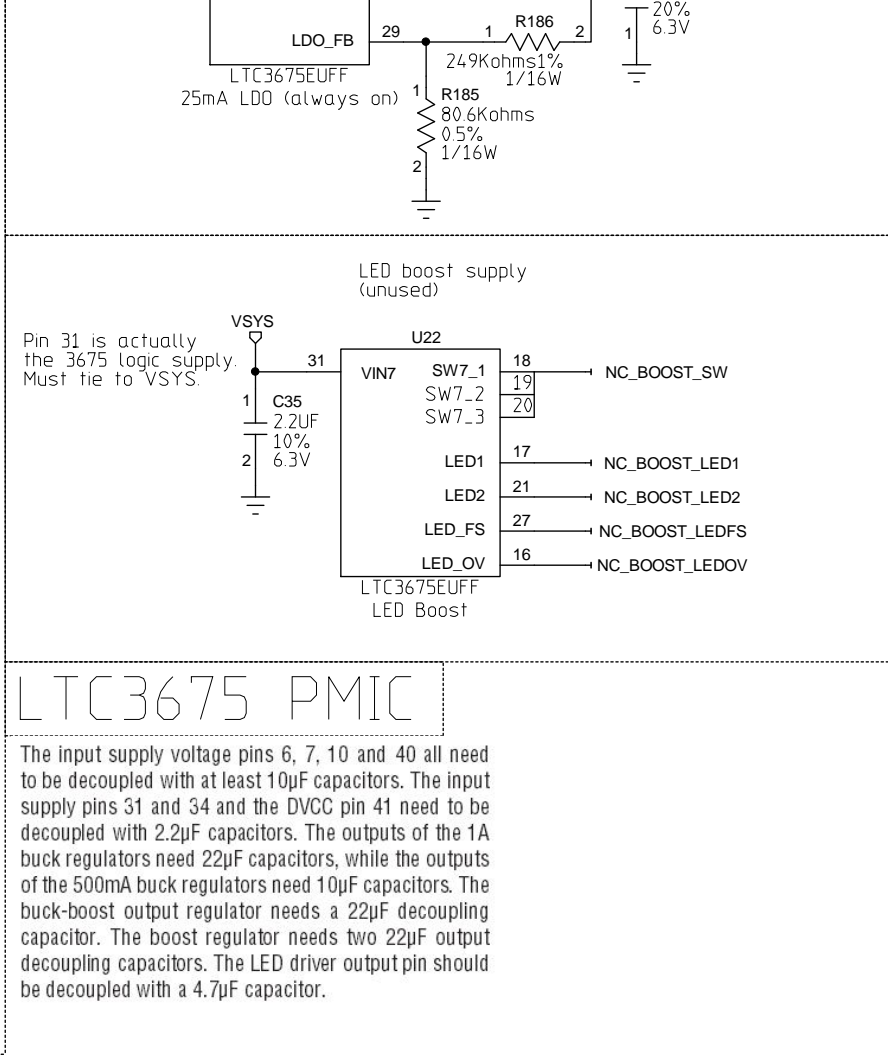
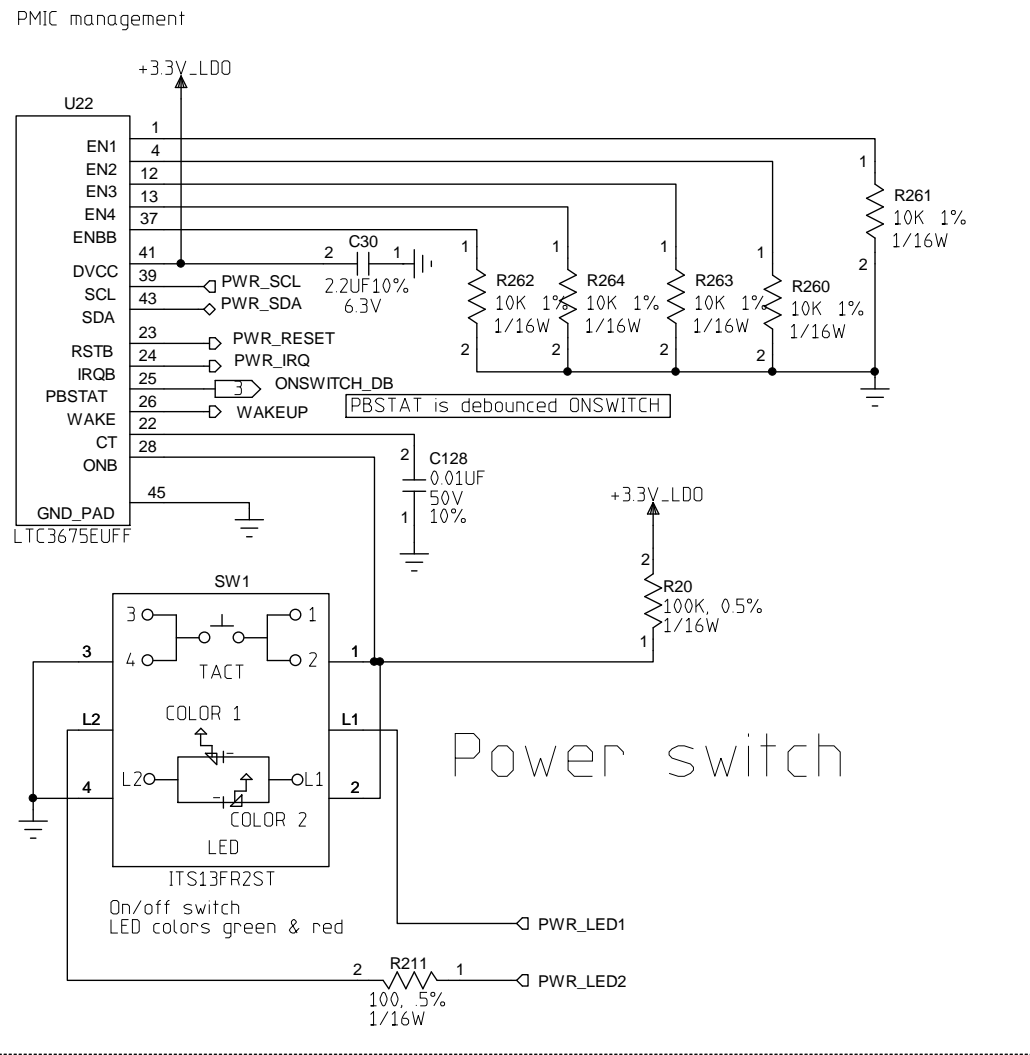
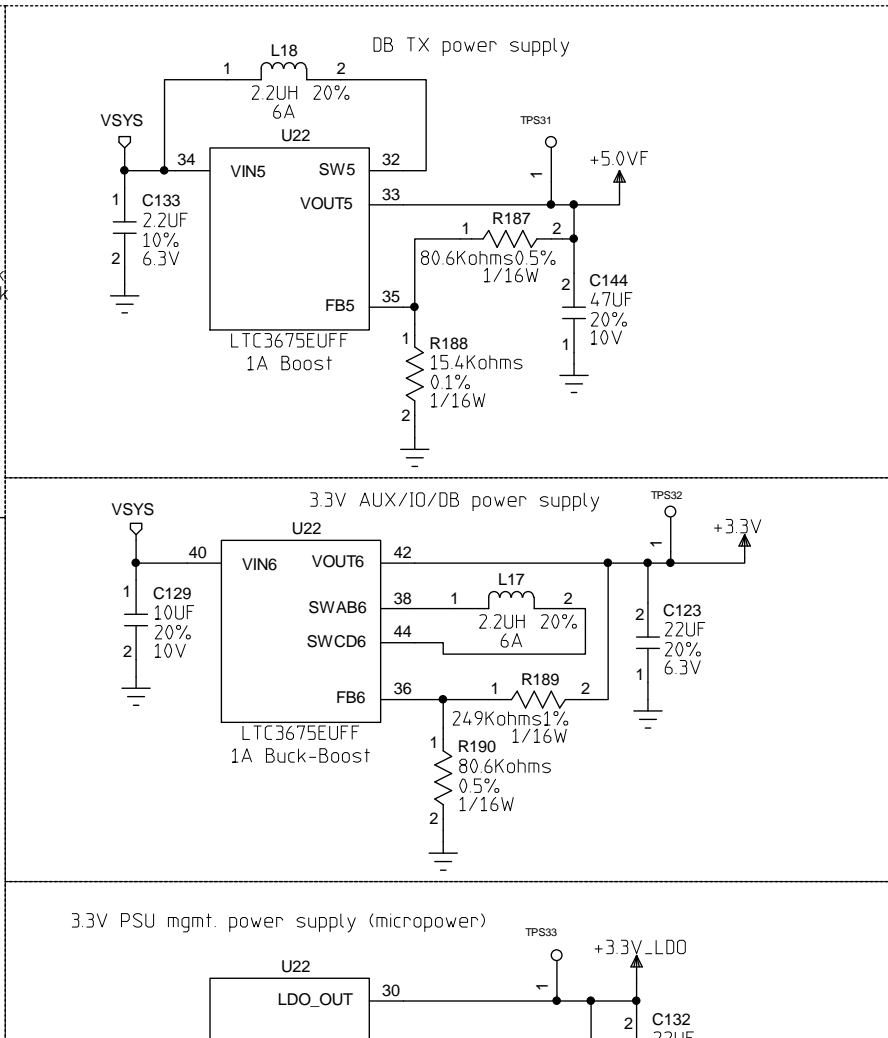
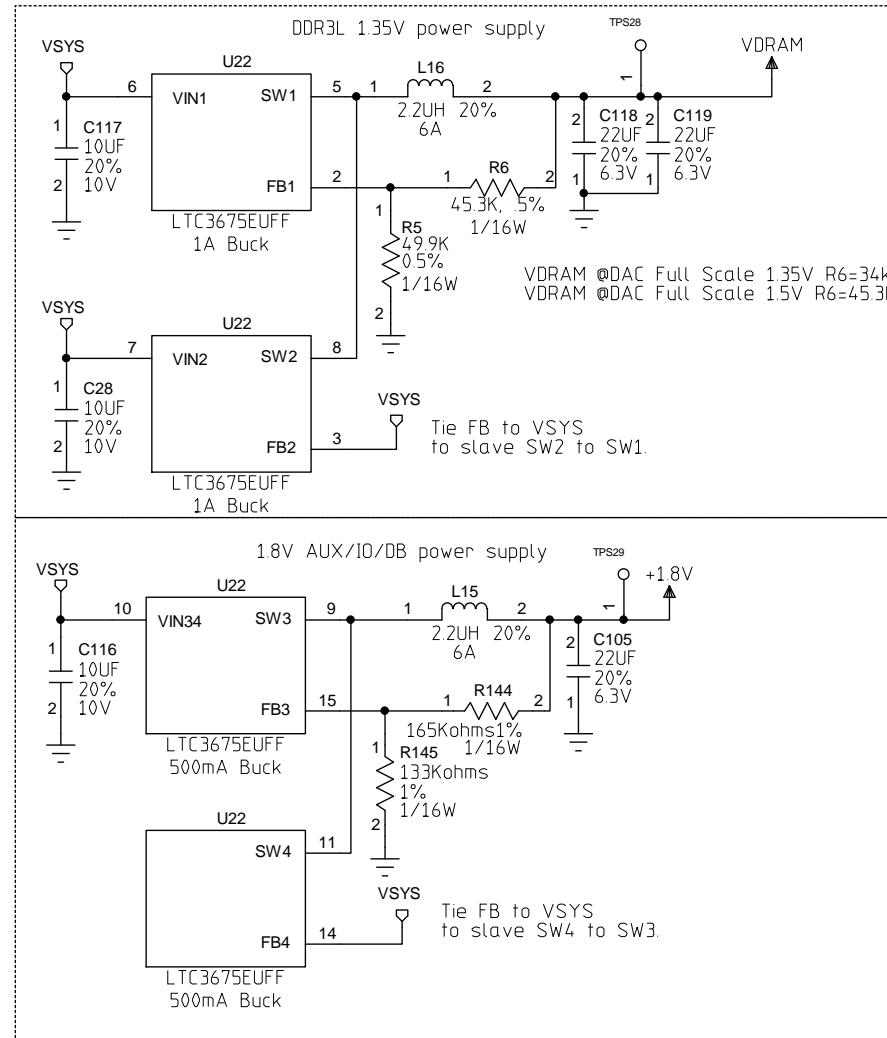
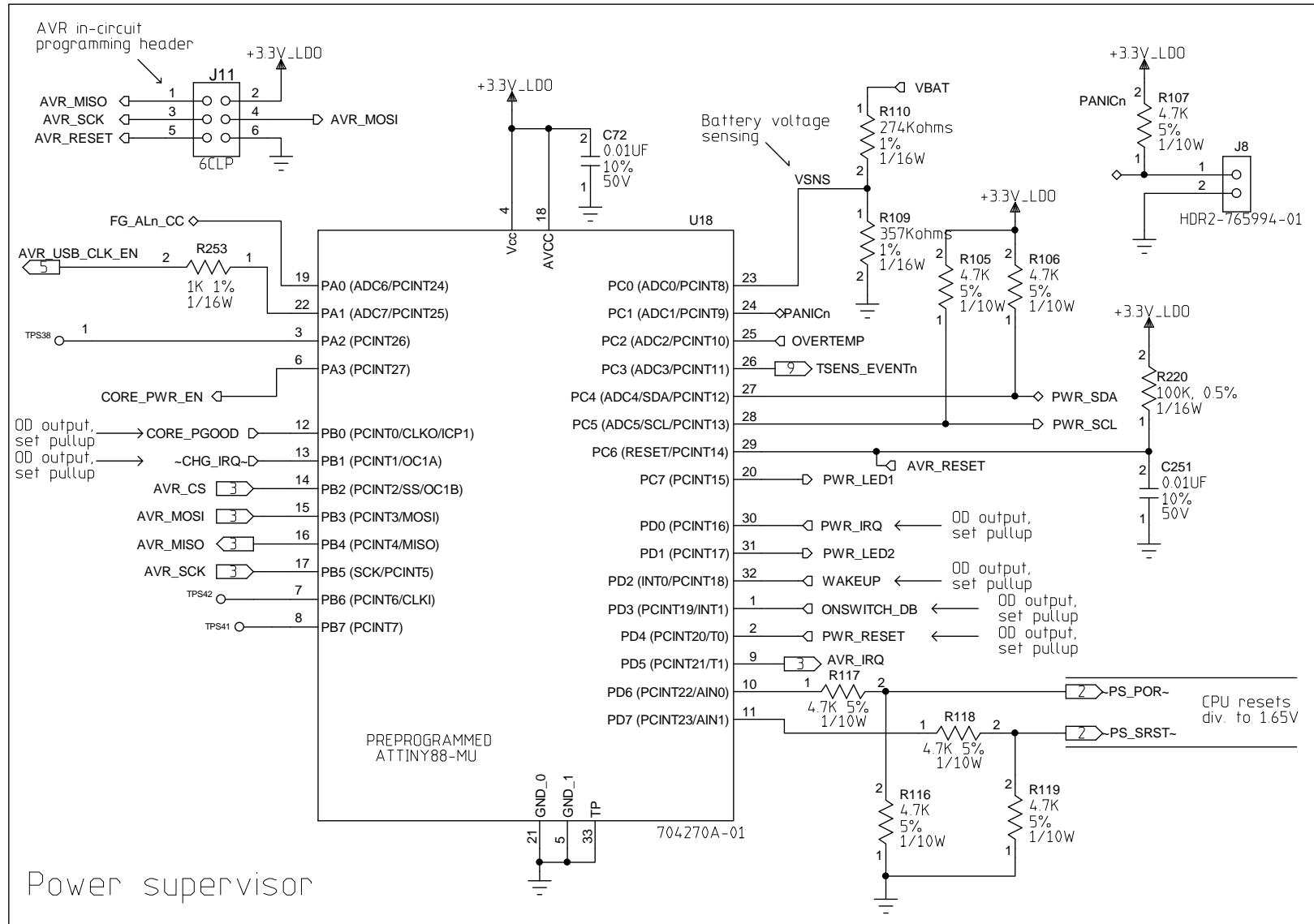
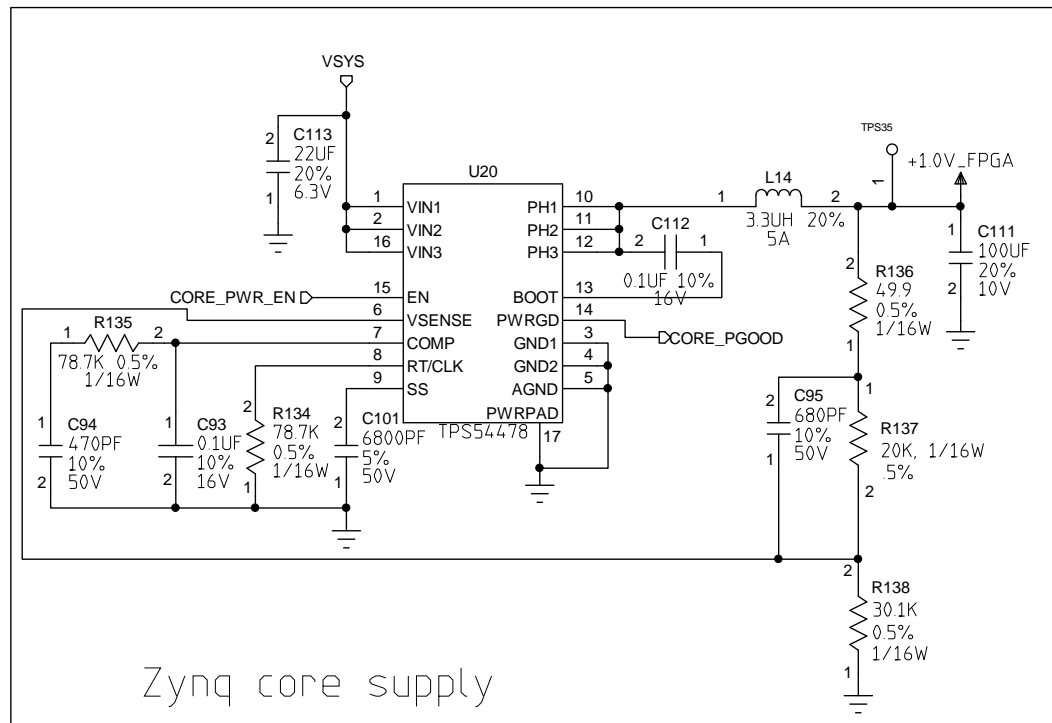
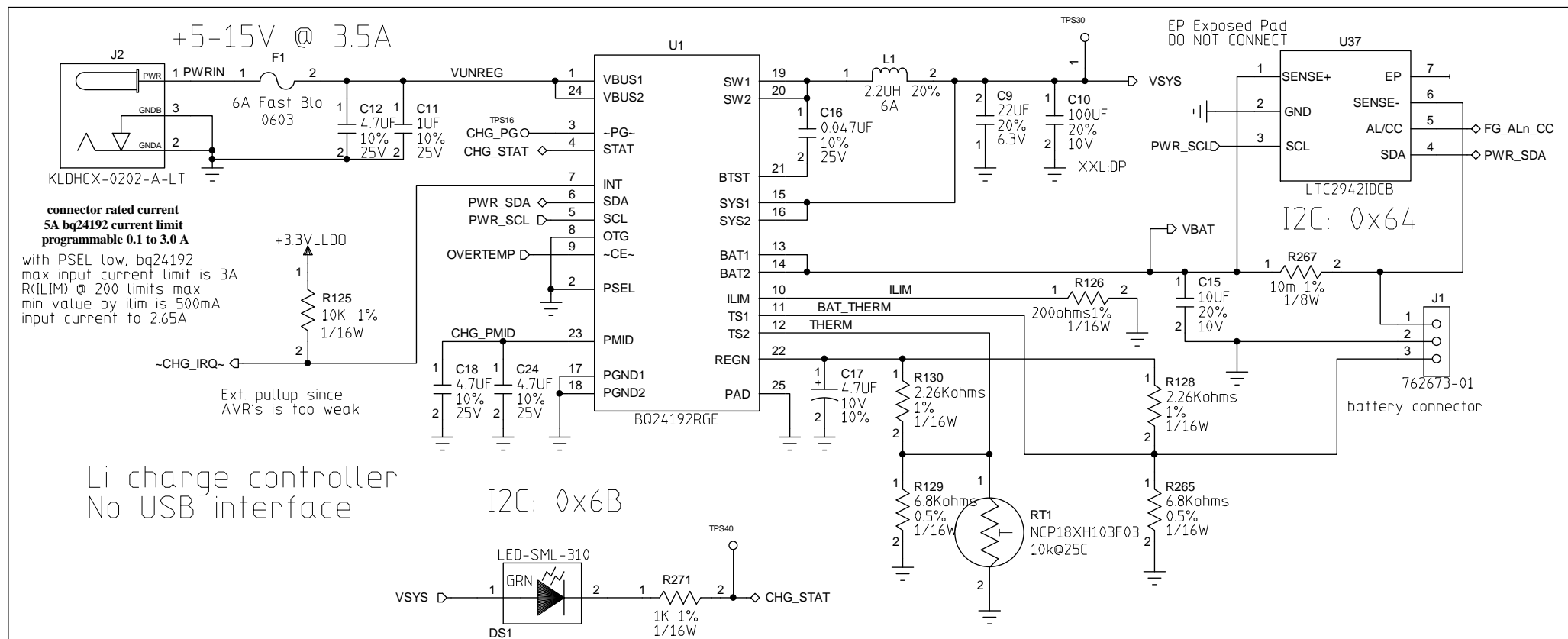
[illegible]

**TOTAL**

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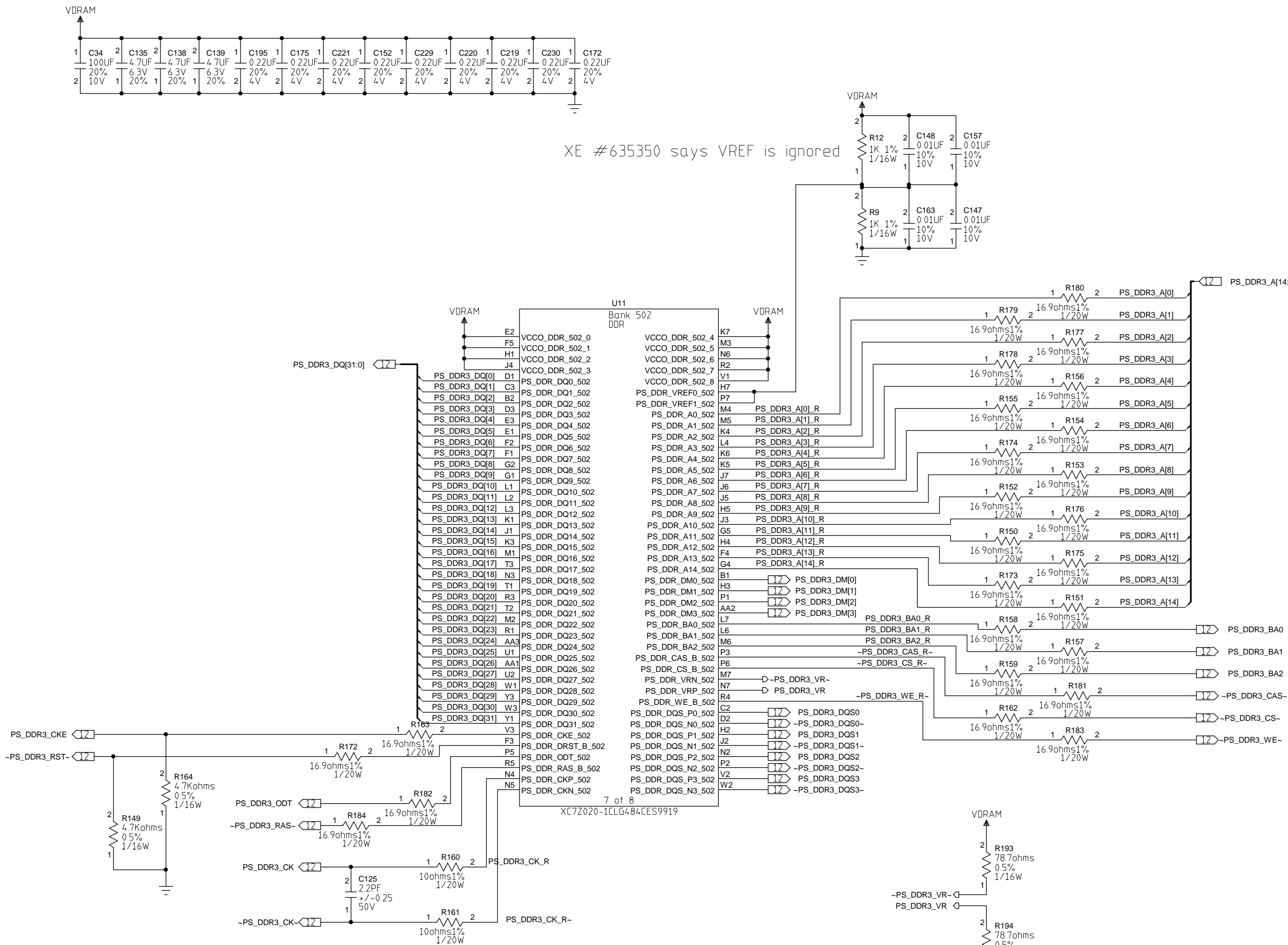


POWER SUPPLIES			
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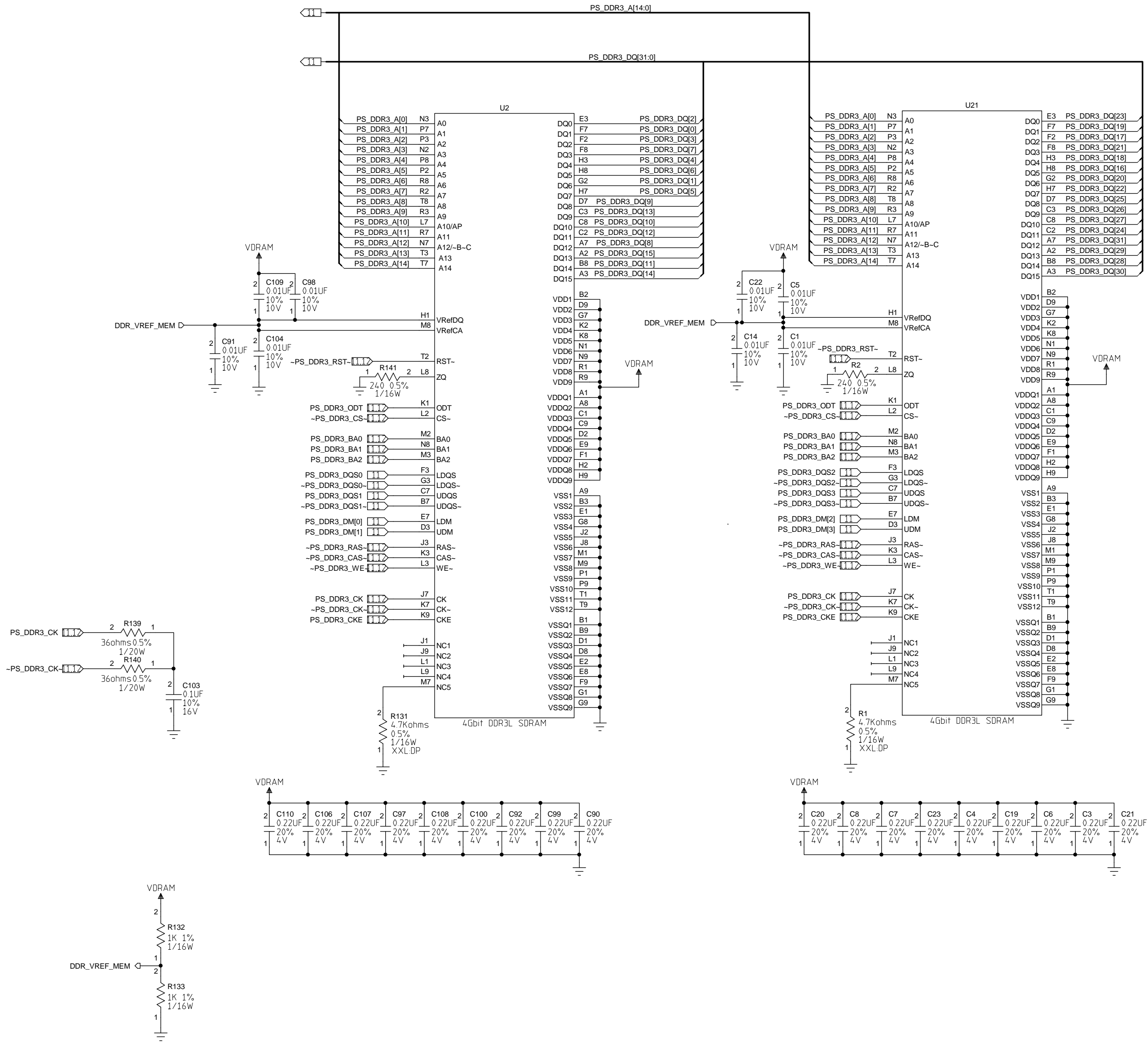


PS DDR3L (CPU SIDE)				
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PS DDR3L (SDRAM SIDE)				
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PL DDR3L SDRAM			
E300			
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