YOUR Group Details:

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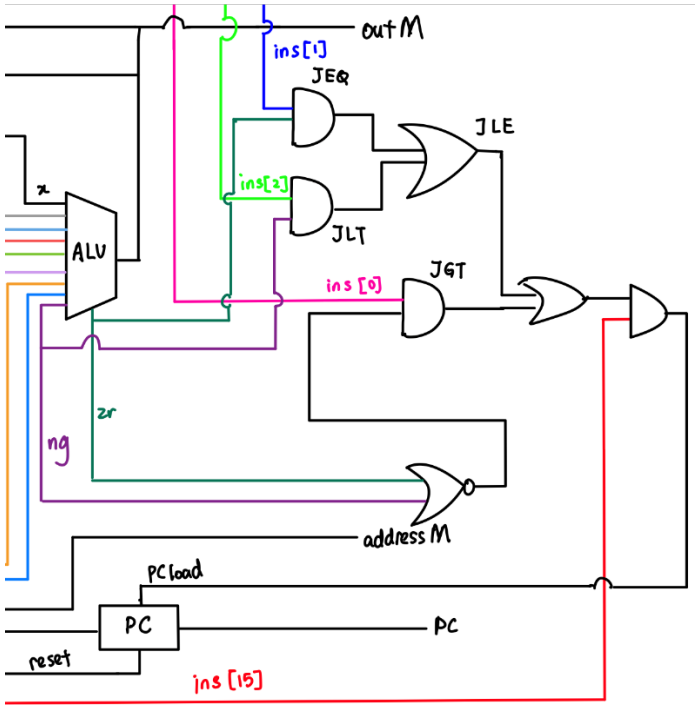
Justification of YOUR Circuitry Diagram Design:

(**NOTE**: No more than 300 words)



- For Central Processing Unit (CPU) chip, built-in Arithmetic Logic Unit (ALU) is used. There are five jump conditions mainly, JEQ, JLT, JGT, JLE, and load Program Counter (PC).
- First, zr and ng, which are ALU outputs are inputs for NOR gate. Universal gate is used to replace one OR gate and one NOT gate which allows information to go through only one gate to improve rate of information processing.
- To produce JGT which means jump if out is more than 0, the output and instruction[0] or j3 become inputs for AND gate.
- For JEQ which implies jump when out is equal to 0, AND gate receives instruction[1] or j2, and zr as its inputs whereas for JLT which means jump when output is less than 0, another AND gate receives instruction[2] or j1, and ng as inputs.
- The output from these two AND gates become inputs for the OR gate to produce JLE which is jump if output is less than or equal to 0.
- JLE and JGT are OR gate inputs where the output and instruction[15] are inputs for AND gate to produce PCload. Hence, it helps PC to load instruction being executed at current time.
- This CPU chip works because all instructions have been used and connected correctly to the respective gates and each instruction is only used once except for instruction[15] which is used 5 times to produce D register load, Mux selector, A register load, PCload, and write memory.
- All the gates used to produce jump conditions are necessary and most optimal because if more gates are added or removed, it will produce an error as jump conditions like less than, more than

and equal to require an AND gate while for less than or equal to, it requires one AND gate and one OR gate.

(300 words)