D1s

Most Cost-effective Decoding Platform SoC

Overview

D1s is a cost-effective AIoT chip designed by Allwinner for the intelligent decoding market. It possesses a 64bit RISC-V ISA Alibaba T-Head C906 CPU and built-in 64M DDR2, and supports Linux system. Besides, it integrates a large number of self-developed audio and video related IP, which support full format decoding such as H.265, H.264, MPEG-1/2/4, JPEG and audio interfaces such as ADC/DAC/I2S/PCM/DMIC/OWA. D1s can be widely used in smart home panels, HMI, industrial control, smart cars and other products.

Highlights

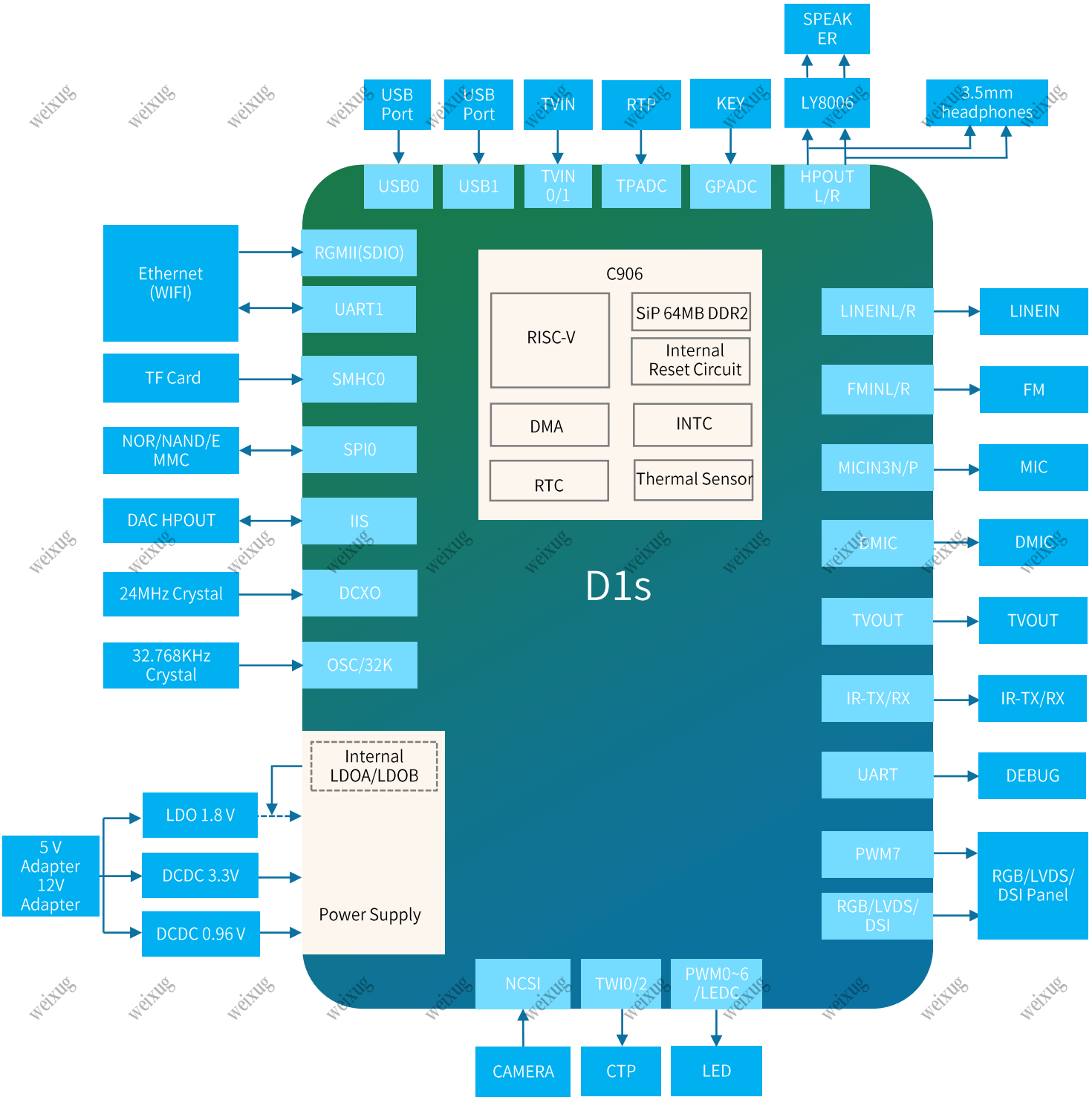
- Integrated 64-bit RISC CPU processor provides powerful computing performance.
- The 1080p full format decoding, rich display output interfaces, and Allwinner SmartColor 2.0 display enhancement technology provide excellent video experience for users.
- To reduce the BOM cost, a 64 MB DDR2 die is embedded for D1s.
- Rich peripheral interfaces, such as USB, SDIO, EMAC, TWI, UART, SPI, PWM, GPADC, IR TX&RX, and so on, greatly facilitate product expansion.
- The advanced process design with lower voltage and lower leakage, the power optimization design for typical scenes and the enhanced heat dissipation package, improve the heating experience of the product.

Features

CPU	• RISC CPU • 32 KB I-cache + 32 KB D-cache
Memory	• SIP 64MB DDR2 • SD3.0/eMMC 5.0, SPI Nor/NAND Flash
Video Engine	• Video decoding -H.265 up to 1080p@60fps -H.264 up to 1080p@60fps -H.263, MPEG-1/2/4, JPEG, Xvid, Sorenson Spark, up to 1080p@60fps • Video encoding -JPEG/MJPEG up to 1080p@60fps -Supports input picture scaler up/down
Display Engine	• Allwinner SmartColor2.0 post processing for an excellent display experience • Supports de-interlace (DI) up to 1080p@60fps • Supports G2D hardware accelerator including rotate, mixer, lbc decompression functions
Video OUT	• CVBS OUT interface, supporting NTSC and PAL format • RGB LCD output interface up to 1920 x 1080@60fps • Dual link LVDS interface up to 1920 x 1080@60fps • 4-lane MIPI DSI interface up to 1920 x 1200@60fps
Video IN	• 8-bit parallel CSI interface • CVBS IN interface, supporting NTSC and PAL format
Audio	• 2 DACs and 3 ADCs • Analog audio interfaces: MICIN3P/N, LINEINL/R, FMINL/R, HPOUTL/R • Digital audio interfaces: I2S/PCM, DMIC, OWA
Connectivity	• USB2.0 DRD, USB2.0 Host • SDIO 3.0, SPI x 2, UART x 6, TWI x 4 • PWM (8-ch), GPADC (1-ch), TPADC (4-ch), IR TX&RX • 10/100/1000M EMAC with RMII and RGMII interfaces
Package	• eLQFP128, 14 mm x 14 mm

Block Diagram

Application Diagram



ABOUT ALLWINNER

Allwinner Technology, founded in 2007, is a outstanding designer dedicated to intelligent application SoC, high performance analog component and wireless connectivity IC. It is headquartered in Zhuhai China, with other R&D centers and offices in Shenzhen, HongKong, Xi'an, Beijing and Shanghai. Listed on the GEM of the Shenzhen Stock Exchange in 2015, with the stock code 300458.

Motivated by customer-oriented strategy, Allwinner aligns remarkable R&D teams with long-term core-technology investment in UHD video processing, high-performance multi-core CPU/GPU integration with AI and advanced manufacturing process in terms of high integration , ultra-low power consumption and full-stack integration platform, providing competitive turnkey solutions with considerate services. The products powered by Allwinner spread across from smart hardware, smart home, consumer electronics, HD media, smart video, connected car, industry control, wireless communication to analog products.

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