

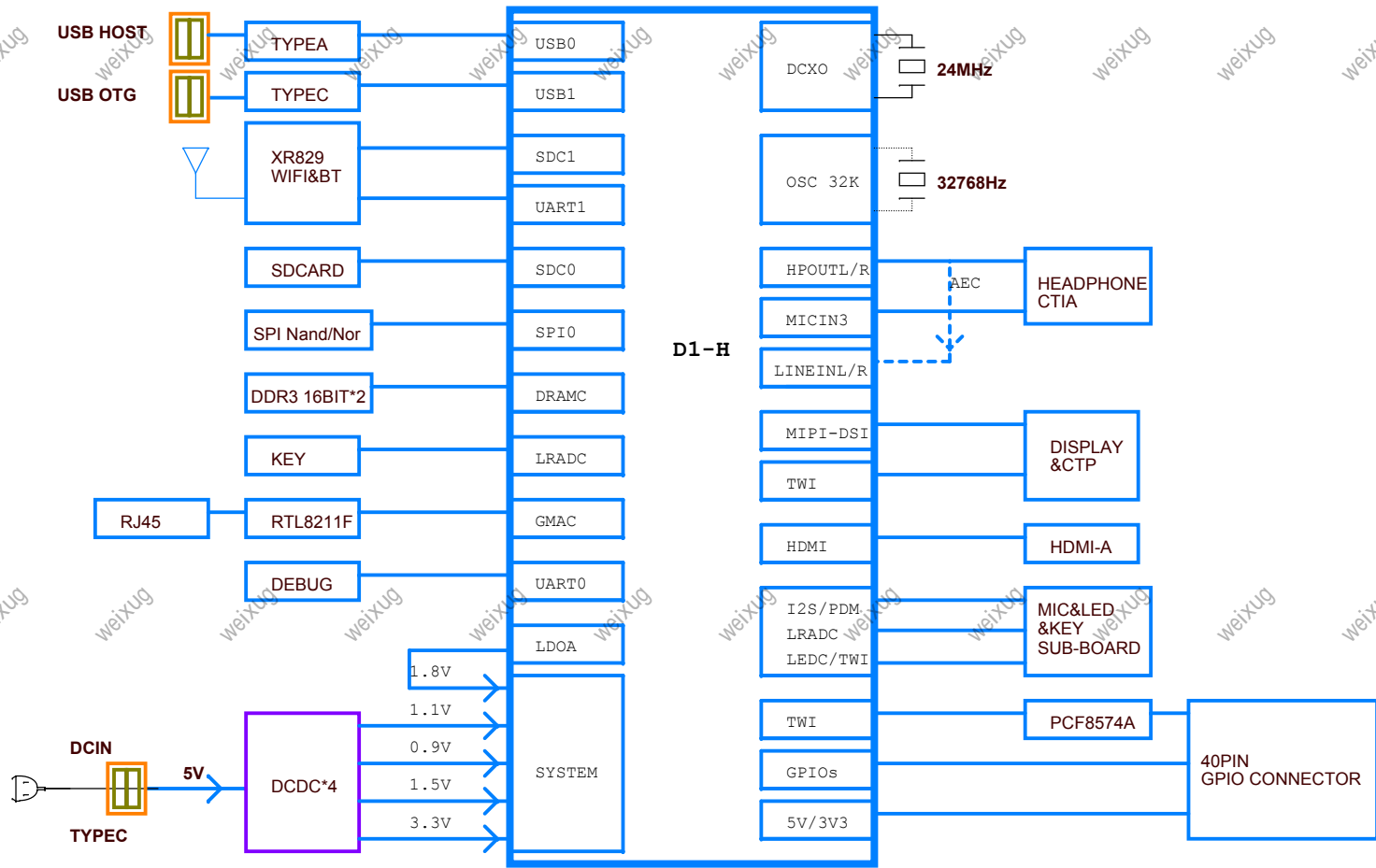
VERSION HISTORY

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Revision	Description	Date	Drawn
Ver 1.0	Releas version	2021/05/10	AWOL010
Ver 1.1	update VDD-SYS 、 HDMI-I2C	2021/11/24	AWOL010
Ver 1.2	update HDMI-I2C 、 HDMI-CEC	2021/11/26	AWOL010

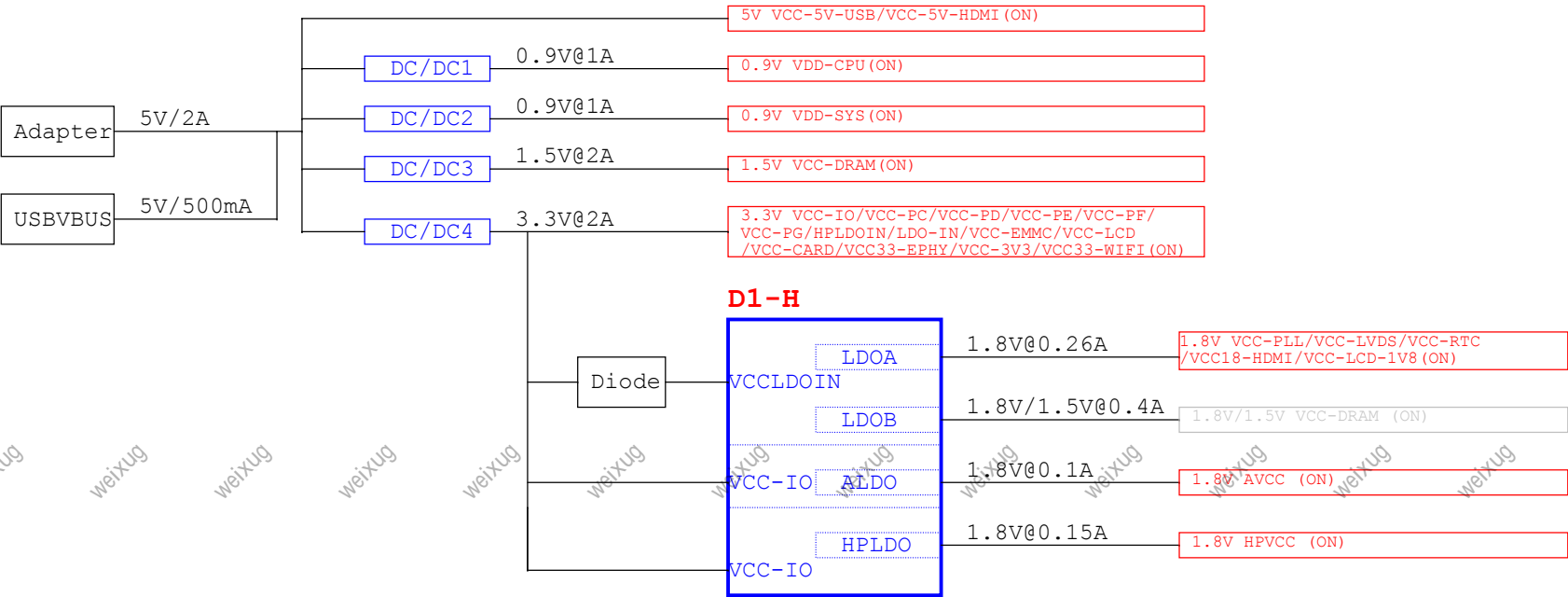
BLOCK



POWER TREE

DEFAULT POWER ON

DEFAULT NC



GPIO ASSIGNMENT

40 PIN CONNECTOR

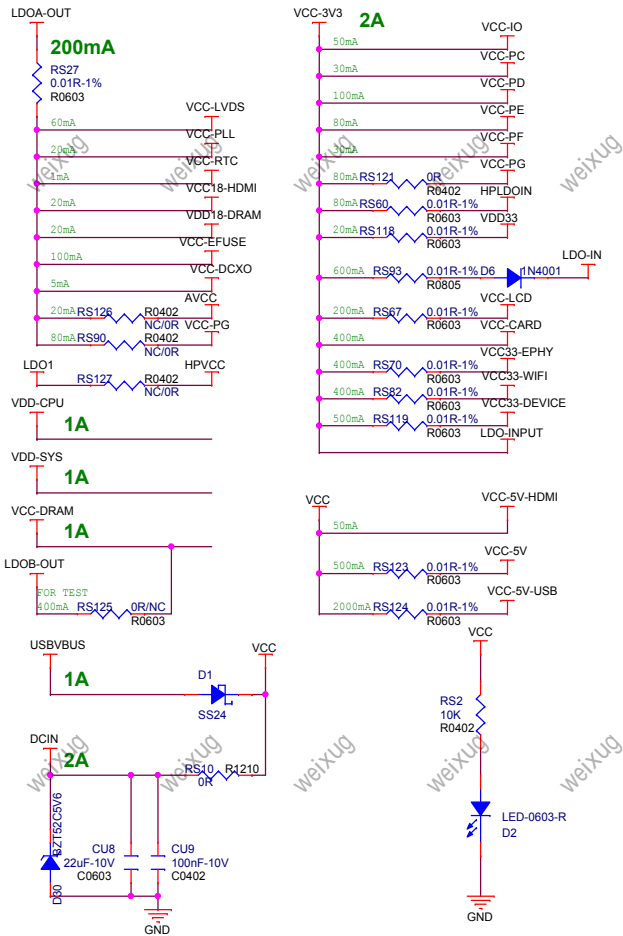
FUNCTION3	FUNCTION2	DEFAULT	SOC.No	PIN		PIN	SOC.No	DEFAULT	FUNCTION2	FUNCTION3
		3V3		1		2		5V		
	TWI2-SDA	GPIO1	PB1	3		4		5V		
	TWI2-SCK	GPIO2	PB0	5		6		GND		
IR-RX	PWM	GPIO3	PD22	7		8	PB8	GPIO4	UART0-TXD	
		GND		9		10	PB9	GPIO5	UART0-RXD	
		GPIO6	PP7	11		12	PB5	GPIO7	I2S2-BCLK	UART5-RX
		GPIO8	PP0	13		14		GND		
PWM	IR-RX	GPIO9	PB12	15		16	PP1	GPIO10		
		3V3		17		18	PP2	GPIO11		
	SPI1-MOSI	GPIO12	PD12	19		20		GND		
UART3-RTS	SPI1-MISO	GPIO13	PD13	21		22	PP4	GPIO14		
UART3-RX	SPI1-CLK	GPIO15	PD11	23		24	PD10	GPIO16	SPI1-CE0	UART3-TX
		GND		25		26	PP3	GPIO17		
UART3-CTS	SPI1-HOLD	GPIO18	PD14	27		28	PP5	GPIO19		
IR-RX	SPI1-WP	GPIO20	PD15	29		30		GND		
		GPIO21	PC1	31		32	PE17	NC	IR-TX	
		NC		33		34		GND		
PWM	I2S2-LRCK	GPIO22	PB6	35		36		NC		
		GPIO23	PP6	37		38	PB3	GPIO24	I2S2-DIN	
		GND		39		40	PB4	GPIO25	I2S2-DOUT	UART5-TX

备注：PP0~PP7为PCF8574A扩展GPIO

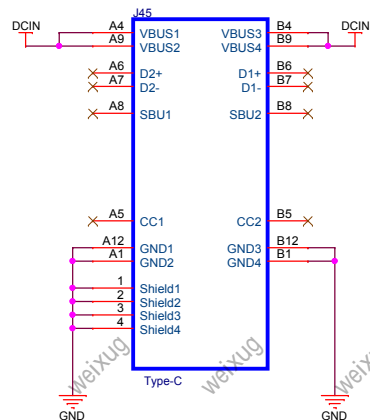
30 PIN CONNECTOR

PIN	SOC.No	DMIC	AMIC
1		GND	GND
2	PB10	DMIC-D1	TWI0-SCK
3	PB11	DMIC-D0	TWI0-SDA
4	PB7	NC	I2S2-MCLK
5	PB5	NC	I2S2-BCLK
6	PB6	NC	I2S2-LRCK
7	PB3	NC	I2S2-DIN0
8-10		NC	NC
11	LRADC	LRADC	LRADC
12	PB10	DMIC-D1	NC
13		GND	GND
14-20		NC	NC
21		GND	GND
22-25		5V	5V
26		3V3	3V3
27	PD17	DMIC-D2	NC
28	PE17	DMIC-CLK	NC
29	PD20	LEDC	LEDC
30		GND	GND

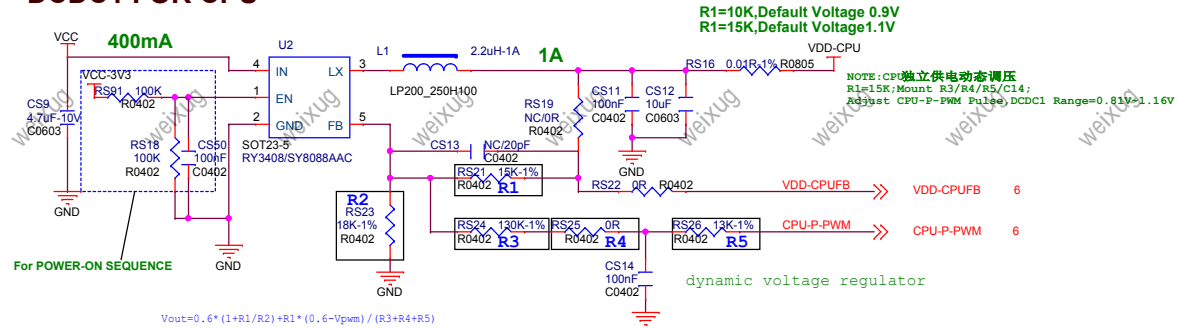
POWER



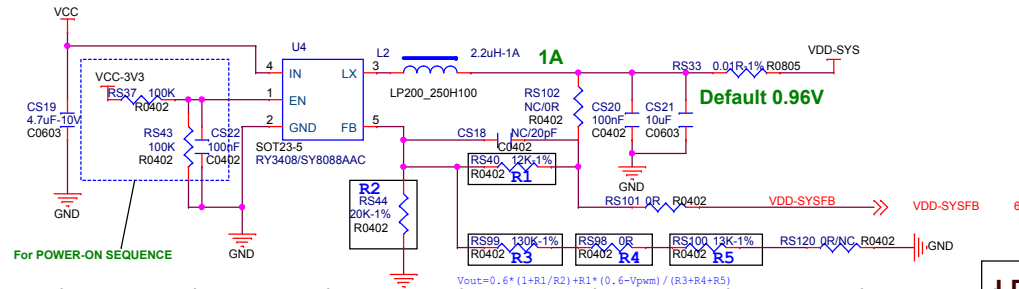
TYPEC-POWER



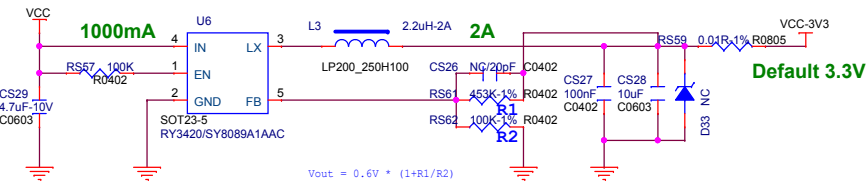
DCDC1 FOR CPU



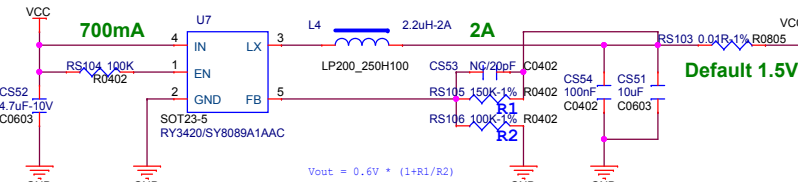
DCDC2 FOR SYS



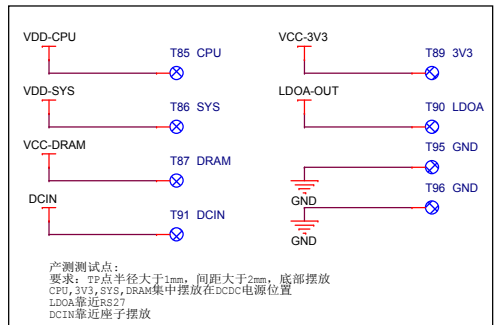
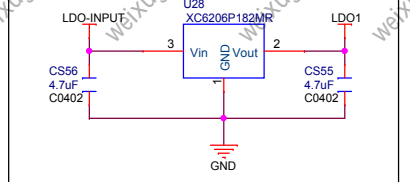
DCDC4 FOR 3V3



DCDC3 FOR DRAM



LDO1 RESERVED FOR HPVCC

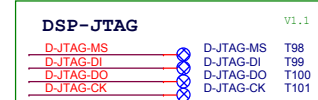
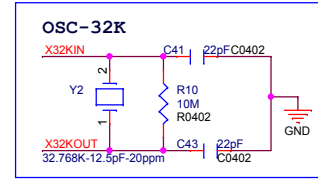
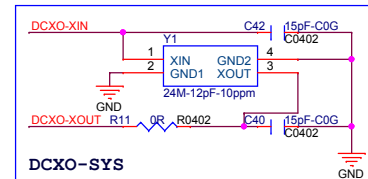
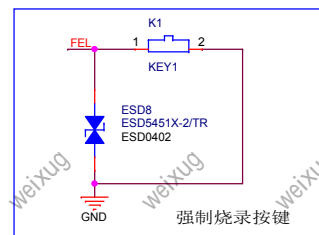
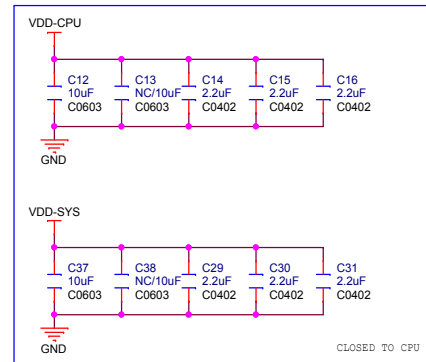
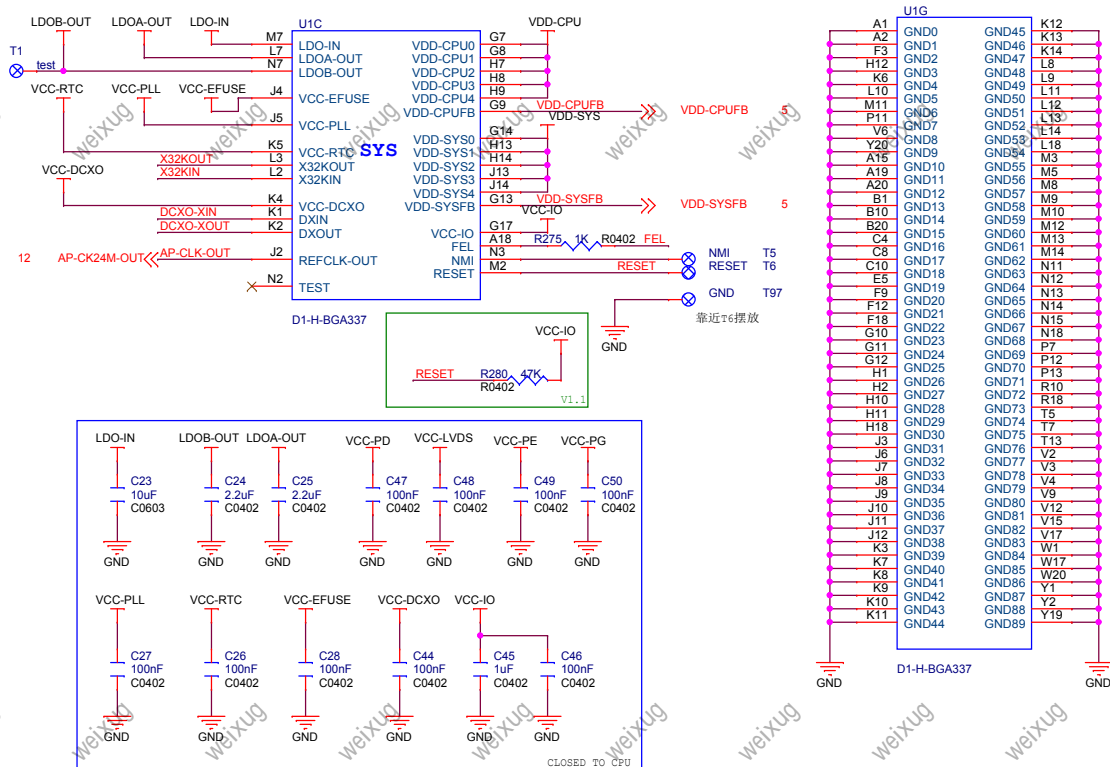
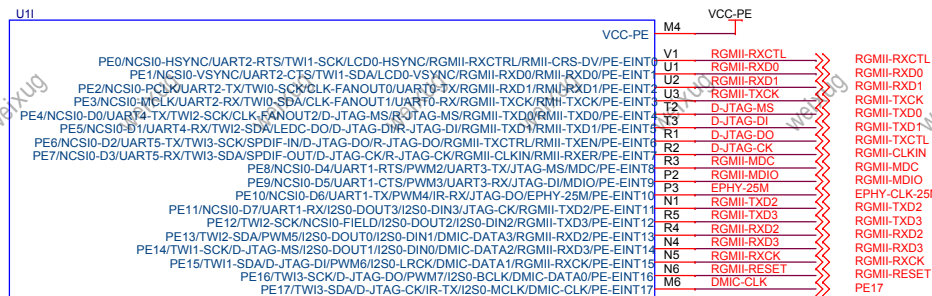


Allwinner Online Technology Co., Ltd
Design Name
D1-H_NEZA

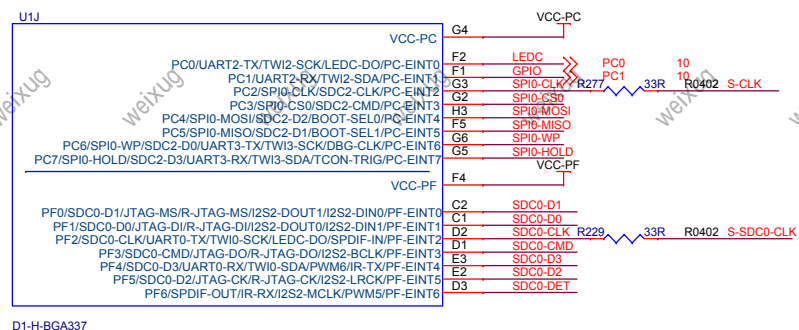
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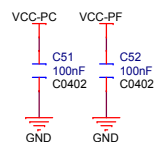
U1H



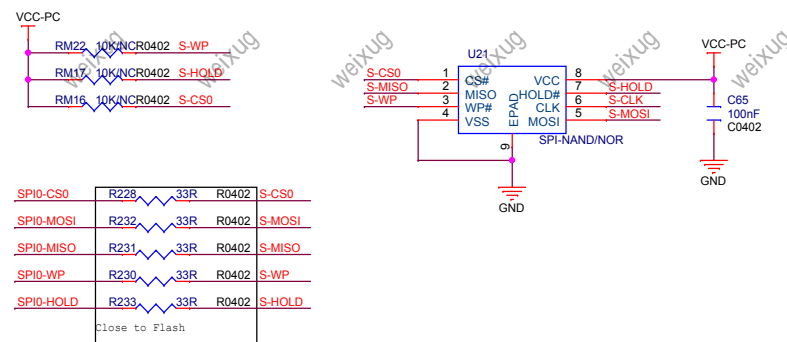
SOC-FLASH&CARD



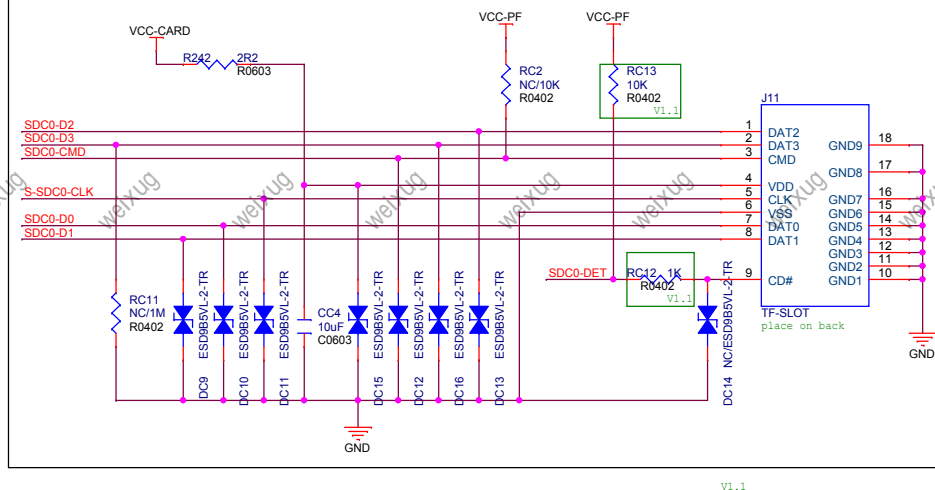
D1-H-BGA337



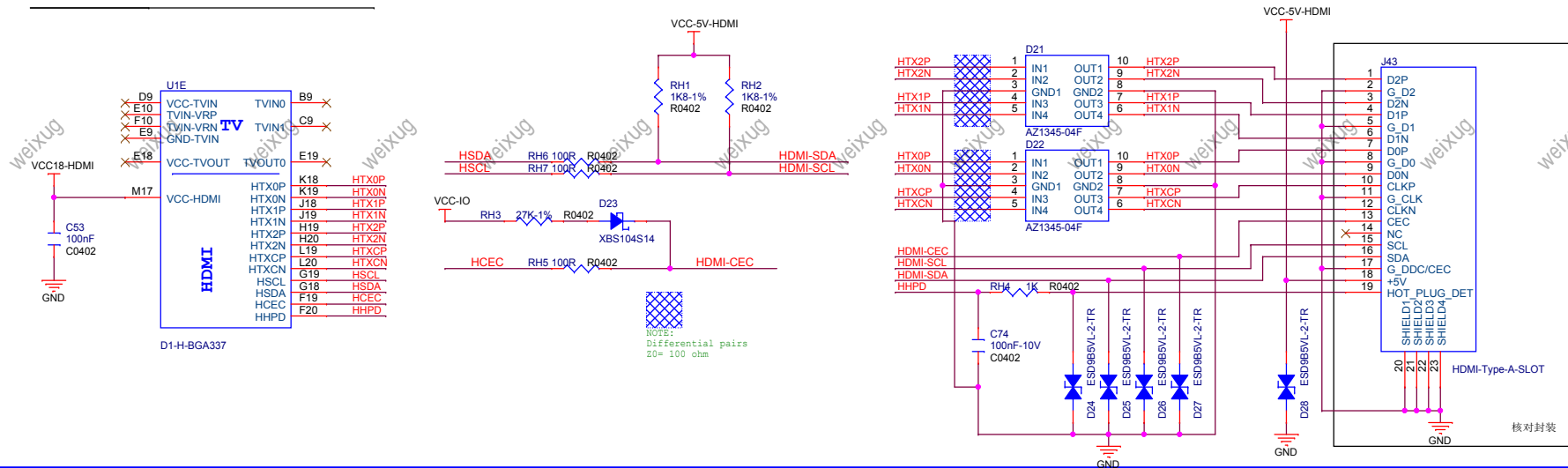
SPI-NAND/NOR



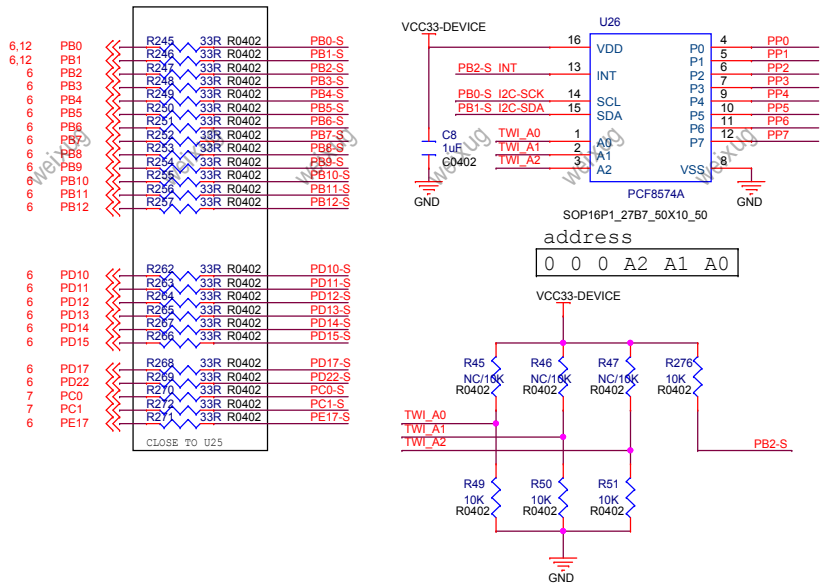
SDCARD



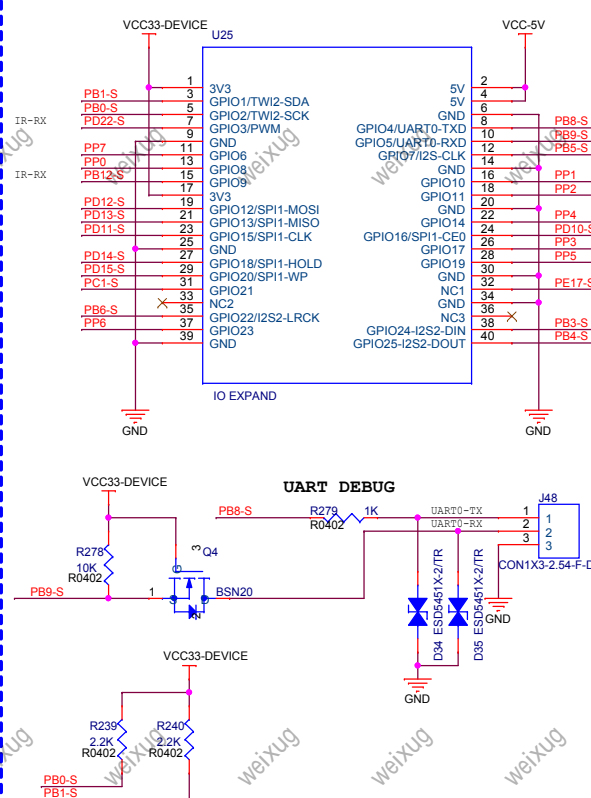
HDMI&IO EXPAND



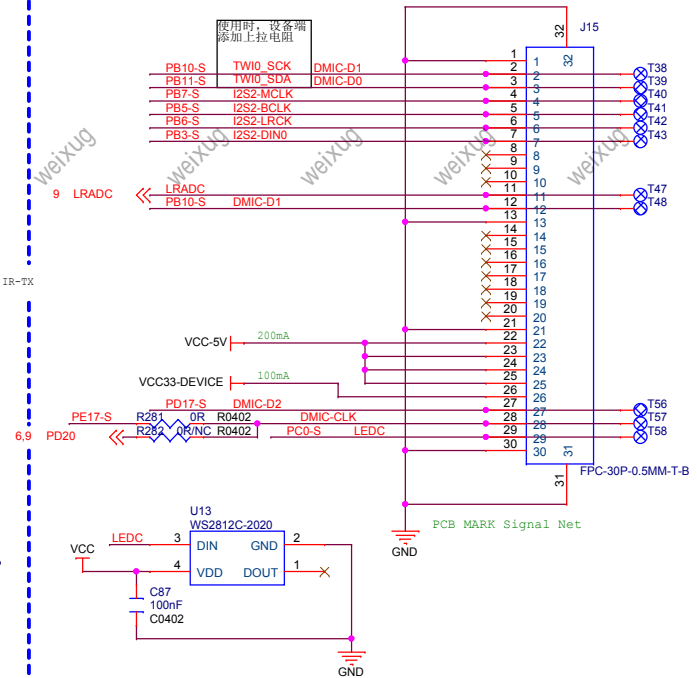
IO EXPAND



GPIO CONNECTOR

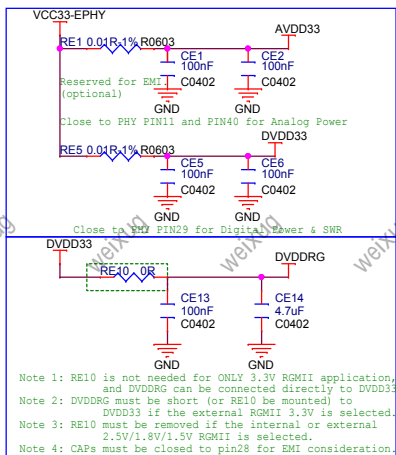


EXTERNAL AMIC/DMIC





External Clock From SOC

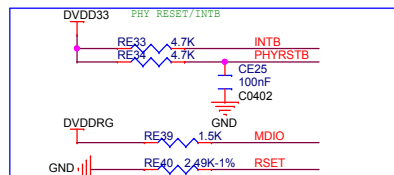
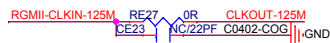
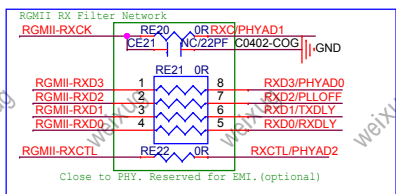
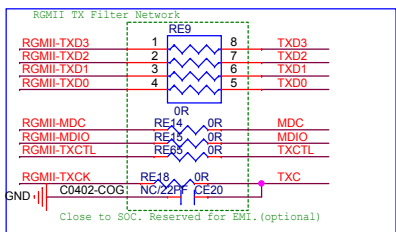


Note 1: RE10 is not needed for ONLY 3.3V RGMII application,
and DVDDR3 and DVDDR4 can be connected directly to DVDDR3.

Note 2: DVDDR3 must be short (or RE10 be mounted) to
DVDDR3 if the external RGMII 3.3V is selected.

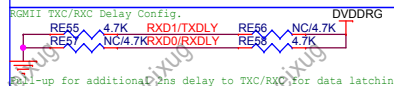
Note 3: RE10 must be removed if the internal or external
2.5V/1.8V/1.5V RGMII is selected.

Note 4: CAPs must be connected to pin28 for EMI consideration.

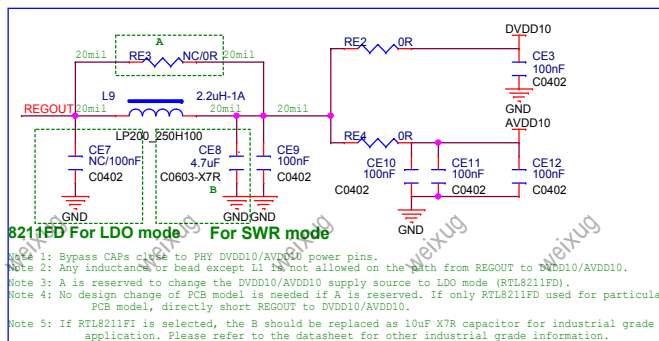


Enable/Disable PLL @ ALDPS

 Pull-up to disable PLL @ ALDPS mode.



Full-up for additional 2ns delay to TXC/RXC for data latching



8211FED For LDO mode For SWR mode GND

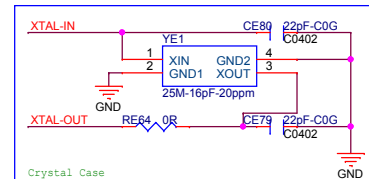
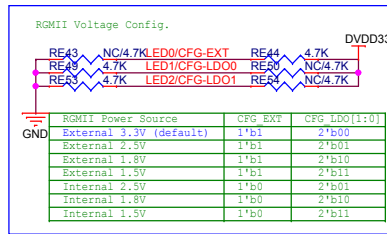
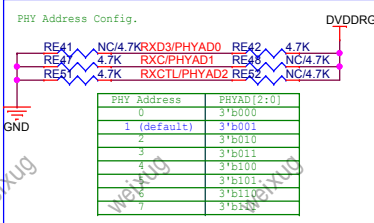
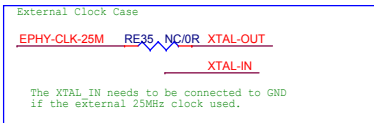
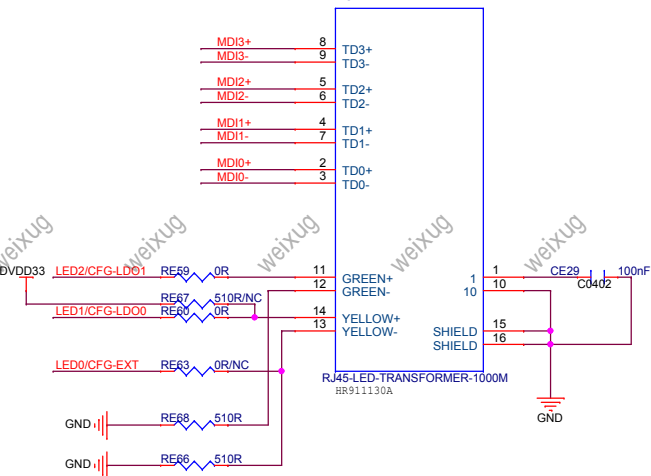
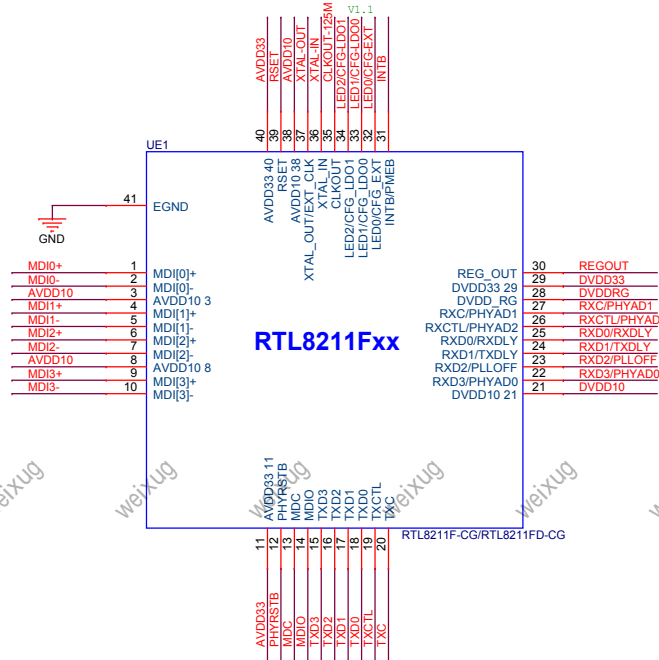
Note 1: Bypass CAPs close to PHY DVD1D0/AVDD1D0 power pins.

Note 2: Any inductance or bead except L1 is not allowed on the path from REGOUT to DVD1D0/AVDD1D0.

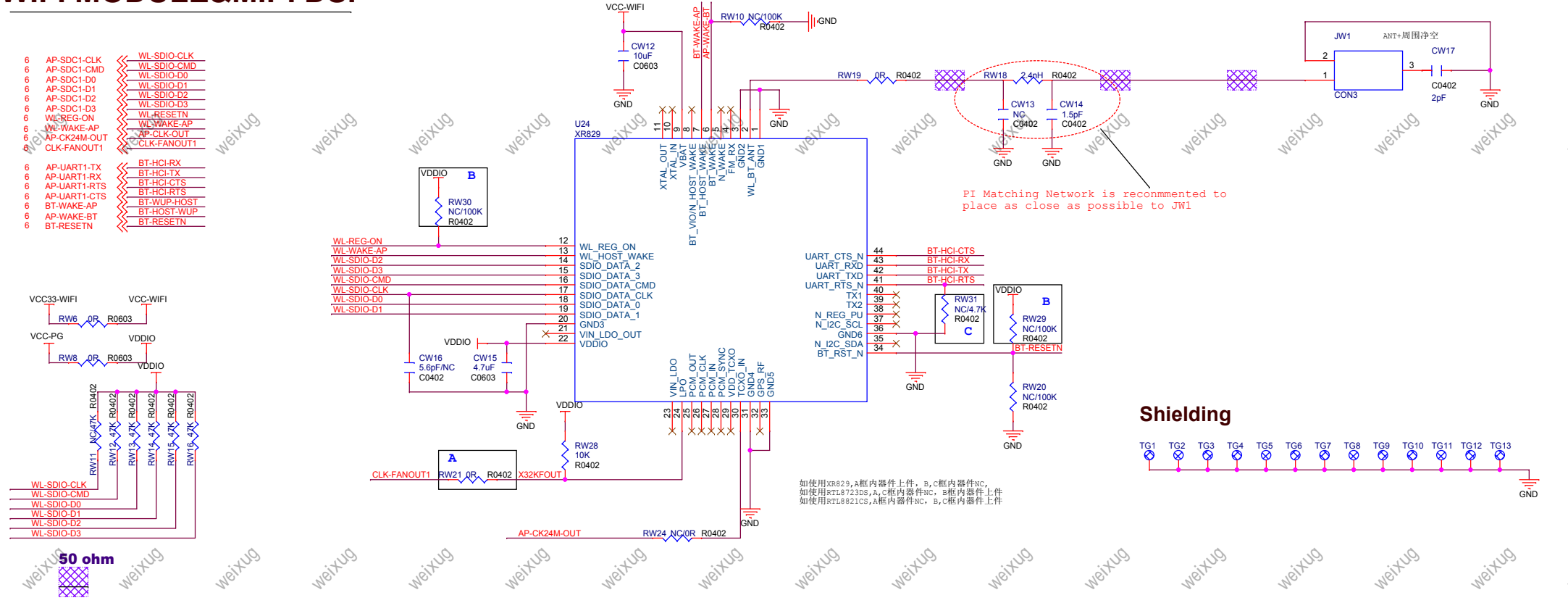
Note 3: A is reserved to change the DVD1D0/AVDD1D0 supply source to LDO mode (RTL211FID).

Note 4: No diode or Schottky diode A is connected. If any RTL211FID used for particular PCB model, directly short REGOUT to DVD1D0/AVDD1D0.

Note 5: If RTL211FID is selected, the B should be replaced as 10uF X7R capacitor for industrial grade application. Please refer to the datasheet for other industrial grade information.



WIFI MODULE&MIPI DSI



MIPI-DSI

