Started on	Monday, 8 July 2024, 7:40 AM
State	Finished
Completed on	Monday, 8 July 2024, 7:46 AM
Time taken	5 mins 20 secs
Grade	**7.00** out of 10.00 (**70**%)

Question **1**
Correct

Mark 1.00 out of 1.00

A JK flip-flop can be used to implement:

- ⦿ a.   Counters ✔
- ○ b.   Multiplexers
- ○ c.   Decoders
- ○ d.   Adders

Question **2**
Correct

Mark 1.00 out of 1.00

The clock signal in flip-flops is used for:

- ○ a.   Data transmission
- ○ b.   Resetting the flip-flop
- ⦿ c.   Synchronizing operations ✔
- ○ d.   Powering the flip-flop

Question **3**
Incorrect

Mark 0.00 out of 1.00

Which type of flip-flop is used in shift registers?

- ○ a.   SR flip-flop
- ○ b.   D flip-flop
- ○ c.   T flip-flop
- ⦿ d.   JK flip-flop ✖

Question 4

Incorrect

Mark 0.00 out of 1.00

Sequential circuits are distinguished from combinational circuits by the presence of:

- a. Clock signals
- b. Memory elements
- c. Logic gates
- ● d. Multiplexers ✖

Your answer is incorrect.

Question 5

Correct

Mark 1.00 out of 1.00

What is a typical use of a register in a computer system?

- a. Storing the program instructions
- ● b. Storing temporary data during arithmetic or logic operations ✔
- c. Performing data routing in the ALU
- d. Controlling the clock signal

Your answer is correct.

Question 6

Correct

Mark 1.00 out of 1.00

The output of a T flip-flop with T=1 is:

- a. 0
- b. 1
- ● c. Toggle ✔
- d. Undefined

Question 7

Correct

Mark 1.00 out of 1.00

The purpose of the clock signal in sequential circuits is to:

- ○ a.   provide power
- ◉ b.   synchronize operations ✔
- ○ c.   amplify signals
- ○ d.   provide external input

Question 8

Correct

Mark 1.00 out of 1.00

What is a fundamental difference between a latch and a flip-flop?

- ◉ a.   Latches are level-sensitive, while flip-flops are edge-sensitive ✔
- ○ b.   Latches are edge-triggered, while flip-flops are level-triggered
- ○ c.   Latches have clock inputs, while flip-flops do not
- ○ d.   Latches are synchronous, while flip-flops are asynchronous

Your answer is correct.

Question 9

Correct

Mark 1.00 out of 1.00

Which flip-flop has an additional input called the enable input?

- ◉ a.   D flip-flop ✔
- ○ b.   SR flip-flop
- ○ c.   JK flip-flop
- ○ d.   T flip-flop

Question 10

Incorrect

Mark 0.00 out of 1.00

Which gate is used to implement the clock signal for flip-flops?

- ○ a.   AND gate
- ○ b.   OR gate
- ○ c.   XOR gate
- ◉ d.   NOT gate ✘