# Task3\_2

## Четверть сумматор

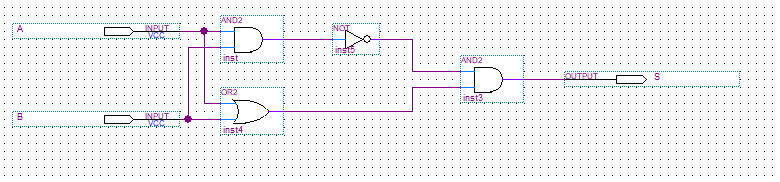
|  |  |  |
| --- | --- | --- |
| **a** | **b** | **S** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Базис реализации: базис Шеффера (И-НЕ)

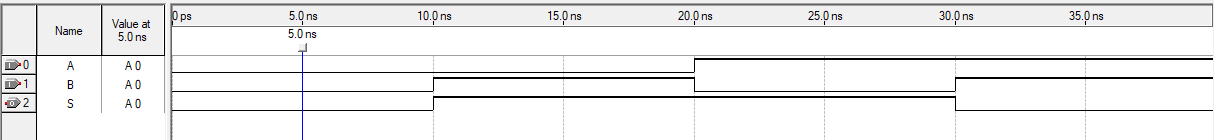
#### Решение:

МДНФ:

### Схема модуля:



### Simulation Report:



|  |  |  |  |
| --- | --- | --- | --- |
| **t** | **a** | **b** | **S** |
| 5 | 0 | 0 | 0 |
| 15 | 0 | 1 | 1 |
| 25 | 1 | 0 | 1 |
| 35 | 1 | 1 | 0 |

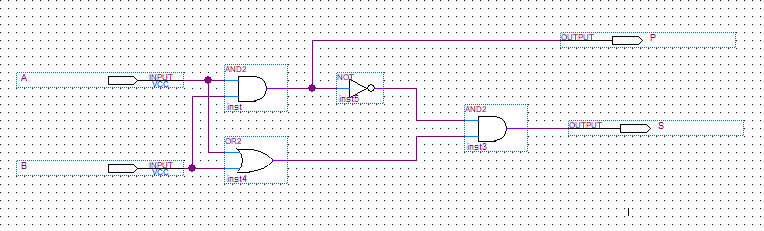
## Полусумматор

|  |  |  |  |
| --- | --- | --- | --- |
| **a** | **b** | **S** | **P** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

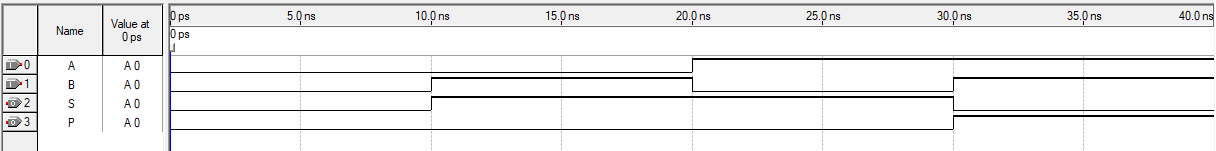
Базис реализации: базис Буля (И, ИЛИ, НЕ)

#### Решение:

### Схема модуля:



### Simulation Report:

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|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **t** | **a** | **b** | **S** | **P** |
| 5 | 0 | 0 | 0 | 0 |
| 15 | 0 | 1 | 1 | 0 |
| 25 | 1 | 0 | 1 | 0 |
| 35 | 1 | 1 | 0 | 1 |

## Полный одноразрядный двоичный сумматор

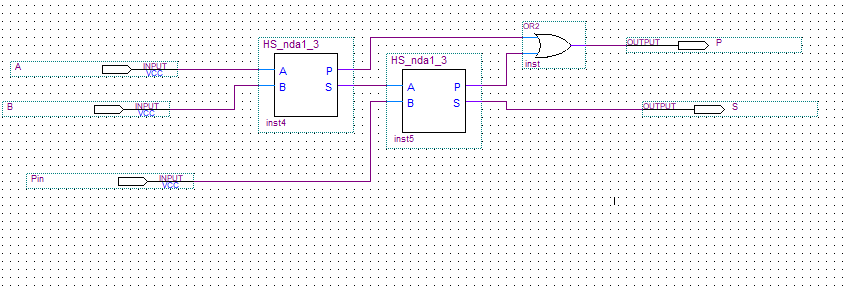
#### **Дано**:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **a** | **b** | **pin** | **S** | **P** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

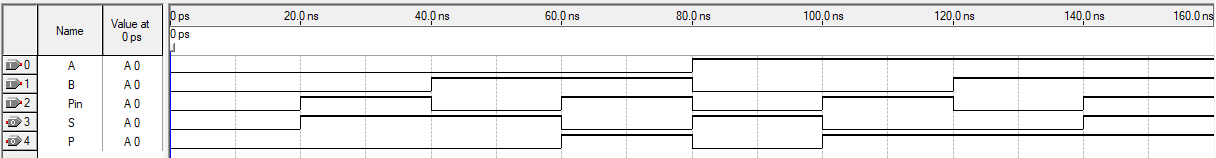
Базис реализации: базис Буля (И, ИЛИ, НЕ)

#### Решение:

### Схема модуля:



### Simulation Report:

****

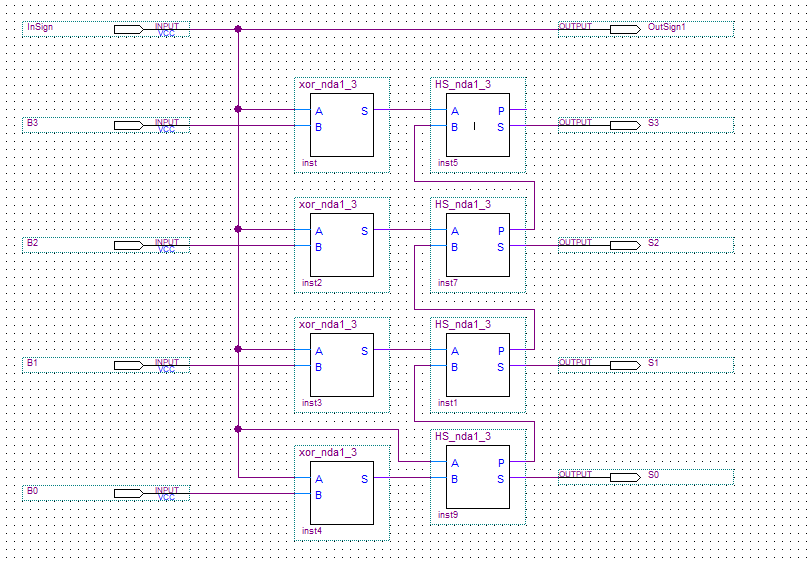
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **t** | **a** | **b** | **pin** | **S** | **P** |
| 10 | 0 | 0 | 0 | 0 | 0 |
| 30 | 0 | 0 | 1 | 1 | 0 |
| 50 | 0 | 1 | 0 | 1 | 0 |
| 70 | 0 | 1 | 1 | 0 | 1 |
| 90 | 1 | 0 | 0 | 1 | 0 |
| 110 | 1 | 0 | 1 | 0 | 1 |
| 130 | 1 | 1 | 0 | 0 | 1 |
| 150 | 1 | 1 | 1 | 1 | 1 |

## Прямой-обратный код

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| InSign | B3 | B2 | B1 | B0 | OutSign | S3 | S2 | S1 | S0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

#### Решение:

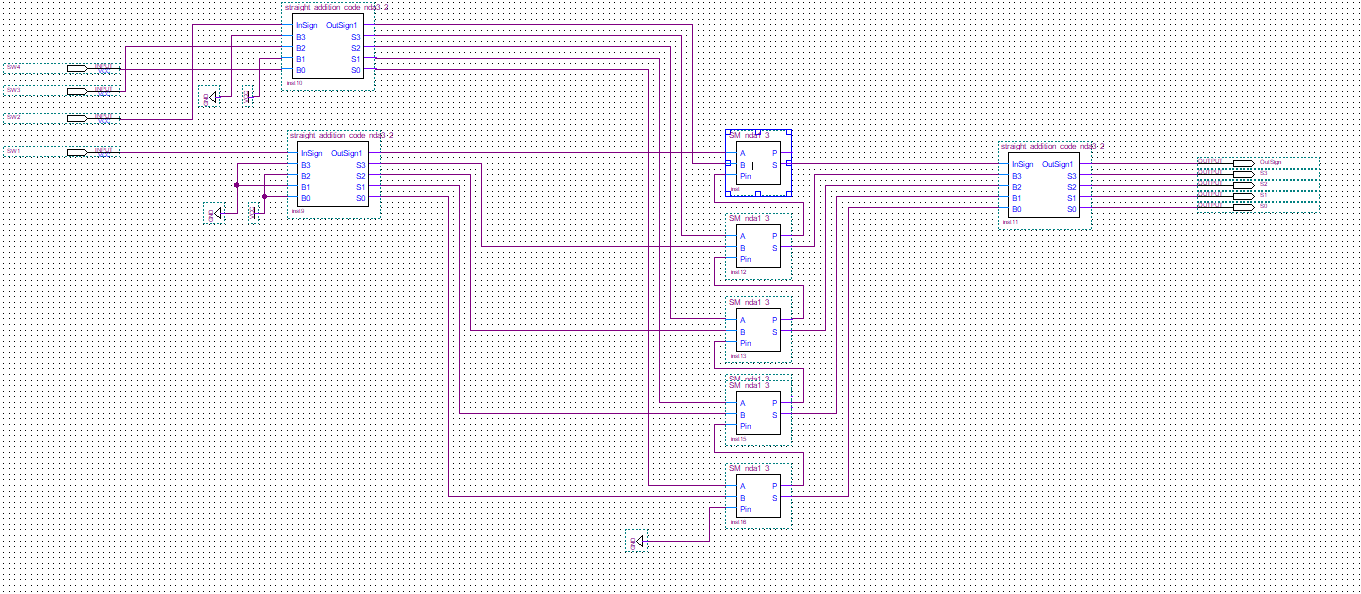
### Схема модуля:



## Арифметико-логическое устройство:

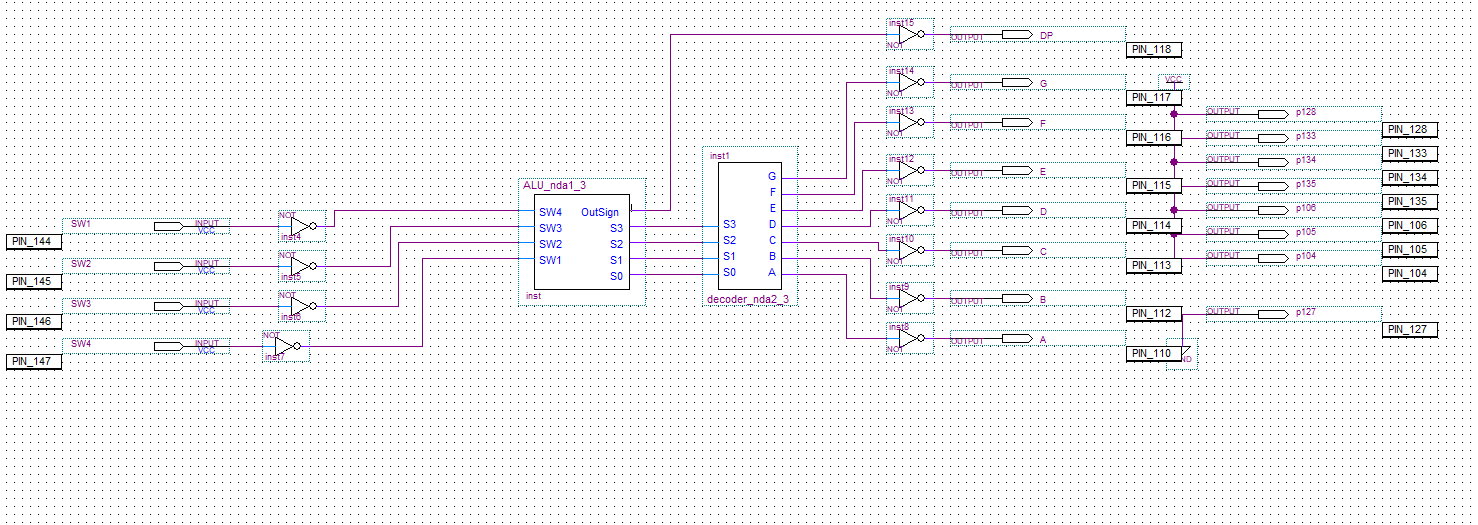
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| SW1 | SW2 | SW3 | SW4 | OutSign | S3 | S2 | S1 | S0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 5+2 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 5+3 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 5+6 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 5+7 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 5-2 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 5-3 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 5-6 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 5-7 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | -5+2 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | -5+3 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | -5+6 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | -5+7 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | -5-2 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | -5-3 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | -5-6 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | -5-7 |

### Схема модуля:



## Стенд:

### Схема модуля:



Заключение:

Разработан АЛУ для сложения положительных и отрицательных двоичных чисел. Кнопки SW1 и SW2 лабораторного стенда определяют знаки 1 и 2 операнда соответственно. Модуль первого операнда равен 510. Модуль второго операнда в двоичной системе счисления задаётся с использованием кнопок лабораторного стенда SW3 и SW4 следующим образом: ((SW3)1(SW4))2.

Максимальное время задержки комбинационной схемы составило 12.383 нс. Таким образом, максимальная частота составляет порядка 40 МГц.

Результат работы:

