**Project Report**

**DATASHEET AND EXPLANATION:**

Wiring between NI myRio(master) and steval-mki172v1 (slave):

Here is the wiring explanation:

* Red wire is connected to the power supply of myRio +5V, the steval-mki172v1 needs at least 1,8V to work. It is also connected to SDA and SCL to have the acknowledge.
* Black wire is connected to the analog ground of myRio.
* Yellow wire is connected to the SDA (Serial Data Line) pin.
* Green wire is connected to the SCL (Serial Clock Line) pin.

A diagram of a circuit

Description automatically generated

Here is the default address for the accelerometer (LSM303AGR) is 0011001b (b means R/W bit):

A screenshot of a computer

Description automatically generated

A close-up of a list

Description automatically generated

33h=51d

32h=50d

A document with text and numbers

Description automatically generated

This is an example of an I2C bus. Of course, it isn’t the same register and device addresses and not the same data.

A screen shot of a computer

Description automatically generated

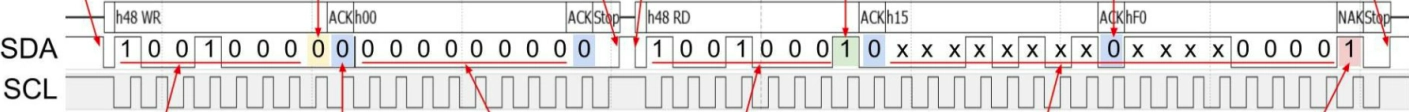
**Labview VI :**

The screen below is the start condition.

A screenshot of a computer program

Description automatically generated

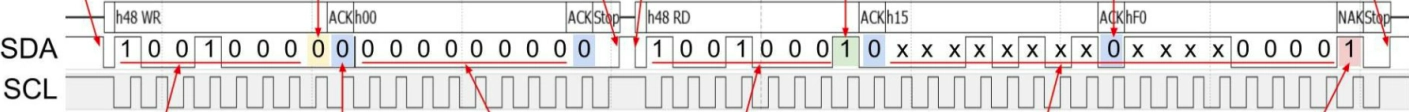
I framed in red the translation of the upper screen.



At the start the SDA and CLK are set to True, and on the second state we had a clock timer of 0,5s who set the SDA to false, who means that the frame is starting and after the second 0,5s clock timer the CLK is also set to false.

***Device address + write***

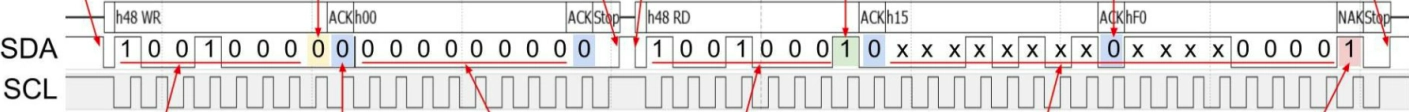
A screenshot of a computer

Description automatically generated

The address device is set to (50)10 = (00110010)2. On the other part of the VI screen we have the CLK function who altern between HIGH and LOW state.

This is the VI screen who correspond to the ACK bitA screenshot of a video game

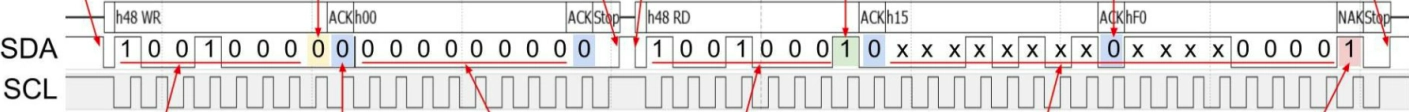
Description automatically generated



We change the state of SDA to enable so that we wait for an answer from the slave if the acknowledge is 0. If so, we carry on the next step.

***Register address***A screen shot of a computer

Description automatically generated

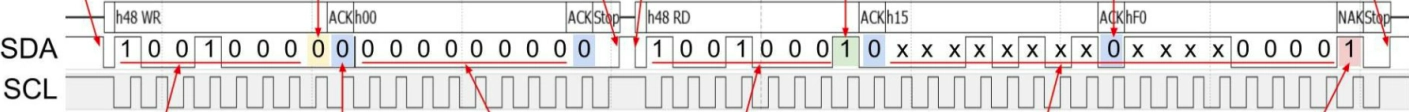


The default address for the register is (15)10 and once again we had the functionment of the CLK.

***Address device + read***

A screenshot of a computer

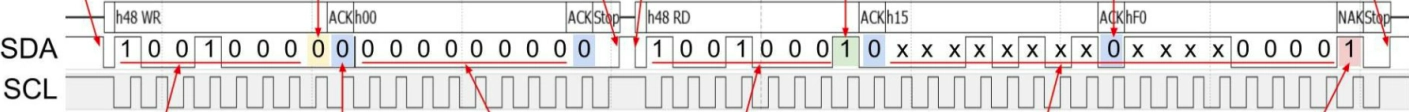
Description automatically generated



We had again the address device but we change the last bit here who is set to 1 which means it is a READ bit.

***Data read***

A screenshot of a computer

Description automatically generated

Thanks to that sequence we want to read the dummy register that is 51(10) and before that we need to change the state of SDA to enable again so that we wait the data that we need to read.

A close-up of a list

Description automatically generated