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A 0.18µm SOI BCD Technology for Automotive Application

Y. Hao, Sim. P.C, B. Toner, M. Frank[+], M. Ackermann[+], A. Tan, U. Kuniss[+], E. Kho, J. Doblaski[+], Hee. E.G, M. Liew, A. Hoelke, S. Wada[#] and T.Oshima[*]

X-FAB, Sarawak, Malaysia; [+]X-FAB, Erfurt, Germany;
[#]Central Research Laboratory, Hitachi Ltd., Japan; [*]Hitachi Automotive Systems, Japan
E-mail: yang.hao@xfab.com

***Abstract*—This paper presents a new SOI BCD technology at the 0.18µm node to fulfill the requirements for smart power IC technology targeted for automotive application. Built on a 1.8V and 5.0V CMOS core, there are 40V and 60V rated N/Pch MOS, with 25mΩ.mm^2 RonA/57V BVdss having been achieved for the 40V NMOS with excellent process stability. Depletion NMOS, LV&HV diodes, 5V zener diode, high gain BJT, excellent matching well resistor, capacitors, top thick Copper Metallization option, embedded memory (OTP, CEEPROM, etc.) are also offered on this comprehensive technology platform.**

INTRODUCTION

There are increasingly stringent requirements for smart power IC technology targeted for automotive application [1] [2]. Traditionally, there has been a strong emphasis on RonA reduction to reduce the foot print of power MOSFETs used in driver stages, while maintaining the safe operating area requirement, which includes HCI, electrical and thermal SOA [3]. For the harsh, high temperature environments often seen by automotive products, a robust CMOS platform is required. Furthermore, for precise analog circuits, high performance BJT and passive devices are a requirement. Both component level and system level ESD protection must also be ensured. All in all, a challenging list of requirements for any technology.

To fulfill this, a new SOI BCD technology at the 0.18µm node has been developed. Built on a 1.8V and 5.0V CMOS core, there are 40V and 60V rated N/Pch MOS, with 25mΩ.mm^2 RonA/57V BVdss having been achieved for the 40V NMOS with excellent process stability. Depletion NMOS, LV&HV diodes, 5V zener diode, high gain BJT, excellent matching well resistor, capacitors, top thick Copper Metallization option, embedded memory (OTP, CEEPROM, etc.) are also offered on this comprehensive technology platform.

SOI BCD TECHNOLOGY

The newly developed primitives were fabricated on X-FAB XT018 [4] process, using the same starting material and full oxide filling deep trench isolation, in order to complement the existing technology for automotive application. The process integration is done by introducing purely additional mask layer with implantation engineering and keeping the baseline process untouched. Furthermore, all of these new primitive devices are offered within a modular process (Fig.1) with flexibility combination and minimum mask count.

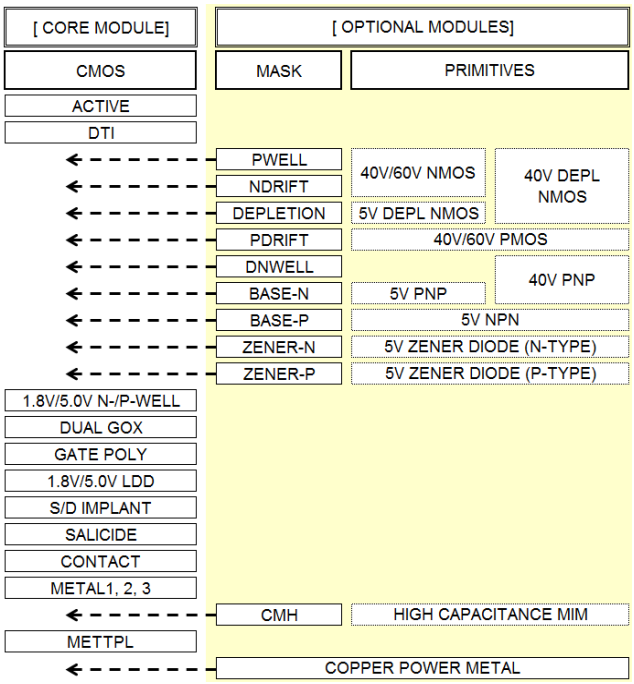


Fig.1 Simplified process flow (modular approach).

HV MOSFET DESIGN

Two additional masks were added to create the PWELL and NDRIFT regions for both 40V and 60V rated NMOS (Fig.2). RESURF (reduced surface electric field) engineering by both NDRIFT implantation and gate poly field plate design enables high drift doping which resulted in low RonA while maintaining a high breakdown voltage. Further RonA reduction was possible by pitch reduction in the source/drain and channel regions. Good HCI reliability was achieved by drift doping profile engineering without impact on other electrical parameters. By carefully designing the PWELL doping profile and adding the baseline 5V PWELL in the body region to make lower body resistance a wider electrical SOA is obtained. This also benefits the thermal SOA for large area Power MOS drivers. Further improvement of the thermal SOA

has been demonstrated by optimizing the top metal layout together with thick Copper metallization. A similar approach to the NMOS was utilized for the PMOS with 1 additional mask PDRIFT being used for both 40V and 60V rated PMOS (Fig.3).

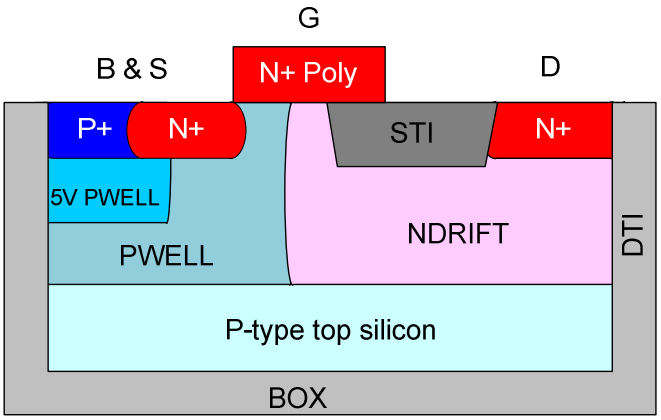


Fig.2 Schematic 40V & 60V NMOS. 2 dedicated mask PWELL & NDRIFT. 5V PWELL added in Body/Source region to improve on-state BV.

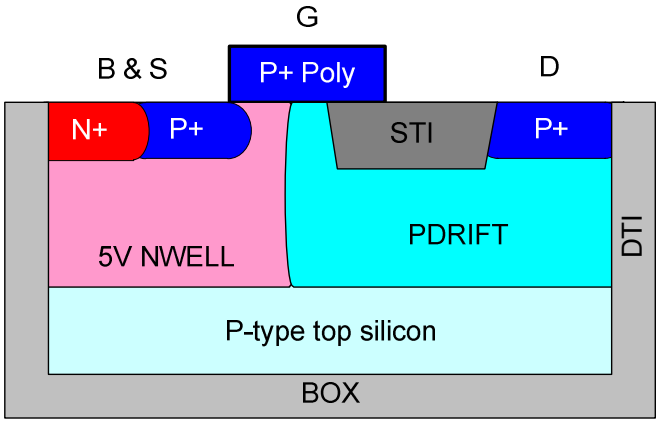


Fig.3 Schematic 40V & 60V PMOS, 1 dedicated mask - PDRIFT.

Experimental Result & Discussion

A . Electrical performance of Main devices

Table I lists the device (HV MOS, LV&HV diode, zener diode, depletion NMOS, resistor, capacitor) and their typical electrical performance. Additional devices are offered in the baseline XT018 process [4].

B. HV MOSFET

There are 2 versions of the HV MOSFET for the 40V node. First a low RonA HV NMOS, suitable as a large power MOSFET which can be self-protecting in the case of an ESD event. The second version, with enhanced ESD design window, provides sufficient electrical BVon(SOA) thereby allowing an ESD protection circuit in parallel (Fig.4). The drift length is the main parameter to adjust BVdss and BVon for different voltage ratings. Experimental results have also been shown for other voltage ratings, which will be released in a future development. The HV NMOSFET electrical performance can be found in Table II, except 127V BVdss device, which requires a dedicated/different N-type drift implant condition. All other devices share the same drift implant. The benchmarking data against the latest published data is shown in Fig.5 for NMOS. The low RonA version NMOS achieves state of the art RonA/BVdss tradeoff [2,5,6,7,8].

Table I: new primitive devices & electrical characteristics.

Primitive Devices		Parameters, Typical Value		
HV MOSs		RonA [mΩ.mm^2]	BVdss [V]	BVon [V] @ Vgs5V, 100ns TLP
40V NMOS[1]		25	57	52
40V NMOS[2]		51	70	80
60V NMOS[2]		100	90	90
40V PMOS[1]		99	61	69
40V PMOS[2]		150	83	82
60V PMOS[2]		248	102	100
40V DEPL NMOS[2]		Vth: -1V, RonA: 50mΩ.mm^2, BVdss: 70V		
Other Primitives				
5V DEPL NMOS		Vth: -1V, BVdss: 9.8V		
5V BJT	NPN	hFE: 80, V_A: 40V		
	PNP	hFE: 65, V_A: 65V		
40V PNP		hFE: 10, V_A: 1000V		
5V Zener Diode	P-type	BV: 5.3V		
	N-type	BV: 5.3V		
6V Forward Diode		VF: 0.72V, BV: 10V		
40V/60V Diode		BV: 70V/90V		
5V NWELL Resistor[3]		Rs: 470Ω/□, AR: 0.38 %.um		
MIM Capacitor[3]		CAA: 2.2fF/μm^2, AC: 0.52%.um		

[1] Low RonA version, [2] ESD design window version, [3] excellent matching version

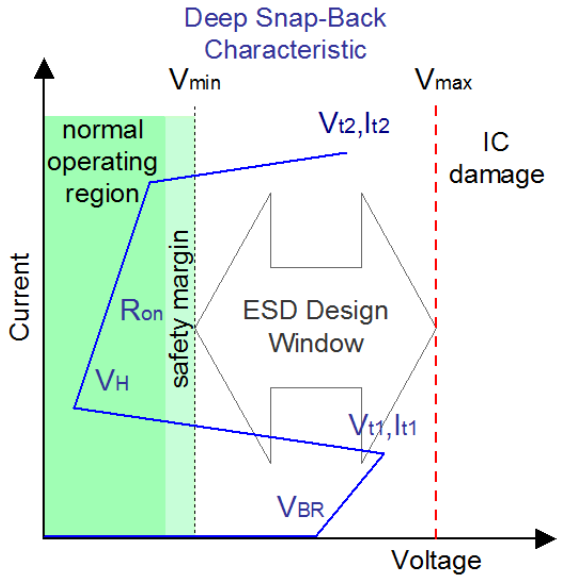


Fig.4 A 40V ESD NMOS provides sufficient Vt1 value, enabling parallel ESD protection when a smaller area HV MOSFET is used.

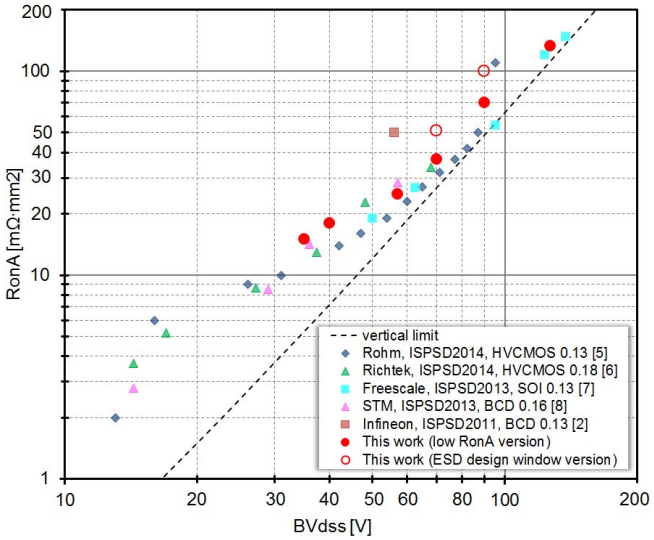


Fig.5 Benchmark data for HV NMOS. State of the art BVdss/RonA has been achieved for the low RonA version. The ESD design window version provides higher on-state BV at the expense of RonA.

Table II: a list of HV MOSFET BVdss/RonA result.

HV NMOS	BVdss [V]	RonA [mΩ.mm^2]
Low RonA Version	35	15
	40	18
	57	25
	70	37
	90	70
	127	133
ESD design window version	70	51
	90	100

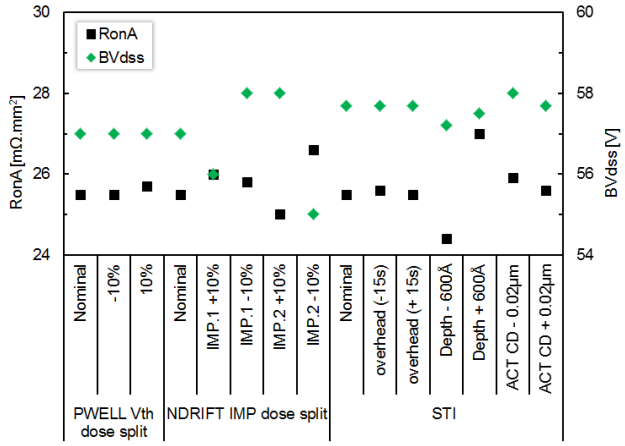


Fig.6 RonA & BVdss result for process boundary splits (40V low RonA NMOS).

Process robustness for HV MOSFETs has been studied, to cover (1) +/-10% dose split for each implant step of drift, (2) Vth implant split of PWELL and (3) STI CD/overhead/trench depth split.

Taking the 40V low Ron NMOS as an example, Fig.6 show BVdss & RonA against process boundary splits indicating good process stability, which also pertains to other HV MOSFETs in this technology.

Fig.7 show a typical 100ns TLP result for the 40V NMOS with ESD version, with no quasi-saturation up to 5V Vgs and providing about 80V BVon at 5V Vgs.

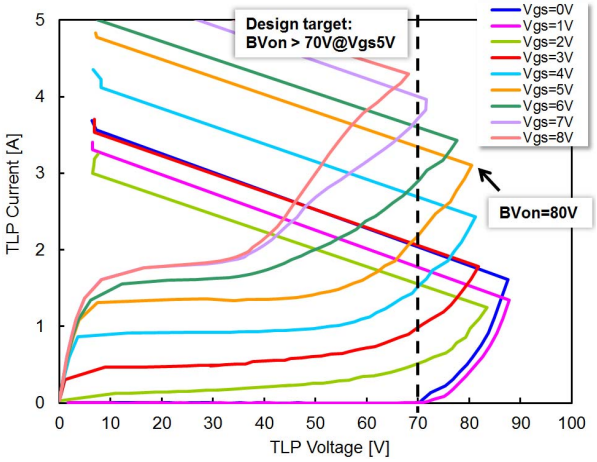


Fig.7 100ns TLP result for 40V NMOS with ESD design window.

By refining the drift doping profile, impact ionization has been reduced at the STI interface/bottom corner (Fig.8); consequently, more than 2 orders lifetime improvement is obtained, with no impact to other electrical parameters (Fig.9).

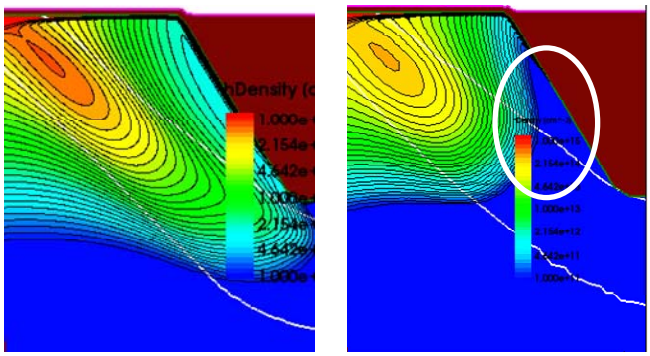


Fig.8 higher impact ionization generated hole concentration is observed in (a) with un optimized NDRIFT implant profile than in (b) with optimized one.

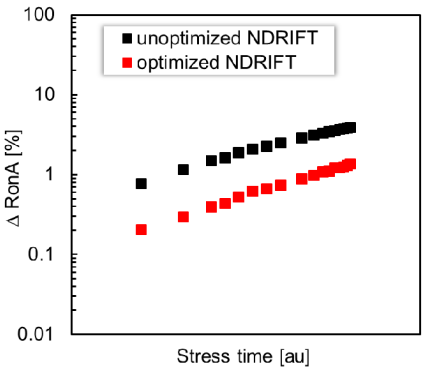


Fig.9 HCI results under worst case stress condition for 40V low RonA NMOS.

For many automotive applications, thermal SOA (energy capability) is an important design consideration. With metal layout optimization and thick copper metallization the junction temperature can be reduced, enabling more even thermal distribution which can improve thermal SOA performance for a µs to ms pulse which typically can be found in inductive switching event - refer to the ETHAN [9] electro-thermal simulation result in Fig. 10.

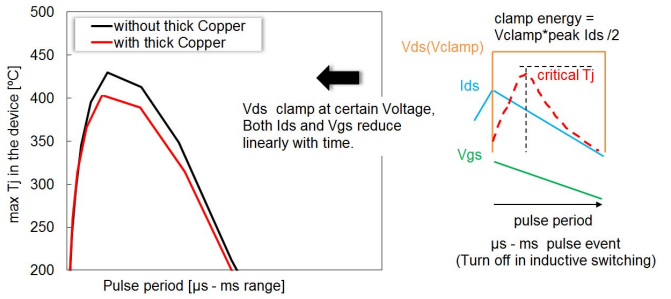
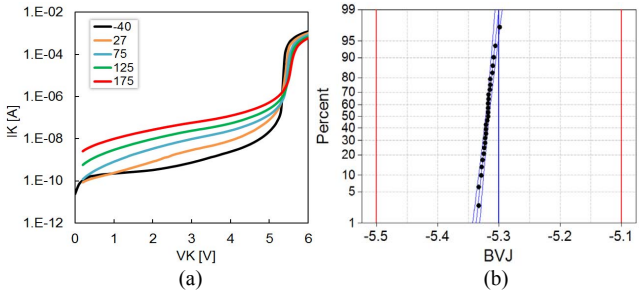


Fig.10 Electro-thermal simulation results shows the impact of metal layout & thick Copper top metal on the max junction temperature, a lower max Tj indicate a higher clamp energy can be gained.

C. Other Primitive Devices

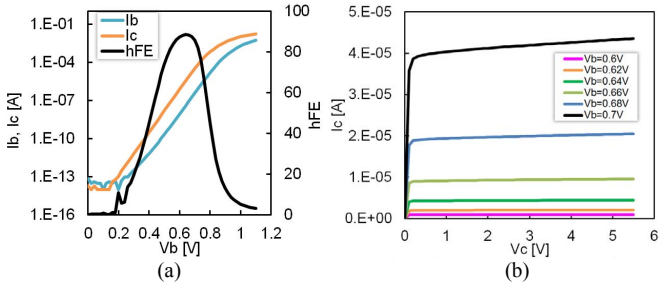
A 5V zener diode with very tight BV distribution and little sensitivity to temperature is shown in Fig.11. This is suitable for 5V gate oxide protection and as a trigger diode in ESD clamps.



(a) (b)

Fig.11 Off-state characterization for 5V Zener diode over temperatures (a) and BVJ distribution (b).

For precise analog design, high gain & early voltage is needed. By dedicated base implant engineering, over 80 hFE and 40V early voltage has been achieved (Fig.12).



(a) (b)

Fig.12 Gummel plot(a) and Vce-Ice plot(b) of 5V NPN. (device size: 10µm x2µm)

Fig.13 demonstrates TrimOTP passing 590hours Data Retention bake@250ºC; cell current of 21µA has large margin to the sensing amplifier limit of 8µA with excellent reliability.

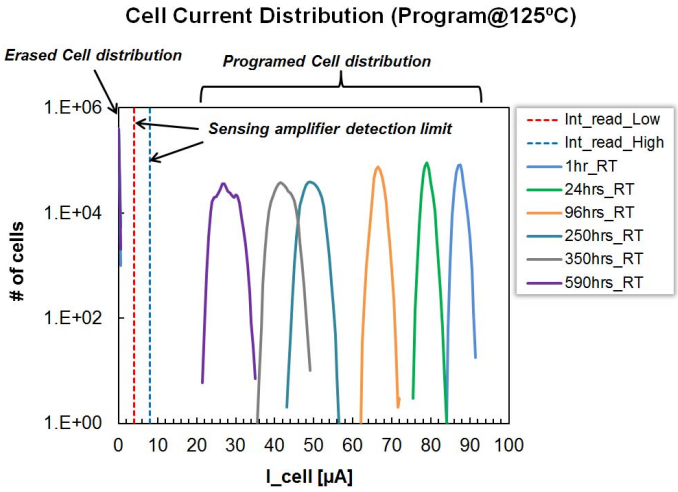


Fig.13 TrimOTP 590hours Data Retention bake@250ºC

CONCLUSION

A new SOI-BCD technology has been developed for automotive applications, including state of the art 40V NMOS and other high performance primitive devices. A comprehensive electrical and reliability evaluation has been performed for HV MOSFETs. The HV device design concept uses implantation engineering alone, with no impact to the baseline process platform. Voltage scalability with drift length has been demonstrated.

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