2-Channel Low-Power Wireless Scalp EEG System Analog Front End PCB Design

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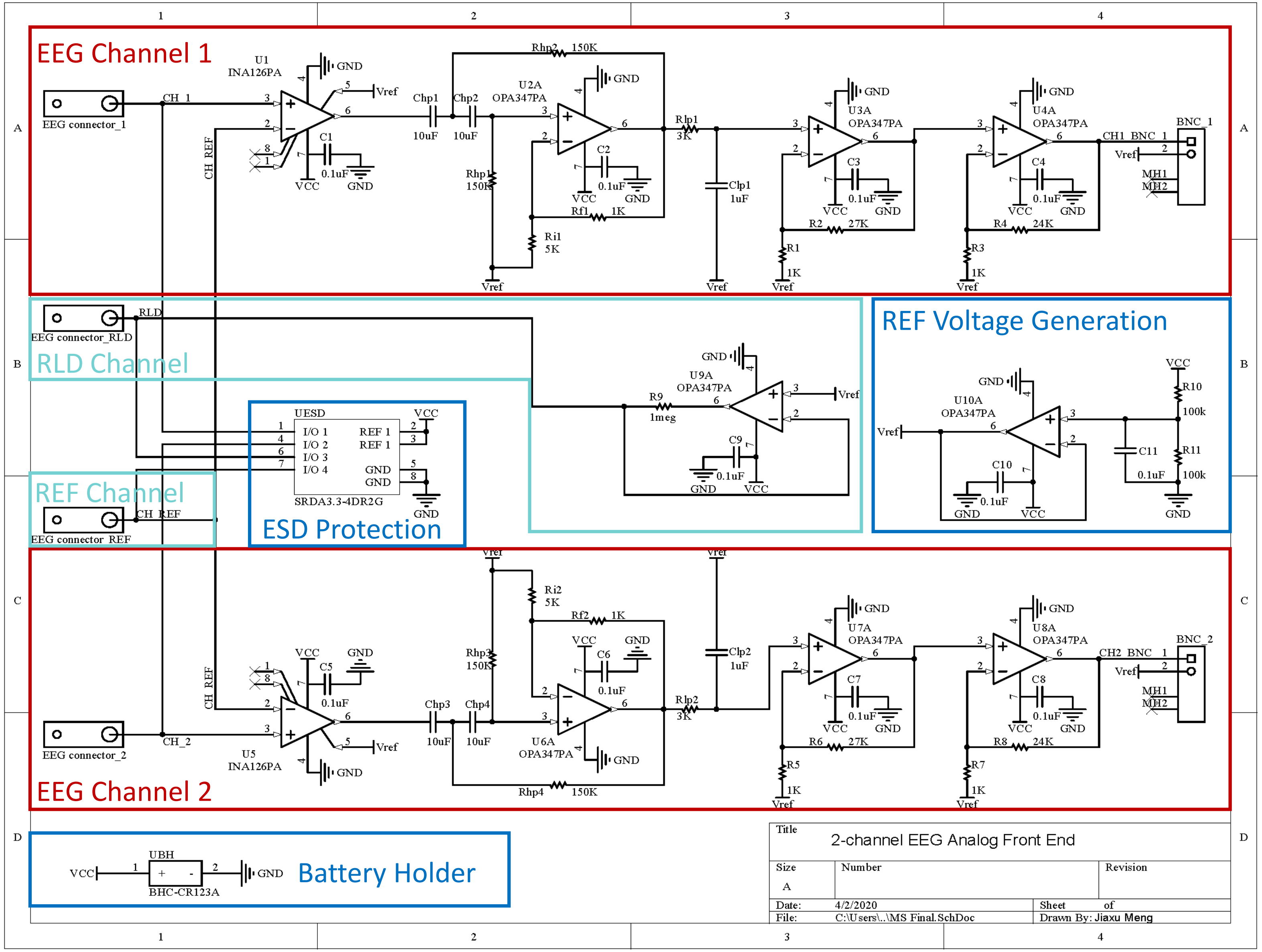
Full Schematic



2 EEG channels

- 1st stage: EEG signal acquisition
- 2nd stage: band pass filtering 0.1-50Hz
- 3rd and 4th stage: amplification
- Gain: 72.5dB (x4200)
- High input impedance
- High CMRR

Reference voltage

- single power supply: +3V battery
- rise subject’s baseline voltage up to +1.5V for signal integrity

RLD channel

- reduce Vcm: negative feedback
- safety: 1MΩ resistance in case of leakage

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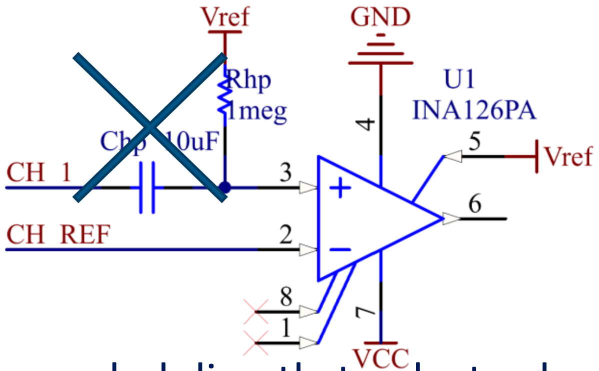
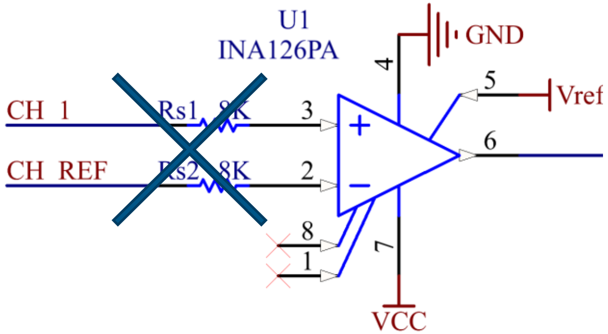
Signal Acquisition and Output

- EEG electrodes

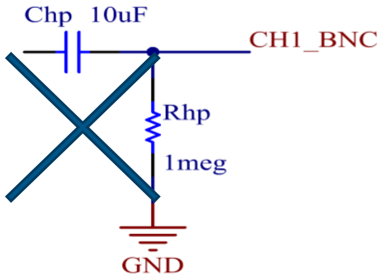


- coupled directly to electrodes



- compensation RES sacrifices Zin

- BNC

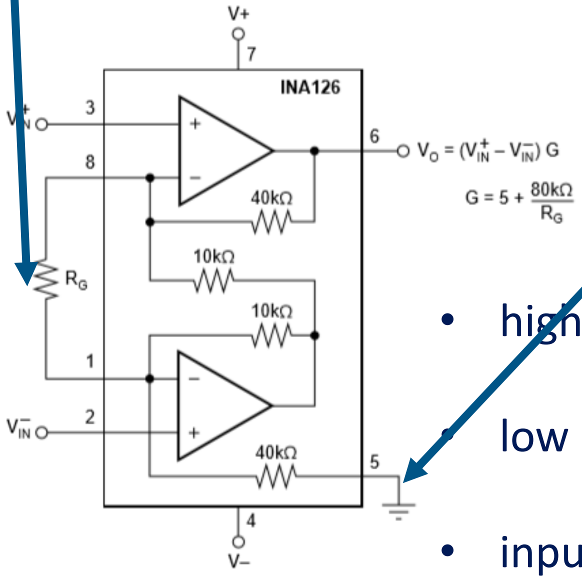


- NI ADC can use floating point

- INA126 circuitry

INA operates on Vref by feeding Vref voltage into pin5

Rg is open circuit → G = 5



- high CMRR
- low input bias current
- input buffering → high Zin
- adjustable differential gain by Rg

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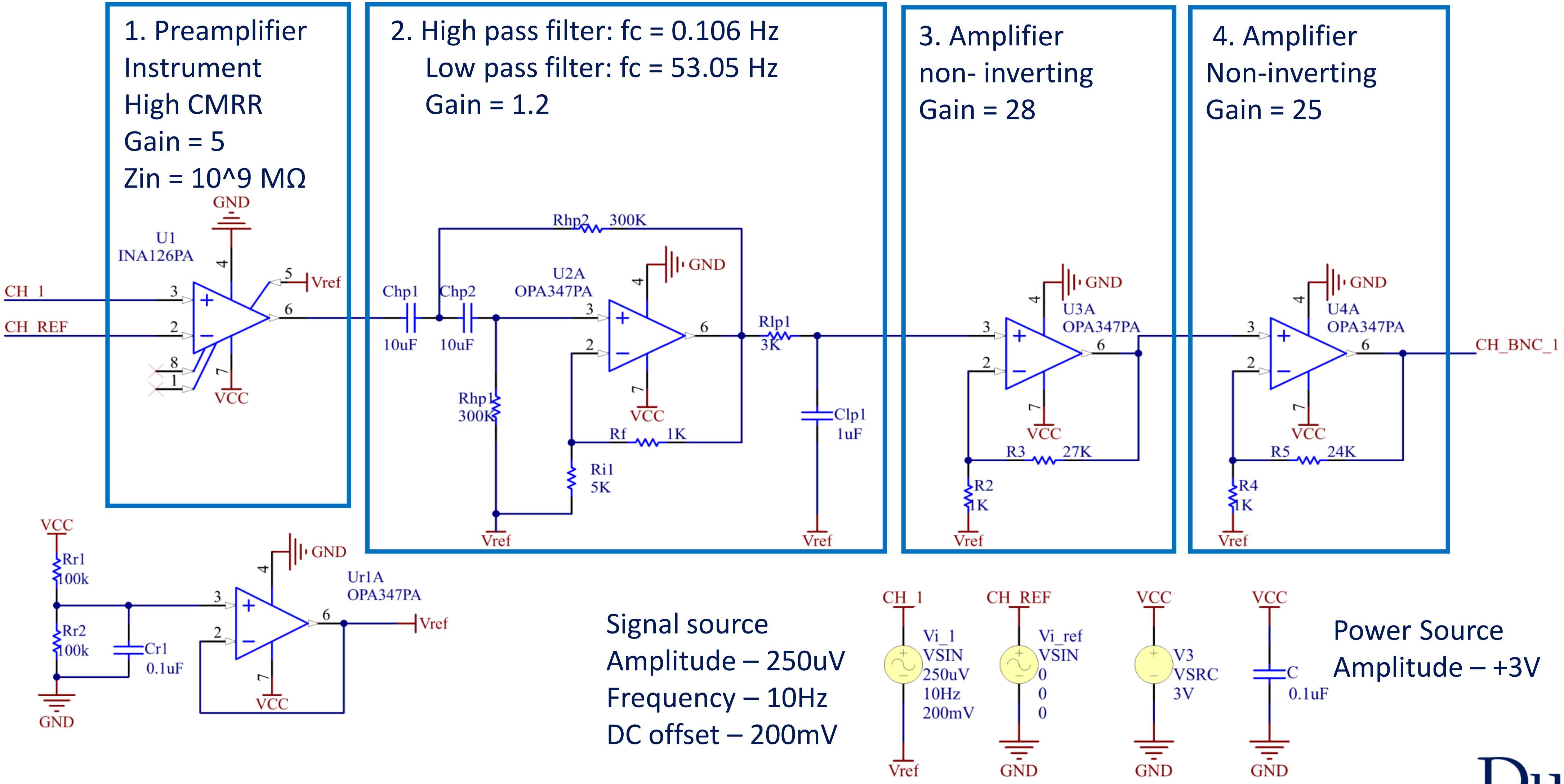
Schematic for Simulation



Signal source
Amplitude – 250uV
Frequency – 10Hz
DC offset – 200mV

Power Source
Amplitude – +3V

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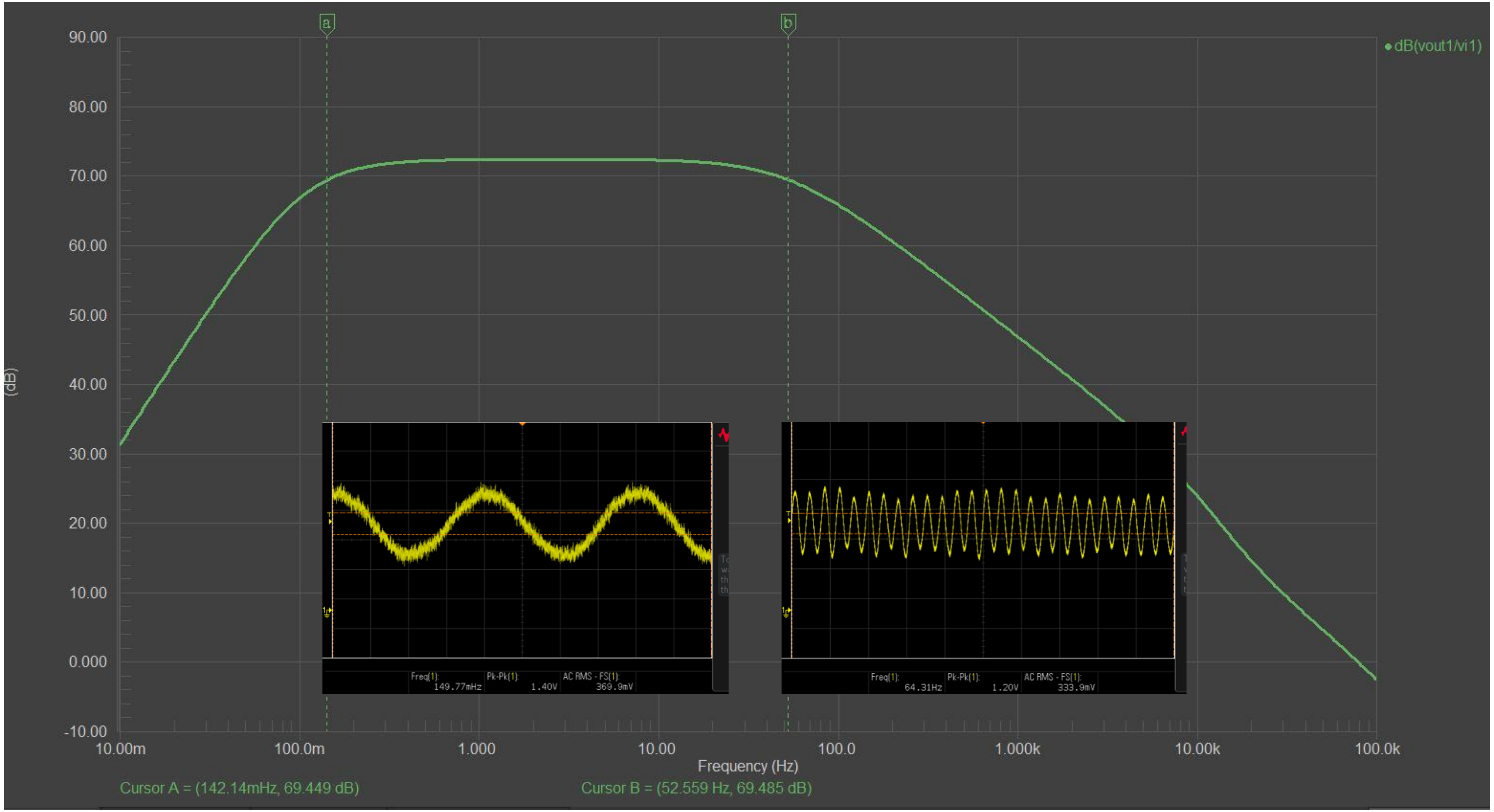
Simulation vs Bench Testing – Frequency Response

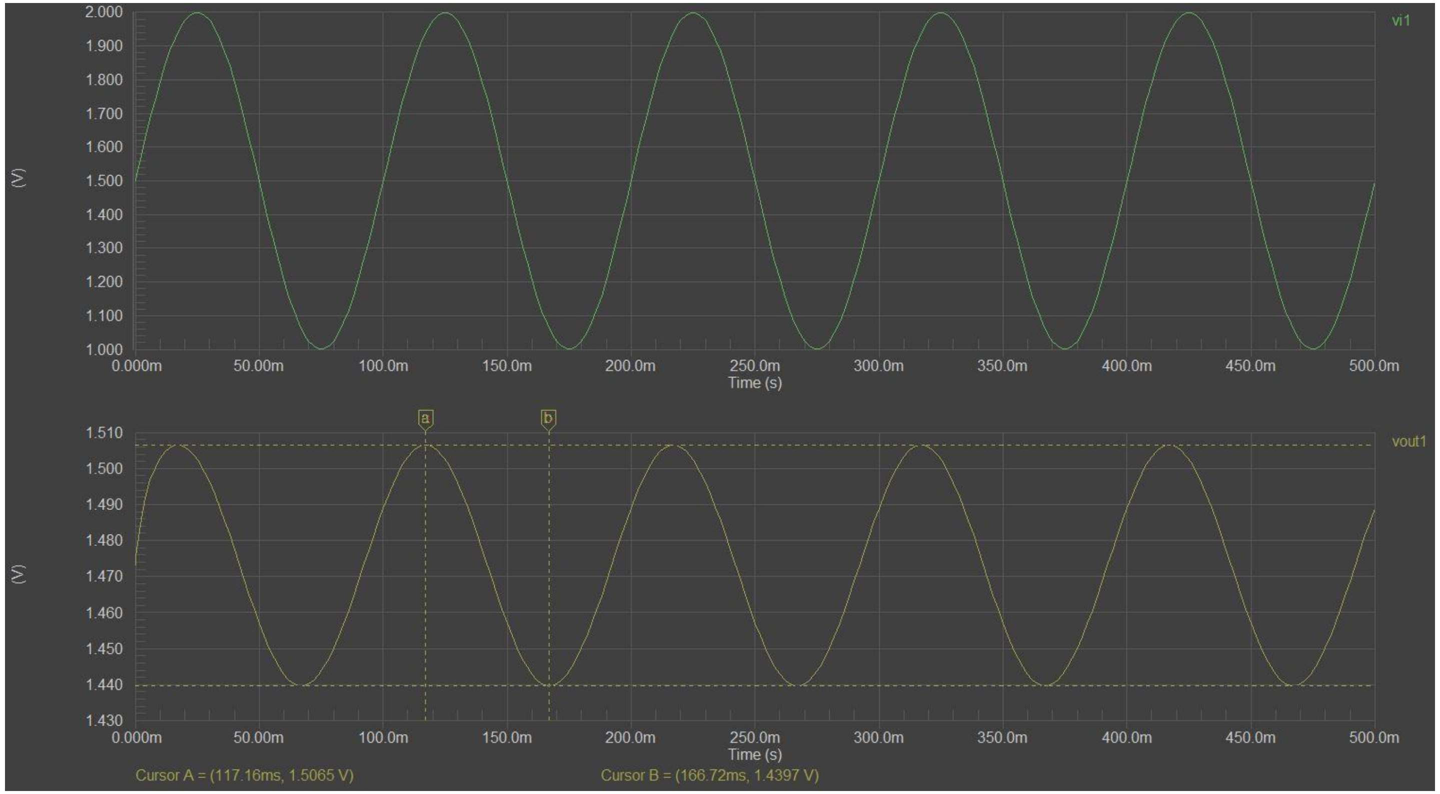


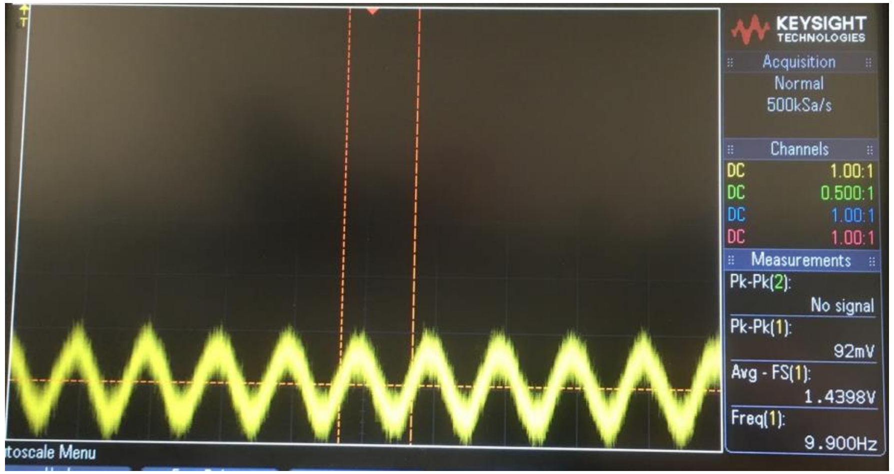
Method: The passband is obtained by manually adjusting input signal frequency until the output signal magnitude decreased by 3dB (became 0.707 times of Vout/Vi) through filtering stage

Simulation: passband is 0.071Hz – 53Hz

Bench Testing: passband is 0.15Hz – 64Hz

Simulation vs Bench Testing – CMRR





CMRR calculation:

Ad = 5 x 1.2 x 28 x 25 = 4200

Vcm_in = 500mV

Acm = $\frac{Vcm\_out}{Vcm\_in} = \frac{1.5065-1.4397}{1} = 0.0668$

CMRR = $20log\frac{Ad}{Acm} = 20log\frac{4200}{0.0668} = 96dB$

Method: Input a Vcm with magnitude of 500mV to both INA input pins and record the output signal for calculation

CMRR calculation:

Ad = 3860

Vcm_in = 500mV

Acm = $\frac{Vcm\_out}{Vcm\_in} = \frac{0.092}{1} = 0.092$

CMRR = $20log\frac{Ad}{Acm} = 20log\frac{3860}{0.092} = 92.45dB$

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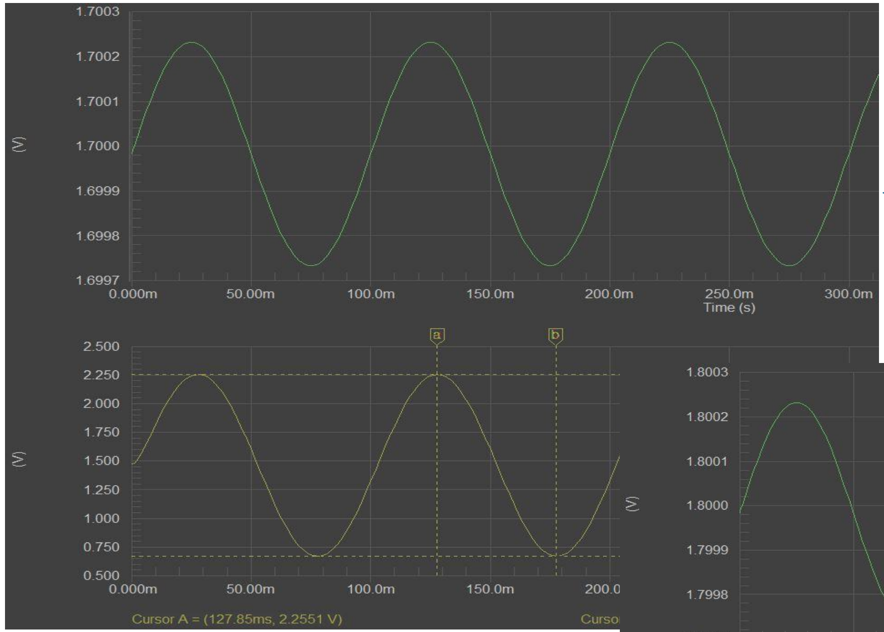
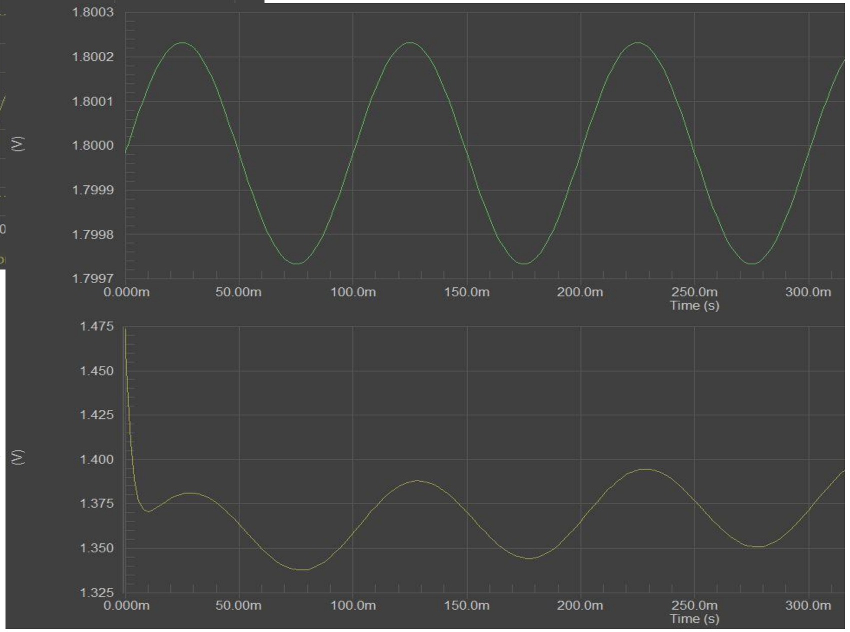
Simulation vs Bench Testing – DC Offset Tolerance

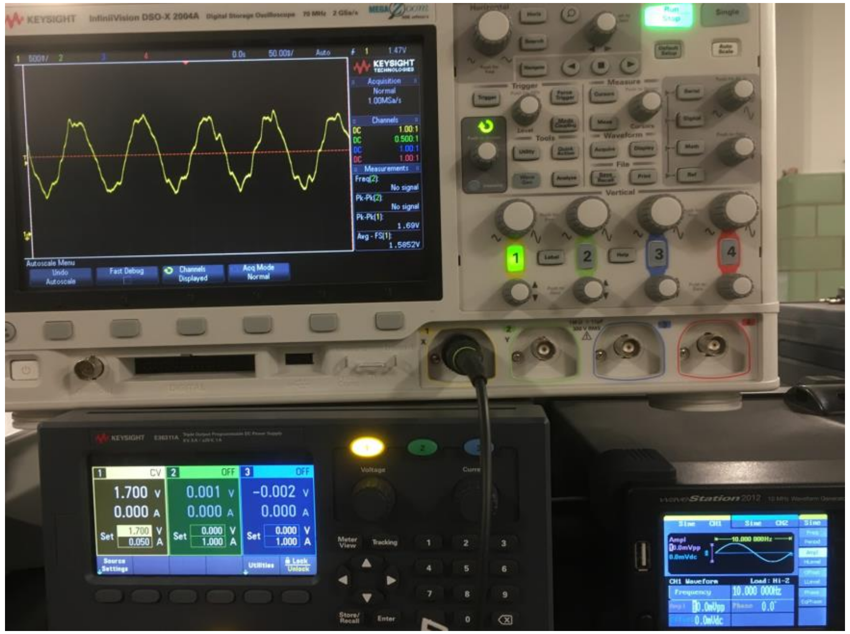


200 mV



300 mV

Simulation tolerance: +/-200 mV



Bench testing tolerance: +/-170 mV

Method: increase the amplitude of DC offset voltage on input signals until the output signal is distorted

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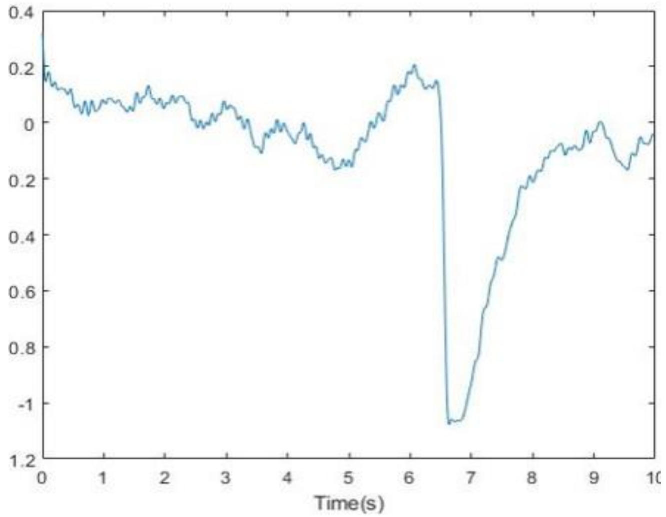
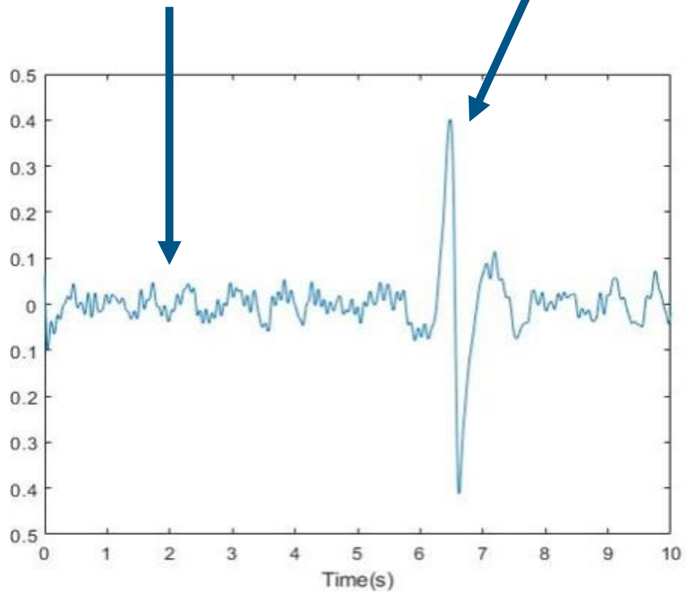
EEG Testing

higher frequency bands
beta and gamma

alpha rhythm





Raw EEG signal obtained from P300 speller BCI2000 system

Low pass filter with cut off frequency 10Hz

Band pass filter within 1 – 10Hz

Result

Specification	Design Value	Simulation Result	Measured Result
Gain	72.5dB = x4200	72.5dB = x4194	71.73dB = x3860
Noise (input-referred)	3.6 µV rms from 0.1 to 50 Hz	Max=0.228 µV rms	3.1 µV rms
Input voltage range	+/- 250 µV	+/- 250 µV	+/- 250 µV
High pass filter -3 dB	0.106 Hz	0.142 Hz	0.149 Hz
Low pass filter -3 dB	53.05 Hz	52.5 Hz	64.3 Hz
Input offset range	+/- 300 mV	+/- 200 mV	+/- 170 mV
Power consumption	33mW	5.96mW	120mW
CMRR (dB)	> 60 dB	96dB	92.45dB
Input Impedance	> 10 MΩ	10^9 MΩ	10^9 MΩ
Leakage Current	< 1 µA	0.12µA	0.02 µA
Distortion	< 1%	0.04%	

- Low pass filter should have lower cut off frequency
- Input offset range should be enlarged without sacrificing input impedance
- EEG testing for suddenly opening eyes in bright light

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