SM500 4-Bit Microcomputer (LCD Driver)

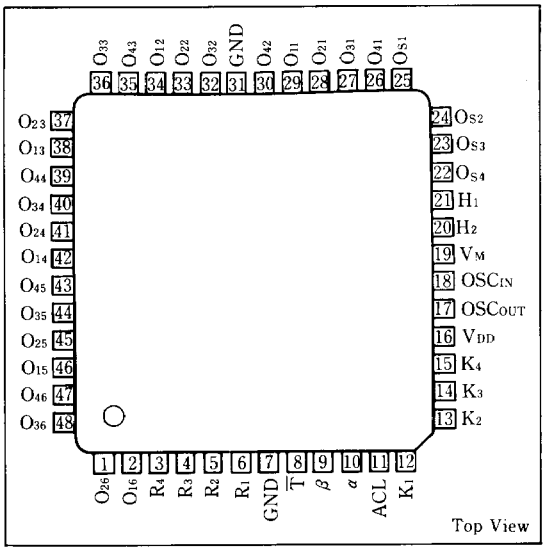
■ Description

The SM500 is a CMOS 4-bit microcomputer which integrates a 4-bit parallel processing function, a 1,197-byte ROM, a 40-word RAM, a 15-stage divider and a 56-segment LCD driver circuit in a single chip. This microcomputer is applicable to LCD systems with low power consumption and reduced cost.

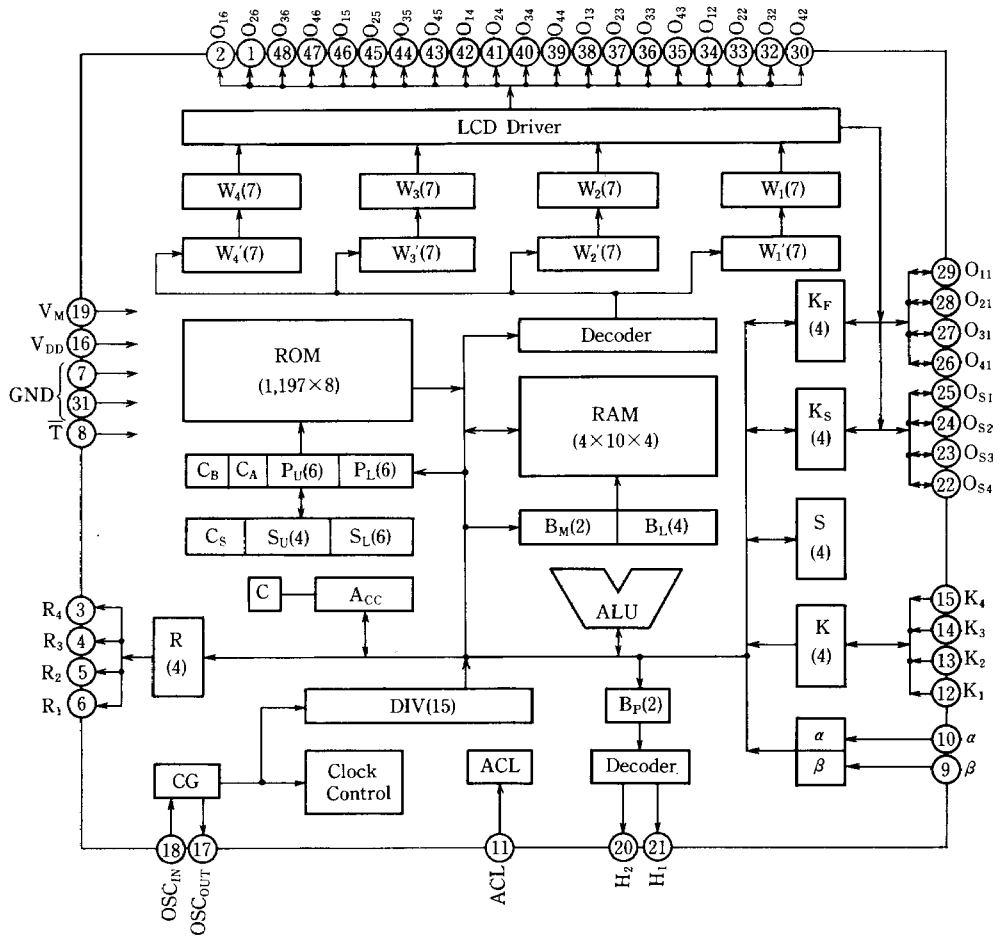
■ Features

1. CMOS process
2. ROM capacity: 1,197×8 bits
3. RAM capacity: 40×4 bits
4. Instruction set: 52
5. Subroutine nesting: 1 level
6. Instruction cycle: 61 μs (TYP.)
7. Input/output ports
   - I/O ports: 8
     (for switching with segment pin)
   - Input ports: 6
   - Output ports: 4
   - LCD output ports: 28 for segment
     (including 8 I/O ports)
     :2 for common
8. On-chip divider circuit for clock
9. On-chip crystal oscillator circuit
10. LCD driver circuit
    (56-segment, 1/2 bias, 1/2 duty)
11. Standby function
12. Single power supply: −3V or −5V (TYP.)
13. 48-pin QFP (QFP48-P-1010)

■ Pin Connections



■ Block Diagram



Symbol description

ALU	: Arithmetic logic unit	W_1-W_4, W_1'-W_4'	: Static shift register
Acc	: Accumulator	B_M, B_L	: RAM address register
ACL	: Auto clear	B_P	: Backplate signal generator circuit
C	: Carry F/F	K_F	: 4-bit F/F
C_A, C_B, P_U, P_L	: Program counter	K_S	: 4-bit F/F
C_S S_U, S_U	: Stack register of program counterr	S	: 4-bit F/F (status register)
CG	: Clock generator	K	: Key input F/F
DIV	: Frequency divider		

■ Pin Description

Symbol	I/O	Circuit type	Function
K_1-K_4	I	Pull down	Acc←K_1-K_4
α, β	I	Pull up	Independent test possible
O_{11}-O_{41}	I/O		W and W' registers output or input/output to/from K_F register
O_{S1}-O_{S4}	I/O		W and W' registers output or input/output to/from K_S register
O_{12}-O_{46}	O		W and W' registers output ; used for LCD segment output
H_1, H_2	O		3-state level output possible ; used for LCD common output
R_1-R_4	O		R_1-R_4←Acc
$\overline{T}$	I	Pull up	For test (Connected to GND normally)
ACL	I	pull down	Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_M			Power supply for LCD driver
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Pin voltage	V_{DD}	−6.0 to +0.3	V	1
	V_M	V_{DD} to +0.3	V	
	V_{IN}	V_{DD}−0.3 to +0.3	V	
	V_{OUT}	V_{DD}−0.3 to +0.3	V	
Operating temperature	Topr	−20 to +70	℃	
Storage temperature	Tstg	−55 to +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

(1) 3V power supply specification

(GND=0V)

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{DD}	−2.7 to −3.3	V	
	V_M	V_{DD}/2 (TYP.)	V	
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz	
Oscillation start voltage	V_{OSC}	−2.7	V	1

(2) 5V power supply specification

(GND=0V)

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{DD}	−4.5 to −5.5	V	
	V_M	V_{DD}/2 (TYP.)	V	
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz	
Oscillation start voltage	V_{OSC}	−4.5	V	1

Note 1: The oscillation start time should be within 10 sec.

■ Electrical Characteristics

(1) 3V power supply specification

($V_{DD}=-3.0V\pm10\%$, GND=0V, Ta=−20 to +70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.6			V	1
	V_{IL}				$V_{DD}+0.6$	V	
Input current	I_{H1}	$V_{IN}=0V$			15	μA	2
	I_{H2}	$V_{IN}=0V$			3	μA	3
	I_{L3}	$V_{IN}=V_{DD}$			1	μA	4
Output voltage	V_{OA}	No load $V_M=V_{DD}/2$	−0.3			V	5
	V_{OB}		$V_M-0.3$		$V_M+0.3$	V	
	V_{OC}				$V_{DD}+0.3$	V	
Output current	I_{OH1}	$V_{OUT}=-0.5V$	30			μA	6
	I_{OL1}	$V_{OUT}=V_{DD}+0.5V$	10			μA	
	I_{OH2}	$V_{OUT}=-0.5V$	100			μA	7
	I_{OL2}	$V_{OUT}=V_{DD}+0.5V$	10			μA	
	I_{O3}	$V_{DS}=0.3V$	100			μA	8
	I_{O4}	$V_{DS}=0.5V$	100			μA	9
Supply current	I_{DA}	During full-range operation		20		μA	10
	I_{DS}	When system clock is stationary		3		μA	

(2) 5V power supply specification

($V_{DD}=-5.0V\pm10\%$, GND=0V, Ta=−20 to +70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.6			V	1
	V_{IL}				$V_{DD}+0.6$	V	
Input current	I_{H1}	$V_{IN}=0V$			50	μA	2
	I_{H2}	$V_{IN}=0V$			10	μA	3
	I_{L3}	$V_{IN}=V_{DD}$			3	μA	4
Output voltage	V_{OA}	No load $V_M=V_{DD}/2$	−0.3			V	5
	V_{OB}		$V_M-0.3$		$V_M+0.4$	V	
	V_{OC}				$V_{DD}+0.4$	V	
Output current	I_{OH1}	$V_{OUT}=-0.5V$	35			μA	6
	I_{OL1}	$V_{OUT}=V_{DD}+0.5V$	12			μA	
	I_{OH2}	$V_{OUT}=-0.5V$	120			μA	7
	I_{OL2}	$V_{OUT}=V_{DD}+0.5V$	12			μA	
	I_{O3}	$V_{DS}=0.3V$	120			μA	8
	I_{O4}	$V_{DS}=0.5V$	120			μA	9
Supply current	I_{DA}	During full-range operation		50	100	μA	10
	I_{DS}	When system clock is stationary		10	30	μA	

Note 1: Applied to pins K_1-K_4, α, β, ACL, O_{11}, O_{21}, O_{31}, O_{41}, O_{S1}-O_{S4}
Note 2: Applied to pins K_1-K_4, O_{11}, O_{21}, O_{31}, O_{41}, O_{S1}-O_{S4}
Note 3: Applied to pin ACL
Note 4: Applied to pins α, β
Note 5: Applied to pins H_1, H_2
Note 6: Applied to pins O_{ij} (i=1 to 4, j=2 to 6)
Note 7: Applied to pins O_{11}−O_{41}, O_{S1}-O_{S4}
Note 8: Applied to pin R_1
Note 9: Applied to pins R_2, R_3, R_4
Note 10: $f_{OSC}=32.768kHz$, supply current with no load, oscillator circuit parameter: $C_D=C_G=22pF$

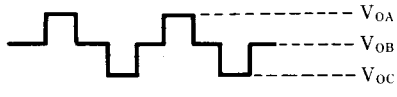


Fig. 1 H1, H2 waveforms

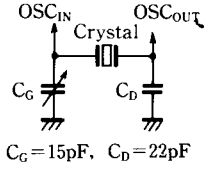


Fig. 2 Oscillator circuit

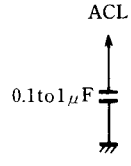


Fig. 3 ACL circuit

■ Pin Functions

(1) K_1-K_4 (Inputs)

The K_1-K_4 are 4-bit parallel input ports which are connected to the accumulator Acc. The contents of the K_1-K_4 are loaded into the A_{CC} by the KTA instruction.

When a system clock is inactivated, if a High level signal is input to any one bit of ports K_1-K_4, the system clock restarts, and the program counter starts at page 0, step 0.

(2) α, β (Inputs)

The input ports α and β can be independently tested by the TA and TB instructions respectively.

These ports are pulled-up to the High level within a chip.

(3) R_1-R_4 (Outputs)

The R_1-R_4 are 4-bit parallel output ports which generate the data stored in the R register.

The R register is connected to the accumulator A_{CC}. The contents of the Acc are loaded into the R register by the ATR instruction, which can be output at ports R_1-R_4.

The R_1 of the R register performs, in conjunction with the f_1, f_4 or f_{12} of a divider, the logical product. It can also provide an alarm output.

(4) H_2, H_1 (LCD common outputs)

The H_2 and H_1 pins are used to drive the common of an LCD with a 1/2 duty, 1/2 bias scheme, and provide a 3-level output.

The display can be turned on or off by the common outputs with the BP register.

(5) O_{ij} (Segment output ports)

The segment output ports O_{ij} (i=1 to 4, j=2 to 6) consist of 20 bits, which are used to output the contents of W′ and W registers for the display on or off with the BP register.

(6) O_{11}, O_{21}, O_{31}, O_{41} (Input/output ports)

The I/O ports O_{11}-O_{41} are used as segment output ports to generate the contents of W′ and W registers with the S register. The I/O ports can also be used as output ports as well as input ports for the K_F register. After ACL operation, it should be input ports with pull-down resistors.

(7) O_{S1}, O_{S2}, O_{S3}, O_{S4} (Input/output ports)

The I/O ports O_{S1}-O_{S4} are used as segment output ports to generate the contents of W′ and W registers with the S register. The I/O ports can also be used for output ports as well af input ports for the K_S register. After ACL operation, it should be input ports with pull-down resistor.

■ Hardware Configuration

(1) Program memory (ROM)

The on-chip ROM has 1,197 bytes organized as 19 pages×63 steps×8 bits. Fig. 1 shows the ROM configuration.

The program counter consists of a 1-bit C_A, C_B, a 4-bit page address counter P_U register and a 6-bit polynomial counter P_L (inhibit code: P_L= 111111).

The C_A is used to specify the field, the P_U for the page, P_L for the steps within a page and the C_B for the case where the field boundary is crossed.

(2) Data memory (RAM)

The data memory has 160 bits organized as 4×10×4 bits. Fig. 2 shows the RAM configuration.

The RAM address is specified by a 2-bit B_M register for the file specification, and a 4-bit B_L register for the word (4-bit) specification.

(3) Crystal oscillator and Divider (DIV)

The device contains a crystal oscillator circuit for the system clock and timer oscillator. A 16.384kHz system clock can be provided and 1 sec signal can be obtained from the final stage of a divider by connecting an external 32.768kHz crystal oscillator between the oscillator pins.

The divider consists of 15 stages, and lower 4 stages can be loaded into the accumulator by the DTA instruction. The lowest 9 stages (f_9-f_1) can be reset with the IDIV instruction or an ACL operation.

(4) Segment decoder

The SM500 contains an on-chip LCD driver which can directly drive an LCD with a 3V, 1/2 duty, 1/2 bias scheme. The device also contains a segment decoder which helps the software to be reduced.

The truth table of a segment decoder is shown in Fig. 5, the LCD segments relative to the decoder shown in Fig. 4, and the LCD driving signal waveform shown in Fig. 6. The display characters other than those described in Fig. 5 are available by directly setting data to W′ with the WR or WS instruction.

(5) Standby mode

The SM500 is a low power consumption design due to CMOS process. For further low power requirement, executing the CEND instruction places the device in standby mode. To reduce power consumption, the system clock is inactivated.

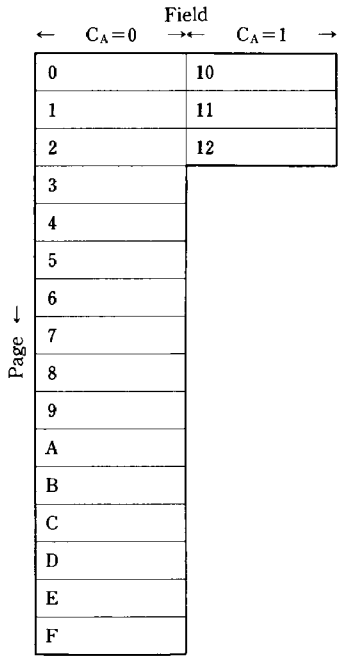


Fig. 1 ROM configuration

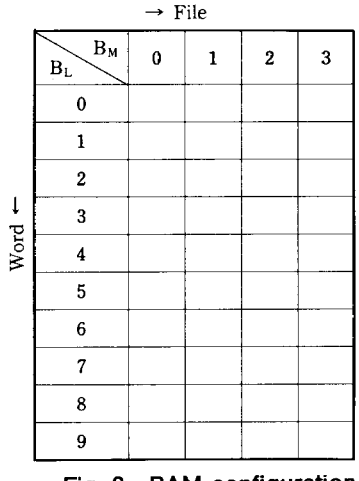


Fig. 2 RAM configuration

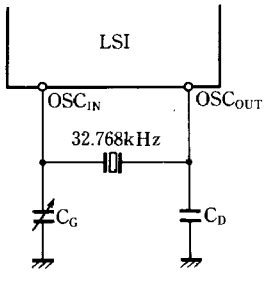


Fig. 3 Crystal oscillator circuit

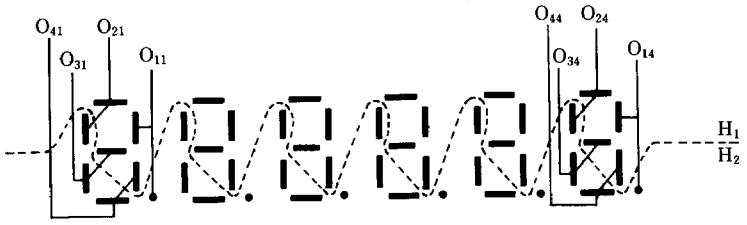


Fig. 4 LCD segment layout for segment decoders

While in standby mode, if more than one input of K_1-K_4 goes High, or γ F/F is reset, the device exits its standby mode and starts execution of the program at address 0000 (C_A=0, P_U=0, P_L=0).

(6) Reset function

Connecting a capacitor between the ACL pin and the GND activates the ACL circuit when it is powered up. The ACL is cleared in about 0.5 sec from a crystal oscillator circuit starts oscillation after power on, and starts execution of the program at C_A=0, P_U=F_H, P_L=0.

While in power on, applying a High level signal to the ACL pin activates the ACL operation. However, it takes about 0.5 sec to start execution of the program after the ACL goes Low. The lowest 9 stages of a divider are reset during the ACL goes High.

Acc	Display character	Acc	Display character
0	0	6	6
1	1	7	7
2	2	8	8
3	3	9	9
4	4	A	–
5	5	B	Blank

Fig. 5 Display decoder truth table

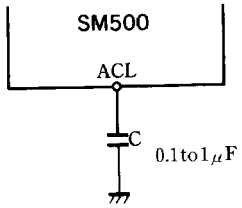


Fig. 7 ACL external circuit

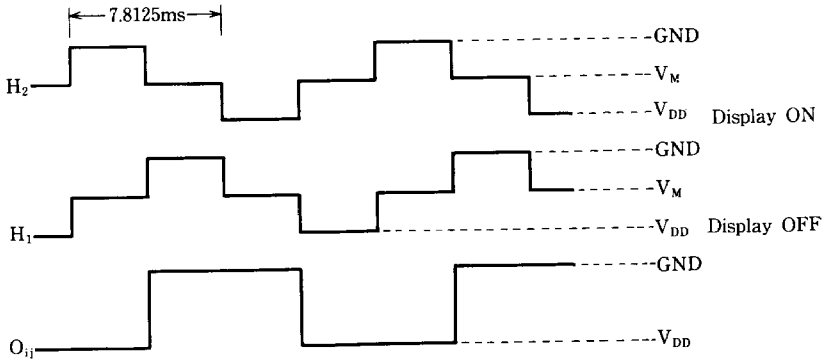


Fig. 6 LCD driving signal waveforms

■ Instruction Set

(1) RAM address instructions

Mnemonic	Machine code	Operation
LB xy	40-4F	$B_L \leftarrow x\ (I_3, I_2)$, $B_M \leftarrow y\ (I_1, I_0)$
LBL xy (2 step)	5F 00-FF	$B_M \leftarrow x\ (I_5, I_4)$, $B_L \leftarrow y\ (I_3, I_0)$
EXBLA	0B	$Acc \leftrightarrow B_L$
INCB	64	$B_L \leftarrow B_L + 1$, Skip if $B_L = 7$
DECB	6C	$B_L \leftarrow B_L - 1$, Skip if $B_L = 0$

(2) ROM address instructions

Mnemonic	Machine code	Operation
COMCB	6D	$C_B \leftarrow \overline{C_B}$
RTN	6E	$C_A \leftarrow C_S$, $P_U \leftarrow S_U$, $P_L \leftarrow S_L$, $R \leftarrow 0$
RTNS	6F	$C_A \leftarrow C_S$, $P_U \leftarrow S_U$, $P_L \leftarrow S_L$ $R \leftarrow 0$, skip the next step
SSRx	70-7F	$S_U \leftarrow x\ (I_3\text{-}I_0)$, $E \leftarrow 1$ next step only
TRx	80-BE	if $R = 0$; $P_L \leftarrow X\ (I_5\text{-}I_0)$, $P_U \leftarrow S_U$, $C_A \leftarrow C_B$ if $R = 1$; $P_L \leftarrow I_5\text{-}I_0$
TRSx	C0-FF	if $R = 0$, $E = 0$; $P_L \leftarrow x\ (I_5\text{-}I_0)$ $P_{U3} \leftarrow 1$, $P_{U2}\text{-}P_{U0} \leftarrow 0$, $S_L \leftarrow P_L + 1$, $S_U \leftarrow P_U$, $C_S \leftarrow C_A \leftarrow 0$, $R \leftarrow 1$ if $R = 0$, $E = 1$; $P_L \leftarrow x\ (I_5, I_0)$, $P_U \leftrightarrow S_U$, $S_L \leftarrow P_L + 1$, $C_S \leftarrow C_A \leftarrow C_B$, $R \leftarrow 1$
TRSAxy	C0-FF	if $R = 1$; P_{U1}, $P_{U0} \leftarrow x\ (I_5, I_4)$ $P_{L3}\text{-}P_{L0} \leftarrow y\ (I_3\text{-}I_0)$, P_{L5}, $P_{L4} \leftarrow 0$

(3) Arithmetic instructions

Mnemonic	Machine code	Operation
ADD	08	$Acc \leftarrow Acc + M$
ADDC	09	$Acc \leftarrow Acc + M + C$, $C \leftarrow C_Y$, Skip if $C_Y = 1$
ADX x	31-3F	$Acc \leftarrow Acc + x\ (I_3\text{-}I_0)$ Skip if $C_Y = 1$ No skip if $I_3I_2I_1I_0 = 1010$ (30 defines inhibit)
COMA	0A	$Acc \leftarrow \overline{Acc}$

(4) Data transfer instruction

Mnemonic	Machine code	Operation
EXCx	10-13	$Acc \leftrightarrow M$, $B_M \leftarrow B_M \oplus x\ (I_1, I_0)$
EXCIx	14-17	$Acc \leftrightarrow M$, $B_M \leftarrow B_M \oplus x\ (I_1, I_0)$ $B_L \leftarrow B_L + 1$, Skip if $B_L = 7$
EXCDx	1C-1F	$Acc \leftrightarrow M$, $B_M \leftarrow B_M \oplus x\ (I_1, I_0)$ $B_L \leftarrow B_L - 1$, Skip if $B_L = 0$
LAXx	20-2F	$Acc \leftarrow x\ (I_3\text{-}I_0)$
LDAx	18-1B	$Acc \leftarrow M$, $B_M \oplus x\ (I_1, I_0)$
ATBP	03	$B_P \leftarrow Acc$
PTW	59	$W_{i6} \leftarrow W'_{i6}$, $W_{i5} \leftarrow W'_{i5}$ (i = 1 to 4)
PDTW	61	$W'_{15} \leftarrow W'_{16} \leftarrow DEC_i$ (i = 1 to 4)
TW	5C	$W_{ij} \leftarrow W'_{ij}$ (i = 1, j = 0 to 6)
DTW	5D	$W'_{i6} \leftarrow DEC_i$ W'_{ij} write shift (i = 1 to 4, j = 0 to 6)
WR	62	$W'_{46} \leftarrow 0$, $W'_{36} \leftarrow Acc_2$, $W'_{26} \leftarrow Acc_1$ $W'_{16} \leftarrow Acc_0$, W'_{ij} write shift (i = 1 to 4, j = 0 to 6)
WS	63	$W'_{46} \leftarrow 1$, $W'_{36} \leftarrow Acc_2$ $W'_{26} \leftarrow Acc_1$, $W'_{16} \leftarrow Acc_0$ W'_{ij} write shift (i = 1 to 4, j = 0 to 6)

(5) I/O control instructions

Mnemonic	Machine code	Operation
ATR	01	$R \leftarrow Acc$
KTA	6A	$Acc \leftarrow K$
ATS	30	$S \leftarrow Acc$
EXKSA	02	if $S_2 = 1$; $Acc \leftarrow K_S$ if $S_2 = 0$; $K_S \leftarrow Acc$
EXKFA	6B	if $S_4 = 1$; $Acc \leftarrow K_F$ if $S_4 = 0$; $K_F \leftarrow Acc$

(6) Divider manipulation instructions

Mnemonic	Machine code	Operation
DTA (2 step)	5E 04	$Acc_3 \leftarrow f_1$, $Acc_2 \leftarrow f_2$ $Acc_1 \leftarrow f_3$, $Acc_0 \leftarrow f_4$
IDIV	65	$f_9\text{-}f_1 \leftarrow 0$

(7) Bit manipulation instructions

Mnemonic	Machine code	Operation
RMx	04-07	$Mx \leftarrow 0$
SMx	0C-0F	$Mx \leftarrow 1$
RMF	68	$m' \leftarrow 0$, $Acc \leftarrow 0$
SMF	69	$m' \leftarrow 1$
COMCN	60	$C_N \leftarrow \overline{C_N}$
RC	66	$C \leftarrow 0$
SC	67	$C \leftarrow 1$

(8) Test instructions

Mnemonic	Machine code	Operation
TA	50	Skip if $\alpha = 1$
TB	51	Skip if $\beta = 1$
TC	52	Skip if C=0
TAM	53	Skip if Acc=M
TMx	54-57	Skip if Mx=1
TG	58	Skip if $\gamma = 0$, $\gamma \leftarrow 0$
TA0	5A	Skip if Acc=0
TABL	5B	Skip if Acc=B_L

(9) Clock control instruction

Mnemonic	Machine code	Operation
GEND	5E	clock stop
(2 step)	00	

(10) Special instruction

Mnemonic	Machine code	Operation
SKIP	00	No operation

■ System Configuration Example (Digital watch)