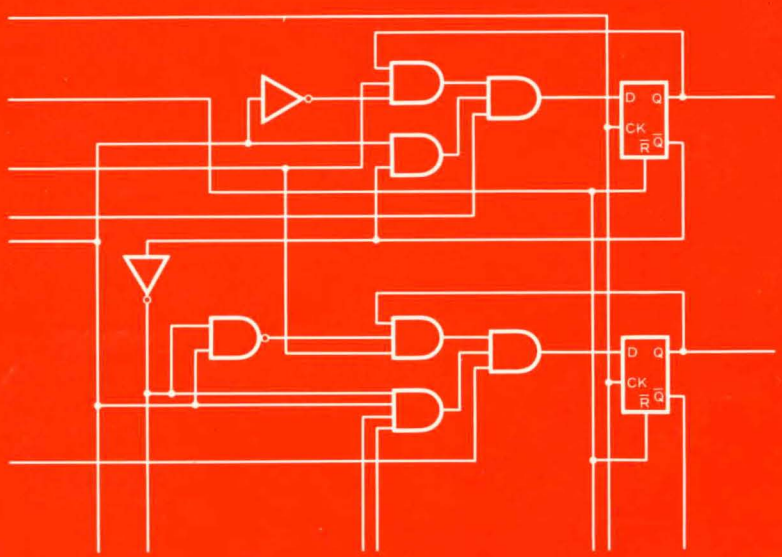
SHARP

1986

SEMICONDUCTOR DATA BOOK

MOS



SHARP CORPORATION

SEMICONDUCTOR DATA BOOK
(MOS Edition)

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Preface

In recent years, the seemingly unlimited progress seen in integrated circuits technology has brought about phenomenal growth in electronic products for consumer and industrial use. As electronics continues to expand in the future, we will direct our efforts at carefully researching trends and supplying our customers with products that meet their needs and contribute to the betterment of their way of life.

We have now completed the "Sharp Semiconductor Data Book —— MOS Edition", which we present to you here now.

This data book lists the microcomputers, memories and MOS LSIs produced and sold by Sharp, which have a wide range of applicability. We hope you will find this data book useful and will contact Sharp if you have any questions.

The information contained in the databook is intended to be a general product description. Sharp reserves the right to make change in specifications at any time and without notice.

Sharp does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied.

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General Information

Products Lineup

■ 4-Bit 1-Chip Microcomputer

Model	Process	Cycle time. (μs)	Supply voltage (V)	Current consumption TYP.(mA) [operating]	Instructions	ROM (bit)	RAM (bit)	Sub-routine nesting	Package	Remarks	Page
SM-3A	PMOS	10	−15	12	57	2268×8	128×4	2	60QFP	External RAM expandable	36
SM-100		10	−9	10	58	1134×8	64×4	2	28DIP		40
SM-105		10	−9	10	58	1134×8	64×4	2	28DIP		40
SM-110		10	−9	13	90	2032×9	128×4	6	60QFP	8-bit A/D conversion	44
SM-115		10	−9	13	90	2032×9	128×4	6	60QFP	8-bit A/D conversion	44
SM-111		10	−9	13	90	4064×9	192×4	6	60QFP	8-bit A/D conversion	49
SM-116		10	−9	13	90	4064×9	192×4	6	60QFP	8-bit A/D conversion	49
SM-114		10	−9	20	90	4064×9	192×4	6	60QFP	8-bit A/D conversion Remote control signal receiver	54
SM-120		10	−9	20	54	1536×8	64×4	2	44QFP	External ROM	59
SM-200	NMOS	10	−5	32	100	3072×9	128×4+16	3	60QFP	External ROM/REM Automatic display circuit	64
SM-4A	CMOS	61	−3	0.05	54	2268×8	96×4	1	60QFP	External RAM	69
SM-5A		61	−3	0.05	51	1827×8	65×4	1	60QFP		74
SM-5L		61	−3	0.05	51	1827×8	65×4	1	60QFP		79
SM-500		61	−2	0.02	52	1197×8	40×4	1	48QFP		84
SM-510		61	−3	0.06	49	2772×8	128×4	2	60QFP		89
SM-511		61	−3	0.04	55	4032×8	128×4	2	60QFP	Melody generator circuit	93
SM-520		11	−5	1.5	93	3072×10	160×4+16×2	4	64DIP	External RAM Automatic display circuit	98
SM-525		11	−5	0.6	93	3072×10	160×4+16×2	4	64DIP	External RAM Automatic display circuit	103
SM-530		91.6	−1.5	0.012	49	2016×8	88×4	1	80QFP	Clock counter circuit Melody generator circuit	108
SM-531		91.6	−1.5	0.01	45	1260×8	52×4	1	60QEP	Clock counter circuit Melody generator circuit	113
SM-540		16	−4.5	0.23	57	2016×8	128×4	2	60QFP	Dot matrix	118
SM-550		1.6	3~5	1	94	1024×8	80×4	using RAM area	48QFP	8-bit serial I/O function	123
SM-555		3.3	3~5	1	94	1024×8	80×4	using RAM area	48QFP	8-bit serial I/O function	123
SM-551		1.6	3~5	1	94	2048×8	128×4	using RAM area	60QFP	8-bit serial I/O function	128
SM-556		3.3	3~5	1	94	2048×8	128×4	using RAM area	60QFP	8-bit serial I/O function	128

(Continued)

SM-552	CMOS	1.6	3~5	1	94	4096×8	256×4	using RAM area	60QFP	8-bit serial I/O function	133
SM-557		3.3	3~5	1	94	4096×8	256×4	using RAM area	60QFP	8-bit serial I/O function	133
SM-5E3		1.6	3~5	1	97	4096×8	256×4	using RAM area	80QFP	8-bit serial I/O function	138
SM-563		6.6	3~5	0.4	93	4096×8	128×4+32×4	using RAM area	64QFP	8-bit serial I/O function	139
SM-572		2	3~5	1.5	93	2032×9	128×4	6	64QFP	8-bit A/D conversion	144
SM-578		2	3~5	1.5	94	4064×9	192×4	6	64DIP 64QFP	8-bit A/D conversion 8-bit Serial I/O function	150
SM-579		2	3~5	1.5	94	6096×9	256×4	6	64DIP 64QFP	8-bit A/D conversion 8-bit serial I/O function	151
SM-590		2	3~5	0.5	41	508×8	32×4	4	20DIP	16DIP, 18DIP	152
SM-591		2	3~5	0.5	41	1016×8	56×4	4	20DIP	16DIP, 18DIP	156

■ 8-Bit 1-Chip Microcomputer

Model	Cycle time MIN. (μs)	Supply voltage (V)	Current consumption MAX.(mA)	I/O pins	ROM (bit)	RAM (bit)	Package	Remarks	Page
LH0801	1.5	5±5%	180	32	2,048×8	144×8	40DIP	Z8601MCU	166
LH0802	1.5	5±5%	180	32	—	144×8	64DIP	Z8602MPD	180
LH0803	1.5	5±5%	180	32	—	144×8	40PBP	Z8603MPE	182
LH0811	1.5	5±5%	180	32	4,096×8	144×8	40DIP	Z8611MCU	184
LH0812	1.5	5±5%	180	32	—	144×8	64DIP	Z8612MPD	186
LH0813	1.5	5±5%	180	32	—	144×8	40PBP	Z8613MPE	189
LH0881	1.5	5±5%	180	24	—	144×8	40DIP	Z8681MCU	191

■ 8-Bit CMOS 1-Chip Microcomputer

Model	Cycle time MIN. (μs)	Supply voltage (V)	Current consumption MAX.(mA)	I/O pins	ROM (bit)	RAM (bit)	Package	Remarks	Page
SM-803	2.2	5±10%		32	4,096×8	144×8	40DIP 44QFP	—	195
SM-812	1	3~5		48	2,048×8	128×8	64DIP 64QFP	—	198
SM-813	1	3~5		48	4,096×8	192×8	64QFP 64DIP	—	201
LU810V1	1	3~5		48	—	128×8	64QFP 64DIP	—	204

■ 8-Bit Microprocessor and Peripheral LSIs

Function	Model	Process	Supply voltage (V)	Current consumption MAX.(mA)	Clock fequency (MHz)	Package	Remarks	Page
CPU	LH0080	NMOS	5±5%	150	2.5	40DIP	Z80 CPU	210
	LH0080A			200	4		Z80A CPU	210
	LH0080B			200	6		Z80B CPU	210
Parallel input/output controller	LH0081	NMOS	5±5%	100	2.5	40DIP	Z80 PIO	235
	LH0081A				4		Z80A PIO	235
	LH0081B				6		Z80B PIO	235
Counter / Timer controller	LH0082	NMOS	5±5%	120	2.5	28DIP	Z80 CTC	245
	LH0082A				4		Z80A CTC	245
	LH0082B				6		Z80B CTC	245
DMA controller	LH0083	NMOS	5±5%	150	2.5	40DIP	Z80 DMA	255
	LH0083A			200	4		Z80A DMA	255
Serial input/output controller	LH0084	NMOS	5±5%	100	2.5	40DIP	Z80 SIO/0	270
	LH0084A				4		Z80A SIO/0	270
	LH0084B				6		Z80B SIO/0	270
	LH0085			100	2.5	40DIP	Z80 SIO/1	270
	LH0085A				4		Z80A SIO/1	270
	LH0085B				6		Z80B SIO/1	270
	LH0086			100	2.5	40DIP	Z80 SIO/2	270
	LH0086A				4		Z80A SIO/2	270
	LH0086B				6		Z80B SIO/2	270
Floppy disk controller	LH0110	NMOS	5±5%	170	2.5	40DIP	—	279
	LH0110A			180	4		—	279
CPU	LH5080	CMOS	5±10%	10(TYP.)	2.5	40DIP	—	296
	LH5080L				2.5		—	296
	LH5080LM				2.5	44QFP	—	296
Parallel input/output controller	LH5081	CMOS	5±10%	2(TYP.)	2.5	40DIP	—	302
	LH5081L				2.5		—	302
	LH5081LM				2.5	44QFP	—	302
Counter/Timer controller	LH5082	CMOS	5±10%	2.5(TYP.)	2.5	28DIP	—	307
	LH5082L				2.5		—	307
	LH5082LM				2.5	44QFP	—	307

■ 16-Bit Microprocessor and Peripheral LSIs

Function	Model	Process	Supply voltage (V)	Current consumption MAX.(mA)	Clock fequency (MHz)	Package	Remarks	Page
CPU	LH8001	NMOS	5±5%	320	4	48DIP	Z8001 CPU	314
	LH8001A				6		Z8001A CPU	314
	LH8002			320	4	40DIP	Z8002 CPU	314
	LH8002A				6		Z8002A CPU	314
Memory control unit	LH8010	NMOS	5±5%	300	4	48DIP	Z8010 MMU	332
	LH8010A				6		Z8010A MMU	332
Serial communication controller	LH8030	NMOS	5±5%	250	4	40DIP	Z8030 SCC	342
	LH8030A				6		Z8030A SCC	342
Counter/Timer parallel input/output unit	LH8036	NMOS	5±5%	200	4	40DIP	Z8036 CIO	356
	LH8036A				6		Z8036A CIO	356
FIFO input/output interface unit	LH8038	NMOS	5±5%	200	4	40DIP	Z8038 FIO	377
	LH8038A				6		Z8038A FIO	377
FIFO buffer unit and Z-FIFO expander	LH8060	NMOS	5±5%	200	4	28DIP	Z8060 FIFO	396
Serial parallel combination controller	LH8071	NMOS	5±5%	250	4	40DIP	—	402
	LH8072						—	413
GPIB controller	LH8073	NMOS	5±5%	250	4	40DIP	—	421
Multitask support processor	LH8075	NMOS	5±5%	250	4	40DIP	—	423
Universal peripheral controller	LH8090	NMOS	5±5%	250	4	40DIP	Z8090 UPC	434
	LH8090A				6		Z8090A UPC	434
	LH8091	NMOS	5±5%	250	4	64DIP	Z8091 development device	451
	LH8091A				6		Z8091A development device	451
	LH8092			250	4	64DIP	Z8092 development device	453
	LH8092A				6		Z8092A development device	453
	LH8093	NMOS	5±5%	250	4	40PBP	Z8093 protopack emulator	455
	LH8093A				6		Z8093A protopack emulator	455
	LH8094	NMOS	5±5%	250	4	40PBP	Z8094 protopack emulator	457
	LH8094A				6		Z8094A protopack emulator	457

■ Peripheral LSIs for Microcomputers

Function	Model	Process	Supply voltage (V)	Current consumption MAX.(mA)	Clock fequency (MHz)	Package	Remarks	Page
Serial communication controller	LH8530	NMOS	5±5%	250	4	40DIP	Z8030 SCC	460
	LH8530A				6		Z8030A SCC	460
Counter/Timer parallel input/output unit	LH8536	NMOS	5±5%	200	4	40DIP	Z8036 CIO	474
	LH8536A				6		Z8036A CIO	474
Serial parallel combination controller	LH8571	NMOS	5±5%	250	4	40DIP	—	491
	LH8572	NMOS	5±5%	250	4	40DIP	—	502
GPIB controller	LH8573	NMOS	5±5%	250	4	40DIP	—	511
Multitask support processor	LH8575	NMOS	5±5%	250	4	40DIP	—	513
	LH8590	NMOS	5±5%	250	4	40DIP	Z8090 UPC	525
	LH8590A				6		Z8090A UPC	525
	LH8591	NMOS	5±5%	250	4	64DIP	Z8091*1	542
	LH8591A				6		Z8091A*1	542
	LH8592	NMOS	5±5%	250	4	64DIP	Z8092*1	544
	LH8592A				6		Z8092A*1	544
Universal peripheral controller	LH8593	NMOS	5±5%	250	4	40PBP	Z8093*2	546
	LH8593A				6		Z8093A*2	546
	LH8594	NMOS	5±5%	250	4	40PBP	Z8094*2	548
	LH8594A				6		Z8094A*2	548
Key-encoder and data transmitter receiver	LH8661	NMOS	5±5%	180	8	40DIP	—	550

*1 Development device
*2 Protopack emulator

■ Microcomputer Development Support System

Model	Function	Page
LH8DH110	Development Support System SM-D-8000 II; SM Series Z8, Z80, Z8000 development device	562
LH8DH130	Development Support System SM-D-8100; Z8, Z80, Z8000 development device	564
LH8DH140	Development Support System SM-D-8200; Z8, Z80, Z8000 development device	566
LH8DH312	Z80B In-circuit Emulator, for SM-D-8000 II	569
LH8DH321	Z8 In-circuit Emulator II, Stand-alone type	571
LH8DH330	Z8000 Evaluation Board, Stand-alone type	572
LH8DH340	Z8000 In-circuit Emulator SM-E-8100, Stand-alone type	573
LH8DH403	PROM Writer SM-E-8000 II	575
LU4DH200	SM Series Emulator Device SME-20, Stand-alone type	576
LUXXXH2	SM Series Evaluation Board	578

■ Mask ROM

Capacity (bit)	Model	Process	Bit composition (bit)	Access time MAX.(ns)	Cycle time MIN.(ns)	Supply voltage (V)	Power consumption MAX.(mW)	Package	Remarks	Page
32K	LH2331	NMOS	4,096×8	450	450	5±5%	580	24DIP		582
	LH2331A			350	350					582
	LH2332			450	450					586
	LH2332A			350	350					586
64K	LH2362B	NMOS	8,192×8	250	250	5±5%	840	24DIP		590
	LH2367			250	250		420	28DIP		594
	LH5366A	CMOS		2,500	4,000	5±10%	30	44QFP		599
	LH5366S			6,000	12,000	3±0.5V	3.5			602
	LH5367			450	750	5±5%	60			605
96K	LH5396	CMOS	12,288×8	6,000	7,500	4.5±0.5V	35	44QFP		608
	LH5396A			3,000	4,500		60			608
	LH5396S			15,000	18,000	3±0.4V	10			612
128K	LH23126	NMOS	16,384×8	250	250	5±10%	440	28DIP		615
	LH53127	CMOS		250	350	5±10%	44	28DIP		618
	LH53129			6,000	7,500	4.5±0.5V	35	44QFP		622
	LH53129A			2,500	3,500	5±10%	80			626
256K	LH23257	NMOS	32,768×8	250	250	5±10%	440	28DIP		630
	LH53256	CMOS		800	900		55	44QFP		634
	LH53257			250	250		165	28DIP		638
512K	LH53512	CMOS	65,536×8	3,000	4,400	5±1V	9	24SOP		642
1M	LH531000	CMOS	131,072×8	80	—	5	—	28DIP		646
1.2M	LH53012 Series	CMOS	103,680×12	250	250	5	—	40DIP		647

■ EPROM

Capacity (bit)	Model	Process	Bit composition (bit)	Access time MAX.(ns)	Cycle time MIN.(ns)	Supply voltage (V)	Power consumption MAX.(mW)	Package	Remarks	Page
64K	LH5764J-20	CMOS	8,192×8	200	——	5±10%	150	28DIP (Ceramic)		650
	LH5764J-25			250	——					650
	LH5764J-30			300	——					650
	LH5764J-45			450	——					650
128K	LH57128J-20	CMOS	16,384×8	200	——	5±10%	150	28DIP (Ceramic)		651
	LH57128J-25			250	——					651
	LH57128J-30			300	——					651
	LH57128J-45			450	——					651
256K	LH57256J-20	CMOS	32,768×8	200	——	5±10%	150	28DIP (Ceramic)		652
	LH57256J-25			250	——					652
	LH57256J-30			300	——					652
	LH57256J-45			450	——					652

■ Static RAM

Capacity (bit)	Model	Process	Bit composition (bit)	Access time MAX.(ns)	Cycle time MIN.(ns)	Supply voltage (V)	Power consumption MAX.(mW)	Package	Remarks	Page
1K	LH5101-30	CMOS	250×4	300	300	5±10%	140	22DIP		653
	LH5101-45			450	450					653
	LH5101			800	800	5±5%	145			658
	LH5101L3			650	650					658
	LH5101S			3,000	3,500	3±0.4V	45			662
	LH5101W			800	800	5±10%	150			666
2K	LH5102	CMOS	512×4	1,200	1,200	5±5%	145	22DIP		670
	LH5102-8			800	900					670
	LH5102W			1,200	1,200	5±10%	150			675
4K	LH2114L-20	NMOS	1,024×4	200	200	5±10%	400	18DIP		680
	LH5114-4	CMOS		450	450		110			684
	LH5104-4	CMOS	4,096×1	450	450	5±10%	85	18DIP		688
16K	LH5116-15	CMOS	2,048×8	150	150	5±10%	220	24DIP	18 pin $\overline{CS}$	693
	LH5116-20			200	200				20 pin $\overline{OE}$	693
	LH5117-15			150	150				18 pin $\overline{CE_2}$	698
	LH5117-20			200	200				20 pin $\overline{CE_1}$	698
	LH5118-15			150	150				18 pin $\overline{CE_2}$	703
	LH5118-20			200	200				20 pin $\overline{CE_1}$	703

■ Dynamic RAM

Capacity (bit)	Model	Process	Bit composition (bit)	Access time MAX.(ns)	Cycle time MIN.(ns)	Supply voltage (V)	Power consumption MAX.(mW)	Package	Remarks	Page
64K	LH2164-15	NMOS	65,536×1	150	270	5±10%	248	16DIP		708
	LH2164-20			200	330					708
	LH2164A-15			150	260		275			717
	LH2164A-20			200	330					717
256K	LH2464-10	NMOS	65,536×4	100	——	5±10%	267.5	18DIP		726
	LH2464-12			120	——				Page mode	726
	LH2464-15			150	——					726
	LH2465-10			100	——					726
	LH2465-12			120	——				Nibble mode	726
	LH2465-15			150	——					726
	LH21256-10	NMOS	262,144×1	100	200	5±10%	467.5	16DIP		728
	LH21256-12			120	230		440		Page mode	728
	LH21256-15			150	260		385			728
	LH21257-10			100	200		467.5			728
	LH21257-12			120	230		440		Nibble mode	728
	LH21257-15			150	260		385			728
	LH21258-10			100	200		467.5			728
	LH21258-12			120	230		440		Byte mode	728
	LH21258-15			150	260		385			728

■ Tone Dialer

Model	Process	Power supply voltage(V)	Operating current TYP.(mA)	Oscillating frequency (MHz)	Oscillater	Tone output	Mute output	Remarks	Package	Page
LR4087	CMOS	3.5～10	1	3.58	Crystal	bipolar output	Complementary		16DIP	732
LR4089	CMOS	3.0～10	1	3.58	Crystal	bipolar output	N-channel open drain		16DIP	735
LR4091	CMOS	3.0～10	1	3.58	Crystal	bipolar output	N-channel open drain	Op amplifier output	18DIP	738
LR4092	CMOS	3.5～10	1	3.58	Crystal	bipolar output	Complementary		16DIP	741

■ Pulse Dialer

Model	Process	Power supply voltage(V)	Operating current MAX.(mA)	Oscillating frequency (kHz)	Oscillator	Make rate (%)	Pluse ratio (pps)	Pluse output	Mute output	Remarks	Package	Page
LR40981A	CMOS	2.5～6	0.15	480	Ceramic	33/39	10	Positive	Negative		16DIP	744
LR40982	CMOS	2.5～6	0.15	480	Ceramic	33/39	10	Negative	Negative		16DIP	748
LR40991	CMOS	2.5～6	0.15	4	CR	34/40	10/20	Negative	Positive		18DIP	752
LR40992	CMOS	2.5～6	0.15	4	CR	34/40	10/20	Negative	Negative		18DIP	756
LR40993	CMOS	2.5～6	0.15	4	CR	34/40	10/20	Negative	Negative	Key signal	18DIP	760
LR40994	CMOS	2.5～6	0.15	4	CR	34/40	10/20	Negative	Negative	Key signal	18DIP	764

■ Pulse / Tone Dialer

Model	Process	Power supply voltage(V)	Operating current TYP.(mA)	Oscillating frequency (MHz)	Oscillator	Make rate (%)	Pluse ratio (pps)	Abbrevication memory	Redical function	Package	Page
LR4801D	CMOS	2～6	2	3.58	Crystal	40	10/20	18 digits ×9 stations	18 digit last number	18DIP	768
LR4802	CMOS	2～6	2	3.58	Crystal	32	10/20	18 digits ×9 stations	18 digit last number	18DIP	773
LR4803	CMOS	2～6	2	3.58	Crystal	40	10/20	18 digits ×9 stations	18 digit last number	18DIP	778
LR4804	CMOS	2～6	2	3.58	Crystal	40	10/20	——	32 digit last number	20DIP	783
LR4805	CMOS	2～6	1	3.58	Crystal	32	10/20	——	32 digit last number	20DIP	788
LR4806B	CMOS	2～6	1	3.58	Crystal	33/37	10/20	16 digits ×20 stations	32 digit last number	28DIP	793

■ MOS IC / LSI

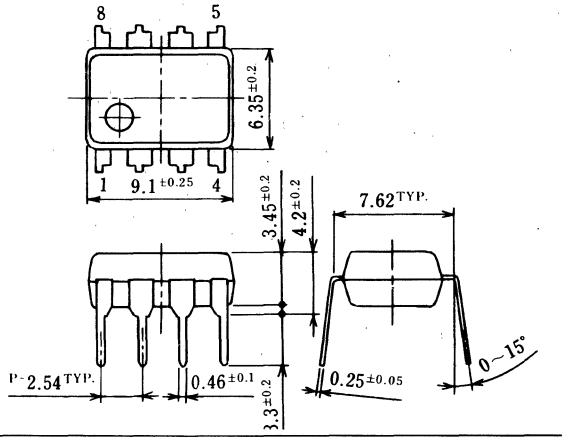
Function	Model	Process	Features	Package	Page
Driver	LH5010	CMOS	6-circuit signal non-inversion type, INHIBIT input	16DIP	908
	LH5011	CMOS	6-circuit signal inversion type, INHIBIT input	16DIP	908
	LH5010D	CMOS	7-circuit signal non-inversion type, INHIBIT input	18DIP	911
	LH5011D	CMOS	7-circuit signal inversion type, INHIBIT input	18DIP	911
	LH5012	CMOS	7-circuit signal non-inversion type	16DIP	914
	LH5013	CMOS	7-circuit signal inversion type	16DIP	914
	LH5012D	CMOS	8-circuit signal non-inversion type	18DIP	917
	LH5013D	CMOS	8-circuit signal inversion type	18DIP	917
Clock/ Timer	LR3428	CMOS	Analog clock, alarm, oscillator : 4.19 MHz crystal	8DIP	920
	LR3429	CMOS	Analog clock, alarm, oscillator : 4.19 MHz crystal	8DIP	923
	LR3464	CMOS	Analog clock, alarm, oscillator : 32kHz crystal	8DIP	926
	LR3468	CMOS	Analog clock, alarm, oscillator : 32kHz crystal	8DIP	929
	LR3465	CMOS	Analog clock, melody generating function oscillator : 32kHz crystal	22DIP	932
	LR3441	CMOS	(Hour, min) LCD display, timecast, alarm, snooze function, oscillator : 32kHz crystal	48QFP	936
	LR3419	CMOS	(Hour, min) Fluorescent display tube indication, power failure display, oscillator 50/60 Hz or 32kHz crystal	48QFP	941
	LR3472	CMOS	(Hour, min) Fluorescent display tube, 6-program-a-week reservation, oscillator : 32kHz crystal	48QFP	945
LCD driver	LH5008	CMOS	7-segment and 14-segment display, display RAM : 128 bits	60QFP	838
	LH5003	CMOS	5×7-dot matrix display (master), display RAM : 240 bits, character generator: 125 types	60QFP	899
	LH5004	CMOS	5×7-dot matrix display (slave), display RAM : 320 bits, character generator: 128 types	60QFP	899
	LH5821	CMOS	Dot matrix display (master), display RAM : 1280 bits, common output: 20 lines, segment output: 44 lines	80QFP	879
	LH5822	CMOS	Dot matrix display (master), display RAM : 1280 bits, common output: 18 lines, segment output: 46 lines	80QFP	879
	LH5823	CMOS	Dot matrix display (master), display RAM : 1280 bits, common output: 16 lines, segment output: 48 lines	80QFP	879
	LH5826	CMOS	Dot matrix display (slave), display RAM : 1280 bits, segment output: 64 lines	80QFP	884
	LH5030	CMOS	Dot matrix display (common), common output: 80 lines	96QFP	892
	LH5031	CMOS	Dot matrix display (common), common output: 32 lines	44QFP	896
	LH5035A	CMOS	Dot matrix display (segment), display RAM : 3200 bits, segment output: 80 lines	96QFP	889
	LH5036A	CMOS	Dot matrix display (segment), display RAM : 3200 bits, segment output: 80 lines	96QFP	889
	LH5006A	CMOS	Dot matrix display, common output or segment output: 40 lines	60QFP	866
	LH5021A	CMOS	Dot matrix display, common output or segment output: 80 lines	100QFP	870
	LH5022	CMOS	Dot matrix display, common output or segment output: 80 lines	100QFP	870
	LR3691A	CMOS	Dot matrix controller, max display capacity: 163,840 dots	60QFP	844
	LR3692	CMOS	Dot matrix controller, max display capacity: 640×256 dots	80QFP	853
Vacuum fluorescent display driver	LI2048	PMOS	5×7-dot matrix display, character generator: 128 types	60QFP	835
	LH1001	PMOS	Grid drive, output voltage (MAX.): −50V, output current (MAX.): 20mA	36QFP	905

■ MOS IC / LSI (continued)

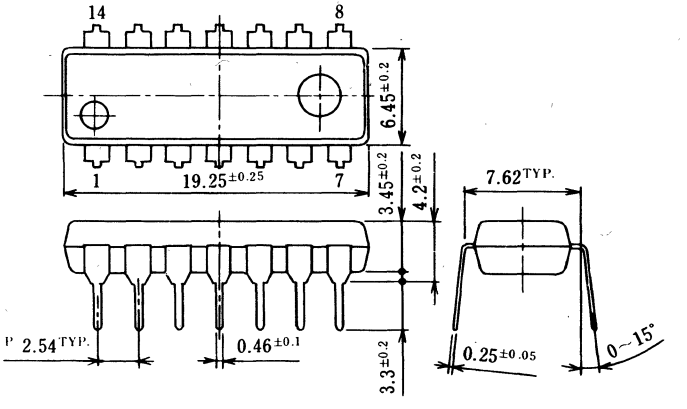
Function	Model	Process	Features	Package	Page
High voltage MOS	LZ1008AD	DMOS	8-output, N-channel, output voltage (MAX.): 300V, output current (TYP.): 35mA	18DIP	804
	LZ1016AD	DMOS	16-output, N-channel, output voltage (MAX.): 250V, output current (TYP.): 45mA	28DIP	807
	LZ1032AM	DMOS	32-output, N-channel, output voltage (MAX.): 250V, output current (TYP.): 45mA	44QFP	811
	LZ1108AD	DMOS	8-output, P-channel, output voltage (MAX.): 300V, output current (TYP.): 20mA	18DIP	815
	LZ1116AD	DMOS	16-output, P-channel, output voltage (MAX.): 300V, output current (TYP.): 30mA	28DIP	818
	LZ1132AM	DMOS	32-output, P-channel, output voltage (MAX.): 300V, output current (TYP.): 30mA	44QFP	821
Audio & Video	LR3617	CMOS	Up / down counter with LCD decoder driver	48QFP	964
	LR3727	CMOS	VTR data back	36QFP	969
	LR3652	CMOS	PLL synthesizer for AM / FM radio	22DIP	977
Remote control	LR3715M	CMOS	56-channel remote-controlled transmitter, oscillator: 455 kHz ceramic	36QFP	952
	LU59001	CMOS	56-channel remote-controlled transmitter, oscillator: 455 kHz ceramic	20DIP	957
Voice Synthesizer/ Melody generator	LR3461	CMOS	8-melody generation with accompaniment, Electromagnetic speaker driver, CR oscillation	22DIP	824
	LR3462	CMOS	8-melody generation, piezo-electric drive, CR oscillation	18DIP	827
	LR3681	CMOS	Speech synthesizer, Waveform coding system, Built-in 32K-bit data ROM, Base frequency : 4.19MHz	48DIP	831
CCD	LZ2020	CMOS	CCD image sensor, dynamic range (TYP.): 54dB, Transfer efficiency more than 99.996%	24DIP (Ceramic)	799
Gate array	LZ92 Series	CMOS	Gate array, 300~5000 gates, 2.8ns/gate	——	796

Package Outline (Unit : mm)

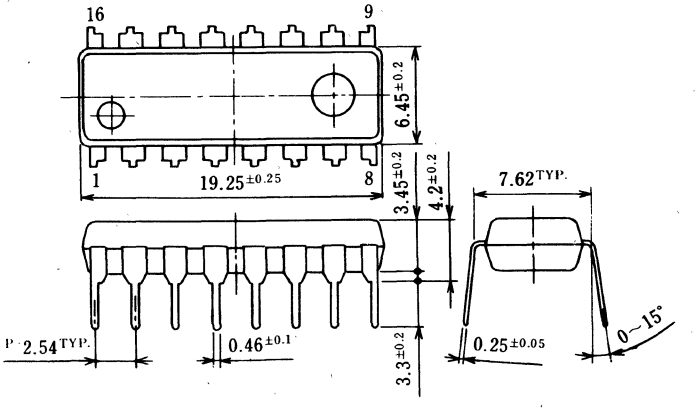
8DIP



14DIP



16DIP



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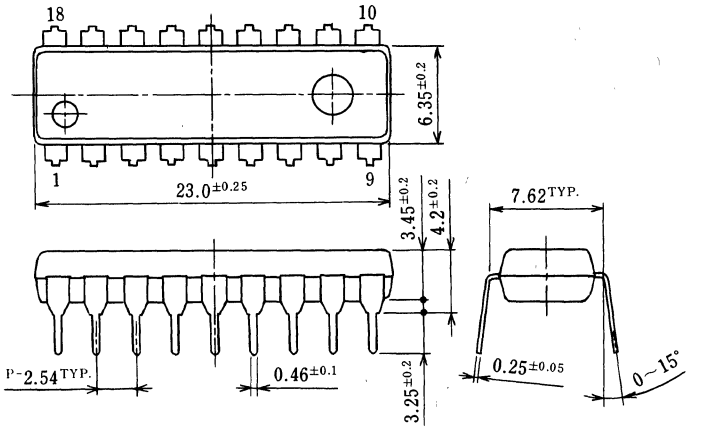
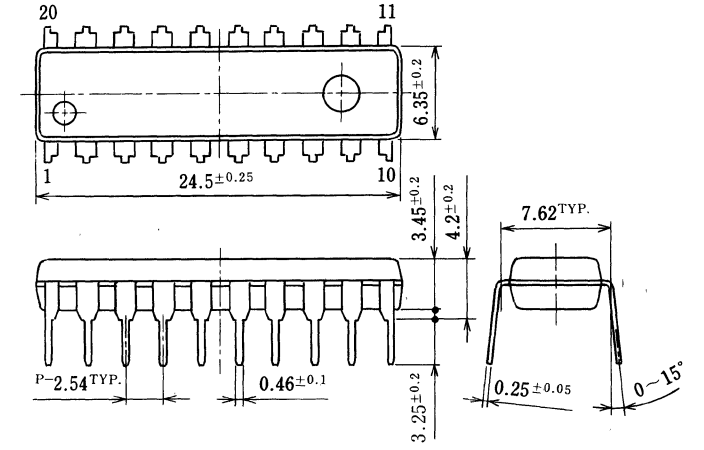
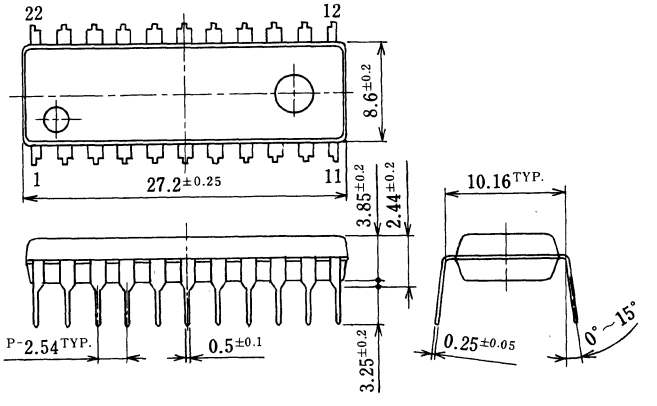


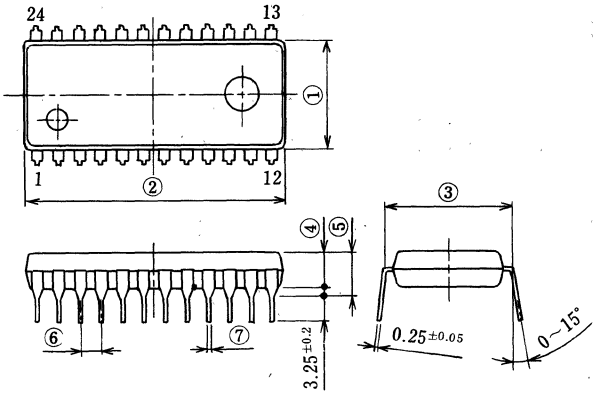
20DIP



22DIP

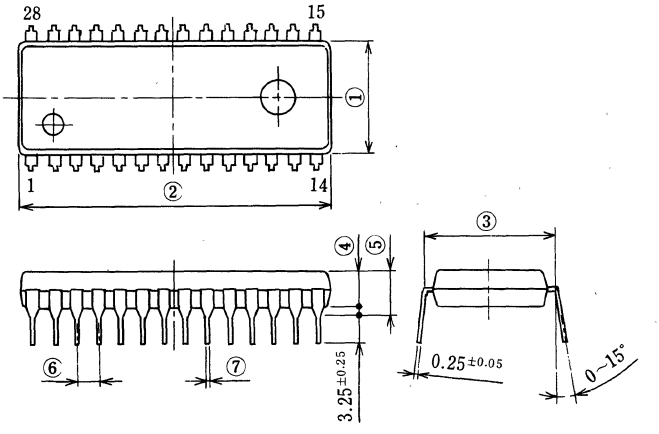


24DIP



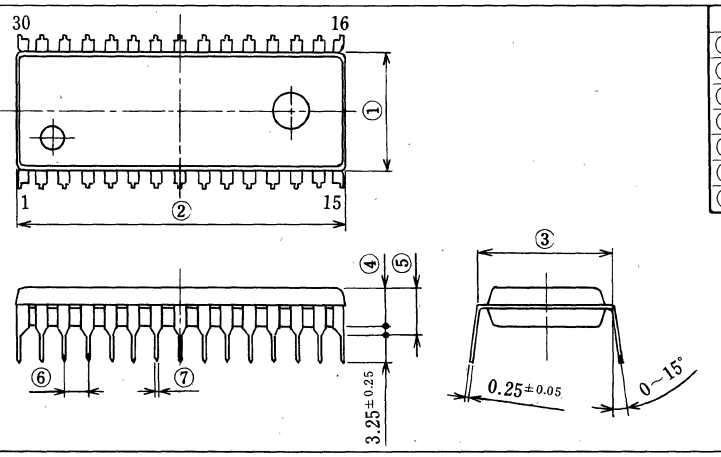
	Normal	Shrink
①	13.2±0.25	6.35±0.2
②	31.0±0.3	22.0±0.25
③	15.24TYP.	7.62TYP.
④	4.25±0.2	3.45±0.2
⑤	5.1±0.2	4.2±0.2
⑥	P-2.54TYP.	P-1.778TYP.
⑦	0.5±0.1	0.46±0.1

28DIP



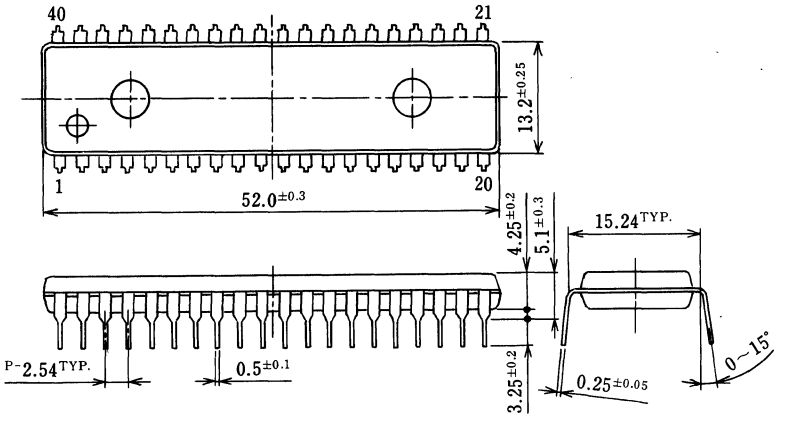
	Normal	Shrink
①	13.2±0.25	8.6±0.2
②	36.0±0.3	25.5±0.25
③	15.24TYP.	10.16TYP.
④	4.25±0.25	3.85±0.2
⑤	5.1±0.2	4.4±0.2
⑥	P-2.54TYP.	P-1.778TYP.
⑦	0.5±0.1	0.46±0.1

30DIP

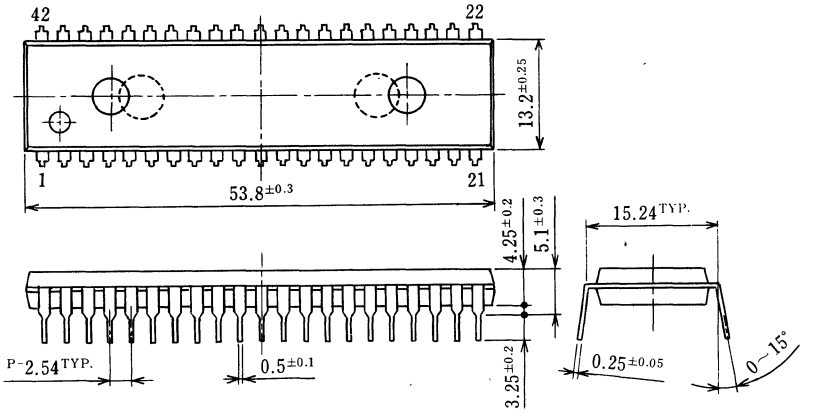


	Normal	Shrink
①	13.2±0.25	8.6±0.2
②	36.0±0.3	27.2±0.25
③	15.24TYP.	10.16TYP.
④	4.25±0.25	3.85±0.2
⑤	5.1±0.2	4.4±0.2
⑥	P-2.54TYP.	P-1.778TYP.
⑦	0.5±0.1	0.46±0.1

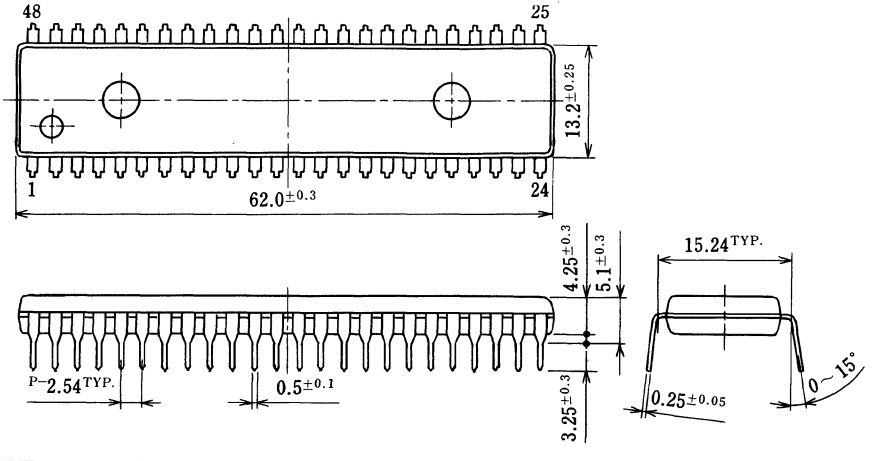
40DIP



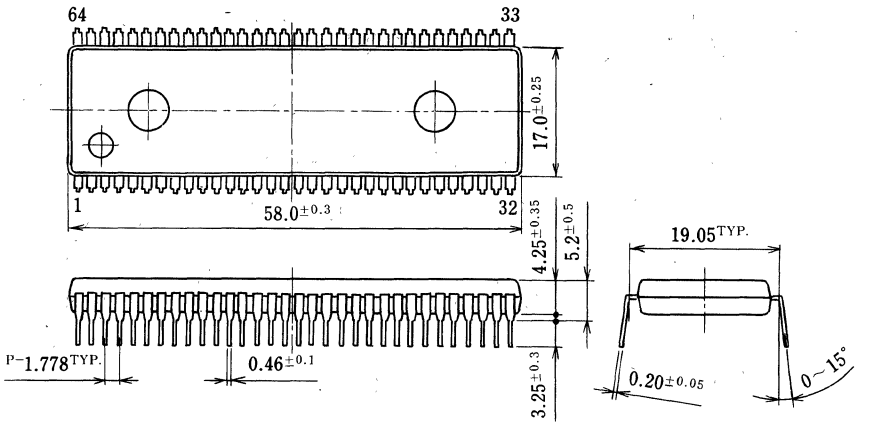
42DIP



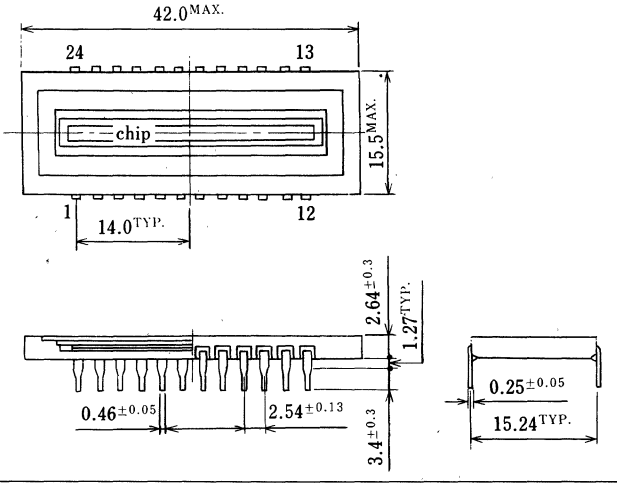
48DIP



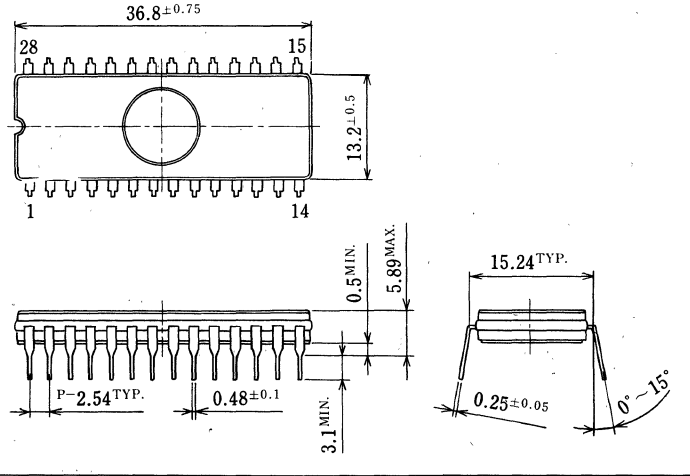
64DIP



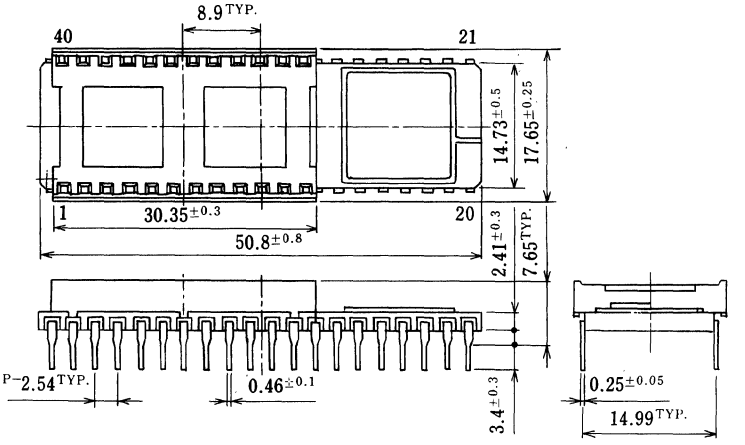
24 DIP (Ceramic)



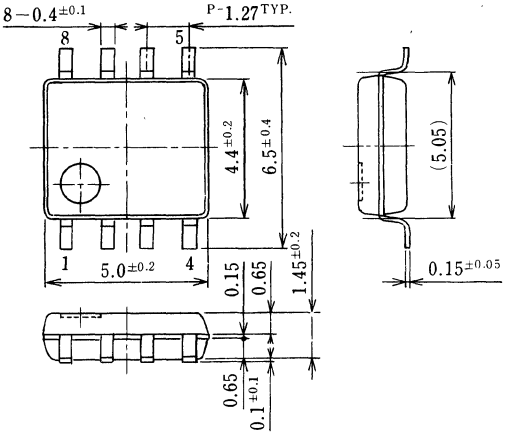
28 DIP(Ceramic)



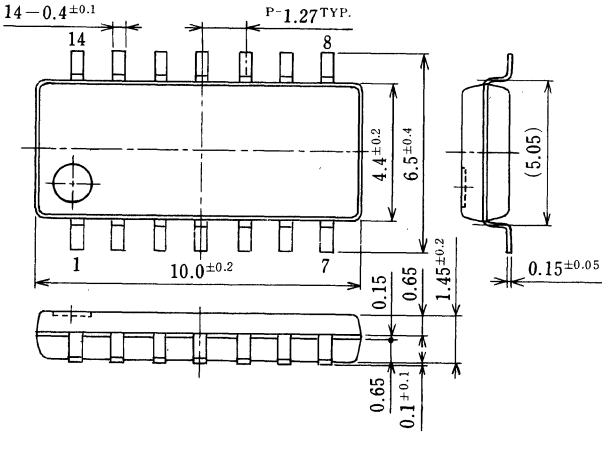
40PBP (Ceramic Piggyback)



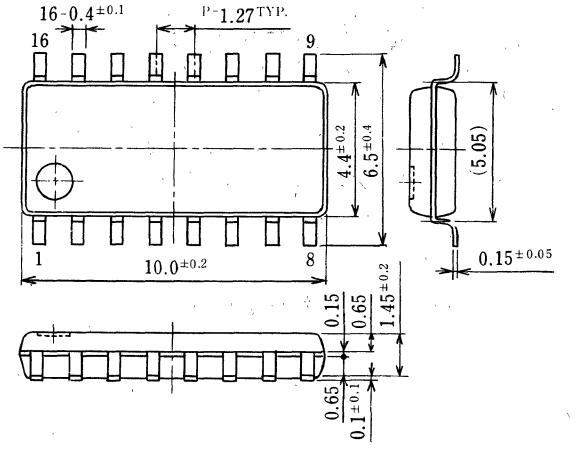
8SOP



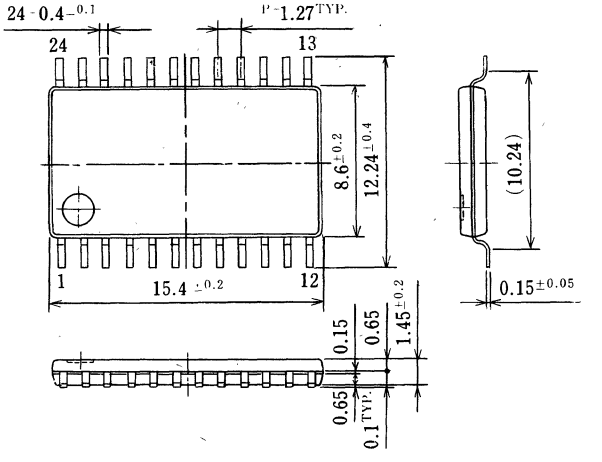
14SOP



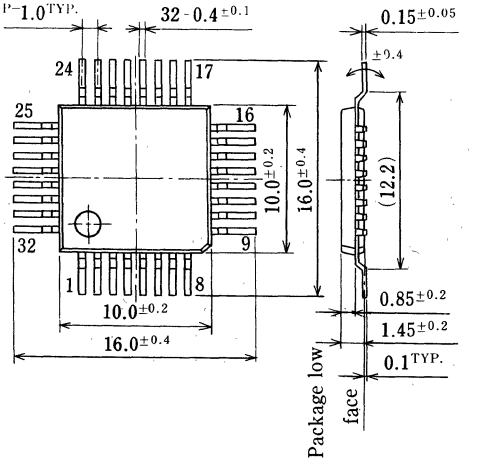
16SOP



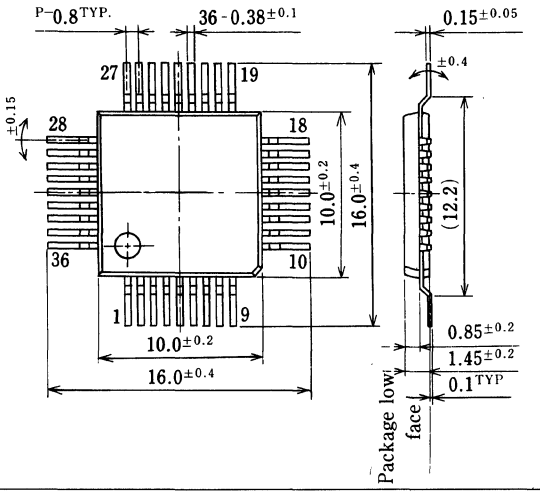
24SOP



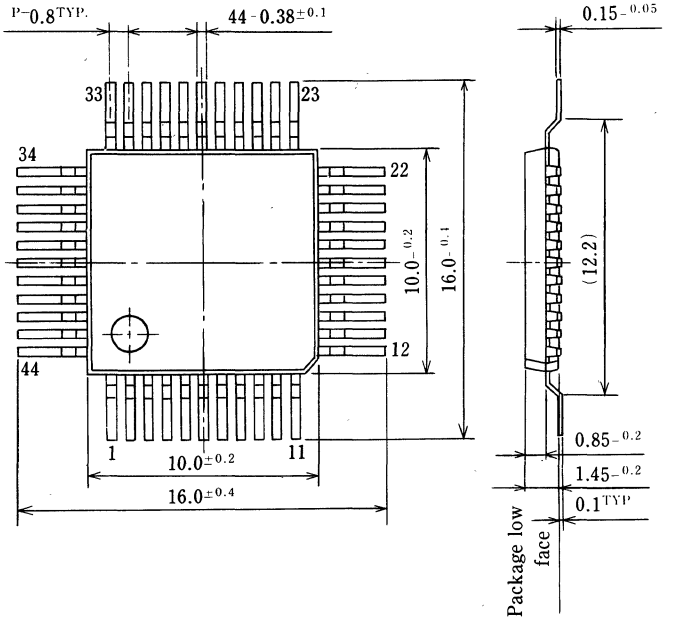
32QFP



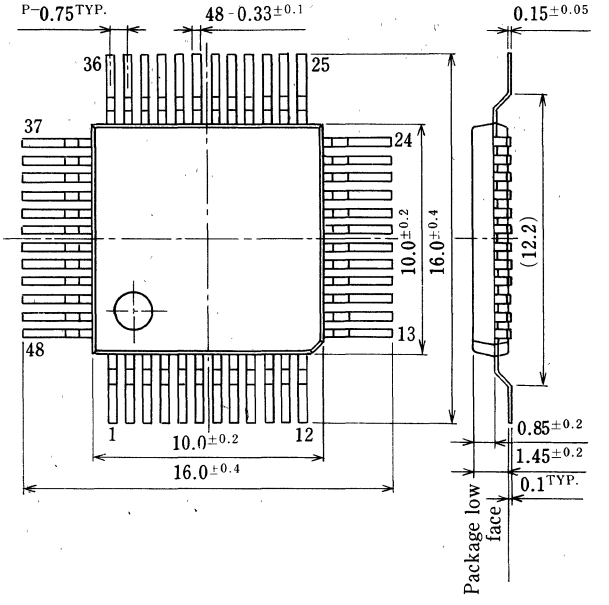
36QFP


P-0.8TYP.
36-0.38±0.1
0.15±0.05
±0.4
27
19
28
18
±0.15
10.0±0.2
16.0±0.4
(12.2)
36
10
1
9
10.0±0.2
16.0±0.4
0.85±0.2
1.45±0.2
0.1TYP
Package low face

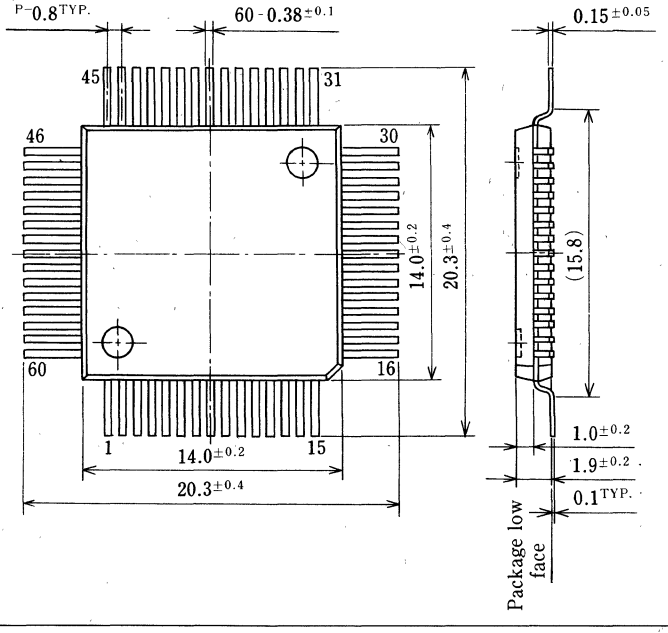
44QFP


P-0.8TYP.
44-0.38±0.1
0.15-0.05
33
23
34
22
10.0-0.2
16.0-0.1
(12.2)
12
44
1
11
10.0±0.2
16.0±0.4
0.85-0.2
1.45-0.2
0.1TYP
Package low face

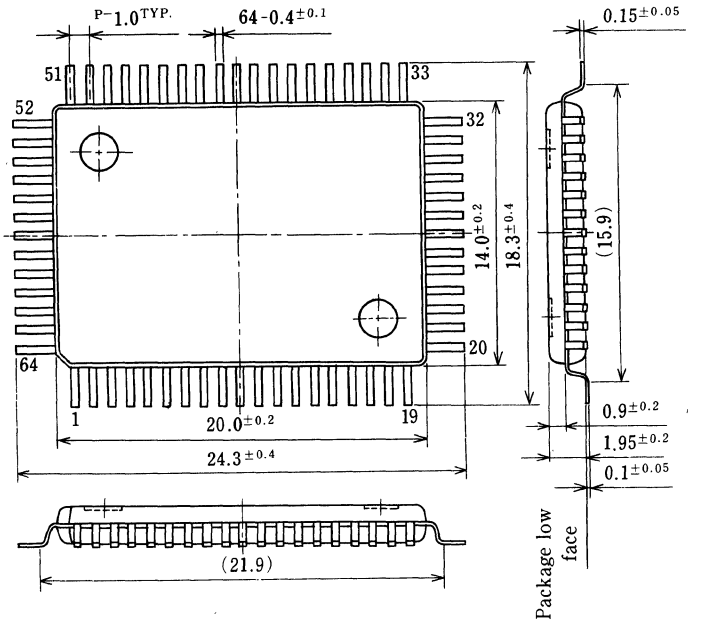
48QFP


P-0.75TYP.
48-0.33±0.1
0.15±0.05
36
25
37
24
13
48
1
12
10.0±0.2
16.0±0.4
(12.2)
0.85±0.2
1.45±0.2
0.1TYP.
Package low face

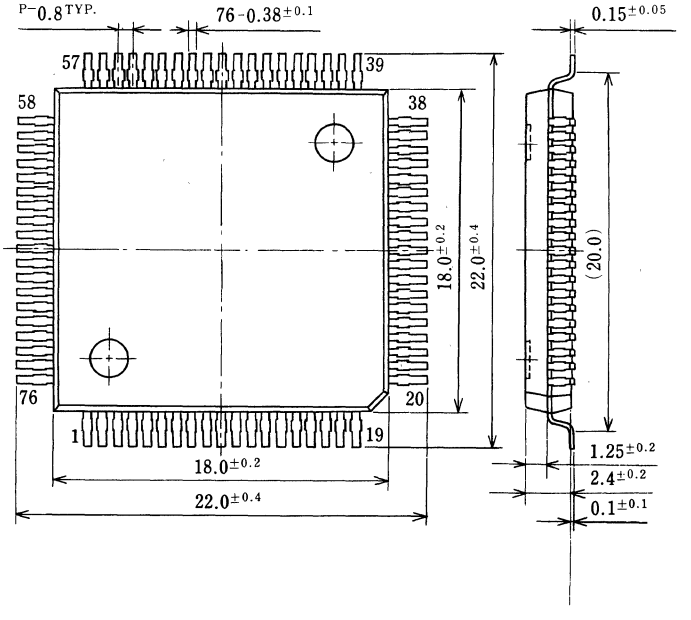
60QFP


P-0.8TYP.
60-0.38±0.1
0.15±0.05
45
31
46
30
60
16
1
15
14.0±0.2
20.3±0.4
(15.8)
1.0±0.2
1.9±0.2
0.1TYP.
Package low face

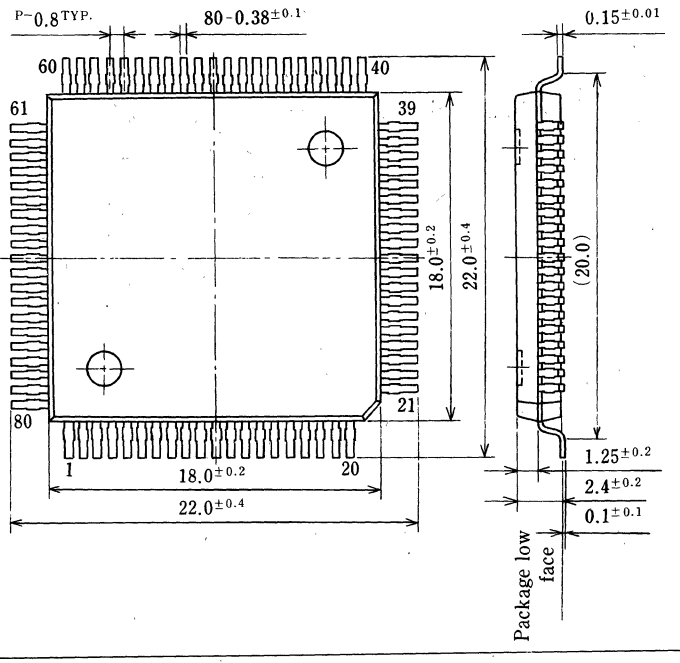
64QFP


P-1.0TYP.
64-0.4±0.1
0.15±0.05
51
33
52
32
14.0±0.2
18.3±0.4
(15.9)
64
20
1
20.0±0.2
19
24.3±0.4
0.9±0.2
1.95±0.2
0.1±0.05
(21.9)
Package low face

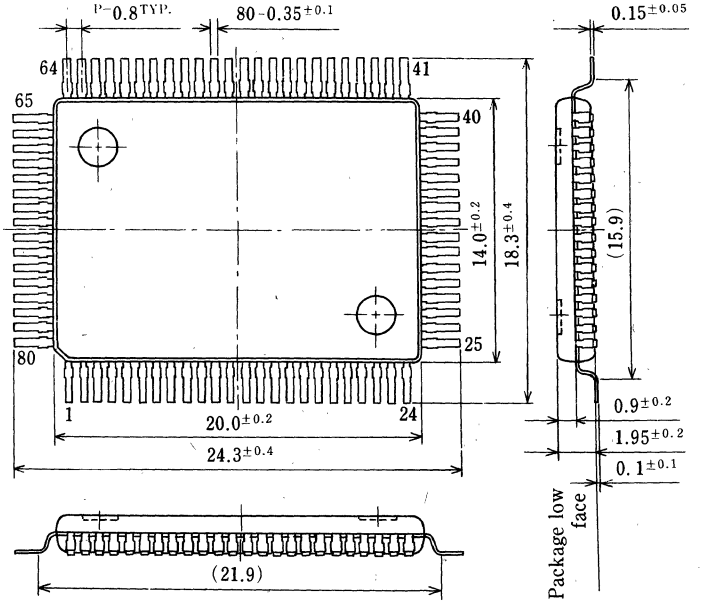
76QFP


P-0.8TYP.
76-0.38±0.1
0.15±0.05
57
39
58
38
18.0±0.2
22.0±0.4
(20.0)
76
20
1
19
18.0±0.2
22.0±0.4
1.25±0.2
2.4±0.2
0.1±0.1

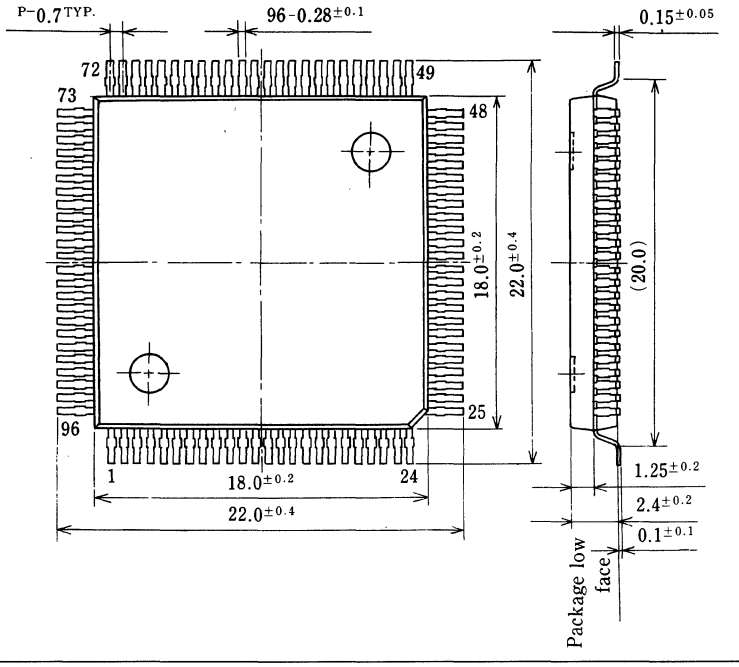
80QFP


P-0.8TYP.
80-0.38±0.1
0.15±0.01
60
40
61
39
18.0±0.2
22.0±0.4
(20.0)
21
80
1
18.0±0.2
20
22.0±0.4
1.25±0.2
2.4±0.2
0.1±0.1
Package low face

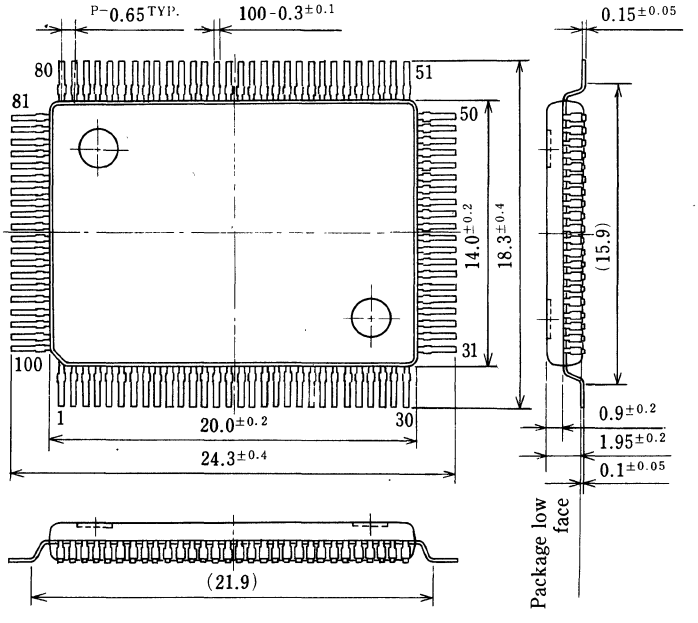
80QFP


P-0.8TYP.
80-0.35±0.1
0.15±0.05
64
41
65
40
14.0±0.2
18.3±0.4
(15.9)
25
80
1
20.0±0.2
24
24.3±0.4
0.9±0.2
1.95±0.2
0.1±0.1
(21.9)
Package low face

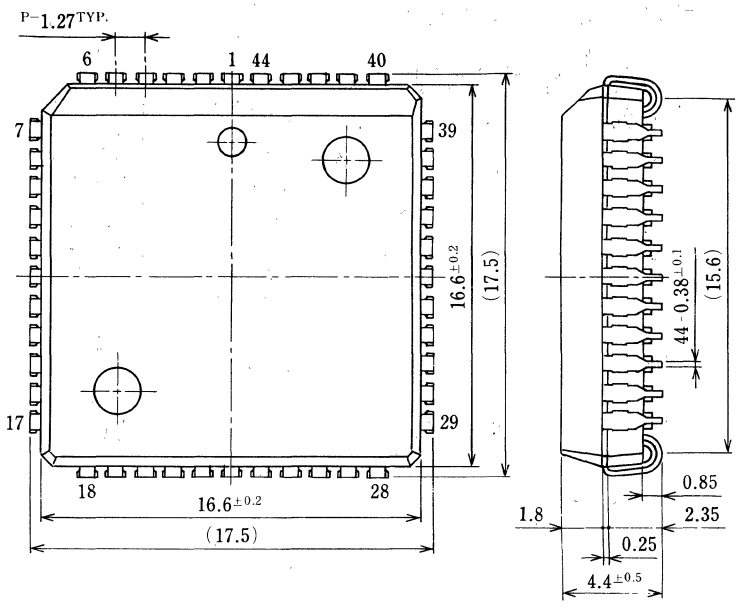
96QFP



100QFP



44PLCC



DIP : Dual-In-Line Package
QFP : Quad Flat Package
SOP : Small-Outline Package
PBP : Piggyback Package
PLCC : Plastic-Leadless-Chip-Carrier

Quality Assurance

1. Quality Assurance System

Sharp develops and manufactures a wide range of consumer and industrial-use semiconductor products, including ICs and LSIs.

In recent years, the applications of ICs and LSIs have expanded significantly, into fields where extremely high levels of quality are critical.

In response, Sharp has implemented a total quality assurance system that encompasses the entire production process from planning to after-sales service. This system ensures that reliability is a priority in the planning and manufacturing stages, and guarantees product quality through rigorous reliability testing. We will introduce a part of this system here.

Sharp's quality and reliability assurance activities are based on the following guidelines:

(1) All personnel should participate in quality assurance by continually cultivating a higher level of quality awareness.

(2) In the developmental stage of new products, create designs that consider reliability in every respect.

(3) In addition to quality control in all manufacturing processes, all working environments, materials, equipment, and measuring devices should be carefully monitored to ensure quality and reliability from the very beginning of the process.

(4) Confirm long-term reliability and obtain a through understanding of practical limits through reliability testing.

(5) Continually work to improve quality through application of data from process inspections, reliability testing, and market surveys.

2. Quality and Reliability Control in New Product Development

The development of new products begins with a thorough understanding of the product specifications and quality that will satisfy the purpose for which the product is intended and with developmental planning that carefully considers pricing, quantity and the time of introduction to the market.

In the design stage, reliability is designed into the product based on test data, process capability, and field data, and experimental models are made. These experimental models are referred to as TS (technical samples), and are evaluated primarily for their ability to function and their performance.

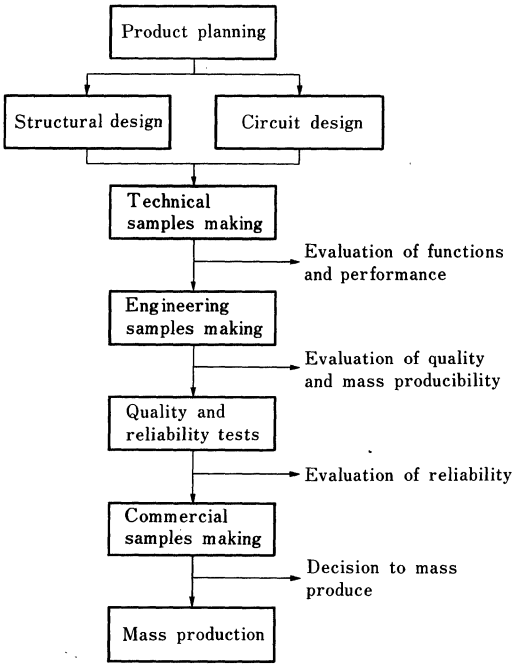


Fig. 1 New Product Development Steps

Next, ES (engineering samples) are made and evaluated to determine whether the functions, performance and quality aimed for in the design stage can be guaranteed under the existing manufacturing conditions. These ES are also evaluated in quality and reliability tests to determine whether their long-term reliability can be guaranteed.

After this, mass producibility is evaluated using CS (commercial samples) obtained from a trial mass production, and the decision to mass produce or not is made. Fig. 1 shows the steps in the development of new products.

3. Quality and Reliability Control in Mass Production

(1) Quality Control of Materials

The quality and reliability of a product is affected by its component materials as well as the manufacturing processes and conditions.

The quality control of purchased component materials is ensured by material qualification and inspection upon receipt.

Table 1 Examples of items considered in material approval

Material	Wafers	Resins	Lead frames	Bonding wire
Items	Crystal growth method Crystal orientation Doping Oxygen content Dislocation density Diameter Thickness Parallelism Specific resistance	Composition Electrical characteristics Thermal characteristics Formability Process characteristics Reliability evaluation Reliability characteristics by elements used	Composition Electrical characteristics Thermal characteristics Physical characteristics Appearance Dimensions Processing accuracy Plating characteristics Process characteristics	Purity Appearance Dimensions Strength Elongation characteristics Process characteristics

Process	Control items	C
Silicon wafers Purchase of material		
Inspection upon receipt	Appearance, dimensions, specific resistance	Eliminate items with incorrect dimensions; scratches, and crystal defects and assure resistance values.
Oxidation		
Oxidation inspection	Appearance, film thickness	Confirm the absence of pin holes and assure film thickness.
On line QC	Surface cleanliness	Check the cleanliness of surfaces.
Photolithography		
Visual inspection	Development, etching	Check the suitability of development and etching.
On line QC	Wire width	Control the wire width.
Ion implantation		
Chip electrical inspection	Electrical characteristics	Eliminate items with unsuitable electrical characteristics.
Dicing		
Breakage screening		
Frame Die inspection	Appearance	Confirm the absence of breakage and chips.
Die bonding		
Gold wire Die bonding inspection	Appearance, bond strength	Check quality of die bond.
Wire bonding		
Wire bonding inspection	Appearance, tensile strength	Check position and shape of bond and assure sufficient tensile strength.

Fig. 2 Example of process quality control

Table 1 shows examples of material qualification items. The inspections performed upon receipt of materials use criteria compiled from the purchase specifications and approval drawings, and employ sampling inspection methods that conform with MIL-STD-105D.

(2) Control of Manufacturing Environment

Environmental conditions in the manufacturing process — such as temperature, humidity, and dust — significantly affect the finished quality of semiconductor products.

Temperature is especially critical in maintaining the accuracy of the measurement of electrical characteristics and the accuracy of various devices. Humidity control is important for the prevention of moisture penetration into a device and the prevention of static electricity. Temperature and humidity are thus strictly maintained at constant levels.

A dust-free environment is vital in the manufacture of refined semiconductor circuits, as dust can be the critical determining factor in their quality and reliability. Thus, the cleanliness of everything from air conditioning equipment to work benches to work clothes and office items is carefully controlled.

Sharp is also concerned about creating an environment conducive to error-free high-precision work, and so provides background music and interior colors appropriate for specific tasks.

(3) Control of Manufacturing Equipment and Measuring Devices

Tremendous technological innovation and progress has been made in semiconductors themselves and in the processes and equipment by which they are produced.

To achieve even higher levels of product uniformity and quality, Sharp is continually furthering the automation of its processes, strictly managing the maintenance of its manufacturing equipment, and carefully monitoring the accuracy of all measuring devices through daily and periodic inspections.

(4) Process Quality Control and Product inspections

Based on the fundamental concept of ensuring quality and reliability throughout the manufacturing process, we check at each stage to determine whether the prescribed characteristics are being obtained and to prevent defective items from going on to the next stage. We do this through strict monitoring, inspection of all items, sampling inspections, and other standardized methods of management.

We perform a final inspection of all finished products as well as further quality assurance inspections through sampling to fully ensure quality.

Detects found in these inspections are promptly reported to the design and production sections, and improvements made in the processes to upgrade our uniform quality capabilities.

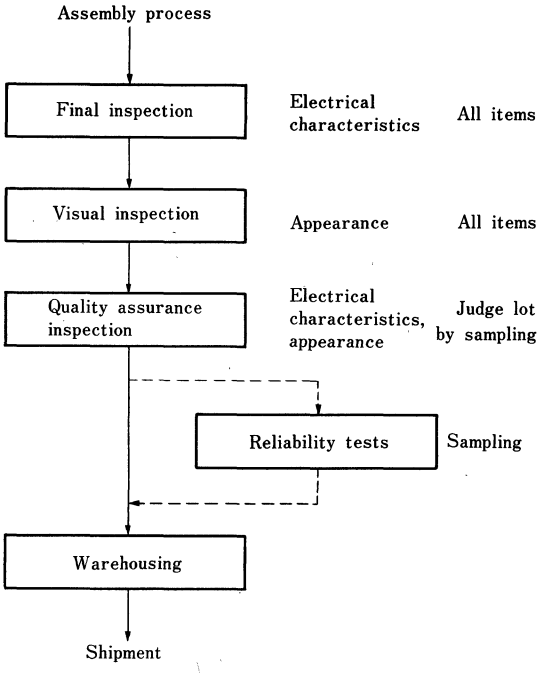


Fig. 3 Product inspection system

Fig. 3 Shows the product inspection system.
Fig. 4 Shows an example of process quality control.

(5) Reliability Assurance

To guarantee the long-term reliability of our products, we periodically sample products and subject them to reliability testing such as life tests and environmental tests.

In addition, reliability tests are performed whenever process changes have been made.

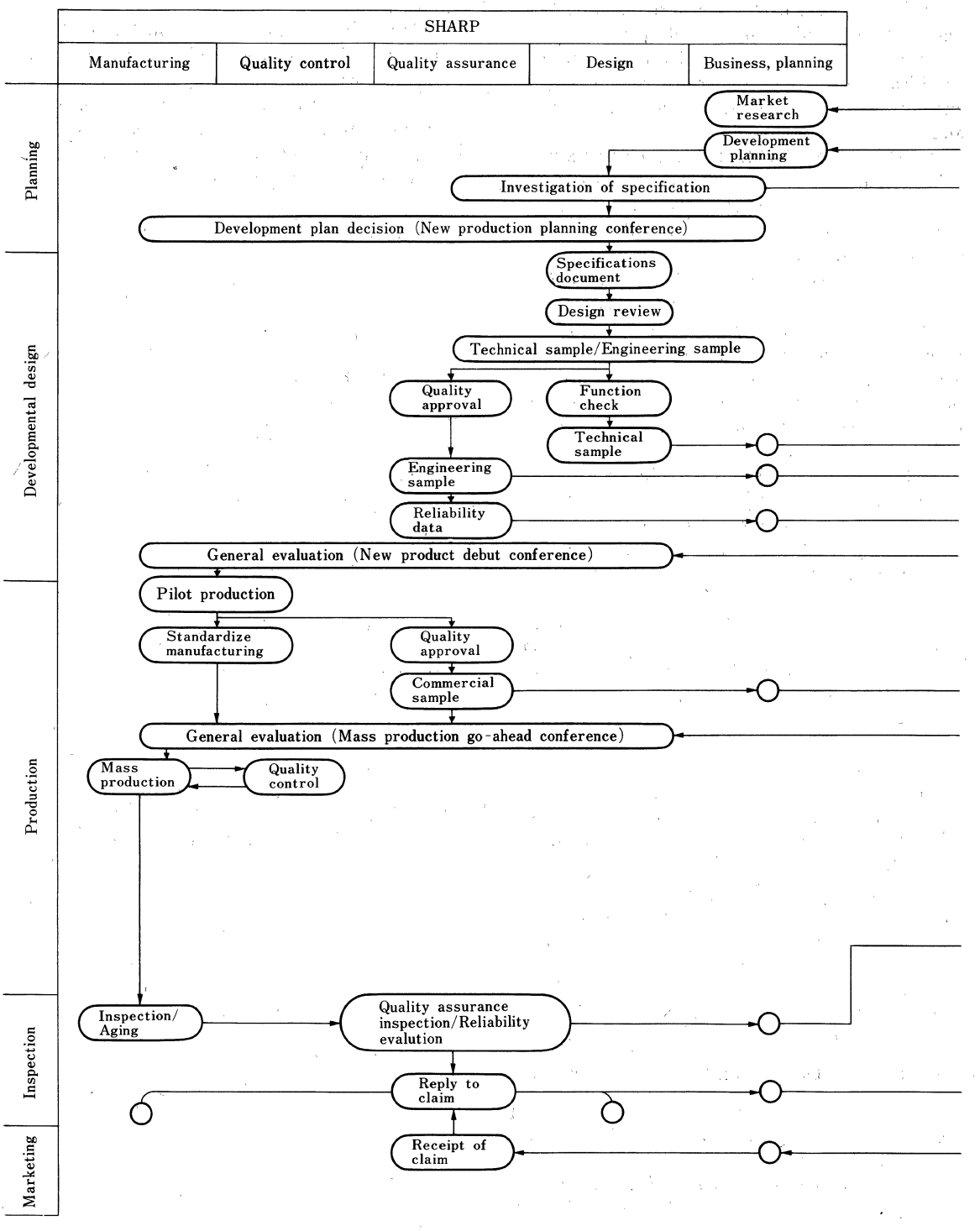


Fig. 4 (a) Quality assurance system (SHARP side)

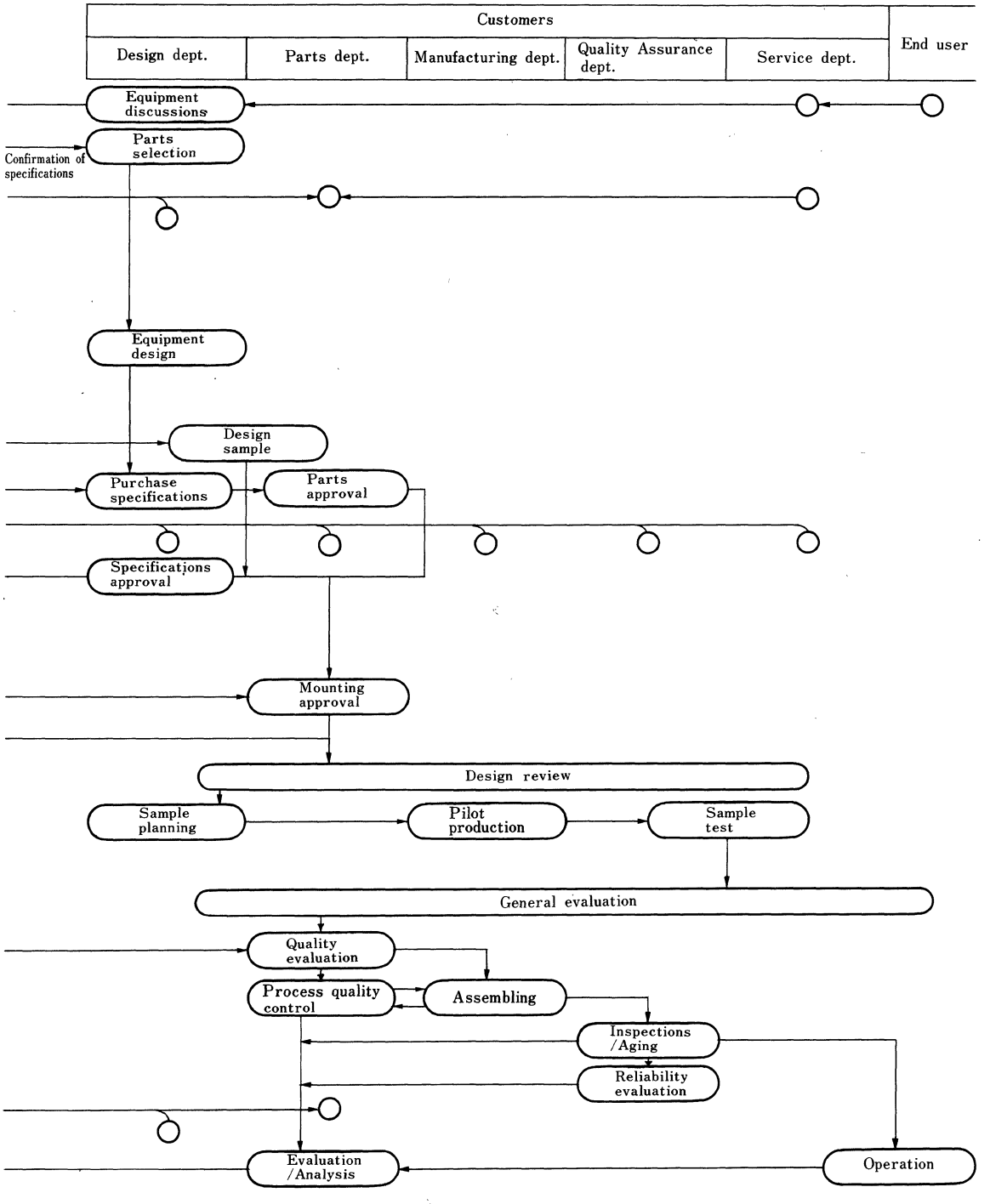


Fig. 4 (b) Quality assurance system (User side)

4. Reliability Tests

In addition to determining the extent to which product reliability can be assured, the objectives of reliability testing include getting an understanding of design limitations and the catastrophic failure mode, and predicting reliability in the field.

The major categories of reliability testing are durability tests, thermal environmental tests, and mechanical tests. The standardized test methods used are those prescribed by official standards or associations such as the International Electronics Commission (IEC), and the U. S. Military Specifications (MIL). Sharp standardizes all specifications to conform with these standards.

Table 2 shows a representative reliability test.

Durability testing of semiconductor products places the greatest emphasis on high temperature operation tests. Priority in the testing of plastic molded products is on high temperature, high humidity storage (operation) tests.

Table 2 Reliability test for semiconductor products

Type	Test item	Test condition	Test objectives
Durability tests	High temperature storage	T_{stg} (max.)	Evaluate resistance to high temperatures in longterm storage.
	High temperature operation	T_{opr} (max.) power supply voltage (max.)	Evaluate resistance to long-term thermal and electrical stress.
	High temperature, high humidity storage	60℃ 90% RH 85℃ 85% RH Pressure cooker at 120℃ and 2 atmospheres	Evaluate resistance to high temperatures and high humidity in long-term storage.
	High temperature, high humidity operation	60℃ 90% RH 85℃ 85% RH	Evaluate resistance to long-term thermal, humidity and electrical stress.
	Low temperature storage	T_{stg} (min.)	Evaluate resistance to low temperatures in long-term storage.
Thermal environmental tests	Temperature cycling test	T_{stg} (max.)−T_{stg} (min.)	Evaluate resistance to sudden extreme temperature changes.
	Heat shock test	0℃−100℃ (liquid)	Evaluate resistance to sudden extreme temperature changes.
	Temperature and humidity cycling test	−10℃ to+65℃ 90% RH	Evaluate resistance to extreme temperature changes at higgh humidity.
	Solder heat resistance	260℃ 10s	Evaluate resistance to thermal stress during soldering.
Mechanical tests	Shock test	1,500G, 0.5 ms ±X, ±Y, ±Z	Evaluate structural and mechanical resistance to strong shocks.
	Variable-frequency vibration test	20G, 20−2,000 Hz, X, Y, Z	Evaluate resistance to vibration during transport and use.
	Pin strengeth	Tensile strength : holds fixed load for 10 seconds Bending strength : bend once 90 in forward and reverse directions (Load is determined based on pin shape and the surface area of pins section.)	Evaluate resistance to mechanical stress applied to pins.
	Air-tightness	Test for minute leaks using helium gas and large leaks using foaming.	Evaluate hermetic sealing.
	Salt spray test	Spray 5% salt solution at Ta=35 ℃ for 24 hours	Evaluate resistance to corrosion in salt spray environment.
	Solderability	230 ℃ for 5 seconds (with flux)	Evaluate solderability of pins.
	Solvent resistance	Dip in isopropanol and acetone for 30 seconds at Ta=25℃	Evaluate resistance to pitting.

5. After-sales Service

If a product malfunctions after shipment, we have the customer return the product for detailed analysis. We also obtain complete information concerning conditions of use, frequency of occurrence, and symptoms.

When the cause has been determined, we report findings concerning the design, manufacturing process, or method of use to the departments concerned for preventive action against recurrence of the malfunction. We then submit a report to the customer.

This process of tracking the performance of our products in actual use is an extremely effective way to enhance product reliability. We direct a lot of energy forwards its full impremention.

Fig. 5 shows the routes through which accidents and malfunctions outside of the company are handled, and Fig. 6 shows the procedures used in their analysis.

6. Handling Precautions

All of the semiconductor products listed in this data book were manufactured based on exacting designs and under comprehensive quality control. However, to take full advantage of the features offered and assure the products' long-life service, please refer to this manual to help in designing systems that make best use of their capabilities.

(1) Maximum Ratings

It is generally known that the failure rate of semiconductor products increases as the temperature increases. It is necessary, of course, that the ambient temperature be within the maximum rated temperature. Further it is desirable from the standpoint of reliability that the ambient temperature be lowered as much as possible. The voltage, current, and electric power used are also factors that significantly influence the life of semiconductor products. Voltage or current that exceeds the rated level may damaged, the semiconductor product; even if applied only momentarily and the unit continues to operate properly, excessive voltage or current will likely increase the failure rate.

Therefore, in actual circuit design, it is important that the semiconductor products used have a certain degree of allowance with respect to the voltage, current and temperature conditions under which they will be used. The greater this allowance, the fewer the failures that will occur.

To keep failures to a minimum, the circuit should be designed so that under all conditions to absolute maximum, the ratings are not exceeded even

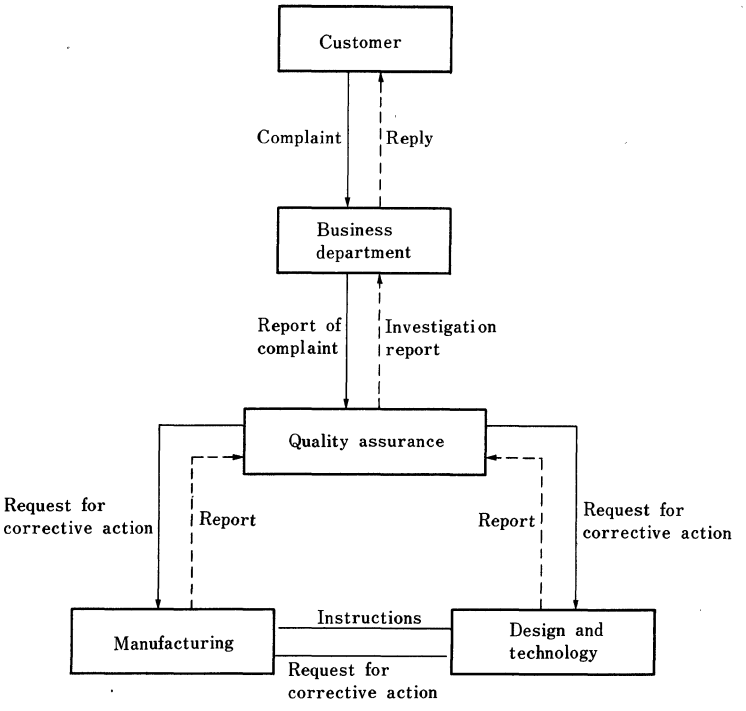


Fig. 5 Routes through which malfunctions outside the company are handled

momentarily and so that the maximum values for any two or more items are not achieved simultaneously. In addition, remember that the circuit functions of semiconductor products are guaranteed within the operating temperature range (T_{opr}) of the absolute maximum ratings, but that storage temperature (T_{stg}) is the range in a nonoperating condition.

(2) Transportation and Storage

Semiconductor products are susceptible to high temperature and high humidity. Please store them in a dry place as near to room temperature as possible.

During shipping and storage, keep semiconductor products in the packaging they were delivered in to prevent damage due to static electricity. If removed from their packaging, the terminals must be shortcircuited with a conductive material or the entire units wrapped in aluminum foil. Also remember that nylon and plastic containers build up electrostatic charges easily and so should not be used for storage or transportation.

Mechanical vibration and shock should also be kept to a minimum.

(3) Assembly

When attached to printed circuit boards, semiconductor products are removed from a conductive container, so electrical equipment, work benches, and operators must be grounded to protect the products from static electricity. It is good to use grounded metal plating on the surfaces of work benches. Grounding metal rings and watch bands is a convenient method for grounding operators. The grounding of operators is required to prevent electric shock due to current leaks from electrical equipment, so it must be performed through a resistance of 1 MΩ.

Working attire made of synthetic fabrics should be avoided in favor of fabrics such as cotton that do not easily generate static electricity.

Keeping the relative humidity in working areas around 50% will also help to prevent the generation of static electricity.

Current leakage from electrical equipment is not desirable from the standpoint of safety. All equipment should therefore be checked periodically for current leakage.

When forming the lead wires of semiconductor products to be mounted, forceps or a similar tool that will prevent stress from being applied to the base of the wires should be used.

To prevent the input terminals of semiconductor products on completed printed circuit boards from becoming open during storage or transport, the terminals of the circuit board should be shortcircuited or the entire circuit board itself should be wrapped in aluminum foil.

(4) Soldering and Cleaning

When using a soldering iron or solder bath, keep the temperature below 260℃ the time and within 10 seconds. If using a soldering iron, use one with no leakage from the soldering tip. An A class soldering iron with an insulation resistance of less than 10 MΩ is recommended. When using a solder bath, it should be grounded to prevent its having an unstable electric potential.

Using a strongly acidic or alkaline flux for soldering can cause corrosion of the lead wires. A resin flux is ideal for this type of soldering.

To assure the reliability of a system, removal of the flux used in soldering is generally required. Freon TE, a freon cleaning fluid, or difron solvent S3-E is recommended for use as the cleaning fluid.

To prevent stress on semiconductor products and circuit board when using ultrasonic cleaning, a cleaning method must be used that will shadow the main unit from the vibrator and keep cleaning time to less than 30 seconds.

(5) Adjustment and Tests

When the set is to be adjusted and tested upon completion of the printed circuit board, the printed circuit board must be checked to ensure that there are no solder bridges or cracks before the power is turned on. Also, if the marked rated voltage and current are to be used, it is wise to use a current limiter.

Whenever a printed circuit board is to be removed or mounted on a socket, the power must be turned off.

When testing with a probe, care must taken to assure that the probe does to come in contact with other signals or the power supply. If the test location has been decided beforehand, it is wise to set up a specially designed test pin for testing.

When testing in high and low temperatures, the constant temperature bath must be grounded and measures taken to protect the set inside the bath from static electricity.

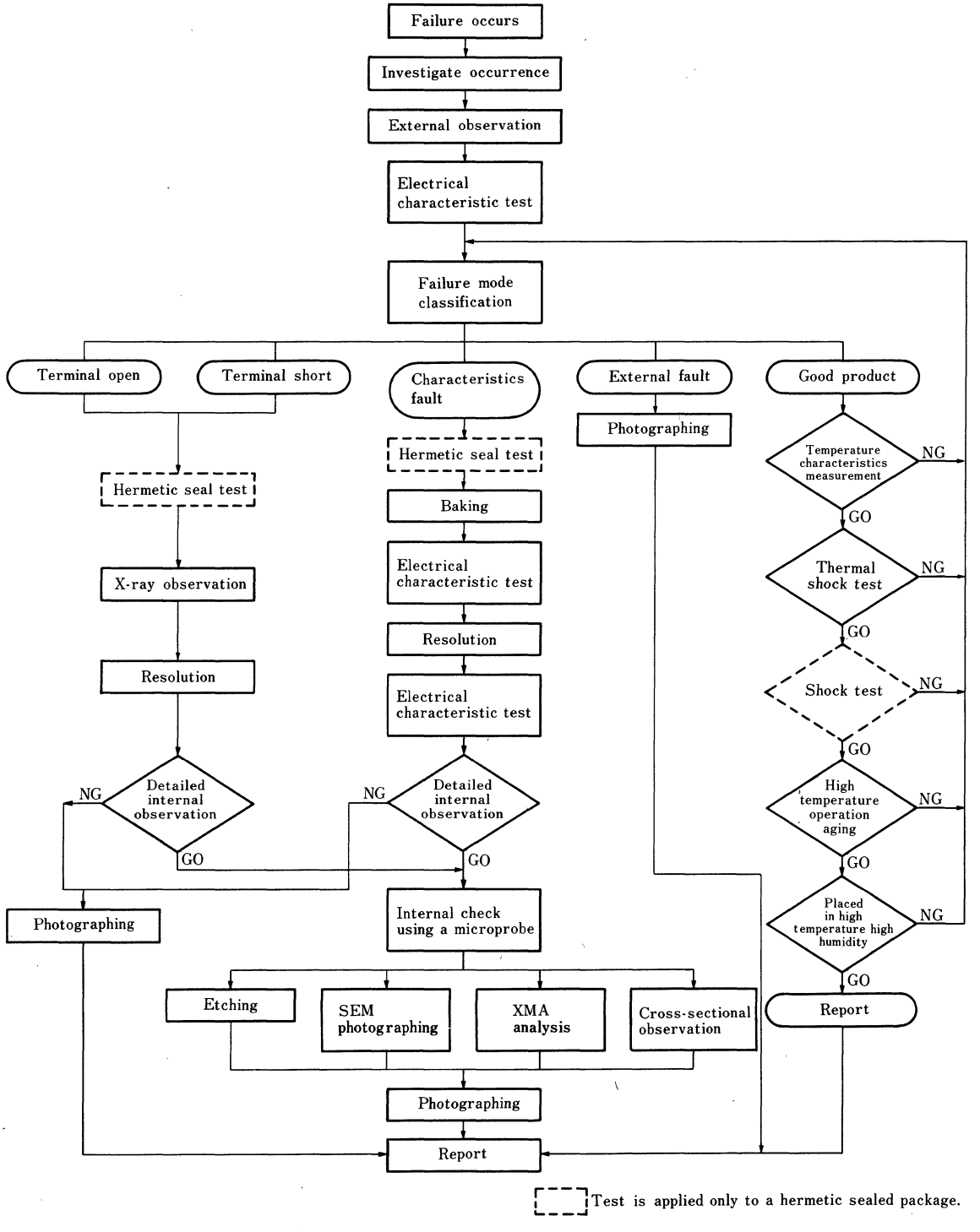


Fig. Failure analysis procedure

4-Bit 1-Chip Microcomputers

2

SM-3A PMOS 4-Bit 1-Chip Microcomputer

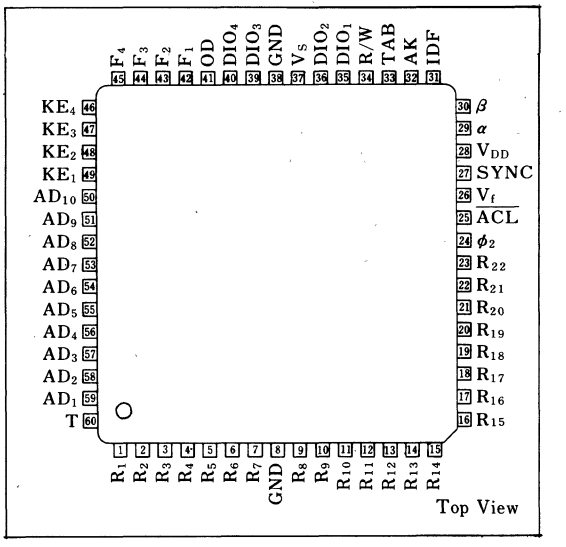
■ Description

The SM-3A is a 4-bit single chip PMOS microcomputer with 2,268 bytes of ROM, and 128 words of RAM. It is well suited for low cost systems requiring many I/O control ports.

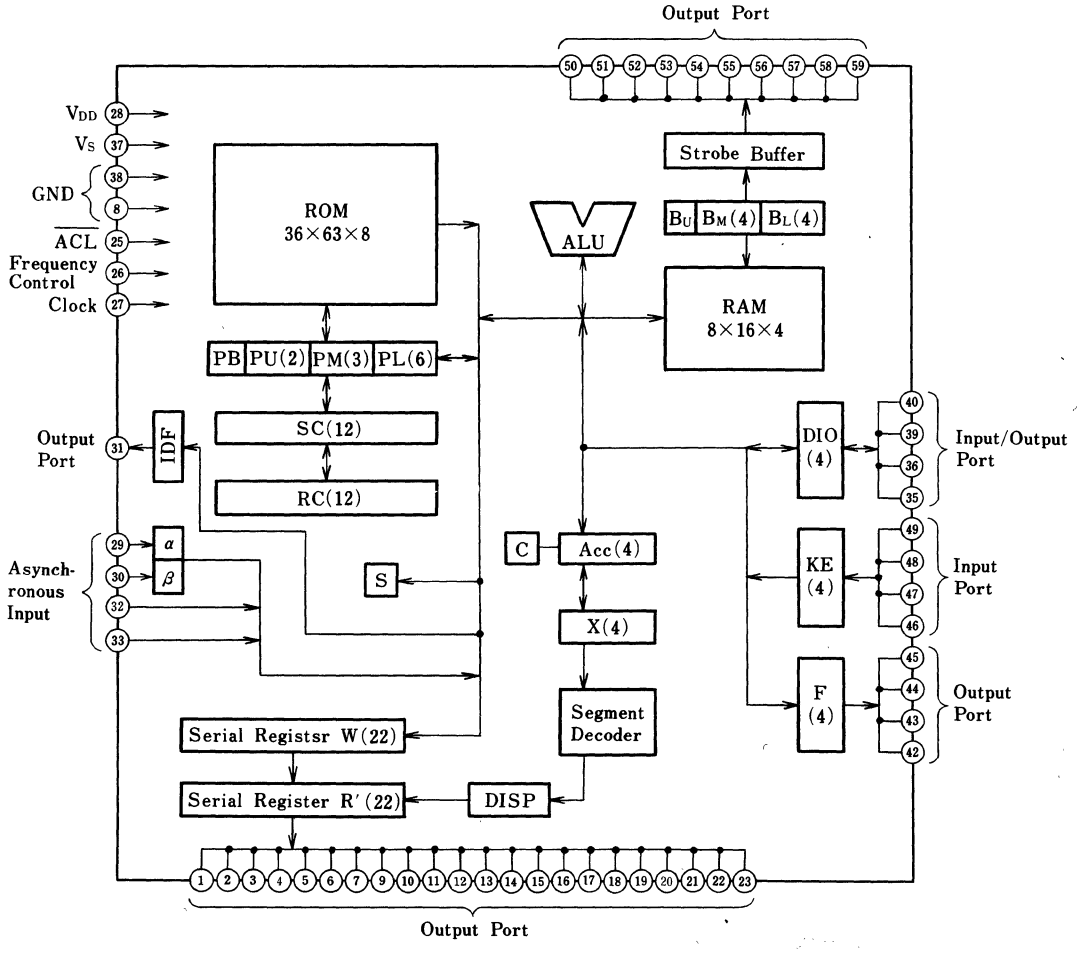
■ Features

1. PMOS process
2. ROM capacity 2,268×8 bits
3. RAM capacity 128×4 bits
4. Instructions 57
5. Subroutine nesting 2 levels
6. Input ports 8 bits
7. Output ports 37 bits
8. Input/Output ports 4 bits
9. On-chip clock generator circuit
10. High voltage outputs (−38V) 27 bits
11. Single power supply −15V (TYP.)
12. Instruction cycle 10 μs
13. 60-pin quad-flat package

■ Pin Connections



Block Diagram



Symbol description

ALU	: Arithmetic logic unit	RC	: Stack register of program counter
Acc	: Accumulator	BU, BM, BL	: RAM address register
C	: Carry F/F	X	: Temporary register
PB, PU, PM, PL	: Program counter	S	: Flag F/F
SC	: Stack register of program counter	DISP	: Display F/F

■ Pin Description

Pin	I/O	Type of circuit	Function
$KE_1 \sim KE_4$	I	Pull down	$A_{CC} \leftarrow KE_1 \sim KE_4$
α, β, AK, TAB	I	Pull down	Possible to test 4 bits independently
$DIO_1 \sim DIO_4$	I/O	Complementary 3 states	$A_{CC} \leftarrow DIO_1 \sim DIO_4$
$R_1 \sim R_7$	O	Open drain	Segment output or R register output
$R_8 \sim R_{22}$	O	Open drain	R register output
$F_1 \sim F_4$	O	Open drain	$F_1 \sim F_4 \leftarrow A_{CC}$
$AD_1 \sim AD_{10}$	O	Open drain	BL decode output or external RAM address output
IDF	O	Open drain	Possible to set, reset and test by command (Suitable for printer motor drive signal)
OD, R/W	O	Complementary	External RAM control output
T	I	Pull down	For test (usually connected to V_{DD})
$\overline{ACL}$	I		Auto clear
ϕ_2	O	Complementary	Synchronizing signal terminal
V_f, SYNC			Frequency control terminal
V_{St}			Power source for external RAM connection
V_{DD}, GND			Power source for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Pin voltage	V_{DD}	$-20 \sim +0.3$	V	1
	V_S	$-20 \sim +0.3$	V	1
	V_{IN}	$-20 \sim +0.3$	V	1
	V_{OUT1}	$-20 \sim +0.3$	V	1,2
	V_{OUT2}	$-40 \sim +0.3$	V	1,3
Operating temperature	T_{opr}	$-10 \sim +60$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Applicable pins include : R/W, DIO_1-DIO_4, OD, AD_1-AD_{10}
Note 3: Applicable pins include : R_1-R_{22}, F_1-F_4, IDF

■ Electrical Characteristics

($V_{DD} = -15.0V \pm 10\%$, $V_N = -38V$, $Ta = -10 \sim +60$℃)

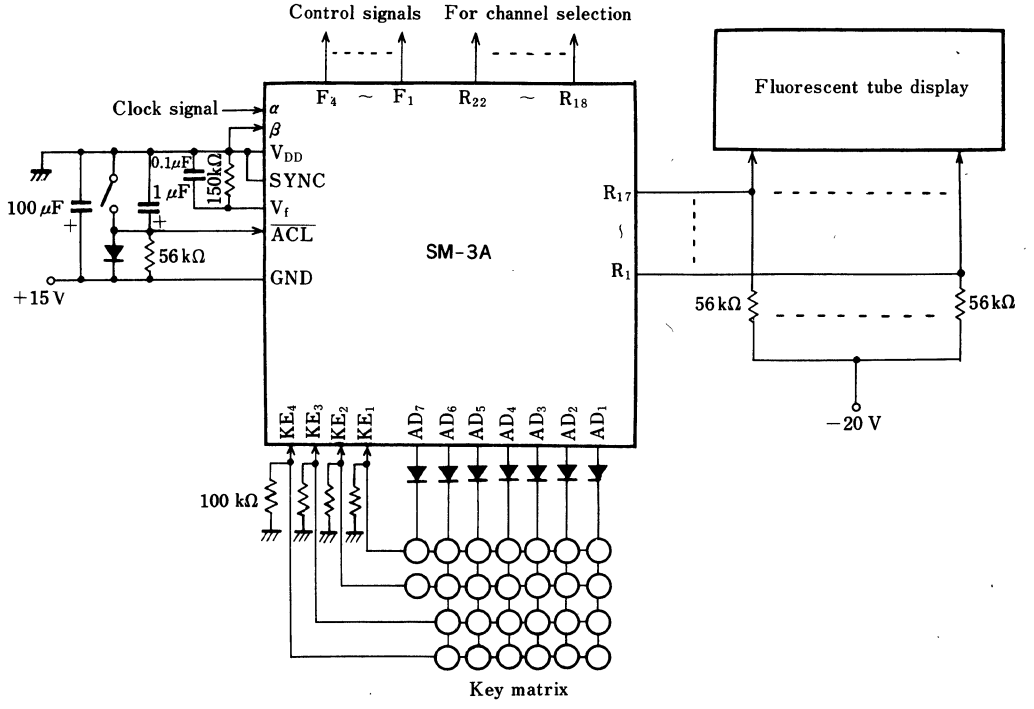
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		-2.5			V	4
	V_{IL1}	$V_{DD} = -13.5V$			-10.0	V	
	V_{IH2}		-0.8			V	5
	V_{IL2}	$V_{DD} = -13.5V$			-10.0	V	
Output voltage	V_{OH1}	$I_O = -2mA$	-2.0			V	6
	V_{OL1}	$R_L = 50k\Omega$ connected to V_N			V_N+1	V	
	V_{OH2}	$I_O = -8mA$	-3.5			V	7
	V_{OL2}	$R_L = 50k\Omega$ connected to V_N			V_N+1	V	
	V_{OH3}	$I_O = -1mA$	-1.0			V	8
	V_{OL3}	$R_L = 50k\Omega$ connected to V_{DD}			$V_{DD}+1$	V	
Supply current	I_{DD}	$V_{DD} = -15.0V$		-12		mA	
Cycle time	t_c			10		μs	

Note 4: Applicable pins $\overline{\alpha}$, β, AK, TAB, $KE_1 \sim KE_4$
Note 5: Applicable pins ACL, V_f SYNC
Note 6: Applicable pins $R_1 \sim R_7$, $F_1 \sim F_4$, IDF
Note 7: Applicable pins $R_8 \sim R_{22}$
Note 8: Applicable pins $AD_1 \sim AD_{10}$

■ Applications

1. Electronic cash register
2. Hard-Hold electronic calculator with printer
3. POS terminal
4. Electronic scale
5. Vending machine
6. Microwave oven controller
7. Electronic sewing machine
8. Controllers of game machines
9. Others electronic appliance controllers

■ System Configuration (for VTR program timer)



SM-100/SM-105 PMOS 4-Bit 1-Chip Microcomputer

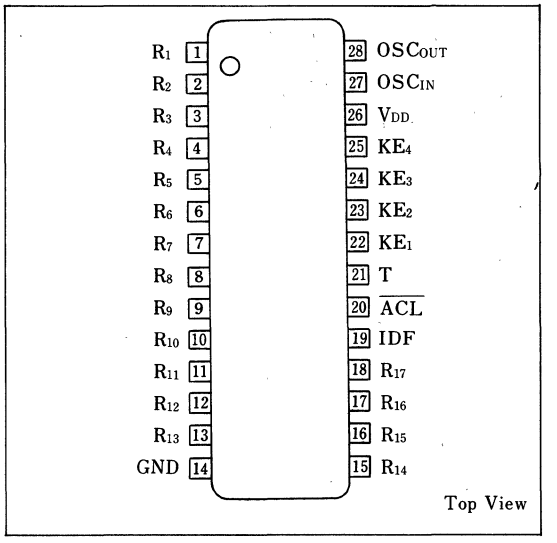
■ Description

The SM-100/SM-105 is a 4-bit single chip PMOS microcomputer with 1,134 bytes of ROM, and 64 words of RAM. It is well suited for low cost systems requiring many I/O control ports.

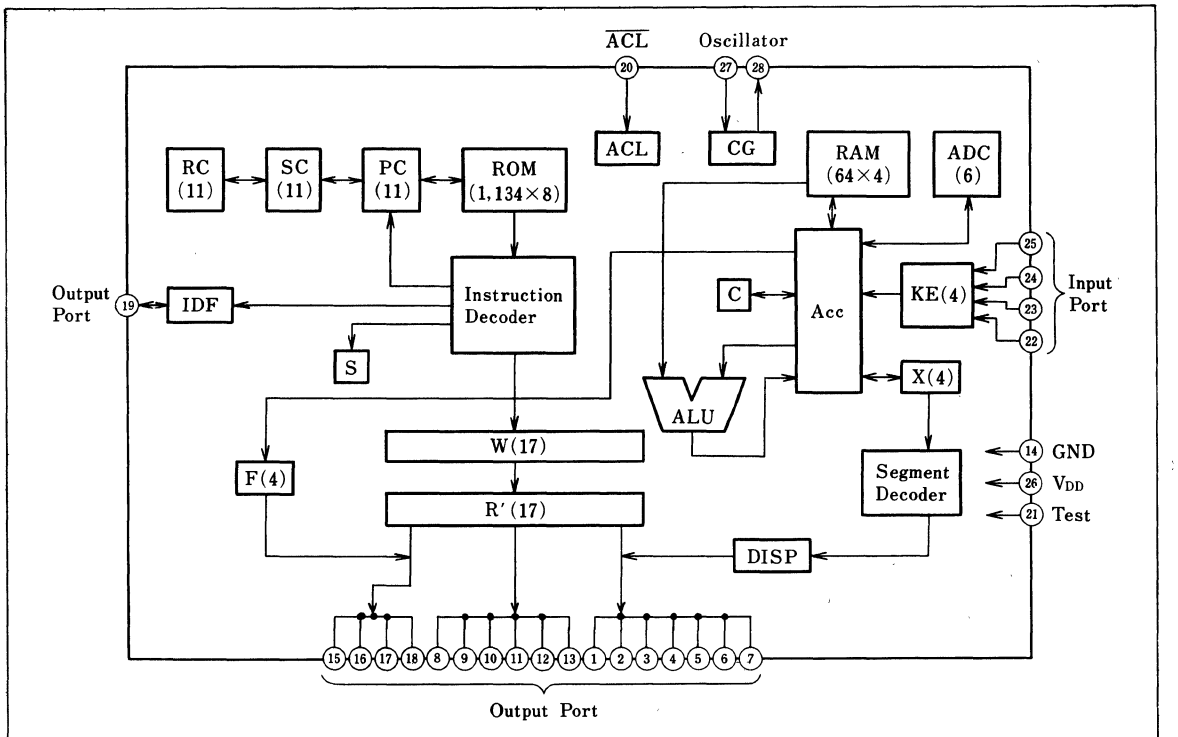
■ Features

1. PMOS process
2. ROM capacity 1,134×8 bits
3. RAM capacity 64×4 bits
4. Instructions 58
5. Subroutine nesting 2 levels
6. Input ports 4 bits
7. Output ports 17 bits
8. Input/Output ports 1 bit
9. On-chip clock generator circuit
10. High voltage outputs (−38V) 18 bits (only SM-100)
11. Single power supply −9V(TYP.)
12. Instruction cycle 10 μs
13. 28-pin dual-in-line package

■ Pin Connections



Block Diagram



Symbol description

ALU	: Arithmetic logic unit	RC	: Stack register of program counter
Acc	: Accumulator	DIV	: Frequency divider
ACL	: Auto clear	CG	: Clock generator
C	: Carry F/F	X	: Temporary register
PC	: Program counter	ADC	: RAM address register
SC	: Stack register of Program counter	S	: Flag F/F

Pin Description

Pin name	I/O	Circuit type	Function
$KE_1 \sim KE_4$	I	Pull down	$A_{CC} \leftarrow KE_1 \sim KE_4$
IDF	I/O	Mid voltage* open drain	Can be set, reset, and tested by instructions
$R_1 \sim R_7$	O	Mid voltage* open drain	Segment output or R register output
$R_8 \sim R_{13}$	O	Mid voltage* open drain	R register output
$R_{14} \sim R_{17}$	O	Mid voltage* open drain	$R_{14} \sim R_{17} \leftarrow A_{CC}$ or R register output
T	I		For test (Connected to V_{DD} normally)
$\overline{ACL}$	I		Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DD}, GND			Power supply for logic circuit

* For SM-100

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{DD}	−12～+0.3	V	1
	V_{IN}	−12～+0.3	V	1,2
	V_{OUT}	−40～+0.3	V	1,3
Operating temperature	T_{opr}	−10～+50	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Apply to pins ACL, K_1-K_4, T, OSC_{IN}, OSC_{OUT}.
Note 3: Apply to pins R_1～R_{17}, IDF.

■ Recommended Operating Conditions

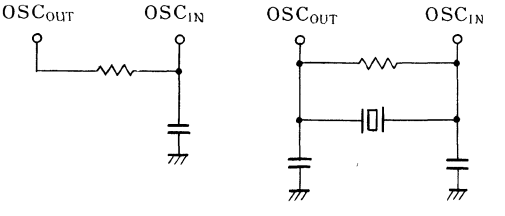
Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−8.1～−9.9	V
Oscillator frequency	f_{osc}	400 (TYP.)	kHz

■ Electrical Characteristics

(V_{DD}=−9.0V±10%, V_N=−38V, Ta=25℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage		V_{IH1}		−1.8			V	4
		V_{IL1}				V_{DD}+1	V	
		V_{IH2}		−0.8			V	5
		V_{IL2}				V_{DD}+1	V	
Output voltage		V_{OH1}	I_{OUT}=−1mA	−1.0			V	6
	SM-100	V_{OL1}	Connect R_L=50kΩ to V_N			V_N+1	V	
	SM-105					V_{DD}+1		
		V_{OH2}	I_{OUT}=−8mA	−1.0			V	7
	SM-100	V_{OL2}	Connect R_L=50kΩ to V_N			V_N+1	V	
	SM-105					V_{DD}+1		
Current consumption		I_{DD}			10		mA	
Oscillator frequency		f_{osc}			400		kHz	8

Note 4: Applied to pins $\overline{KE_1}$～KE_4.
Note 5: Applied to pins $\overline{ACL}$, T, IDF.
Note 6: Applied to pins R_1～R_7, IDF.
Note 7: Applied to pins R_8～R_{17}.
Note 8: Reference oscillation : 10 μs/cycle at 400 kHz



SM-110/SM-115 PMOS 4-Bit 1-Chip Microcomputer

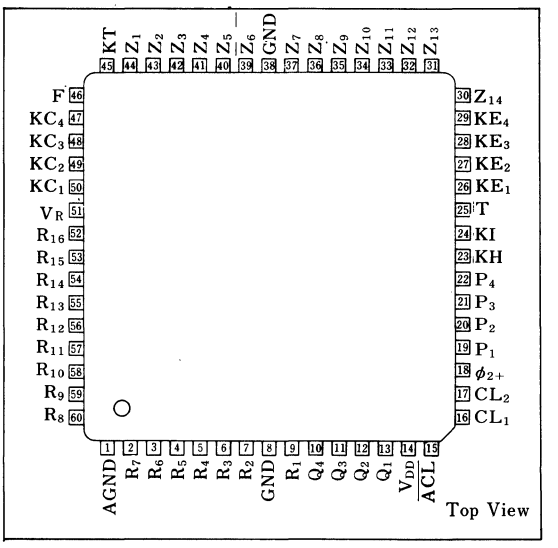
■ Description

The SM-110/SM-115 is a 4-bit single chip PMOS microcomputer with 2,032×9 bits of ROM, 128 words of RAM, and A/D converter. It is well suited for low cost systems requiring many I/O control ports.

■ Features

1. PMOS process
2. ROM capacity 2,032×9 bits
3. RAM capacity 128×4 bits
4. Instructions 90
5. Subroutine nesting 6 levels
6. Input ports 11 bits
7. Output ports 35 bits
8. Input/Output ports 4 bits
9. On-chip clock generator circuit
10. Interrupt function
    - External interrupt 1
    - Timer interrupt 1
11. 8 bits A/D conversion
12. Internal divider (1/50 or 1/60)
13. High voltage outputs (−35V) 21bits (only SM-110)
14. Single power supply −9V (TYP.)
15. Instruction cycle 10 μs
16. 60-pin quad-flat package

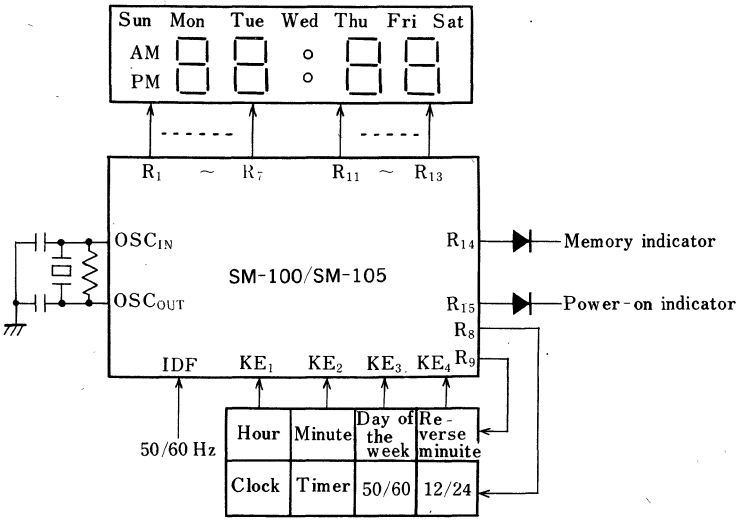
■ Pin Connections



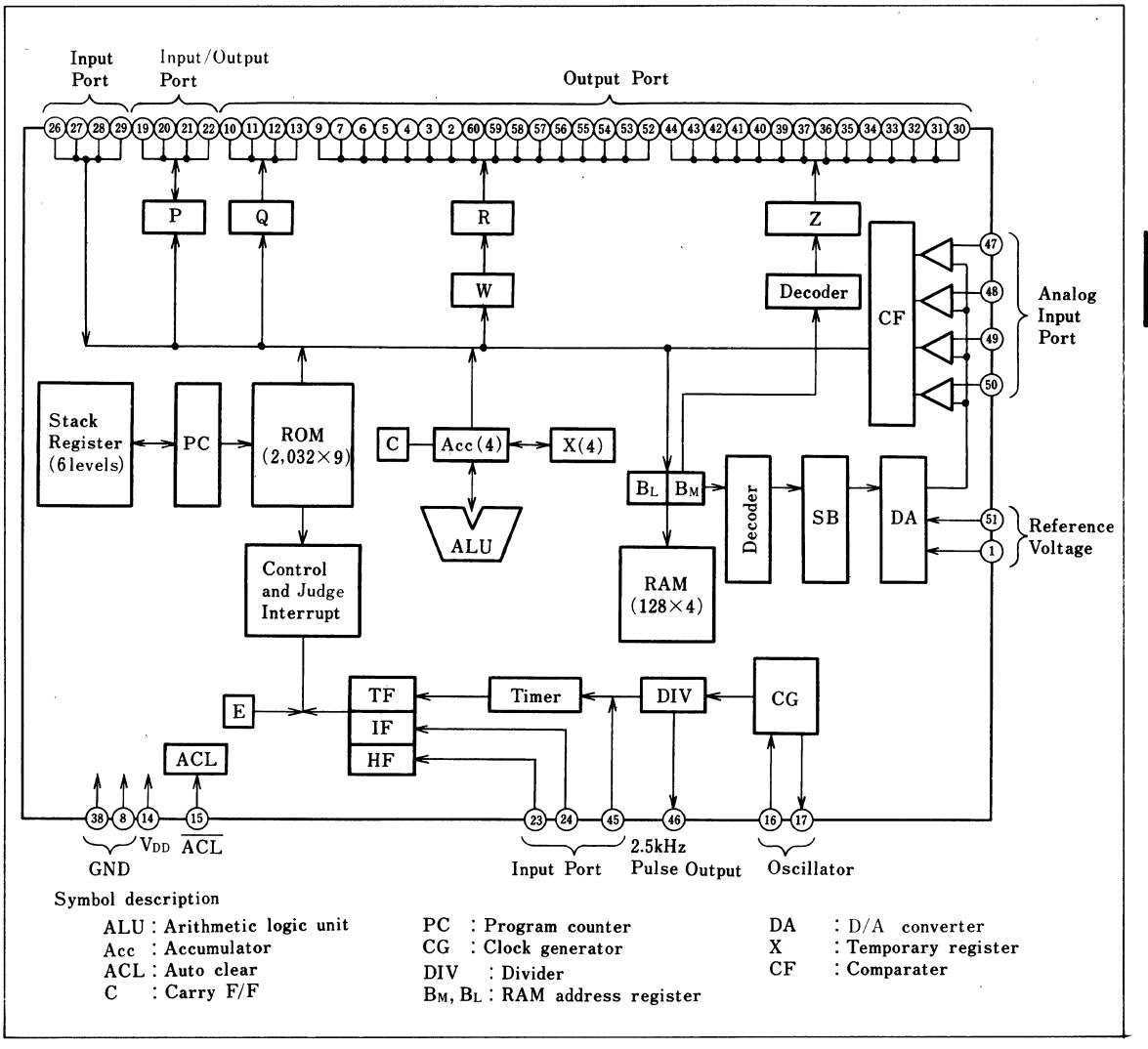
■ Applications

1. Various types of mechanical controllers for video players, vending machines, etc.
2. Game machines

■ System Configuration (Video timer)



■ Block Diagram



Symbol description

ALU : Arithmetic logic unit
Acc : Accumulator
ACL : Auto clear
C : Carry F/F
PC : Program counter
CG : Clock generator
DIV : Divider
B_M, B_L : RAM address register
DA : D/A converter
X : Temporary register
CF : Comparater

Pin Description

Pin name	I/O	Circuit type	Function
$KE_1 \sim KE_4$	I	Pull down	$A_{CC} \leftarrow KE_1 \sim KE_4$
KH	I	Pull down	HF flag set on ↑ ; reset by instruction
KI	I	Pull down	IF flag set on ↑ ; reset by instruction
KT	I	Pull down	External timer signal input (50 or 60Hz)
$KC_1 \sim KC_4$	I		Analog input or $A_{CC} \leftarrow KC_1 \sim KC_4$
$P_1 \sim P_4$	I/O	Open drain	$P_1 \sim P_4 \leftarrow A_{CC}$
$Q_1 \sim Q_4$	O	Mid voltage* open drain	$Q_1 \sim Q_4 \leftarrow A_{CC}$
$R_1 \sim R_{16}$	O	Mid voltage* open drain	R register output
$Z_1 \sim Z_{14}$	O	Mid voltage* open drain	Z register output
T	I		For test (Connected to V_{DD} normally)
$\overline{ACL}$	I		Auto clear
F	O		2.5 kHz pulse output (System clock-100kHz)
ϕ_{2+}	O		Sync signal output
CL_1, CL_2			For clock oscillation
V_R, AGND			A/D conversion standard power supply
V_{DD}, GND			Power supply for logic circuit

* For SM-110, Z_1 pin only is high voltage

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{DD}	−12 ~ +0.3	V	1
	V_{IN}	V_{DD} −0.3 ~ +0.3	V	1,2
	V_{OUT1}	V_{DD} −0.3 ~ +0.3	V	1,3
	V_{OUT2}	−37 ~ +0.3	V	1,4
Operating temperature	T_{opr}	−10 ~ +70	℃	
Storage temperature	T_{stg}	−55 ~ +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Applied to pins $KH_1 \sim KE_4$, $KC_1 \sim KC_4$, $P_1 \sim P_4$, KI, KH, KT.
Note 3: Applied to pins F, $P_1 \sim P_4$, $Z_2 \sim Z_4$.
Note 4: Applied to pins $Q_1 \sim Q_4$, $R_1 \sim R_{16}$, Z_1.

Recommended Operating Conditions

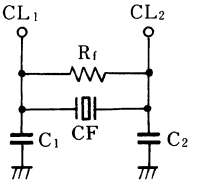
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	−9.9		−8.1	V
Reference voltage	V_R	$5/9\,V_{DD}-0.2$		−4.5	V

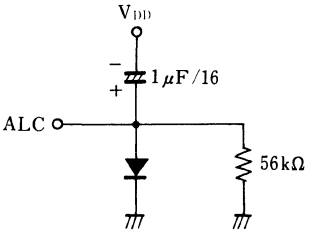
■ Electrical Characteristics

($V_{DD}=-9V\pm10\%$, $V_{N(MAX.)}=-35V$, $Ta=-10\sim70℃$)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage		V_{IH1}		−2			V	1
		V_{IL1}				$V_{DD}+2$	V	1
		V_{IH2}		−0.8			V	2
		V_{IL2}				−4.5	V	2
Output voltage		V_{OH1}	$I_O=-10mA$	−2.5			V	3
	SM-110	V_{OL1}	Connect $R_L=50k\Omega$ to V_N.			V_N+1	V	3
		V_{OH2}	$I_O=-1mA$	−0.2			V	4
	SM-110	V_{OL2}	Connect $R_L=50k\Omega$ to V_N.			V_N+1	V	4
		V_{OH3}	$I_O=-0.5mA$	−1			V	5
		V_{OH4}	$I_O=-0.2mA$	−1			V	6
		V_{OL4}	$I_O=10\ \mu A$			$V_{DD}+1$	V	6
Input current		I_{IH}	$V_{IN}=0V$		180	450	μA	7
		I_R	$V_R=-5V$		900	1200	μA	8
Output current		I_{OL3}	$V_O=V_{DD}$	−1			μA	5
Current consumption		I_{DD}			13	30	mA	10
Oscillator frequency		f_{osc}			400		kHz	11
A/D conversion linear error			$V_R=-5V$ $V_{DD}=-9V$			±3	LSB	
A/D conversion zero error			$V_R=-5V$ $V_{DD}=-9V$			±3	LSB	
A/D coversion full scale error			$V_R=-5V$ $V_{DD}=-9V$			±3	LSB	
A/D conversion overall error			$V_R=-5V$ $V_{DD}=-9V$			±3	LSB	
Reset time		t_{ACL}	At power up	20			ms	12

Note 1: Applied to pins $KE_1\sim KE_3$, $P_1\sim P_4$, KI, KH, KT
Note 2: Applied to pins $KC_1\sim KC_3$. (When used as a digital input), $\overline{ACL}$.
Note 3: Applied to pins $R_{16}\sim R_9$
Note 4: Applied to pins $R_8\sim R_1$, $Q_1\sim Q_3$, Z_2.
Note 5: Applied to pins $P_1\sim P_4$, $Z_{11}\sim Z_1$
Note 6: Applied to pins F.
Note 7: Applied to pins $KE_1\sim KE_3$, KI, KH, KT.
Note 8: Applied to pins V_R. (current flowing into ladder resistance for A/D conversion).
Note 9: Applied to pins $R_{16}\sim R_1$, $P_1\sim P_4$, $Q_1\sim Q_3$, $Z_{11}\sim Z_1$.
Note 10: Measured in no-load condition.
Note 11: Externally connected to oscillation circuit.
CF : Ceramic oscillator
KBR-400B(made by Kyocera Corp.)
R_f : 1MΩ
C_1 : 220pF, C_2 : 220pF



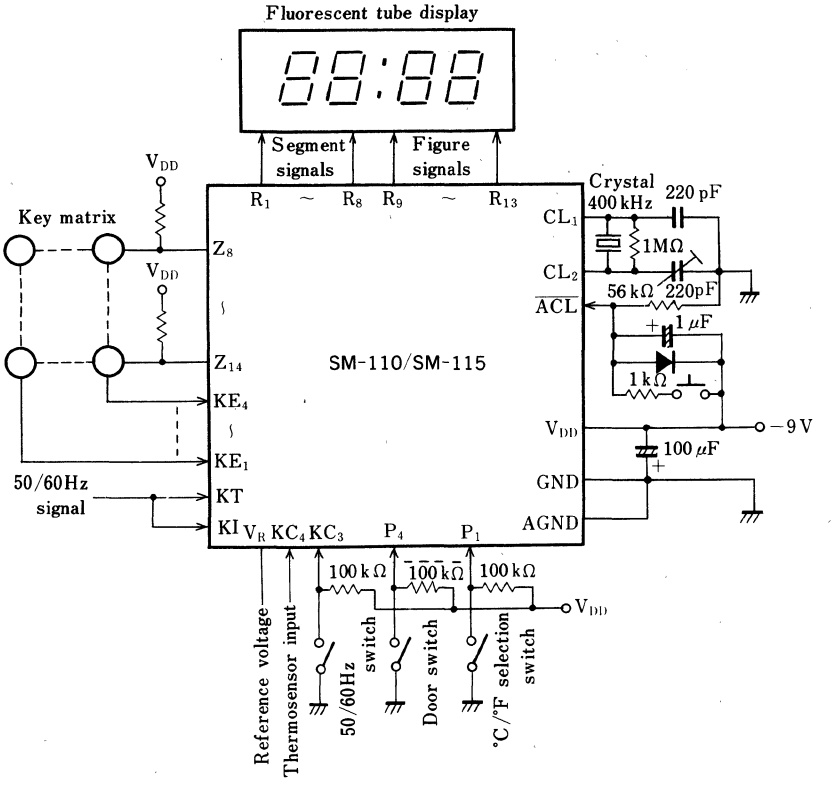


Note 12: The time for reset of "Low" signal that is applied to the $\overline{ACL}$ terminal after supply voltage returns to rated level.

■ Applications

1. Microwave oven controllers
2. Blood pressure monitors
3. Controllers for home appliances and audio equipment

■ System Configuration (Microwave oven controllers)



SM-111/SM-116 PMOS 4-Bit 1-Chip Microcomputer

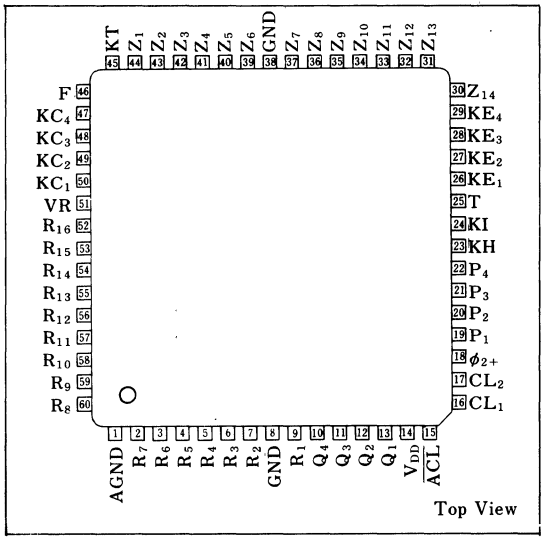
■ Description

The SM-111/SM-116 is a 4-bit single chip PMOS microcomputer with 4,064×9 bits of ROM, 192 words of RAM, and A/D converter. It is well suited for low cost systems requiring many I/O control ports.

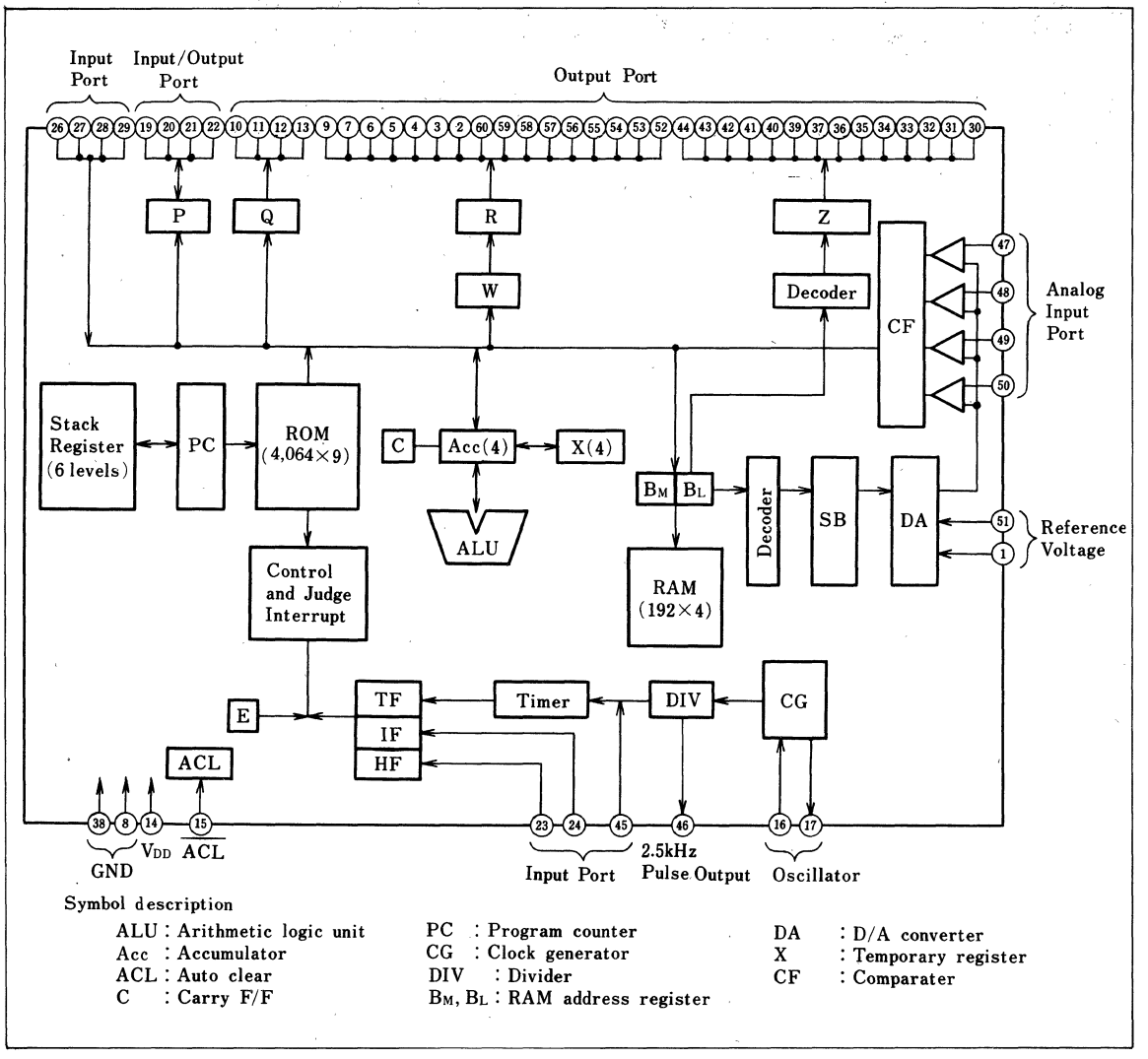
■ Features

1. PMOS process
2. ROM capacity 4,064×9 bits
3. RAM capacity 192×4 bits
4. Instructions 90
5. Subroutine nesting 6 levels
6. Input ports 11 bits
7. Output ports 35 bits
8. Input/Output ports 4 bits
9. On-chip clock generator circuit
10. Interrupt function
    - External interrupt 1
    - Timer interrupt 1
11. 8 bits A/D conversion
12. Internal divider (1/50 or 1/60)
13. High voltage outputs (−35V) 21bits (only SM-111)
14. Single power supply −9V (TYP.)
15. Instruction cycle 10 μs
16. 60-pins quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

ALU : Arithmetic logic unit	PC : Program counter	DA : D/A converter
Acc : Accumulator	CG : Clock generator	X : Temporary register
ACL : Auto clear	DIV : Divider	CF : Comparater
C : Carry F/F	B_M, B_L : RAM address register	

■ Pin Description

Pin name	I/O	Circuit type	Function
$KE_1 \sim KE_4$	I	Pull down	$A_{CC} \leftarrow KE_1 \sim KE_4$
KH	I	Pull down	HF flag set on ↑; reset by instruction
KI	I	Pull down	IF flag set on ↑; reset by instruction
KT	I	Pull down	External timer signal input (50 or 60Hz)
$KC_1 \sim KC_4$	I		Analog input or $A_{CC} \leftarrow KC_1 \sim KC_4$
$P_1 \sim P_4$	I/O	Open drain	$P_1 \sim P_4 \leftarrow A_{CC}$
$Q_1 \sim Q_4$	O	Mid voltage* open drain	$Q_1 \sim Q_4 \leftarrow A_{CC}$
$R_1 \sim R_{16}$	O	Mid voltage* open drain	R register output
$Z_1 \sim Z_{14}$	O	Mid voltage* open drain	Z register output
T	I		For test (Connected to V_{DD} normally)
$\overline{ACL}$	I		Auto clear
F	O		2.5 kHz pulse output (System clock-100kHz)
ϕ_{2+}	O		Sync signal output
CL_1, CL_2			For clock oscillation
V_R, AGND			A/D conversion standard power supply
V_{DD}, GND			Power supply for logic circuit

* For SM-111, Z_1 pin only is high voltage.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{DD}	$-12 \sim +0.3$	V	1
	V_{IN}	$V_{DD}-0.3 \sim +0.3$	V	1,2
	V_{OUT1}	$V_{DD}-0.3 \sim +0.3$	V	1,3
	V_{OUT2}	$-37 \sim +0.3$	V	1,4
Operating temperature	T_{opr}	$-10 \sim +70$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Applied to pins $KE_1 \sim KE_4$, $KC_1 \sim KC_4$, $P_1 \sim P_4$, KI, KH, KT.
Note 3: Applied to pins F, $P_1 \sim P_4$, $Z_2 \sim Z_4$.
Note 4: Applied to pins $Q_1 \sim Q_4$, $R_1 \sim R_{16}$, Z_1.

■ Recommended Operating Conditions

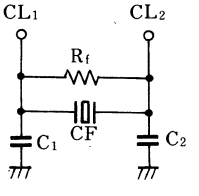
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	-9.9		-8.1	V
Reference voltage	V_R	$5/9\,V_{DD}-0.2$		-4.5	V

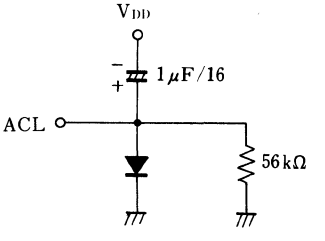
■ Electrical Characteristics

($V_{DD}=-9V\pm10\%$, $V_{N(MAX.)}=-35V$, $Ta=-10\sim70℃$)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage		V_{IH1}		−2			V	1
		V_{IL1}				$V_{DD}+2$	V	1
		V_{IH2}		−0.8			V	2
		V_{IL2}				−4.5	V	2
Output voltage		V_{OH1}	$I_O=-10mA$	−2.5			V	3
	SM-111	V_{OL1}	Connect $R_L=50k\Omega$ to V_N.			V_N+1	V	3
		V_{OH2}	$I_O=-1mA$	−2			V	4
	SM-111	V_{OL2}	Connect $R_L=50k\Omega$ to V_N.			V_N+1	V	4
		V_{OH3}	$I_O=-0.5mA$	−1			V	5
		V_{OH4}	$I_O=-0.2mA$	−1			V	6
		V_{OL4}	$I_O=10\mu A$			$V_{DD}+1$	V	6
Input current		I_{IN}	$V_{IN}=0V$		180	450	μA	7
		I_R	$V_R=-5V$		900	1200	μA	8
Output current		I_{OL3}	$V_O=V_{DD}$	−1			μA	5
Current consumption		I_{DD}			13	30	mA	10
Oscillator frequency		f_{osc}			400		kHz	11
A/D conversion linear error			$V_R=-5V$ $V_{DD}=-9V$			±3	LSB	
A/D conversion zero error			$V_R=-5V$ $V_{DD}=-9V$			±3	LSB	
A/D coversion full scale error			$V_R=-5V$ $V_{DD}=-9V$			±3	LSB	
A/D conversion overall error			$V_R=-5V$ $V_{DD}=-9V$			±3	LSB	
Reset time		t_{ACL}	At power up	20			ms	12

Note 1: Applied to pins $KE_1\sim KE_3$, $P_1\sim P_4$, KI, KH, KT
Note 2: Applied to pins $KC_1\sim KC_4$. (When used as a digital input), $\overline{ACL}$.
Note 3: Applied to pins $R_{16}\sim R_9$
Note 4: Applied to pins $R_8\sim R_1$, $Q_1\sim Q_4$, Z_2.
Note 5: Applied to pins $P_1\sim P_4$, $Z_{11}\sim Z_1$
Note 6: Applied to pin F.
Note 7: Applied to pins $KE_1\sim KE_3$, KI, KH, KT.
Note 8: Applied to pin V_R. (current flowing into ladder resistance for A/D conversion).
Note 9: Applied to pins $R_{16}\sim R_1$, $P_1\sim P_4$, $Q_1\sim Q_4$, $Z_{11}\sim Z_1$.
Note 10: Measured in no-load condition.
Note 11: Externally connected to oscillation circuit.
CF : Ceramic oscillator
KBR-400B(made by Kyocera Corp.)
R_f : 1MΩ
C_1 : 220pF, C_2 : 220pF





Note 12: The time for reset of "Low" signal that is applied to the $\overline{ACL}$ terminal after supply voltage returns to rated level.

SM-114 PMOS 4-Bit 1-Chip Microcomputer

■ Description

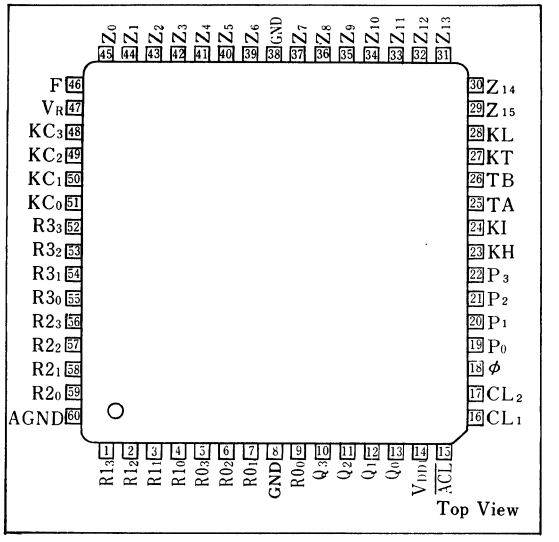
The SM-114 is a 4-bit single chip PMOS microcomputer with 4,064×9 bits of ROM, 192×4 bits of RAM, 8-bit A/D converter, timer/counter and remote control signal receiver.

It is best suited to controllers which measure temperature and humidity of analog value from a sensor.

■ Features

1. PMOS process
2. ROM capacity 4,064×9 bits
3. RAM capacity 192×4 bits
4. Instructions 92
5. Subroutine nesting 6 levels
6. Input ports 8 bits
7. Output ports 17bits
8. Input/Output ports 24 bits
9. Timer/counter
   - 7-bit 1
   - 8-bit 1
10. Interrupt functions
    - External interrupt 1
    - Timer interrupt 2
11. 8-bit A/D conversion
12. Remote control signal receiver
13. Single power supply −9V(TYP.)
14. Instruction cycle 10 μs (TYP.)
15. 60-pin quad-flat package

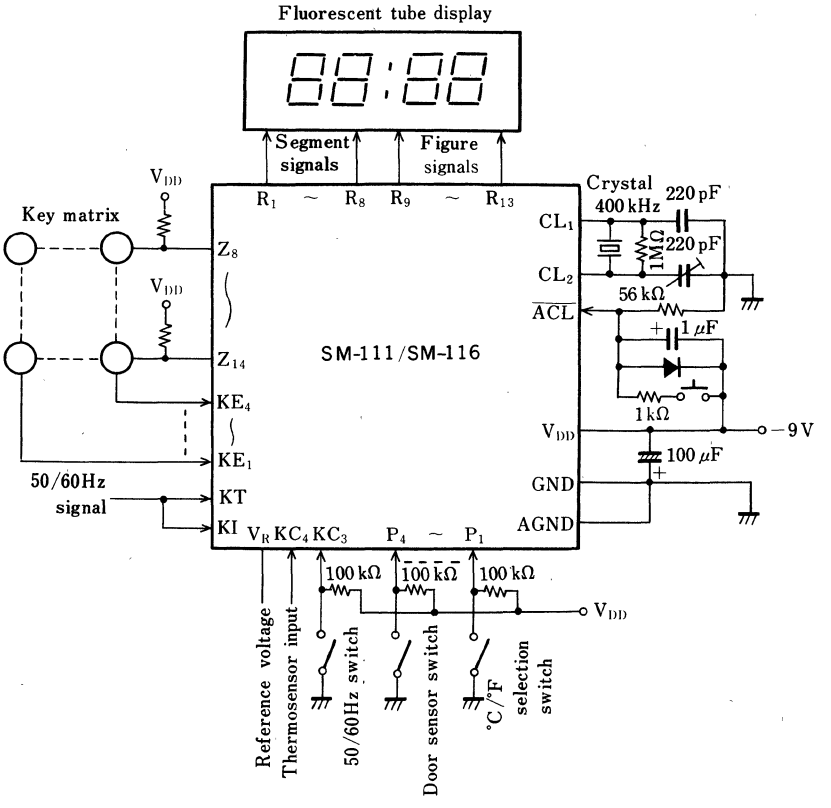
■ Pin Connections



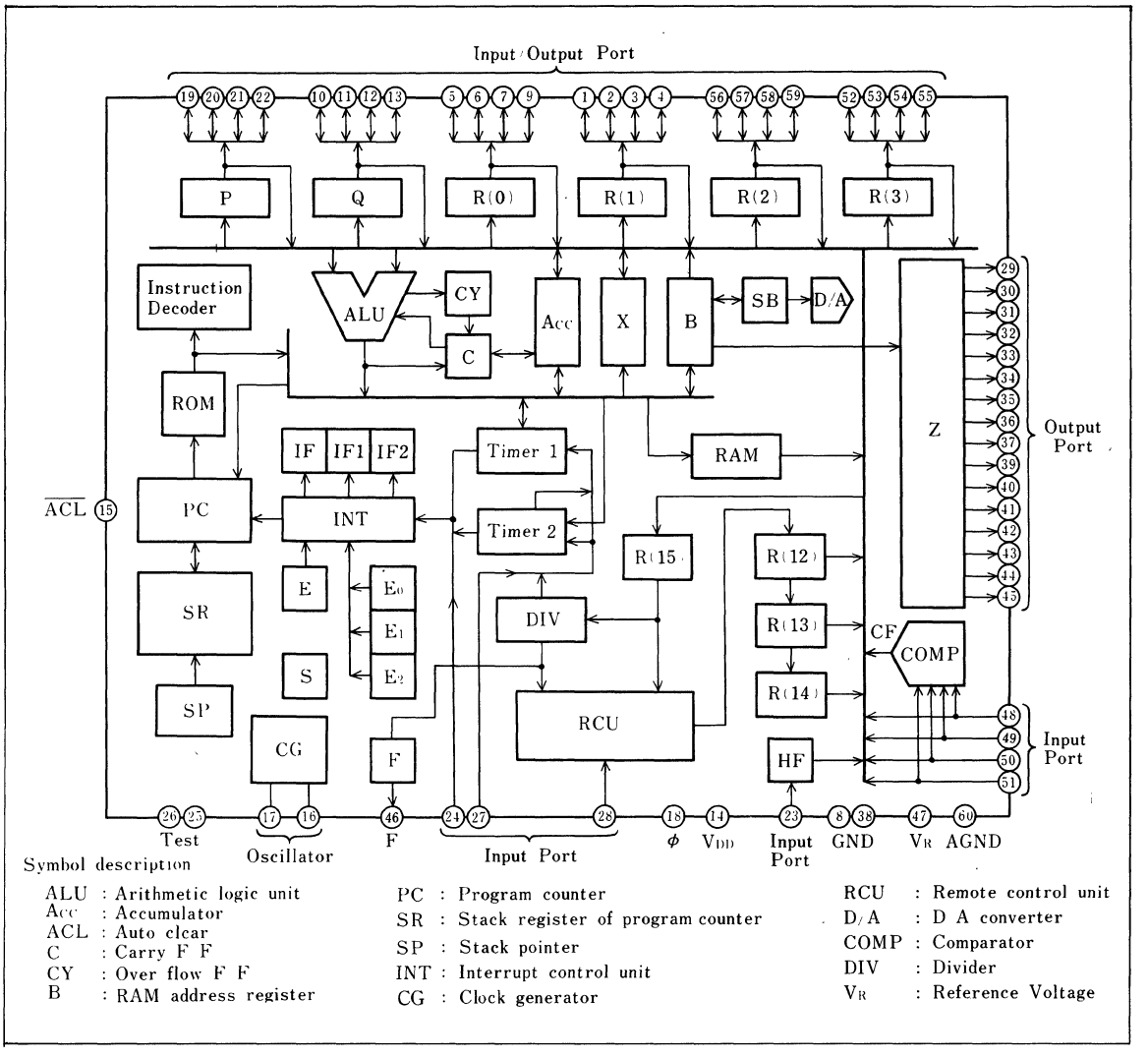
■ Applications

1. Microwave oven controllers
2. Blood pressure monitors
3. Controllers for home appliances and audio equipment

■ System Configuration (Microwave oven controllers)



■ Block Diagram



Symbol description

ALU : Arithmetic logic unit
Acc : Accumulator
ACL : Auto clear
C : Carry F F
CY : Over flow F F
B : RAM address register
PC : Program counter
SR : Stack register of program counter
SP : Stack pointer
INT : Interrupt control unit
CG : Clock generator
RCU : Remote control unit
D/A : D A converter
COMP : Comparator
DIV : Divider
VR : Reference Voltage

■ Pin Description

Pin name	I/O	Circuit type	Function
$KC_0 \sim KC_3$	I		Analog input or Acc←$KC_0 \sim KC_3$
KL	I	Pull down*	For optical remote control circuit
KI, KH	I	Pull down*	IF, HF flag set on ↑
KT	I	Pull down*	External timer signal input
$P_0 \sim P_3$ $Q_0 \sim Q_3$ $R0_0 \sim R3_3$	I/O	Open drain/Pull down*	Acc←→ {$P_0 \sim P_3$, $Q_0 \sim Q_3$, R0, R1, R3} R0, R1, R3←RAM
$Z_0 \sim Z_{15}$	O	Open drain/Pull down*	Can be set, reset individually
F	O		Sound output
TA, TB	I	Pull down	For test (Connected to V_{DD} normally)
$\overline{ACL}$	I		Auto clear
ϕ	O		System clock output
CL_1, CL_2			For clock oscillation
V_R, AGND			A/D coversion standard power supply
V_{DD}, GND			Power supply for logic circuit

*Mask option

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{DD}	$-12 \sim +0.3$	V	1
	V_{IN}	$(V_{DD}-0.3) \sim +0.3$	V	
	V_{OUT}	$(V_{DD}-0.3) \sim +0.3$	V	
Operating temperature	T_{opr}	$-10 \sim +70$	℃	
Storage temperature	T_{stg}	$-50 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

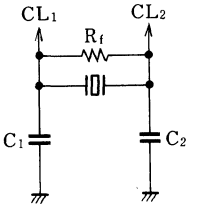
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	−9.9		−8.1	V
Reference voltage	V_R	−4.5		$5/9V_{DD}-0.2$	V

■ Electrical Characteristics

($V_{CC}=-9V\pm10\%$, $Ta=-10\sim70℃$)

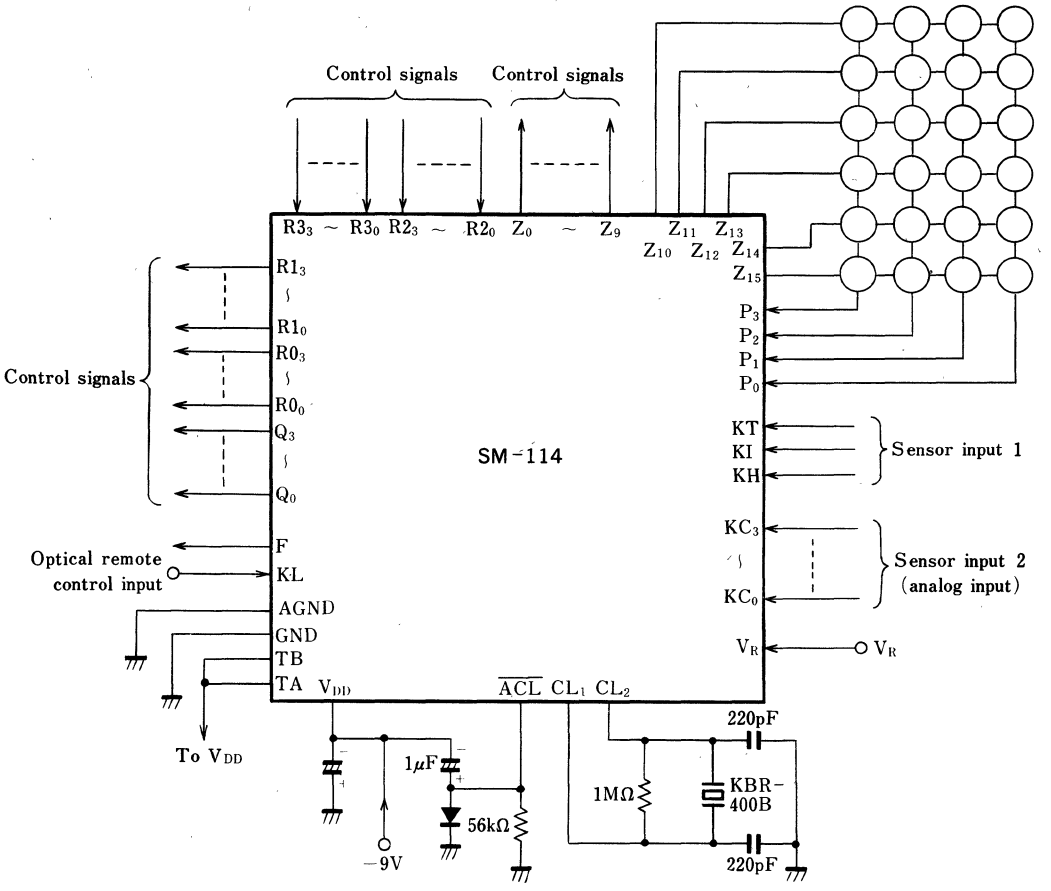
Parameter	Symbol	Conditions	Ratings			Unit	Note
			MIN.	TYP.	MAX.		
Input voltage	V_{IH1}		−1			V	1
	V_{IL1}				$V_{DD}+1$	V	
	V_{IH2}		−2			V	2
	V_{IL2}				$V_{DD}+1$	V	
	V_{IH3}		−0.8			V	3
	V_{IL3}				$V_{DD}+1$	V	
Output voltage	V_{OH1}	$I_O=-2mA$	−1			V	4
	V_{OL1}	$I_O=20\mu A$		$V_{DD}+1$	$V_{DD}+1.5$	V	
	V_{OH2}	$I_O=-2mA$	−1			V	5
	V_{OL2}	$R_L=50k\Omega$			$V_{DD}+1$	V	
Input current	I_{IH1}	$V_{IN}=0V$		180		μA	6
	I_R	$V_R=-5V$		500	900	μA	7
Current consumption	I_{DD}			20		mA	8
Oscillator frequency	f_{OSC}			400		kHz	9
A/D conversion linear error		$V_R=-5V$			±3	LSB	
A/D conversion zero error		$V_R=-5V$			±3	LSB	
A/D conversion full scale error		$V_R=-5V$			±3	LSB	

Note 1: Applied to pins $R0_3\sim R0_0$, $R1_3\sim R1_0$, $R2_3\sim R2_0$, $R3_3\sim R3_0$, $P_3\sim P_0$, $Q_3\sim Q_0$
Note 2: Applied to pins KI, KH, KL, KT
Note 3: Applied to pins $KC_3\sim KC_0$ (when used as a digital input), $\overline{ACL}$.
Note 4: Applied to pins $R0_3\sim R0_0$, $R1_3\sim R1_0$, $R2_3\sim R2_0$, $R3_3\sim R3_0$, $P_3\sim P_0$, $Q_3\sim Q_0$, $Z_{15}\sim Z_0$, F
(when an internal pull-down resistance is attached to R, P, Q, and Z)
Note 5: Applied to pins $R0_3\sim R0_0$, $R1_3\sim R1_0$, $R2_3\sim R2_0$, $R3_3\sim R3_0$, $P_3\sim P_0$, $Q_3\sim Q_0$, $Z_{15}\sim Z_0$
(when an internal pull-down resistance is not attached).
Note 6: Applied to pins $R0_3\sim R0_0$, $R1_3\sim R1_0$, $R2_3\sim R2_0$, $R3_3\sim R3_0$, $P_3\sim P_0$, $Q_3\sim Q_0$, KI, KH, KL, KT
(when an internal pull-down resistance is attached)
Note 7: Applied to pin V_R (current folwing into ladder resistance for A/D conversion)
Note 8: Measured in no-load condition.
Note 9: Externally connected to oscillation circuit



$R_f=1M\Omega$
$C_1=220pF$
$C_2=220pF$

■ System Configuration (Controllers)



SM-120 PMOS 4-Bit 1-Chip Microcomputer

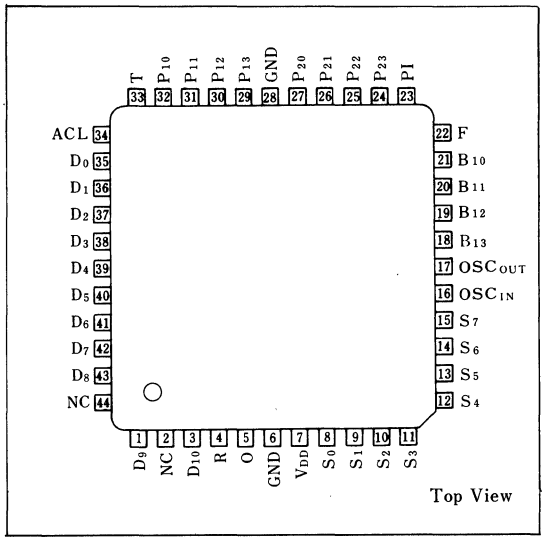
■ Description

The SM-120 is a 4-bit single chip PMOS microcomputer with 1,536 bytes of ROM, 64 words of RAM, and a 17-stage divider. It is well suited for low cost systems requiring many I/O control ports.

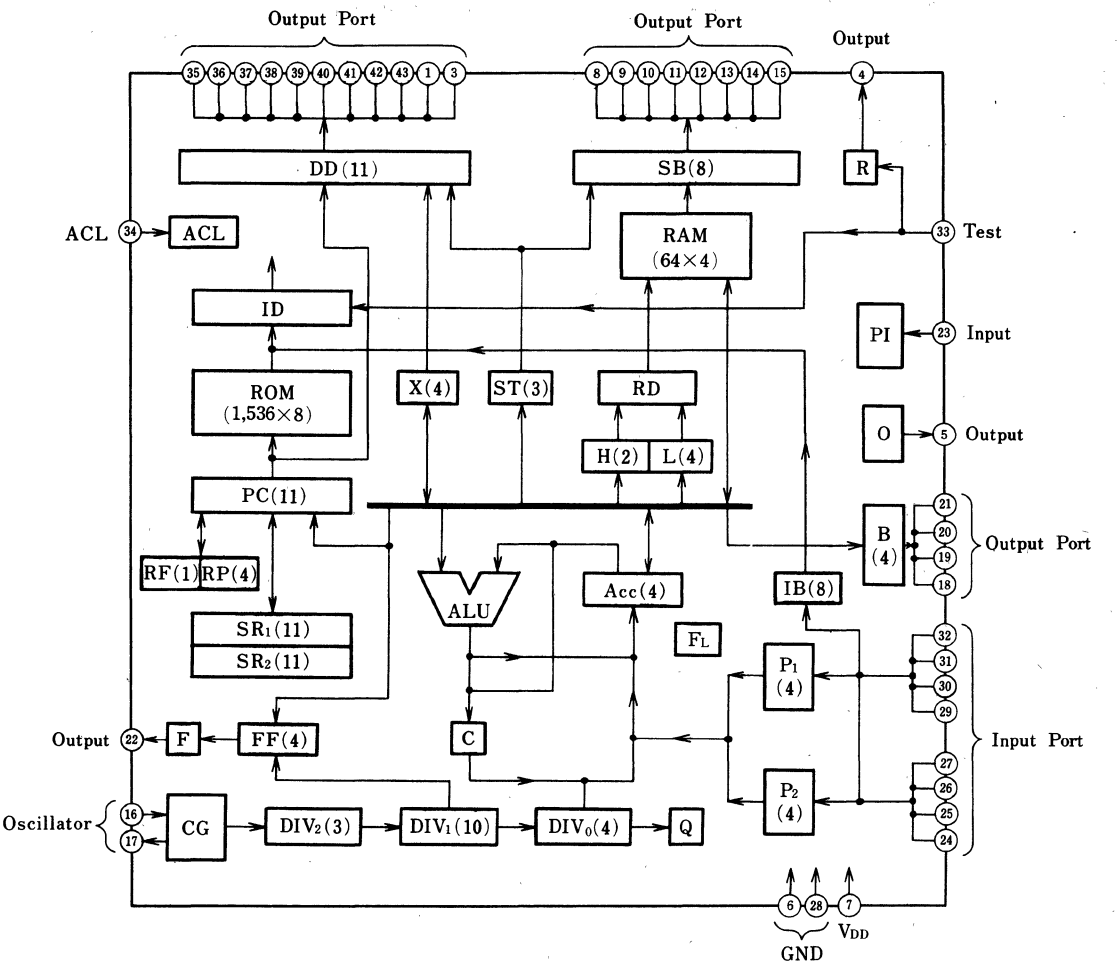
■ Features

1. PMOS process
2. ROM capacity 1,536×8 bits
3. RAM capacity 64×4 bits
4. Instructions 54
5. Subroutine nesting 2 levels
6. Input ports 9 bits
7. Output ports 26 bits
8. External ROM expandable (512×8 bits)
9. On-chip clock generator circuit
10. Internal 17-stage divider with reset (timer circuit)
11. Alarm sound generator circut
12. High voltage outputs (−38V) 19 bits
13. Single power supply −9V (TYP.)
14. Instruction cycle 10 μs
15. 44-pin quad-flat package

■ Pin Connections



Block Diagram



Symbol description

ALU	: Arithmetic logic unit	SR_1, SR_2	: Stack register of program counter
Acc	: Accumulator	DIV_0, DIV_1, DIV_2	: Divider
ACL	: Auto clear	CG	: Clock generator
PC	: Program counter	H, L	: RAM address register

■ Pin Description

Pin	I/O	Type of circuit	Function
P_{10}~P_{13}	I	Pull down	A_{CC}←P_{10}~P_{13}
P_{20}~P_{23}	I	Pull down	A_{CC}←P_{20}~P_{23}
PI	I	Pull down	PI flag set by ↑, reset by command
B_{10}~B_{13}	O	Pull down	B_{10}~B_{13}←A_{CC}
R	O	Pull down	Possible to set, reset, or $\overline{CE}$ signal output
O	O	Pull down	Possible to set and reset
S_0~S_7	O	Open drain	Display segment signal output or internal ROM data output
D_0~D_{10}	O	Open drain	Display digit signal output
F	O	Pull down	Alarm sound output
T	I	Pull down	For test
ACL	I	Pull down	Auto clear
OSC_{IN}, OSC_{OUT}			Clock oscillation
V_{DD}, GND			Power source for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Pin voltage	V_{DD}	−20~+0.3	V	1
	V_{IN}	−20~+0.3	V	1,2
	V_{OUT1}	−20~+0.3	V	1,3
	V_{OUT2}	−40~+0.3	V	1,4
Operating temperature	T_{opr}	−10~+65	℃	
Storage temperature	T_{stg}	−55~+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Applicable to inputs
Note 3: Applicable Pins B_{10}~B_{13}, O, OSC_{OUT}, R, F
Note 4: Applicable Pins D_0~D_{10}, S_0~S_7

■ Operating Conditions

Parameter	Symbol	Specified value	Unit	Note
Supply voltage	V_{DD}	−8.1~−9.9	V	
Oscillator frequency	f_{OSC}	300~800	kHz	5

Note 5: Frequency supplied to OSC_{IN} Pin.

■ Electrical Characteristics

(V_{DD}=−9.0±10%, V_N=−36V, Ta=−10~+65℃)

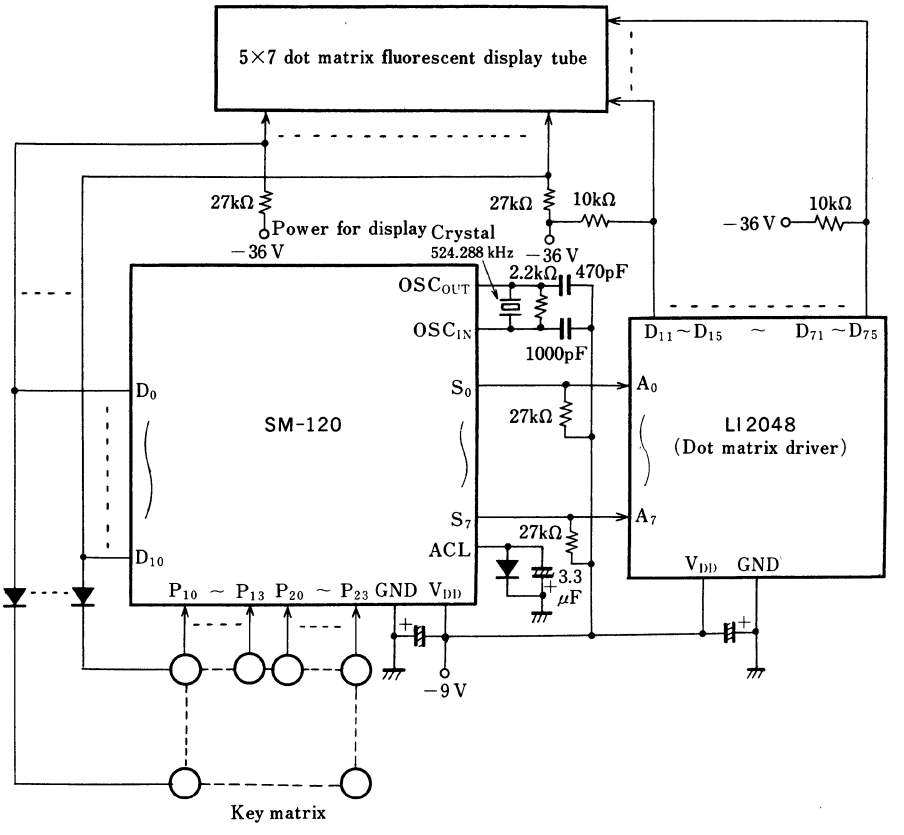
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		−3.5			V	6
	V_{IL1}				−7.0	V	
	V_{IH2}		−1.5			V	7
	V_{IL2}				−7.0	V	
Input current	I_{IH1}	V_{IN}=GND			200	μA	8
	I_{IL1}	V_{IN}=V_{DD}			−10.0	μA	
	I_{IH2}	V_{IN}=GND			700	μA	9
	I_{IL2}	V_{IN}=V_{DD}			−10.0	μA	
	I_{IH3}	V_{IN}=GND			5.0	μA	10
	I_{IL3}	V_{IN}=V_{DD}			−10.0	μA	
Output voltage	V_{OH1}	I_{OH}=−6.0mA	−2.5			V	11
	V_{OL1}	R_L=50kΩ connected to V_N			V_N+1.0	V	
	V_{OH2}	I_{OH}=−2.0mA	−2.0			V	12
	V_{OL2}	R_L=50kΩ connected to V_N			V_N+1.0	V	
	V_{OH3}	I_{OH}=−0.5mA	−3.0			V	
	V_{OL3}	I_{OL}=50 μA			V_{DD}+1.5	V	
	V'_{OL3}	I_{OL}=200 μA			V_{DD}+3.0	V	
	V_{OH4}	I_{OH}=−1.0mA	−1.5			V	14
	V_{OL4}	I_{OL}=50 μA			V_{DD}+1.5	V	
	V'_{OL4}	I_{OL}=200 μA			V_{DD}+3.0	V	
	V_{OH5}	I_{OH}=−1.0mA	−1.5			V	15
	V_{OL5}	I_{OL}=100 μA			V_{DD}+1.5	V	
	V'_{OL5}	I_{OL}=300 μA			V_{DD}+3.0	V	
Current consumption	I_{DD}			20		mA	

Note 6: Applicable pins P_{10}~P_{13}, P_{20}~P_{23}
Note 7: Applicable pins PI, ACL, OSC_{IN}, T
Note 8: Applicable pins P_{10}~P_{18}, P_{20}~P_{23}, PI, T
Note 9: Applicable pin ACL
Note 10: Applicable pin OSC_{IN}
Note 11: Applicable pins D_{10}~D_{13}
Note 12: Applicable pins S_0~S_7
Note 13: Applicable pins B_{10}~B_{13}, F
Note 14: Applicable pins R, O
Note 15: Applicable pin OSC_{OUT}

■ Applications

1. VTR timer
2. Electronic home appliance controller
3. Game machine

■ System Configuration (for 5 × 7 dot matrix fluorescent display tube drive)



SM-200 NMOS 4-Bit 1-Chip Microcomputer

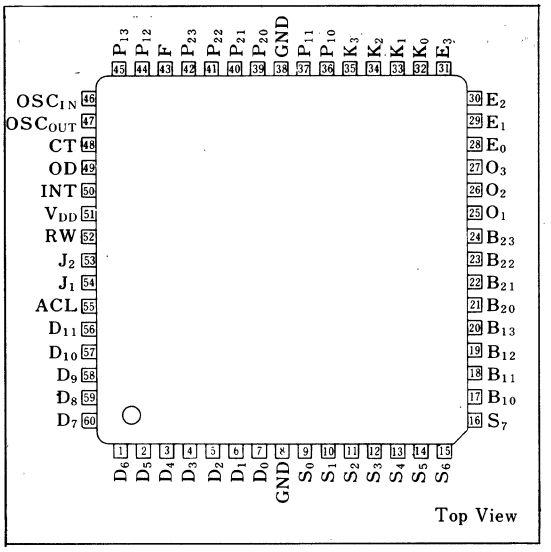
■ Description

The SM-200 is 4-bit single chip NMOS microcomputer with 3,072×9 bits of ROM, 132 words of RAM, automatic display circuit, and a 16-stage divider. It is well suited for low cost systems requiring many I/O control ports.

■ Features

1. NMOS process
2. ROM capacity 3,072×9 bits
3. RAM capacity 128×4+16 bits
4. Instructions 100
5. Subroutine nesting 3 levels
6. Input ports 10 bits
7. Output ports 37 bits
8. Input/Output ports 4 bits
9. Enable 8 bits parallel input/output
10. Externally ROM/RAM expandable
11. External interrupt function
12. Internal 16-stage divider with reset (timer circuit)
13. Serial interfaces 8 bits
14. On-chip clock generator circuit
15. Single power supply 5V (TYP.)
16. Instruction cycle 10 μs
17. 60-pin quad-flat package

■ Pin Connections



■ Pin Description

Pin	I/O	Type of circuit	Function
$K_0 \sim K_3$	I	Pull down	$Acc_1 \leftarrow K_0 \sim K_3$
J_1	I		Set by ↑, reset of after test instruction execution
J_2	I		Internal clock period type, test possible
CT	I	Open	For pulse count per unit time
$P_{10} \sim P_{13}$	I	Pull down	$Acc_1 \leftarrow P_{10} \sim P_{13}$, Instruction code input for external ROM
$P_{20} \sim P_{23}$	I/O	Pull down for input	$Acc_2 \leftarrow P_{20} \sim P_{23}$, Instruction code input for external ROM data transter from/to RAM for external RAM
RW	O		Set, reset by instruction ; chip select for external ROM Connected to RW pin for external RAM
OD	O		Set, reset by instruction ; Instruction code input for external ROM ; connected to OD pin for external RAM
$E_0 \sim E_3$	O		$E_0 \sim E_3 \leftarrow A_{CC1}$
$B_{10} \sim B_{13}$	O		$B_{10} \sim B_{13} \leftarrow A_{CC1}$
$B_{20} \sim B_{23}$	O		$B_{20} \sim B_{23} \leftarrow A_{CC2}$
$O_1 \sim O_3$	O		Set, reset by instruction
$D_0 \sim D_{11}$	O		Display digit signal output ; Address signal output for external ROM, RAM
$O_0 \sim O_7$	O		Display segment signal output
F	O		Alarm sound output
INT	I	Pull down	Set of INT F/F by ↑
ACL	I	Pull down	Auto clear
OSC_{IN}, OSC_{OUT}			Clock oscillation
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

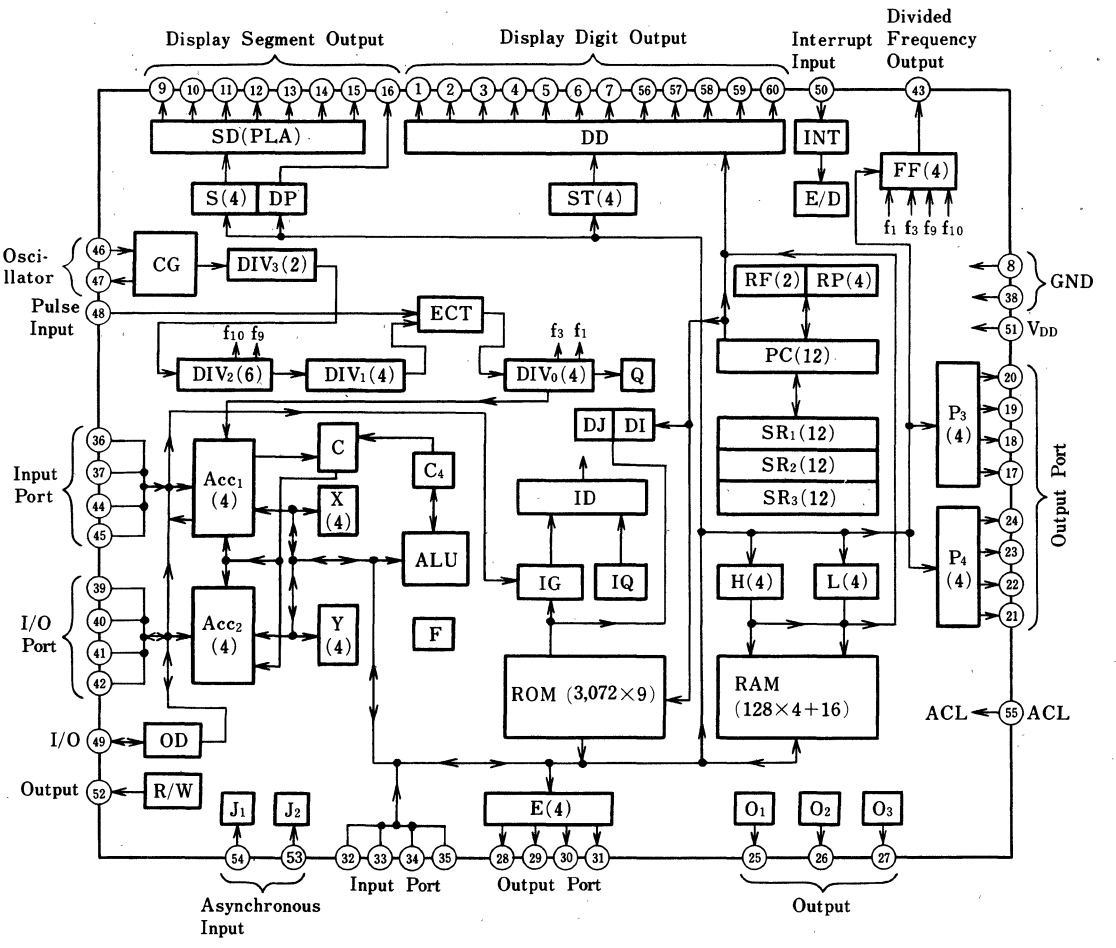
Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{DD}	$-0.5 \sim +7$	V	1
	V_{IN}	$-0.5 \sim V_{DD}+0.3$	V	
Operating temperature	T_{opr}	$-10 \sim +65$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to V_{SS} (GND)

■ Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	4.5～5.5	V
Oscillator frequency	f_{OSC}	262.144	kHz

■ Block Diagram



Symbol description

ALU	: Arithmetic logic unit	CG	: Clock generator
Acc_1, Acc_2	: Accumulator	DIV	: Divider
ACL	: Auto clear	H,L	: RAM address register
C	: Carry F/F	SD	: Segment decoder
PC	: Program counter	DD	: Digit decoder
SR_1, SR_2, SR_3	: Stack register of program counter	X,Y	: Temporary register

■ Electrical Characteristics

(V_{DD}=5V, V_{SS}=GND, f_{OSC}=262kHz, Ta=25℃)

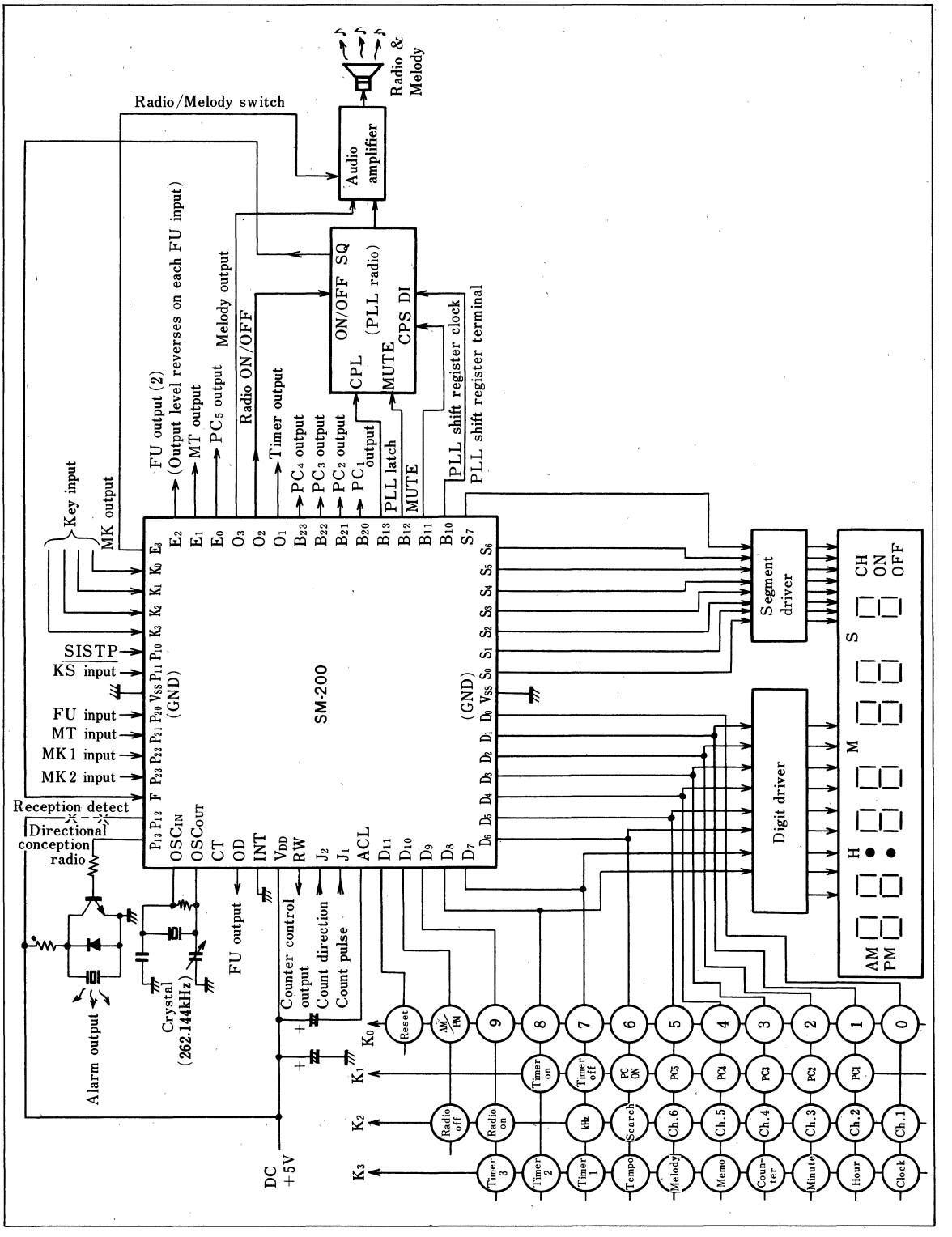
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		2.4		5	V	2
	V_{IL1}		0		0.5	V	
	V_{IH2}		2.4		5	V	3
	V_{IL2}		0		0.6	V	
Input current	I_{IH1}	V_{IN}=5V		15	50	μA	4
	I_{IL1}	V_{IN}=GND		−1	−10	μA	
	I_{IH2}	V_{IN}=5V		1	10	μA	5
	I_{IL2}	V_{IN}=GND		−1	−10	μA	
	I_{IH3}	V_{IH}=5V		5	25	μA	6
	I_{IH4}			15	50	μA	7
	I_{IL4}					μA	
Output voltage	V_{OH1}	I_{OH}=10 μA	3.6		5	V	8
	V'_{OH1}	I_{OH}=0.2mA	2.4		5	V	
	V_{OL1}	$\|I_{OL}\|$=0.15mA	0		0.5	V	
	V_{OH2}	I_{OH}=25 μA	3.6		5	V	9
	V'_{OH2}	I_{OH}=0.6mA	2.4		5	V	
	V_{OL2}	$\|I_{OL}\|$=0.25mA	0		0.5	V	
	V_{OH3}	I_{OH}=10 μA	3.6		5	V	10
	V'_{OH3}	I_{OH}=0.4mA	2.4		5	V	
	V_{OL3}	$\|I_{OL}\|$=0.3mA	0		0.5	V	
	V_{OH4}	I_{OH}=10 μA	3.6		5	V	11
	V'_{OH4}	I_{OH}=0.3mA	2.4		5	V	
	V_{OL4}	$\|I_{OL}\|$=0.3mA	0		0.5	V	
	V_{OH5}	I_{OH}=10 μA	3.5		5	V	12
	V'_{OH5}	I_{OH}=0.3mA	2.4		5	V	
	V_{OL5}	$\|I_{OL}\|$=50 μA	0		0.5	V	
	V_{OH6}	I_{OH}=0.2mA	2.4		5	V	13
	V_{OL6}	$\|I_{OL}\|$=0.25mA	0		0.5	V	
	V_{OH7}	I_{OH}=0.15mA	2.4		5	V	14
	V_{OL7}	$\|I_{OL}\|$=0.15mA	0		0.5	V	
	V_{OH8}	I_{OH}=50 μA	3.6		5	V	15
	V_{OL8}	$\|I_{OL}\|$=50 μA	0		0.5	V	
Current consumption	I_{DD}	Open all input and output pins		32	56	mA	

Note 2: Applicable pins P_{10}~P_{13}, J_1~J_2, INT, CT, ACL, P_{20}~P_{23} in input mode, OD in input mode.
Note 3: Applicable pins K_0~K_3
Note 4: Applicable pins P_{10}~P_{13}, K_0~K_3, J_1, J_2, INT, P_{20}~P_{23} in input mode, OD in input mode
Note 5: Applicable pin CT
Note 6: Applicable pin OSC_{IN}
Note 7: Applicable pin ACL
Note 8: Applicable pins B_{10}~B_{13}, B_{20}~B_{23}, E_0~E_3, O_1~O_3
Note 9: Applicable pins S_0~S_7
Note 10: Applicable pin RW
Note 11: Applicable pin F
Note 12: Applicable pins D_0~D_{11}
Note 13: Applicable pin OD in output mode
Note 14: Applicable pins P_{20}~P_{23} in output mode
Note 15: Applicable pin OSC_{OUT}

■ Applications

1. General-purpose program timer
2. Controllers for electronic home appliances, Audio equipment, Office machines
3. Door chime, Home security system
4. Hand-held calculator with printer
5. Cash register
6. Copy machine controller
7. Vending Machine
8. Radio cassette tape recorder and PLL controller
9. TV remote control and channel controller

System Configuration (for multipurpose controller)



SM-4A CMOS 4-Bit 1-Chip Microcomputer

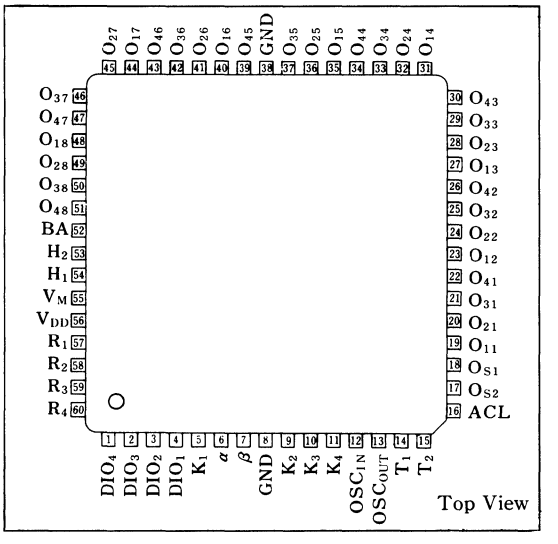
■ Description

The SM-4A is a 4-bit single chip CMOS microcomputer with 2,268 bytes of ROM, 96 words of RAM, a 15-stage divider and 68-segment liquid crystal driver circuits. It is well suited for applications of low power hand-held equipment with many liquid crystal display segments.

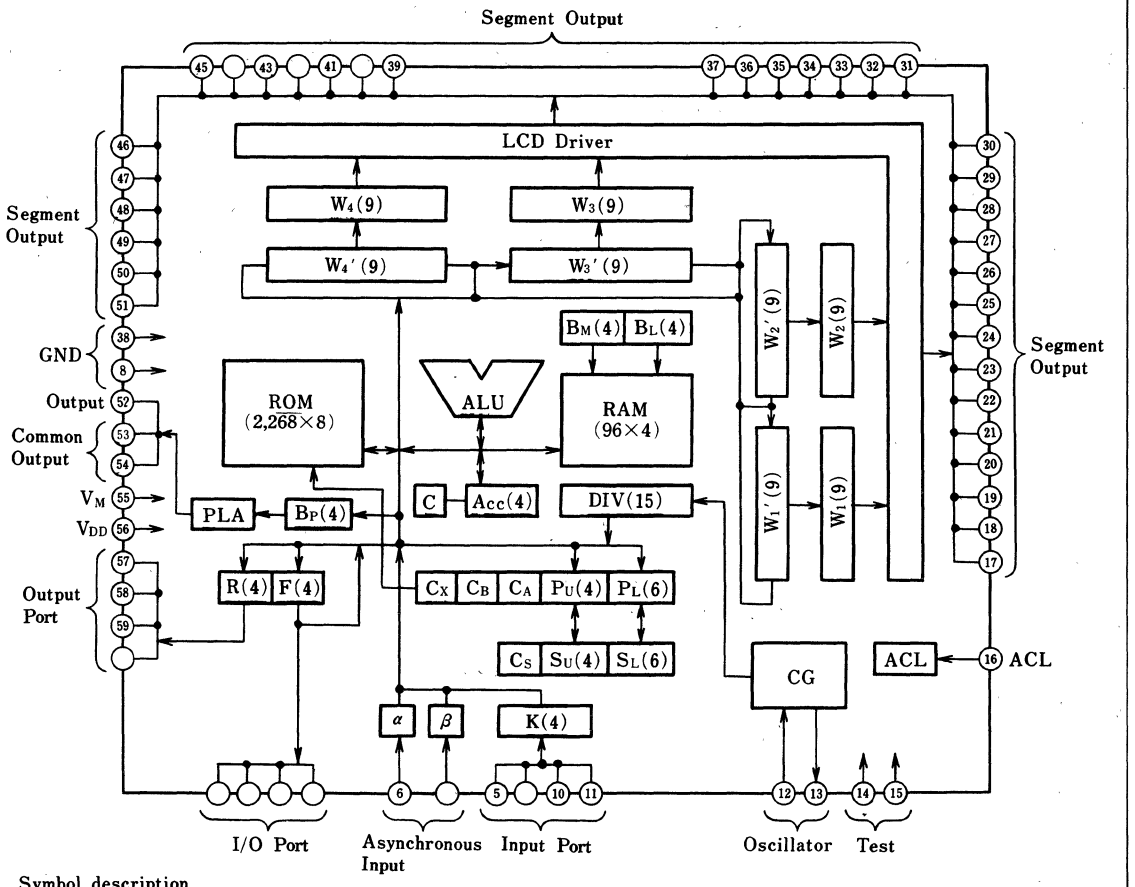
■ Features

1. CMOS process
2. ROM capacity 2,268×8 bits
3. RAM capacity 96×4 bits
4. Instructions 54
5. Subroutine nesting 1 level
6. Input ports 6 bits
7. Output ports 40 bits
8. Input/Output ports 4 bits
9. On-chip 50-stage divider with reset (timer circuit)
10. External RAM driver (256×4 bits)
11. Direct LCD driver circuits (3V, 1/2 duty, 1/2 bias and 68 segments MAX.)
12. Standby mode (10 μA current consumption)
13. Single power supply −3V (TYP.)
14. Instruction cycle 61 μs
15. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

ALU	: Arithmetic logic unit	B_M, B_L	: RAM address register
Acc	: Accumulator	DIV	: Frequency divider
ACL	: Auto clear	PLA	: Programable logic array
C	: Carry F/F	CG	: Clock generator
C_X, C_A, P_U, P_L	: Program counter	$W_1 \sim W_4$, $W_1' \sim W_4'$	: Static shift register
C_S, S_U, S_L	: Stack register of program counter		

Pin Description

Pin	I/O	Type of circuit	Function
$K_1 \sim K_4$	I	Pull down	Acc←$K_1 \sim K_4$
α	I	Pull down	Set by ↑, reset after test instruction execution
β	I	Pull down	Input signal is held for 1 instruction, test possible
$DIO_1 \sim DIO_4$	I/O	3-state output	Acc↔$DIO_1 \sim DIO_4$
$R_1 \sim R_4$	O	Complementary	$R_1 \sim R_4$←Acc
$O_{11} \sim O_{48}$ OS_1, OS_2	O		Output of W and W' registers' content ; used for LCD segment output
H_1, H_2	O		3-state level output possible, used for LCD common output
BA	I	Pull up	For low voltage detection circuit
T_1, T_2	I		For test (usually connected to V_{DD})
ACL	I		Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_M			Power supply for LCD driver
GND, V_{DD}			Power supply for logic circuit

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{DD}	−3.5 ~ +0.3	V	1
	V_M	−3.5 ~ +0.3	V	
	V_{IN}	V_{DD}−0.3 ~ +0.3	V	
Operating temperature	T_{opr}	−5 ~ +55	℃	
Storage temperature	T_{stg}	−55 ~ +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.

Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	−3.2 ~ −2.6	V
Supply voltage	V_M	$V_{DD}/2$ (TYP.)	V
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz

■ Electrical Characteristics

(V_{DD}=−3.2～−2.6V, Ta=25℃)

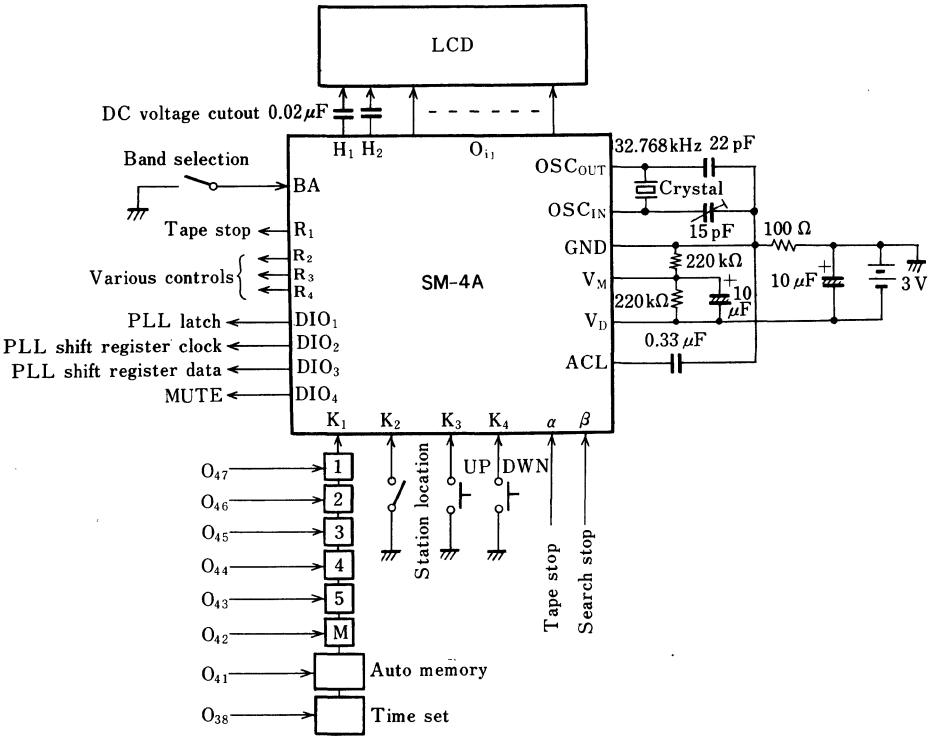
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		−0.6			V	2
	V_{IL1}				V_{DD}+0.6	V	
	V_{IH2}		−0.3			V	3
	V_{IL2}				V_{DD}+0.3	V	
Output voltage	V_{OH1}	I_{OUT}=50 μA to V_{DD}	−0.5			V	4
	V_{OL1}	I_{OUT}=5 μA to GND			V_{DD}+0.5	V	
	V_{OH2}	I_{OUT}=50 μA to V_{DD}	−0.5			V	5
	V_{OL2}	I_{OUT}=30 μA to GND			V_{DD}+0.5	V	
	V_{OH3}	I_{OUT}=50 μA to V_{DD}	−0.5			V	6
	V_{OL3}	I_{OUT}=50 μA to GND			V_{DD}+0.5	V	
	V_{OA}	No load	−0.3			V	7
	V_{OB}	V_{DD}=−3.0V		−1.5		V	
	V_{OC}	V_M=−1.5V			−2.7	V	
Output current	I_{SO}	V_{OUT}=−0.2V	100			μA	8
	I_{SIN}	V_{OUT}=V_{DD}+0.2V	100			μA	
Current consumption	I_{DA}	In full-range operation		50	100	μA	
	I_{DS}	When system clock is stationary		10	20	μA	

Note 2: Applicable pins K_1, K_2, K_3, K_4, α, β
Note 3: Applicable pin ACL
Note 4: Applicable pins O_{48}～O_{11}, O_{S1}, O_{S2}
Note 5: Applicable pins DIO_1～DIO_4
Note 6: Applicable pins R_2, R_3, R_4
Note 7: Applicable pins H_1, H_2
Note 8: Applicable pin R_1

■ Applications

1. Hand-held calculator with clock function
2. High-quality clock
3. Cash register
4. General-purpose timer
5. Electronic scale
6. Game machine
7. Vending machine
8. Controllers for electronic home appliances and audio equipment

■ System Configuration (for radio PLL controller)



SM-5A CMOS 4-Bit 1-Chip Microcomputer

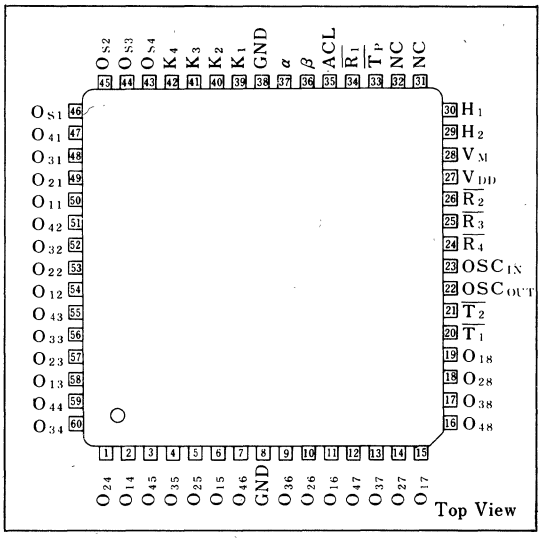
■ Description

The SM-5A is a 4-bit single chip CMOS microcomputer with 1,827 bytes of ROM, 65 words of RAM, a 15-stage divider and 72-segment liquid crystal driver circuit. It is well suited for applications of low power hand-held equipment with many liquid crystal display segments.

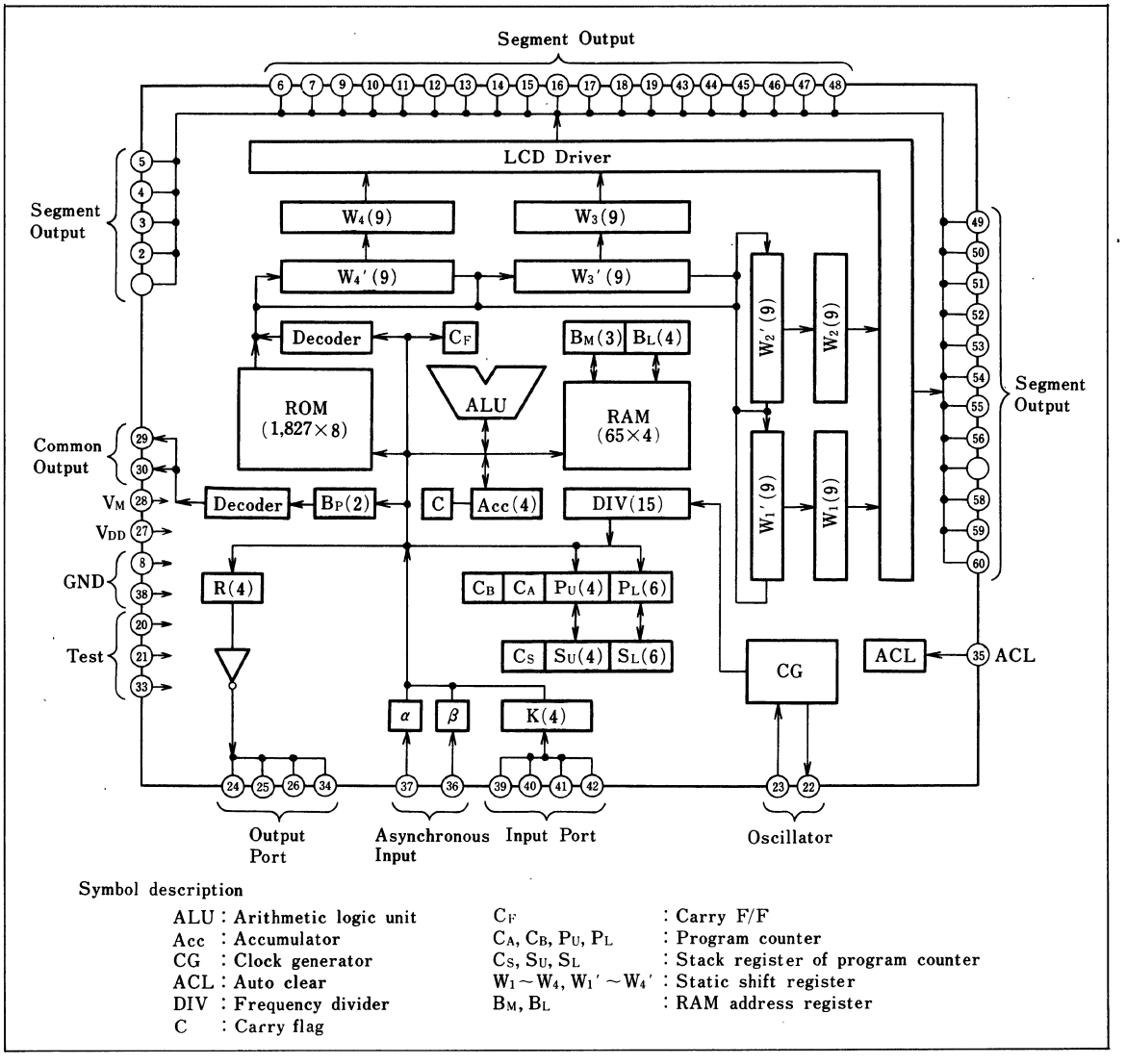
■ Features

1. CMOS process
2. ROM capacity 1,827×8 bits
3. RAM capacity 65×4 bits
4. Instructions 51
5. Subroutine nesting 1 level
6. Input ports 6 bits
7. Output ports 42 bits
8. On-chip 15-stage divider with reset (timer circuit)
9. Direct LCD driver circuit (3V, 1/2 duty, 1/2 bias and 72 segments MAX.)
10. On-chip crystal-controlled oscillator (32.768kHz)
11. Standby mode (10 μA current consumption)
12. Single power supply −3V (TYP.)
13. Instruction cycle 61 μs
14. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

ALU	: Arithmetic logic unit	C_F	: Carry F/F
Acc	: Accumulator	C_A, C_B, P_U, P_L	: Program counter
CG	: Clock generator	C_S, S_U, S_L	: Stack register of program counter
ACL	: Auto clear	$W_1 \sim W_4$, $W_1' \sim W_4'$	: Static shift register
DIV	: Frequency divider	B_M, B_L	: RAM address register
C	: Carry flag		

■ Pin Description

Pin	I/O	Type of circuit	Function
$K_1 \sim K_4$	I	Pull down	Acc←$K_1 \sim K_4$
α, β	I	Pull up	Independent test possible
$O_{11} \sim O_{48}$ $O_{S1} \sim O_{S4}$	O		Output of contents of W and W′ registers ; used for output of LCD segment
H_1, H_2	O		3-state level output possible ; used for LCD common output
$\overline{R_1} \sim \overline{R_4}$	O		$\overline{R_1} \sim \overline{R_4}$←Acc, $\overline{R_1}$…Control output or alarm sound output
$\overline{T_P}$	I		For test (usually open)
$\overline{T_1}$, $\overline{T_2}$	I		For test (usually connected to GND)
ACL	I		Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_M			Power supply for LCD driver
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Pin voltage	V_{DD}	−3.5～+0.3	V	1
	V_M	−3.5～+0.3	V	
	V_{IN}	V_{DD}−0.3～+0.3	V	
Operating temperature	T_{opr}	−5～+50	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND (GND=0V)

■ Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	−3.3～−2.7	V
Supply voltage	V_M	$V_{DD}/2$ (TYP.)	V
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz

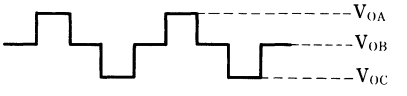
■ Electrical Characteristics

($V_{DD}=-3.0V\pm10\%$, GND=0V, Ta=25℃)

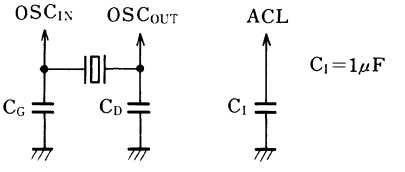
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.6			V	2
	V_{IL}				$V_{DD}+0.6$	V	
Input current	I_{IH1}	$V_{IN}=0V$			15	μA	3
	I_{IL1}	$V_{IN}=-3.0V$			1.5	μA	
	I_{IH2}	$V_{IN}=0V$			1	μA	4
	I_{IL2}	$V_{IN}=-3.0V$			1	μA	
Output voltage	V_{OH1}	$I_{OUT}=30$ μA to V_{DD}	−0.5			V	5
	V_{OL1}	$I_{OUT}=10$ μA to GND			$V_{DD}+0.5$	V	
	V_{OH2}	$I_{OUT}=100$ μA to V_{DD}	−0.5			V	6
	V_{OL2}	$I_{OUT}=100$ μA to GND			$V_{DD}+0.5$	V	
	V_{OA}	No load $V_M=-1.5V$	−0.3		0	V	7
	V_{OB}		−1.8	−1.5	−1.2	V	
	V_C		−3.0		−2.7	V	
Current consumption	I_{DA}	In full-range operation		50	100	μA	8
	I_{DS}	When system clock is stationary		10	20	μA	
Oscillator start time	T_{OSC}			2	5	s	9

Note 2: Applicable pins K_1, K_2, K_3, K_4, α, β, ACL
Note 3: Applicable pins K_1, K_2, K_3, K_4
Note 4: Applicable pins α, β
Note 5: Applicable pins $\overline{O_{S1}}$, $\overline{O_{S2}}$, $\overline{O_{S3}}$, O_{S4}, O_{U}
Note 6: Applicable pins $\overline{R_1}$, $\overline{R_2}$, $\overline{R_3}$, $\overline{R_4}$
Note 7: Applicable pins H_1, H_2
Note 8: Mean current consumption at 32.768 kHz
Note 9: Oscillating circuit constant

● H_1, H_2 waveform



● Oscillator circuit

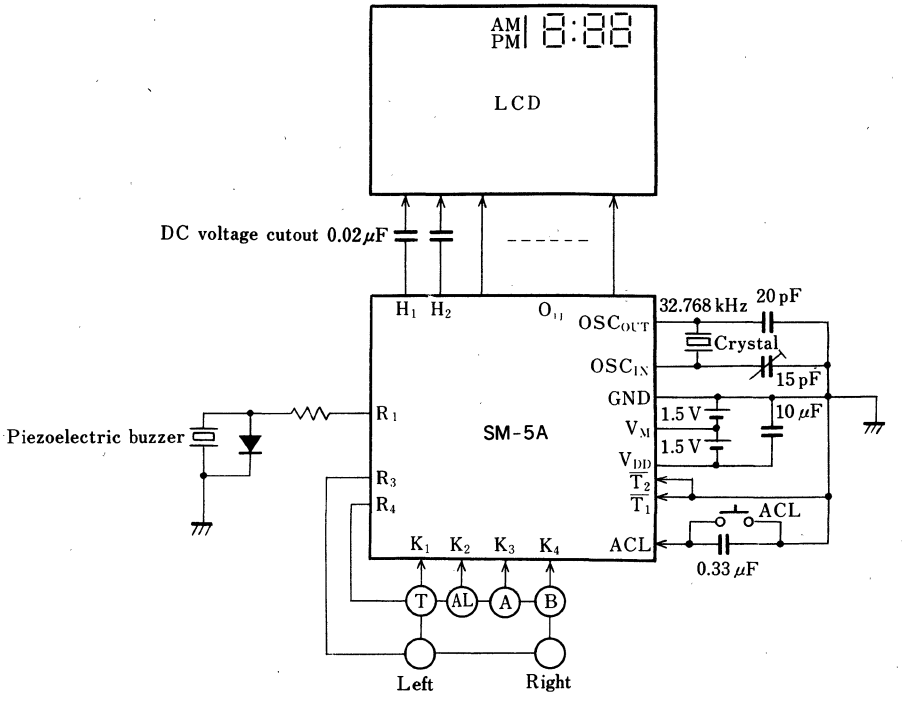


Oscillator circuit constant
$C_D=C_G=15\sim20\mu F$

Applications

1. Hand-held electronic calculator with clock
2. High-quality clock
3. Cash register
4. Hand-held electronic culculator with printer
5. POS terminal
6. Electronic scale
7. Game machine
8. Vending machine
9. Controller for electronic home appliances and audio equipment

System Configuration (for LCD game machine)



SM-5L CMOS 4-Bit 1-Chip Microcomputer

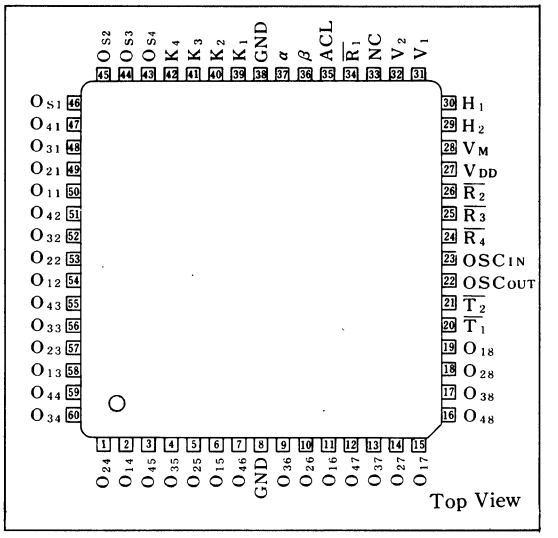
■ Description

The SM-5L is a 4-bit single chip CMOS microcomputer with 1,827 bytes of ROM, 65 words of RAM, a 15-stage divider and 72-segment liquid crystal driver circuit. It is well suited for applications of low power hand-held equipment with many liquid crystal display segments.

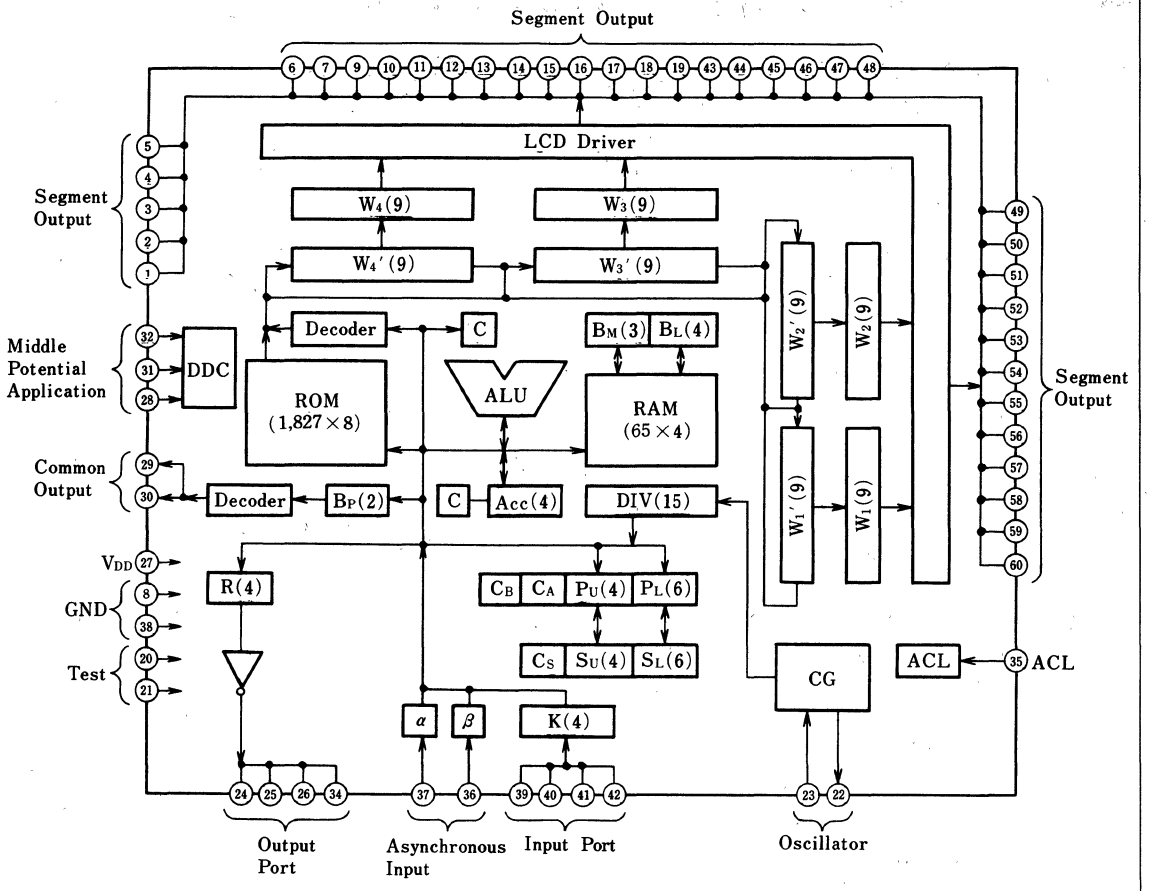
■ Features

1. CMOS process
2. ROM capacity 1,827×8 bits
3. RAM capacity 65×4 bits
4. Instructions 51
5. Subroutine nesting 1 level
6. Input ports 6 bits
7. Output ports 42 bits
8. On-chip 15-stage divider with reset (timer circuit)
9. Direct LCD driver circuit (3V, 1/2 duty, 1/2 bias and 72 segments MAX.)
10. On-chip crystal controlled oscillator (32.768kHz)
11. Standby mode (2.5 μA current consumption)
12. Single power supply −3V (TYP.)
13. Instruction cycle 61 μs
14. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

ALU	: Arithmetic logic unit	C_A, C_B, P_U, P_L	: Program counter
Acc	: Accumulator	C_S, S_U, S_L	: Stack register of program counter
CG	: Clock generator	$W_1 \sim W_4$, $W_1' \sim W_4'$	: Static shift resister
ACL	: Auto clear	B_M, B_L	: RAM address register
DIV	: Frequency divider	DDC	: LCD supply voltage generator
C	: Carry F/F		

■ Pin Description

Pin	I/O	Type of circuit	Function
$K_1 \sim K_4$	I	Pull down	Acc←$K_1 \sim K_4$
α, β	I	Pull up	Independent test possible
$O_{11} \sim O_{48}$ $O_{S1} \sim O_{S4}$	O		Output of contents of W and W′ registers ; used for output of LCD segment
H_1, H_2	O		3-state level output possible ; used for LCD common output
$\overline{R_1} \sim \overline{R_4}$	O		$\overline{R_1} \sim \overline{R_4}$←Acc, $\overline{R_1}$…Control output or alarm sound output
$\overline{T_P}$	I		For test (usually open)
$\overline{T_1}$, $\overline{T_2}$	I		For test (usually connected to GND)
ACL	I		Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_M			Power supply for LCD driver
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Pin voltage	V_{DD}	−3.5～+0.3	V	1
	V_{IN}	V_{DD}−0.3～+0.3	V	
Operating temperature	T_{opr}	−5～+50	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND (GND=0V)

■ Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	−3.3～−2.7	V
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz

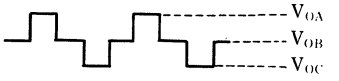
■ Electrical Characteristics

(V_{DD}=−3.0V±10%, GND=0V, Ta=25℃)

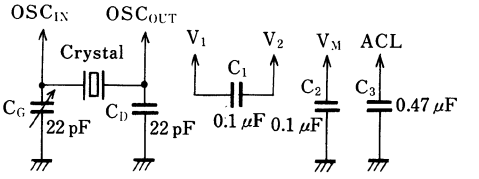
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.6			V	2
	V_{IL}				V_{DD}+0.6	V	
Input current	I_{IH1}				15	μA	3
	I_{IL2}				1	μA	4
	I_{IH3}				3	μA	5
Output voltage	V_{OH1}	I_{OUT}=30 μA to V_{DD}	−0.5			V	6
	V_{OL1}	I_{OUT}=10 μA to GND			V_{DD}+0.5	V	
	V_{OH2}	I_{OUT}=100 μA to V_{DD}	−0.5			V	7
	V_{OL2}	I_{OUT}=100 μA to GND			V_{DD}+0.5	V	
	V_{OA}	No load V_M=−1.5V	−0.3			V	8
	V_{OB}		−1.8		−1.2	V	
	V_{OC}				−2.7	V	
	V_M	C_1=C_2=0.1 μF	−1.8	−1.5	−1.2	V	9
Current consumption	I_{DO}	In Full-range operation		50	100	μA	10
	I_D	When system clock is stationary		2.5	5	μA	
Oscillation start time	T_{OSC}			2	5	s	11

Note 2: Applicable pins K_1~K_4, α, β, ACL
Note 3: Applicable pins K_1~K_4
Note 4: Applicable pins α, β
Note 5: Applicable pin ACL
Note 6: Applicable pins $\overline{O_{S1}}$~$\overline{O_{S4}}$, O_{ij} (i=1~4, j=1~8)
Note 7: Applicable pins R_1~R_4
Note 8: Applicable pins H_1, H_2
Note 9: Applicable pin V_M
Note 10: Mean current consumption at 32.768kHz
Note 11: Oscillating circuit constant C_C, C_D=15~22pF

• Waveform of H_1, H_2



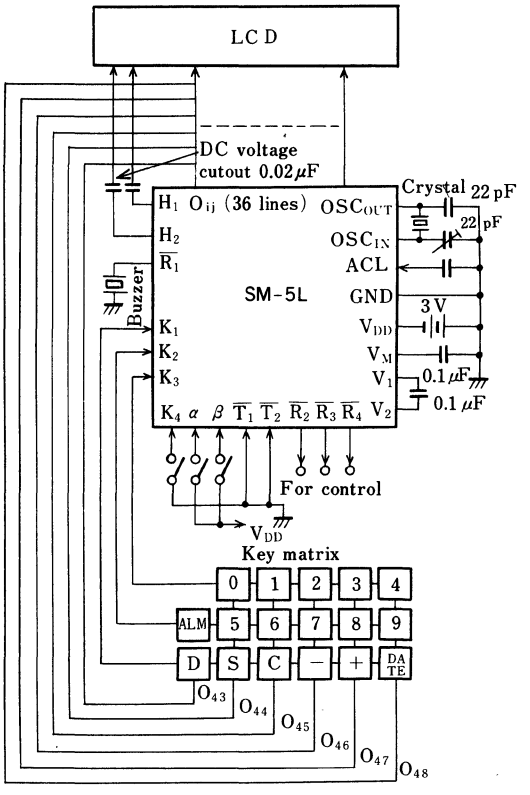
• Oscillation circuit, Intermediate potential generator circuit



■ Applications

1. Digital watch
2. Game machine
3. Controller for electronic home appliances and audio equipment
4. Hand-held electronic calculator with clock

■ System Configuration



SM-500 CMOS 4-Bit 1-Chip Microcomputer

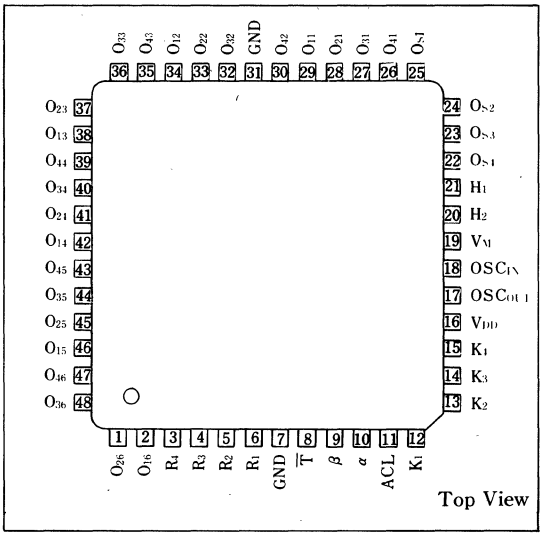
■ Description

The SM-500 is a 4-bit single chip CMOS microcomputer with 1,197 bytes of ROM, 40 words of RAM, a 15-stage divider and 40-segment liquid crystal driver circuits. It is well suited for applications of low cost, low-power hand-held equipment with liquid crystal display.

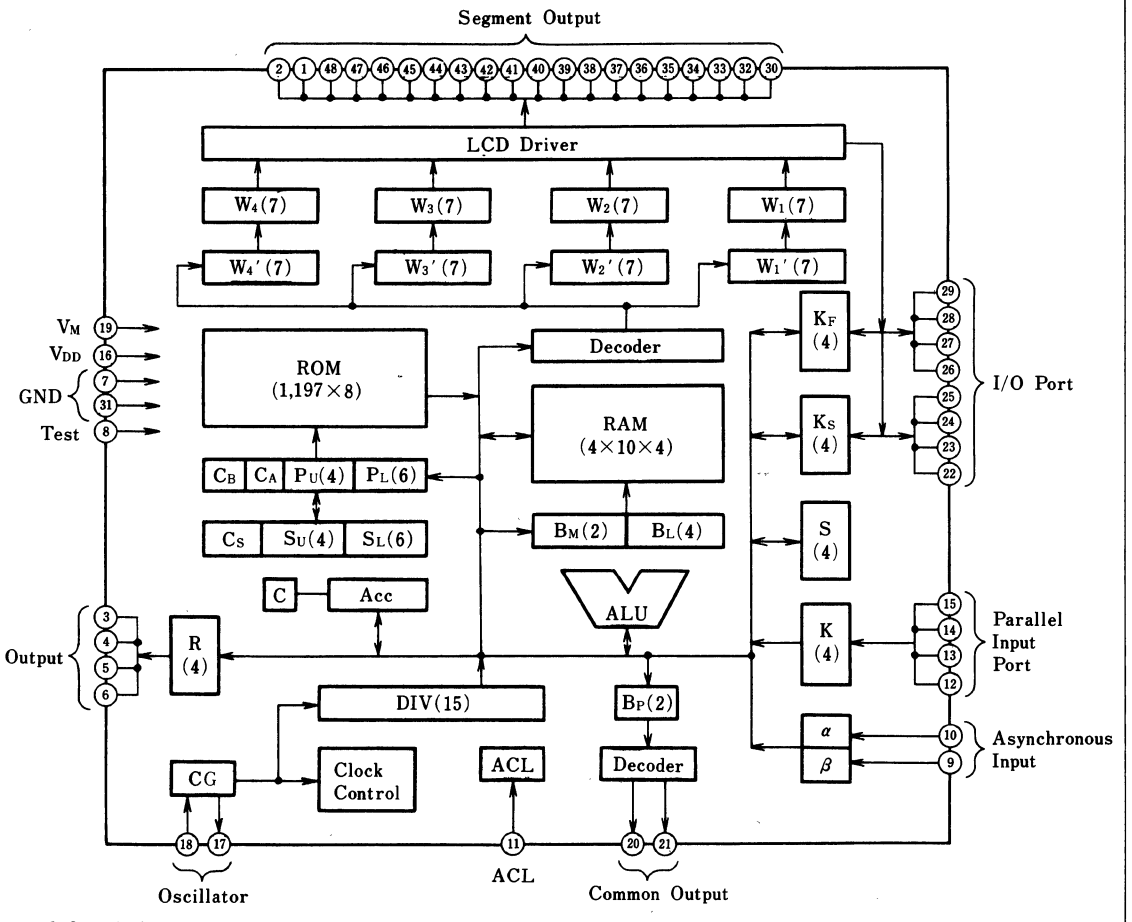
■ Features

1. CMOS process
2. ROM capacity 1,197×8 bits
3. RAM capacity 40×4 bits
4. Instructions 52
5. Subroutine nesting 1 level
6. Input ports 6 bits
7. Output ports 26 bits
8. Input/Output ports 8 bits
9. On-chip 15-stage divider with reset (timer circuit)
10. Direct LCD driver circuit (3V, 1/2 duty, 1/2 bias and 56 segments MAX.)
11. On-chip crystal controlled oscillator (32.768kHz)
12. Standby mode (3μA current consumption)
13. Single power supply −3V (TYP.)
14. Instruction cycle 61 μs
15. 48-pin quad-flat package

■ Pin Connections



Block Diagram



Symbol description

ALU	: Arithmetic logic unit	$W_1 \sim W_4, W_1' \sim W_4'$	: Static shift register
Acc	: Accumulator	B_M, B_L	: RAM address register
ACL	: Auto clear	B_P	: Backplate signal generator circuit
C	: Carry F/F	K_F	: 4-bit F/F
C_A, C_B, P_U, P_L	: Program counter	K_S	: 4-bit F/F
C_S, S_U, S_L	: Stack register of program counter	S	: 4-bit F/F (status register)
CG	: Clock generator	K	: Key input F/F
DIV	: Frequency divider		

■ Pin Description

Pin	I/O	Type of circuit	Function
$K_1 \sim K_4$	I	Pull down	Acc←$K_1 \sim K_4$
α, β	I	Pull up	Independent test possible
$O_{11} \sim O_{41}$	I/O		Output of contents of W and W′ registers or input/output to/from K_F register
$O_{S1} \sim O_{S4}$	I/O		Output of contents of W and W′ registers or input/output to/from K_S register
$O_{12} \sim O_{46}$	O		Output of contents of W and W′ registers ; Used for LCD segment output
H_1, H_2	O		3-state level output possible ; used for LCD common output
$R_1 \sim R_4$	O		$R_1 \sim R_4$←Acc
$\overline{T}$	I	Pull up	For test (usually connected to GND)
ACL	I	Pull down	Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_M			Power supply for LCD driver
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Pin voltage	V_{DD}	−4.0 ~ +0.3	V	1
	V_M	V_{DD} ~ +0.3	V	
	V_{IN}	V_{DD} − 0.3 ~ +0.3	V	
	V_{OUT}	V_{DD} − 0.3 ~ +0.3	V	
Operating temperature	T_{opr}	−10 ~ +70	℃	
Storage temperature	T_{stg}	−55 ~ +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.

■ Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	−3.3 ~ −2.7	V
	V_M	$V_{DD}/2$ (TYP.)	V
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz

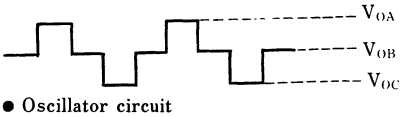
■ Electrical Characteristics

(V_{DD}=−3.0V±10%, GND=0V, Ta=25℃)

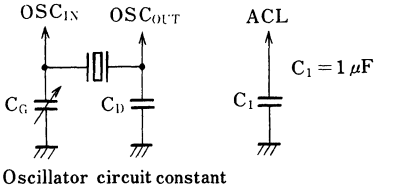
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.6			V	2
	V_{IL}				V_{DD}+0.6	V	
Input current	I_{H1}	V_{IN}=0V			15	μA	3
	I_{H2}	V_{IN}=0V			3	μA	4
	I_{L3}	V_{IN}=V_{DD}			1	μA	5
Output voltage	V_{OA}	No load V_M=V_{DD}/2	−0.3			V	6
	V_{OB}		V_M−0.3		V_M+0.3	V	
	V_{OC}				V_{DD}+0.3	V	
Output Current	I_{OH1}	V_{OUT}=−0.5V	30			μA	7
	I_{OL1}	V_{OUT}=V_{DD}+0.5V	10			μA	
	I_{OH2}	V_{OUT}=−0.5V	100			μA	8
	I_{OL2}	V_{OUT}=V_{DD}+0.5V	10			μA	
	I_{O3}	V_{DS}=0.3V	100			μA	9
	I_{O4}	V_{DS}=0.5V	100			μA	10
Current consumption	I_{DA}	In full-range operation		20		μA	11
	I_{DS}	When system clock is stationary		3		μA	

Note 2: Applicable pins K_1~K_4, α, β, ACL, O_{11}~O_{41}, O_{S1}~O_{S4}
Note 3: Applicable pins K_1~K_4, O_{11}~O_{41}, O_{S1}~O_{S4}
Note 4: Applicable pin ACL
Note 5: Applicable pins α, β
Note 6: Applicable pins H_1, H_2
Note 7: Applicable pins O_{ij} (i=1~4, j=2~6)
Note 8: Applicable pin O_{11}~O_{41}, O_{S1}~O_{S4}
Note 9: Applicable pin R_1
Note 10: Applicable pins R_2, R_3, R_4
Note 11: Current consumption under no load conditions at fosc=32.768kHz

● H_1,H_2 waveform



● Oscillator circuit



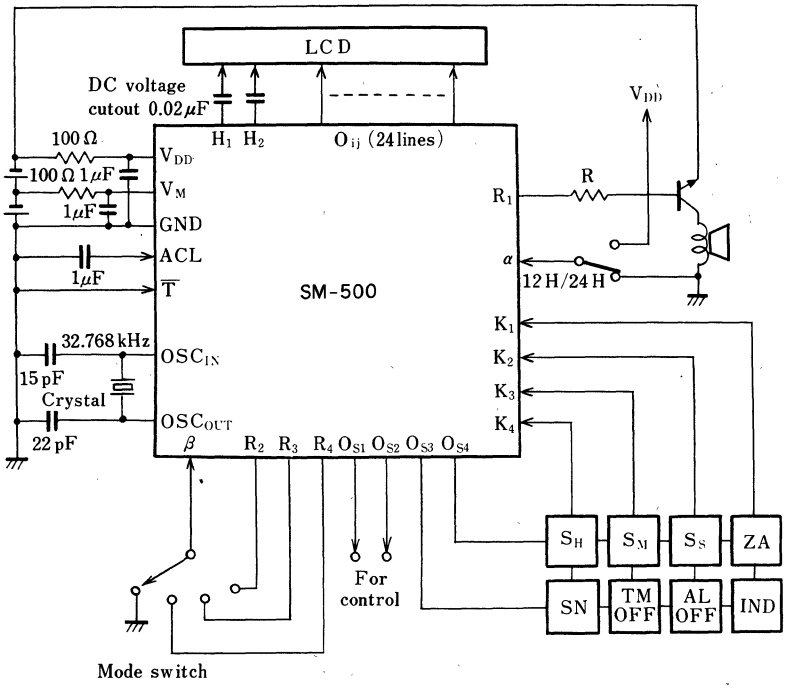
Oscillator circuit constant

C_D=C_G=22pF

■ Applications

1. Digital watch
2. Game machine
3. POS terminal
4. Electronic scale
5. Controller for electronic home appliances and audio equipment

■ System Configuration (for digital watch)



SM-510 CMOS 4-Bit 1-Chip Microcomputer

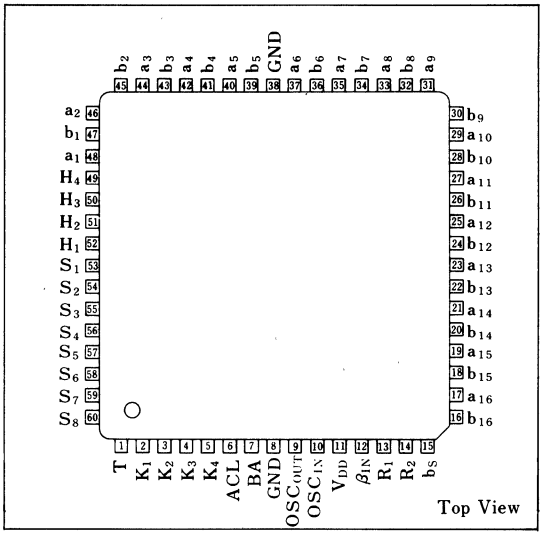
■ Description

The SM-510 is a 4-bit single chip CMOS microcomputer with 2,772 bytes of ROM, 128 words of RAM, a 15-stage divider and 132-segment liquid crystal driver circuits. It is well suited for applications of low cost, low power hand-held equipment with liquid crystal display.

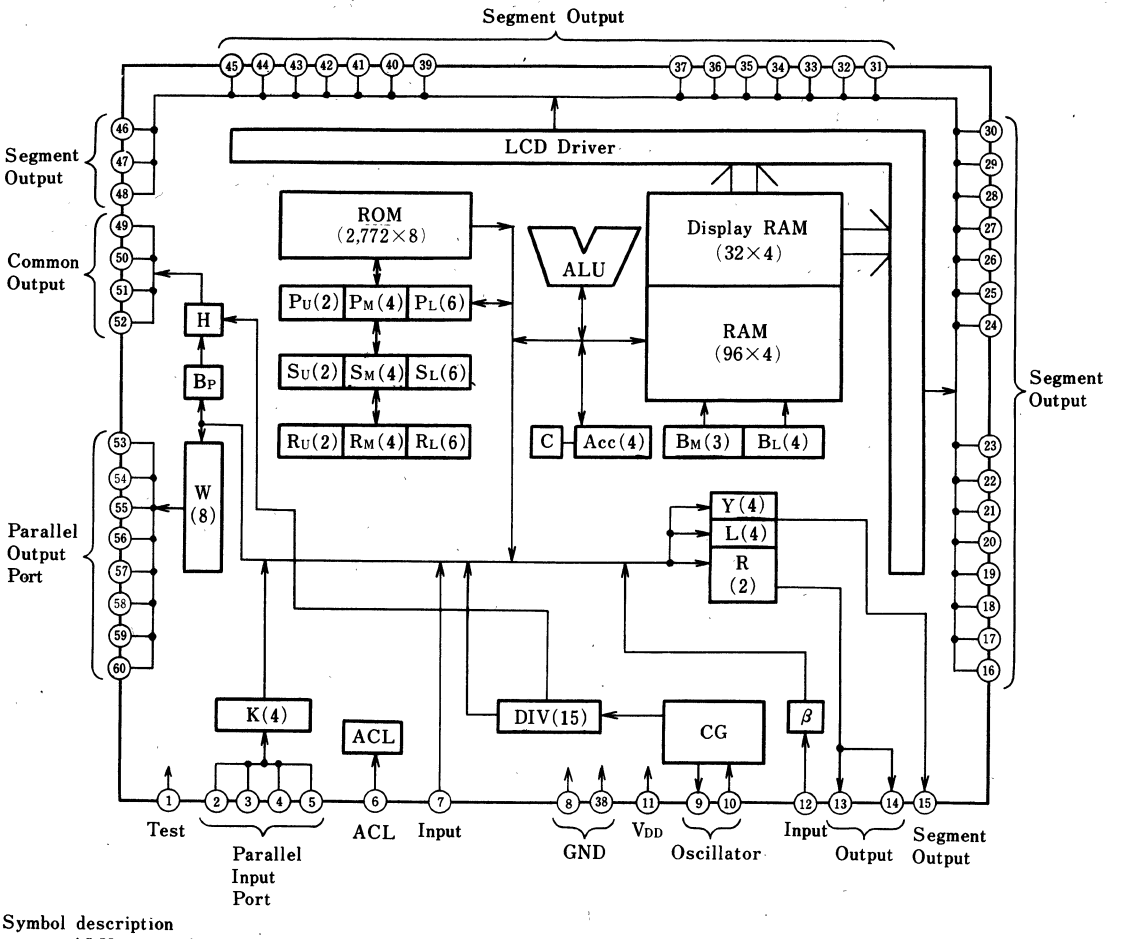
■ Features

1. CMOS process
2. ROM capacity 2,772×8 bits
3. RAM capacity 96×4+32×4 bits
4. Instructions 49
5. Subroutine nesting 2 levels
6. Input ports 6 bits
7. Output ports 47 bits
8. On-chip 15-stage divider with reset (timer circuit)
9. Direct LCD driver circuit (3V, 1/4 duty, 1/3 bias and 132 segments MAX.)
10. On-chip crystal controlled oscillator (32.768kHz)
11. Standby mode (10 μA current consumption)
12. Single power supply −3V (TYP.)
13. Instruction cycle 61 μs
14. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

ALU	: Arithmetic logic unit	W	: 8-bit shift register
Acc	: Accumulator	B_M, B_L	: RAM address register
C	: Carry F/F	B_P	: Backplate signal generator circuit
P_U, P_M, P_L	: Program counter	H, L, Y	: 4-bit F/F
S_U, S_M, S_L	: Stack register of program counter	R	: 2-bit F/F
R_U, R_M, R_L	: Stack register of program counter	K	: Key input F/F
DIV	: Frequency divider	CG	: Clock Generator

■ Pin Description

Pin	I/O	Type of circuit	Function
$K_1 \sim K_4$	I	Pull down	Acc←$K_1 \sim K_4$
BA, β_{IN}	I	Pull up	Independent test possible
$a_1 \sim a_{16}$, $b_1 \sim b_{16}$ bs	O		Output of contents of display RAM as LCD segment signal
$H_1 \sim H_4$	O		4-state level output possible ; used for LCD common output
$S_1 \sim S_8$	O		Output of contents of W register
R_1, R_2	O		For piezo-electric buzzer direct drive
T	I		For Test (usually connected to V_{DD})
ACL	I	Pull down	Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Pin voltage	V_{DD}	$-3.5 \sim +0.3$	V	1
	V_{IN}	$V_{DD} \sim +0.3$	V	
Operating temperature	T_{opr}	$0 \sim +50$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.

■ Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	$-3.2 \sim -2.6$	V
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz

■ Electrical Characteristics

($V_{DD}=-3V \pm 10\%$, Ta=25℃)

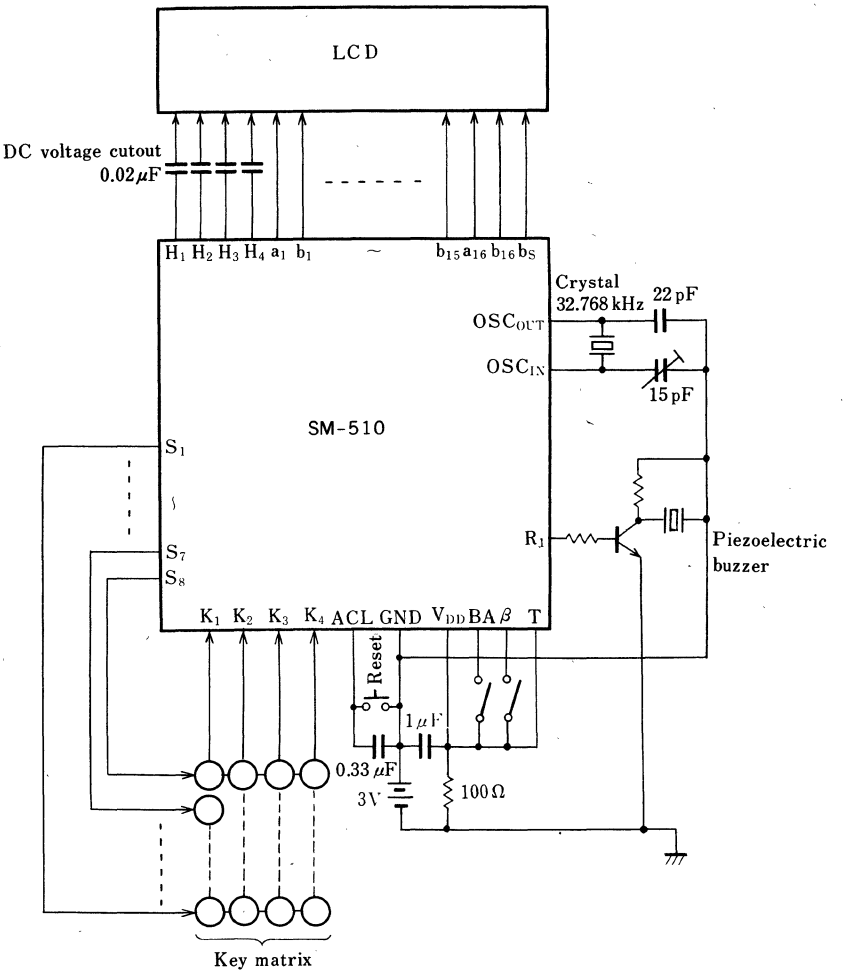
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		−0.6			V	2
	V_{IL1}				$V_{DD}+0.6$	V	
	V_{IH2}		−0.3			V	3
	V_{DL2}				$V_{DD}+0.3$	V	
Input current	I_{IH}	$V_{IN}=0V$	3		15	μA	4
	I_{IL}	$V_{IN}=V_{DD}$	3		15	μA	5
Output voltage	V_{OH}	$I_{OUT}=50$ μA to V_{DD}	−0.5			V	6
	V_{OL}	$I_{OUT}=5$ μA to GND			$V_{DD}+0.5$	V	
	V_{OA}	$V_{DD}=-3.0V$ No load	−0.3	0	0	V	7
	V_{OB}		−1.3	−1.0	−0.7	V	
	V_{OC}		−2.3	−2.0	−1.7	V	
	V_{OD}		−3.0	−3.0	−2.7	V	
Output current	I_{SO}	$V_{OUT}=-0.2V$	100			μA	8
	I_{SIN}	$V_{OUT}=V_{DD}+0.2V$	100			μA	
Current consumption	I_{DA}	In full-range operation		60		μA	9
	I_{DS}	When system clock is stationary		10		μA	

Note 2: Applicable pins $K_1 \sim K_4$, β_{IN}
Note 3: Applicable pins ACL, BA
Note 4: Applicable pins $K_1 \sim K_4$
Note 5: Applicable pin β_{IN}
Note 6: Applicable pins $S_1 \sim S_8$
Note 7: Applicable pins $a_1 \sim a_{16}$, $b_1 \sim b_{16}$, b_8, $H_1 \sim H_4$
Note 8: Applicable pins R_1, R_2
Note 9: Current consumption when fosc is 32.768kHz (TYP.) and −3.0V of V_{DISP} is applied

■ Applications

1. Hand-held electronic calcuator with multi-digit display and clock
2. High-quality clock
3. Handy game machine
4. Equipment that need multiple LCD display segments

■ System Configuration (Hand-held electronic calcuator with clock)



SM-511 CMOS 4-Bit 1-Chip Microcomputer

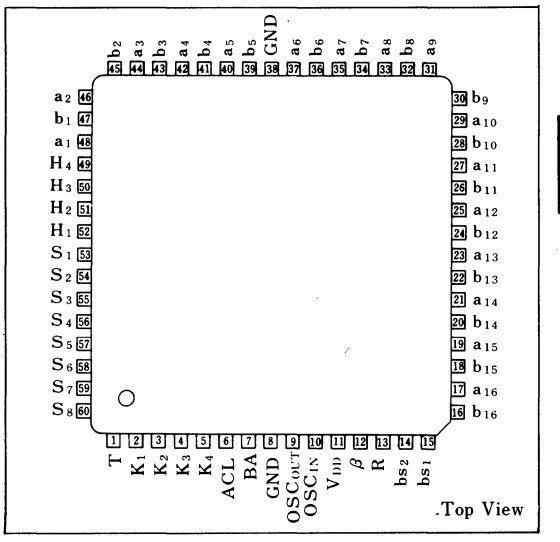
■ Description

The SM-511 is a 4-bit single chip CMOS microcomputer with 4,032 bytes of ROM, 128 words of RAM , a 15-stage divider, melody generator and 136-segment liquid crystal driver circuits. It is well suited for low cost, low power hand-held equipment with liquid crystal displays.

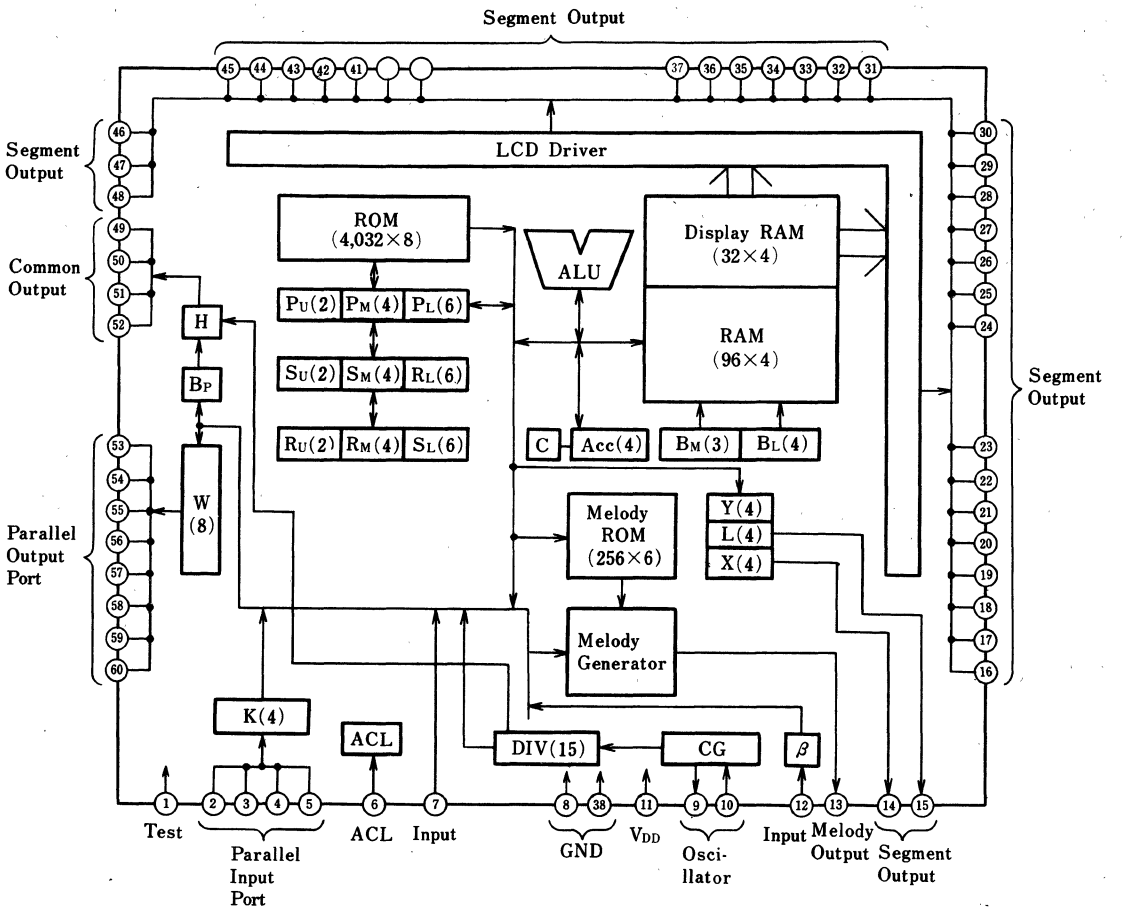
■ Features

1. CMOS process
2. ROM capacity 4,032×8 bits
3. RAM capacity 96×4+32×4 bits
4. Instructions 55
5. Subroutine nesting 2 levels
6. Input ports 6 bits
7. Output ports 47 bits
8. On-chip 15-stage divider with reset (timer circuit)
9. Melody generator circuit
10. Direct LCD driver circuit (3V, 1/4 duty, 1/3 bias and 136 segments MAX.)
11. On-chip crystal controlled oscillator (32.768kHz)
12. Standby mode (10 μA current consumption)
13. Single power supply −3V (TYP.)
14. Instruction cycle 61 μs
15. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

ALU	: Arithmetic logic unit	W	: 8-bit shift register
Acc	: Accumulator	B_M, B_L	: RAM address register
ACL	: Auto clear	B_P	: Backplate signal generator circuit
C	: Carry F/F	H, L, X, Y	: 4-bit F/F
P_U, P_M, P_L	: Program counter	K	: Key input F/F
S_U, S_M, S_L	: Stack register of program counter	CG	: Clock generator
R_U, R_M, R_L	: Stack register of program counter		
DIV	: Frequency divider		

Pin Description

Pin	I/O	Type of circuit	Function
$K_1 \sim K_4$	I	Pull down	Acc←$K_1 \sim K_4$
BA, β	I	Pull up	Independent test possible
$a_1 \sim a_{16}$, $b_1 \sim b_{16}$	O		Output of contents of display RAM as LCD segment signal
bs_1	O		LCD segment or LCD flashing output
bs_2	O		Input of X register contents as LCD segment signal
$H_1 \sim H_4$	O		4-state level output possible ; used for LCD common output
$S_1 \sim S_8$	O		Output of contents of W register
R	O		Melody output
T	I		For Test (usually connected to V_{DD})
ACL	I	Pull down	Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DD}, GND			Power supply for logic circuit

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Pin voltage	V_{DD}	$-3.5 \sim +0.3$	V	1
	V_{IN}	$V_{DD} \sim +0.3$	V	
Operating temperature	T_{opr}	$0 \sim 50$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND (GND=0V)

Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	$-3.2 \sim -2.6$	V
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz

■ Electrical Characteristics

(V_{DD}=−3V±10%, Ta=25℃)

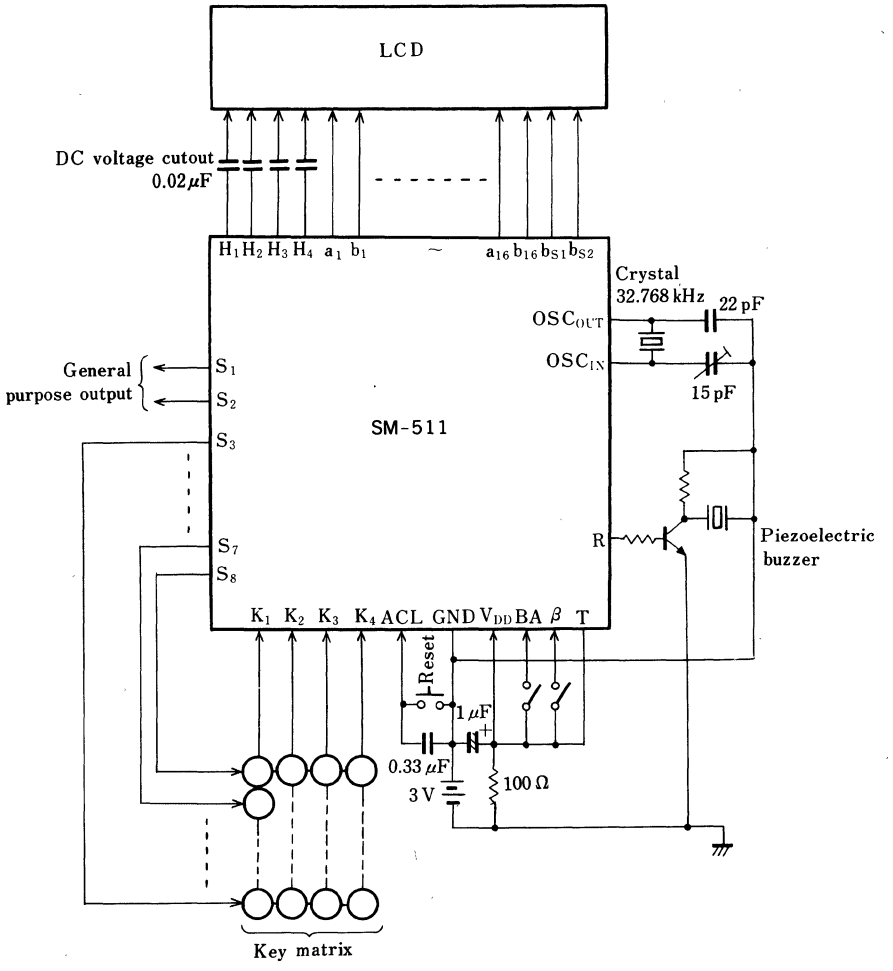
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		−0.6			V	2
	V_{IL1}				V_{DD}+0.6	V	
	V_{IH2}		−0.3			V	3
	V_{IL2}				V_{DD}+0.3	V	
Input current	I_{IH1}	V_{IN}=0V	3		15	μA	4
	I_{IH2}	V_{IN}=V_{DD}	3		15	μA	5
Output voltage	V_{OH}	I_{OUT}=50μA to V_{DD}	−0.5			V	6
	V_{OL}	I_{OUT}=5μA to GND			V_{DD}+0.5	V	
	V_{OA}	V_{DD}=−3.0V No load	−0.3	0		V	7
	V_{OB}		−1.3	−1.0	−0.7	V	
	V_{OC}		−2.3	−2.0	−1.7	V	
	V_{OD}		−3.0	−3.0	−2.7	V	
Output current	I_{SO}	V_{OUT}=−0.2V	100			μA	8
	I_{SIN}	V_{OUT}=V_{DD}+0.2V	100			μA	
Current consumption	I_{DA1}	In full-range operation		40	60	μA	9
	I_{DS1}	When system clock is stationary		10	20	μA	
Current consumption	I_{DA1}	In full-range operation		25	35	μA	10
	I_{DS2}	When system clock is stationary		10	20	μA	

Note 2: Applicable pins K_1~K_4, β
Note 3: Applicable pins ACL, BA
Note 4: Applicable pins K_1~K_4
Note 5: Applicable pin β
Note 6: Applicable pins S_1~S_8
Note 7: Applicable pins a_1~a_{16}, b_1~b_{16}, bs_1, bs_2, H_1~H_4
Note 8: Applicable pin R
Note 9: When melody circuit is inoperative with V_{DD} at −3.0V and system clock at 16.384kHz.
Note 10: When melody circuit is inoperative with V_{DD} at −3.0V and system clock at 8.192kHz.

■ Applications

1. Hand-held electronic calculator with multidigit display and clock
2. Hand-held electronic calculator with function calculation capability
3. Hand-held game machine
4. Equipment that need multiple LCD display segments

■ System Configuration (for melody alarm, watch, and hand-held electronic calculator with game function)



SM-520 CMOS 4-Bit 1-Chip Microcomputer

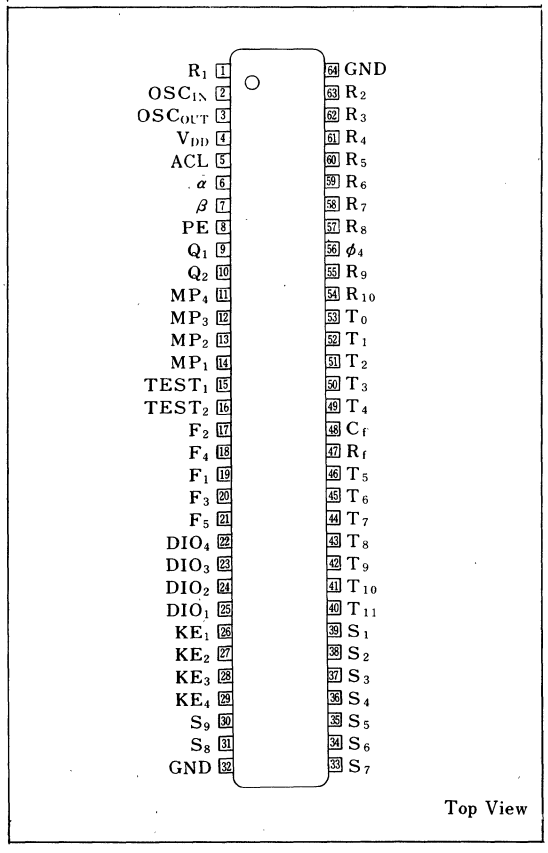
■ Description

The SM-520 is a 4-bit single chip CMOS microcomputer with 3,072×10 bits of ROM, 168 words of RAM, a 15-stage divider, and automatic display circuit. It is well suited for applications with many control ports.

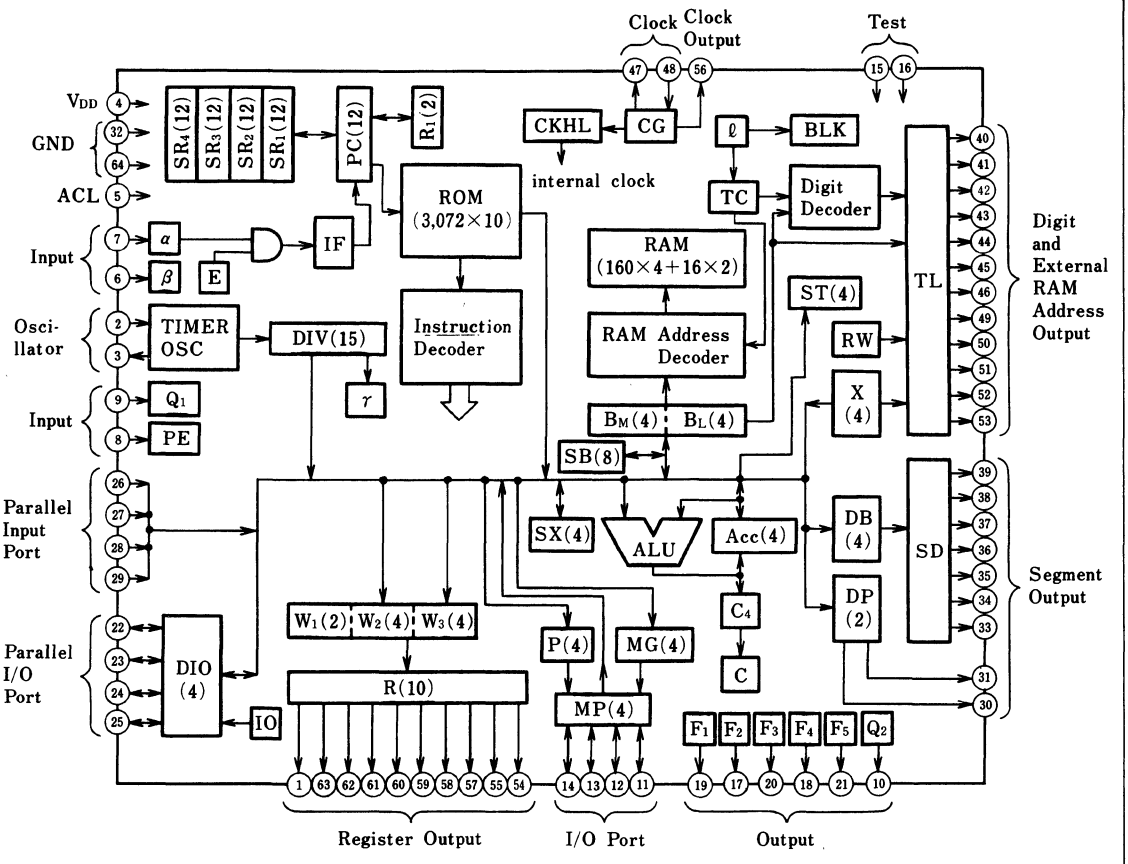
■ Features

1. CMOS process
2. ROM capacity 3,072×10 bits
3. RAM capacity 160×4+16×2 bits (including 16×2 bits for display)
4. Instructions 93
5. Subroutine nesting 4 levels
6. Input ports 8 bits
7. Output ports 37 bits
8. Input/Output ports 8 bits
9. On-chip 15-stage divider with reset (timer circuit)
10. External interrupt function
11. External RAM expandable (1,704×4 bits)
12. Clock generator circuit
13. On-chip crystal controlled oscillator
14. Standby mode (50 μA current consumption)
15. Single power supply −5V (TYP.)
16. Instruction cycle 11 μs
17. 64-pin dual-in-line package

■ Pin Connections



■ Block Diagram



Symbol description

Acc	: Accumulator	DB, DP	: Registers for automatic display use
ALU	: Arithmetic logic unit	W_{ij}	: Shift register
PC	: Program counter	IO	: DIO control F/F
SR	: Stack register	C	: Carry F/F
B_M, B_L	: RAM address counter	SD	: Segment decoder
SB	: RAM address counter stack	IF	: Interrupt flag F/F
X, SX	: Temporary registers	E	: Interrupt mask F/F
ST	: T output control register	DIV	: Divider
TC, ℓ	: Counters for automatic display use	CG	: Clock generator

■ Pin Description

Pin	I/O	Type of circuit	Function
$KE_1 \sim KE_4$	I	Pull down	Acc←$KE_1 \sim KE_4$
α, β, PE, Q_1	I	Pull down	Test possible by separate input
$DIO_1 \sim DIO_4$	I/O	Pull down	Acc↔$DIO_1 \sim DIO_4$
$MP_1 \sim MP_4$	I/O		MG register output, on-the-way stage signal output of divider or Acc←$MP_1 \sim MP_4$
$T_0 \sim T_{11}$	O		Digit signal or external RAM address signal output
$R_1 \sim R_{10}$	O		W register content output
$S_1 \sim S_9$	O		Segment signal output
$F_1 \sim F_5$	O		Can be set or reset independently
Q_2	O		Can be set or reset
$TEST_1$ $TEST_2$	I	Pull down	For test (usually connected to V_{DD})
ACL	I	Pull down	Auto clear
Rf, Cf			For system clock oscillator
OSC_{IN}, OSC_{OUT}			For clock oscillator
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{DD}	−6.0 ~ +0.3	V	1
	V_{IN}	V_{DD}−0.3 ~ +0.3	V	1,2
	V_{OUT}	V_{DD}−0.3 ~ +0.3	V	1,3
Operating temperature	T_{opr}	−10 ~ +60	℃	
Storage temperature	T_{stg}	−55 ~ +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND (GND=0V)
Note 2: Applicable to inputs
Note 3: Applicable to outputs

■ Operating Conditions

Parameter	Symbol	Conditions	Specified value	Unit	Note
Operating voltage	V_{DD}		−5.5 ~ −4.5	V	
		In "Low" clock	−5.5 ~ −3.5	V	4

Note 4: When the clock frequency fc is lowered to 1/8 of that in normal operation

■ Electrical Characteristics

($V_{DD}=-5.0\pm10\%$, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		−1.5			V	5
	V_{IL1}				$V_{DD}+1.0$	V	
	V_{IH2}		−0.3			V	6
	V_{IL2}				$V_{DD}+0.3$	V	
Output voltage	V_{OH1}	$I_{OUT}=-250\,\mu A$	−0.6			V	7
	V_{OL1}	$I_{OUT}=30\,\mu A$			$V_{DD}+0.6$	V	
	V_{OH2}	$I_{OUT}=-250\,\mu A$	−1.0			V	8
	V_{OL2}	$I_{OUT}=50\,\mu A$			$V_{DD}+0.6$	V	
	V_{OH3}	$I_{OUT}=-500\,\mu A$	−1.0			V	9
	V_{OL3}	$I_{OUT}=50\,\mu A$			$V_{DD}+0.6$	V	
	V_{OH4}	$I_{OUT}=-1.0$mA	−2.5			V	10
	V_{OL4}	$I_{OUT}=50\,\mu A$			$V_{DD}+0.6$	V	
	V_{OH5}	$I_{OUT}=-100\,\mu A$	−0.6			V	11
	V_{OL5}	$I_{OUT}=50\,\mu A$			$V_{DD}+0.6$	V	
	V_{OH6}	$I_{OUT}=-150\,\mu A$	−0.6			V	12
	V_{OL6}	$I_{OUT}=150\,\mu A$			$V_{DD}+0.6$	V	
Current consumption	I_{DD1}	In normal operating		1.5		mA	13
	I_{DD2}	When clock is stationary		50	150	μA	14
Clock frequency	f_C			90		kHz	15
	f_{CL}	In "Low" clock		11.2		kHz	
Oscillator frequency	f_{CRY}			32.768		kHz	16

Note 5: Applicable pins ACL, α, β, PE, Q_1, KE_1~KE_4, DIO_1~DIO_4, MP_1~MP_4
Note 6: Applicable pin C_f
Note 7: Applicable pins T_0~T_{11}
Note 8: Applicable pins S_1~S_9, F_1, F_3~F_3, Q_2
Note 9: Applicable pins R_1~R_{10}
Note 10: Applicable pins MP_1~MR_4, F_2
Note 11: Applicable pins DIO_1~DIO_4
Note 12: Applicable pin Rf
Note 13: No-load state (internal CG out attached capacity C=15pF)
Note 14: $V_{DD}=-3.5$V, No-load state (〃)
Note 15: For C and R elements out-attached to internal CG, C=15pF±2%, R=82kΩ±2%, they are connected as shown in Fig.1
Note 16: For connection of out-attached element of crystal oscillator, see Fig. 2.

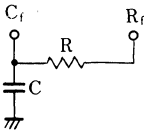


Fig. 1

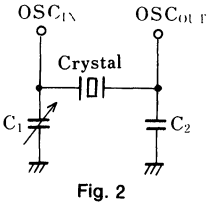
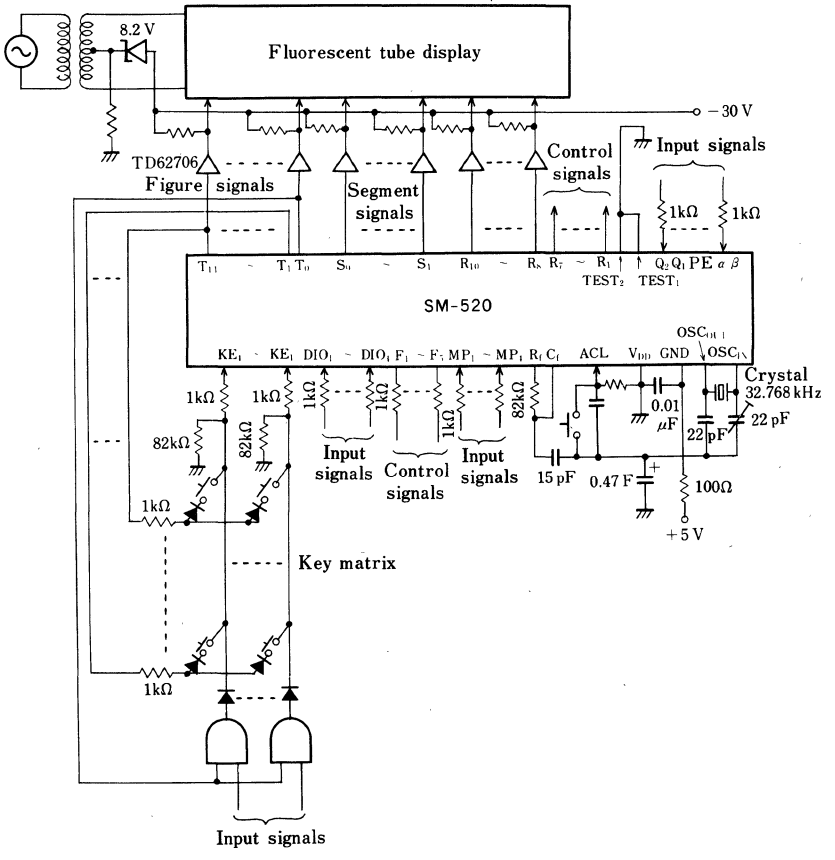


Fig. 2

■ Applications

1. Cash register
2. Hand-held electronic calculator with printer
3. Electrical copy machine
4. Microwave oven
5. Vending machine
6. Game machine
7. POS terminal
8. Electronic scale
9. Controller for electronic and electric home appliances

■ System Configuration (for VTR timer)



SM-525 CMOS 4-Bit 1-Chip Microcomputer

■ Description

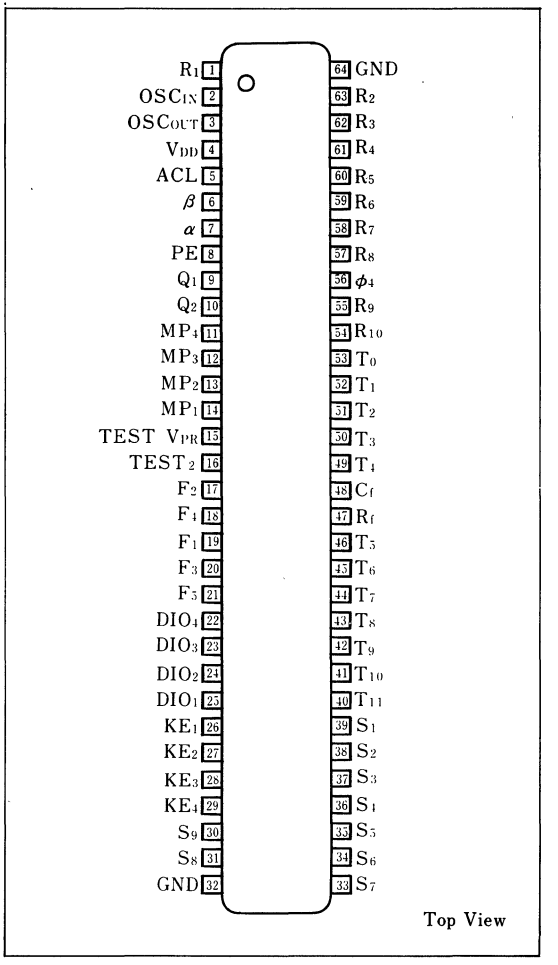
The SM-525 is a 4-bit single chip CMOS microcomputer with 3,072×10 bits of ROM, 168 words of RAM, a 15-stage divider and automatic display circuit.

It is well suited for applications with fluorescent display tube (VFD), due to built-in high voltage outputs.

■ Features

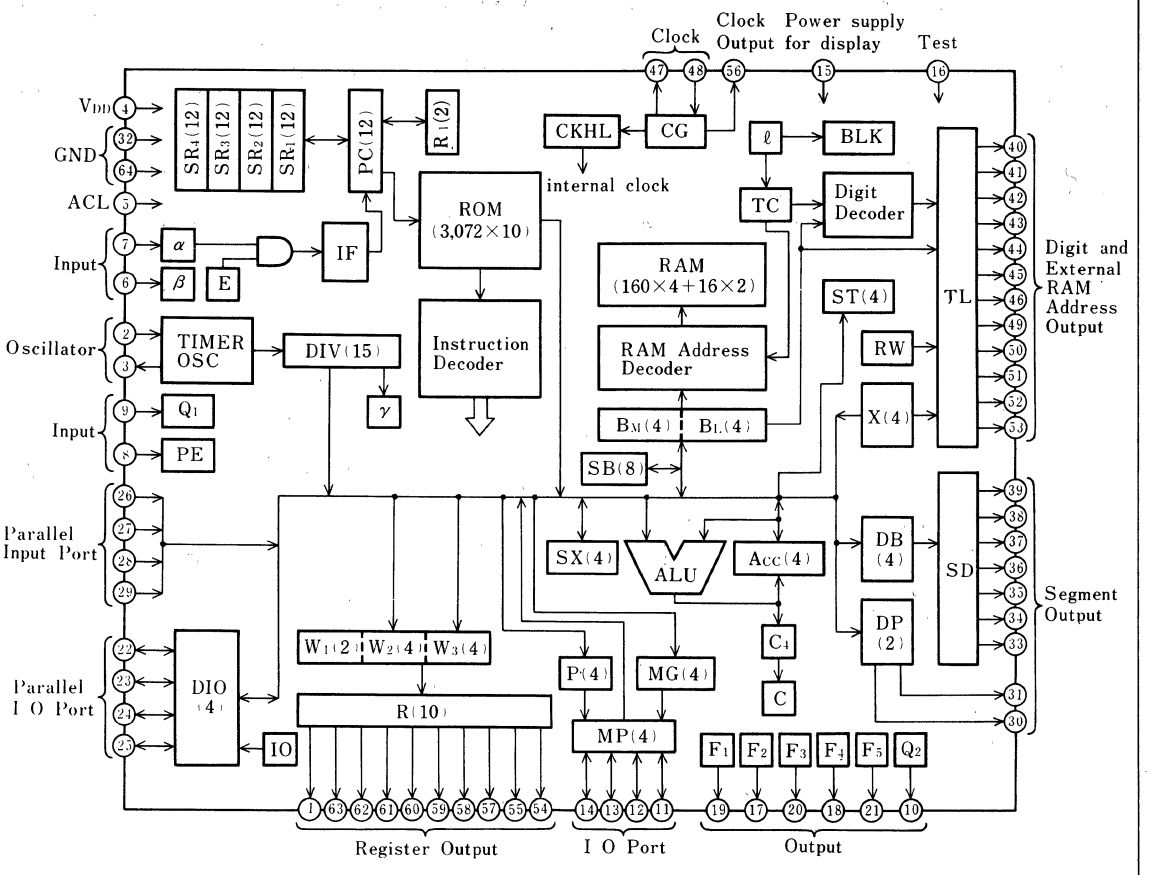
1. CMOS process
2. ROM capacity 3,072×10 bits
3. RAM capacity 168×4 bits (including 16×2 bits for display)
4. Instructions 93
5. Subroutine nesting 4 levels
6. Input ports 8 bits
7. Output ports 37 bits
8. Input/Output ports 8 bits
9. High voltage outputs (−30V) 21bits
10. On-chip 15-stage divider with reset (timer circuit)
11. External interrupt function
12. External RAM expandable (1,704×4 bits)
13. Clock generator circuit
14. On-chip crystal controlled oscillator
15. Standby mode (50 μA current consumption)
16. Single power supply −5V (TYP.)
17. Instruction cycle 11 μs
18. 64-pin dual-in-line package

■ Pin Connections



Top View

■ Block Diagram



Symbol description

ACC	: Accumulator	DB,DP	: Registers for automatic display use
ALU	: Arithmetic logic unit	W_n	: Shift register
PC	: Program counter	DIO	: DIO control F F
SR	: Stack register	C	: Carry F F
B_M,B_L	: RAM address counter	SD	: Segment decoder
SB	: RAM address counter stack	IF	: Interrupt flag F/F
X,SX	: Temporary registers	E	: Interrupt mask F/F
ST	: T output control register	DIV	: Divider
TC, ℓ	: Counters for automatic display use	CG	: Clock generator

■ Pin Description

Pin name	I/O	Circuit type	Function
$KE_1 \sim KE_4$	I	Pull down	Acc→$KE_1 \sim KE_4$
α, β, PE, Q_1	I	Pull down	Can be tested on individual input
$DIO_1 \sim DIO_4$	I/O	Pull down	Acc ⟷ $DIO_1 \sim DIO_4$
$MP_1 \sim MP_4$	I/O		MG register output or divider middle stage signal output or Acc ← $MP_1 \sim MP_4$
$T_0 \sim T_{11}$	O		Digit signal or external RAM address signal output
$R_1 \sim R_{10}$	O		W register output
$S_1 \sim S_9$	O		Segment signal output
$F_1 \sim F_5$	O		Can be set or reset individually
Q_2	O		Can be set or reset
TEST, $TEST_2$	I	Pull down	For test (Connected to V_{DD} normally)
ACL	I	Pull down	Auto clear
Rf, Cf			For system clock oscillation
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

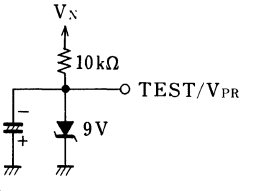
Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{DD}	−6 ~ +0.3	V	1,2
	V_{PR}	−12 ~ +0.3		1,3
	V_{IN}	V_{DD} −0.3 ~ +0.3		1,4
	V_{OUT1}	V_{DD} −0.3 ~ +0.3		1,5,6
	V_{OUT2}	−35 ~ +0.3		1,7
Output current	I_{OUT1}	−70	mA	7,8
	I_{OUT2}	−15		5,8
	I_{OUT3}	4		5,9
Operating temperature	T_{opr}	−10 ~ +60	℃	
Storage temperature	T_{stg}	−55 ~ +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Applied to pin V_{DD}.
Note 3: Applied to pin TEST/V_{PR}.
Note 4: Applied to pins ACL, α, β, PE, Q, $DIO_1 \sim DIO_4$, $KE_1 \sim KE_4$, $MP_1 \sim MP_4$, Cf.
Note 5: Applied to pins $DIO_1 \sim DIO_4$, $MP_1 \sim MP_4$, $F_1 \sim F_5$, $R_1 \sim R_{10}$, Q_2.
Note 6: Applied to pin Rf.
Note 7: Applied to pins $T_0 \sim T_{11}$, $S_1 \sim S_9$
Note 8: Total high level output current
Note 9: Total low level output current

■ Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}	During normal operation	−5.5		−4.5	V	
	V_{DDL}	During low clock	−5.5		−3		10
Auxiliary voltage	V_{PR}		−9.9		−8.1	V	11
Display voltage	V_N		−30		V_{DD}	V	

Note 10: Condition in which the clock frequency fc has been dropped to 1/8 of that during normal operation.
Note 11: The auxiliary voltage V_{PR} is applied from the TEST/V_{PR} pin.



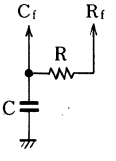
(Example of circuit with V_{PR} externally attached)

■ Electrical Characteristics

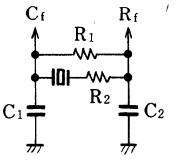
($V_{DD}=-5V\pm10\%$, $V_{PR}=-9V\pm10\%$, $V_N=-30V$, f=90kHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		−1.5			V	12
	V_{IL1}				$V_{DD}+0.6$		
	V_{IH2}		−2.3			V	13
	V_{IL2}				$V_{DD}+0.6$		
	V_{IH3}		−0.3			V	14
	V_{IL3}				$V_{DD}+0.3$		
Input current	I_{IH}	$V_I=0V$		5	35	μA	15
Output voltage	V_{OH1}	$I_O=-17mA$	−1.8			V	16
	V_{OL1}	Connect $R_L=50k\Omega$ to V_N			V_N+1		
	V_{OH2}	$I_O=-2mA$	−2			V	17
	V_{OL2}	Connect $R_L=50k\Omega$ to V_N			V_N+1		
	V_{OH3}	$I_O=-250\mu A$	−1			V	18
	V_{OL3}	$I_O=100\mu A$			$V_{DD}+0.6$		
	V_{OH4}	$I_O=-250\mu A$	−1			V	19
	V_{OL4}	$I_O=300\mu A$			$V_{DD}+0.6$		
	V_{OH5}	$I_O=-2mA$	−2.5			V	20
	V_{OL5}	$I_O=50\mu A$			$V_{DD}+0.6$		
	V_{OH6}	$I_O=-1.5mA$	−2.5			V	21
	V_{OL6}	$I_O=100\mu A$			$V_{DD}+0.6$		
	V_{OH7}	$I_O=-100\mu A$	−0.6			V	22
	V_{OL7}	$I_O=100\mu A$			$V_{DD}+0.6$		
	V_{OH8}	$I_O=-150\mu A$	−0.6			V	23
	V_{OL8}	$I_O=150\mu A$			$V_{DD}+0.6$		
Current consumption	I_{DD1}	During normal operation		600		μA	24
	I_{DD2}	During clock stop		50	150	μA	25
Clock frequency	f_C			90		kHz	26
	f_{CL}	During low clock		11.2			
Crystal oscillator frequency	f_{CRY}			32.768		kHz	27

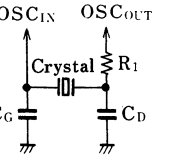
Note 12: Applied to pins ACL, α, β, PE, Q_1, $DIO_1\sim DIO_4$, $MP_1\sim MP_4$
Note 13: Applied to pins $KE_1\sim KE_4$
Note 14: Applied to pin Cf
Note 15: Applied to pins α, β, Q_1, $KE_1\sim KE_4$, $DIO_1\sim DIO_4$, $MP_1\sim MP_4$, F_2 (during floating condition)
Note 16: Applied to pins $T_0\sim T_{11}$
Note 17: Applied to pins $S_1\sim S_9$
Note 18: Applied to pins F_1, F_3, F_5
Note 19: Applied to pins $R_1\sim R_6$, Q_2, F_1
Note 20: Applied to pins $R_7\sim R_{10}$
Note 21: Applied to pins $MP_1\sim MP_4$, F_2
Note 22: Applied to pins $DIO_1\sim DIO_4$
Note 23: Applied to pin Rf
Note 24: No-load condition
Note 25: No-load condition, $V_{DD}=-3.5V$, internal CG with externally attached capacitance C= 15pF
Note 26: Internal circuit with externally attached CG
Note 27: Circuit with externally attached crystal oscillator



R = 82kΩ
C = 15pF



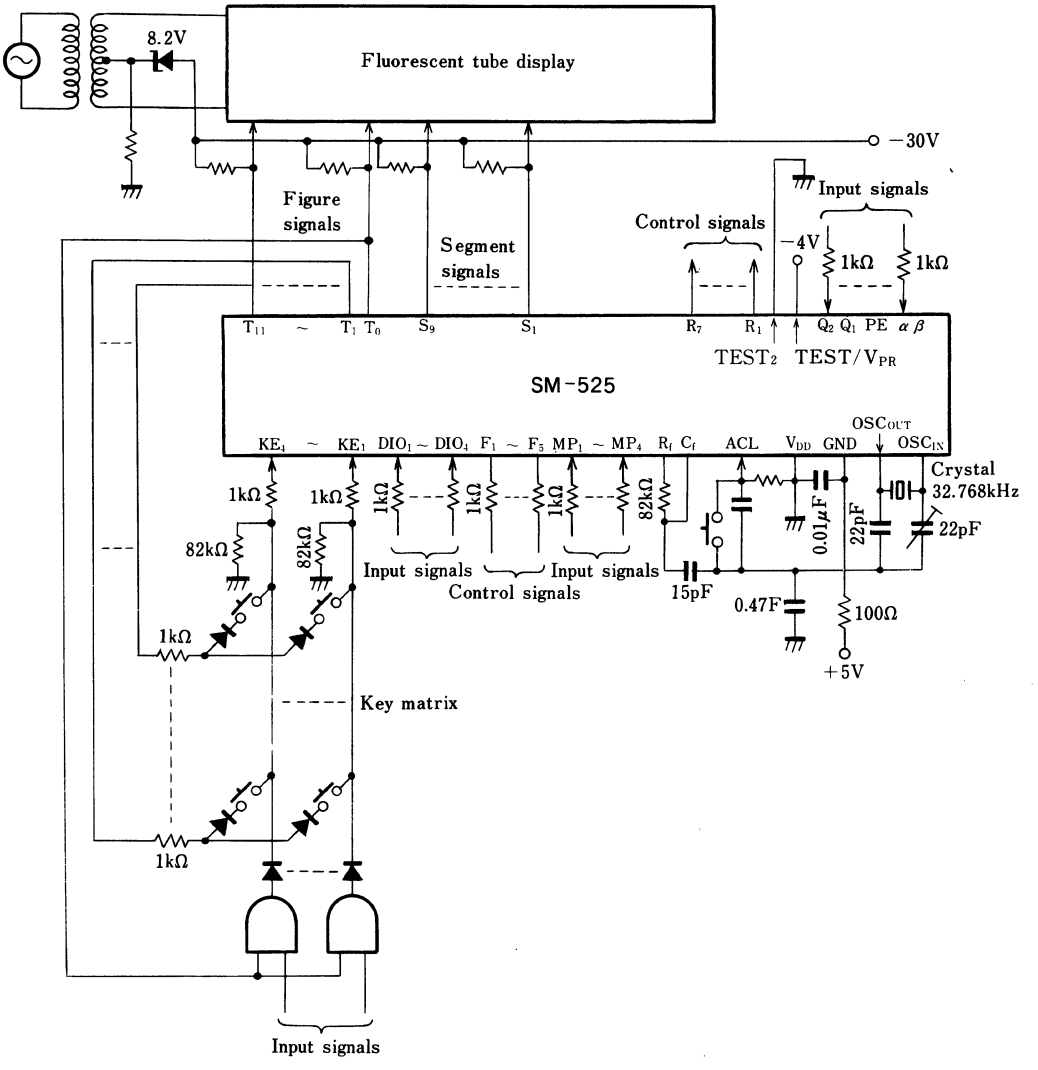
C1 = 330pF
C2 = 150pF
R1 = 1MΩ
R2 = 560Ω
Ceramic oscillator : KBR-
(made by Kyocera Corp.)



R1 = 200kΩ
CG = 10pF
CD = 33pF
Crystal : KF-38G
(made by Kyocera Corp.)

- When a ceramic oscillator is used, the operating voltage V_{DD} is limited to −5.5 to −4.5V.
- Oscillation starting voltage becomes larger than the CR oscillation.

System Configuration (for VTR timer)



SM-530 CMOS 4-Bit 1-Chip Microcomputer

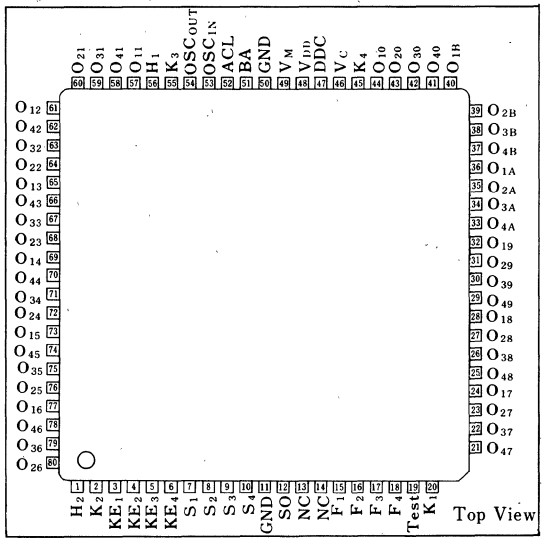
■ Description

The SM-530 is a 4-bit single chip CMOS microcomputer with 2,016 bytes of ROM, 88 words of RAM, melody generator circuit and 96-segment LCD driver circuit. It is well suited for low cost, low power systems with many LCD segments.

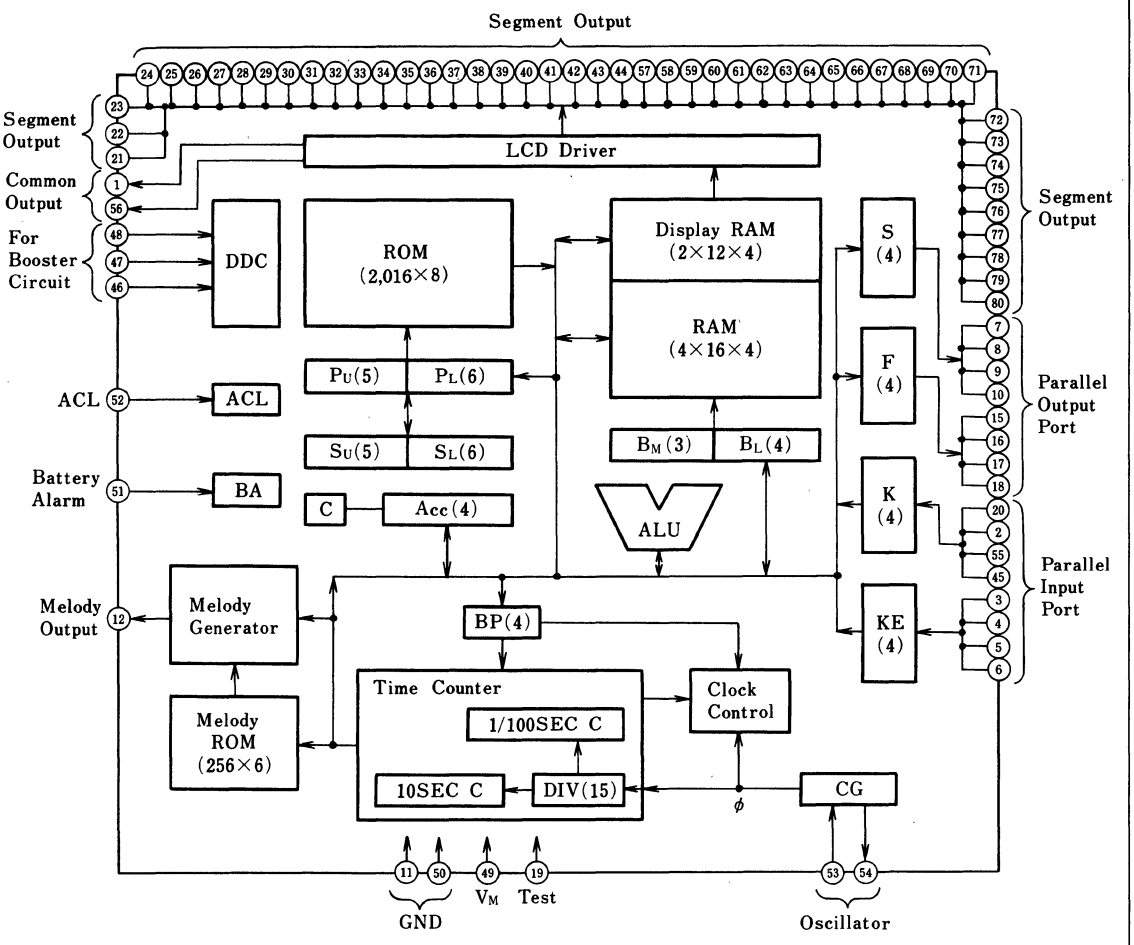
■ Features

1. CMOS process
2. ROM capacity 2,016×8 bits
3. RAM capacity 64×4+24×4 bits
4. Instructions 49
5. Subroutine nesting 1 level
6. Input ports 8 bits
7. Output ports 58 bits
8. Timer/Counter
   (On-chip 15-stage divider with reset, 10-second counter and 1/100-second counter)
9. Direct LCD driver circuit (3V, 1/2 duty, 1/2 bias and 96 segments MAX.)
10. On-chip crystal controlled oscillator (32.768kHz)
11. Melody generator circuit
12. Standby mode (1.5 μA current consumption)
13. Single power supply −1.5V (TYP.)
14. Instruction cycle 91.6 μs
15. 80-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

ALU	: Arithmetic logic unit	DDC	: LCD supply voltage generator
Acc	: Accumulator	DIV	: Frequency divider
ACL	: Auto clear	CG	: Clock generator
C	: Carry F/F	BA	: Battery alarm circuit
P_U, P_L	: Program counter	B_M, B_L	: RAM address register
S_U, S_L	: Stack register of program counter		

■ Pin Description

Pin name	I/O	Circuit type	Function
$K_1 \sim K_4$	I	Pull down	Acc ← $K_1 \sim K_4$
$KE_1 \sim KE_4$	I	Pull down	Acc ← $KE_1 \sim KE_4$
$O_{10} \sim O_{4B}$	O		Display RAM contents output as LCD segment signals
$H_1 \sim H_2$	O		Tri-value output capability ; used for LCD common output
$F_1 \sim F_4$	O		$F_1 \sim F_4$ ← Acc
$S_1 \sim S_4$	O		$S_1 \sim S_4$ ← Acc
S_0	O		Melody output
BA	I		For battery alarm
Test	I	Pull down	For test (Connected to V_{DD} normally)
ACL	I	Pull down	Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DD}, V_{CC}, DDC			LCD driver power supply
V_M, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_M	−2.0 ~ +0.3	V	1
	V_{DD}	−4.0 ~ +0.3	V	1,2
	V_{IN1}	V_M −0.3 ~ +0.3	V	1,3
	V_{IN2}	V_{DD} −0.3 ~ +0.3	V	1
Operating temperature	T_{opr}	−10 ~ +60	℃	
Storage temperature	T_{stg}	−55 ~ +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Applied to pins $K_1 \sim K_4$, $KE_1 \sim KE_4$, $S_1 \sim S_4$, $F_1 \sim F_4$, SO, Test, DDC, BA, ACL, OSC_{IN}, OSC_{OUT}
Note 3: Applied to pins O_{ij}(i=1~4, j=0~B)H_1, H_2, V_C

■ Recommended Operating Conditions

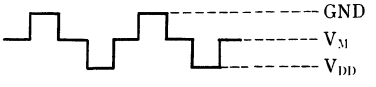
Parameter	Symbol	Ratings	Unit
Supply voltage	V_M	−1.2 ~ −1.8	V
	V_{DD}	−2.3 ~ −3.6	V
Oscillation start voltage	V_{OSC}	−1.4	V
Oscillator frequency	f_{OSC}	32.768(TYP.)	kHz

■ Electrical Characteristics

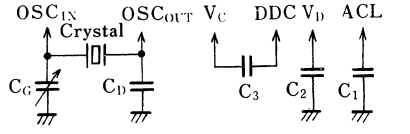
(V_M=−1.45～1.55V, V_{DD}=−2.9～−3.1V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.5			V	4
	V_{IL}				V_M+0.5	V	
Input current	I_{IH1}	V_{IN}=0V	0.155		3	μA	5
	I_{IH2}	V_{IN}=0V	1.55		30	μA	6
Boost output voltage	V_{DD1}	V_M=−1.55V, R_L=5MΩ			−2.80	V	7
	V_{DD2}	V_M=−1.30V, R_L=5MΩ			−2.30	V	
Output current	I_{O1}	V_{DS}=0.5V	10			μA	8
	I_{O2}	V_{DS}=0.5V	60			μA	9
	I_{O3}	V_{DS}=0.5V	60			μA	10
	I_{O4}	V_{DS}=0.5V	120			μA	11
	I_{OH1}	V_{OUT}=−0.5V	160			μA	12
	I_{OL1}	V_{OUT}=V_M+0.5V	10			μA	
	I_{OH2}	V_{OUT}=−0.5V	10			μA	13
	I_{OL2}	V_{OUT}=V_M+0.5V	1.5			μA	
	I_{OH3}	V_{OUT}=−0.5V	100			μA	14
	I_{OL3}	V_{OUT}=V_M+0.5V	3			μA	
	I_{O5}	V_{DS}=0.5V	100			μA	15
Current consumption	I_{DO}	During all operation		12		μA	16
	I_{DS}	During system clock stop		1.5		μA	
Oscillation start time	T_{OSC}			10		s	17

Note 4: Applied to pins K_1～K_4, KE_1～KE_4, Test, ACL, OSC_{IN}
Note 5: Applied to pins K_1～K_4, KE_1～KE_4, ACL
Note 6: Applied to pin Test
Note 7: Applied to pin V_{DD}
Note 8: Applied to pins O_{ij} (i=1～4, j=0～B)
Note 9: Applied to pins H_1, H_2
Note 10: Applied to pin DDC
Note 11: Applied to pin V_C
Note 12: Applied to pin SO
Note 13: Applied to pins S_1～S_4
Note 14: Applied to pin F_1
Note 15: Applied to pins F_2～F_4
Note 16: Current consumption during 32.768kHz
Note 17: Oscillation circuit constant, C_G=15pF, C_P=22pF



● H_1, H_2 Waveform



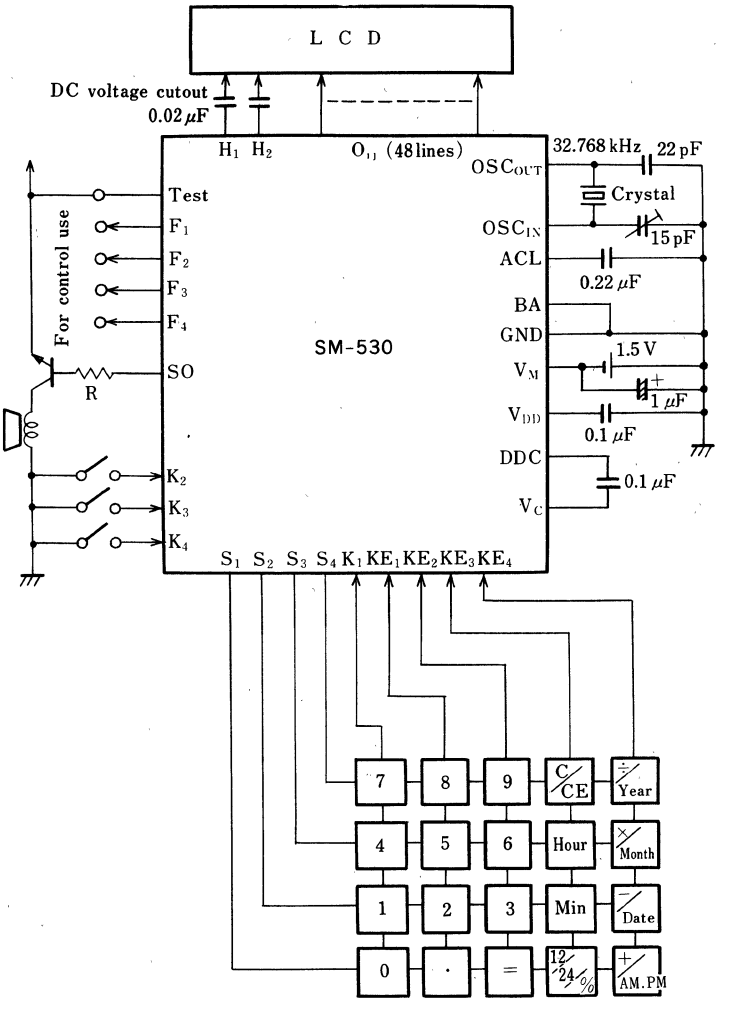
C_G=15pF, C_D=22pF ● Oscillation circuit

C_1=C_2=C_3=0.1μF ● Boost circuit

■ Applications

1. Digital watch
2. Game machine
3. Digital clock
4. Controllers for home appliances and audio equipment
5. Calculator with clock

■ System Configuration Example (Caluculator watch)



Key matrix

SM-531 CMOS 4-Bit 1-Chip Microcomputer

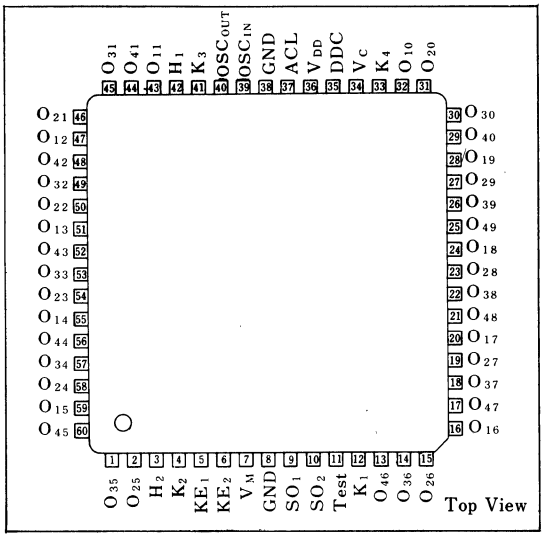
■ Description

The SM-531 is a 4-bit single chip CMOS microcomputer with 1,260 bytes of ROM, 52 words of RAM, melody generator circuit and 80-segment LCD driver circuit. It is well suited for low cost, low power applications with many LCD segments.

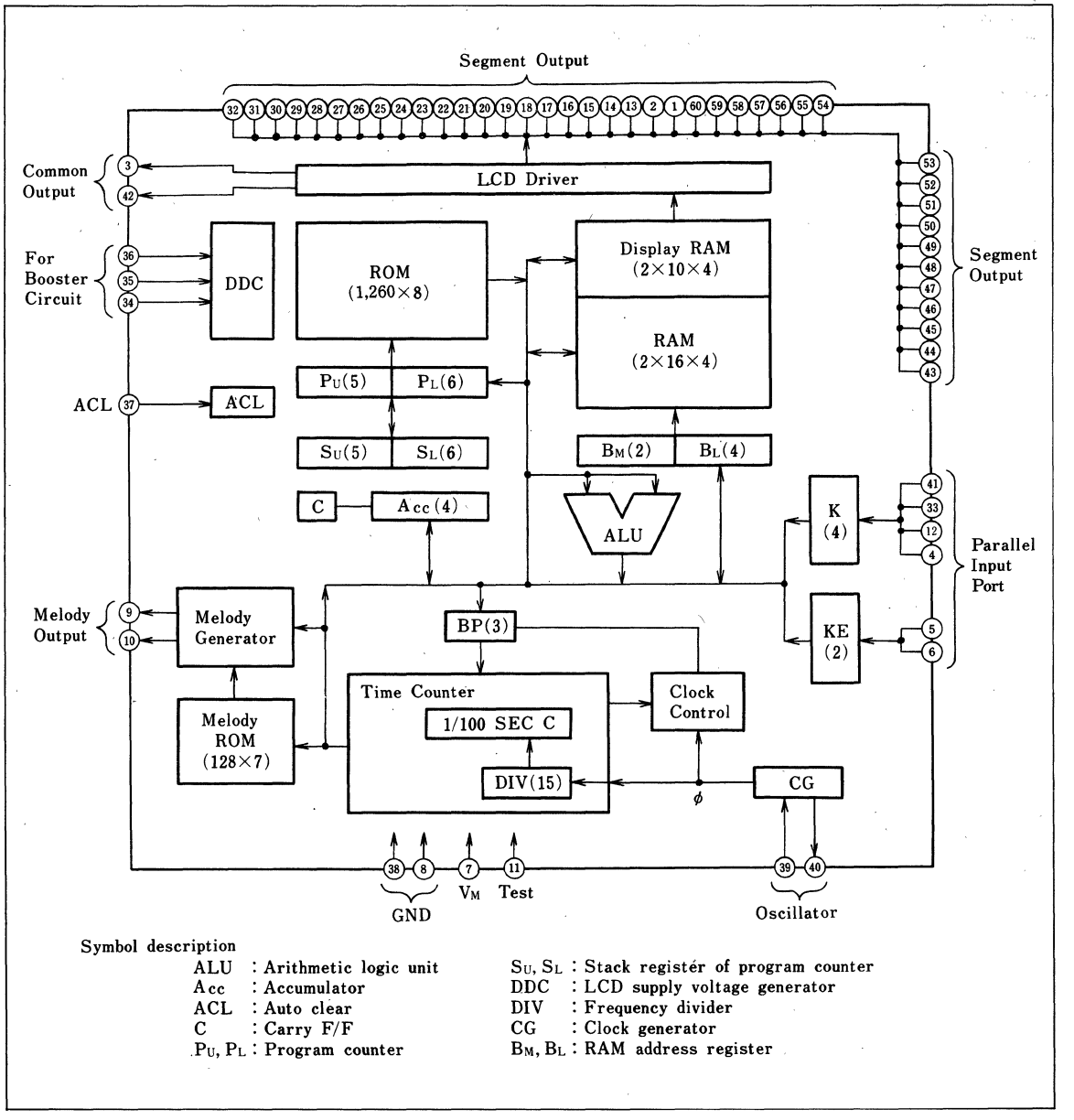
■ Features

1. CMOS process
2. ROM capacity 1,260×8 bits
3. RAM capacity 32×4+20×4 bits
4. Instructions 45
5. Subroutine nesting 1 level
6. Input ports 6 bits
7. Output ports 42 bits
8. Timer/Counter
   (On-chip 15-stage divider with reset, 1/100-second counter)
9. Direct LCD driver circuit (3V, 1/2 duty, 1/2 bias and 80 segments MAX.)
10. On-chip crystal controlled cscillator (32.768kHz)
11. Melody generator circuit
12. Standby mode (1.5 μA current consumption)
13. Single power supply −1.5V (TYP.)
14. Instruction cycle 91.6 μs
15. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

ALU	: Arithmetic logic unit	S_U, S_L	: Stack register of program counter
Acc	: Accumulator	DDC	: LCD supply voltage generator
ACL	: Auto clear	DIV	: Frequency divider
C	: Carry F/F	CG	: Clock generator
P_U, P_L	: Program counter	B_M, B_L	: RAM address register

■ Pin Description

Pin name	I/O	Circuit type	Function
$K_1 \sim K_4$	I	Pull down	Acc ← $K_1 \sim K_4$
KE_1, KE_2	I	Pull down	Acc ← KE_1, KE_2
$O_{10} \sim O_{49}$	O		Display RAM contents output as LCD segment signals
H_1, H_2	O		Tri-value output capability ; used for LCD common output
SO_1, SO_2	O		Melody output
Test	I	Pull down	For test (Connected to V_M normally)
ACL	I		Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DD}, , V_{CC}, DDC			LCD driver power supply
V_M, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_M	$-2.0 \sim +0.3$	V	1
	V_{DD}	$-4.0 \sim +0.3$	V	1
	V_{IN1}	$V_M - 0.3 \sim +0.3$	V	1,2
	V_{IN2}	$V_{DD} - 0.3 \sim +0.3$	V	1,3
Operating temperature	T_{opr}	$-10 \sim +60$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Applied to pins $K_1 \sim K_4$, KE_1, KE_2, SO_1, SO_2, Test, DDC, ACL, OSC_{IN}, OSC_{OUT}
Note 3: Applied to pins O_{ij}(i=1~4, j=0~9), H_1, H_2, Vc

■ Recommended Operating Conditions

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_M	$-1.8 \sim 1.2$	V	
	V_{DD}	$-3.6 \sim 2.3$	V	
Oscillation start voltage	V_{OSC}	-1.4	V	4
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz	

Note 4: Oscillation ciruit constant C_G=15pF, C_D=22pF
Oscillation start time : within 10 seconds

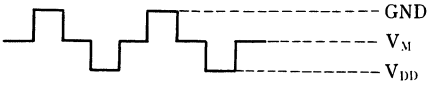
■ Electrical Characteristics

(V_M=−1.45~−1.55V, V_{DD}=−2.9~−3.1V, Ta=25℃)

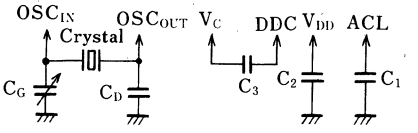
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.5			V	5
	V_{IL}				V_M+0.5	V	
Input current	I_{IH1}	V_{IN}=0V	0.155		3	μA	6
	I_{IH2}	V_{IN}=0V	1.55		50	μA	7
Boost output voltage	V_{DD1}	V_M=−1.55V, R_L=5MΩ			−2.80	V	8
	V_{DD2}	V_M=−1.30V, R_L=5MΩ			−2.30	V	
Output current	I_{O1}	V_{DS}=0.5V	10			μA	9
	I_{O2}	V_{DS}=0.5V	60			μA	10
	I_{O3}	V_{DS}=0.5V	60			μA	11
	I_{O4}	V_{DS}=0.5V	120			μA	12
	I_{O5}	V_{DS}=0.5V	900			μA	13
Current consumption	I_{DO}	During all operation		10		μA	14
	I_{DS}	During system clock stop		1.5		μA	
Oscillation starting time	T_{OSC}			10		s	15

Note 5: Applied to pins K_1~K_4, KE_1, KE_2, , ACL, OSC_{IN}
Note 6: Applied to pins K_1~K_4, KE_1, KE_2, ACL
Note 7: Applied to pin Test
Note 8: Applied to pin V_{DD}
Note 9: Applied to pins O_{ij} (i=1~4, j=0~9)
Note 10: Applied to pins H_1, H_2
Note 11: Applied to pin DDC
Note 12: Applied to pin V_C
Note 13: Applied to pins SO_1, SO_2
Note 14: Current consumption at 32.768kHz
Note 15: Oscillation circuit constant C_G=15pF, C_D=22pF

● H_1, H_2 Waveform



● Oscillation circuit, Boost circuit

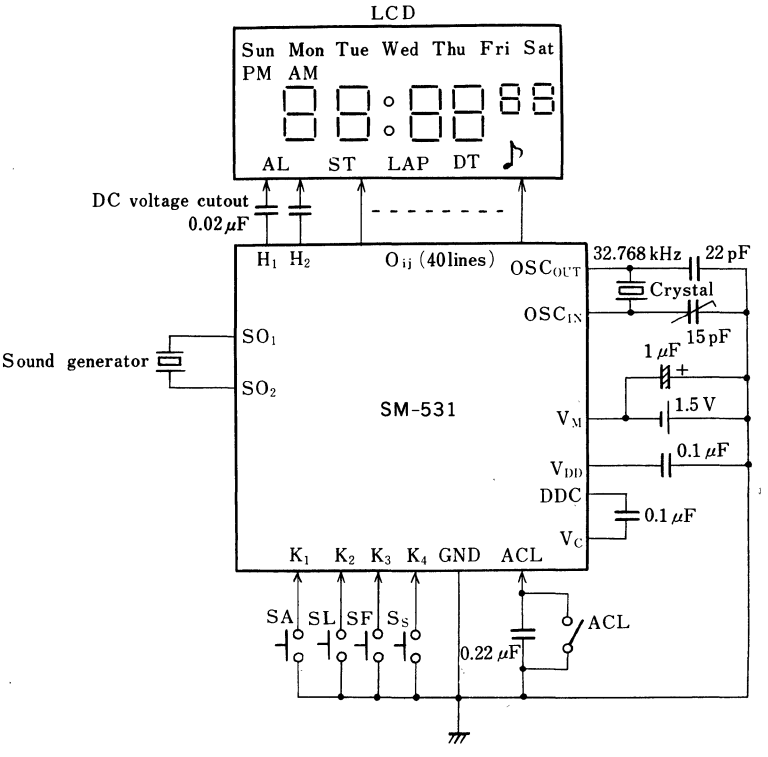


C_G=15pF, C_D=22pF C_1=C_2=C_3=0.1μF

Applications

1. Digital watch
2. Game machine
3. Controllers for home appliances and audio equipment
4. Calculator with clock

System Configuration (for melody alarm watch)



SM-540 CMOS 4-Bit 1-Chip Microcomputer

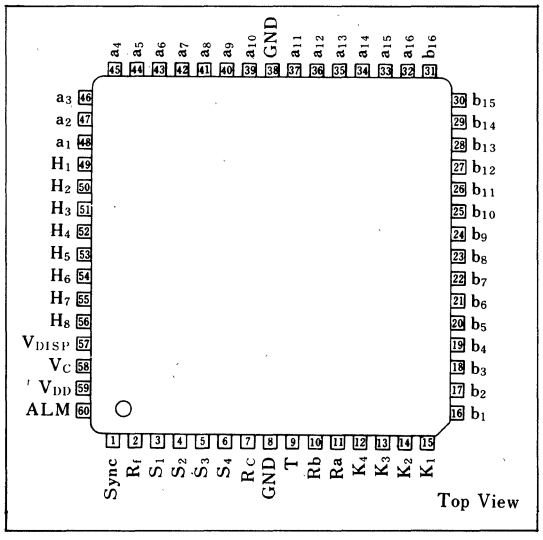
■ Description

The SM-540 is a 4-bit single chip CMOS microcomputer with 2,016 bytes of ROM, 128 words of RAM, a 15-stage divider and a 256-segment liquid crystal driver circuit. It is well suited for low power applications with 16×16 dot-matrix liquid crystal display.

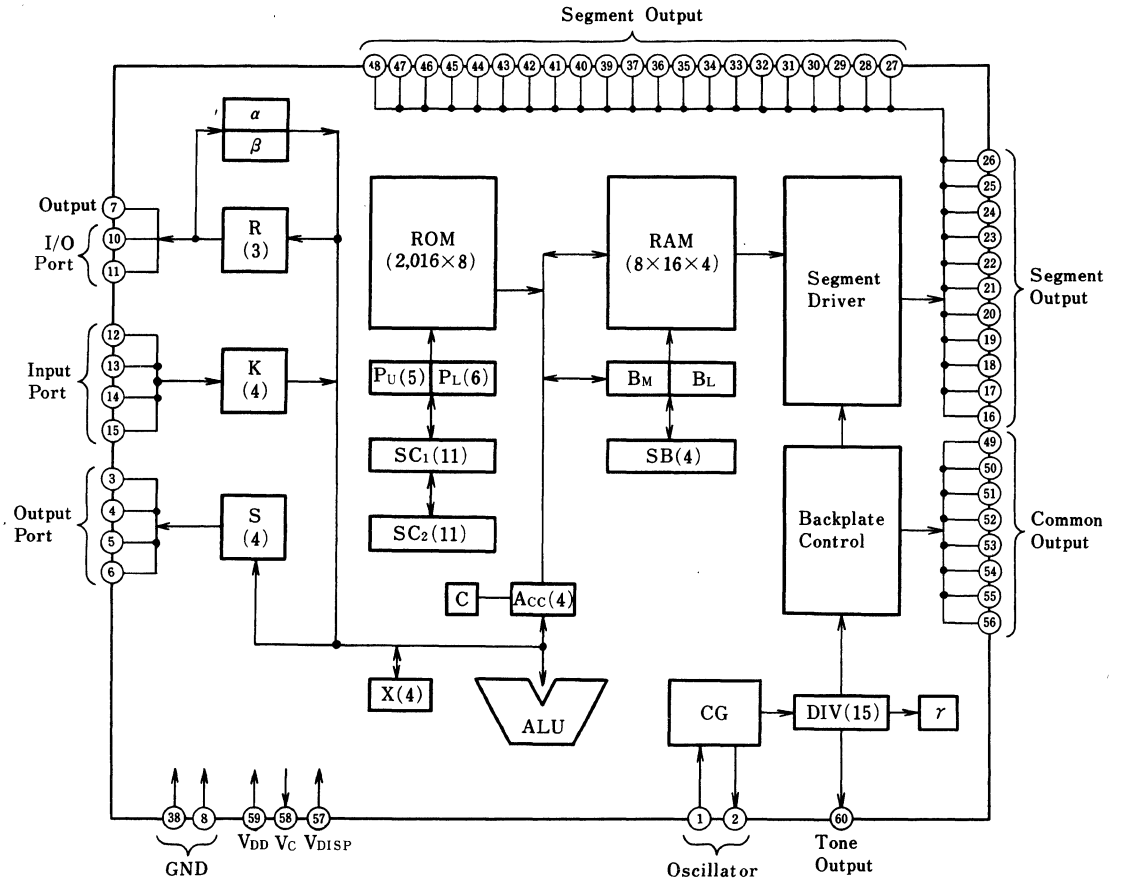
■ Features

1. CMOS process
2. ROM capacity 2,016×8 bits
3. RAM capacity 128×4 bits
4. Instructions 57
5. Subroutine nesting 2 levels
6. Input ports 6 bits
7. Output ports 55 bits
8. On-chip 15-stage divider with reset (timer circuit)
9. Direct LCD driver circuit (4.5V, 1/8 duty, 1/3 bias and 256 segments MAX.)
10. On-chip clock generator circuit
11. Standby mode (1 μA current consumption)
12. Single power supply −4.5V (TYP.)
13. Instruction cycle 16 μs
14. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

ALU	: Arithmetic logic unit	CG	: Clock generator
Acc	: Accumulator	DIV	: Frequency divider
C	: Carry F/F	B_M, B_L	: RAM address register
P, P_L	: Program counter	S	: Shift register
SC_1, SC_2	: Stack register of program counter	X, SB	: Temporary register

■ Pin Description

Pin name	I/O	Circuit type	Function
$K_1 \sim K_4$	I		Acc ← $K_1 \sim K_4$
Ra	I/O	Pull down	R register output ; α F/F is input when R register Ra is reset
Rb	I/O	Pull down	R register output ; β F/F is input when R register Rb is reset
$a_1 \sim a_{16}$ $b_1 \sim b_{16}$	O		Display RAM contents output as LCD segment signals
$H_1 \sim H_8$	O		8-value output capability;used for LCD common output
$S_1 \sim S_4$	O		S register output
RC	O		R register output
ALM	O		For sound generator
T	I	Pull up	For test (Connected to GND normally)
Sync	I		External clock input
Rf	O		System clock output
Vc	O		When system clock is running, output at the same voltage as V_{DD}
V_{DISP}			LCD driver power supply
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{DD}	$-5.5 \sim +0.3$	V	1
	V_{DISP}	$-5.5 \sim +0.3$	V	1,2
	V_{IN}	$V_M - 0.3 \sim +0.3$	V	1
Operating temperature	T_{opr}	$-5 \sim +50$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: $V_{DISP} \leqq V_{DD}$

■ Recommended Operating Conditions

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	$-5.5 \sim +4.0$	V
	V_{DISP}	$-5.5 \sim + - 3.0$	V
Oscillator frequency	f_{osc}	120(TYP.)	kHz

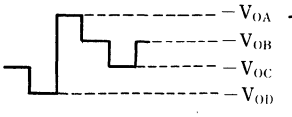
■ Electrical Characteristics

(V_{DD}=−4.5V, Ta=25℃)

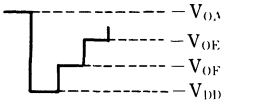
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}				0.6	V	3
	V_{IL}		V_{DD}+0.6			V	
Input current	I_{IH1}	V_{IN}=0V			20	μA	4
	I_{IL1}	V_{IN}=−4.5V			1.5	μA	
	I_{IH2}	V_{IN}=0V			3.0	μA	5
	I_{IL2}	V_{IN}=−4.5V			1.5	μA	
Output voltage	V_{OA}	No load condition V_{DISP}=−4.5V	−0.2			V	6
	V_{OB}	No load condition V_{DISP}=−4.5V	−1.38		−0.97	V	
	V_{OC}	No load condition V_{DISP}=−4.5V	−3.53		−3.12	V	
	V_{OD}	No load condition V_{DISP}=−4.5V			−4.3	V	
	V_{OE}	No load condition V_{DISP}=−4.5V	−2.35		−1.95	V	
	V_{OF}	No load condition V_{DISP}=−4.5V	−2.55		−2.15	V	
Output current	I_{OH1}	V_{OUT}=−0.5V	40			μA	7
	I_{OL1}	V_{OUT}=V_{DD}+0.5V	2			μA	
	I_{OH2}	V_{OUT}=−0.5V	100			μA	5
	I_{OL2}	V_{OUT}=V_{DD}+0.5V	2			μA	
	I_{OH3}	V_{OUT}=−0.5V	100			μA	8
	I_{OL3}	V_{OUT}=V_{DD}+0.5V	5			μA	
	I_{OH4}	V_{OUT}=−0.5V	100			μA	9
	I_{OL4}	V_{OUT}=V_{DD}+0.5V	100			μA	
Current consumption	I_{DA}	During operation		230		μA	10
	I_{DS}	During system clock stop		1		μA	

Note 3: Applied to pins K_1~K_4, R_a, R_b
Note 4: Applied to pins K_1~K_4
Note 5: Applied to pins R_a, R_b
Note 6: Applied to pins H_1~H_8, a_1~a_{16}, b_1~b_{16}
Note 7: Applied to pins S_1~S_4
Note 8: Applied to pin RC
Note 9: Applied to pin ALM
Note 10: f_{OSC}=120kHz(TYP.) and V_{DISP}=−4.5V

● H_1~H_8 Waveform



● a_1~a_8, b_1~b_8 Waveform

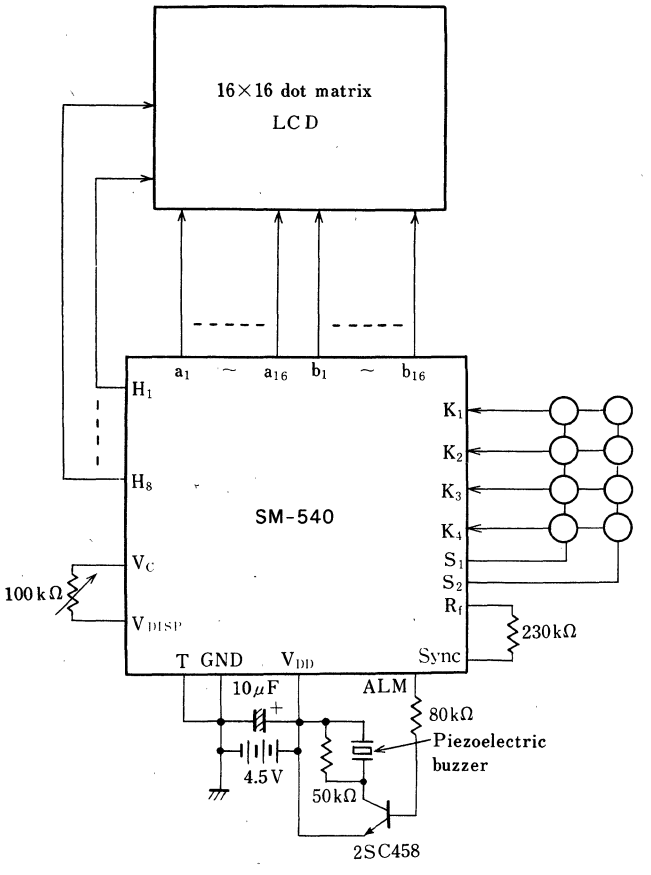


● Clock from external input pin SYNC
50kHz~144kHz

■ Application

1. Game machine

■ System Configuration (for LCD game)



SM-550/SM-555 CMOS 4-Bit 1-Chip Microcomputer

■ Description

The SM-550/SM-555 are 4-bit single chip CMOS microcomputers with 1,024 bytes of ROM, 80 words of RAM, a 15 stage divider and an event counter.

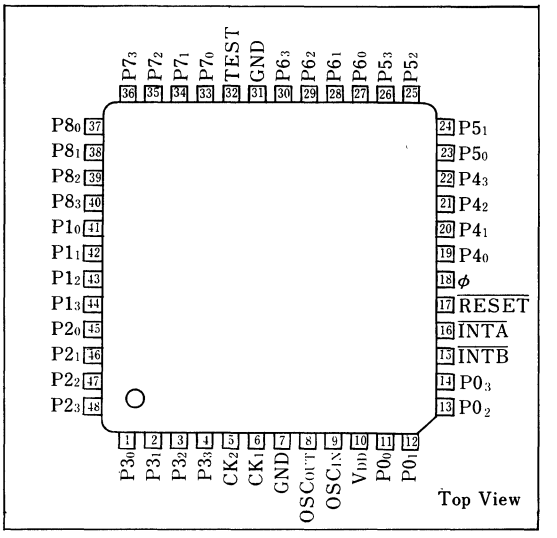
They has the advantages of high-speed instruction cycle of 1.6 μs(SM-550)/3.3 μs(SM-555), 5 different interrupts, subroutine stack in the RAM area, and byte-by-byte data transfer capability.

They are well suited for low power application systems with many control ports.

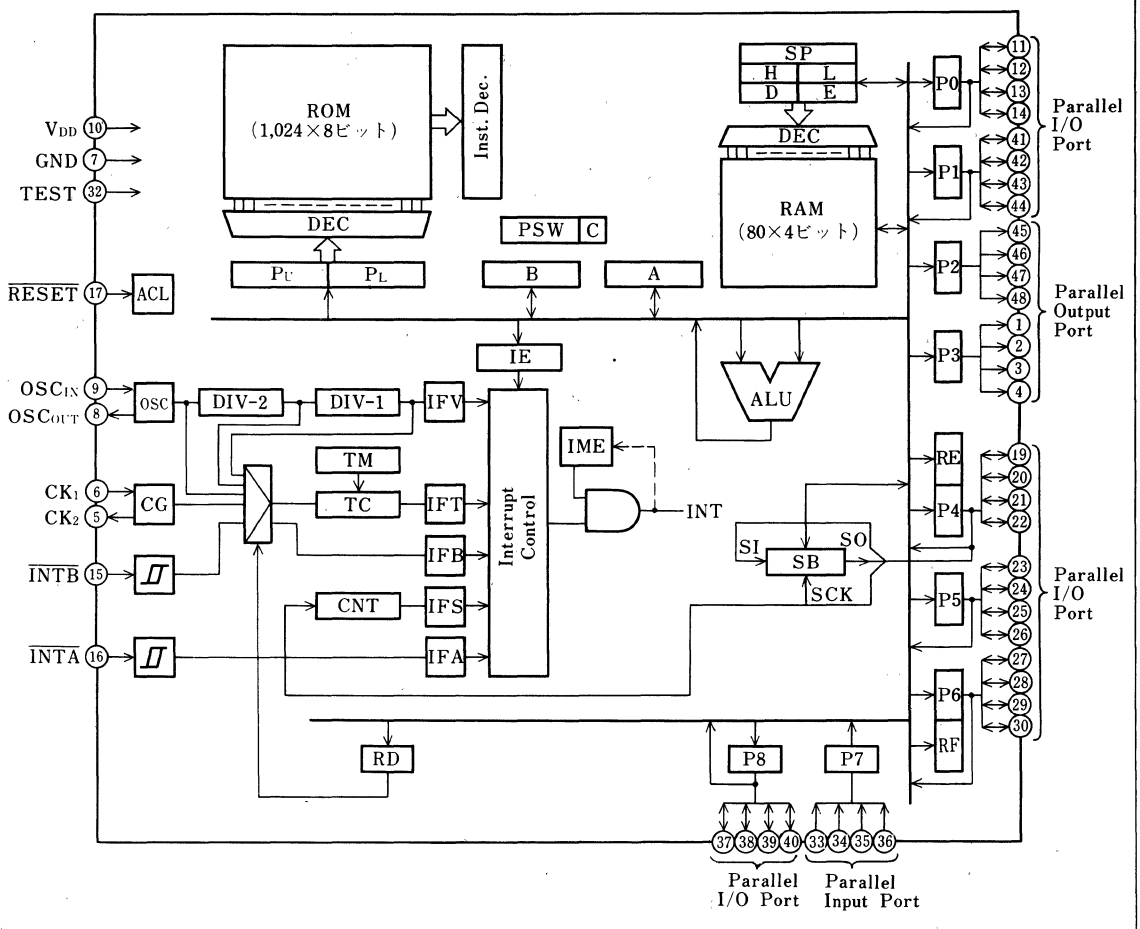
■ Features

1. CMOS process
2. ROM capacity 1,024×8 bits
3. RAM capacity 80×4 bits
4. Instructions 94
5. Subroutine nesting using RAM area
6. Input ports 4 bits
7. Output ports 8 bits
8. Input/Output ports 24 bits
9. Interrupt function
   - External interrupts 2
   - Internal interrupts 3
10. External ROM/RAM expandable
11. Timer/event counter
12. Serial interface 8 bits
13. Standby mode (10 μA current consumption)
14. Single power supply (2.7～5.5V)
15. Instruction cycle (MIN.)
    - 1.6 μs(SM-550)
    - 3.3 μs(SM-555)
16. 48-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

A,B	: Accumulators	PU, PL	: Program counters
ACL	: Auto clear circuit	P0～PB	: Registers
ALU	: Arithmetic logic unit	PSW	: Program status word register
CG	: Clock generator	RD,RE,RF	: Mode registers
DIV	: Divider	SB	: Shift registers
H,L,D,E	: General-purpose registers	SP	: Stack pointer
IE	: Interrupt enable F/F	TC	: Count registers
IFT,IFA,IFS		TM	: Module registers
IFB,IFV	: Interrupt requests		
IME	: Interrupt mask enable F/F		

■ Pin Description

Pin name	I/O	Circuit type	Function
P7	I	Pull up	4-bit parallel
P0, P1 P5, P8	I/O	Input-pull up	I/O selectable by instruction
P6	I/O	Input-pull up	I/O selectable using RF register
P4	I/O	Input-pull up	Serial interface input capability using RE register
P2, P3	O		4-bit parallel
$\overline{\text{INTA}}$, $\overline{\text{INTB}}$	I	Pull up	Interrupt input
$\overline{\text{TEST}}$	I	Pull down	For test (Connected to GND normally)
$\overline{\text{RESET}}$	I	Pull up	Auto clear
ϕ	O		System clock output
CK_1, CK_2			For system clock oscillation
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	$-0.3 \sim +7.5$	V	1
Input voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V	1
Output voltage	V_{OUT}	$-0.3 \sim V_{DD}+0.3$	V	1
Output current	I_{OUT}	40	mA	2
Operating temperature	T_{opr}	$-20 \sim +70$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Sum of current output from (or flowing into) output pin.

■ Recommended Operating Conditions

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage		V_{DD}		2.7		5.5	V	
Crystal oscillator frequency		f_{OSC}			32.768		kHz	3
Basic clock oscillator frequency	SM-550	f	$V_{DD}=5V$	0.25		2.5	MHz	4
			$V_{DD}=3V$	0.25		1		
	SM-555	f	$V_{DD}=5V$	0.25		1.2	MHz	
			$V_{DD}=3V$	0.25		0.48		

Note 3: Oscillation start time : within 10 seconds
Note 4: Degree of fluctuation frequency : ±30%
(tolerance of voltage fluctuation: ±10%)

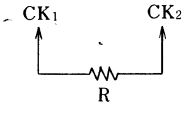
■ Electrical Characteristics

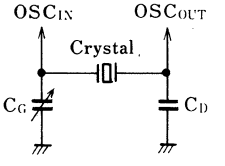
(V_{DD}=2.7～5.5V, Ta=−20～+70℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}			0.7V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.3V_{DD}	V	
	V_{IH2}			V_{DD}−0.5		V_{DD}	V	2
	V_{IL2}			0		0.5	V	
Input current	I_{IN}	V_{IH}=0V		2		200	μA	1
			V_{DD}=5.0V±10%	20		200		
Output current	I_{OH1}	V_{OH}=V_{DD}−0.5V		50			μA	3
	I_{OL1}	V_{OL}=0.5V		250			μA	
	I_{OH2}	V_{OH}=V_{DD}−0.5V		100			μA	4
	I_{OL2}	V_{OL}=0.5V		500			μA	
	I_{OH3}	V_{OH}= V_{DD}−0.5V		100			μA	5
			V_{DD}=5.0V±10%	400				
	I_{OL3}	V_{OL}=0.5V		0.5			mA	
			V_{DD}=5.0V±10%	1.6				
Current consumption	I_{OP}	f=0.5 MHz, V_{DD}=3.0V±10%			0.9		mA	6
		f=1 MHz, V_{DD}=5.0V±10%			1			
	I_{ST}				5		μA	7
		Standby current	V_{DD}=3.0V±10%		12			8
			V_{DD}=5.0V±10%		50			

Note 1: Applied to pins $P0_0$～$P0_3$, $P1_0$～$P1_3$, $P4_0$～$P4_3$, $P5_0$～$P5_3$, $P6_0$～$P6_3$, $P8_0$～$P8_3$ (during input mode)
$P7_0$～$P7_3$, $\overline{INTA}$, $\overline{INTB}$, $\overline{RESET}$.
Note 2: Applied to pins CK_1, OSC_{IN}, TEST.
Note 3: Applied to pin CK_2
Note 4: Applied to pin ϕ
Note 5: Applied to pins $P0_0$～$P0_3$, $P1_0$～$P1_3$, $P4_0$～$P4_3$, $P5_0$～$P5_3$, $P6_0$～$P6_3$,
$P8_0$～$P8_3$ (during output mode)
$P2_0$～$P2_3$, $P3_0$～$P3_3$
Note 6: No-load condition
Note 7: No-load condition when crystal oscillation circuit is not operating. Connect OSC_{IN} pin to GND.
Note 8: No-load condition when crystal oscillation circuit is operating

● Oscillation circuit



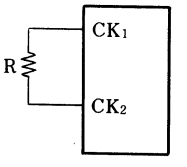


C_G=15pF, C_D=22pF

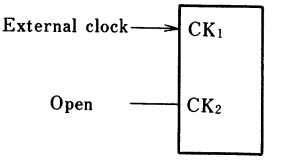
● Clock oscillation circuit

The clock oscillation circuit is composed by connecting a resistance to the CK_1 and CK_2 pins. When inputting an external clock directly, input it through CK_1 and leave CK_2 open.

The system clock (ϕ) used is the clock supplied to CK_1 divided by 4.



CR oscillation

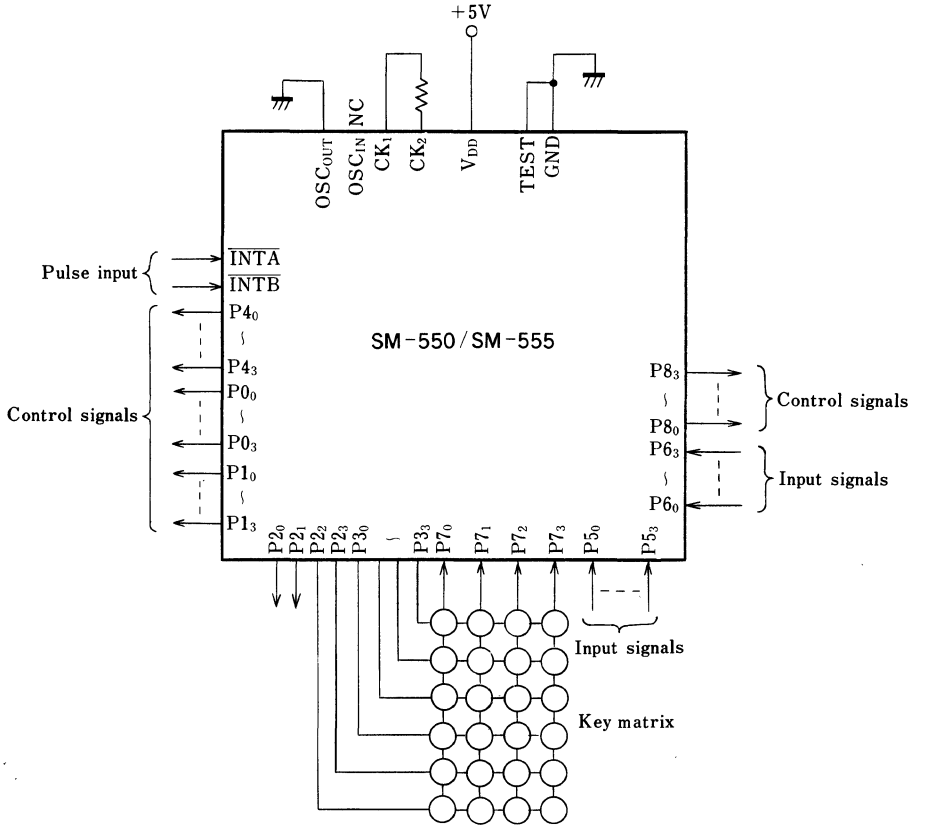


External clock

■ Applications

1. Controllers for various home appliances, audio equipment, office equipment, etc.
2. Vending machines

■ System Configuration (for mechanism controller)

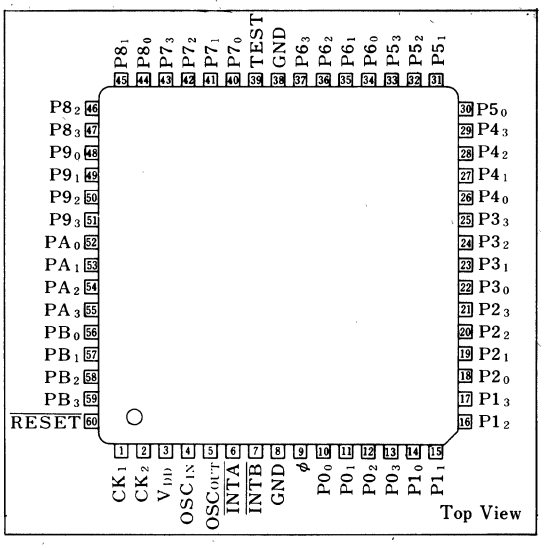


SM-551/SM-556 CMOS 4-Bit 1-Chip Microcomputer

■ Description

The SM-551/SM-556 is a 4-bit single chip CMOS microcomputer with 2,048 bytes of ROM, 128 words of RAM, a 15-stage divider, an event counter and 48 I/O ports. It has the advantages of a high-speed instruction cycle of 1.6 μs, 5 different interrupts, subroutine stack in the RAM area, and byte-by-byte transfer capability. It is well suited for low power application systems with many control ports.

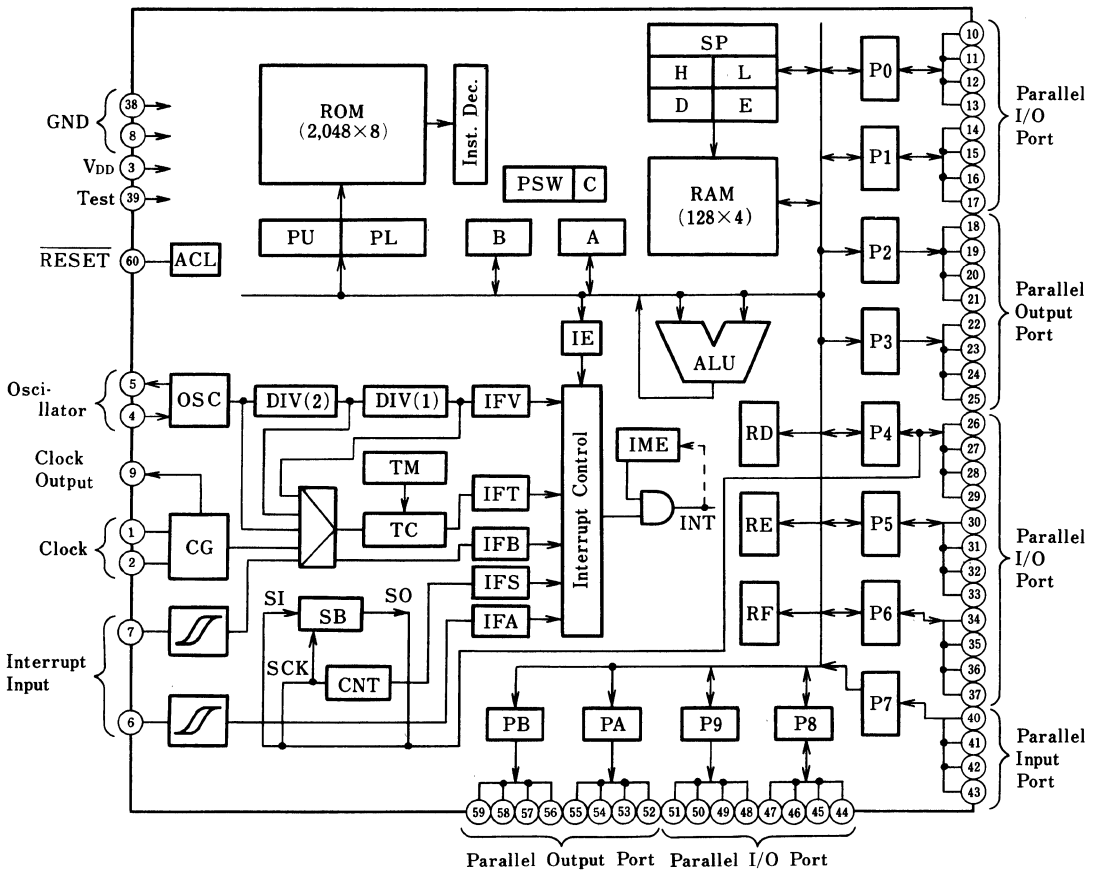
■ Pin Connections



■ Features

1. CMOS process
2. ROM capacity 2,048×8 bits
3. RAM capacity 128×4 bits
4. Instructions 94
5. Subroutine nesting using RAM area
6. Input ports 4 bits
7. Output ports 16 bits
8. Input/Output ports 28 bits
9. Interrupt function
   - External interrupt 2
   - Internal interrupt 3
10. External ROM/RAM expandable
11. Timer/event counter
12. Serial interface 8 bits
13. Standby mode (10 μA current consumption)
14. Single power supply (+2.7～+5.5V)
15. Instruction cycle (MIN.)
    - 1.6 μs(SM-551)
    - 3.3 μs(SM-556)
16. 60-pin quad-flat package

■ Block Diagram



Symbol description

A, B	: Accumulators	IME	: Interrupt mask enable F/F
ACL	: Auto clear	PU, PL	: Program counters
ALU	: Arithmetic logic unit	P0～PB	: Registers
CG	: Clock generator	PSW	: Program status word register
DIV	: Divider	RD, RE, RF	: Mode registers
H, L,D, E	: General-purpose registers	SB	: Shift register
IE	: Interrupt enable F/F	SP	: Stack pointer
IFT, IFA, IFS, IFB, IFV	: Interrupt requests	TC	: Count register
		TM	: Module register

■ Pin Description

Pin name	I/O	Circuit type	Function
P7	I	Pull up	4-bit pararell
P0, P1 P5, P8	I/O	Input-pull up	I/O selectable by instruction
P6	I/O	Input-pull up	I/O selectable using RF register
P4	I/O	Input-pull up	Serial interface input capability using RE register
P9, PA, PB	I/O	Input-pull up	I/O selectable by instruction
P2, P3	O		4-bit pararell
$\overline{INTA}$, $\overline{INTB}$	I	Pull up	Interrupt input
TEST	I	Pull down	For test (Connected to GND normally)
$\overline{RESET}$	I	Pull up	Auto clear
ϕ	O		System clock output
CK_1, CK_2			For system clock oscillation
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DD},GND			Power supply for logic curcuit

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	$-0.3 \sim +7.5$	V	1
Input voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V	1
Output voltage	V_{OUT}	$-0.3 \sim V_{DD}+0.3$	V	1
Output current	I_{OUT}	40	mA	2
Operating temperature	T_{opr}	$-20 \sim +70$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Sum of current output from (or flowing into) output pin.

■ Recommended Operating Conditions

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage		V_{DD}		2.7		5.5	V	
Crystal oscillator frequency		f_{OSC}			32.768		kHz	3
Basic clock oscillation frequency	SM-551	f	$V_{DD}=5.0V$	0.25		2.5	MHz	4
			$V_{DD}=3.0V$	0.25		1.0		
	SM-556	f	$V_{DD}=5.0V$	0.25		1.2	MHz	
			$V_{DD}=3.0V$	0.25		0.48		

Note 3: Oscillation start time : within 10 seconds
Note 4: Degree of fluctuation frequency : ±30%
(tolerance of voltage fluctuation : ±10%)

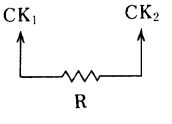
■ Electrical Characteristics

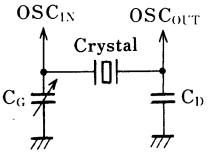
(V_{DD}=2.7～5.5V, Ta=−20～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		0.7V_{DD}		V_{DD}	V	5
	V_{IL1}		0		0.3V_{DD}	V	
	V_{IH2}		V_{DD}−0.5		V_{DD}	V	6
	V_{IL2}		0		0.5	V	
Input current	I_{IN}	V_{IH}=0V	2		200	μA	5
		V_{DD}=5.0V±10%	20		200		
Output current	I_{IH1}	V_{OH}=V_{DD}−0.5V	50			μA	7
	I_{OL1}	V_{OL}=0.5V	250			μA	
	I_{OH2}	V_{OH}=V_{DD}−0.5V	100			μA	8
	I_{OL2}	V_{OL}=0.5V	500			μA	
	I_{OH3}	V_{OH}=	100			μA	9
		V_{DD}−0.5V, V_{DD}=5.0V±10%	400				
	I_{OL3}	V_{OL}=0.5V	0.5			mA	
		V_{DD}=5.0V±10%	1.6				
Current consumption	I_{OP}	f=0.5 MHz, V_{DD}=3.0V±10%		0.9		mA	10
		f=1 MHz, V_{DD}=5.0V±10%		1			
	I_{ST}	Standby current		5		μA	11
		V_{DD}=3.0V±10%		12			12
		V_{DD}=5.0V±10%		50			

Note 5: Applied to pins $P0_0$～$P0_3$, $P1_0$～$P1_3$, $P4_0$～$P4_3$, $P5_0$～$P5_3$, $P6_0$～$P6_3$, $P8_0$～$P8_3$, $P9_0$～$P9_3$ (during input mode) $P7_0$～$P7_3$, INTA, INTB, RESET.
Note 6: Applied to pins CK_1, OSC_{IN}, TEST.
Note 7: Applied to pin CK_2
Note 8: Applied to pin ϕ
Note 9: Applied to pins $P0_0$～$P0_3$, $P1_0$～$P1_3$, $P4_0$～$P4_3$, $P5_0$～$P5_3$, $P6_0$～$P6_3$, $P8_0$～$P8_3$, $P9_0$～$P9_3$ (during output mode) $P2_0$～$P2_3$, $P3_0$～$P3_3$, PA_0～PA_3, PB_0～PB_3
Note 10: No-load condition
Note 11: No-load condition when crystal oscillation circuit is not operating
Note 12: No-load condition when crystal oscillation circuit is operating

● Oscillation Circuit



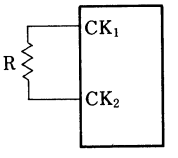


C_G=15 pF, C_D=22 pF

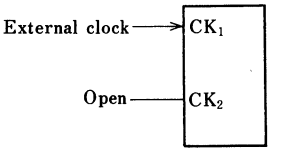
● Clock Oscillation Circuit

The clock oscillation circuit is composed by connecting a resistance to the CK_1 and CK_2 pins. When inputting an external clock directly, input it through CK_1 and leave CK_2 open.

The system clock (ϕ) used is the clock supplied to CK_1 divided by 4.



CR oscillation

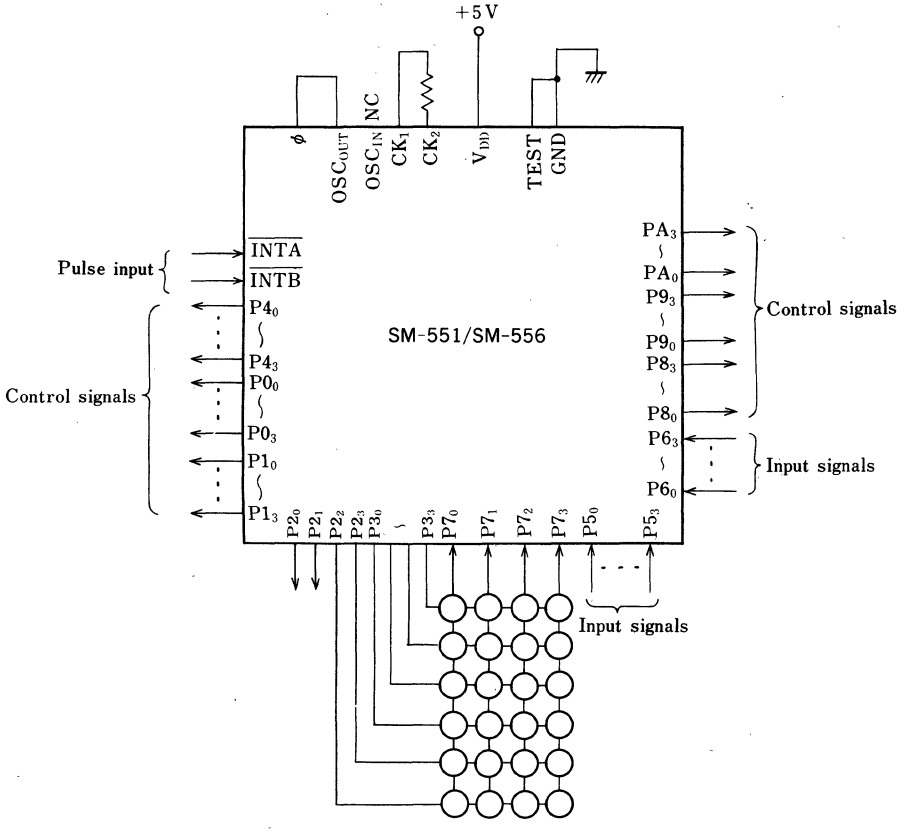


External clock

■ Applications

1. Controllers for various home appliances, audio equipment, office equipment, etc.
2. Vending machines

■ System Configuration (for mechanism controller)



SM-552/SM-557 CMOS 4-Bit 1-Chip Microcomputer

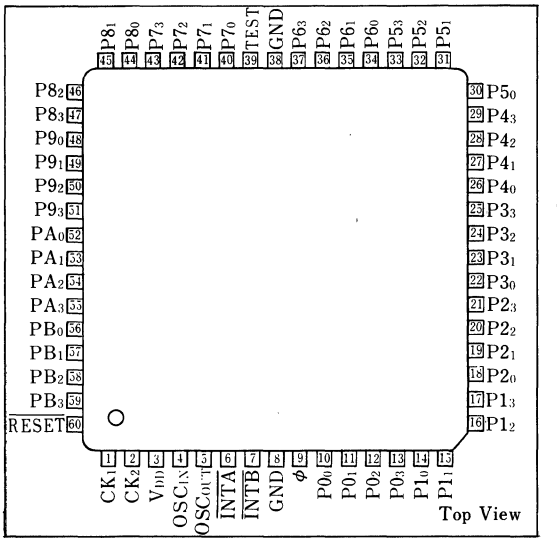
■ Description

The SM-552/SM-557 is a 4-bit single chip CMOS microcomputer with 4,096 bytes of ROM, 256words of RAM, a 15 stage divider and an event counter.

They has the advantages of high-speed instruction cycle of 1.6 μs (SM-552)/3.3 μs (SM-557), 5 different interrupts, subroutine stack in the RAM area, and byte-by-byte data transfer capability.

They are well suited for low power application systems with many control ports.

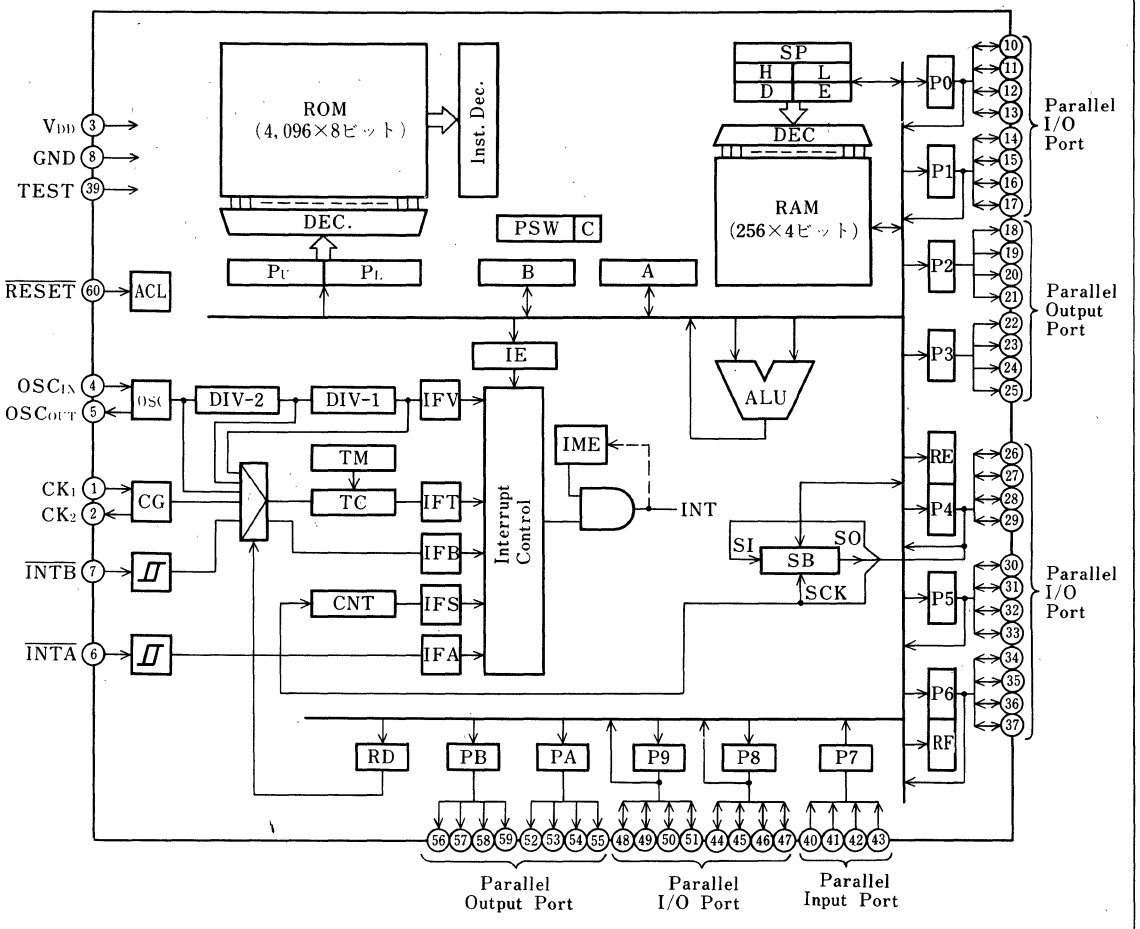
■ Pin Connections



■ Features

1. CMOS process
2. ROM capacity 4,096×8 bits
3. RAM capacity 256×4 bits
4. Instructions 94
5. Subroutine nesting using RAM area
6. Input ports 4 bits
7. Output ports 16 bits
8. Input/Output ports 28 bits
9. Interrupt function
   - External interrupts 2
   - Internal interrupts 3
10. External ROM/RAM expandable
11. Timer/event counter
12. Serial interface 8 bits
13. Standby mode (10 μA current consumption)
14. Single power supply (2.7～5.5V)
15. Instruction cycle (MIN.)
    - 1.6 μs(SM-552)
    - 3.3 μs(SM-557)
16. 60-pin quad-flat package

■ Block Diagram



Symbol description

A,B	: Accumulators	PU, PL	: Program counters
ACL	: Auto clear circuit	P0~PB	: Registers
ALU	: Arithmetic logic unit	PSW	: Program status word register
CG	: Clock generator	RD,RE,RF	: Mode registers
DIV	: Divider	SB	: Shift registers
H,L,D,E	: General-purpose registers	SP	: Stack pointer
IE	: Interrupt enable F/F	TC	: Count registers
IFT,IFA,IFS		TM	: Module registers
IFB,IFV	: Interrupt requests		
IME	: Interrupt mask enable F/F		

■ Pin Description

Pin name	I/O	Circuit type	Function
P7	I	Pull up	4-bit parallel
P0, P1 P5, P8	I/O	Input-pull up	I/O selectable by instruction
P6	I/O	Input-pull up	I/O selectable using RF register
P4	I/O	Input-pull up	Serial interface input capability using RE register
P9, PA, PB	I/O	Input-pull up	I/O selectable by instruction
P2, P3	O		4-bit parallel
$\overline{\text{INTA}}$, $\overline{\text{INTB}}$	I	Pull up	Interrupt input
TEST	I	Pull down	For test (Connected to GND normally)
$\overline{\text{RESET}}$	I	Pull up	Auto clear
ϕ	O		System clock output
CK_1, CK_2			For system clock oscillation
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	$-0.3 \sim +7.5$	V	1
Input voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V	1
Output voltage	V_{OUT}	$-0.3 \sim V_{DD}+0.3$	V	1
Output current	I_{OUT}	40	mA	2
Operating temperature	T_{opr}	$-20 \sim +70$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Sum of current output from (or flowing into) output pin.

■ Recommended Operating Conditions

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage		V_{DD}	2.7		5.5	V	
Crystal oscillator frequency		f_{OSC}		32.768		kHz	
Basic clock oscillator frequency	SM-552	f	0.25		2.5	MHz	3
			0.25		1		4
	SM-557	f	0.25		1.2	MHz	3
			0.25		0.48		4

Note 3: $V_{DD}=5.0V$
Note 4: $V_{DD}=3.0V$

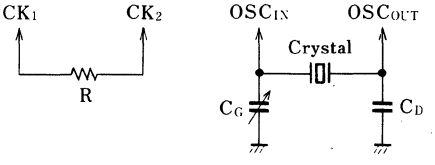
■ Electrical Characteristics

(V_{DD}=2.7～5.5V, Ta=−20～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		0.7V_{DD}		V_{DD}	V	5
	V_{IL1}		0		0.3V_{DD}	V	
	V_{IH2}		V_{DD}−0.5		V_{DD}	V	6
	V_{IL2}		0		0.5	V	
Input current	I_{IN}	V_{IN}=0V	2		200	μA	5
		V_{DD}=5.0V±10%	20		200		
Output current	I_{OH1}	V_{OH}=V_{DD}−0.5V	50			μA	7
	I_{OL1}	V_{OL}=0.5V	250			μA	
	I_{OH2}	V_{OH}=V_{DD}−0.5V	100			μA	8
	I_{OL2}	V_{OL}=0.5V	500			μA	
	I_{OH3}	V_{OH}=	100			μA	9
		V_{DD}−0.5V, V_{DD}=5.0V±10%	400				
	I_{OL3}	V_{OL}=0.5V	0.5			mA	
		V_{DD}=5.0V±10%	1.6				
Current consumption	I_{OP}	f=0.5 MHz V_{DD}=3.0V±10%		0.3		mA	10
		f=1 MHz V_{DD}=5.0V±10%		1			
	I_{ST}	Standby current		50		μA	11
				5			12

Note 5: Applied to pins $P0_0$～$P0_3$, $P1_0$～$P1_3$, $P4_0$～$P4_3$, $P5_0$～$P5_3$, $P6_0$～$P6_3$, $P8_0$～$P8_3$, $P9_0$～$P9_3$ (during input mode) $P7_0$～$P7_3$, $\overline{INTA}$, $\overline{INTB}$, $\overline{RESET}$.
Note 6: Applied to pins CK_1, OSC_{IN}, TEST.
Note 7: Applied to pin CK_2
Note 8: Applied to pin ϕ
Note 9: Applied to pins $P0_0$～$P0_3$, $P1_0$～$P1_3$, $P4_0$～$P4_3$, $P5_0$～$P5_3$, $P6_0$～$P6_3$, $P8_0$～$P8_3$, $P9_0$～$P9_3$, (during output mode) $P2_0$～$P2_2$, $P3_0$～$P3_3$, PA_0～PA_3, PB_0～PB_3
Note. 10: No-load condition
Note. 11: No-load condition when crystal oscillation circuit is operating
Note. 12: No-load condition when crystal oscillation circuit is not operating

● Oscillation Circuit

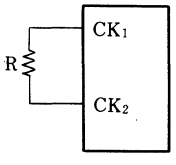


C_G=15pF, C_D=22pF

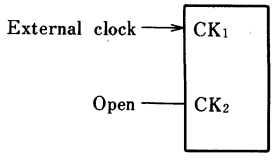
● Clock Oscillation Circuit

The clock oscillation circuit is composed by connecting a resistance to the CK_1 and CK_2 pins. When inputting an external clock directly, input it through CK_1 and leave CK_2 open.

The system clock (ϕ) used is the clock supplied to CK_1 divided by 4.



CR oscillation

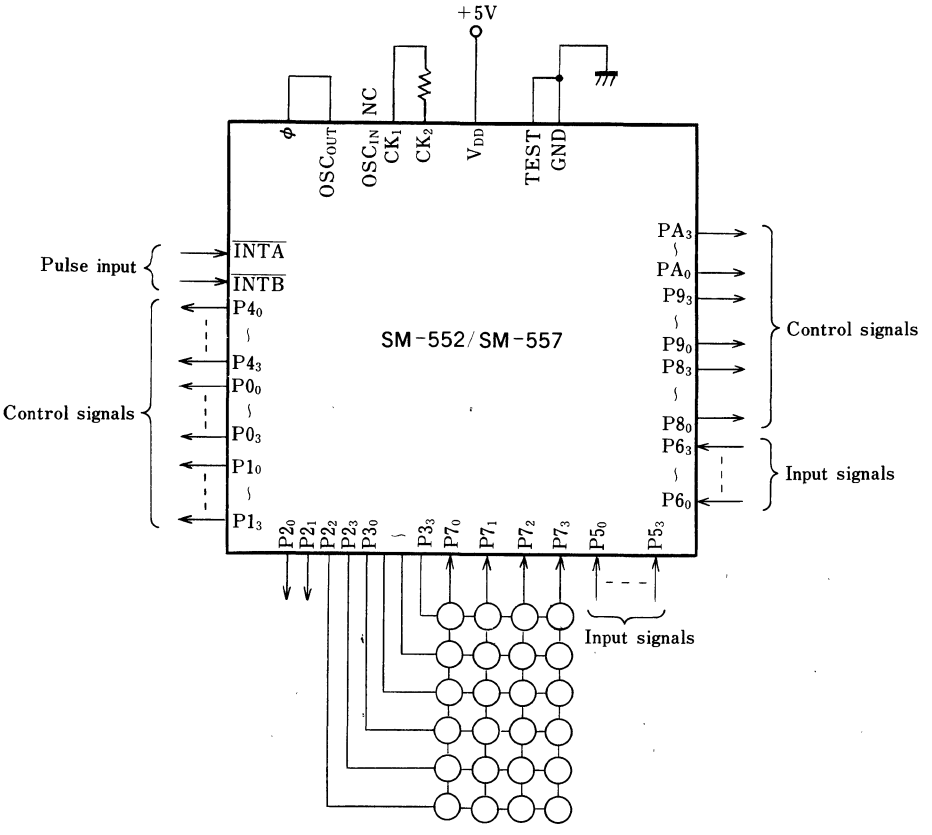


External clock

■ Applications

1. Controllers for various home appliances, audio equipment, office equipment, etc.
2. Vending machines

■ System Configuration (for mechanism controller)



SM-5E3 CMOS 4-Bit 1-Chip Microcomputer

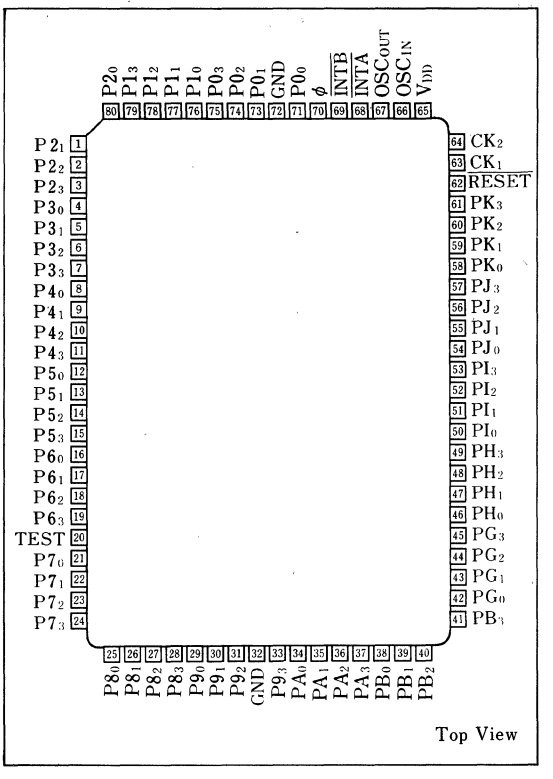
■ Description

The SM-5E3 is a 4-bit single chip CMOS microcomputer with 4,096 bytes of ROM, 256 words of RAM, a 15 stage divider and an event counter. It has the advantages of a high-speed instruction cycle of 1.6 μs, 5 different interrupts, subroutine stack in the RAM area, and byte-by-byte data transfer capability. It is well suited for low power application systems with many control ports.

■ Features

1. CMOS process
2. ROM capacity 4,096×8 bits
3. RAM capacity 256×4 bits
4. Instructions 99
5. Subroutine nesting using RAM area
6. Input ports 4 bits
7. Output ports 16 bits
8. Input/Output ports 48 bits
9. Interrupt function (External interrupts 2 and internal interrupts 3)
10. External ROM/RAM expandable
11. Timer/event counter
12. Serial interface 8 bits
13. Standby mode (50 μA current consumption)
14. Single power supply (+2.7～+5.5V)
15. 1.6 μs instruction cycle (MIN.)
16. 80-pin quad-flat package

■ Pin Connections



SM-563 CMOS 4-Bit 1-Chip Microcomputer

■ Description

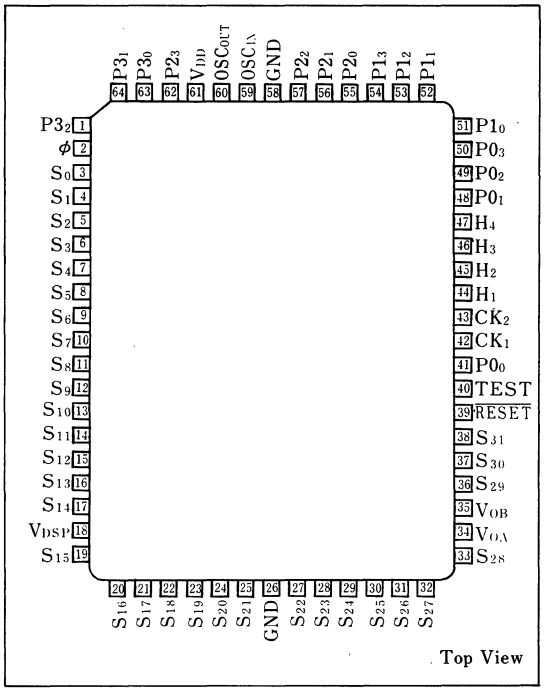
The SM-563 is a 4-bit single chip CMOS microcompter with 4,096 bytes of ROM, 160×4 bits of RAM, timer/event-counter and multiplex interrupt.

It is best suited to controllers of application systems to drive multi LCD segments.

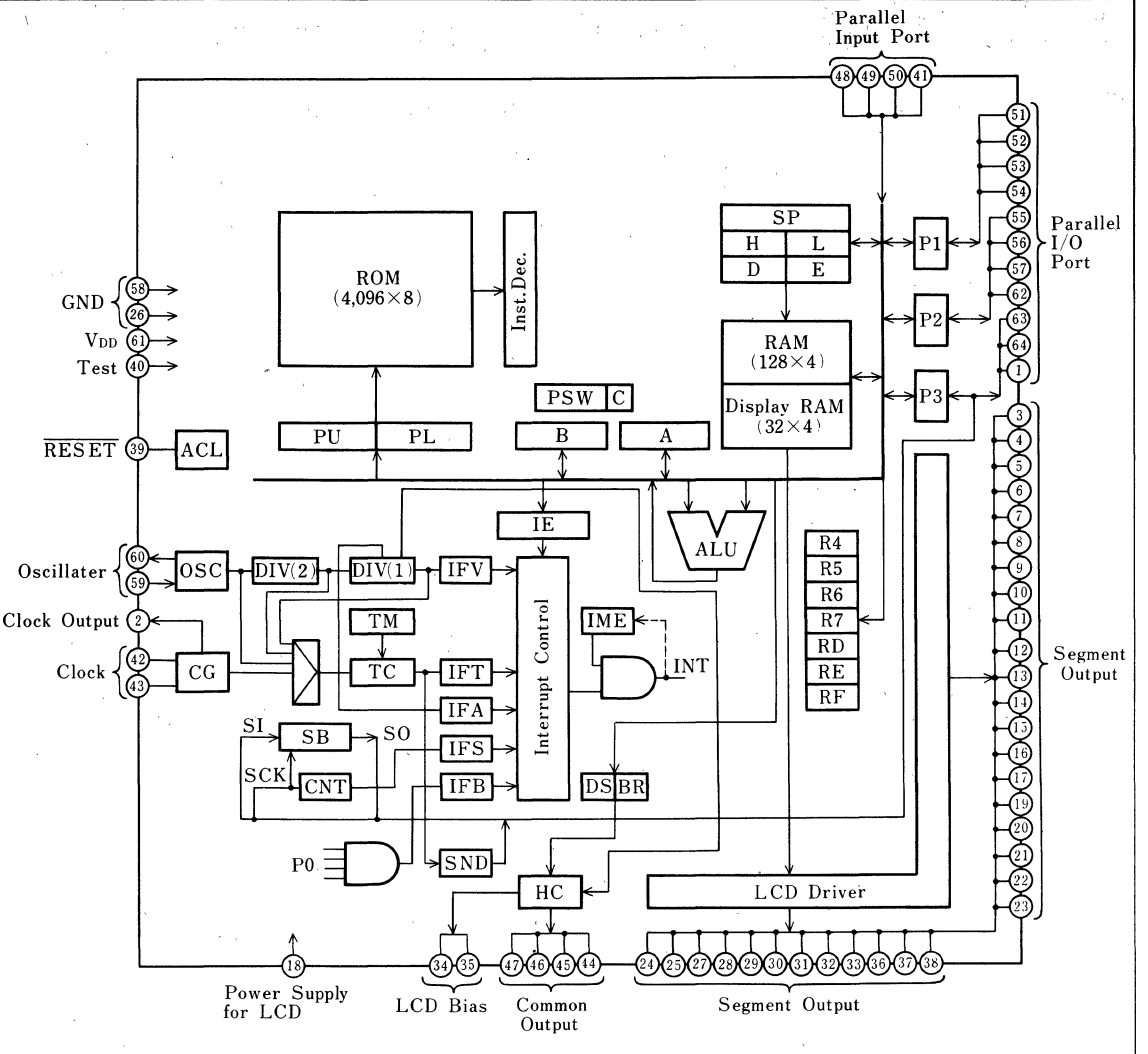
■ Features

1. CMOS process
2. ROM capacity 4,096×8 bits
3. RAM capacity 160×4 bits
   (including 32×4 bits for display)
4. Instructions 93
5. Subroutine nesting using RAM area
6. Input ports 4 bits
7. Input/Output ports 11 bits
8. Timer/event-counter
9. Interrupt functions 5
   - External interrupt
   - Serial I/O interrupt
   - Timer/event-counter interrupt
   - f_4 signal interrupt
   - Divider overflow interrupt
10. Serial interface 8 bits
11. Standby mode
12. Direct LCD driver circuits (1/4 duty, 1/3 bias and 128 segments (MAX.))
13. Insturuction cycle 6.67 μs (MIN.)
14. Single power supply (2.7～5.5V)
15. 64-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

A,B	: Accumulators	IME	: Interrupt mask enable F F
ACL	: Auto clear	P1~P3	: Registers
ALU	: Arithmetic logic unit	PL,PU	: Program counters
BR,DS	: Common signal control F/F	PSW	: Program status word register
CG	: Clock generator	R4~R7	: General-purpose registers
DIV	: Divider	RD,RE,RF	: Mode registers
D,E,H,L	: General-purpose registers	SB	: Shift register
HC	: Common signal circuit	SP	: Stack pointer
IE	: Interrupt enable F/F	TC	: Count register
IFA,IFB		TM	: Module register
IFS,IFT,IFV	: Interrupt requests		

■ Pin Description

Pin name	I/O	Circuit type	Function
$P0_0 \sim P0_3$	I	Pull up	Acc ← $P0_0 \sim P0_3$
$P1_0 \sim P1_3$	I/O	Pull up	I/O selectable by instruction
$P2_0 \sim P2_3$	I/O	Pull up	I/O selectable individually Sound output only when $P2_3$ pin is used for output
$P3_0 \sim P3_3$	I/O	Pull up	Serial interface input capability using RE register
$S_0 \sim S_{31}$	O		Display RAM contents output as LCD segment signals
$H_1 \sim H_4$	O		4-value output capability ; used for LCD common output
TEST	I	Pull down	For test (Connected to GND normally)
$\overline{\text{RESET}}$	I	Pull up	Auto clear
ϕ	O		System clock output
CK_1, CK_2			For system clock oscillation
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DSP}, V_{OA}, V_{OB}			LCD driver power supply
V_{DD}, GND			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	$-0.3 \sim +7$	V	1
	V_{DSP}	$-0.3 \sim +7$	V	
Input voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V	1
Output voltage	V_{OUT}	$-0.3 \sim V_{DD}+0.3$	V	1
Output current	I_{OUT}	20	mA	2
Operating temperature	T_{opr}	$-20 \sim +70$	℃	
Storage temperature	T_{stg}	$-55 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Sum of current output from (or flowing into) output pin.

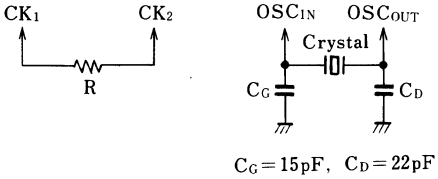
■ Recommended Operating Conditions

($V_{DD}=2.7 \sim 5.5V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		2.7		5.5	V	
	V_{DSP}		2.7		V_{DD}	V	
Basic clock oscillator frequency	f		250		600	kHz	3
		$V_{DD}=4.5 \sim 5.5V$	250		2000		
Instruction cycle	t		6.6		16	μs	
		$V_{DD}=4.5 \sim 5.5V$	2		16		
Crystal oscillator frequency	f_{OSC}			32.768		kHz	

Note 3: Degree of fluctuation frequency: ±30%

● Oscillation circuit



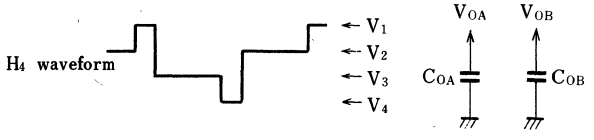
$C_G=15pF$, $C_D=22pF$

■ Electrical Characteristics

(V_{DD}=2.7~5.5V, Ta=−20~+70℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}			0.7V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.3V_{DD}	V	
	V_{IH2}			V_{DD}−0.5		V_{DD}	V	2
	V_{IL2}			0		0.5	V	
Input current	I_{IH}	V_{IN}=0V		20		200	μA	1
			V_{DD}=4.5~5.5V	2		200		
Output current	I_{OH1}	V_{OH}=V_{DD}−0.5V		50			μA	3
	I_{OL1}	V_{OL}=0.5V		250			μA	
	I_{OH2}	V_{OH}=V_{DD}−0.5V		5		250	μA	4
	I_{OL2}	V_{OL}=0.5V		500			μA	
	I_{OH3}	V_{OH}=V_{DD}−0.5V		400			μA	5
			V_{DD}=4.5~5.5V	100				
	I_{OL3}	V_{OL}=0.5V		1.6			mA	
			V_{DD}=4.5~5.5V	0.5				
Output impedance	R_C				5	20	kΩ	6
	R_S				10	40	kΩ	7
Output voltage	V_1			2.7		3	V	8
	V_2	V_{DSP}=3.0V		1.7	2	2.3	V	
	V_3	No-load		0.7	1	1.3	V	
	V_4			0		0.3	V	
Current consumption	I_{OP}	f=600kHz, V_{DD}=3.0V			0.4	1.5	mA	9
	I_{ST}	Standby mode	V_{DSP}=3.0V		15	40	μA	10
			V_{DD}=3.0V		8	20		11

Note 1: Applied to pins $P0_0$~$P0_1$, $\overline{RESET}$
$P1_0$~$P1_3$, $P2_0$~$P2_3$, $P3_0$~$P3_2$ (during input mode)
Note 2: Applied to pins CK_1, Test, OSC_{IN}
Note 3: Applied to pin CK_2
Note 4: Applied to pins $P1_0$~$P1_3$ (during output mode)
Note 5: Applied to pins $P2_0$~$P2_3$, $P3_0$~$P3_2$ (during output mode)
ϕ
Note 6: Applied to pins H_1~H_4
Note 7: Applied to pins S_0~S_{31}
Note 8: Applied to pins H_2~H_4, S_0~S_{31}



C_{OA}=1μF, C_{OB}=1μF

Note 9: No-load condition
Note 10: No-load condition when bleader resistance is ON
Note 11: No-load condition when bleader resistance is OFF

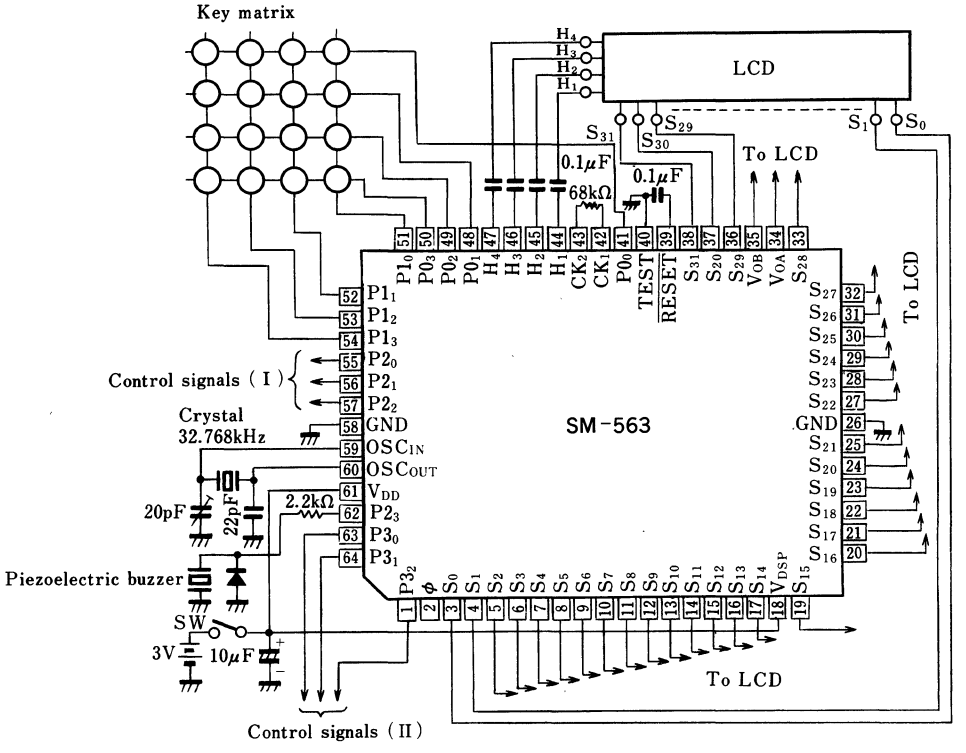
■ Applications

The instruction cycle of the SM563 is fast and the unit operates on little power, and therefore it is ideal for use as a controller with a liquid crystal display in a wide range of hand-held equipment and home appliances.

■ Applications Example

Portable devices, auto dialers, sphygmomanometers, thermometers, pulsemeters, radio controllers, cameras, home appliances, various timers, VTR timers, home security system, pocket games

■ System Configuration



SM-572 CMOS 4-Bit 1-Chip Microcomputer

■ Description

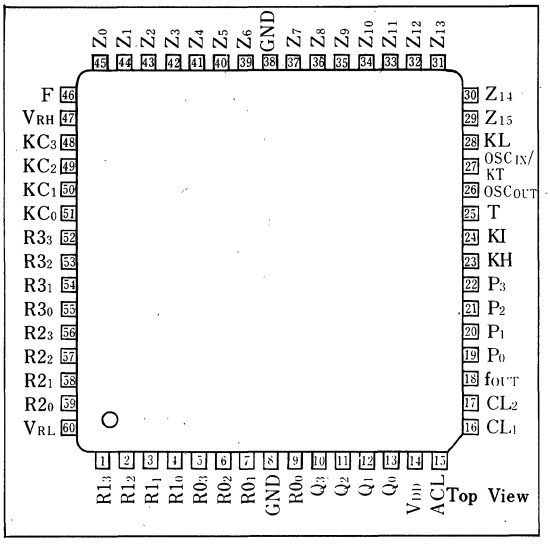
The SM-572 is a 4-bit single chip CMOS microcomputer with 2,032×9 bits of ROM, 128×4 bits of RAM, 8 bits A/D converter and timer/counter.

It is best suited for applications requiring A/D circuits.

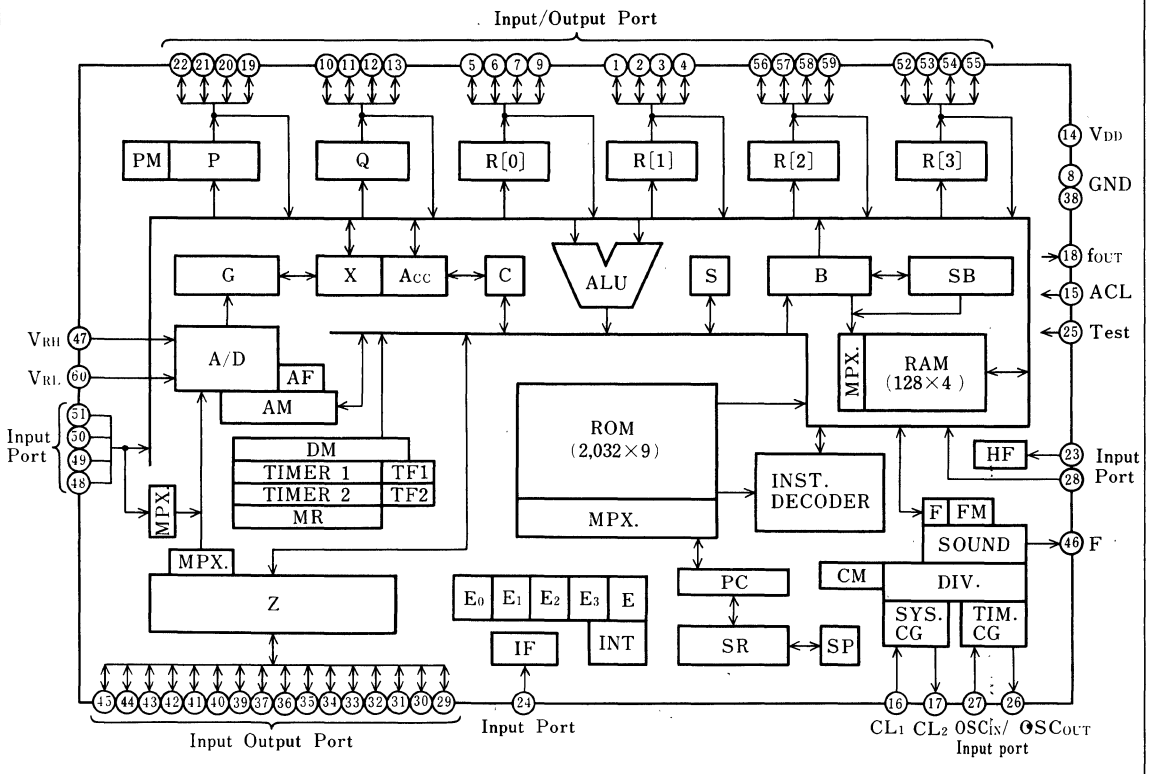
■ Features

1. CMOS process
2. ROM capacity 2,032×9 bits
3. RAM capacity 128×4 bits
4. Instructions 93
5. Subroutine nesting 6 levels
6. Input ports 8 bits
7. Output port 1 bit
8. Input/Output ports 40 bits
9. Timer/counter
   8-bit counters 2
10. Interrupt function
    External interrupt 2
    Timer interrupt 2
11. A/D converter 8 bits
    Conversion time 32 μs(MIN.)
12. Single power supply (2.7～5.5V)
13. Instruction cycle 2 μs (MIN.)
14. 60-pin quad-flat package

■ Pin Connections



Block Diagram



Symbol description

ALU	: Arithmetic logic unit	Acc	: Accumulator
X	: X register	SR	: Stack register
B	: RAM address register	R0,R1,R2,R3	: Latch
C	: Carry F/F	DIV	: Divider
PC	: Program counter		
SP	: Stack pointer		
CG	: System clock generator		
MPX.	: Multiplexer		
A/D	: A D convertor and Comparator unit		

■ Pin Description

Pin name	I/O	Circuit type	Function
$KC_0 \sim KC_3$	I		Acc ← $KC_0 \sim KC_3$ or A/D conversion analog input
KI, KH KT, KL	I		Acc ← KI, KH, KT, KL KI ← (IF flag set), KH ← (HF flag set), KT ← (External timer signal input)
$Z_0 \sim Z_{15}$	I/O		Z registor contents output;Can be tested individually Reset ZF/F when used as input pins
$P_0 \sim P_3$	I/O	3 states	Acc ⟷ $P_0 \sim P_3$
$Q_0 \sim Q_3$	I/O		$Q_0 \sim Q_3$ ← Acc Reset QF/F when used as input pins
R0, R1, R2	I/O		R0, R1, R2 ← Acc Reset RF/F when used as input pins
F	O		Sound output or 1 bit output
T	I	Pull down	For test (Connected to GND normally)
ACL	I	Pull down	Auto clear
f_{OUT}	O		System clock output
CL_1, CL_2			For system clock oscillation
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{RH}, V_{RL}			A/D conversion standard power supply
V_{DD}, GND			Power supply for logic curcuit

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	$-0.3 \sim +7.5$	V
Input voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V
Output voltage	V_{OUT}	$-0.3 \sim V_{DD}+0.3$	V
Output current*	I_{OUT}	30	mA
Operating temperature	T_{opr}	$-10+70$	℃
Storage temperature	T_{stg}	$-55+150$	℃

*Source current from output pin or sum of sync current.

■ Recommended Operating Conditions

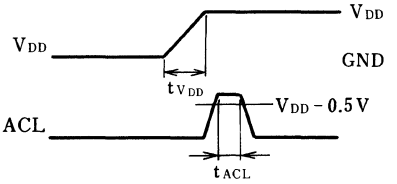
Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	2.7~5.5	V
System oscillator frequency	f_{CL}	4~0.2 (V_{DD}=5V)	MHz
		2~0.2 (V_{DD}=3V)	
System clock frequency	f_S	500~50 (V_{DD}=5V)	kHz
		250~50 (V_{DD}=3V)	
Timer clock frequency	f_{OSC}	32.768 (TYP.)	kHz

■ Electrical Characteristics

(V_{DD}=2.7~5.5V, Ta=−20~+70℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}			0.7V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.3V_{DD}		
	V_{IH2}			V_{DD}−0.5		V_{DD}	V	2
	V_{IL2}			0		0.5		
Input current	I_{IH1}	$V_{IN}=V_{DD}$	V_{DD}=5.0V±10%	80	300	800	μA	3
			V_{DD}=3.0V±10%	20	90	300		
	I_{IH2}	$V_{IN}=V_{DD}$	V_{DD}=5.0V±10%	8	25	100	μA	4
			V_{DD}=3.0V±10%	2	8	35		
Output current	I_{OH1}	$V_{OH}=V_{DD}$−0.5V	V_{DD}=5.0V±10%	1			mA	5,6
			V_{DD}=3.0V±10%	0.4				
	I_{OL1}	V_{OH}=0.5V	V_{DD}=5.0V±10%	25			μA	5
				10				
	I_{OL2}	V_{OH}=0.5V	V_{DD}=5.0V±10%	1			mA	6
				0.4				
	I_{OH}	$V_{OH}=V_{DD}$−0.5V		200			μA	7
	I_{OH2}	V_{OH}=0.5V		200				
ACL input pulse width	t_{ACL}		V_{DD}=5.0V±10%	1			μs	13
			V_{DD}=3.0V±10%					
V_{DD} rise time for the internal ACL operation	t_{VDD}		V_{DD}=5.0V±10%			50	ms	14
			V_{DD}=3.0V±10%					
Current consumption	I_A	f_s=500kHz	V_{DD}=5.0V±10%		1.5		mA	8
			V_{DD}=3.0V±10%		1			
		f_s=100kHz	V_{DD}=5.0V±10%		0.5			
			V_{DD}=3.0V±10%		0.3			
	I_{ST}	OFF mode	V_{DD}=5.0V±10%		5		μA	9
			V_{DD}=3.0V±10%		3			
			V_{DD}=5.0V±10%		50		μA	10
			V_{DD}=3.0V±10%		30			
		Hold mode	V_{DD}=5.0V±10%		400		μA	11
			V_{DD}=3.0V±10%		100			
			V_{DD}=5.0V±10%		600		μA	12
			V_{DD}=3.0V±10%		200			

Note 1: Applied to pins KH, KL, KI, P_3~P_0, Q_3~Q_0, $R0_3$~$R0_0$, $R1_3$~$R1_0$, $R2_3$~$R2_0$, $R3_3$~$R3_2$, KC_3~KC_0
Note 2: Applied to pins Z_{15}~Z_0, CL_1, OSC_{IN}/KT, ACL
Note 3: Applied to pins Q_3~Q_0, $R0_3$~$R0_0$, $R1_3$~$R1_0$, *$R2_3$~$R2_0$, *$R3_3$~$R3_0$, *Z_{15}~Z_0
Note 4: Applied to pin ACL
Note 5: Applied to pins Q_3~Q_0, $R0_3$~$R0_0$, $R1_3$~$R1_0$, $R2_3$~$R2_0$, $R3_3$~$R3_0$, Z_{15}~Z_0
(*If CMOS buffer is specified for mask option, Note 6 applies to these pins.)
Note 6: Applied to pins P_3~P_0, F, f_{OUT}
Note 7: Applied to pin CL_2
Note 8: No-load condition
Note 9: When the OSC_{IN}/KT pin is connected to GND and in no-load condition.
Note 10: When the timer clock crystal oscillation circuit and timer 1 are operating and in no-load condition.
Note 11: When the OSC_{IN}/KT pin is connected to GND and in no-load condition, f_s=100kHz
Note 12: When the OSC_{IN}/KT pin is connected to GND and in no-load condition, f_s=500kHz
Note 13: t_{ACL} is the ACL input pulse width required to cause ACL to operate when V_{DD} has completely risen.

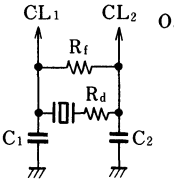


Note 14: tV_{DD} is the power supply rise time necessary for the built-in ACL to operate (ACL input pin is connected to GND).

■ Oscillation Circuit (values for reference)

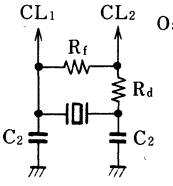
(a) System clock frequency generating circuit (example 1)

(1) 400kHz oscillation



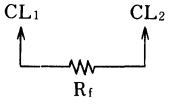
Oscillator KBR-400B : Made by Kyocera Corp.
$R_f = 1M\Omega$
$R_d = 560\Omega$
$C_1 = 330pF$
$C_2 = 330pF$

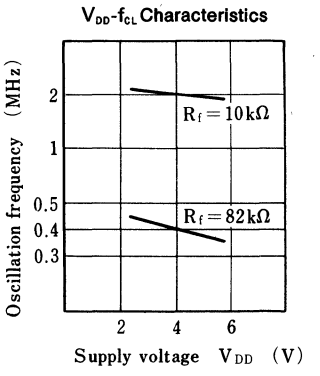
(2) 2 MHz oscillation

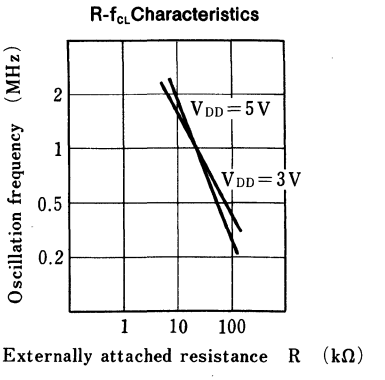


Oscillator KBR-2.0MS : Made by Kyocera Corp.
$R_f = 1M\Omega$
$R_d = 820\Omega$
$C_1 = 33pF$
$C_2 = 33pF$

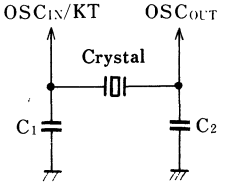
(b) System clock frequency generating circuit (example 2)





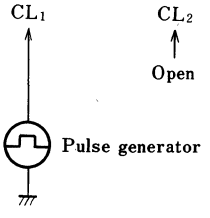


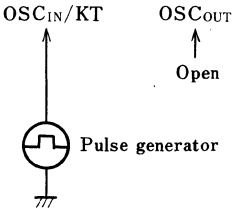
(c) Clock generating circuit for timer (example)



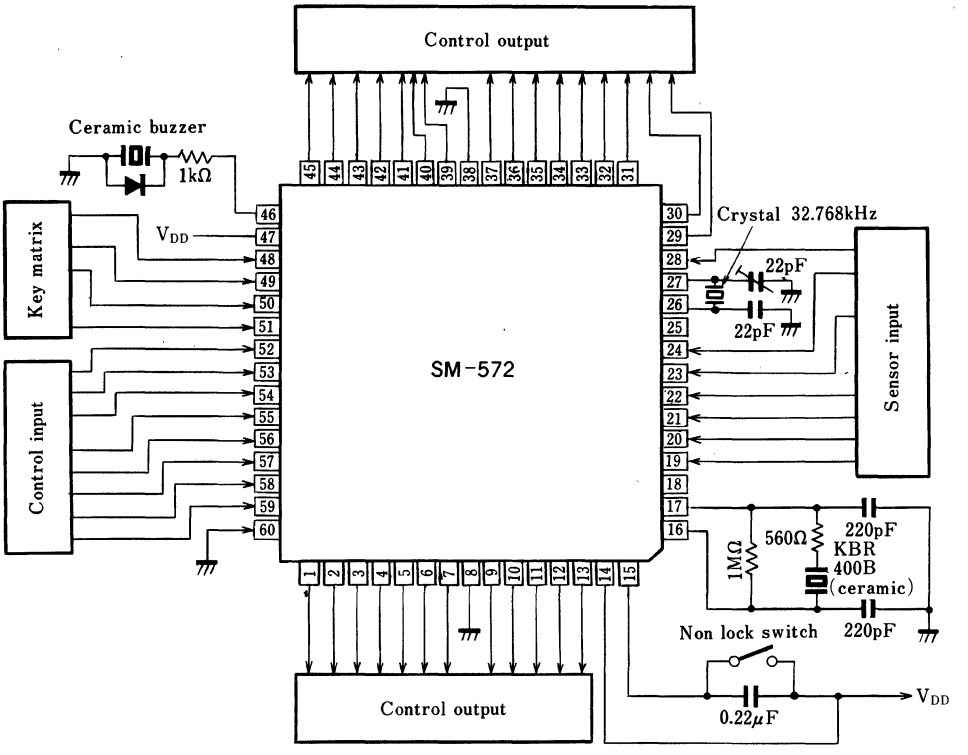
When $f_{OSC} = 32.768kHz$
$C_1 = 22pF$, $C_2 = 22pF$
Crystal : 32.768kHz

(d) External clock input circuit





System Configuration



SM-578 CMOS 4-Bit 1-Chip Microcomputer

■ Description

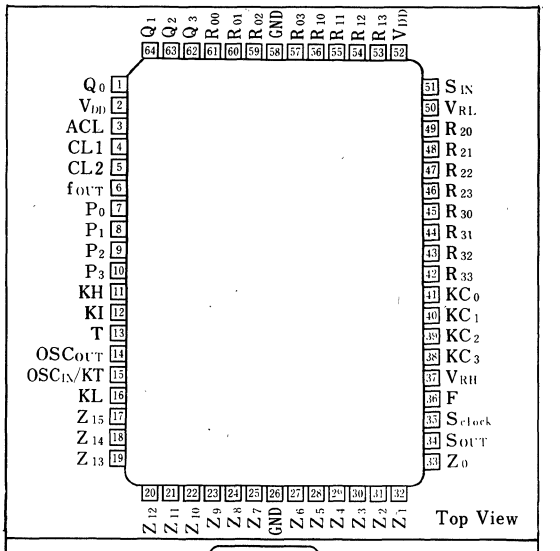
The SM-578 is a 4-bit single chip CMOS microcomputer with 4,064×9 bits of ROM, 192×4 bits of RAM, 8-bit A/D converter, timer/counter and 8-bit serial I/O.

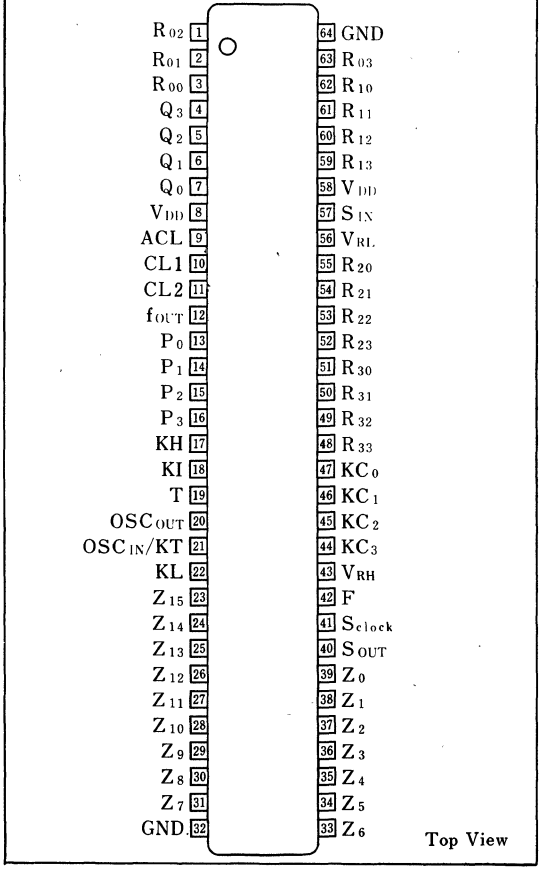
It is best suited for applications requiring A/D circuits.

■ Features

1. CMOS process
2. ROM capacity 4,069×9 bits
3. RAM capacity 192×4 bits
4. Instructions 93
5. Subroutine nesting 6 levels
6. Input ports 8 bits
7. Output ports 1 bit
8. Input/Output ports 40 bits
9. Timer/counter : 8-bit counters 2
10. Interrupt function
    External interrupts 2/Timer interrupts 2
11. A/D converter 8 bits
12. Single power supply (2.7～5.5V)
13. Instruction cycle 2 μs (MIN.)
14. 64-pin quad-flat package
    64-pin dual-in-line package

■ Pin Connections





SM-579 CMOS 4-Bit 1-Chip Microcomputer

■ Description

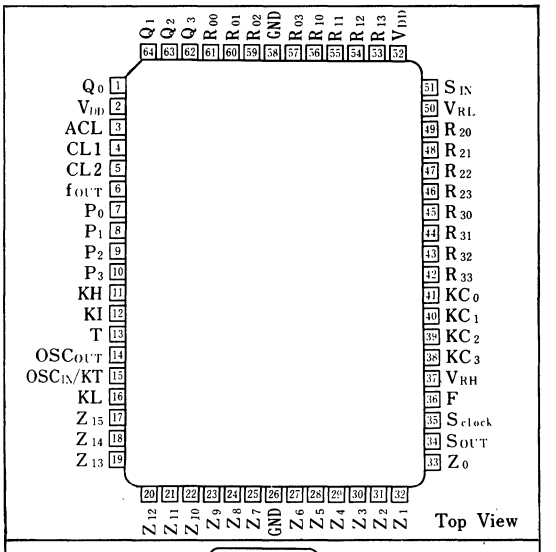
The SM-579 is a 4-bit single chip CMOS microcomputer with 6,094×9 bits of ROM, 256×4 bits of RAM, 8-bit A/D converter, timer/counter and 8-bit Serial I/O.

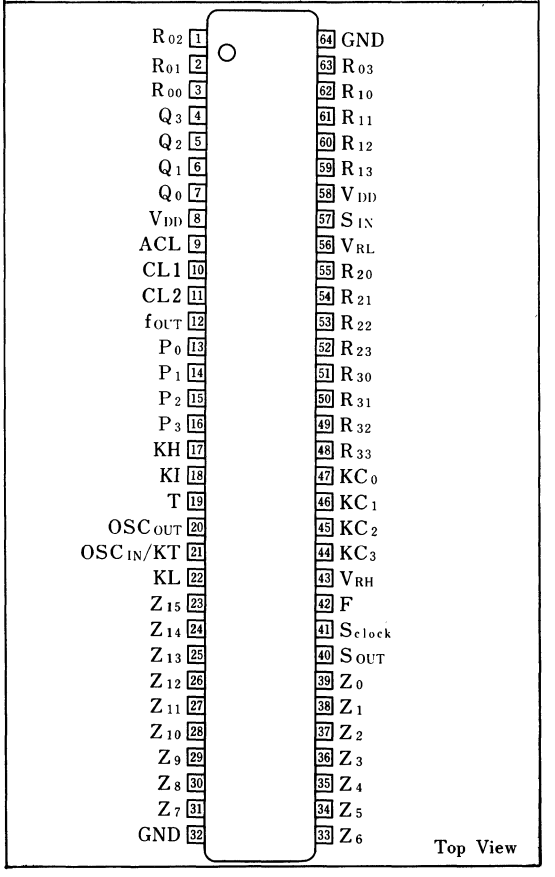
It is best suited for applications requiring A/D circuits.

■ Features

1. CMOS process
2. ROM capacity 6,096×9 bits
3. RAM capacity 256×4 bits
4. Instructions 93
5. Subroutine nesting 6 levels
6. Input ports 8 bits
7. Output ports 1 bit
8. Input/Output ports 40 bits
9. Timer/counter : 8-bit counters 2
10. Serial interface 8 bits
11. Interrupt function
    - External interrupts 2
    - Timer interrupts 2
12. A/D converter 8 bits
13. Single power supply (2.7～5.5V)
14. Instruction cycle 2 μs (MIN.)
15. 64-pin quad-flat package
    64-pin dual-in-line package

■ Pin Connections





SM-590 CMOS 4-Bit 1-Chip Microcomputer

■ Description

The SM-590 is a 4-bit single chip CMOS microcomputer with 508 bytes of ROM, 32×4 bits of RAM.

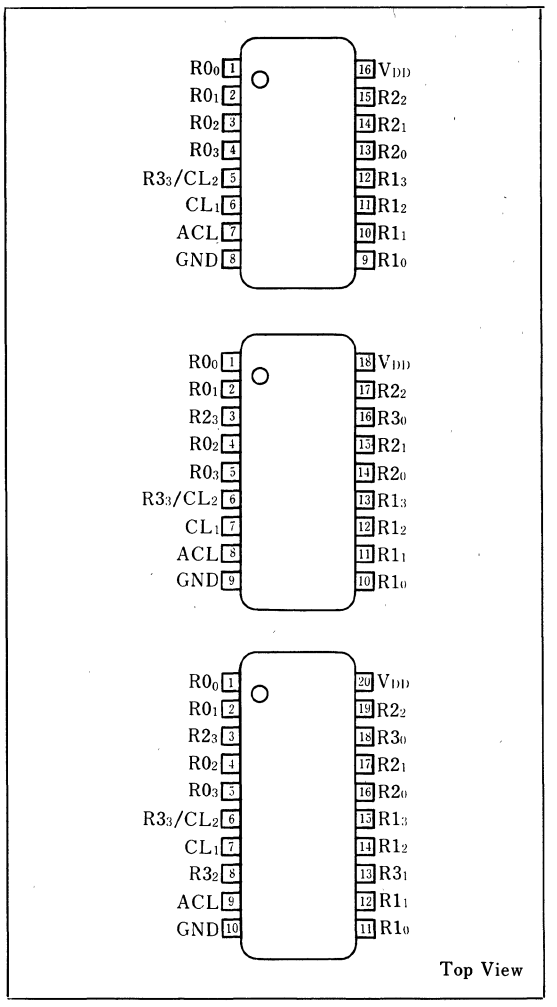
It is best suited for use in a compact controller, a system subcontroller and other various application systems.

■ Features

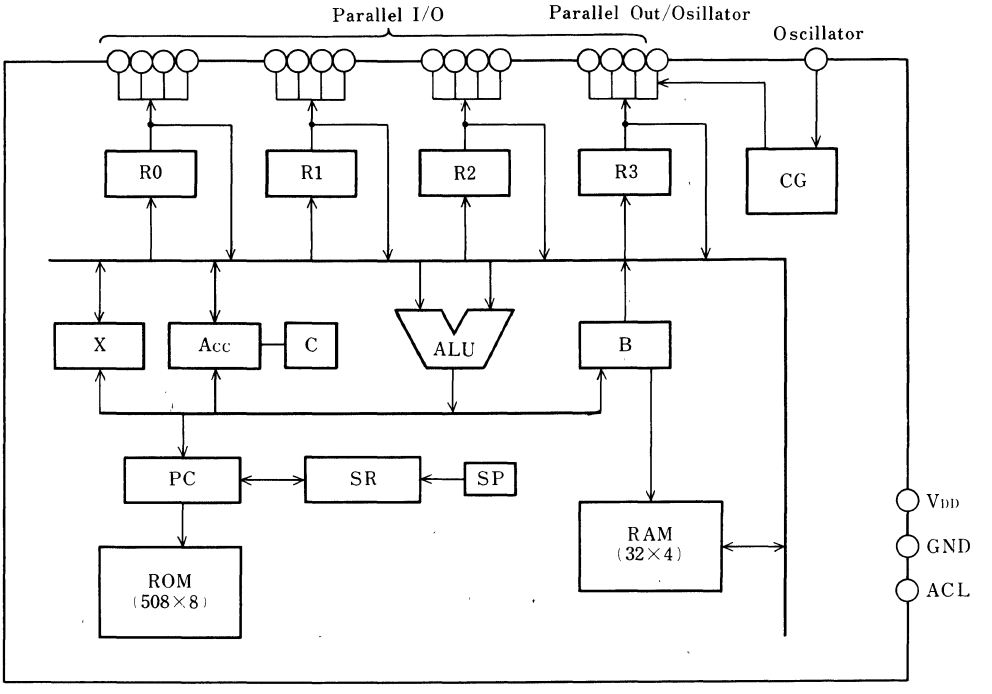
1. CMOS process
2. ROM capacity 508×8 bits
3. RAM capacity 32×4 bits
4. Instructions 41
5. Subroutine nesting 4 levels
6. Input/Output ports 15 bits(MAX.)
   Available for use as 10mA output port
   10 bits (MAX.) by mask option
   ($R0_0$~$R0_3$, $R1_0$~$R1_3$, $R3_1$, $R3_2$)
7. Standby mode
8. Single power supply (2.5~5.5V)
9. Instruction cycle 1 μs
10.

Package	I/O ports
16DIP	11bits
18DIP	13bits
20DIP	15bits

■ Pin Connections



Block Diagram



Symbol description

Acc	: Accumulators	PC	: Program counter
ALU	: Arithmetic logic unit	R0~R3	: Register
B	: RAM address register	SP	: Stack pointer
C	: Carry F F	SR	: Stack register
CG	: Clock generator	X	: Temporary register

Pin Description

Pin name	I/O	Circuit type	Function
$R0_0$~$R0_3$	I/O	Pull down*1	Acc ⟷ $R0_0$~$R0_3$, $R0_0$~$R0_3$ ← RAM
$R1_0$~$R1_3$	I/O	Pull down*1	Acc ⟷ $R1_0$~$R1_3$, $R1_0$~$R1_3$ ← RAM
$R2_0$~$R2_3$	I/O	Pull down/open drain*2	Acc ⟷ $R2_0$~$R2_3$, $R2_0$~$R2_3$ ← RAM
$R3_0$~$R3_3$	I/O	Pull down*1	Acc ⟷ $R3_0$~$R3_3$, $R3_0$~$R3_3$ ← RAM
ACL	I	Pull down	Auto clear
CL_1, CL_2			For system clock oscillation
V_{DD}, GND			Power supply for logic circuit

*1 Mask option ; Open drain I/O or CMOS output selectable
*2 Mask option

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3～+7.5	V
Input voltage	V_I	−0.3～V_{DD}+0.3	V
Output voltage	V_O	−0.3～V_{DD}+0.3	V
Source output current sum	ΣI_{OH}	120	mA
Sync output current sum	ΣI_{OL}	20	mA
Operating temperature	T_{opr}	−10～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

■ Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.5		5.5	V
Command execution time	t_{SYS}	3V±0.5V	4		50	μs
		5V±0.5V	1		50	

■ Clock Input Signal AC Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock rise time	t_r	V_{DD}=2.5～5.5V			50	ns
Clock fall time	t_f	V_{DD}=2.5～5.5V			50	
Clock pulse width	t_L	V_{DD}=5V±0.5V	0.08		6.3	μs
	t_H	V_{DD}=3V±0.5V	0.45		6.3	

Note: When external clock is input

■ Electrical Characteristics

(V_{DD}=2.7V～5.5V, Ta=−10℃～+70℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}			0.7V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.3V_{DD}	V	
	V_{IH2}			V_{DD}−0.5		V_{DD}	V	2
	V_{IL2}			0		0.5	V	
	V_{IL3}	V_{DD}=5V±10%		0.7	1.4	2.1	V	3
	ΔV_I	V_{DD}=5V±10%		1.1	2	3.1	V	
Input current	I_{IH1}	V_{IN}=V_{DD}	V_{DD}=3V±10%	15	70	200	μA	1
			V_{DD}=5V±10%	70	250	750		
	I_{IH2}	V_{IN}=V_{DD}	V_{DD}=3V±10%		7	20	μA	4
			V_{DD}=5V±10%		20	60		
Current consumption	I_{A1}	t_{SYS}=2 μs	V_{DD}=5V±10%		1	3	mA	5
	I_{A2}	t_{SYS}=10 μs	V_{DD}=3V±10%		100	200	μA	
			V_{DD}=5V±10%		200	500		
	I_{ST}	Standby mode			1	2	μA	

Output current (Ta=−10℃ ~ +70℃)

I_O (MIN.)	I_{OH} (mA)		I_{OL} (mA)		I_{OL} (μA)		Note
Condition / Pin	V_{DD}=5V±10%	V_{DD}=3V±10%	V_{OL}=0.4V		V_{OL}=0.4V		
	V_{OH}=V_{DD}−2V	V_{OH}=V_{DD}−0.5V	V_{DD}=5V±10%	※	V_{DD}=5V±10%	※	
$R0_0$	10	1	1.6	0.8	15	8	
$R0_1$	10	1	1.6	0.8	15	8	
$R0_2$	10	1	1.6	0.8	15	8	
$R0_3$	10	1	1.6	0.8	15	8	
$R1_0$	10	1	1.6	0.8	15	8	
$R1_1$	10	1	1.6	0.8	15	8	
$R1_2$	10	1	1.6	0.8	15	8	
$R1_3$	10	1	1.6	0.8	15	8	
$R2_0$	4	0.5			15	8	
$R2_1$	4	0.5			15	8	
$R2_2$	4	0.5			15	8	
$R2_3$	4	0.5			15	8	
$R3_0$	4	0.5	1.6	0.8	15	8	
$R3_1$	10	1	1.6	0.8	15	8	
$R3_2$	10	1	1.6	0.8	15	8	6
	3	0.4					7
$CL_2/R3_3$	1	0.15	0.6	0.3			
Mask option switch number			2		1		

Note 1: Applied to pin $R0_0$, $R0_1$, $R0_2$, $R0_3$, $R1_0$, $R1_1$, $R1_2$, $R1_3$, $R2_0$, $R2_1$, $R2_2$, $R2_3$, $R3_0$, $R3_1$, $R3_2$
Note 2: Applied to pins ACL, CL_1
Note 3: Applied to pin $R2_2$ (when standby cancel signal is input)
$\Delta V_I = V_{IH3} - V_{IL3}$ (See the SM590 programming manual for details)
Note 4: Applied to pin ACL
Note 5: No-load condition
Note 6: When the contents of the R latch is output to the $R3_2$ pin.
Note 7: When the clock input to the CL_1 pin is output from the $R3_2$ pin.
※: V_{DD}=3V±10%

SM-591 CMOS 4-Bit 1-Chip Microcomputer

■ Description

The SM-591 is a 4-bit single chip CMOS microcomputer with 1,016 bytes of ROM, 56×4 bits of RAM.

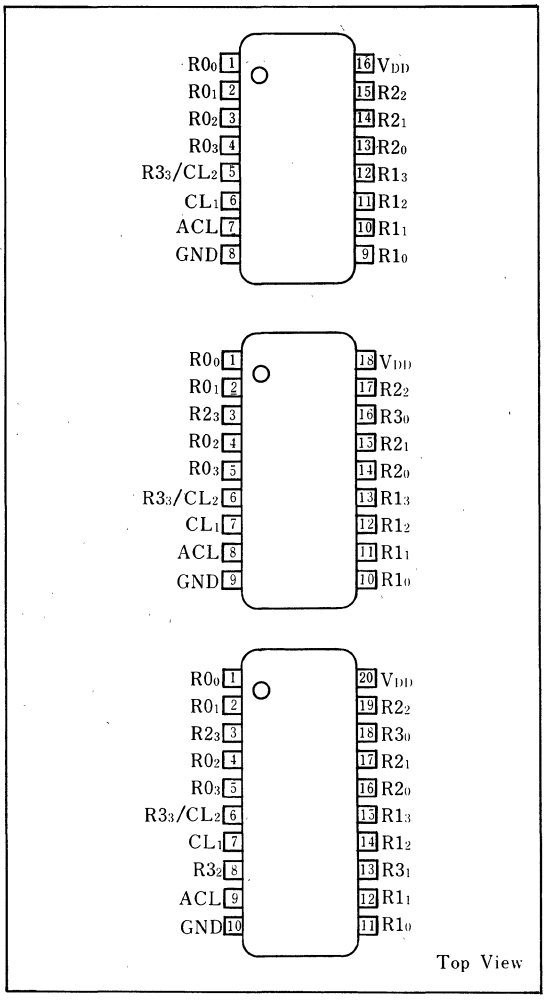
It is best suited for use in a compact controller, a system subcontroller and other various application systems.

■ Features

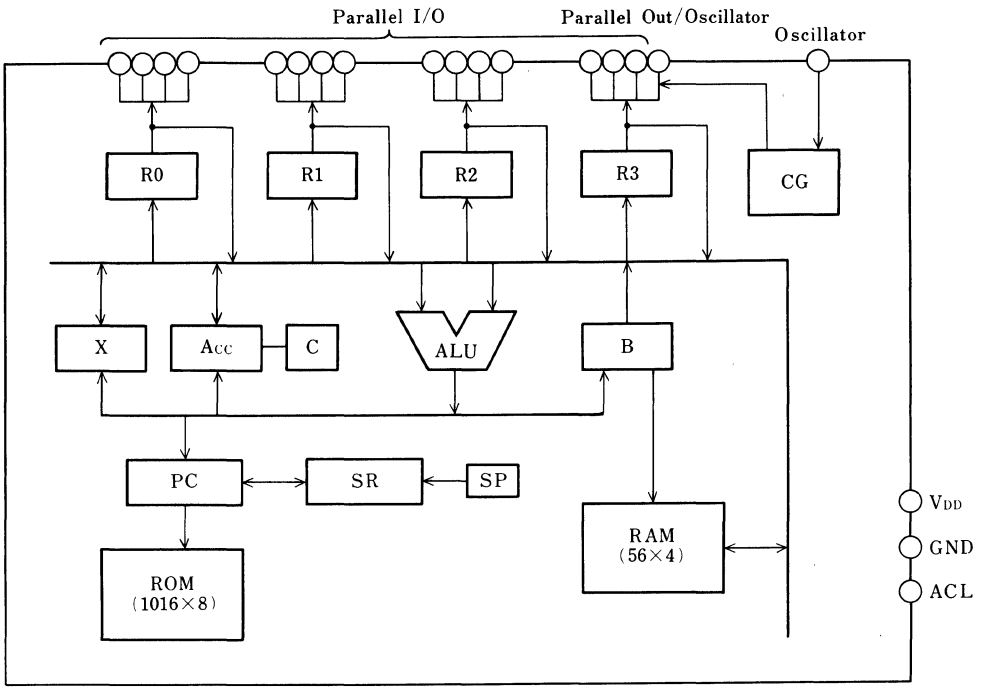
1. CMOS process
2. ROM capacity 1,016×8 bits
3. RAM capacity 56×4 bits
4. Instructions 41
5. Subroutine nesting 4 levels
6. Input/Output ports 15 bits (MAX.)
   Available for use as 10mA output port 10 bits (MAX.) by mask option
   ($R0_0$~$R0_3$, $R1_0$~$R1_3$, $R3_1$, $R3_2$)
7. Standby mode
8. Single power supply (2.5~5.5V)
9. Instruction cycle 1 μs
10.

Package	I/O ports
16DIP	11bits
18DIP	13bits
20DIP	15bits

■ Pin Connections



■ Block Diagram



Symbol description

Acc	: Accumulators	PC	: Program counter
ALU	: Arithmetic logic unit	R0~R3	: Register
B	: RAM address register	SP	: Stack pointer
C	: Carry F/F	SR	: Stack register
CG	: Clock generator	X	: Temporary register

■ Pin Description

Pin name	I/O	Circuit type	Function
$R0_0$~$R0_3$	I/O	Pull down*1	Acc ⟷ $R0_0$~$R0_3$, $R0_0$~$R0_3$ ← RAM
$R1_0$~$R1_3$	I/O	Pull down*1	Acc ⟷ $R1_0$~$R1_3$, $R1_0$~$R1_3$ ← RAM
$R2_0$~$R2_3$	I/O	Pull down/open drain*2	Acc ⟷ $R2_0$~$R2_3$, $R2_0$~$R2_3$ ← RAM
$R3_0$~$R3_3$	I/O	Pull down*1	Acc ⟷ $R3_0$~$R3_3$, $R3_0$~$R3_3$ ← RAM
ACL	I	Pull down	Auto clear
CL_1, CL_2			For system clock oscillation
V_{DD}, GND			Power supply for logic circuit

*1 Mask option ; Open drain I/O or CMOS output selectable
*2 Mask option

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3～+7.5	V
Input voltage	V_I	−0.3～V_{DD}+0.3	V
Output voltage	V_O	−0.3～V_{DD}+0.3	V
Source output current sum	ΣI_{OH}	120	mA
Sync output current sum	ΣI_{OL}	20	mA
Operating temperature	T_{opr}	−10～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

■ Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.5		5.5	V
Command execution time	T_{SYS}	3V±0.5V	4		50	μs
		5V±0.5V	1		50	

■ Clock Input Signal AC Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock rise time	t_r	V_{DD}=2.5～5.5V			50	ns
Clock fall time	t_f	V_{DD}=2.5～5.5V			50	
Clock pulse width	t_L	V_{DD}=5V±0.5V	0.08		6.3	μs
	t_H	V_{DD}=3V±0.5V	0.45		6.3	

Note: When external clock is input

■ Electrical Characteristics

(V_{DD}=2.7V～5.5V, Ta=−10℃～+70℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}			0.7V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.3V_{DD}	V	
	V_{IH2}			V_{DD}−0.5		V_{DD}	V	2
	V_{IL2}			0		0.5	V	
	V_{IL3}	V_{DD}=5V±10%		0.7	1.4	2.1	V	3
	ΔV_I	V_{DD}=5V±10%		1.1	2	3.1	V	
Input current	I_{IH1}	V_{IN}=V_{DD}	V_{DD}=3V±10%	15	70	200	μA	1
			V_{DD}=5V±10%	70	250	750		
	I_{IH2}	V_{IN}=V_{DD}	V_{DD}=3V±10%		7	20	μA	4
			V_{DD}=5V±10%		20	60		
Current consumption	I_{A1}	t_{SYS}=2 μs	V_{DD}=5V±10%		1	3	mA	5
	I_{A2}	t_{SYS}=10 μA	V_{DD}=3V±10%		100	200	μA	
			V_{DD}=5V±10%		200	500		
	I_{ST}	Standby mode			1	2	μA	

Output current (Ta=−10℃～+70℃)

I_O (MIN.)	I_{OH} (mA)		I_{OL} (mA)		I_{OL} (μA)		Note
Condition / Pin	$V_{DD}=5V\pm10\%$ $V_{OH}=V_{DD}-2V$	$V_{DD}=3V\pm10\%$ $V_{OH}=V_{DD}-0.5V$	$V_{OL}=0.4V$ $V_{DD}=5V\pm10\%$	※	$V_{OL}=0.4V$ $V_{DD}=5V\pm10\%$	※	
$R0_0$	10	1	1.6	0.8	15	8	
$R0_1$	10	1	1.6	0.8	15	8	
$R0_2$	10	1	1.6	0.8	15	8	
$R0_3$	10	1	1.6	0.8	15	8	
$R1_0$	10	1	1.6	0.8	15	8	
$R1_1$	10	1	1.6	0.8	15	8	
$R1_2$	10	1	1.6	0.8	15	8	
$R1_3$	10	1	1.6	0.8	15	8	
$R2_0$	4	0.5			15	8	
$R2_1$	4	0.5			15	8	
$R2_2$	4	0.5			15	8	
$R2_3$	4	0.5			15	8	
$R3_0$	4	0.5	1.6	0.8	15	8	
$R3_1$	10	1	1.6	0.8	15	8	
$R3_2$	10	1	1.6	0.8	15	8	6
	3	0.4		0.8			7
$CL_2/R3_3$	1	0.15	0.6	0.3			
Mask option switch number			2		1		

Note 1: Applied to pins $R0_0$, $R0_1$, $R0_2$, $R0_3$, $R1_0$, $R1_1$, $R1_2$, $R1_3$, $R2_0$, $R2_1$, $R2_2$, $R2_3$, $R3_0$, $R3_1$, $R3_2$
Note 2: Applied to pins ACL, CL_1
Note 3: Applied to pins $R2_2$ (when standby cancel signal is input)
$\Delta V_I=V_{IH3}-V_{IL3}$ (see the SH591 programming manual for details)
Note 4: Applied to pin ACL
Note 5: No-load condition
Note 6: When the contents of the R latch is output to the $R3_2$ pin.
Note 7: When the clock input to the CL_1 pin is output from the $R3_2$ pin.

※: $V_{DD}=3V\pm10\%$

Development guide for 4-Bit 1-Chip Microcomputers (SM Series)

(1) Description

To facilitate efficient product development using Sharp's SM series 4-bit, 1-chip microcomputers, we have established a general development procedure covering determination of specifications to actual delivery of the microcomputer as shown below.

(2) Development Procedure

① Determination of specifications

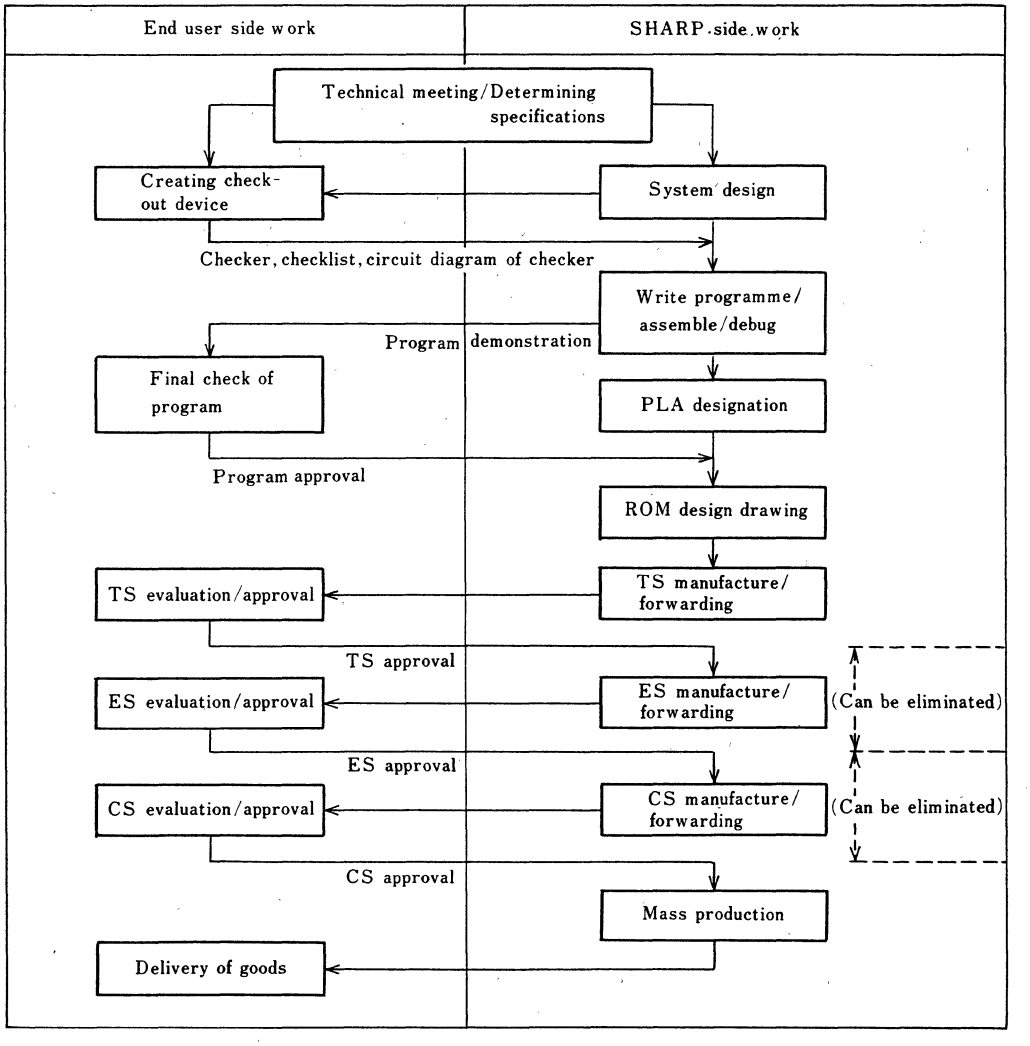
Specifications for a product you intend to develop must be determined in such a way that the functions required of the microcomputer are clear. Specifications should be prepared by the user, but consultation on SM series microcomputers will be provided on request. In addition, a programming manual is available for each microcomputer.

② Determining the microcomputer to be used

Select a microcomputer most suitable for the product. After determining the model of microcomputer, we will work out a rough development schedule in consultation with the user.

③ System design

Detailed specifications for the operation of the



microcomputer and its peripheral circuitry are determined of this stage. We recommend that the user confer with Sharp's staff even if the user himself under takes program development.

If Sharp is to carry out program development, the user must prepare the specifications first. After consultation with Sharp, the user determines the final specifications. The subsequent schedule will then be settled after consultation with the user.

④ Writing the program

A flow chart is worked out and based on it, machine code is written. The mnemonic codes used for coding are covered in the programming manual or cross-assembler manual. After coding, a source file is prepared using a computer editor. Sharp's microcomputer development tools, the SM-D-8000II or SM-D-80 system can be used for this purpose. A microcomputer development system running under the CP/M (Digital Research Inc.) operating system can also be used. For the preparation of source file, refer to the respective development systems' manuals (SM-D-8000II User's Manual, for example).

⑤ Assembler

The object file is created from the source file using the cross-assembler prepared for the development system.

There are a number of cross-assemblers available to meet the requirements of respective SM series products. Please, contact us for details.

⑥ Debugging and program revision

After the object file has been created, the program must be debugged by operating the EVA board or CPU unit while using the checker to monitor program operation. If the program is not running properly, it must be revised and re-assembled until a satisfactory object file is prepared. A number of development tools are available to perform this task efficiently.

⑦ Final confirmation of program operation

The final confirmation of the program is included in the debugging work described in (2) ⑥ if program development was made by the user.

If Sharp undertook program development, three copies of programming specifications are usually presented to the user for final confirmation of program operation one week before the ROM is submitted. If no problem is found in the programming specifications, a copy of programming specifications shall be sent back to us bearing a signature of approval.

In the event that probelms are discovered in the program at this time, the program will be revised after consultating with the user.

⑧ PLA (Programmable Logic Array) assignments

If the program is developed by the user, the user prepares the PLA assignments diagram which should be submitted to Sharp about two weeks before the date on which the ROM is scheduled to be submitted. The procedure for PLA assignment is covered in the programming manual. Pre-printed PLA assignment forms will be provided to the user on request.

When the program is developed by Sharp, we will make the PLA assignments.

⑨ ROM submission

If the program is developed by the user, the ROM must be submitted in the form of either an EPROM or diskettes. Along with the ROM , the ROM map should also be submitted to make sure that the correct data can be read from the ROM.

Whoever develops the program, it is impossible to change the program after the ROM is submitted. The final confirmation of program operation must be extremely thorough.

⑩ TS (Technical Sample)

The TS is submitted to the user in a ceramic package for performance evaluation as a trial model. If no problems are found, the user shall issue a statement of performance approval. Note that the TS package is a ceramic type and differs from that which will be mass produced.

⑪ ES (Engineering Sample)

After approval of the TS, the ES is prepared and submitted to the user. The ES is normally contained in a plastic package the same shape as that which will be mass produced.

After evaluating the performance of the ES, the user shall issue performance approval, assuming no problems are encountered. The ES may be skipped if desired.

⑫ CS (Commercial Sample)

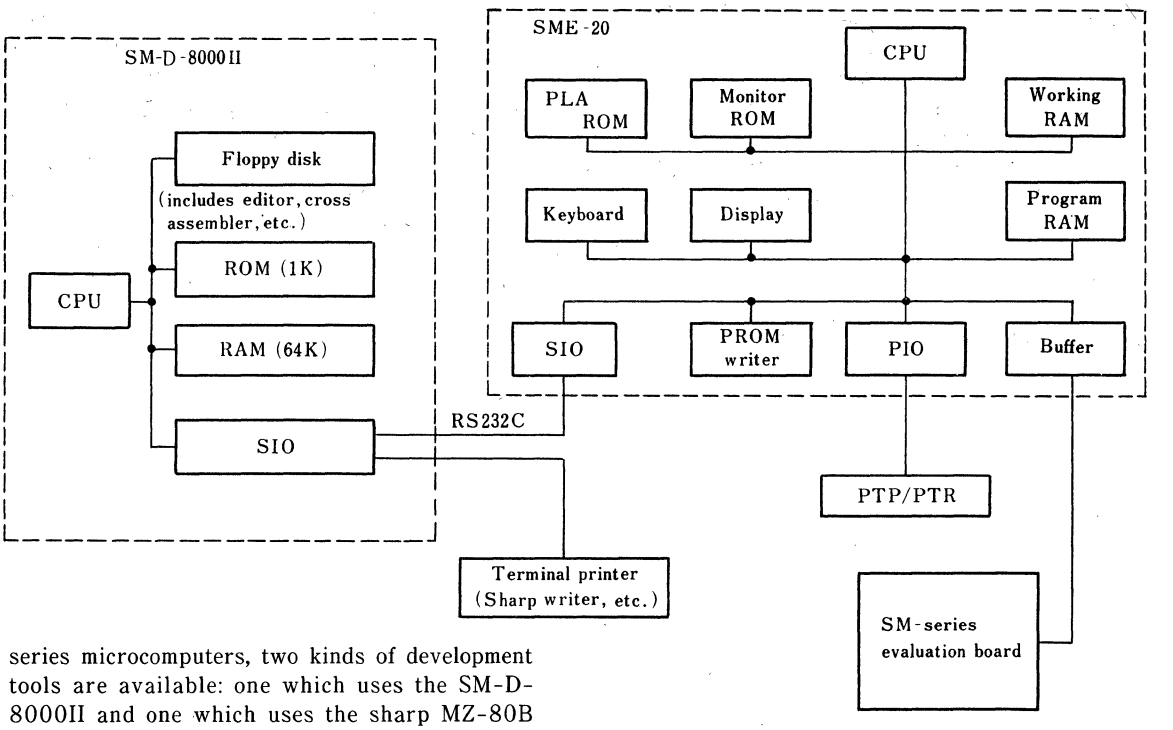
After approval of the ES, the CS is prepared and submitted to the user. The CS is the mass-production trial model so it is made in the same shape and quality as that which will be mass produced. After evaluating the performance of the CS, the user shall issue performance approval, assuming no problems are encountered. The CS may be skipped if desired.

⑬ Mass production

After approval of the CS, mass production is initiated. If the ES and/or CS is omitted, the user shall advise us when to start mass production.

(3) Development Tools

To facilitate program development for SM



series microcomputers, two kinds of development tools are available: one which uses the SM-D-8000II and one which uses the sharp MZ-80B computer.

Development tools equipped with an RS232C interface running under the CP/M OS can also be used.

① SM-D-8000II system

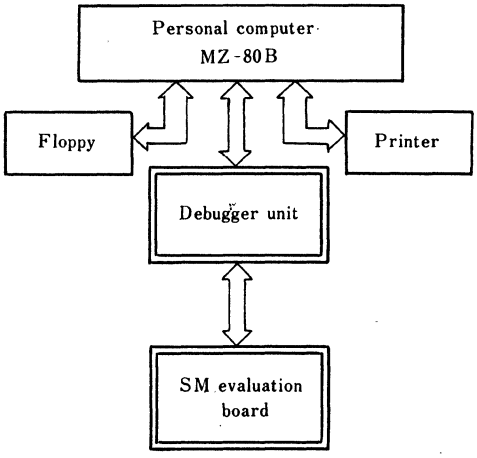
This emulator consists of the keyboard, display LED, PROM writer, and interfaces. Although it is possible for the SME-20 to debug the program by connecting the CPU unit or EVA board, more efficient debugging can be achieved by transferring the object file through the SM-D-8000II and RS232C interface.

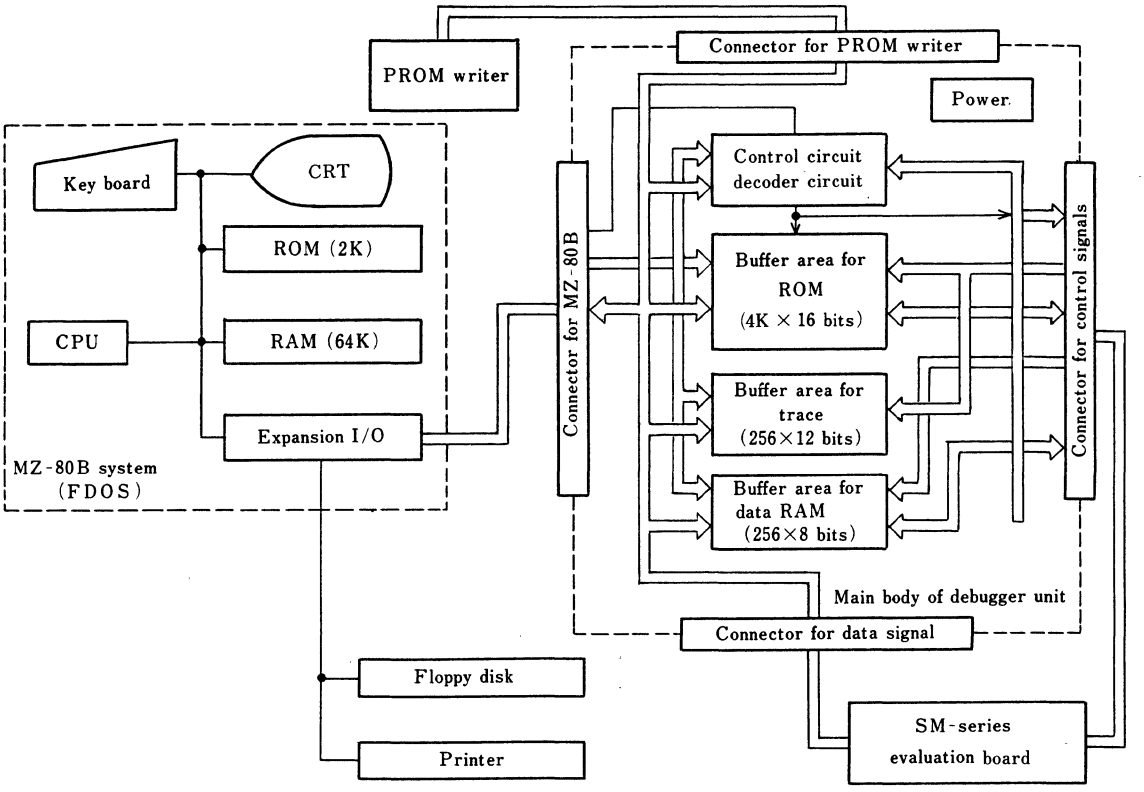
For details, see the SM software package manual and instruction manuals of the SM series, SM-D-8000II and SME-20.

The SME-20 can be connected not only to the SM-D-8000II, but to any development device equipment with an RS232C interface.

② SM-D-80 system

The SM series development system can be configured by connecting the debugger unit and SM evalution board to the basic FDOS system (MZ-80B, floppydisk, printer) of the commercial personal computer MZ-80B. Various utility programs such as a cross-assembler, debugger and editor which operate under the control of the FDOS are provided as standard equipment to facilitate efficient program debugging.




PROM writer
Connector for PROM writer
Power
Key board
CRT
ROM (2K)
CPU
RAM (64K)
Expansion I/O
MZ-80B system
(FDOS)
Connector for MZ-80B
Control circuit
decoder circuit
Buffer area for
ROM
(4K × 16 bits)
Buffer area for
trace
(256×12 bits)
Buffer area for
data RAM
(256×8 bits)
Connector for control signals
Main body of debugger unit
Connector for data signal
Floppy disk
Printer
SM-series
evaluation board

8-Bit 1-Chip Microcomputers

LH0801 Z8-01 Microcomputer Unit

Description

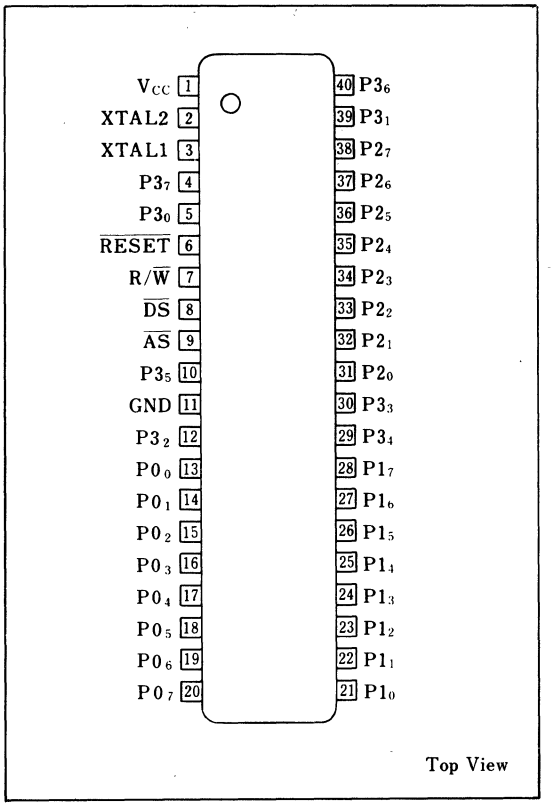
Compared to earlier single-chip microcomputers, the Z8 offers faster execution ; more efficient use of memory, more sophisticated interrupt, input/output and bit-manipulation capabilities ; and easier system expansion.

Under program control, the Z8 can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 2K bytes of internal ROM, a traditional microprocessor that manages up to124K bytes of external memory,or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-BUS. In all configurations, a large number of pins remain available for I/O.

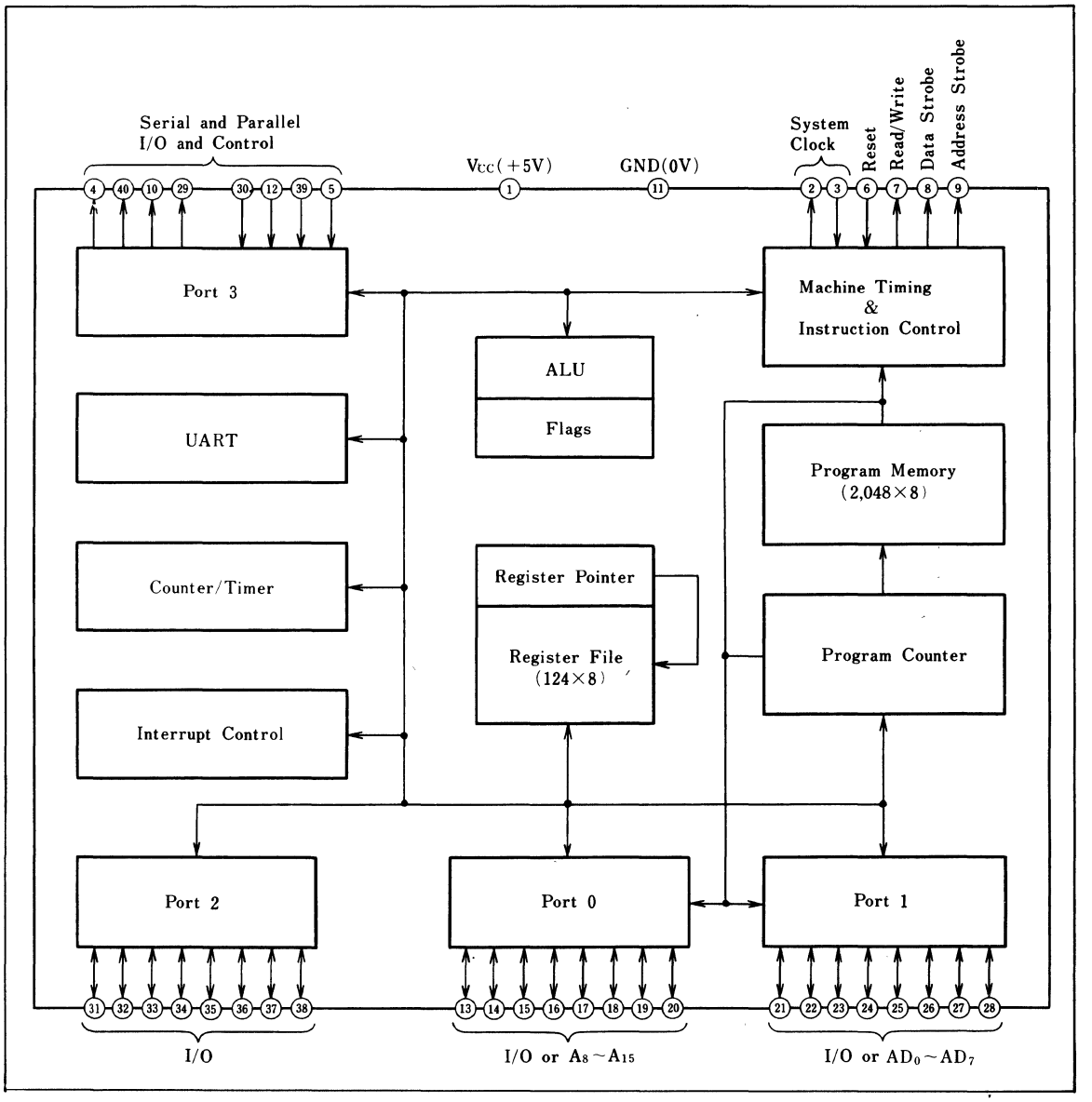
Features

1. Complete single-chip microcomputer with internal ROM, RAM and I/O
   - RAM 124 bytes
   - ROM 2K bytes
   - I/O 32 lines
2. On-chip two programmable 8-bit counter/timers, each with a 6-bit programmble prescaler
3. Full-duplex UART
4. 144-byte register file
5. Register pointer so that short, fast instructions can access any working register groups
6. Vectored, priority interrupts for I/O, counter/timers, and UART
7. Up to 62K bytes addressable external space each for program and data memory
8. On-chip oscillator
9. High speed instruction execution
   - Working register operating time : 1.5 μs
   - Average instruction execution time : 2.2 μs
   - Maximum instruction execution time : 5.0 μs
10. Low-power standby option which retains contents of general-purpose registers
11. Single + 5V power supply
12. All pins are TTL compatible

Pin Connections



Block Diagram



■ Pin Description

Pin	Meaning	I/O	Function
$P0_0$~$P0_7$	Port 0	I/O	8-bit I/O port, programmable for I/O.
Pl_0~Pl_7	Port 1	I/O	Programmable for I/O in btyes.
$P2_0$~$P2_7$	Port 2	I/O	Programmable for I/O in bits.
$P3_0$~$P3_7$	Port 3	I/O	$P3_0$-$P3_3$ for input, $P3_4$-$P3_7$ for output.
$\overline{AS}$	Address Strobe	O	Active "Low", activated for external address memory transfer.
$\overline{DS}$	Data Strobe	O	Active "Low", activated for external data memory transfer.
R/$\overline{W}$	Read/Write	O	Read at "High", Write at "Low".
$\overline{RESET}$	Reset	I	Active "Low". Initializes.
XTAL1	Clock 1	I	Clock terminal pin.
XTAL2	Clock 2	O	Clock terminal pin.

■ Absolute Maximum Ratings

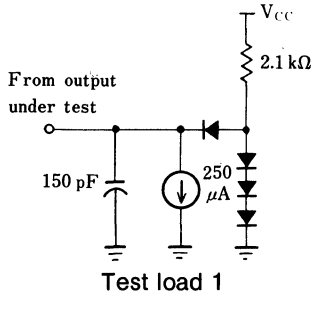
Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3~+7	V
Output voltage	V_{OUT}	−0.3~+7	V
Operating temperature	T_{opr}	0~+70	℃
Storage temperature	T_{stg}	−65~+150	℃

■ DC Characteristics

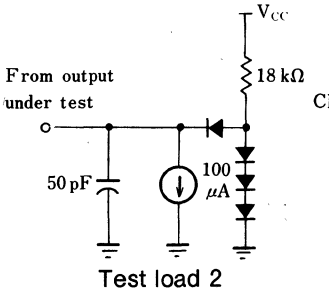
(V_{CC}=5V±5%, Ta=0~+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock input high voltage	V_{CH}	Driven by external clock oscillator	3.8		V_{CC}	V	
Clock input low voltage	V_{CL}	Driven by external clock oscillator	−0.3		0.8	V	
Input high voltage	V_{IH}		2.0		V_{CC}	V	
Input low voltage	V_{IL}		−0.3		0.8	V	
Reset input high voltage	V_{RH}		3.8		V_{CC}	V	
Reset input low voltage	V_{RL}		−0.3		0.8	V	
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4			V	1
Output low voltage	V_{OL}	I_{OL}=+2.0mA			0.4	V	1
Input leakage current	I_{IL}	0V≦V_{IN}≦+5.25V	−10		10	μA	
Output leakage current	I_{OL}	0V≦V_{IN}≦+5.25V	−10		10	μA	
Reset input current	I_{IR}	V_{CC}=5.25V, V_{RL}=0V			−50	μA	
Supply current	I_{CC}				180	mA	
Supply current	I_{MM}				10	mA	

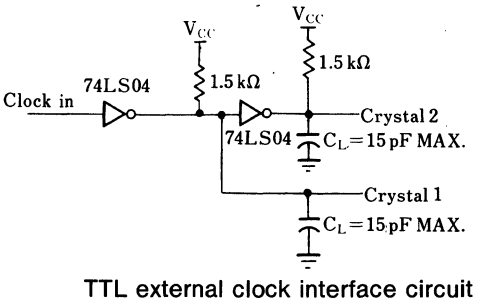
Note 1: I_{OH}=−100 μA and I_{OL}=1.0mA as to A0-A11, $\overline{MDS}$, $\overline{SYNC}$, SCLK and IACK in LH0802.



Test load 1



Test load 2



TTL external clock interface circuit

■ External I/O or Memory Read/Write

(V_{CC}=5V±5%, Ta=0～+70℃)

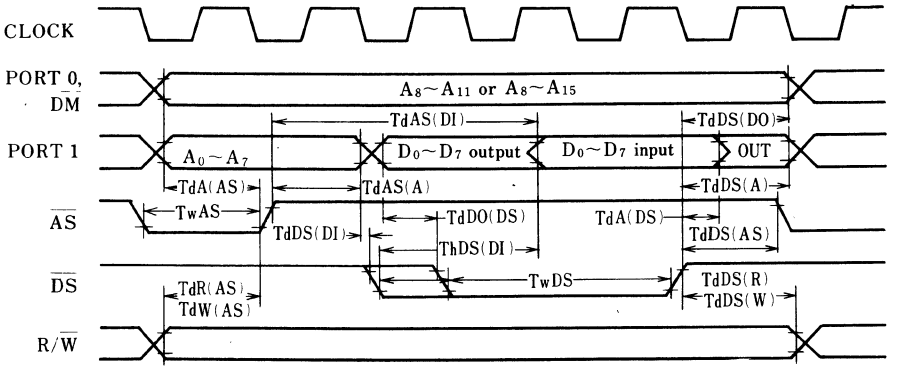
Symbol	Parameter		Conditions	MIN.	MAX.	Unit	Note
TdA (AS)	Address valid to $\overline{AS}$ ↑ delay		Test load 1	50		ns	2
TdAS (A)	$\overline{AS}$ ↑ to address float delay		Test load 1	70		ns	2
TdAS (DI)	$\overline{AS}$ ↑ to input data required valid delay		Test load 1		360	ns	4
TwAS	$\overline{AS}$ ↑ low width		Test load 1	80		ns	2
TdA (DS)	Address float to $\overline{DS}$ ↓ delay		Test load 1	0		ns	
TwDS	$\overline{DS}$ low width	Read	Test load 1	250		ns	3
		Write	Test load 1	160			3
TdDS (DI)	$\overline{DS}$ ↓ to input data required valid		Test load 1		200	ns	4
ThDS (DI)	Input data hold time			0		ns	
TdDS (A)	$\overline{DS}$ ↑ to address active delay		Test load 1	80		ns	2
TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay		Test load 1	70		ns	2
TdR (AS)	Read valid to $\overline{AS}$ ↑ delay		Test load 1	50		ns	2
TdDS (R)	DS ↑ to read not valid		Test load 1	60		ns	2
TdDO (DS)	Output data valid to $\overline{DS}$ ↓ delay		Test load 1	50		ns	2
TdDS (DO)	$\overline{DS}$ ↑ to output data not valid delay		Test load 1	80		ns	2
TdW (AS)	Write valid to $\overline{AS}$ ↑ delay		Test load 1	50		ns	2
TdDS (W)	$\overline{DS}$ to write not valid delay		Test load 1	60		ns	2

Note 1: All timing references use 2.0 V for a logic "1" and 0.8 V for a logic "0".

Note 2: Delay times are for an input clock frequency of 8 MHz. If below this frequency, add the incremental clock period to the standard delay time.

Note 3: $\overline{DS}$ lower width is for an input clock frequency of 8 MHz. If below this frequency, add 3 increments of clock period to the standard. The width varies with execution command.

Note 4: These delay times show system memory access time with an 8-MHz QC unit. If below this frequency, add 4 increments of clock period for TdAS (DI) or 3 increments of clock period for TdDS (DI).

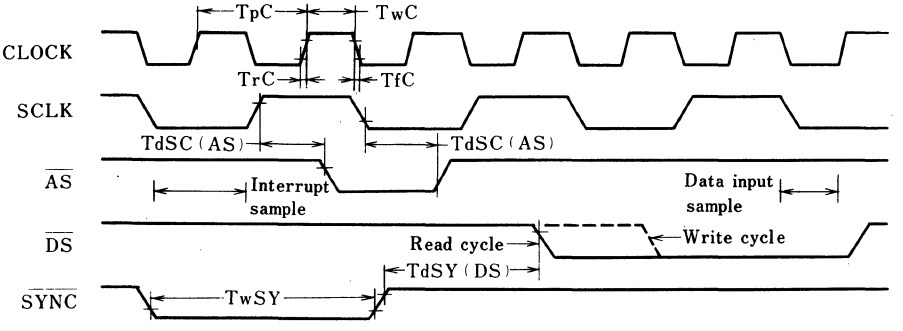


■ Additional Timing Table

(V_{CC}=5V±5%, Ta=0~+70℃)

Symbol	Parameter	Conditions	MIN.	MAX.	Unit	Note
TpC	Input clock period		125	1,000	ns	
TrC, TfC	Clock input rise and fall times	Driven by external clock oscillator		25	ns	
TwC	Input clock width	Driven by external clock oscillator	37		ns	
TdSC (AS)	System clock input to $\overline{AS}$ delay				ns	5
TdSY (DS)	Command sync output to DS delay		200		ns	5, 6
TwSY	Command sync output pulse width		160		ns	5, 6

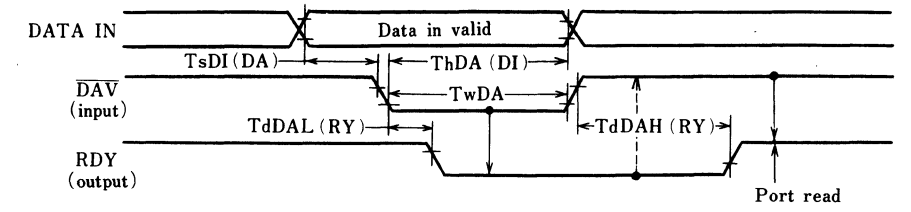
Note : All timing references use 2.0 V for a logic "1" and 0.8 V for a logic "0".
Note 5: Test load 1 is used when SCLK and $\overline{SYNC}$ are outputt via port 3, and test load 2 when SCLK and $\overline{SYNC}$ are direct-output with 64-pin version.
Note 6: With an 8 MHz QC unit. If below this frequency, add 2 increments of clock period.



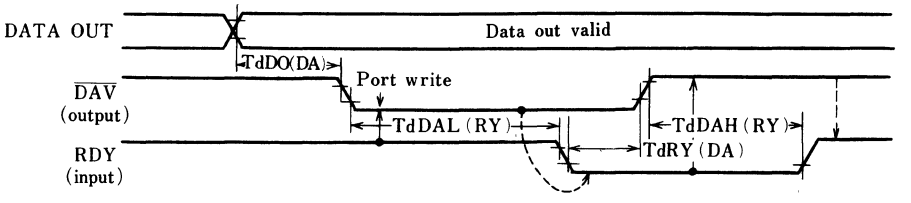
■ Handshake Timing

(V_{CC}=5V±5%, Ta=0~+70℃)

Symbol	Parameter	Conditions	MIN.	MAX.	Unit	Note
TsDI (DA)	Data in setup time		0		ns	
ThDA (DI)	Data in hold time		230		ns	
TwDA	Data available width	Input handshake Test load 1	175		ns	
TdDAL (RY)	$\overline{DAV}$↓ to RDY↓ delay	Input handshake Test load 1	20	175	ns	
		Output handshake Test load 1	0		ns	
TdDAH (RY)	$\overline{DAV}$↑ to RDY↑ delay	Input handshake Test load 1		150	ns	
		Output handshake Test load 1	0		ns	
TdDO (DA)	Data out to $\overline{DAV}$ ↓ delay	Test load 1	50		ns	
TdRY (DA)	RDY to $\overline{DAV}$ ↑ delay	Test load 1	0	205	ns	



Input handshake



Output handshake

■ Architecture

(1) Address Spaces

(i) **Program Memory** The 16-bit program counter addresses 64K bytes of program memory space. Program memory can be located in two areas : one internal and the other external (Fig. 1). The first 2048 bytes consist of on-chip mask-programmed ROM. At addresses 2048 and greater, the Z8 executes external program memory fetches.

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts.

(ii) **Data Memory** The Z8 can address 62K bytes of external data memory beginning at location 2048 (Fig. 2). External data memory may be include with or separated from the external program memory space. $\overline{DM}$, an optical I/O function that can be programmed to appear on pin $P3_4$, is used to distinguish between data and program memory space.

(iii) **Register File** The 144-byte register file includes four I/O port registers (R0-R3), 124 general-purpose registers (R4-R127) and 16 control and status registers (R240-R255). These registers are assigned the address locations shown in Fig. 3.

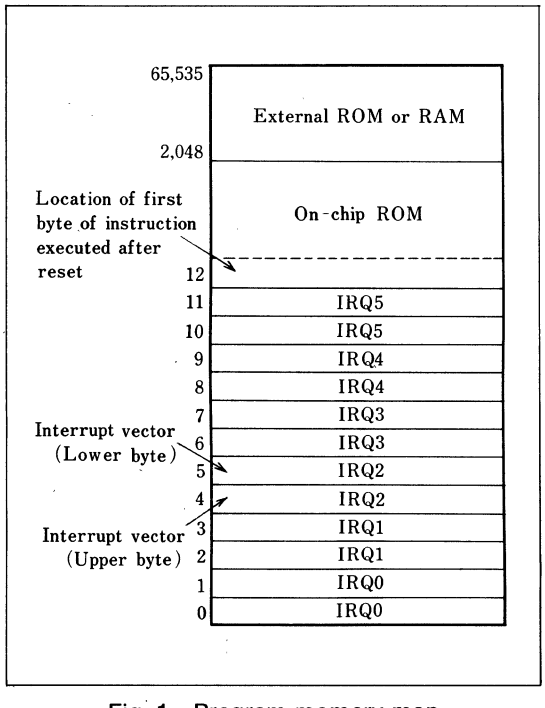


Fig. 1 Program memory map

Z8 instructions can access registers directly or indirectly with an 8-bit address field. The Z8 also allows short 4-bit register addressing using the Register Pointer (one of the control registers). In the 4-bit mode, the register file is divided into nine working-register groups, each occupying 16 contiguous locations. The Register Pointer addresses the starting location of the active working-register group.

(iv) **Stacks** Either the internal register file or the external data memory can be used for the stack. A 16-bit Stack Pointer (R254 and R255) is used for the external stack, which can reside anywhere in data memory between locations 2048 and 65535. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 124 general-purpose registers (R4-R127).

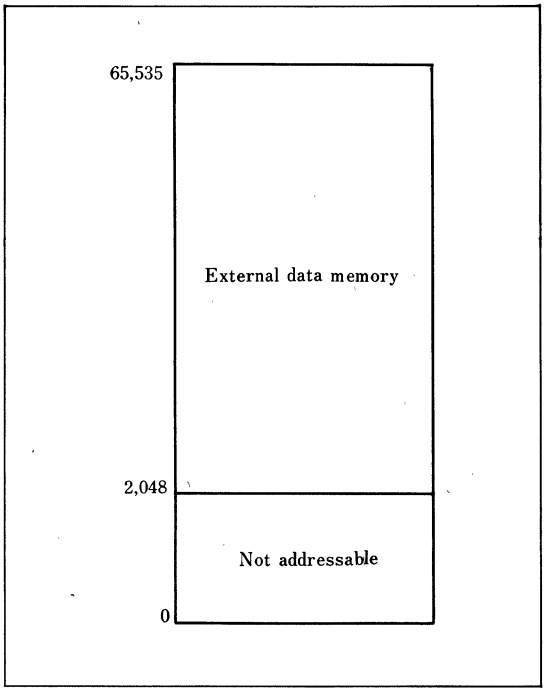


Fig. 2 Data memory map

LOCATION		IDENTIFIERS
255	STACK POINTER(BITS 7-0)	SPL
254	STACK POINTER(BITS 15-8)	SPH
253	REGISTER POINTER	RP
252	PROGRAM CONTROL FLAGS	FLAGS
251	INTERRUPT MASK REGISTER	IMR
250	INTERRUPT REQUEST REGISTER	IRQ
249	INTERRUPT PRIORITY REGISTER	IPR
248	PORTS 0-1 MODE	P01M
247	PORT 3 MODE	P3M
246	PORT 2 MODE	P2M
245	TO PRESCALER	PRE0
244	TIMER/COUNTER 0	T0
243	T1 PRESCALER	PRE1
242	TIMER/COUNTER 1	T1
241	TIMER MODE	TMR
240	SERIAL I/O	SIO
	NOT IMPLEMENTED	
127	GENERAL-PURPOSE REGISTERS	
4		
3	PORT 3	P3
2	PORT 2	P2
1	PORT 1	P1
0	PORT 0	P0

Fig. 3 The register file

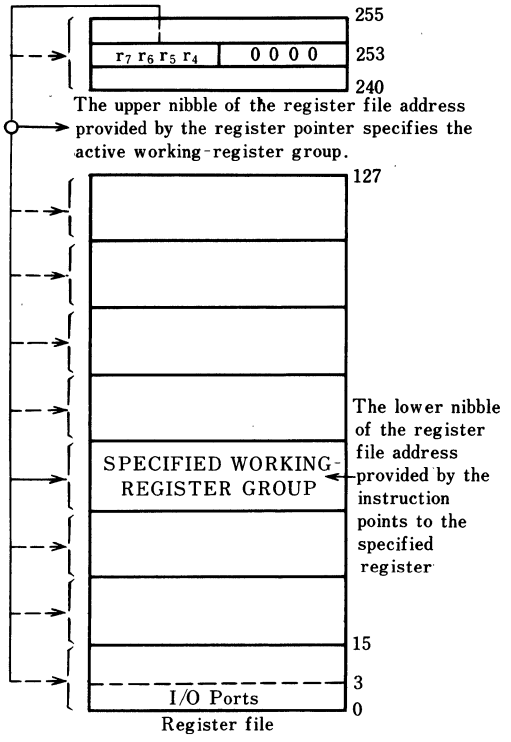


Fig. 4 The register pointer

(2) I/O ports

The Z8 has 32 lines dedicated to input and output. These lines are grouped into four ports of eight lines each and are configurable as input, output or address/data. Under software control, the ports can be programmed to provide address outputs, timing, status signals, serial I/O, and parallel I/O with or without handshake. All ports have active pull-ups and pull-downs compatible with TTL loads.

(i) **Port 1** can be programmed as a byte I/O port or an address/data port for interfacing external memory.

Memory locations greater than 2048 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Adress/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

(ii) **Port 0** can be programmed as a nibble I/O port, or as an address port for interfacing external memory.

For external memory references, Port 0 can provide address bits A_8A_{11} (lower nibble) or A_8-A_{15} (lower and upper nibble) depending on the required address space.

(iii) **Port 2** bits can be programmed independently as input or output. The port is always available for I/O operations. In addition, Port 2 can be configured to provide open-drain outputs.

(iv) **Port 3** lines can be configured as I/O or control lines. In either case, the direction of the eight lines is fixed as four input ($P3_0$-$P3_3$) and four output ($P3_4$-$P3_7$). For serial I/O, lines $P3_0$ and $P3_7$ are programmed as serial in and serial out respectively.

- handshake for Ports 0, 1 and 2 ($\overline{DAV}$ and RDY)
- four external interrupt request signals (IRQ_0-IRQ_3)
- timer input and output signals (T_{IN} and T_{OUT})
- Data Memory Select ($\overline{DM}$).

(3) Serial Input/Output

Port 3 lines $P3_0$ and $P3_7$ can be programmed as serial I/O lines for full-duplex serial asynchronous

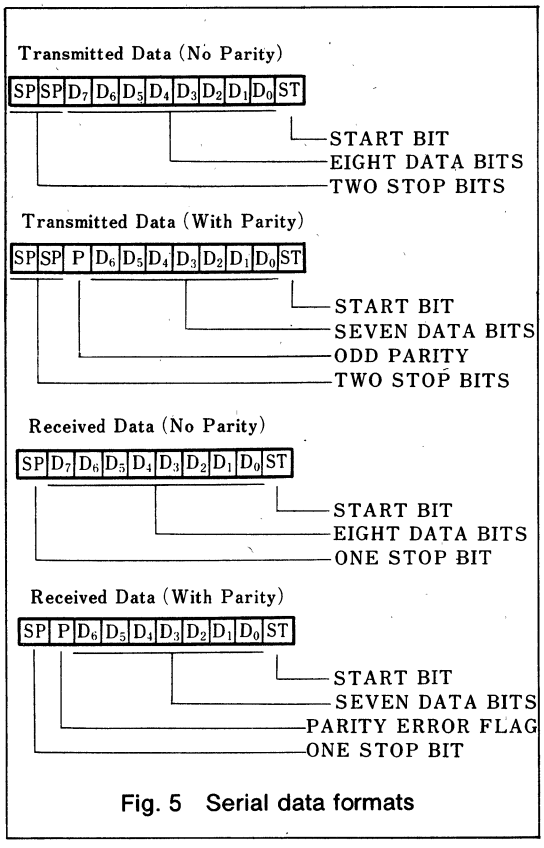


Fig. 5 Serial data formats

receiver/transmitter operation. The bit rate is controlled by Counter/Timer 0, with a maximum rate of 62.5K bits/second.

The Z8 automatically adds a start bit and two stop bits to transmitted data (Fig. 5). Odd parity is also available as an option.

(4) Counter/Timer

The Z8 contains two 8-bit programmable counter/timers (T_0 and T_1), each driven by its own 6-bit programmable prescaler. The T_1 prescaler can be driven by internal or external clock sources; however, the T_0 prescaler is driven by the internal clock only.

The counters can be started, stopped, restarted to continue, or restarted from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuos mode). The counters, but not the prescalers, can be read any time without disturbing their value or count mode.

(5) Interrupts

The Z8 allows six different interrupts from eight sources: the four Port 3 lines $P3_0$-$P3_3$, Serial In, Serial Out, and the two counter/timers. These interrupts are both maskable and prioritized.

All Z8 interrupts are vectored. Polled interrupt systems are also supported.

■ Instruction Set Notation

(1) Addressing modes

The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

(2) Symbols

The following symbols are used in describing the instruction set.

dst	Destination location or contents
src	Source location or contents
cc	Condition code (see list)
@	Indirect address prefix
SP	Stack pointer (control registers 254-255)
PC	Program counter
FLAGS	Flag register (control register 252)
RP	Register pointer (control register 253)
IMR	Interrupt mask register (control register 251)

Assignment of a value is indicated by the symbol "←". For example.

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit "n" of a given location. For example, dst (7) refers to bit 7 of the destination operand.

(3) Flags.

Control Register R252 contains the following six flags :

C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by :

0	Cleared to zero
1	Set to one
*	Set or cleared according to operation
—	Unaffected
×	Undefined

(4) Condition codes

See Table 1.

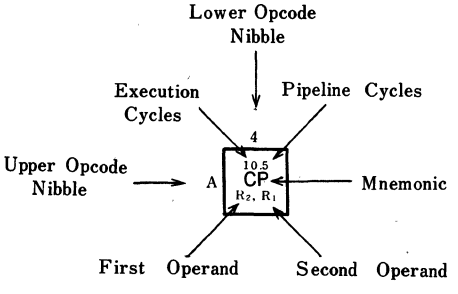
Table 1 Condition codes

Value	Mnemonic	Meaning	Flags set
1000		Always true	.....
0111	C	Carry	C=1
1111	NC	No carry	C=0
0110	Z	Zero	Z=1
1110	NZ	Not Zero	Z=0
1101	PL	Plus	S=0
0101	MI	Minus	S=1
0100	OV	Overflow	V=1
1100	NOV	No overflow	V=0
0110	EQ	Equal	Z=1
1110	NE	Not equal	Z=0
1001	GE	Greater than or equal	(S XOR V) =0
0001	LT	Less than	(S XOR V) =1
1010	GT	Greater than	[Z OR (S XOR V)] =0
0010	LE	Less than or equal	[Z OR (S XOR V)] =1
1111	UGE	Unsigned greater than or equal	C=0
0111	ULT	Unsigned less than	C=1
1011	UGT	Unsigned greater than	(C=0 AND Z=0) =1
0011	ULE	Unsigned less than or equal	(C OR Z) =1
0000		Never true	.....

(5) Opcode map

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 DEC R_1	6.5 DEC IR_1	6.5 ADD r_1, r_2	6.5 ADD r_1, Ir_2	10.5 ADD R_2, R_1	10.5 ADD IR_2, R_1	10.5 ADD R_1, IM	10.5 ADD IR_1, IM	6.5 LD r_1, R_2	6.5 LD r_2, R_1	12/10.5 DJNZ r_1, RA	12/10.0 JR cc, RA	6.5 LD r_1, IM	12/10.0 JP cc, DA	6.5 INC r_1	
1	6.5 RLC R_1	6.5 RLC IR_1	6.5 ADC r_1, r_2	6.5 ADC r_1, Ir_2	10.5 ADC R_2, R_1	10.5 ADC IR_2, R_1	10.5 ADC R_1, IM	10.5 ADC IR_1, IM								
2	6.5 INC R_1	6.5 INC IR_1	6.5 SUB r_1, r_2	6.5 SUB r_1, Ir_2	10.5 SUB R_2, R_1	10.5 SUB IR_2, R_1	10.5 SUB R_1, IM	10.5 SUB IR_1, IM								
3	8.0 JP IRR_1	6.1 SRP IM	6.5 SBC r_1, r_2	6.5 SBC r_1, Ir_2	10.5 SBC R_2, R_1	10.5 SBC IR_2, R_1	10.5 SBC R_1, IM	10.5 SBC IR_1, IM								
4	8.5 DA R_1	8.5 DA IR_1	6.5 OR r_1, r_2	6.5 OR r_1, Ir_2	10.5 OR R_2, R_1	10.5 OR IR_2, R_1	10.5 OR R_1, IM	10.5 OR IR_1, IM								
5	10.5 POP R_1	10.5 POP IR_1	6.5 AND r_1, r_2	6.5 AND r_1, Ir_2	10.5 AND R_2, R_1	10.5 AND IR_2, R_1	10.5 AND R_1, IM	10.5 AND IR_1, IM								
6	6.5 COM R_1	6.5 COM IR_1	6.5 TCM r_1, r_2	6.5 TCM r_1, Ir_2	10.5 TCM R_2, R_1	10.5 TCM IR_2, R_1	10.5 TCM R_1, IM	10.5 TCM IR_1, IM								
7	10/12.1 PUSH R_2	12/14.1 PUSH IR_2	6.5 TM r_1, r_2	6.5 TM r_1, Ir_2	10.5 TM R_2, R_1	10.5 TM IR_2, R_1	10.5 TM R_1, IM	10.5 TM IR_1, IM								
8	10.5 DECW RR_1	10.5 DECW IR_1	12.0 LDE r_1, Irr_2	18.0 LDEI Ir_1, Irr_2												6.1 DI
9	6.5 RL R_1	6.5 RL IR_1	12.0 LDE r_2, Irr_1	18.0 LDEI Ir_2, Irr_1												6.1 EI
A	10.5 INCW RR_1	10.5 INCW IR_1	6.5 CP r_1, r_2	6.5 CP r_1, Ir_2	10.5 CP R_2, R_1	10.5 CP IR_2, R_1	10.5 CP R_1, IM	10.5 CP IR_1, IM								14.0 RET
B	6.5 CLR R_1	6.5 CLR IR_1	6.5 XOR r_1, r_2	6.5 XOR r_1, Ir_2	10.5 XOR R_2, R_1	10.5 XOR IR_2, R_1	10.5 XOR R_1, IM	10.5 XOR IR_1, IM								16.0 IRET
C	6.5 RRC R_1	6.5 RRC IR_1	12.0 LDC r_1, Irr_2	18.0 LDCI Ir_1, Irr_2				10.5 LD r_1, x, R_2								6.5 RCF
D	6.5 SRA R_1	6.5 SRA IR_1	12.0 LDC r_2, Irr_1	18.0 LDCI Ir_2, Irr_1	20.0 CALL* IRR_1		20.0 CALL DA	10.5 LD r_2, x, R_1								6.5 SCF
E	6.5 RR R_1	6.5 RR IR_1		6.5 LD r_1, Ir_2	10.5 LD R_2, R_1	10.5 LD IR_2, R_1	10.5 LD R_1, IM	10.5 LD IR_1, IM								6.5 CCF
F	8.5 SWAP R_1	8.5 SWAP IR_1		6.5 LD Ir_1, r_2		10.5 LD R_2, IR_1										6.0 NOP
Bytes per Instruction					3						2			3	1	



Legend:
R = 8-Bit Address
r = 4-Bit Address
R_1 or r_1 = Dst Address
R_2 or r_2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: The blank areas are not defined.

(6) Instruction Summary

Instruction and Operation	Addr Mode dst	Addr Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst,src dst←dst+src+C	(Note 1)		1□	*	*	*	*	0	*
ADD dst,src dst←dst+src	(Note 1)		0□	*	*	*	*	0	*
AND dst,src dst←dst AND src	(Note 1)		5□	-	*	*	0	-	-
CALL dst SP←SP−2 @SP←PC;PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			E F	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst,src dst←src	(Note 1)		A□	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst−1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst−1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZ r,dst r←r−1 if r 0 PC←PC+dst Range: +127,−128	RA		rA r=0−F	-	-	-	-	-	-
EI IMR(7) ←1			9F	-	-	-	-	-	-
INC dst dst←dst+1	r R IR		rE r=0−F 20 21	-	*	*	*	-	-
INCW dst dst←dst+1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP+1 PC←@SP;SP←SP+2;IMR(7)←1			BF	*	*	*	*	*	*
JP cc,dst if cc is true PC←dst	DA IRR		cD c=0−F 30	-	-	-	-	-	-
JR cc,dst if cc is true, PC←PC+dst Range: +127,−128	RA		cB c=0−F	-	-	-	-	-	-
LD dst,src dst←src	r r R r X r r Ir Ir r R R R IR R IM IR IM IR R	IM R r X r Ir r R IR IM	rC r8 r9 r=0−F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst,src dst←src	r Irr	Irr r	C2 D2	-	-	-	-	-	-
LDCI dst,src dst←src r←r+1;rr←rr+1	Ir Irr	Irr Ir	C3 D3	-	-	-	-	-	-
LDE dst,src dst←src	r Irr	Irr r	82 92	-	-	-	-	-	-
LDEI dst,src dst←src r←r+1;rr←rr+1	Ir Irr	Irr Ir	83 93	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-
OR dst,src dst←dst OR src	(Note 1)		4□	-	*	*	0	-	-
POP dst dst←@SP SP←SP+1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP−1;@SP←src	R IR		70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC @SP;SP←SP+2			AF	-	-	-	-	-	-
RL dst	R IR		90 91	*	*	*	*	-	-
RLC dst	R IR		10 11	*	*	*	*	-	-
RR dst	R IR		E0 E1	*	*	*	*	-	-
RRC dst	R IR		C0 C1	*	*	*	*	-	-
SBC dst,src dst←dst−src−C	(Note 1)		3□	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src	IM		31	-	-	-	-	-	-
SUB dst,src dst←dst−src	(Note 1)		2□	*	*	*	*	1	*
SWAP dst	R IR		F0 F1	X	*	*	X	-	-
TCM dst,src (NOT dst) AND src	(Note 1)		6□	-	*	*	0	-	-
TM dst,src dst AND src	(Note 1)		7□	-	*	*	0	-	-
XOR dst,src dst←dst XOR src	(Note 1)		B□	-	*	*	0	-	-

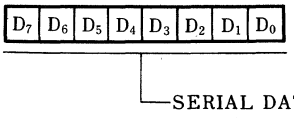
Note 1 These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a □ in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, to determine the opcode of an ADC instruction use the addressing modes r (destination) and Ir (source). The result is 13

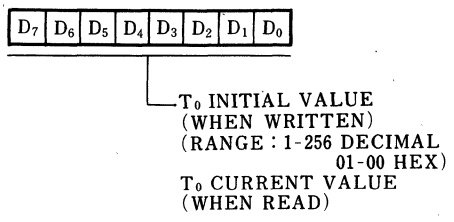
Addr Mode dst	Addr Mode src	Lower Opcode Nibble
r	r	2
r	Ir	3
R	R	4
R	IR	5
R	IM	6
IR	IM	7

■ Register

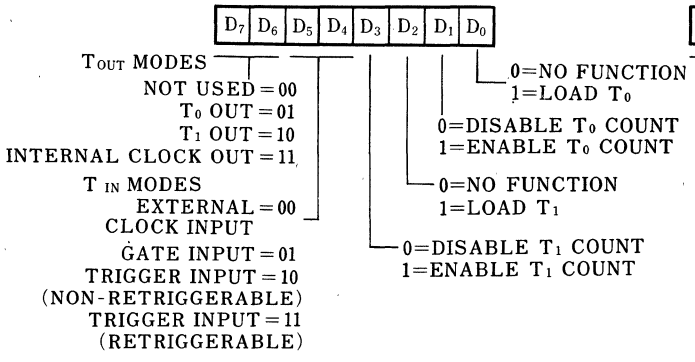
R240 (SIO)
Serial I/O Register
(F0H : Read/Write)



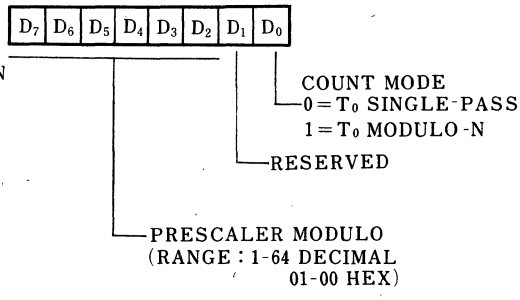
R244 (T0)
Counter/Timer 0 Register
(F4H : Read/Write)



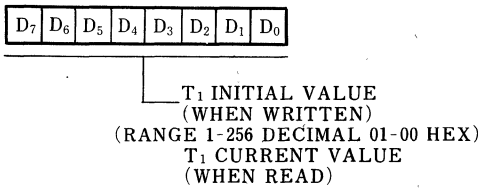
R241 (TMR)
Timer Mode Register
(F1H : Read/Write)



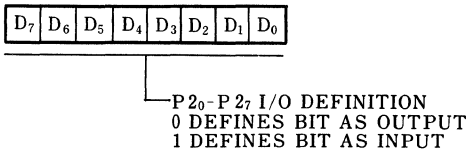
R245 (PRE0)
Prescaler 0 Register
(F5H : Write Only)



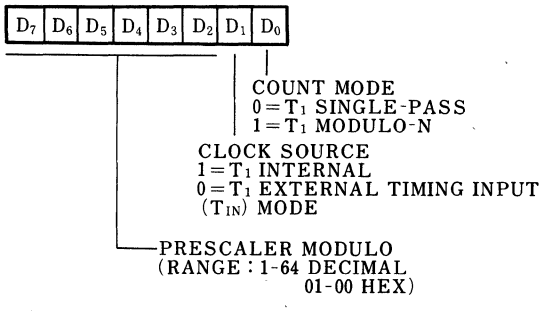
R242 (T1)
Counter Timer 1 Register
(F2H : Read/Write)



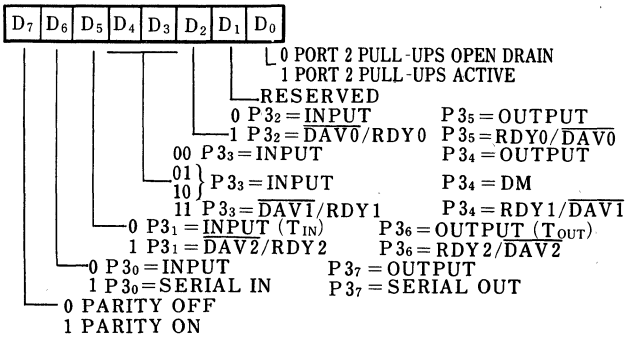
R246 (P2M)
Port 2 Mode Register
(F6H : Write Only)



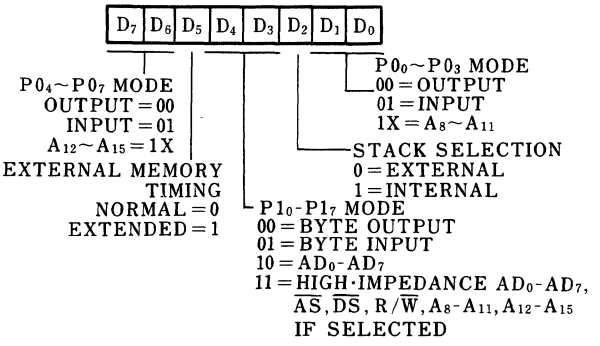
R243 (PRE1)
Prescaler 1 Register
(F3H : Write Only)



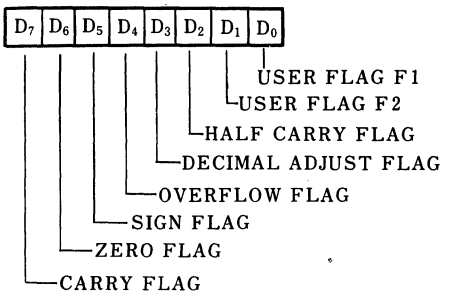
R247 (P3M)
Port 3 Mode Register
(F7H : Write Only)



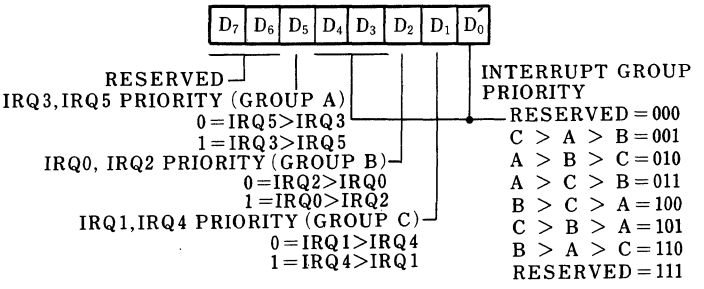
R248 (P01M)
Port 0 and 1 Mode Register
($F8_H$: Write Only)



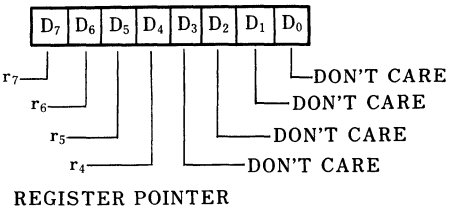
R252 (FLAGS)
Flag Register
(FC_H : Read/Write)



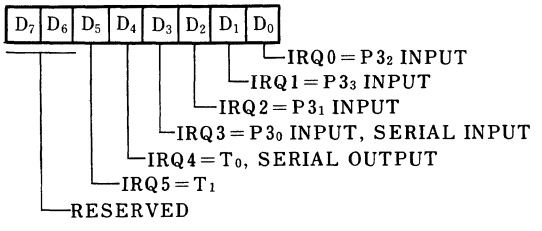
R249 (IPR)
Interrupt Priority Register
($F9_H$: Write Only)



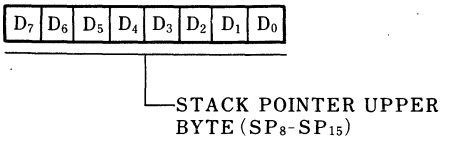
R253 (RP)
Register Pointer
(FD_H : Read/Write)



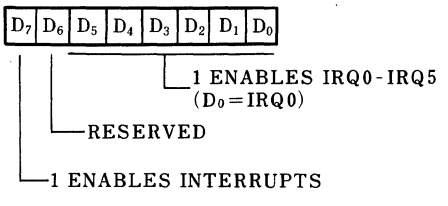
R250 (IRQ)
Interrupt Request Register
(FA_H : Read/Write)



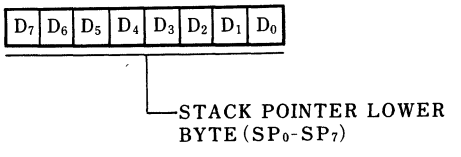
R254 (SPH)
Stack Pointer
(FE_H : Read/Write)



R251 (IMR)
Interrupt Mask Register
(FB_H : Read/Write)



R255 (SPL)
Stack Pointer
(FF_H : Read/Write)



LH0802 Z8-02 Development Device

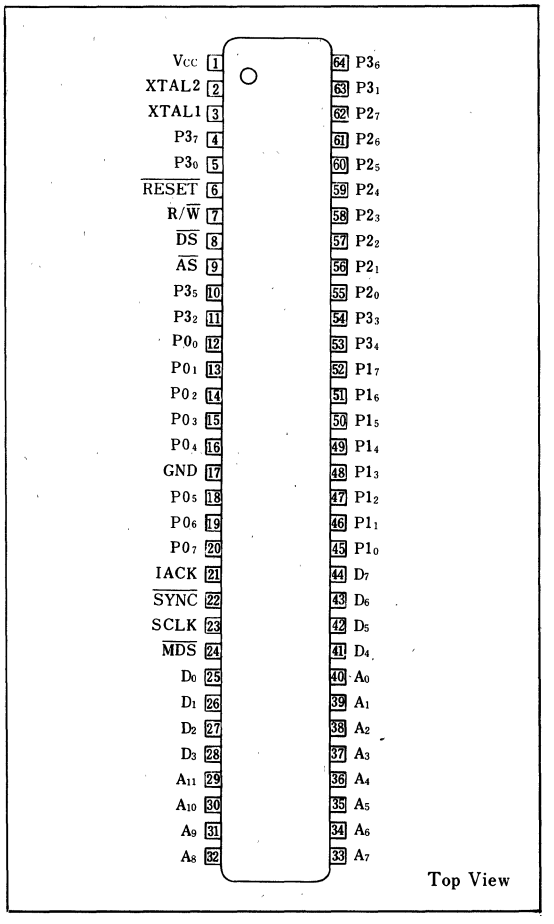
■ Description

The 64-pin Z8-02 is the development version of the Z8-01 with internal mask-programmed ROM. This device allows the user to build the prototype systems in hardware with an actual device and to develop the code that is eventually mask-programmed into the on-chip ROM of the Z8-01.

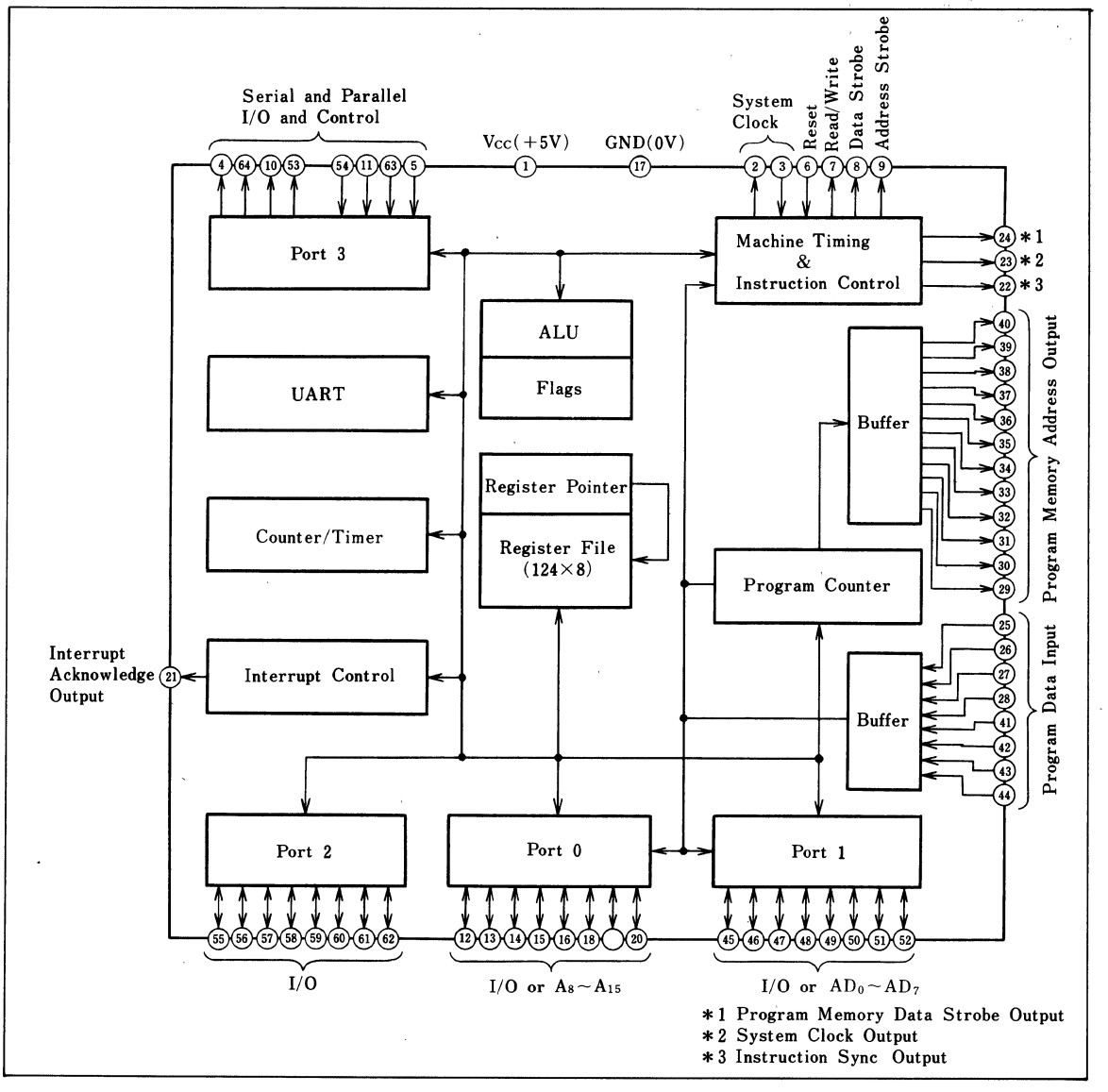
The Z8-02 is identical to the Z8-01 with the following exceptions :

- The internal ROM has been removed.
- The ROM address lines and data lines are buffered and brought out to external pins.
- Control lines for the new memory have been added.

■ Pin Connections



■ Block Diagram



■ Pin Description

The Z8-20 has 64 pins, 40 of which are the same as those on the Z8-01. The remaining 24 pins are as follows.

Pin	Meaning	I/O	Function
$A_0 \sim A_{11}$	Address Bus	O	Address signal for internal ROM.
$D_0 \sim D_7$	Data Bus	I	Data signal for internal ROM.
$\overline{MDS}$	Data Strobe	O	Active "Low". Internal ROM addresses are valid.
IACK	Interrupt Acknowledge	O	Active "High". Detects an interrupt.
$\overline{SYNC}$	Command Synchronization	O	Active "Low". For synchronizing the command fetch cycle.
SCLK	System Clock	O	Internal system clock. 1/2 of the external clock.

LH0803 Z8-03 Protopack Emulator

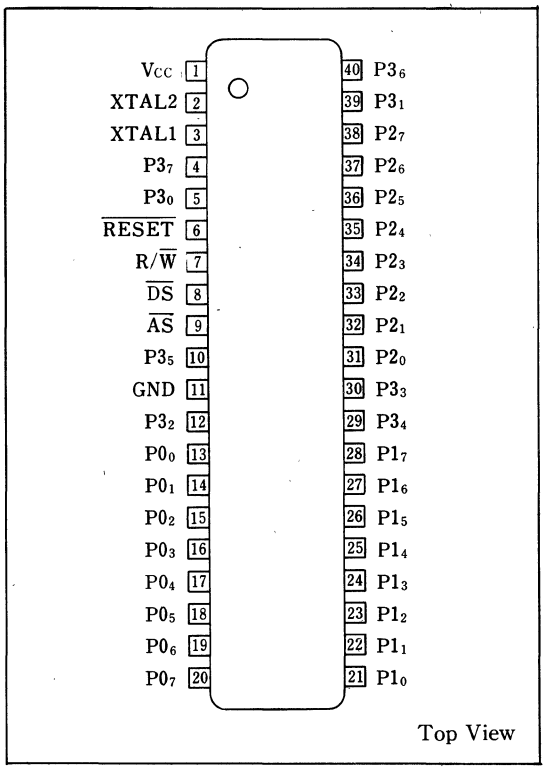
■ Description

The Z8-03 (LH0803) is a ROMless version of the standard Z8-01, housed in a pin compatible 40-pin package.

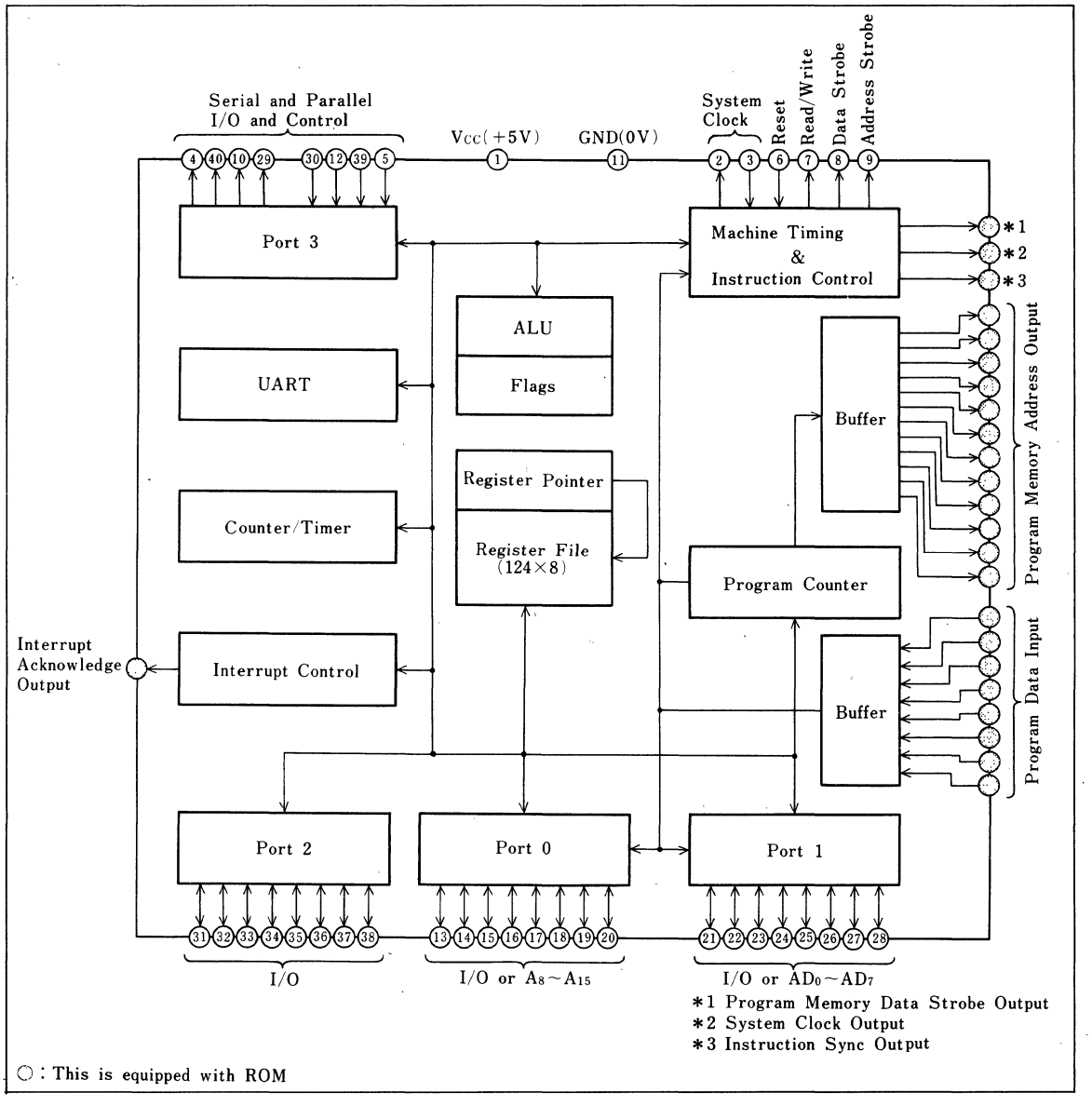
The Z8-03 carries a 24-pin socket for a direct interface to program memory. 2716 type EPROM can be used for program memory.

The Z8-03 allows the user to build the prototype and pilot production units. When the final program is established, the user can then switch over to the Z8-01.

■ Pin Connections



■ Block Diagram



■ Pin Description

The pins of the Z8-03 are compatible with those of the Z8-01. For the pin description, refer back to the Z8-01 explanation.

LH0811 Z8-11 Microcomputer Unit

■ Description

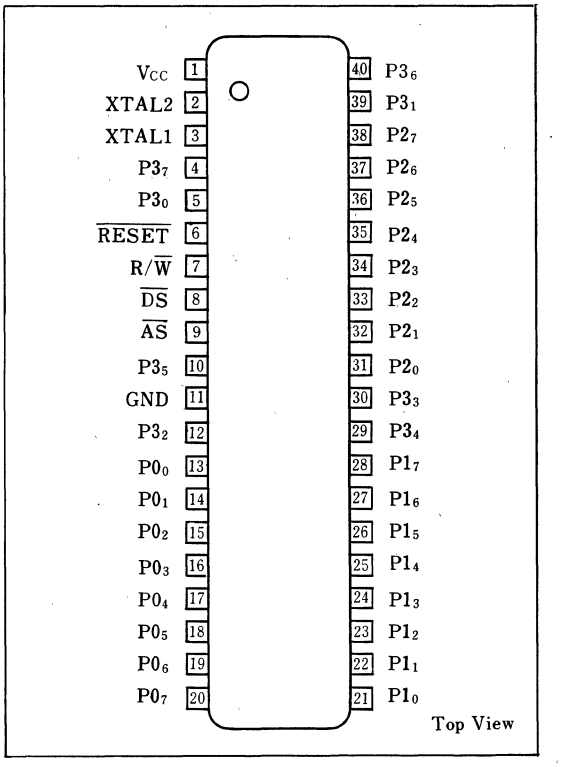
Compared to earlier single-chip microcomputers, the Z8 offers faster execution ; more efficient use of memory ; more sophisticated interrupt, input/output and bit-manipulation capabilities ; and easier system expansion.

Under program control, the Z8 can be tailored to the needs of user. It can be configured as a standalone microcomputer with 4K bytes of internal ROM, a traditional microprocessor that manages up to 120K bytes of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-BUS. In all configurations, a large number of pins remain available for I/O.

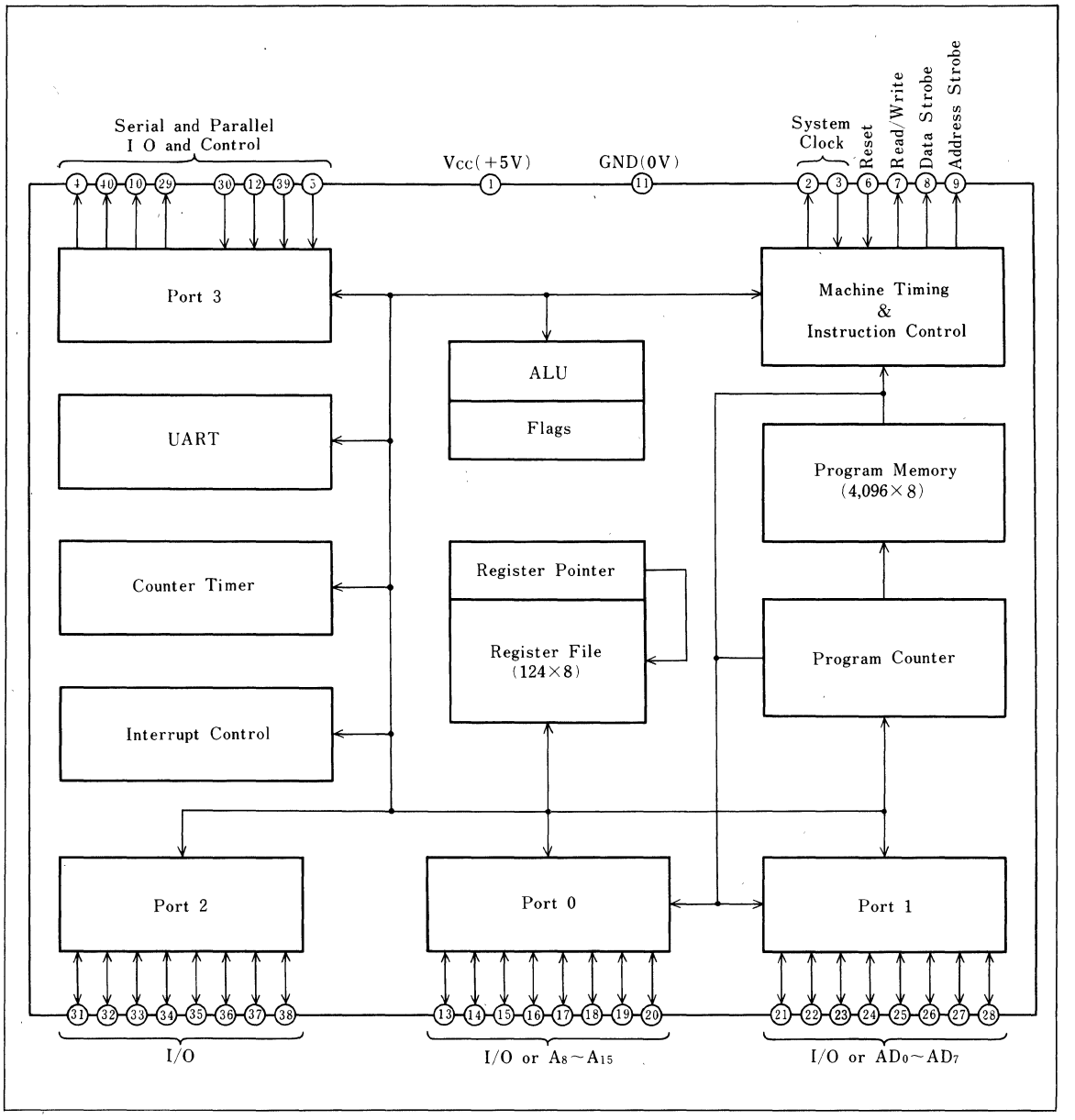
■ Features

1. Complete single-chip microcomputer with internal ROM, RAM and I/O
   - RAM 124 bytes
   - ROM 4K bytes
   - I/O 32 lines
2. On-chip two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler
3. Full-duplex UART
4. 144-byte register file
5. Register pointer so that short, fast instructions can access any working register groups
6. Vectored, priority interrupts for I/O, counter/timers, and UART
7. Up to 60K bytes addressable external space each for program and data memory
8. On-chip oscillator
9. High speed instruction execution
   - Working register operating time : 1.5 μs
   - Average instruction execution time : 2.2 μs
   - Maximum instruction execution time : 5.0 μs
10. Low-power standby option which retains contents of general-purpose registers
11. Single +5V power supply
12. All pins are TTL compatible

■ Pin Connections



■ Block Diagram



■ Pin Description

The pins of the Z8-11 are compatible with those of the Z8-01. For the pin description, refer back to the Z8-01 explanation.

LH0812 Z8-12 Development Device

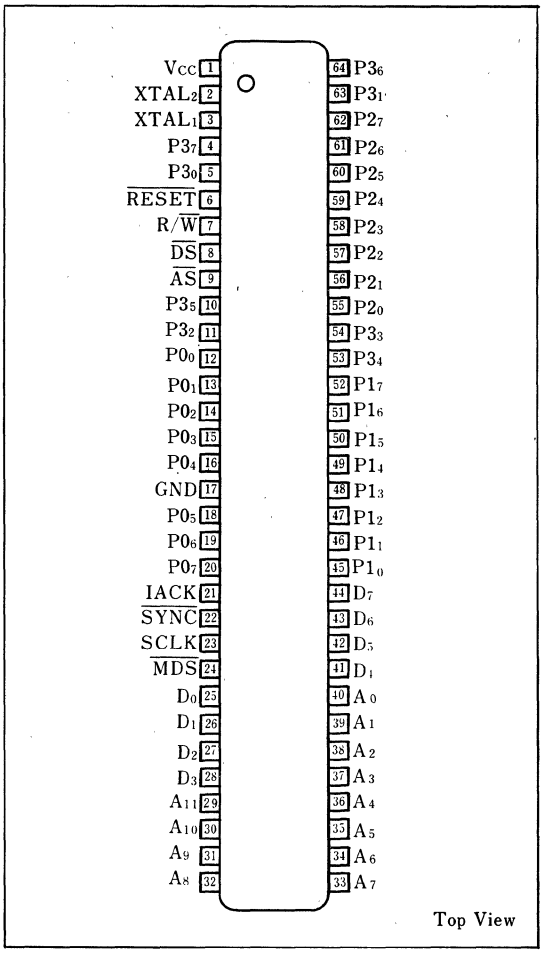
■ Description

The 64-pin Z8-12 is the development version of the Z8-11 with internal mask-programmed ROM. This device allows the user to build the prototype systems in hardware with an actual device and to develop the code that is eventually mask-programmed into the on-chip ROM of the Z8-11.

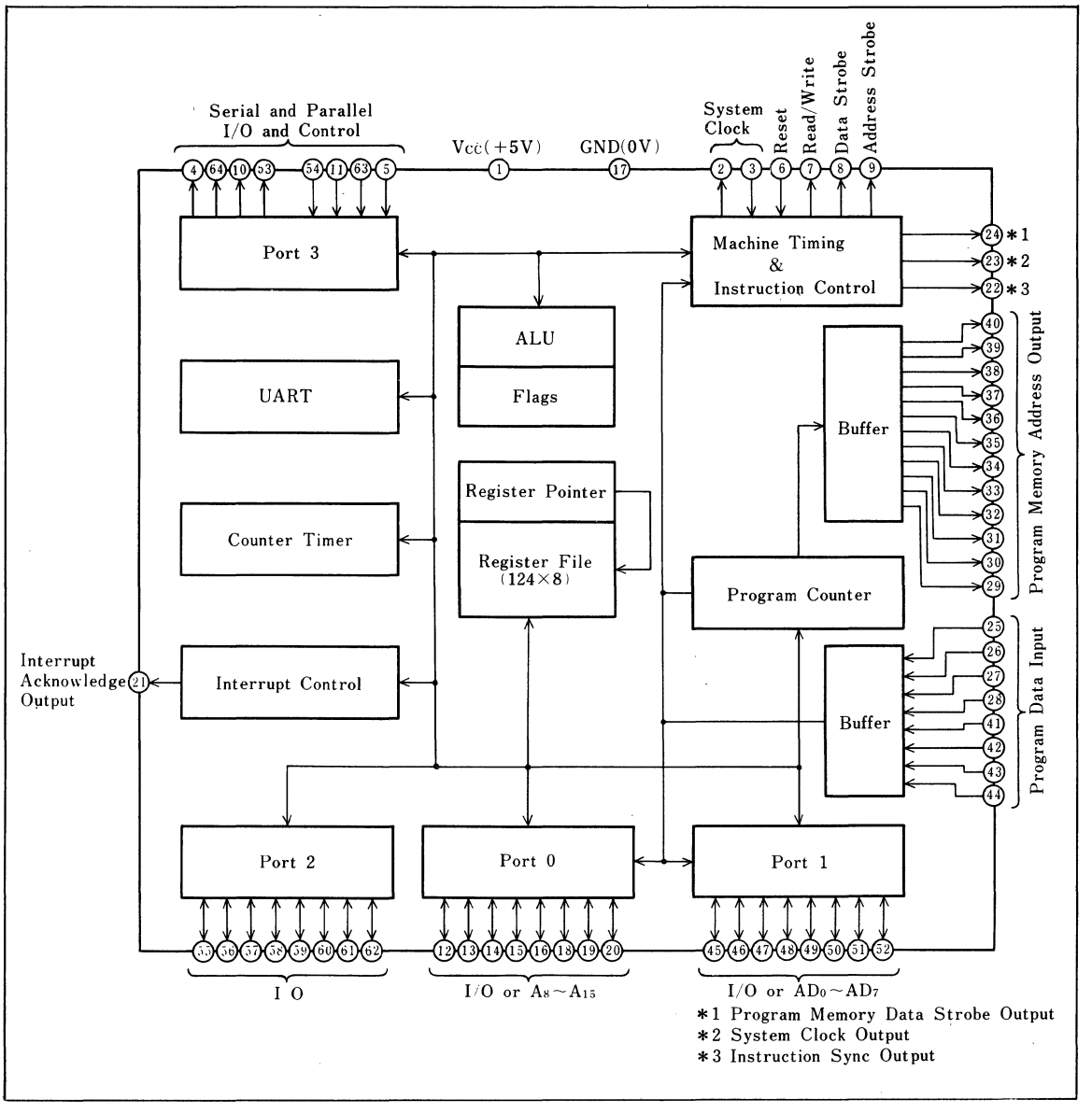
The Z8-12 is identical to the Z8-11 with the following exceptions :

- The internal ROM has been removed.
- The ROM address lines and data lines are buffered and brought out to external pins.
- Control lines for the new memory have been added.

■ Pin Connections



■ Block Diagram



■ Pin Description

The Z8-12 has 64 pins, 40 of which are the same as those on the Z8-11. The remaining 24 pins are as follows.

Pin	Meaning	I/O	Function
$A_0 \sim A_{11}$	Address Bus	O	Address signal for internal ROM
$D_0 \sim D_7$	Data Bus	I	Data signal for internal ROM.
$\overline{MDS}$	Data Strobe	O	Active "Low". Internal ROM addresses are valid.
IACK	Interrupt Acknowledge	O	Active "High". Detects an interrupt.
$\overline{SYNC}$	Command Synchronization	O	Active "Low". For synchronizing the command fetch cycle.
SCLK	System Clock	O	Internal system clock. 1/2 of the external clock.

LH0813 Z8-13 Protopack Emulator

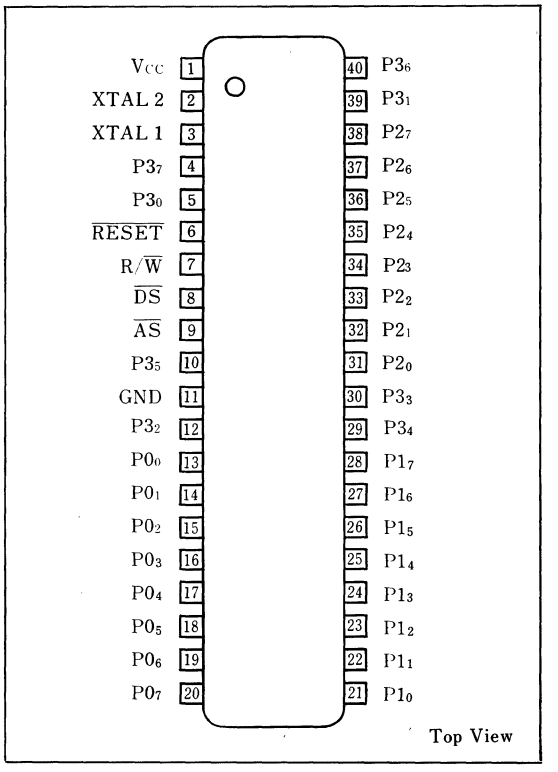
Description

The Z8-13 (LH0813) is a ROMless version of the standard Z8-11, housed in a pin compatible 40-pin package.

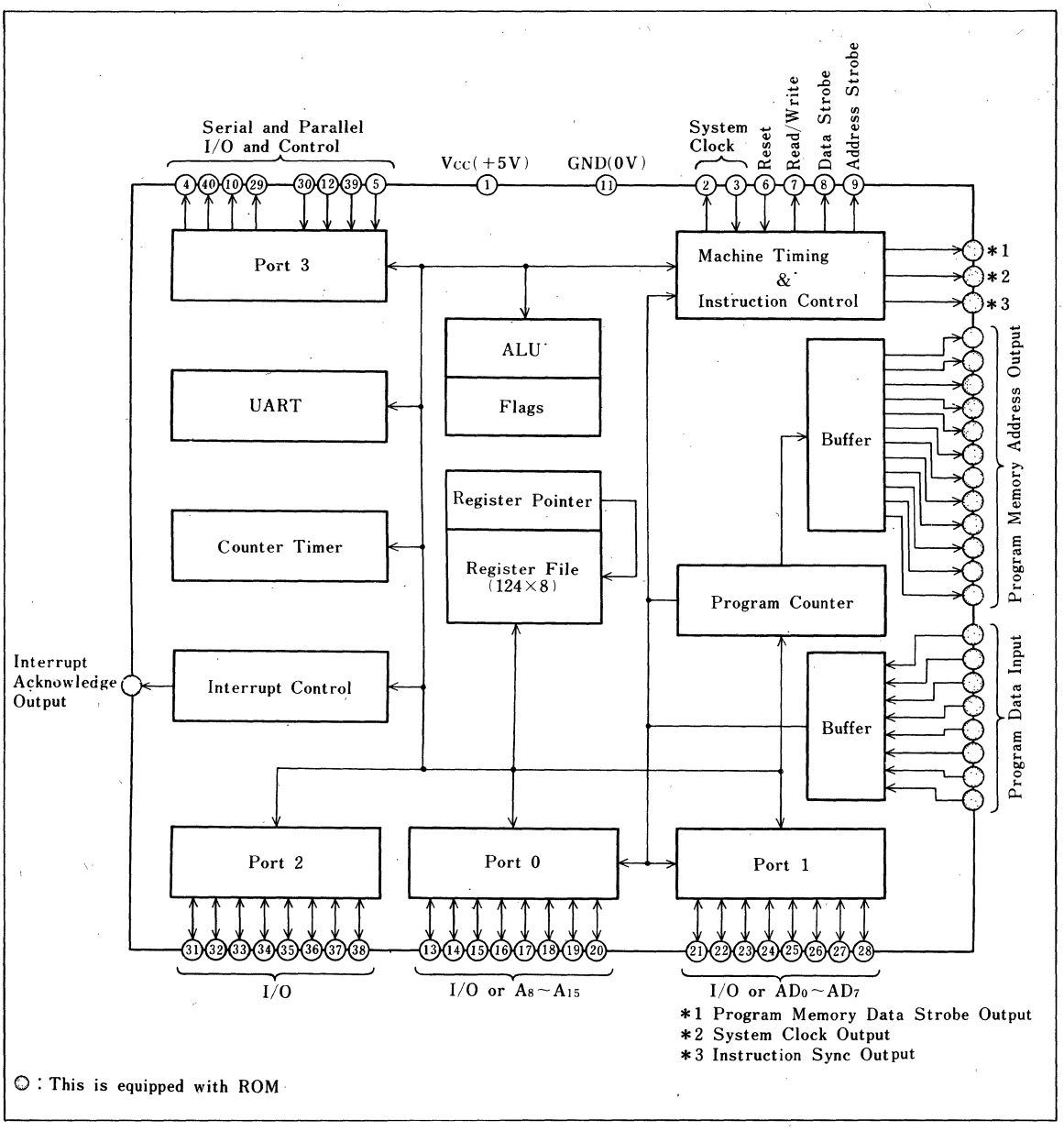
The Z8-13 carries a 24-pin socket for a direct interface to program memory. 2732 type EPROM can be used for program memory.

The Z8-13 allows the user to build the prototype and pilot production units. When the final program is established, the user can then switch over to the Z8-11.

Pin Connections



■ Block Diagram



■ Pin Description

The pins of the Z8-13 are compatible with those of the Z8-11 and Z8-01 as well. For the pin description, refer back to the Z8-01 explanation.

LH0881 Z8-81 Microcomputer Unit

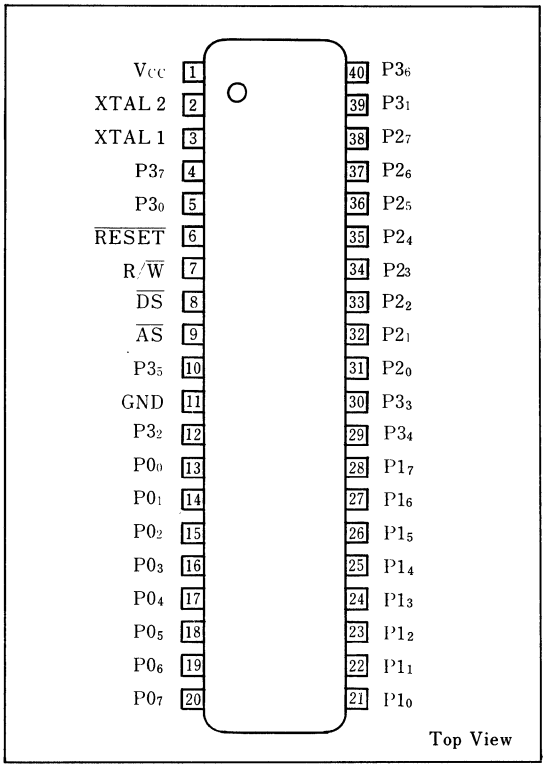
■ Description

LH0881 is the ROMless version of the LH0801/LH0811(Z8) single-chip microcomputer and offer the outstanding feature of the Z8 Family architecture. Port 1 is configured to function as multiplexed Address/Data bus (AD_0~AD_7), while Port 0 is software configurable to output address bus (A_8~A_{15}). Therefore, this device is capable of addressing up to 128K bytes of the external memory space. Using the external memory instead of the internal memory, it is possible to design more powerful microcomputer system incorporating a minimum number of support devices.

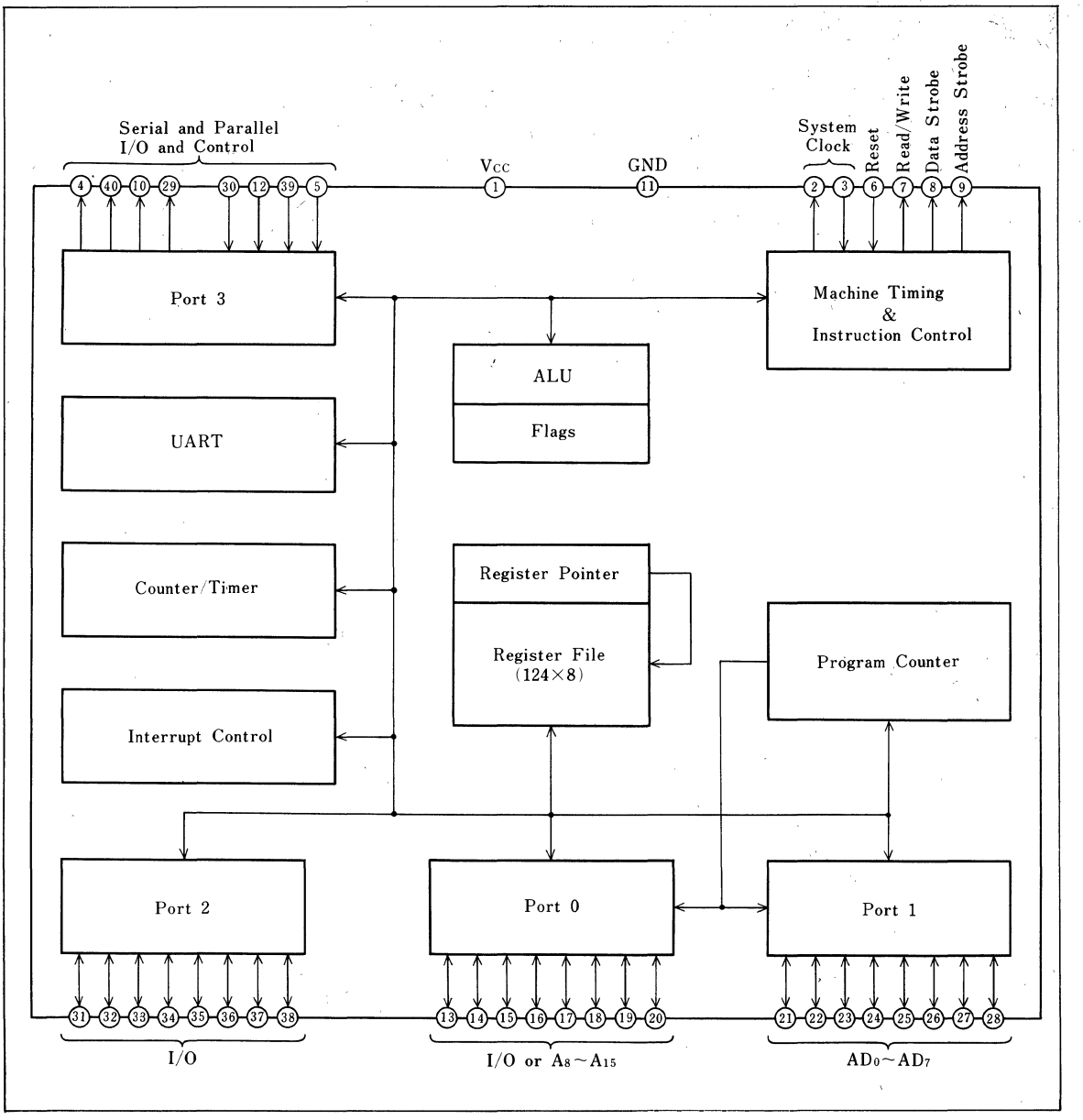
■ Features

1. Complete microcomputer, 24 I/O lines, and up to 64K bytes addressable external space each for program and data memory.
2. 143 bytes register file, including 124 general-purpose registers, three I/O port registers, and 16 status and control registers.
3. Register pointer so that short, fast instructions can access any one of the nine working-register groups.
4. Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
5. Vectored priority interrupts for I/O, counter/timers, and UART.

■ Pin Connections



Block Diagram



Pin Description

The pins of the Z8-81 have the same functions as those of the Z8-01 and Z8-11, except pins $P1_0$ to $P1_7$.

Pin	Meaning	I/O	Function
$P1_0$~$P1_7$	Address/Data bus	I/O	Multiplexed address/data bus.

■ Address space

(1) Program Memory

The Z8-81, having a 16-bit program counter, addresses 64K-bytes of external program memory. All the command codes are fetched from these external program memories.

For the Z8-81, the first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at location 000C$_H$ after a reset.

(2) Data Memory *

The Z8-81 can address 64K bytes of external data memory. External data memory may be included with or separated from the external program memory space. $\overline{DM}$, an optional I/O function that can be programmed to appear on pin P3$_4$, is used to distinguish between data and program memory space.

(3) Register File

The 143-byte register file includes three I/O port registers (RO, R2, R3), 124 general-purpose registers (R4-R127) and 16 control and status registers (R240-R255).

These registers are assigned the address locations shown in Fig. 2.

Z8-81 instructions can access registers directly or indirectly with an 8-bit address field. This also allows short 4-bit register addressing using the Register Pointer (one of the control registers). In the 4-bit mode, the regiter file is divided into nine working register groups, each occupying 16 contiguous locations. The Register Pointer addresses the starting location of the active working-register group.

(4) Stacks

Either the internal register file or the external data memory can be used for the stack. A 16-bit Stack Pointer (R254 and R255) is used for the external stack, which can reside anywhere in data memory. An 8-bit Stack Pointer (R255) is used for the interanl stack that resides within the 124 general-purpose registers (R4-R127).

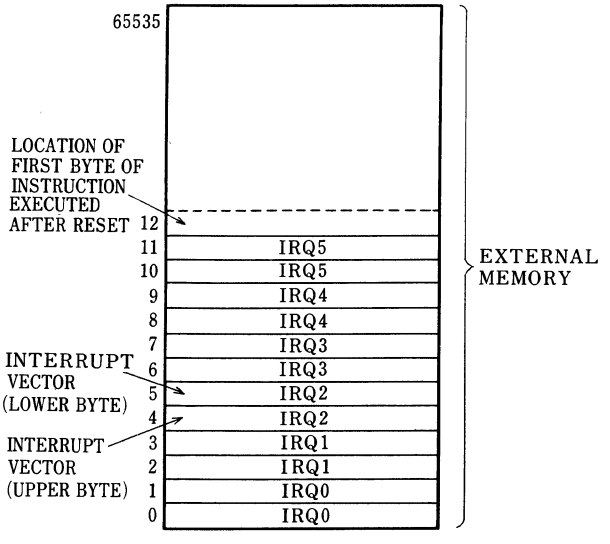


Fig. 1 Program memory map

LOCATION		IDENTIFIERS
255	STACK POINTER (BITS 7-0)	SPL
254	STACK POINTER (BITS 15-8)	SPH
253	REGISTER POINTER	RP
252	PROGRAM CONTROL FLAGS	FLAGS
251	INTERRUPT MASK REGISTER	IMR
250	INTERRUPT REQUEST REGISTER	IRO
249	INTERRUPT PRIORITY REGISTER	IPR
248	PORTS 0-1 MODE	P01M
247	PORT 3 MODE	P3M
246	PORT 2 MODE	P2M
245	T0 PRESCALER	PRE0
244	TIMER/COUNTER 0	T0
243	T1 PRESCALER	PRE1
242	TIMER/COUNTER 1	T1
241	TIMER MODE	TMR
240	SERIAL I/O	SIO
	NOT IMPLEMENTED	
127		
	GENERAL-PURPOSE REGISTERS	
4		
3	PORT 3	P3
2	PORT 2	P2
1	NOT IMPLEMENTED	
0	PORT 0	P0

Fig. 2 The register file

■ Port Functions

The Z8-81 has a dedicated memory interface port (Port 1) and input/output ports (Port 0, 2, 3). These ports are given eight lines each. The functions of Port 0, 2 and 3 are the same as those of the Z8-01/11.

Port 1 is a dedicated Z-bus compatible memory interface. The operations of Port 1 are supported by the Address Strobe ($\overline{AS}$) and Data Strobe ($\overline{DS}$) lines, and by the Read/Write (R/$\overline{W}$) and Data Memory ($\overline{DM}$) control lines.

The low-order program and data memory address (A_0-A_7) are output through Port 1 and are multiplexed with data in/out (D_0-D_7). Instruction fetch and data memory read/write operations are done through this port.

Port 1 cannot be used as a register nor can a handshake mode be used with this port.

If more than eight address lines are required with the Z8-81, additional lines can be obtained by programming Port 0 bits as address bits. The least-significant four bits of Port 0 can be configured to supply address bits A_8-A_{11} for 4K byte addressing or both nibbles of Port 0 can be configured to supply address bits A_8-A_{15} for 64K byte addressing.

■ Registers

The Z8-81 control registers are the same as on the Z8-01/Z8-11, except two bits D_3 and D_4 in the Port 0, 1 Mode Register (R248).

■ Serial Input/Output

The Z8-81 serial input/output functions are the same as those of the Z8-01/Z8-11. (Refer back to the Z8-01 description.)

■ Counter/Timers

The Z8-81 counter/timer functions are the same as those of the Z8-01/Z8-11. (Refer back to the Z8-01 description.)

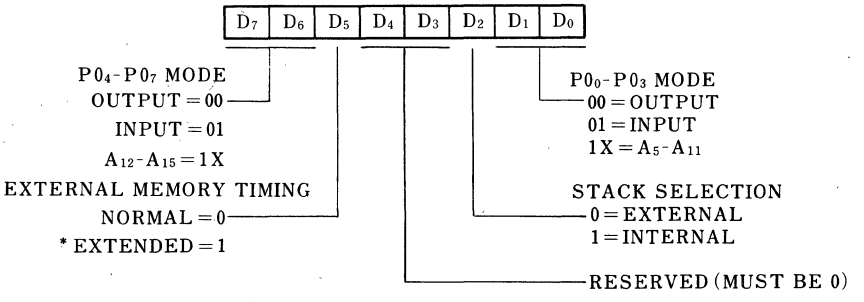
■ Interrupts

The Z8-81 interrupt functions are the same as those of the Z8-01/Z8-11. (Refer back to the Z8-01 description.)

■ Instructions and AC/DC Characteristics

These data of the Z8-81 are the same as for the Z8-01/Z8-11. (Refer back to the Z8-01 description.)

R248 (P01M) Port 0, 1 Mode Register ($F8_H$ Write only)



SM-803 CMOS 8-Bit 1-Chip Microcomputer

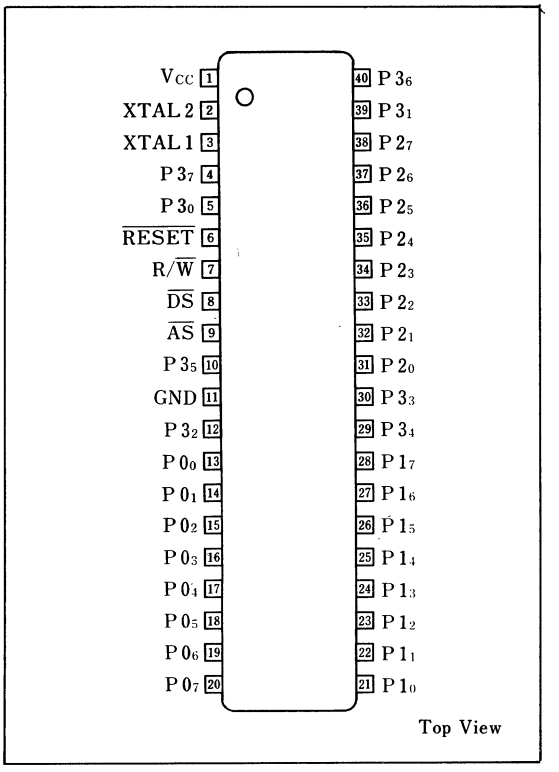
■ Description

The SM-803 is the CMOS version of LH0811 (Z8). This device is configured as a stand-alone microcomputer with 4K bytes of internal ROM, 128 bytes of RAM, up to 60K bytes addressable external space each for program and data memory, two programmable 8-bit counter/timers, and UART.

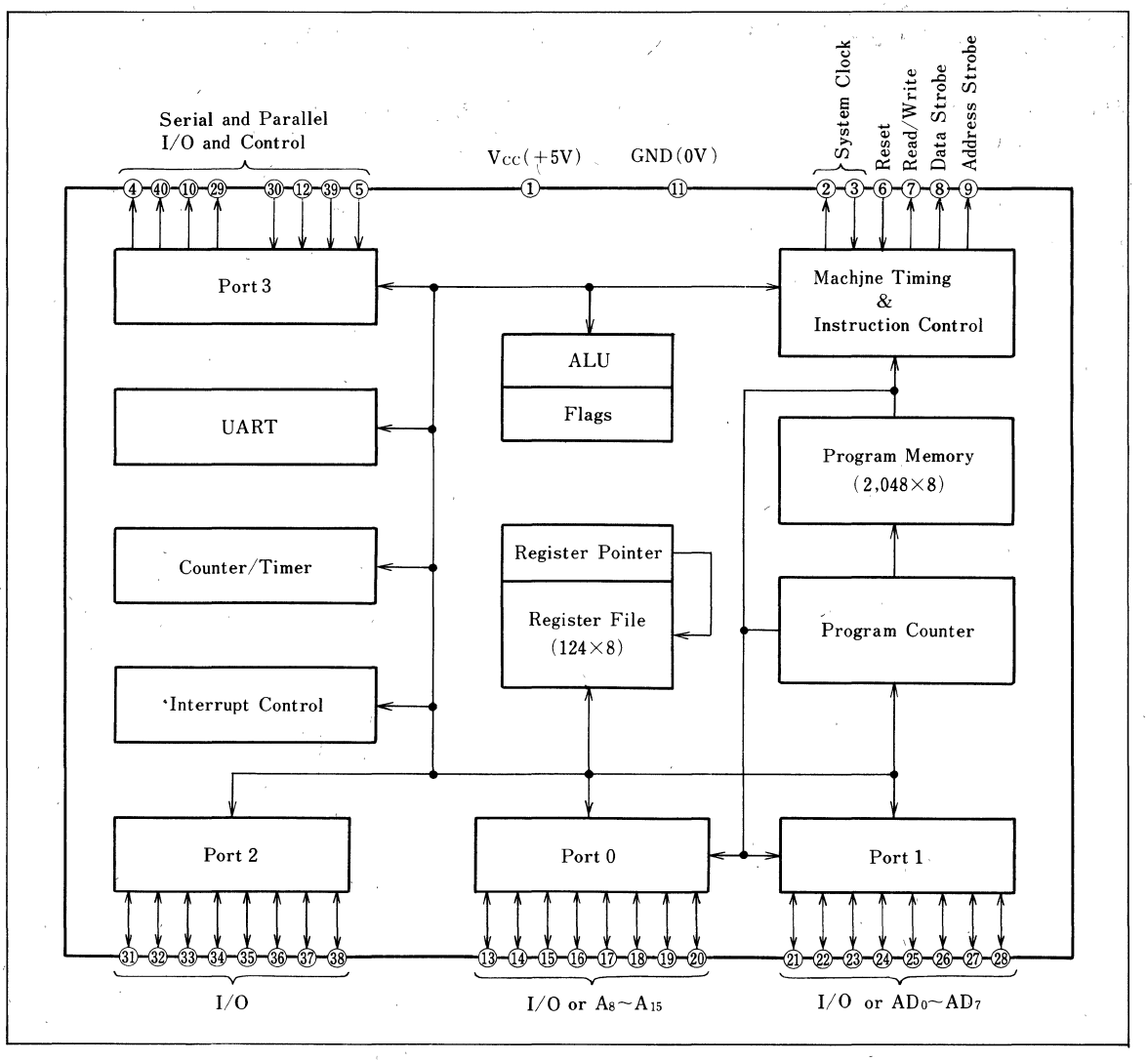
■ Features

1. CMOS silicon-gate process technology
2. Complete microcomputer, 4K bytes of ROM, 128 bytes of RAM, 32 I/O lines, and up to 60K bytes addressable external space each for program and data memory
3. 144-byte register file, including 124 general-purpose registers, four I/O port registers, and 16 status and control registers
4. Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler
5. Vectored priority interrupts for I/O, counter/timers, and UART
6. Average instruction execution time of 2.2 μs
7. On-chip oscillator which accepts crystal or external clock drive
8. Power saving function (HALT/STOP instruction mode)
9. Low power consumption 12mA (TYP.)
10. Single +5V power supply
11. 40-pin dual-in-line package (or 44-pin quad-flat package)

■ Pin Connections



Block Diagram



Pin Description

Pin	Meaning	I/O	Function
$P0_0$~$P0_7$	Port 0	I/O	8-bit I/O port, programmable for I/O.
$P1_0$~$P1_7$	Port 1	I/O	Programmable for I/O in bytes.
$P2_0$~$P2_7$	Port 2	I/O	Programmable for I/O in bits.
$P3_0$~$P3_7$	Port 3	I/O	$P3_0$-$P3_3$ for input, $P3_4$-$P3_7$ for output.
$\overline{AS}$	Address strobe	O	Active "Low", activated for external address memory transfer.
$\overline{DS}$	Data strobe	O	Active "Low", activated for external data memory transfer.
R/$\overline{W}$	Read/Write	O	Read at "High", write at "Low".
$\overline{RESET}$	Reset	I	Active "Low". initializes.
XTAL1	Clock 1	I	Clock pin.
XTAL2	Clock 2	O	Clock pin.

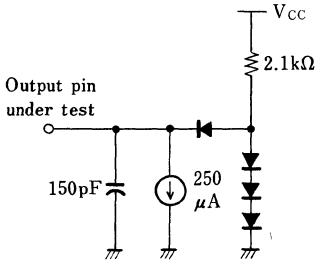
■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7	V
Output voltage	V_{OUT}	−0.3～+7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

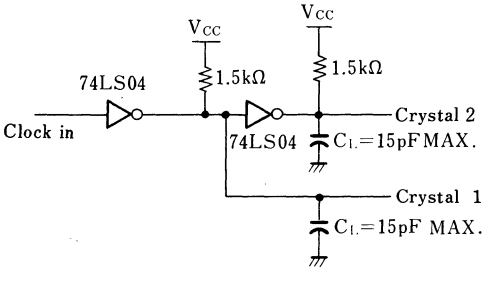
■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock input high voltage	V_{CH}	Driven by external clock oscillator	3.8		V_{CC}	V	
Clock input low voltage	V_{CL}	Driven by external clock oscillator	−0.3		0.8	V	
Input high voltage	V_{IH}		2.0		V_{CC}	V	
Input low voltage	V_{IL}		−0.3		0.8	V	
Reset input high voltage	V_{RH}		3.8		V_{CC}	V	
Reset input low voltage	V_{RL}		−0.3		0.8	V	
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4			V	
Output low voltage	V_{OL}	I_{OL}=+2.0mA			0.4	V	
Input leakage cuurrent	$\lvert I_{IL} \rvert$	0V≦V_{IN}≦+5.25V			10	μA	
Output leakage current	$\lvert I_{OL} \rvert$	0V≦V_{IN}≦+5.25V			10	μA	
Reset input current	I_{IR}	V_{CC}=5.25V, V_{RL}=0V			−50	μA	
Supply current	I_{CC}			12		mA	



Test load 1



TTL external clock interface circuit

■ AC Characteristics

The SM-803 is compatible with the Z8-01 as to the AC characteristics. Refer back to the Z8-01 description.

■ New Functions

The SM-802 has two standby modes ; HALT and STOP.

(1) HALT mode

The HALT mode is introduced by decoding a HALT instruction ($FF7F_H$). In this mode, the oscillation circuit is kept in operation, but no system clock is internally supplied any more.

So there is no power consumption now. This mode is cleared by a reset input, port 3 input, or timer interrupt at a mask option (designated at the time of ROM input).

(2) STOP mode

The STOP mode is brought by decoding a STOP instruction ($FF6F_H$).

SM-812 CMOS 8-Bit 1-Chip Microcomputer

■ Description

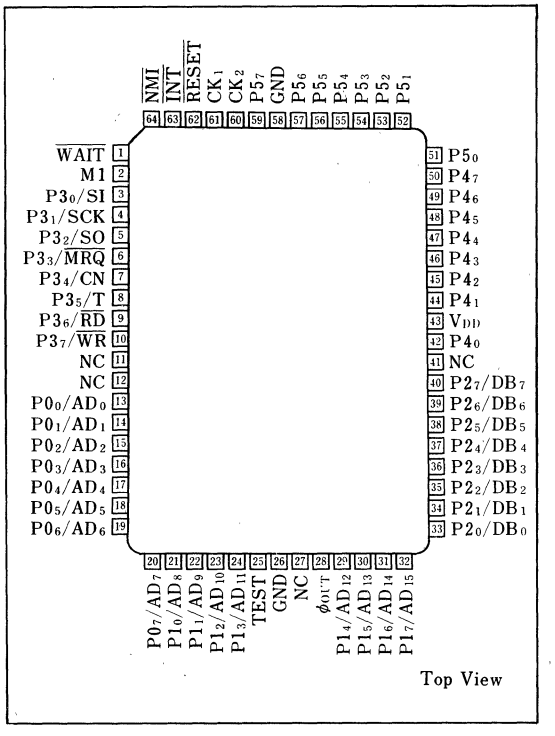
The SM-812 is an 8-bit single chip CMOS microcomputer with 2,048-byte of ROM, 128-byte of RAM, timer/counter and multiplex interrupt capability.

It is best suited to high-function controllers due to its single power supply and high-speed processing capability.

■ Features

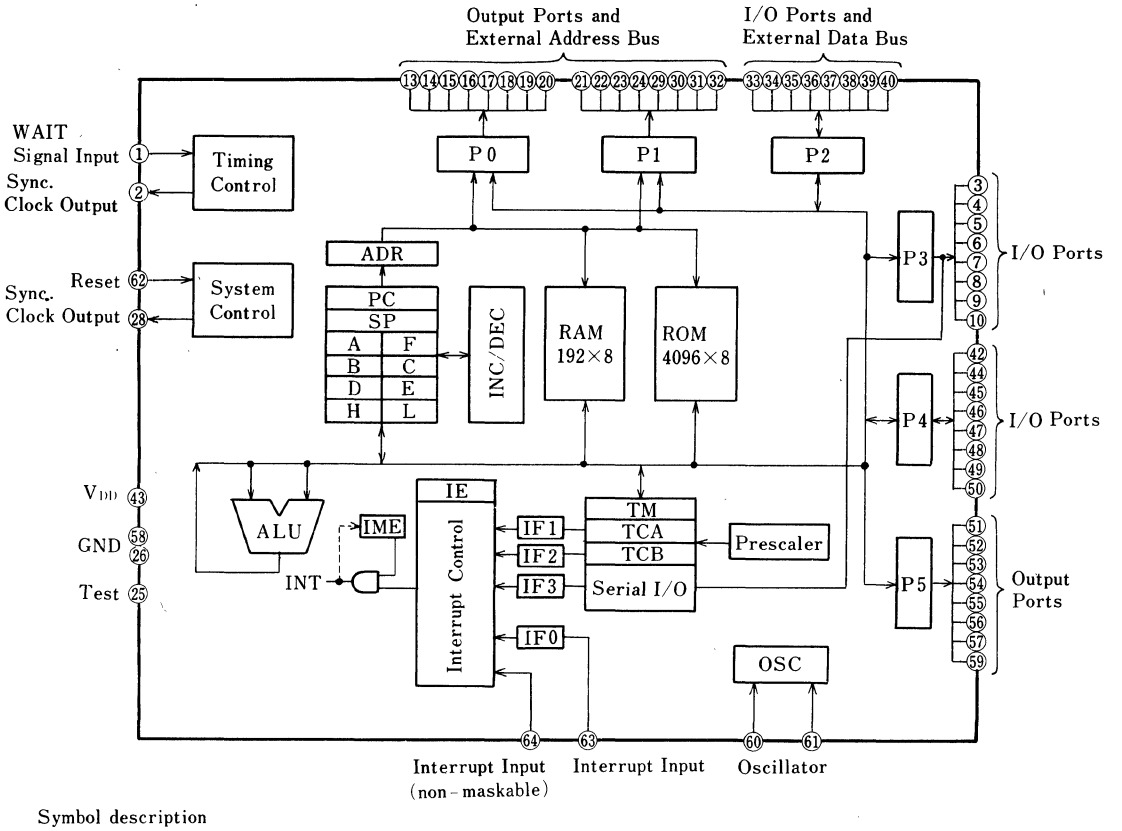
1. CMOS process
2. ROM capacity 2,048×8 bits
3. RAM capacity 128×8 bits
4. 64-byte (MAX.) of address space
5. Instructions 81
6. Subroutine nesting using RAM area
7. Output ports 32 bits
8. Input/Output ports 16 bits
9. Timer/counter
   - 8 bit counter 2
   - 8 bit prescaler 1
10. Interrupt function
    - External interrupt 1
    - Serial I/O interrupt 1
    - Timer interrupts 2
    - Non-maskable interrupt 1
11. Serial interface 8 bits
12. Standby mode (HALT mode, STOP mode)
13. Single power supply (2.7～5.5V)
14. Instruction cycle 1 μs(MIN.)
15. 64-pin quad-flat package

■ Pin Connections



Top View

Block Diagram



Symbol description

ADR	: Address latch	TM	: Timer modular register
ALU	: Arithmetic logic unit	TAC, TCB	: Timer counter
PC	: Program counter	IE	: Interrupt enable F/F
SP	: Stack pointer	IME	: Interrupt master enable F/F
F	: Flag register	IF0~IF3	: Interrupt request register
A, B, C, D, E, H, L	: General-purpose registers	OSC	: System clock oscillator
INC/DEC	: Incrementer/decrementer	P0~P5	: Port register

■ Pin Description

Pin	I/O	Circtit	Function	
$P4_0 \sim P4_7$	I/O	Pull-up	Programmable for I/O in bits	
$P2_0/DB_0 \sim P2_7/DB_7$	Bidirectional	Pull-up at input	I/O in bytes	External memory data bus signal
$P0_0/AD_0 \sim P1_7/AD_{15}$	O		Output in bytes	External memory address signal
$P3_0$/SI	O/I	Pull-up at input		Serial data input
$P3_1$/SCK	O/Bidirectional	Pull-up at input		Serial clock input/output
$P3_2$/SO	O			Serial data output
$P3_3/\overline{MRQ}$	O		Output in bytes	Memory request output
$P3_4$/CN	O/I	Pull-up at input		Timer counter input
$P3_5$/T	O			Counter signal output
$P3_6/\overline{RD}$	O			Read signal output
$P3_7/\overline{WR}$	O			Write signal output
$P5_0 \sim P5_7$	O	Pull-up	Settable/resettable in bits	
$\overline{WAIT}$	I	Pull-up	Used to prolong an access time for external memory or to clear the standby mode.	
$\overline{INT}$	I	Pull-up	Maskable interrupt request	
$\overline{NMI}$	I	Pull-up	Non-maskable interrupt request	
$\overline{RESET}$	I	Pull-up	Auto clear	
TEST	I		For testing (usually connected to GND)	
ϕ_{OUT}, M1	O		Synchronization clock output	
CK_1, CK_2			For clock oscillator	
V_{DD}, GND			Logic circuit power supply	

SM-813 CMOS 8-Bit 1-Chip Microcomputer

■ Description

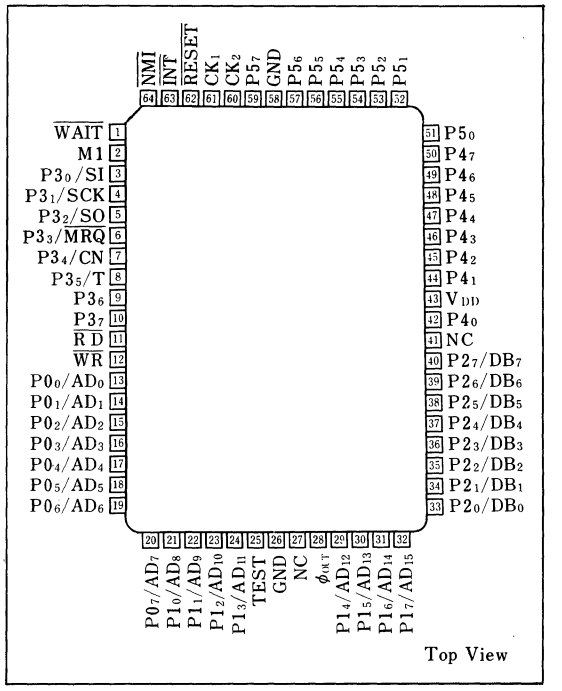
The SM-813 is an 8-bit single chip CMOS microcomputer with 4,096-byte of ROM, 192-byte of RAM, timer/counter and multiplex interrupt capability.

It is best suited to high-function controllers due to its single power supply and high-speed processing capability.

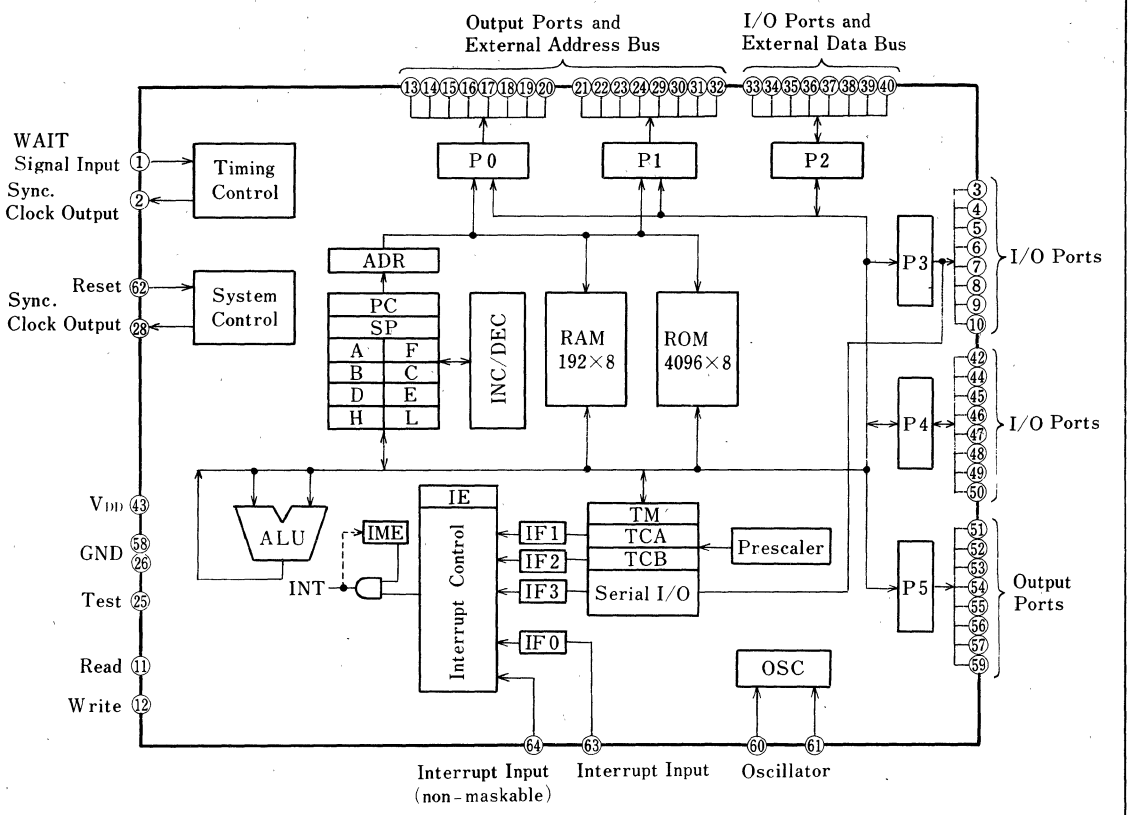
■ Features

1. CMOS process
2. ROM capacity 4,096×8 bits
3. RAM capacity 192×8 bits
4. 64K-byte (MAX.) of address space
5. Instructions 81
6. Subroutine nesting using RAM area
7. Output ports 16 bits
9. Timer/counters
   - 8-bit counters 2
   - 8-bit prescaler 1
10. Interrupt function
    - External interrupt 1
    - Serial I/O interrupt 1
    - Timer interrupt 2
    - Non-maskable interrupt 1
11. Serial interface 8 bits
12. Standby mode (HALT mode, STOP mode)
13. Single power supply (2.7～5.5V)
14. Instruction cycle 1 μs (MIN.)
15. 64-pin quad-flat package

■ Pin Connections



Block Diagram



Symbol description

ADR	: Address latch	TM	: Timer modular register
ALU	: Arithmetic logic unit	TAC, TCB	: Timer counter
PC	: Program counter	IE	: Interrupt enable F/F
SP	: Stack pointer	IME	: Interrupt master enable F/F
F	: Flag register	IF0~IF3	: Interrupt request register
A, B, C, D, E, H, L	: General-purpose registers	OSC	: System clock oscillator
INC/DEC	: Incrementer/decrementer	P0~P5	: Port register

■ Pin Description

Pin	I/O	Circtit	Function	
$P4_0$~$P4_7$	I/O	Pull-up	Programmable for I/O in bits	
$P2_0/DB_0$~ $P2_7/DB_7$	I/O	Pull-up at input	I/O in bytes	External memory data bus signal
$P0_0/AD_0$ ~$P1_7/AD_{15}$	O		Output in bytes	External memory address signal
$P3_0$/SI	O/I	Pull-up at input		Serial data input
$P3_1$/SCK	O/Bidirectional	Pull-up at input		Serial clock input/output
$P3_2$/SO	O			Serial data output
$P3_3/\overline{MRQ}$	O		Output in bytes	Memory output
$P3_4$/CN	O/I	Pull-up at input		Timer counter input
$P3_5$/T	O			Counter signal output
$P3_6$	O			
$P3_7$	O			
$P5_0$~$P5_7$	O	Pull-up	Settable/resettable in bits	
$\overline{RD}$	O		Read signal for external memory	
$\overline{WR}$	O		Write signal for external memory	
$\overline{WAIT}$	I	Pull-up	Used to prolong an access time for external memory or to clear the standby mode.	
$\overline{INT}$	I	Pull-up	Maskable interrupt request	
$\overline{NMI}$	I	Pull-up	Non-maskable interrupt request	
$\overline{RESET}$	I	Pull-up	Auto clear	
TEST	I		For testing (usually connected to GND)	
ϕ_{OUT}, M1	O		Synchronization clock output	
CK_1, CK_2			For clock oscillation	
V_{DD}, GND			Logic circuit power supply	

LU810V1 CMOS 8-Bit 1-Chip Microcomputer

■ Description

LU810V1, eliminating the internal ROM from SM-812, is the ROM less version of SM-812 and it uses Port 0 and Port 1 exclusively as the address bus and Port 2 as the data bus. Other functions are compatible with those of SM-812.

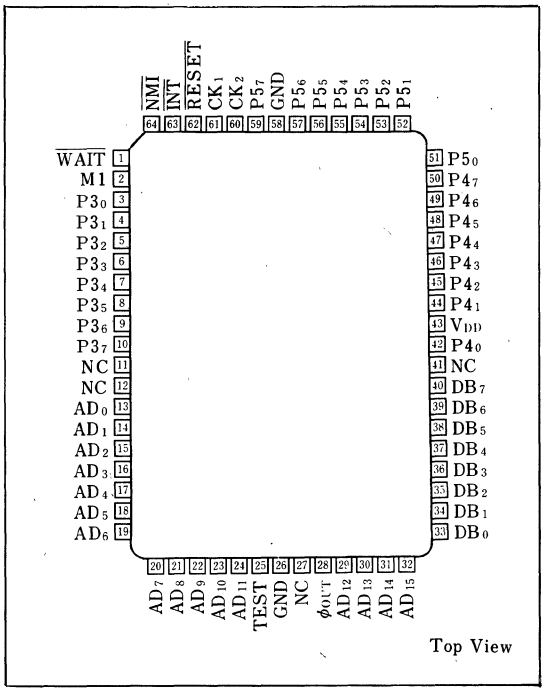
■ Features

1. CMOS process
2. ROM capacity 128×8 bits
3. 64K-byte (MAX.) of address space
4. Instructions 81
5. Subroutine nesting using RAM area
6. Output ports 16 bits
7. Input/Output ports 8 bits
8. Timer/counter
   - 8-bit counters 2
   - 8-bit prescaler 1
9. Interrupt function

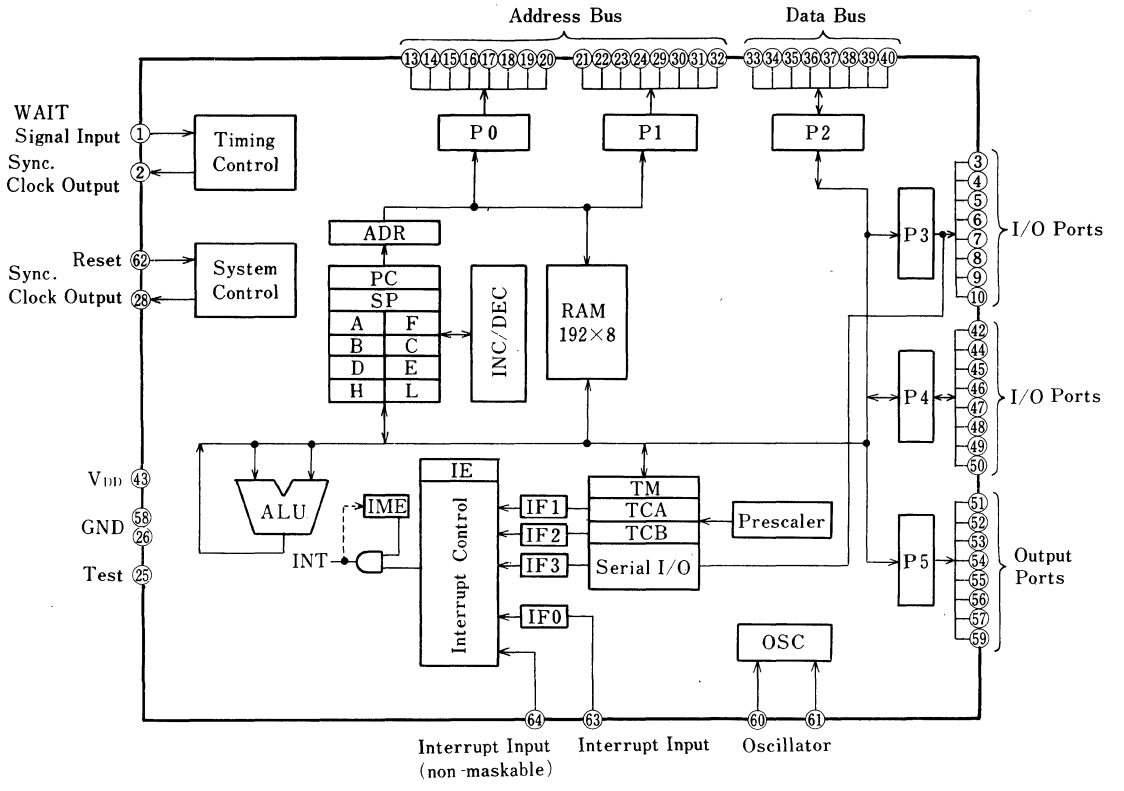
External interrupt	1
Serial I/O interrupt	1
Timer interrupts	2
Non-maskable interrupt	1

10. Serial interface 8 bits
11. Standby mode (HALT mode, STOP mode)
12. Single power supply (2.7～5.5V)
13. Instruction cycle 1 μs(MIN.)
14. 64-pin quad-flat package

■ Pin Connections



■ Block Diagram



Symbol description

ADR	: Address latch	TM	: Timer modular register
ALU	: Arithmetic logic unit	TAC, TCB	: Timer counter
PC	: Program counter	IE	: Interrupt enable F/F
SP	: Stack pointer	IME	: Interrupt master enable F/F
F	: Flag register	IF0~IF3	: Interrupt request register
A, B, C, D, E, H, L	: General-pupose registers	OSC	: System clock oscillator
INC/DEC	: Incrementer/decrementer	P0~P5	: Port register

■ Pin Description

Pin	I/O	Circtit	Function	
$P4_0$~$P4_7$	I/O	Pull up	Programmable for I/O in bits	
DB_0~DB_7	I/O	Pull up at input	I/O in bytes	External memory data bus signal
AD_0~AD_{15}	O		Output in bytes	External memory address signal
$P3_0$/SI	O/I	Pull up at input		Serial data input
$P3_1$/SCK	O/I	Pull up at input		Serial clock input/output
$P3_2$/SO	O			Serial data output
$P3_3$/$\overline{MRQ}$	O		Output in bytes	Memory request output
$P3_4$/CN	O/I	Pull up at input		Timer counter input
$P3_5$/T	O			Counter signal output
$P3_6$/$\overline{RD}$	O			Read signal output
$P3_7$/$\overline{WR}$	O			Write signal output
$P5_0$~$P5_7$	O	Pull up	Settable/resettable in bits	
$\overline{WAIT}$	I	Pull up	Used to prolong an access time for external memory or to clear the standby mode.	
$\overline{INT}$	I	Pull up	Maskable interrupt request	
$\overline{NMI}$	I	Pull up	Non-maskable interrupt request	
$\overline{RESET}$	I	Pull up	Auto clear	
TEST	I		For testing (usually connected to GND)	
ϕ_{OUT}, M1	O		Synchronization clock output	
CK_1, CK_2			For clock oscillation	
V_{DD}, GND			Logic circuit power supply	

Z8 Series Ordering Information

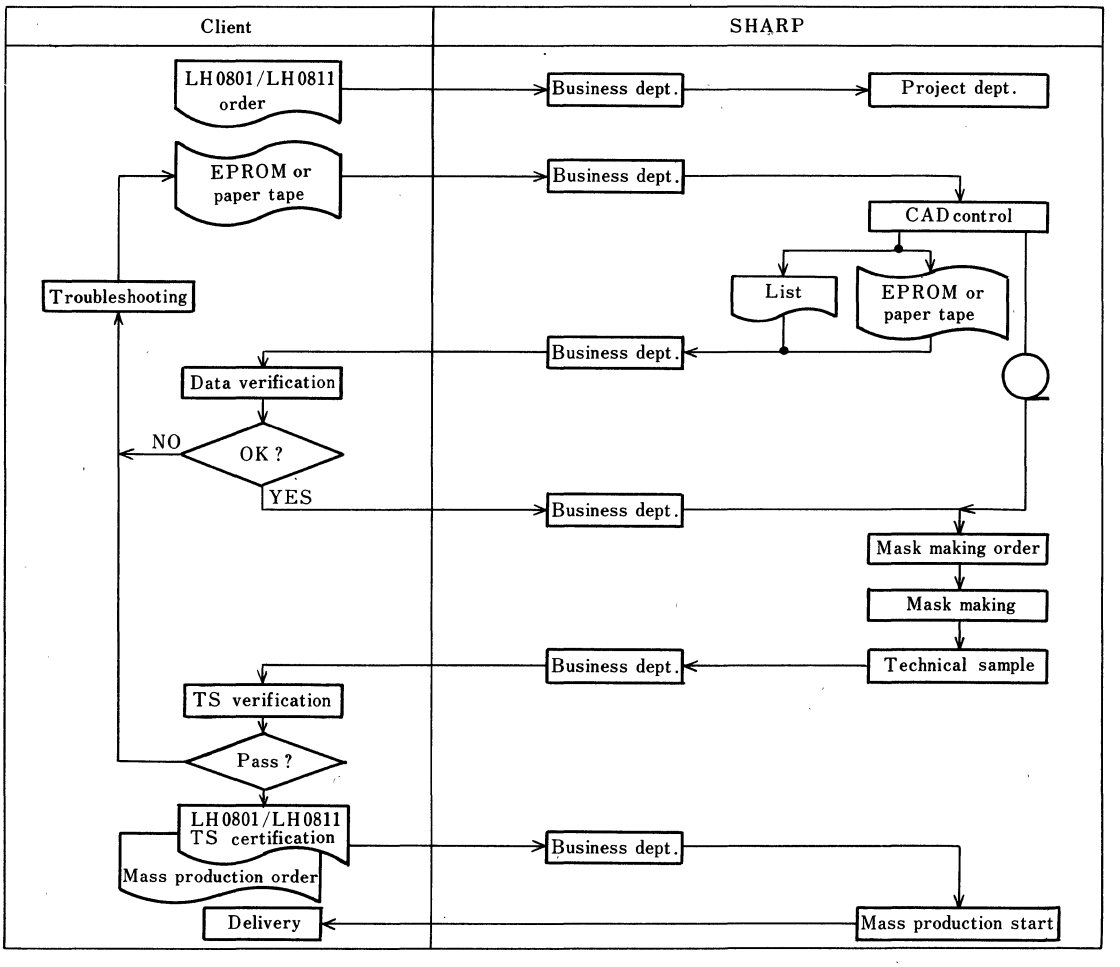
Below is discussed how to order the Z8 series products.

Customers are requested to submit an EPROM or paper tape as the ROM data media. The following information should be attached in any form and any means.

(1) ROM data media
(2) Specific data (chip select, marking, and other information)
(3) Your company's name, your own name, and stamp
(4) Ordering date

When submitting the ROM drawings, two sets of ROM data media are also required together with a list of ROM to see if the read-out data are correct.

With the ROM data media, we computer-aided-design a ROM masking magnetic tape and make up EPROM or paper tapes, and their list, in order to make sure the designed ROM data are correct. These materials are then checked up by the customer for approval. If it is okay, we start masking and make some technical evaluation samples (TS), which are delivered to the customer. When the samples are accepted, the customer will send us a "TS Confirmation". By a mass-production order at the moment or later, we will start producing the product in large quantities.



8-Bit Microprocessor and Peripheral LSIs

LH0080/LH0080A/LH0080B

Z80/Z80A/Z80B Central Processing Unit

■ Description

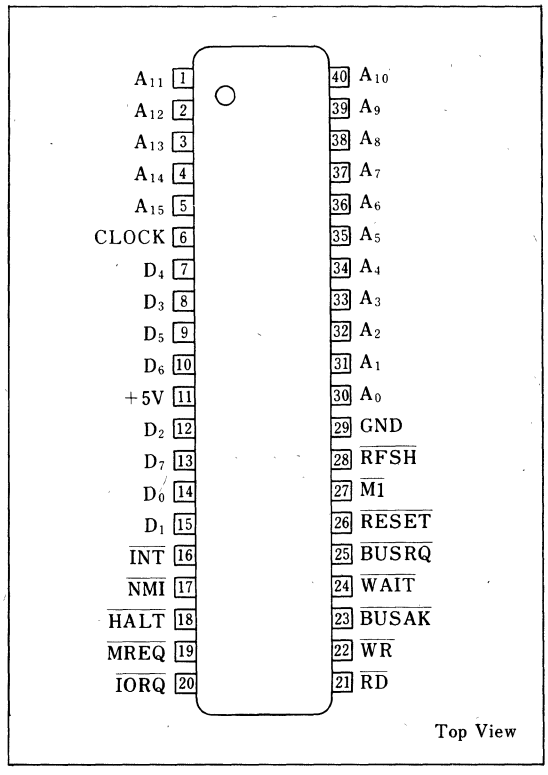
The Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

The LH0080 Z80 CPU (Z80 CPU for short below) is the third generation microprocessor implemented using an N-channel silicon-gate process.

The Z80 CPU is designed for using the standard memory components, higher system throughput and more efficient memory utilization. In addition, the output signals of the Z80 CPU is decoded to control peripherals. The Z80 CPU requires only single +5V DC power supply and single phase clock, therefore it is easy for the Z80 CPU to implement into a system.

The LH0080A Z80A and LH0080B Z80B CPU are the high speed version which can operate at the 4MHz and 6MHz system clock, respectively.

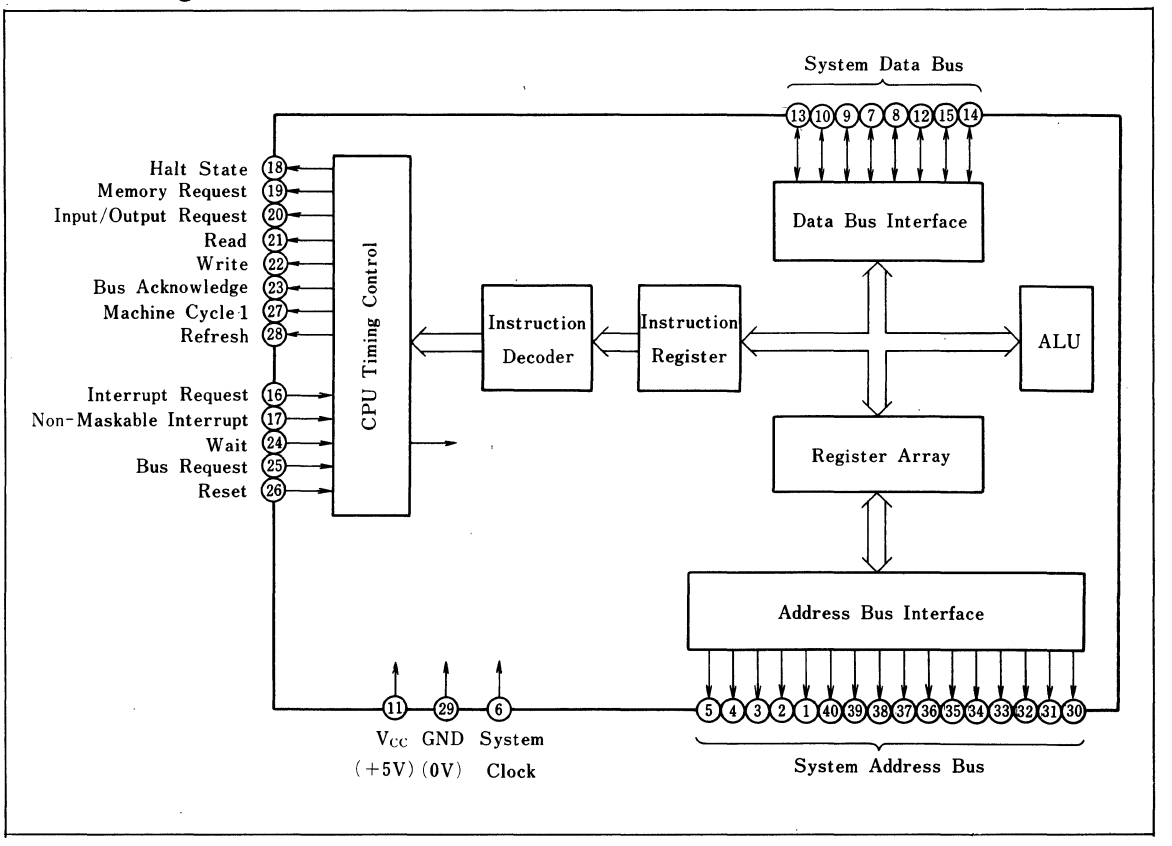
■ Pin Connections



■ Features

1. 8-bit parallel processing single-chip microprocessor
2. N-channel silicon-gate process
3. 158 instructions (The instruction of the 8080A are included as a subset ; 8080A software compatibility is maintained)
4. 22 registers
5. The capability of 3 modes maskable interrupt and non-maskable interrupt
6. On-chip dynamic memory refresh counter
7. Instruction fetch cycle : 1.6 μs(Z80), 1.0 μs (Z80A), 0.67 μs(Z80B)
8. Single+5V power supply and single phase clock
9. All inputs and outputs fully TTL compatible
10. 40-pin dual-in-line package

Block Diagram



■ Pin Description

Pin	Meaning	I/O	Function
A_0~A_{15}	Address bus	3-state O	System address bus
D_0~D_7	Data bus	Bidirectional 3-state	System data bus
$\overline{M1}$	Machine cycle one	O	Active "Low". Indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.
$\overline{MREQ}$	Memory request	3-state O	Active "Low". Indicates that the address bus holds a valid address for a memory read or memory write operation.
$\overline{IORQ}$	I/O request	3-state O	Active "Low". Indicates that the lower 8 bits of the address bus holds a valid I/O address for an I/O read or write operation. Also generated concurrently with $\overline{M1}$ during an interrupt acknowledge cycle to indicate an interrupt response.
$\overline{RD}$	Memory read	3-state O	Active "Low". Indicates that the CPU wants to read data from memory or an I/O device.
$\overline{WR}$	Memory write	3-state O	Active "Low". Indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.
$\overline{RFSH}$	Refresh	O	Active "Low". Indicates that the lower 7 bits of the system address bus can be used as a refresh address to the system's dynamic memories. Together with $\overline{MREQ}$ at "Low".
$\overline{HALT}$	Halt state	O	Active "Low". Indicates that a Halt instruction is being executed. While halted, the CPU executes NOPs to maintain memory refresh. The Halt state is cleared with $\overline{RESET}$, $\overline{NMI}$, or $\overline{INT}$ (when allowed).
$\overline{WAIT}$	Wait	I	Active "Low". Indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a wait state as long as this signal is active.
$\overline{INT}$	Maskable interrupt request	I	Active "Low". Generated by I/O devices. The CPU honors a request at the end of the current instruction if the interrupt enable flip-flop is enabled.
$\overline{NMI}$	Non-maskable interrupt request	I	Active "Low". Has a higher priority than $\overline{INT}$. Always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. Automatically forces the Z80 CPU to restart at location 0066H.
$\overline{RESET}$	Reset	I	Active "Low". Resets the interrupt enable flip-flop, the program counter interrupt vector register and the memory refresh register, and sets the interrupt status to Mode O, in order to initialize the CPU.
$\overline{BUSRQ}$	Bus request	I	Active "Low". Has a higher priority than NMI. Always recognized at the end of the current machine cycle. Activated to allow a bus master other than the CPU to control the system bus.
$\overline{BUSAK}$	Bus acknowledge	O	Active "Low". Indicates to the requesting device that the external circuitry can control the system bus.
CLOCK	System clock	I	Inputs +5V single-phase clock.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7.0	V
Output voltage	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

All ac parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for address and control lines.

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Clock input low voltage	V_{ILC}			−0.3		0.45	V
Clock input high voltage	V_{IHC}			V_{CC}−0.6		V_{CC}+0.3	V
Input low voltage	V_{IL}			−0.3		0.8	V
Input high voltage	V_{IH}			2.0		V_{CC}	V
Output low voltage	V_{OL}	I_{OL}=1.8mA				0.4	V
Output high voltage	V_{OH}	I_{OH}=−250 μA		2.4			V
Current consumption	I_{CC}		Z80 CPU			150	mA
			Z80A CPU			200	mA
			Z80B CPU			200	mA
Input leakage current	$\lvert I_{LI} \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$				10	μA
3-state output leakage current in float	$\lvert I_{LEAK} \rvert$	V_{OUT}=0.4V～V_{CC}				10	μA

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground			35	pF
Input capacitance	C_{IN}				5	pF
Output capacitance	C_{OUT}				10	pF

■ AC Characteristics

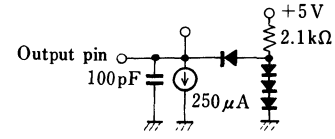
(V_{CC}=5V±5%, Ta=0～+70℃)

No.	Parameter	Symbol	Z80 CPU		Z80A CPU		Z80B CPU*		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
1	Clock cycle time	TcC	400*		250*		165*		ns
2	Clock pulse width (High)	TwCh	180*		110*		65*		ns
3	Clock pulse width (Low)	TwCl	180	2000	110	2000	65	2000	ns
4	Clock fall time	TfC		30		30		20	ns
5	Clock rise time	TrC		30		30		20	ns
6	Clock ↑ to address valid delay	TdCr (A)		145		110		90	ns
7	Address valid to $\overline{MREQ}$ ↓ delay	TdA (MREQf)	125*		65*		35*		ns
8	Clock ↓ to $\overline{MREQ}$ ↓ delay	TdCf (MREQf)		100		85		70	ns
9	Clock ↑ to $\overline{MREQ}$ ↑ delay	TdCr (MREQr)		100		85		70	ns
10	$\overline{MREQ}$ pulse width (High)	TwMREQh	170*		110*		65*		ns
11	$\overline{MREQ}$ pulse width (Low)	TwMREQ1	360*		220*		135*		ns
12	Clock ↓ to $\overline{MREQ}$ ↑ delay	TdCf (MREQr)		100		85		70	ns
13	Clock ↓ to $\overline{RD}$ ↓ delay	TdCf (RDf)		130		95		80	ns
14	Clock ↑ to $\overline{RD}$ ↑ delay	TdCr (RDr)		100		85		70	ns
15	Data setup time to clock ↑	TsD (Cr)	50		35		30		ns
16	Data hold time from $\overline{RD}$ ↑	ThD (RDr)	0		0		0		ns
17	$\overline{WAIT}$ setup time to clock ↓	TsWAIT (Cf)	70		70		60		ns
18	$\overline{WAIT}$ hold time after clock ↓	ThWAIT (Cf)	0		0		0		ns
19	Clock ↑ to $\overline{M1}$ ↓ delay	TdCr (Mlf)		130		100		80	ns
20	Clock ↑ to $\overline{M1}$ ↑ delay	TdCr (Mlr)		130		100		80	ns
21	Clock ↑ to $\overline{RFSH}$ ↓ delay	TdCr (RFSHf)		180		130		110	ns
22	Clock ↑ to $\overline{RFSH}$ ↑ delay	TdCr (RFSHr)		150		120		100	ns
23	Clock ↓ to $\overline{RD}$ ↑ delay	TdCf (RDr)		110		85		70	ns
24	Clock ↑ to $\overline{RD}$ ↓ delay	TdCr (RDf)		100		85		70	ns
25	Data Setup to clock ↑ during M_2, M_3, M_4 or M_5 cycles	TsD (Cf)	60		50		40		ns
26	Address stable prior to $\overline{IORQ}$ ↓	TdA (IORQf)	320*		180*		110*		ns
27	Clock ↑ to $\overline{IORQ}$ ↓ delay	TdCr (IORQf)		90		75		65	ns
28	Clock ↓ to $\overline{IORQ}$ ↑ delay	TdCf (IORQr)		110		85		70	ns
29	Data stable prior to $\overline{WR}$ ↓	TdDm (WRf)	190*		80*		25*		ns
30	Clock ↓ to $\overline{WR}$ ↓ delay	TdCf (WRf)		90		80		70	ns
31	$\overline{WR}$ pulse width	TwWR	360*		220*		135*		ns
32	Clock ↓ to $\overline{WR}$ ↑ delay	TdCf (WRr)		100		80		70	ns
33	Data stable prior to $\overline{WR}$ ↓	TdDi (WRf)	20*		−10*		−55*		ns
34	Clock ↑ to $\overline{WR}$ ↓ delay	TdCr (WRf)		80		65		60	ns
35	Data stable from $\overline{WR}$ ↑	TdWRr (D)	120*		60*		30*		ns
36	Clock ↓ to $\overline{HALT}$ ↑ or ↓	TdCf (HALT)		300		300		260	ns
37	$\overline{NMI}$ pulse width	TwNMI	80		80		70		ns
38	$\overline{BUSREQ}$ setup time to clock ↑	TsBUSRQ (Cr)	80		50		50		ns
39	$\overline{BUSREQ}$ hold time after clock ↑	ThBUSRQ (Cr)	0		0		0		ns
40	Clock ↑ to $\overline{BUSACK}$ ↓ delay	TdCr (BUSAKf)		120		100		90	ns
41	Clock ↓ to $\overline{BUSACK}$ ↑ delay	TdCf (BUSAKr)		110		100		90	ns
42	Clock ↑ to data float delay	TdCr (Dz)		90		90		80	ns
43	Clock ↑ to control output float delay ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$)	TdCr (CTz)		110		80		70	ns
44	Clock ↑ to address float delay	TdCr (Az)		110		90		80	ns
45	$\overline{MREQ}$ ↑, $\overline{IORQ}$ ↑, $\overline{RD}$ and $\overline{WR}$ ↑ to address hold time	TdCTr (A)	160*		80*		35*		ns

↑ Rising edge, ↓ Falling edge

No.	Parameter	Symbol	Z80 CPU		Z80A CPU		Z80B CPU*		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
46	$\overline{\text{RESET}}$ ↓ to clock ↑ setup time	TsRESET (Cr)	90		60		60		ns
47	$\overline{\text{RESET}}$ from clock ↑ hold time	ThRESET (Cr)	0		0		0		ns
48	$\overline{\text{INT}}$ to clock ↑ setup time	TsINTf (Cr)	80		80		70		ns
49	$\overline{\text{INT}}$ from clock ↑ hold time	ThINTr (Cr)	0		0		0		ns
50	$\overline{\text{M1}}$ ↓ to $\overline{\text{IORQ}}$ ↓ delay	TdM1f (IORQf)	920*		565*		365*		ns
51	Clock ↓ to $\overline{\text{IORQ}}$ ↓ delay	TdCf (IORQf)		110		85		70	ns
52	Clock ↑ to $\overline{\text{IORQ}}$ ↑ delay	TdCf (IORQr)		100		85		70	ns
53	Clock ↓ to data valid delay	TdCf (D)		230		150		130	ns

All ac parameters assume a load capacitance of 100 pF. Add 10 μs delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for address and control lines.
*For clock periods other than the minimums shown in the table, calculate parameters using the following expressions.
*All timings are preliminary and subject to change.



■ Footnotes to AC Characteristics

No.	Symbol	Z80	Z80A	Z80B
1	TcC	TwCh+TwCl+TrC+TfC	TwCh+TwCl+TrC+TfC	TwCh+TwCl+TrC+TfC
2	TwCh	MAX. 200 μs	MAX. 200 μs	MAX. 200 μs
7	TdA (MREQf)	TwCh+TfC−75	TwCh+TfC−65	TwCh+TfC−50
10	TwMREQh	TwCh+TfC−30	TwCh+TfC−20	TwCh+TfC−20
11	TwMREQl	TcC−40	TcC−30	TcC−30
26	TdA (IORQf)	TcC−80	TcC−70	TcC−55
29	TdD (WRf)	TcC−210	TcC−170	TcC−140
31	TwWR	TcC−40	TcC−30	TcC−30
33	TdD (WRf)	TwCl+TrC−180	TwCl+TrC−140	TwCl+TrC−140
35	TdWRr (D)	TwCl+TrC−80	TwCl+TrC−70	TwCl+TrC−55
45	TdCTr (A)	TwCl+TrC−40	TwCl+TrC−50	TwCl+TrC−50
50	TdMlf (IORQf)	2TcC+TwCh+TfC−80	2TcC+TwCh+TfC−65	2TcC+TwCh+TfC−50

AC Test Conditions :

$V_{IH}=2.0V$ $V_{IHC}=V_{CC}-0.6V$ $V_{OH}=2.0V$ FLOAT$=\pm0.5$
$V_{IL}=0.8V$ $V_{ILC}=0.45V$ $V_{OL}=0.8V$

■ CPU Timing

The Z80 CPU executes instructions by proceeding through a specific sequence of operations:

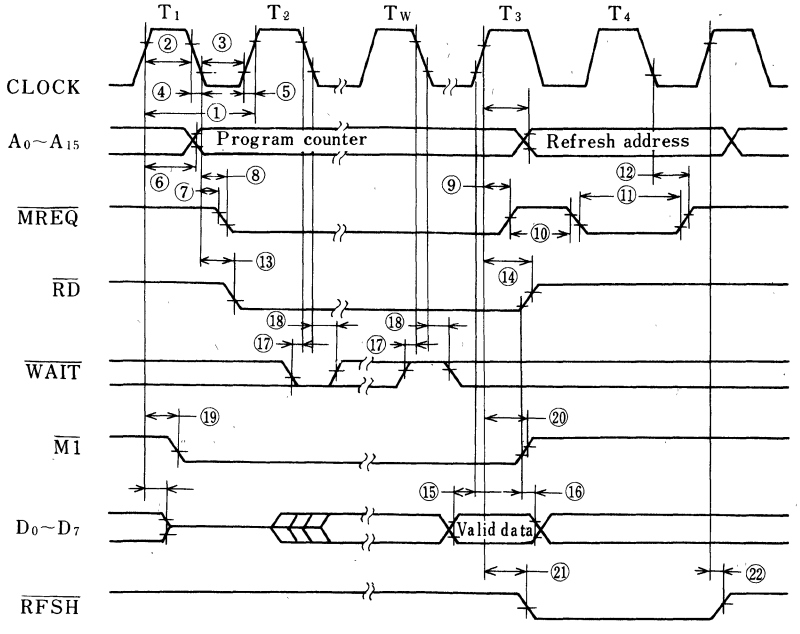
- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a T time or cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

(1) Instruction Opcode Fetch

The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Fig. 1). Approximately one-half clock cycle later, $\overline{MREQ}$ goes active. When active, $\overline{RD}$ indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the $\overline{WAIT}$ input with the falling edge of clock state T_2. During clock states T_3 and T_1 of an $\overline{M1}$ cycle dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction. When the Refresh Control signal becomes active, refreshing of dynamic memory can take place.



Note: T_W-Wait cycle added when necessary for slow ancilliary devices.

Fig. 1 Instruction opcode fetch

(2) Memory Read or Write Cycles

Fig. 2 shows the timing of memory read or write cycles other than an opcode fetch ($\overline{M1}$) cycle.
The $\overline{MREQ}$ and $\overline{RD}$ signals function exactly as in the fetch cycle. In a memory write cycle, MREQ also becomes active when the address bus is stable. The $\overline{WR}$ line is active when the data bus is stable, so that it can be used directly as an R/$\overline{W}$ pulse to most semiconductor memories.

(3) Input or Output Cycles

Fig. 3 shows the timing for an I/O read or I/O write operation.
During I/O operations, the CPU automatically inserts a single wait state (T_W). This extra wait state allows sufficient time for an I/O port to decode the address from the port address lines.

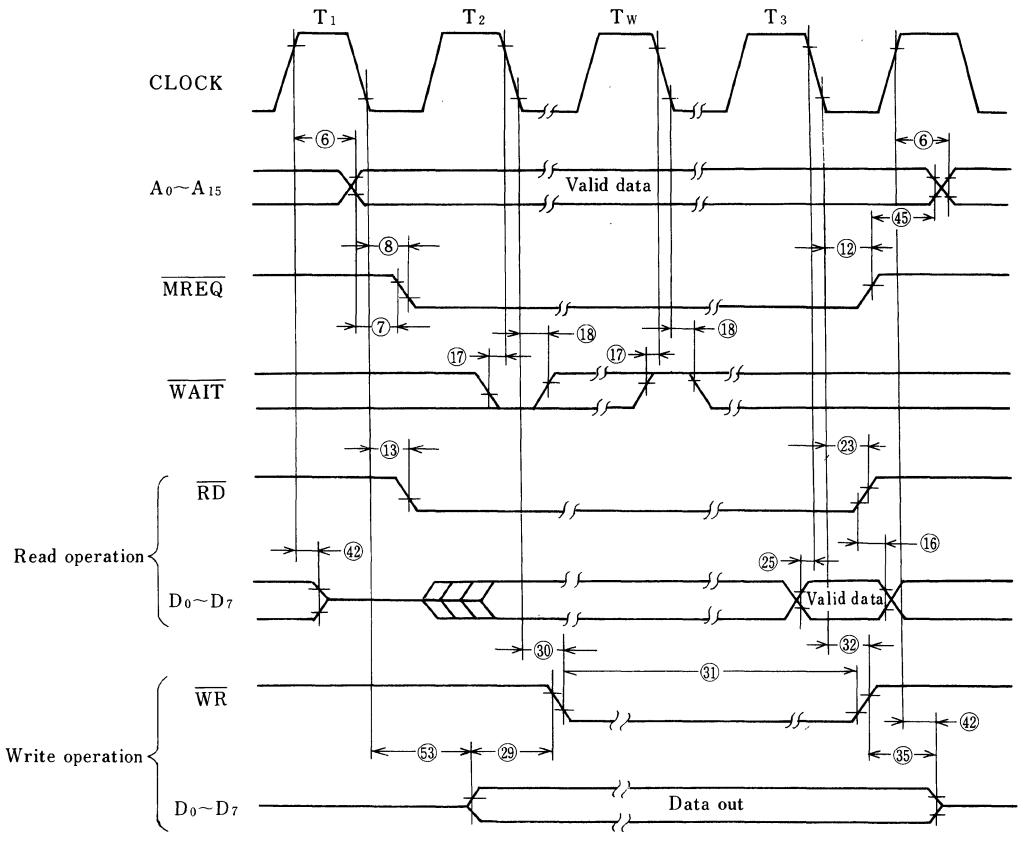
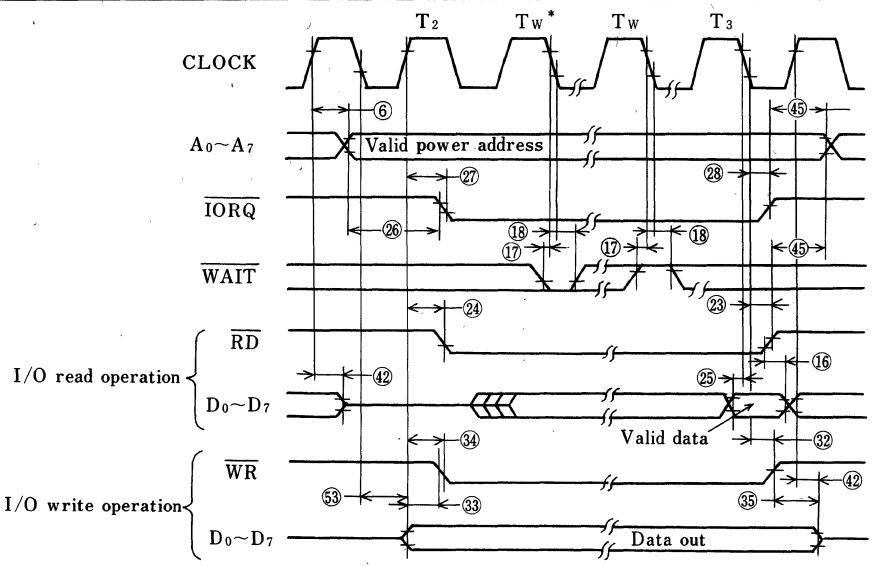


Fig. 2 Memory read or write cycles

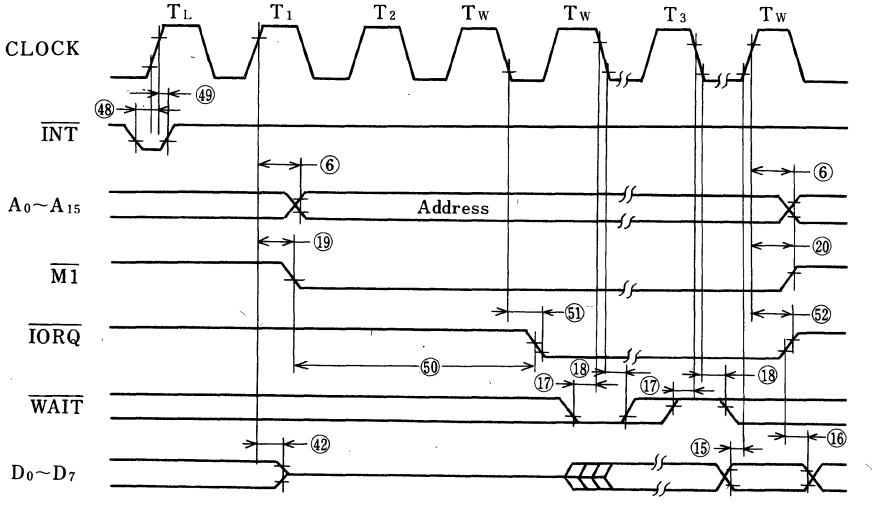


Note : Tw=One wait cycle automatically inserted by CPU.

Fig. 3 Input or output

(4) Interrupt request/acknowledge cycle

The CPU samples the interrupt signal with the rising edge of the last clock at the end of any instruction (Fig. 4). When an interrupt is accepted, a special M1 cycle is generated. During this M1 cycle, IORQ becomes active (instead of MREQ) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two wait states to this cycle.



Note 1 : TL=Last state of previous instruction.

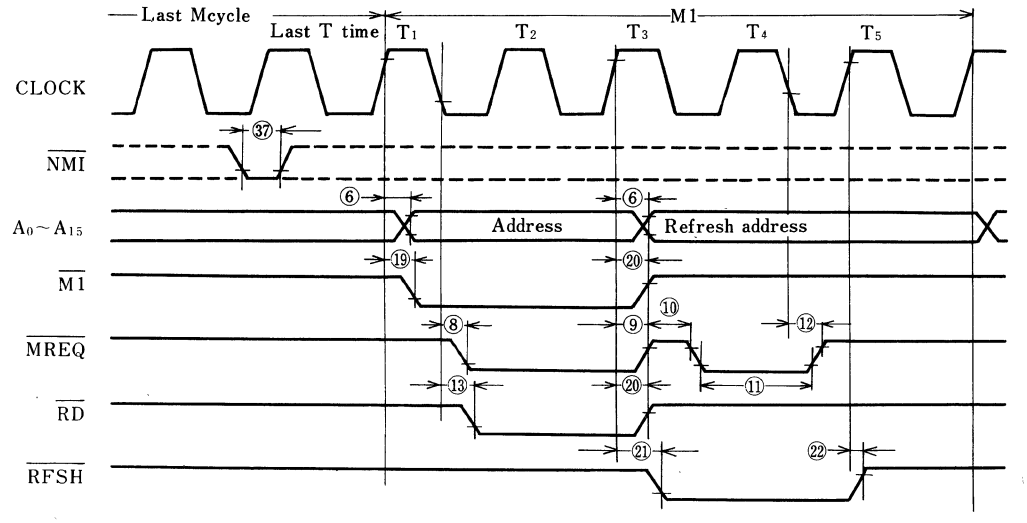
Note 2 : Two wait cycles automatically inserted by CPU (*).

Fig. 4 Interrupt request/acknowledge cycle

(5) Non-maskable interrupt request cycle

$\overline{NMI}$ is sampled at the same time as the maskable interrupt $\overline{INT}$ but has higher priority and cannot be disabled under software control.

The subsequent timing is similar to that of a normal instruction fetch except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the $\overline{NMI}$ service routine located at address 0066H (Fig. 5).



*Although $\overline{NMI}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{NMI}$'s falling edge must occur no later than rising edge of the clock cycle preceding T_{LAST}.

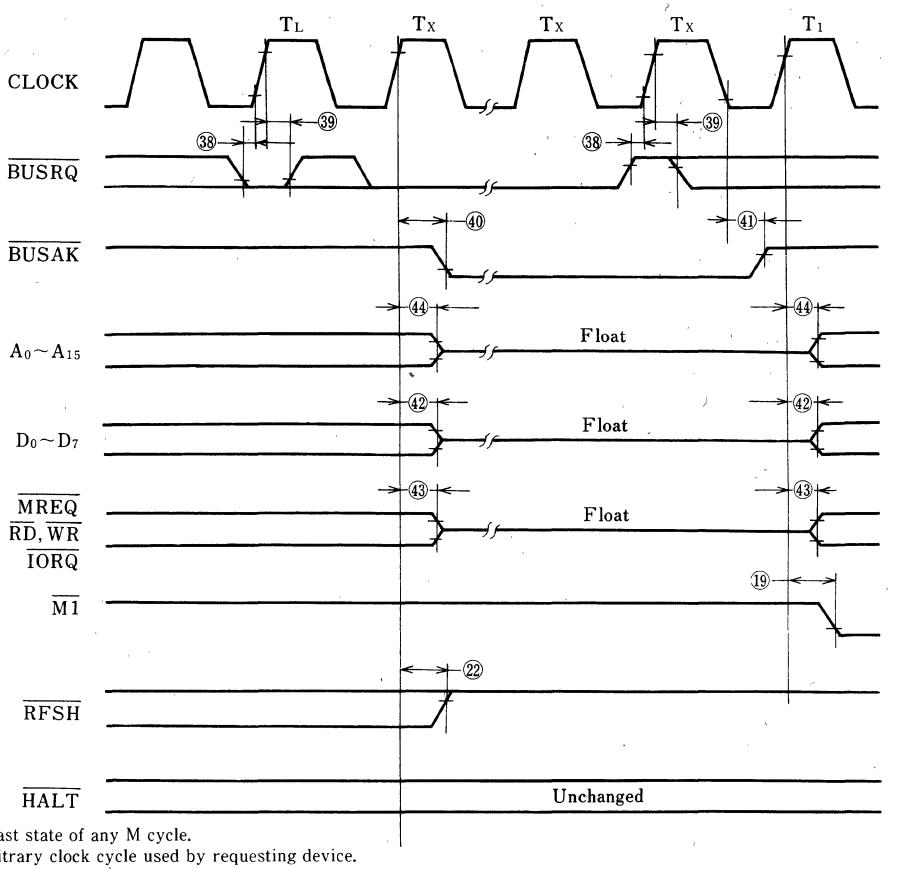
Fig. 5 Non-maskable interrupt request operation

(6) Bus request/acknowledge cycle

The CPU samples $\overline{BUSREQ}$ with the rising edge of the last clock period of any machine cycle (Fig. 6). If $\overline{BUSREQ}$ is active, the CPU sets its address, data, and $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ lines to a high-impedance state with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.

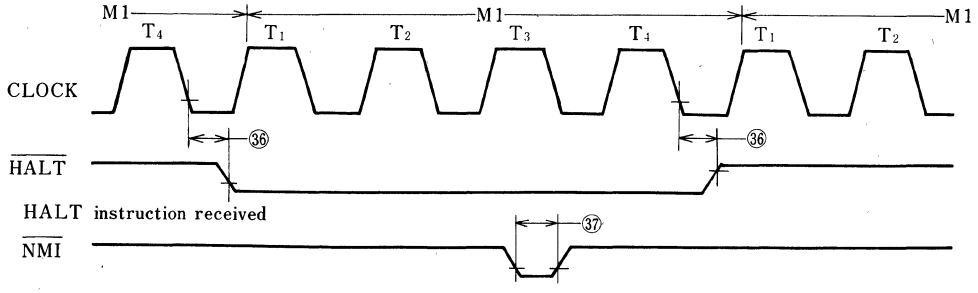
(7) Reset cycle

$\overline{RESET}$ must be active for at least three clock cycles for the CPU to properly accept it. As long as $\overline{RESET}$ remains active, the address and data buses float, and the control outputs are inactive. Once $\overline{RESET}$ goes inactive, three internal T cycles are consumed before the CPU resumes normal processing operation. $\overline{RESET}$ clears the PC register, so the first opcode fetch will be location 0000 (Fig. 8).



Note: TL=Last state of any M cycle.
TX=An arbitrary clock cycle used by requesting device.

Fig. 6 Z-bus request/acknowledge cycle



Note: INT will also force a Halt exit.

Fig. 7 Halt acknowledge cycle

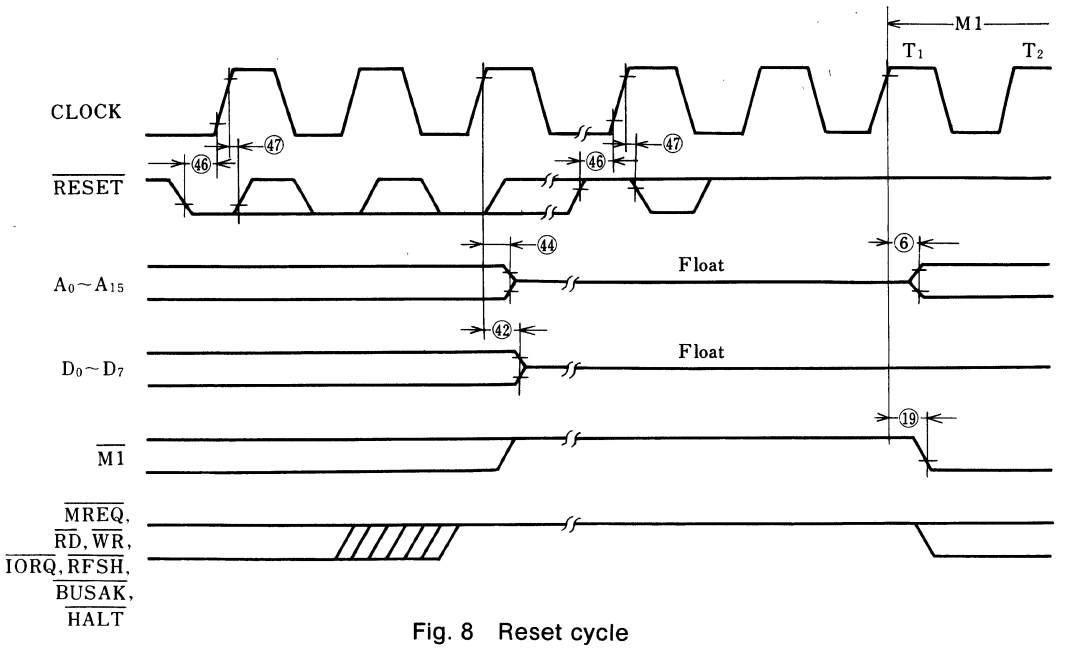


Fig. 8 Reset cycle

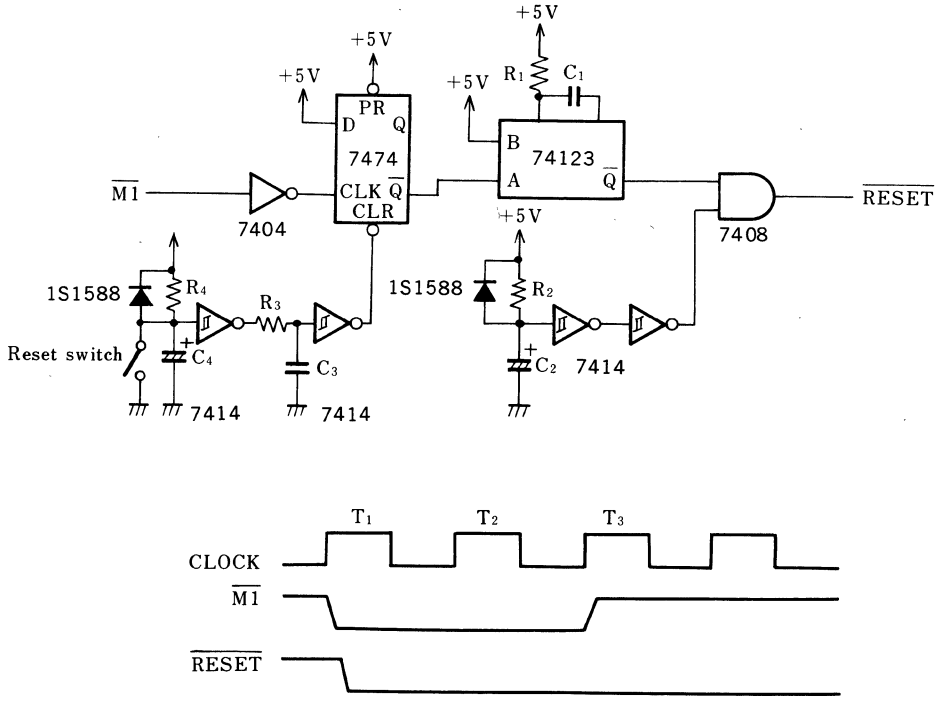


Fig. 9 Reset circuit and timing diagram when M1 cycle has no wait state

〈Reference circuit〉

The RAM contents may be adversely affected by resetting the CPU while it is in operation.

To prevent this, a $\overline{\text{RESET}}$ signal should be input in the following timings.

(1) No walt state in the M1 cycle

Input a $\overline{\text{RESET}}$ signal to start sampling this signal at the clock rising in the M1 cycle's T_2 state.

Fig. 9 shows a typical circuit generating such a $\overline{\text{RESET}}$ signal.

(2) A walt state in the M1 cycle

Input a $\overline{\text{RESET}}$ signal to start sampling this signal at the clock rising in the M1 cycle's T_3 state.

When a 1 walt state occurs, this type of $\overline{\text{RESET}}$ signal can be generated by the circuit diagrammed in Fig. 10. In the circuit shown in Fig. 2, no $\overline{\text{RESET}}$ signal is given during an interrupt acknowledge cycle.

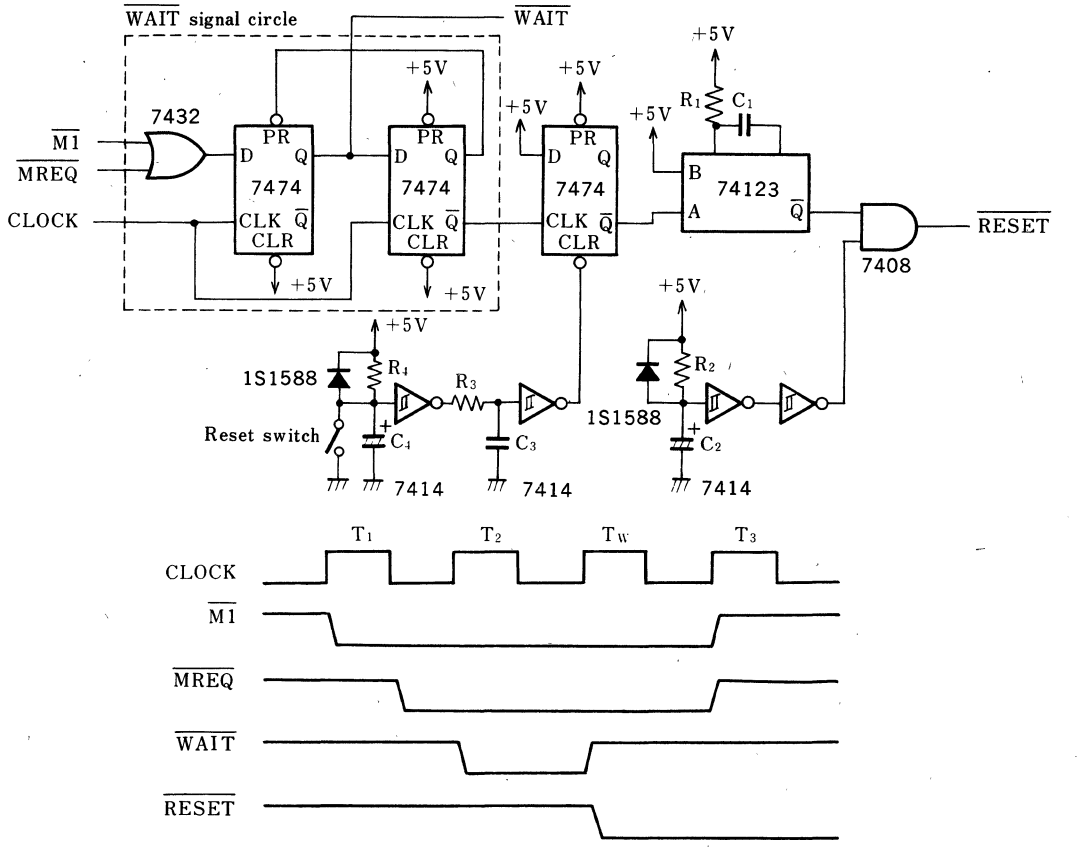


Fig. 10 Reset circuit and timing diagram when M1 cycle has a wait state

CPU Registers

A Accumulator	F Flag Register	A′ Accumulator	F′ Flag Register
B General Purpose	C General Purpose	B′ General Purpose	C′ General Purpose
D General Purpose	E General Purpose	D′ General Purpose	E′ General Purpose
H General Purpose	L General Purpose	H′ General Purpose	L′ General Purpose

← 8 bits →

I Interrupt Vector	R Memory Refresh
IX Index Register	
IY Index Register	
SP Stack pointer	
PC Program Counter	

← 16 bits →

Architecture

(1) CPU Registers

(i) **Program Counter (PC)** The program counter holds the 16 bits memory address of a current instruction. The CPU fetches the contents from memory address specified by the PC.

The PC feeds the data to the address line, automatically setting the PC value to +1. When a program jump takes place, a new value is directly set to the PC.

(ii) **Stack Pointer (SP)** The stack pointer holds the top 16-bit address of the stack with an external RAM. An external file is based on LIFO (Last-In, First-Out).

The data are transferred between a CPU-specified register and the stack by a PUSH or POP instruction. The last-pushed data are first popped from the stack.

(iii) **Index Register (IX & IY)** For index mode addressing, there are independent index registers IX and IY, each of which holds 16-bit reference address.

In the index mode, the index registers are used to designate the memory area for data input/output.

With an INDEX ADDRESSING instruction, an effective address comes by adding a one-byte displacement to the register content. This displacement is an integral signed two's complement number

(iv) **Interrupt Register (I)** The Z80 CPU has indirect subroutine call mode for any memory area according to an interrupt. For this purpose, this register stores the upper 8 bits of memory address for vectored interrupt processing and the lower 8 bits for the interrupting device.

(v) **Refresh Register (R)** The built-in refresh register provides user-transparent dynamic memory refresh. Its lower 7 bits are automatically incremented during each instruction fetch cycle.

While the CPU records a fetched instruction and executes the instruction, the refresh register data are placed on the address bus by a REFRESH control signal.

(vi) **Accumulator and Flag Register (A & F)** The CPU has also two independent 8-bit accumulators in combination with two 8-bit flag registers.

The accumulators store an operand or the results of an 8-bit operation. The flag registers, on the other hand, deal with the results of an 8-bit or 16-bit operation; for example, seeing if the result is equal to 0 or not.

(vii) **General-Purpose Registers** There are several pairs of general-purpose registers. In each pair, they can be used separately or as a 16-bit paired register. The paired registers are BC, DE, HL, as well as BC′ DE′ HL′. Either of these sets can work by an "Exchange" instruction at any time on a program.

(2) Arithmetic/Logical Unit (ALU)

An 8-bit arithmetic/logical operation instruction is executed by the ALU inside the CPU. The ALU connects to each register through the internal bus for data transfer between them.

(3) Instruction Register, CPU Control

Each instruction is read out of the memory, held in the instruction register, and decoded. The con-

trol unit controls this action and gives control signals necessary to read and write data from and to the registers.

The control unit also makes ALU control signal and other external control signals.

〈Interrupts : General Operation〉 The Z80 CPU accepts two interrupt input signals: $\overline{NMI}$ and $\overline{INT}$. The $\overline{NMI}$ is a non-maskable interrupt and has the highest priority. $\overline{INT}$ is a lower priority interrupt and it requires that interrupts be enabled in software in order to operate.

(1) Non-Maskable Interrupt ($\overline{NMI}$)

The non-maskable interrupt will be accepted at all times by the CPU.

After recognition of the $\overline{NMI}$ signal, the CPU jumps to restart location 0066H.

(2) Maskable Interrupt ($\overline{INT}$)

The maskable interrupt, $\overline{INT}$, has three programmable response modes available.

(i) **Mode 0 Interrupt Operation.** This mode is similar to the 8080A microprocessor interrupt service procedures. The interrupting device places an instruction on the data bus. This is a Restart instruction or a Call instruction.

(ii) **Mode 1 Interrupt Operation.** Mode 1 operation is very similar to that for the $\overline{NMI}$. The principal difference is that the Mode 1 interrupt has a restart location of 0038H only.

(iii) **Mode 2 Interrupt Operation.** This interrupt mode has been designed to utilize most effectively the capabilities of the Z80 microprocessor and its associated peripheral family. The interrupting peripheral device selects the starting address (16 bits) of the interrupt service routine. It does this by placing an 8-bit vector on the data bus during the interrupt acknowledge cycle. The CPU forms a pointer using this byte as the lower 8-bits and the contents of the I register as the upper 8-bits. This points to an entry in a table of addresses for interrupt service routines. The CPU then jumps to the routine at that address.

All the Z80 peripheral devices have the interrupt priority circuit with a daisy-chain configuration. During an interrupt acknowledge cycle, vectors are automatically fed. For more details, refer to the Z80 PIO description.

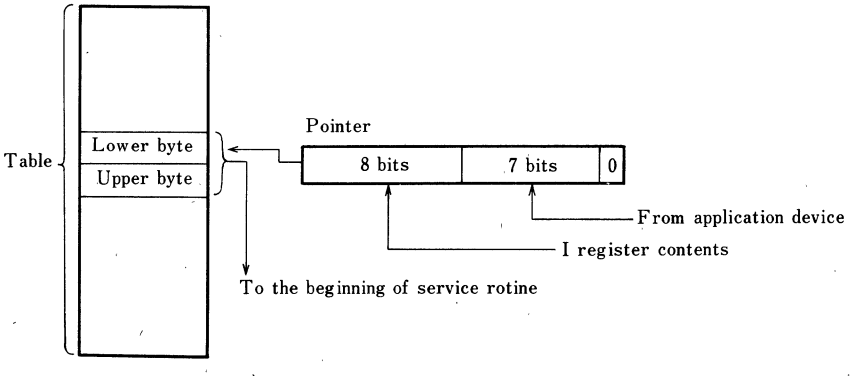


Fig. 1 Mode 2 interrupt diagram

Instruction Set

Table 1 8-bit load group

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	Flags C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD r, r′	r←r′	01 r r′	40+	●	●	●	●	●	●	1	1	4	
LD r, n	r←n	00 r 110 ← n →	06+	●	●	●	●	●	●	2	2	7	
LD r, (HL)	r← (HL)	01 r 110	46+	●	●	●	●	●	●	1	2	7	
LD r, (IX+d)	r← (IX+d)	11 011 101 01 r 110 ← d →	DD 46+	●	●	●	●	●	●	3	5	19	
LD r, (IY+d)	r← (IY+d)	11 111 101 01 r 110 ← d →	FD 46	●	●	●	●	●	●	3	5	19	
LD (HL), r	(HL)←r	01 110 r	70+	●	●	●	●	●	●	1	2	7	
LD (IX+d), r	(IX+d)←r	11 011 101 01 110 r ← d →	DD 70+	●	●	●	●	●	●	3	5	19	
LD (IY+d), r	(IY+d)←r	11 111 101 01 110 r ← d →	FD 70+	●	●	●	●	●	●	3	5	19	
LD (HL), n	(HL)←n	00 110 110 ← n →	36	●	●	●	●	●	●	2	3	10	
LD (IX+d), n	(IX+d)←n	11 011 101 00 110 110 ← d → ← n →	DD 36	●	●	●	●	●	●	4	5	19	
LD (IY+d), n	(IY+d)←n	11 111 101 00 110 110 ← d → ← n →	FD 36	●	●	●	●	●	●	4	5	19	
LD A, (BC)	A ← (BC)	00 001 010	0A	●	●	●	●	●	●	1	2	7	
LD A, (DE)	A ← (DE)	00 011 010	1A	●	●	●	●	●	●	1	2	7	
LD A, (nn)	A ← (nn)	00 111 010 ← n → ← n →	3A	●	●	●	●	●	●	3	4	13	
LD (BC), A	(BC) ← A	00 000 010	02	●	●	●	●	●	●	1	2	7	
LD (DE), A	(DE) ← A	00 010 010	12	●	●	●	●	●	●	1	2	7	
LD (nn), A	(nn) ← A	00 110 010 ← n → ← n →	32	●	●	●	●	●	●	3	4	13	
LD A, I	A ← I	11 101 101 01 010 111	ED 57	●	↕	IFF	↕	0	0	2	2	9	
LD A, R	A ← R	11 101 101 01 011 111	ED 5F	●	↕	IFF	↕	0	0	2	2	9	
LD I, A	I ← A	11 101 101 01 000 111	ED 47	●	●	●	●	●	●	2	2	9	
LD R, A	R ← A	11 101 101 01 001 111	ED 4F	●	●	●	●	●	●	2	2	9	

r,r	Reg.
000	B
001	C
010	D
011	E
100	H
101	L
111	A

Notes : r, r′ means any of the registers A, B, C, D, E, H, L, IFF the content of the interrupt enable flip-flop, (IFF) is copied into the P/V flag.
Flags : C (carry), Z (zero), S (sign), P/V (parity/overflow), H (half carry), N (add/substract).
: ● =unchanged, 0=reset, 1=set, X=undefined.
: ↕ set or reset according to the result of the operation.

Table 2 16-bit load group

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	Flags C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd, nn	dd ← nn	00 dd0 001 ← n → ← n →	01+	●	●	●	●	●	●	3	3	10	
LD IX, nn	IX ← nn	11 011 101 00 100 001 ← n → ← n →	DD 21	●	●	●	●	●	●	4	4	14	
LD IY, nn	IY ← nn	11 111 101 00 100 001 ← n → ← n →	FD 21	●	●	●	●	●	●	4	4	14	
LD HL, (nn)	H ← (nn+1) L ← (nn)	00 101 010 ← n → ← n →	2A	●	●	●	●	●	●	3	5	16	nn : 2-byte number. Lower byte just after opcode.
LD dd, (nn)	dd_H ← (nn+1) dd_L ← (nn)	11 101 101 01 dd1 011 ← n → ← n →	ED 4B+	●	●	●	●	●	●	4	6	20	Upper byte comes next.
LD IX, (nn)	IX_H ← (nn+1) IX_L ← (nn)	11 011 101 00 101 010 ← n → ← n →	DD 2A	●	●	●	●	●	●	4	6	20	
LD IY, (nn)	IY_H ← (nn+1) IY_L ← (nn)	11 111 101 00 101 010 ← n →	FD 2A	●	●	●	●	●	●	4	6	20	
LD (nn), HL	(nn+1) ← H (nn) ← L	00 100 010 ← n → ← n →	22	●	●	●	●	●	●	3	5	16	
LD (nn), dd	(nn+1) ← dd_H (nn) ← dd_L	11 101 101 01 dd0 011 ← n → ← n →	ED 43+	●	●	●	●	●	●	4	6	20	
LD (nn), IX	(nn+1)←IX_H (nn) ← IX_L	11 011 101 00 100 010 ← n → ← n →	DD 22	●	●	●	●	●	●	4	6	20	
LD (nn), IY	(nn+1)←IY_H (nn) ← IY_L	11 111 101 00 100 010 ← n → ← n →	FD 22	●	●	●	●	●	●	4	6	20	
LD SP, HL	SP ← HL	11 111 001	F9	●	●	●	●	●	●	1	1	6	
LD SP, IX	SP ← IX	11 011 101 11 111 001	DD F9	●	●	●	●	●	●	2	2	10	
LD SP, IY	SP ← IY	11 111 101 11 111 001	FD F9	●	●	●	●	●	●	2	2	10	
PUSH qq	(SP−2)←qq_L (SP−1)←qq_H	11 qq0 101	C5+	●	●	●	●	●	●	1	3	11	
PUSH IX	(SP−2)←IX_L (SP−1)←IX_H	11 011 101 11 100 101	DD E5	●	●	●	●	●	●	2	4	15	
PUSH IY	(SP−2)←IY_L (SP−1)←IY_H	11 111 101 11 100 101	FD E5	●	●	●	●	●	●	2	4	15	
POP qq	qq_H ← (SP+1) qq_L ← (SP)	11 qq0 001	C1+	●	●	●	●	●	●	1	3	10	
POP IX	IX_H←(SP+1) IX_L ← (SP)	11 011 101 11 100 001	DD E1	●	●	●	●	●	●	2	4	14	
POP IY	IY_H ← (SP+1) IY_L ← (SP)	11 111 101 11 100 001	FD E1	●	●	●	●	●	●	2	4	14	

dd	Reg.
00	BC
01	DE
10	HL
11	SP

qq	Reg.
00	BC
01	DE
10	HL
11	AF

Notes : dd is any of the register pairs BC, DE, HL, SP.
qq is any of the register pairs AF, BC, DE, HL.
$(PAIR)_H$, $(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively, e.g., BC_L=C, AF_H=A.

Flags : ● =unchanged, 0=reset, 1=set, X=undefined, ‡ =set or reset according to the result of the operation

Table 3 Exchange, block transfer, block search groups

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	Flags C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	DE ↔ HL	11 101 011	EB	●	●	●	●	●	●	1	1	4	
EX AF, AF′	AF ↔ AF′	00 001 000	08	●	●	●	●	●	●	1	1	4	
EXX	(BC) (DE) (HL) ↔ (BC′) (DE′) (HL′)	11 011 001	D9	●	●	●	●	●	●	1	1	4	Register bank and auxiliary register bank exchange
EX (SP), HL	H ↔ (SP+1) L ↔ (SP)	11 100 011	E3	●	●	●	●	●	●	1	5	19	
EX (SP), IX	IX_H ↔ (SP+1) IX_L ↔ (SP)	11 011 101 11 100 011	DD E3	●	●	●	●	●	●	2	6	23	
EX (SP), IY	IY_H ↔ (SP+1) IY_L ↔ (SP)	11 111 101 11 100 011	FD E3	●	●	●	●	●	●	2	6	23	
LDI	(DE) ← (HL) DE ← DE+1 HL ← HL+1 BC ← BC−1	11 101 101 10 100 000	ED A0	●	●	↕ ①	●	0	0	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)
LDIR	(DE) ← (HL) DE ← DE+1 HL ← HL+1 BC ← BC−1	11 101 101 10 110 000	ED B0	●	●	0	●	0	0	2	5	21	If BC≠0
	If BC=0 end									2	4	16	If BC=0
LDD	(DE) ← (HL) DE ← DE−1 HL ← HL−1 BC ← BC−1	11 101 101 10 101 000	ED A8	●	●	↕ ①	●	0	0	2	4	16	
LDDR	(DE) ← (HL) DE ← DE−1 HL ← HL−1 BC ← BC−1	11 101 101 10 111 000	ED B8	●	●	0	●	0	0	2	5	21	If BC≠0
	If BC=0 end									2	4	16	If BC=0
CPI	A− (HL) HL ← HL+1 BC ← BC−1	11 101 101 10 100 001	ED A1	●	↕ ②	↕ ①	↕	1	↕	2	4	16	
CPIR	A− (HL) HL ← HL+1 BC ← BC−1	11 101 101 10 110 001	ED B1	●	↕ ②	↕ ①	↕	1	↕	2	5	21	If BC≠0 and A≠(HL)
	If A= (HL) or BC=0 end									2	4	16	If BC=0 or A= (HL)
CPD	A− (HL) HL ← HL−1 BC ← BC−1	11 101 101 10 101 001	ED A9	●	↕ ②	↕ ①	↕	1	↕	2	4	16	
CPDR	A− (HL) HL ← HL−1 BC ← BC−1	11 101 101 10 111 001	ED B9	●	↕ ②	↕ ①	↕	1	↕	2	5	21	If BC≠0 and A≠(HL)
	If A= (HL) or BC=0 end									2	4	16	If BC=0 or A= (HL)

Note: ①P/V flag is 0 if the result of BC=0, otherwise P/V=1
②Z flag is 1 if A= (HL), otherwise Z=0

Flags : ● = unchanged
0 = set, 1 = reset
↕ = set or reset according to the result of the operation

Table 4 8-bit arithmetic and logical group

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	Flags C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A, r	A ← A+r	10 k r	80+	↕	↕	V	↕	0	↕	1	1	4	
ADD A, n	A ← A+n	11 k 110 ← n →	C6+	↕	↕	V	↕	0	↕	2	2	7	
ADD A, (HL)	A ← A+ (HL)	10 k 110	86+	↕	↕	V	↕	0	↕	1	2	7	
ADD A, (IX+d)	A ← A+ (IX+d)	11 011 101 10 k 110 ← d →	DD 86+	↕	↕	V	↕	0	↕	3	5	19	
ADD A, (IY+d)	A ← A+ (IY+d)	11 111 101 10 k 110 ← d →	FD 86+	↕	↕	V	↕	0	↕	3	5	19	
ADC A, s	A ← A+s+C	4 types available based on the above ADD instruction (see Comments)		↕	↕	V	↕	0	↕	1※1 2 1 3	1※1 2 2 5	4※1 7 7 19	
SUB s	A ← A−s			↕	↕	V	↕	1	↕				
SBC A, s	A ← A−s−C			↕	↕	V	↕	1	↕				
AND s	A ← A∧s			0	↕	P	↕	0	1				
OR s	A ← A∨s			0	↕	P	↕	0	0				
XOR s	A ← A⊕s			0	↕	P	↕	0	0				
CP s	A−s			↕	↕	V	↕	1	↕				
INC r	r ← r+1	00 r ℓ	00+	●	↕	V	↕	0	↕	1	1	4	
INC (HL)	(HL) ← (HL)+1	00 110 ℓ	30+	●	↕	V	↕	0	↕	1	3	11	
INC (IX+d)	(IX+d) ← (IX+d)+1	11 011 101 00 110 ℓ ← d →	DD 30+	●	↕	V	↕	0	↕	3	6	23	
INC (IY+d)	(IY+d) ← (IY+d)+1	11 111 101 00 110 ℓ ← d →	FD 30+	●	↕	V	↕	0	↕	3	6	23	
DEC m	m ← m−1	4 types available based on the above INC instruction		●	↕	V	↕	1	↕	1※2 1 3 3	1※2 3 6 6	4※2 11 23 23	

r	Reg.
000	B
001	C
010	D
011	E
100	H
101	L
111	A

Mnemonic	k
ADD	000
ADC	001
SUB	010
SBC	011
AND	100
OR	110
XOR	101
CP	111

S=r, n, (HL), (IX+d), (IY+d)

Mnemonic	ℓ
INC	100
DEC	101

m=r, (HL), (IX+d), (IY+d)

Note : V and P mean overflow and parity, respectively.

Flags : ● =unchanged
0=reset
1=set
X=undefined
↕ =set or reset according to the result of the operation

※1: depends on s.
※2: depends on m.

Table 5 General purpose arithmetic and CPU control groups

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	Flags C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States	Comments
DAA	Decimal adjustment (add/subtract)	00 100 111	27	↕	↕	P	↕	●	↕	1	1	4	Decimal adjust accumulator.
CPL	A ← $\overline{A}$	00 101 111	2F	●	●	●	●	1	1	1	1	4	Complement accumulator (one's complement).
NEG	A ← 0−A	11 101 101 01 000 100	ED 44	↕	↕	V	↕	1	↕	2	2	8	Negate acc. (two's complement).
CCF	C ← $\overline{C}$	00 111 111	3F	↕	●	●	●	0	X	1	1	4	Complement carry flag.
SCF	C ← 1	00 110 111	37	1	●	●	●	0	0	1	1	4	Set carry flag.
NOP	No operation	00 000 000	00	●	●	●	●	●	●	1	1	4	
HALT	CPU halted	01 110 110	76	●	●	●	●	●	●	1	1	4	
DI	IFF ← 0	11 110 011	F3	●	●	●	●	●	●	1	1	4	Interrupt not enable
EI	IFF ← 1	11 111 011	FB	●	●	●	●	●	●	1	1	4	Interrupt enable
IM 0	Set interrupt mode 0	11 101 101 01 000 110	ED 46	●	●	●	●	●	●	2	2	8	Set interrupt mode.
IM 1	Set interrupt mode 1	11 101 101 01 010 110	ED 56	●	●	●	●	●	●	2	2	8	
IM 2	Set interrupt mode 2	11 101 101 01 011 110	ED 5E	●	●	●	●	●	●	2	2	8	

Note : IFF indicates the interrupt enable flip-flop, CY indicates the carry flip-flop.
Flags : ● =unchanged, 0=reset, 1=set, X=undefined, ↕ =set or reset according to the result of the operation

Table 6 16-bit arithmetic group

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	Flags C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD HL, ss	HL ← HL +ss	00 ss1 001	09+	↕	●	●	●	0	X	1	3	11	
ADC HL, ss	HL ← HL +ss+C	11 101 101 01 ss1 010	ED 4A+	↕	↕	V	↕	0	X	2	4	15	
SBC HL, ss	HL ← HL −ss−C	11 101 101 01 ss0 010	ED 42+	↕	↕	V	↕	1	X	2	4	15	
ADD IX, pp	IX ← IX+pp	11 011 101 00 pp1 001	DD 09+	↕	●	●	●	0	X	2	4	15	
ADD IY, rr	IY ← IY+rr	11 111 101 00 rr1 001	FD 09+	↕	●	●	●	0	X	2	4	15	
INC ss	ss ← ss+1	00 ss0 011	03+	●	●	●	●	●	●	1	1	6	
INC IX	IX ← IX+1	11 011 101 00 100 011	DD 23	●	●	●	●	●	●	2	2	10	
INC IY	IY ← IY+1	11 111 101 00 100 011	FD 23	●	●	●	●	●	●	2	2	10	
DEC ss	ss ← ss−1	00 ss1 011	0B+	●	●	●	●	●	●	1	1	6	
DEC IX	IX ← IX−1	11 011 101 00 101 011	DD 2B	●	●	●	●	●	●	2	2	10	
DEC IY	IY ← IY−1	11 111 101 00 101 011	FD 2B	●	●	●	●	●	●	2	2	10	

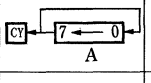
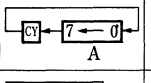
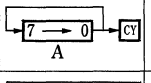
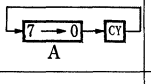
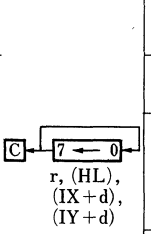
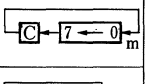
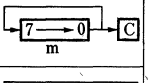
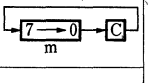
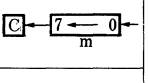
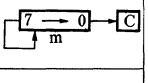
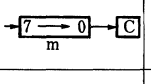
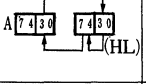
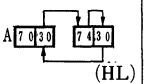
ss	Reg.
00	BC
01	DE
10	HL
11	SP

pp	Reg.
00	BC
01	DE
10	IX
11	SP

rr	Reg.
00	BC
01	DE
10	IY
11	SP

Note : ss is any of the register pairs BC, DE, HL, SP.
pp is any of the register pairs BC, DE, IX, SP.
rr is any of the register pairs BC, DE, IY, SP.
Flags : ● =unchanged, 0=reset, 1=set, X=undefinede, ↕ =set or reset according to the result of the operation

Table 7 Rotate and shift groups

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	Flags C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA		00 000 111	07	‡	●	●	●	0	0	1	1	4	Rotate left circular accumulator.
RLA		00 010 111	17	‡	●	●	●	0	0	1	1	4	Rotate left accumulator.
RRCA		00 001 111	0F	‡	●	●	●	0	0	1	1	4	Rotate right circular accumulator.
RRA		00 011 111	1F	‡	●	●	●	0	0	1	1	4	Rotate right accumulator.
RLCr		11 001 011 00 k r	CB 00+	‡	‡	P	‡	0	0	2	2	8	Rotate left circular register r.
RLC (HL)		11 001 011 00 k 110	CB 06+	‡	‡	P	‡	0	0	2	4	15	
RLC (IX+d)		11 011 101 11 001 011 ← d → 00 k 110	DD CB 06+	‡	‡	P	‡	0	0	4	6	23	
RLC (IY+d)		11 111 101 11 001 011 ← d → 00 k 110	FD CB 06+	‡	‡	P	‡	0	0	4	6	23	
RL m				‡	‡	P	‡	0	0				
RRC m				‡	‡	P	‡	0	0				
RR m				‡	‡	P	‡	0	0	2* 2 4 4	2* 4 6 6	8* 15 23 23	
SLA m				‡	‡	P	‡	0	0				
SRA m				‡	‡	P	‡	0	0				
SRL m				‡	‡	P	‡	0	0				
RLD		11 101 101 01 101 111	ED 6F	●	‡	P	‡	0	0	2	5	18	Rotate digit left and right between the accumulator and location (HL).
RRD		11 101 101 01 100 111	ED 67	●	‡	P	‡	0	0	2	5	18	The content of the upper half of the accumulator is unaffected.

r	Reg.
000	B
001	C
010	D
011	E
100	H
101	L
111	A

Mnemonic	k
RLC	000
RRC	001
RL	010
RR	011
SLA	100
SRA	101
SRL	111

m=r, (HL), (IX+d), (IY+d)

*depends on m.

Flags : ● =unchanged
0=reset
1=set
×=undefined
‡ =set or reset according to the result of the operation

Table 8 Bit set, reset and test group

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	Flags C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States
BIT b, r	$Z \leftarrow \bar{r}_b$	11 001 011 01 b r	CB 40+	●	‡	X	X	0	1	2	2	8
BIT b, (HL)	$Z \leftarrow \overline{(HL)}_b$	11 001 011 01 b 110	CB 46+	●	‡	X	X	0	1	2	3	12
BIT b, (IX+d)	$Z \leftarrow \overline{(IX+d)}_b$	11 011 101 11 001 011 ← d → 01 b 110	DD CB 46+	●	‡	X	X	0	1	4	5	20
BIT b, (IY+d)	$Z \leftarrow \overline{(IY+d)}_b$	11 111 101 11 001 011 ← d → 01 b 110	FD CB 46+	●	‡	X	X	0	1	4	5	20
SET b, r	$r_b \leftarrow 1$	11 001 011 a b r	CB	●	●	●	●	●	●	2	2	8
SET b, (HL)	$(HL)_b \leftarrow 1$	11 001 011 a b 110	CB 06+	●	●	●	●	●	●	2	4	15
SET b, (IX+d)	$(IX+d)_b \leftarrow 1$	11 011 101 11 001 011 ← d → a b 110	DD CB 06+	●	●	●	●	●	●	4	6	23
SET b, (IY+d)	$(IY+d)_b \leftarrow 1$	11 111 101 11 001 011 ← d → a b 110	FD CB 06+	●	●	●	●	●	●	4	6	23
RES b, m	$m_b \leftarrow 0$									2* 2 4 4	2* 4 6 6	8* 15 23 23

r	Reg.
000	B
001	C
010	D
011	E
100	H
101	L
111	A

b	Bit Tested
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Mnemonic	a
SET	11
RES	10

m=r, (HL), (IX+d), (IY+d)
*depends on m

Note : The notation m_b indicates bit b (0 to 7) or location m.
Flags : ● =unchanged
0=reset
1=set
X=undefined
‡ =set or reset according to the result of the operation

Table 9 Jump group

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP nn	PC ← nn	11 000 011 ← n → ← n →	C3	●	●	●	●	●	●	3	3	10	
JP cc, nn	If condition cc is true PC ← nn,	11 cc 010 ← n → ← n →	C2+	●	●	●	●	●	●	3	3	10	
	otherwise continue									3	3	10	
JR e	PC ← PC+e	00 011 000 ← e-2 →	18	●	●	●	●	●	●	2	3	12	
JR C, e	If C=1 PC ← PC+e	00 111 000 ← e-2 →	38	●	●	●	●	●	●	2	3	12	
	If C=0 continue									2	2	7	
JR NC, e	If C=0 PC ← PC+e	00 110 000 ← e-2 →	30	●	●	●	●	●	●	2	3	12	
	If C=1 continue									2	2	7	
JR Z, e	If Z=1 PC ← PC+e	00 101 000 ← e-2 →	28	●	●	●	●	●	●	2	3	12	
	If Z=0 continue									2	2	7	
JR NZ, e	If Z=0 PC ← PC+e	00 100 000 ← e-2 →	20	●	●	●	●	●	●	2	3	12	
	If Z=1 continue									2	2	7	
JP (HL)	PC ← HL	11 101 001	E9	●	●	●	●	●	●	1	1	4	
JP (IX)	PC ← IX	11 011 101 11 101 001	DD E9	●	●	●	●	●	●	2	2	8	
JP (IY)	PC ← IY	11 111 101 11 101 001	FD E9	●	●	●	●	●	●	2	2	8	
DJNZ, e	If B ← B−1 B≠0 PC ← PC+1	00 010 000 ← e-2 →	10	●	●	●	●	●	●	2	3	13	
	If B=0 continue									2	2	8	

cc	Condition
000	NZ
001	Z
010	NC
011	C
100	PO
101	PE
110	P
111	M

NZ : non-zero
Z : zero
C : carry
PO : parity odd
PE : parity even
P : sign positive
M : sign negative

Note : e represents the extension in the relative addressing mode.
e is a signed two's complement number in the range <−126, 129>
e −2 in the opcode provides an effective address of pc+e as PC is incremented by 2 prior to the addition of e.
e itself is obtained from opcode position.

Flags : ● =unchanged
0=reset
1=set
X=undefined
↕ =set or reset according to the result of the operation

Table 10 Call and return group

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	Flags C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States
CALL nn	(SP−1) ← PC_H (SP−2) ← PC_L PC ← nn	11 001 101 ← n → ← n →	CD	●	●	●	●	●	●	3	5	17
CALL cc, nn	If condition cc is false continue, otherwise same as CALL nn	11 cc 100 ← n → ← n →	C4+	●	●	●	●	●	●	3 3	5 3	17 10
RET	PC_L ← (SP) PC_H ← (SP+1)	11 001 001	C9	●	●	●	●	●	●	1	3	10
RET cc	If condition cc is false continue, otherwise same as RET	11 cc 000	C0+	●	●	●	●	●	●	1 1	3 1	11 5
RETI	Return from interrupt	11 101 101 01 001 101	ED 4D	●	●	●	●	●	●	2	4	14
RETN	Return from non-maskable interrupt	11 101 101 01 000 101	ED 45	●	●	●	●	●	●	2	4	14
RST p	(SP−1) ← PC_H (SP−2) ← PC_L PC_H ← 0 PC_L ← p	11 t 111	C7+	●	●	●	●	●	●	1	3	11

Comments

cc	Condition
000	NZ
001	Z
010	NC
011	C
100	PO
101	PE
110	P
111	M

r	p
000	00_H
001	08_H
010	10_H
011	18_H
100	20_H
101	28_H
110	30_H
111	38_H

Flags : ● = unchanged
0 = reset
1 = set
X = undefined
↕ = set or reset according to the result of the operation

Table 11 Input and output group

Mnemonic	Symbolic operation	OP code 76 543 210	HEX code (Basic)	C	Z	P/V	S	N	H	No. of Bytes	No. of M Cycles	No. of T States	Comments
IN A, (n)	A ← (n)	11 011 011 ← n →	DB	●	●	●	●	●	●	2	3	11	n → A_0~A_7 Acc → A_8~A_{15}
IN r, (C)	r ← (C)	11 101 101 01 r 000	ED 40+	●	↕	P	↕	0	↕	2	3	12	
INI	(HL) ← (C) B ← B−1 HL ← HL+1	11 101 101 10 100 010	ED A2	X	↕ ①	X	X	1	X	2	4	16	C → A_0~A_7 B → A_8~A_{15}
INIR	(HL) ← (C) B ← B−1 HL ← HL+1 Repeat until B=0	11 101 101 10 110 010	ED B2	X	1 ②	X	X	1	X	2 2	5 (If B≠0) 4 (If B=0)	21 16	
IND	(HL) ← (C) B ← B−1 HL ← HL−1	11 101 101 10 101 010	ED AA	X	↕ ①	X	X	1	X	2	4	16	
INDR	(HL) ← (C) B ← B−1 HL ← HL−1 Repeat until B=0	11 101 101 10 111 010	ED BA	X	1 ②	X	X	1	X	2 2	5 (If B≠0) 4 (If B=0)	21 16	
OUT (n), A	(n) ← A	11 010 011 ← n →	D3	●	●	●	●	●	●	2	3	11	n → (A-BUS)$_{0\sim7}$ Acc → (A-BUS)$_{8\sim15}$
OUT (C), r	(C) ← r	11 101 101 01 r 001	ED 41+	●	●	●	●	●	●	2	3	12	
OUTI	(C) ← (HL) B ← B−1 HL ← HL+1	11 101 101 10 100 011	ED A3	X	↕ ①	X	X	1	X	2	4	16	C → A_0~A_7
OTIR	(C) ← (HL) B ← B−1 HL ← HL+1 Repeat until B=0	11 101 101 10 110 011	ED B3	X	1 ②	X	X	1	X	2 2	5 (If B≠0) 4 (If B=0)	21 16	B → A_8~A_{15}
OUTD	(C) ← (HL) B ← B−1 HL ← HL−1	11 101 101 10 101 011	ED AB	X	↕ ①	X	X	1	X	2	4	16	
OTDR	(C) ← (HL) B ← B−1 HL ← HL−1 Repeat until B=0	11 101 101 10 111 011	ED BB	X	1 ②	X	X	1	X	2 2	5 (If B≠0) 4 (If B=0)	21 16	

r	Reg.
000	B
001	C
010	D
011	E
100	H
101	L
111	A

Note : ①If the result of B−1 is zero the Z flag is set, otherwise it is reset.
②Z flag is set upon instruction completion only.

Flags : ● = unchanged
0 = reset
1 = set
X = undefined
↕ = set or reset according to the result of the operation

LH0081/LH0081A/LH0081B

Z80/Z80A/Z80B Parallel Input/Output Controller

■ Description

The Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

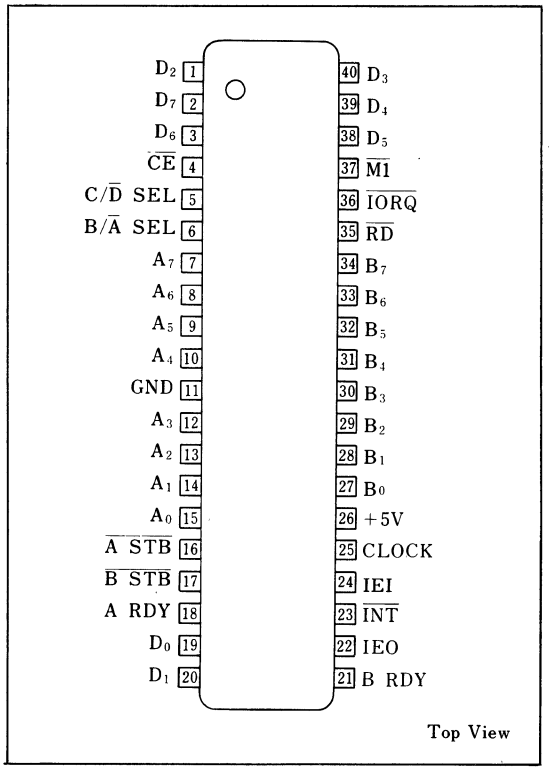
The LH0081 Z80 PIO (Z80 PIO for short below) is a programmable two port device which provides TTL compatible interfacing between peripheral devices and the Z80 CPU. The Z80 CPU configures Z80 PIO to interface with standard peripheral devices such as tape punchers, printers, keyboards, etc.

The LH0081A Z80A and LH0081B Z80B PIO are the high speed version which can opeate at the 4MHz and 6MHz system clock, respectively.

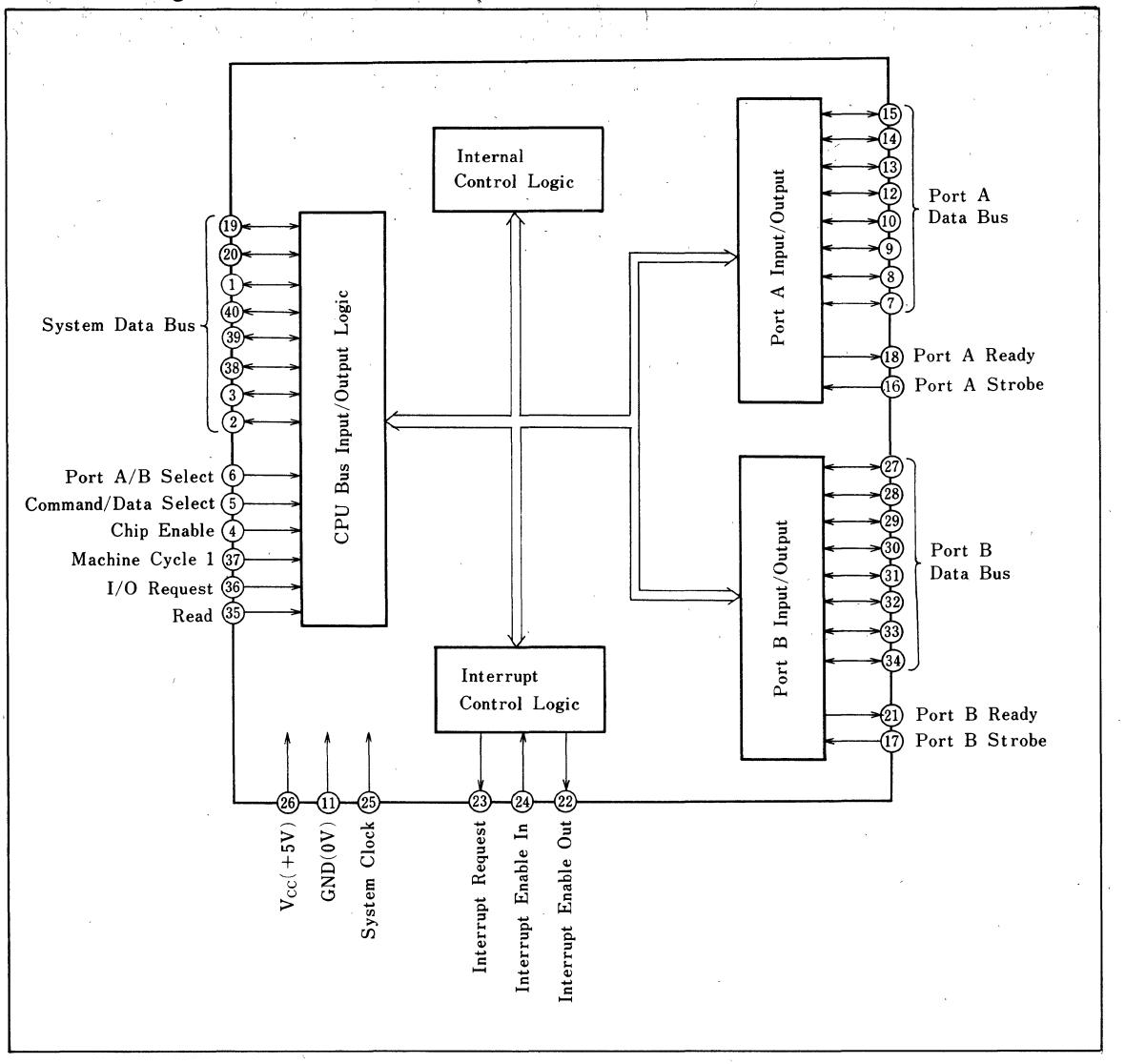
■ Features

1. Two independent 8-bit bidirectional peripheral interface ports with "handshake" data transfer control
2. N-channel silicon-gate process
3. Any one of the following four modes of operation may be selected.
   - Byte output mode
   - Byte input mode
   - Byte bidirectional bus (available on Port A only)
   - Bit mode
4. Programmable interrupt
5. Vectored daisy chain priority interrupt logic included
6. The port B outputs can drive Darlington transistors
7. All inputs and outputs fully TTL compatible
8. Single +5V power supply and single phase clock
9. 40-pin dual-in-line package

■ Pin Connections



Block Diagram



Pin Description

Pin	Meaning	I/O	Function
$D_0 \sim D_7$	Data bus	Bidirectional 3-state	System data bus.
B/$\overline{A}$ SEL	Port B or A select	I	Defines which port is accessed. A high selects port B, and a low port A.
C/$\overline{D}$ SEL	Control or data select	I	Defines the type of data transfer on the data bus. A high selects control, and a low data.
$\overline{CE}$	Chip enable	I	Active "Low". A low enables the CPU to transmit and receive control words and data.
CLOCK	System clock	I	Standard Z80 system clock used for internal synchronization signals.
$\overline{M1}$	Machine cycle one	I	Active "Low". Indicates that the CPU is acknowledging an interrupt, when both $\overline{M1}$ and $\overline{IORQ}$ are active.
$\overline{IORQ}$	Input/output request	I	Active "Low". Read operation when $\overline{RD}$ is active, and write operation when it is not active. Indicates that the CPU is acknowledging an interrupt, when both $\overline{IORQ}$ and $\overline{M1}$ are active.
$\overline{RD}$	Read cycle status	I	Active "Low". Read operation when active.
IEI	Interrupt enable in	I	Active "High". Forms a priority-interrupt daisy-chain.
IEO	Interrupt enable out	O	Active "High". Forms a priority-interrupt daisy-chain.
$\overline{INT}$	Interrupt request	Open drain, O	Active "Low". Active when requesting an interrupt.
$A_0 \sim A_7$	Port A bus	Bidirectional 3-state	Transfers information between port A and a peripheral device.
$\overline{A\ STB}$	Port A strobe	I	Active "Low". Used as a handshake line for data transfer synchronization on port A. Not used in the bit control mode.
A RDY	Port A ready	O	Active "High". Used as a handshake line for data transfer synchronization on port A. Not used in the bit control mode.
$B_0 \sim B_7$	Port B bus	Bidirectional 3-state	Transfers information between port B and a peripheral device.
$\overline{B\ STB}$	Port B strobe	I	Active "Low". Used as a handshake line for data transfer synchronization on port B. Not used in the bit control mode.
B RDY	Port B ready	O	Active "High". Used as a handshake line for data transfer synchronization on port B. Not used in the bit control mode.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7	V
Output voltage	V_{OUT}	−0.3～+7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0~+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock input low voltage	V_{ILC}		−0.3		0.45	V
Clock input high voltage	V_{IHC}		V_{CC}−0.6		V_{CC}+0.3	V
Input low voltage	V_{IL}		−0.3		0.8	V
Input high voltage	V_{IH}		2.0		5.5	V
Output low voltage	V_{OL}	I_{OL}=2mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4			V
Supply current	I_{CC}	V_{OH}=1.5V			100	mA
Input leakage current	$\|I_{LI}\|$	$0 \leqq V_{IN} \leqq V_{CC}$			10	μA
3 state output/data bus input leakage current	$\|I_z\|$	$0 \leqq V_{IN} \leqq V_{CC}$			10	μA
Darlington drive current	I_{OHD}	R_{EXT}=390Ω	−1.5			mA

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground			12	pF
Input capacitance	C_{IN}				7	pF
Output capacitance	C_{OUT}				10	pF

■ AC Characteristics

(V_{CC}=5V±5%, Ta=0~+70℃)

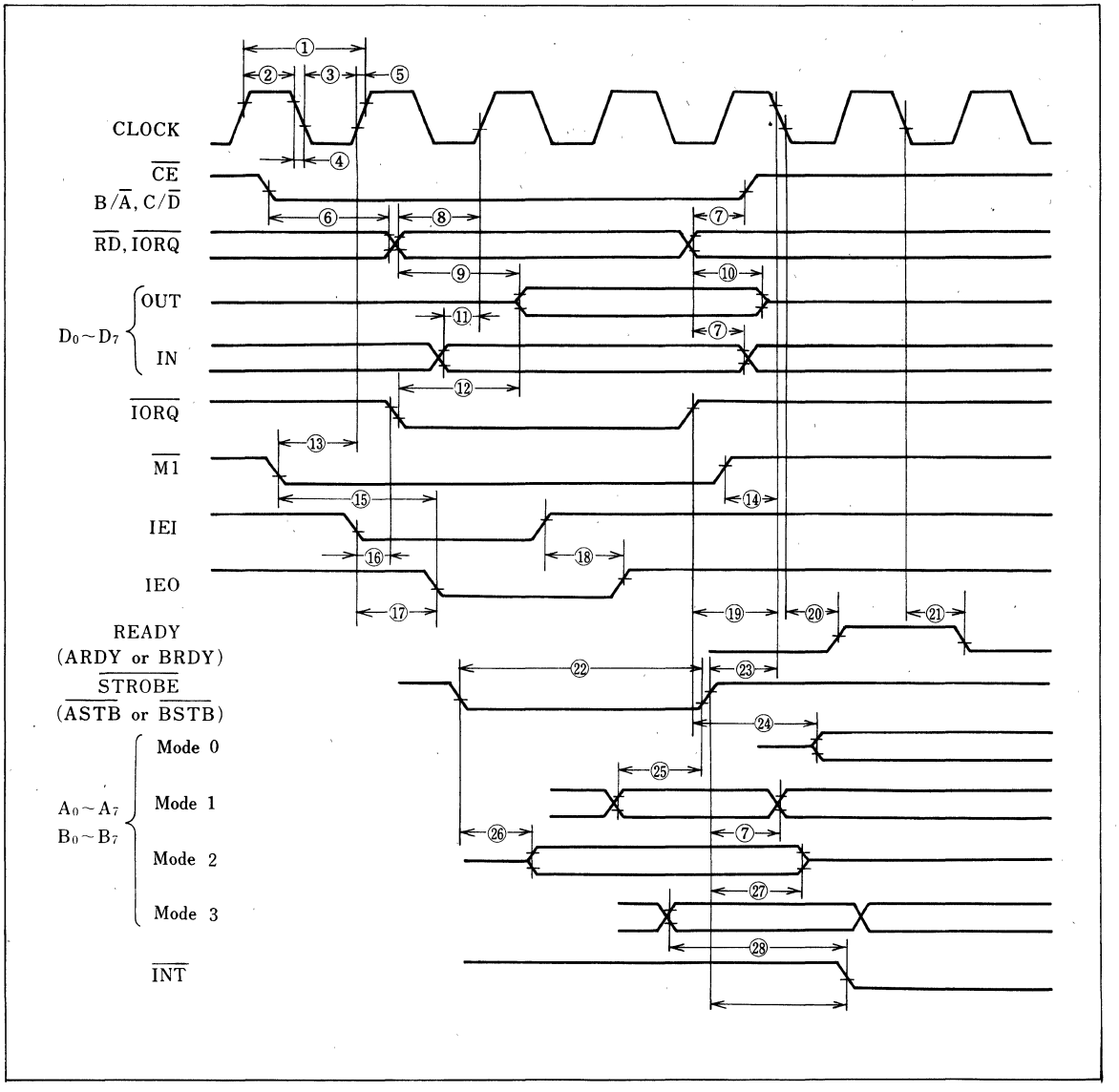
No.	Parameter	Symbol	Z80 PIO		Z80A PIO		Z80B PIO (Note 9)		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	Clock cycle time	TcC	400	(Note 1)	250	(Note 1)	165	(Note 1)	ns	
2	Clock width (high)	TwCh	170	2000	105	2000	65	2000	ns	
3	Clock width (low)	TwCl	170	2000	105	2000	65	2000	ns	
4	Clock fall time	TfC		30		30		20	ns	
5	Clock rise time	TrC		30		30		20	ns	
6	$\overline{CE}$, B/$\overline{A}$, C/$\overline{D}$ to $\overline{RD}$, $\overline{IORQ}$ ↓ setup time	TsCS (RI)	50		50		50		ns	6
7	Any hold times for specified setup time	Th	0		0		0		ns	
8	$\overline{RD}$, $\overline{IORQ}$ to clock ↑ setup time	TsRI (C)	115		115		70		ns	
9	$\overline{RD}$, $\overline{IORQ}$ ↓ to data out delay	TdRI (DO)		430		380		300	ns	2
10	$\overline{RD}$, $\overline{IORQ}$ ↑ to data out float delay	TdRI (DOs)		160		110		70	ns	
11	Data in to clock ↑ setup time	TsDI (C)	50		50		40		ns	C_L=50pF
12	$\overline{IORQ}$ ↓ to vector out delay (INTACK cycle)	TdIO (DOI)	340		160		120		ns	3
13	$\overline{M1}$ ↓ to clock ↑ setup time	TsM1 (Cr)	210		90		70		ns	
14	$\overline{M1}$ ↑ to clock ↓ setup time ($\overline{M1}$ cycle)	TsM1 (Cf)	0		0		0		ns	8
15	$\overline{M1}$ ↓ to IEO ↓ delay (interrupt immediately preceding $\overline{M1}$ ↓)	TdMI (IEO)		300		190		100	ns	5, 7
16	IEI to $\overline{IORQ}$ ↓ setup time (INTACK cycle)	TsIEI (IO)	140		140		100		ns	7
17	IEI ↓ to IEO ↓ delay	TdIEI (IEOf)		190		130		120	ns	5 C_L=50pF
18	IEI ↑ to IEO ↑ delay (After ED decode)	TdIEI (IEOr)		210		160		160	ns	5

No.	Parameter	Symbol	Z80 PIO		Z80A PIO		Z80B PIO (Note 9)		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
19	$\overline{IORQ}$ ↑ to clock ↓ setup time (to activate READY on next clock cycle)	TcIO (C)	220		200		170		ns	
20	Clock ↓ to READY ↑ delay	TdC (RDYr)	200		190		170		ns	5 C_L=50pF
21	Clock ↓ to READY ↓ delay	TdC (RDYf)	150		140		120		ns	5
22	$\overline{STROBE}$ pulse width	TwSTB	150		150		120		ns	4
23	$\overline{STROBE}$ ↑ to clock ↓ setup time (to activate READY on next clock cycle)	TsSTB (C)	220		220		150		ns	5
24	$\overline{IORQ}$ ↑ to PORT DATA stable delay (Mode 0)	TdIO (PD)		200		180		160	ns	5
25	PORT DATA to $\overline{STROBE}$ ↑ setup time (mode 1)	TsPD (STB)	260		230		190		ns	
26	$\overline{STROBE}$ ↓ to PORT DATA stable (mode 2)	TdSTB (PD)		230		210		180	ns	5
27	$\overline{STROBE}$ ↑ to PORT DATA float delay (mode 2)	TdSTB (PDr)		200		180		160	ns	C_L=50pF
28	PORT DATA match to $\overline{INT}$ ↓ delay (mode 3)	TdPD (INT)		540		490		430	ns	
29	$\overline{STROBE}$ ↑ to $\overline{INT}$ ↓ delay	TdSTB (INT)		490		440		350	ns	

↑ Rising edge, ↓ Falling edge

Note 1: TcC=TwCh+TwCl+TrC+TfC.
Note 2: Increase TdRI (DO) by 10 ns for each 50 pF increase in load up to 200 pF max.
Note 3: Increase TdIO (DOI) by 10 ns for each 50 pF, increase in load up to 200 pF max.
Note 4: For Mode 2 : TwSTB>TsPD (STB).
Note 5: Increase these values by 2 ns for each 10 pF increase in load up to 100 pF max.
Note 6: TsCS (RI) may be reduced. However, the time subtracted from TsCS (RI) will be added to TdRI (DO).
Note 7: 2.5 TcC>(N−2) TdIEI (IEOf)+TdM1 (IEO)+TsIEI (IO)+TTL buffer delay, if any.
Note 8: M1 must be active for a minimum of two clock cycles to reset the PIO.
Note 9: Z80B PIO numbers are preliminary and subject to change.

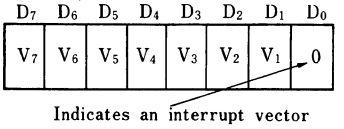
■ AC Timing Chart



■ Programming

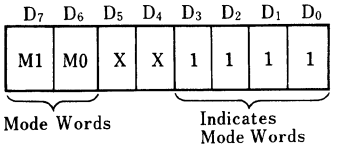
(1) Interrupt vector read

An interrupting device needs giving an 8-bit interrupt vector to the CPU. Using this vector, the CPU forms an interrupt service routine address.



(2) Operation mode select

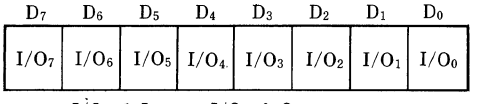
An operation mode is selected by writing data to the 2-bit mode control register in the following manner.



X means they are not used

Mode	M1	M0
Byte output mode	0	0
Byte input mode	0	1
Bidirectional byte bus mode	1	0
Bit control mode	1	1

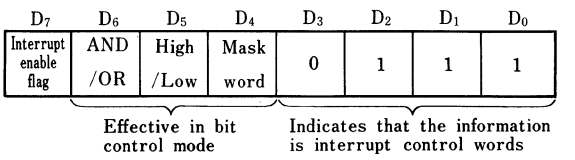
In selecting the bit control mode, an input/output direction should be set later.



I/O=1:Input; I/O=0:Output

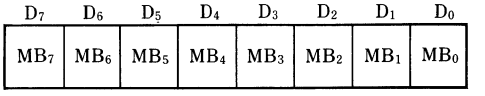
(3) Interrupt control

The interrupt control words are as follows.

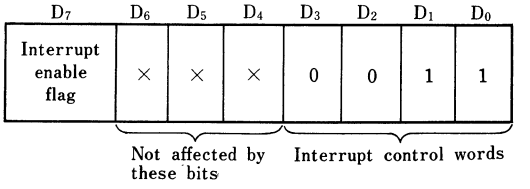


Bit7=1: Interrupt enable flag is set to enable an interrupt.
Bit7=0: Interrupt enable flag is reset to disable an interrupt.
Bit6~4: Defines interrupt conditions in the bit mode. Ignored in other modes.
Bit3~0: Indicates interrupt control words.

If bit4=1, the following control words are supposed to be written in the mask register.



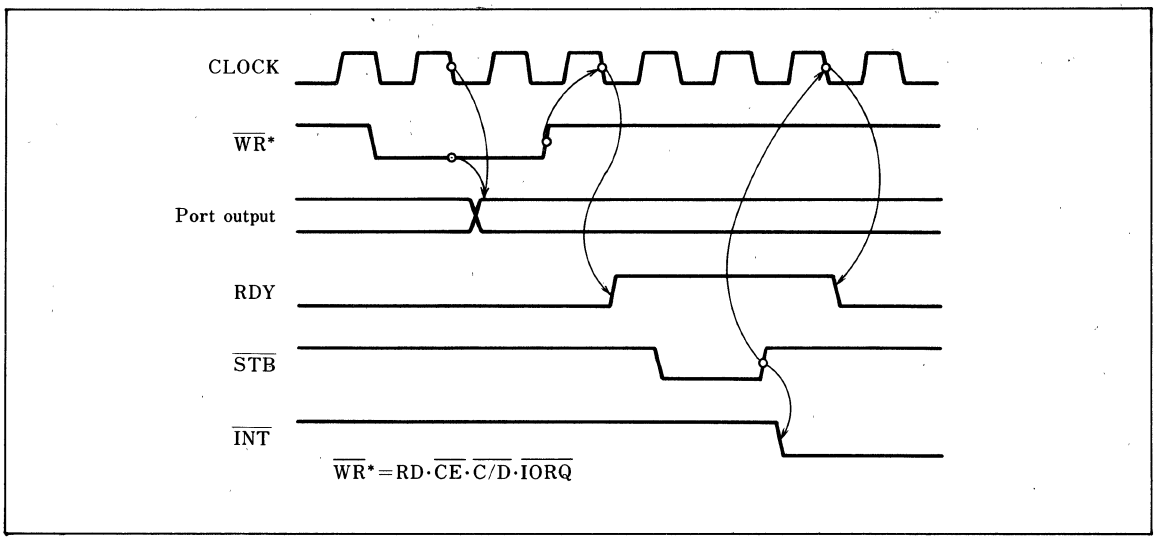
Only the port data line with MB=0 is monitored. When the interrupt conditions are satisfied, an interrupt takes place.



■ Timing

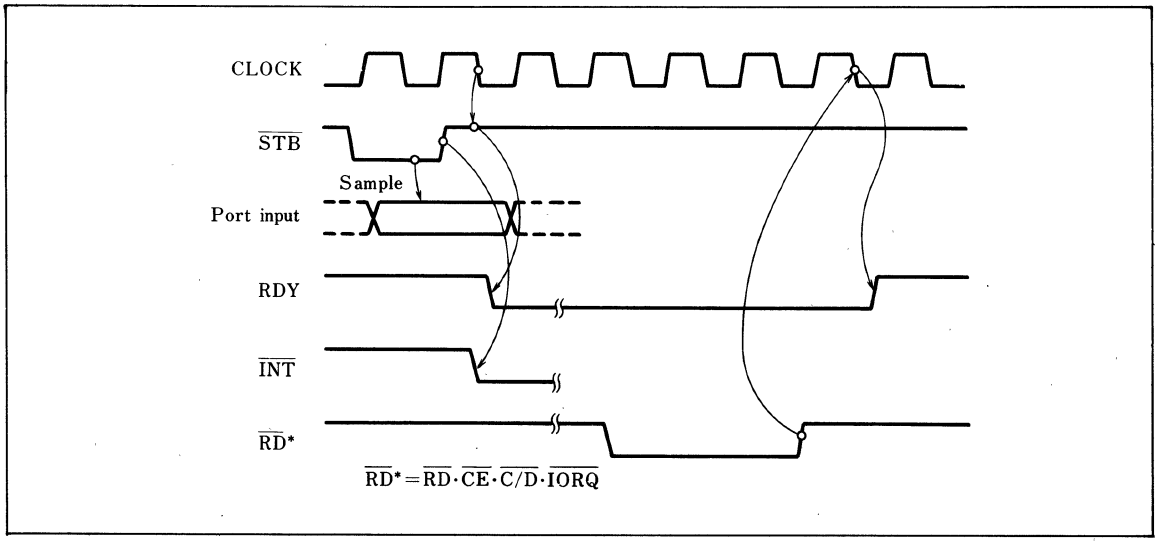
(1) Output mode (Mode 0)

An output cycle is always started by the execution of an output instruction by the CPU. The $\overline{WR}$* pulse from the CPU latches the data from the CPU data bus into the selected port's output register. The $\overline{WR}$* pulse sets the Ready flag after a Low-going edge of CLK, indicating data is available. Ready stays active until the positive edge of the strobe line is received, indication that data was taken by the peripheral. The positive edge of the strobe pulse generates an $\overline{INT}$ if the interrupt enable flipflop has been set and if this device has the highest priority.



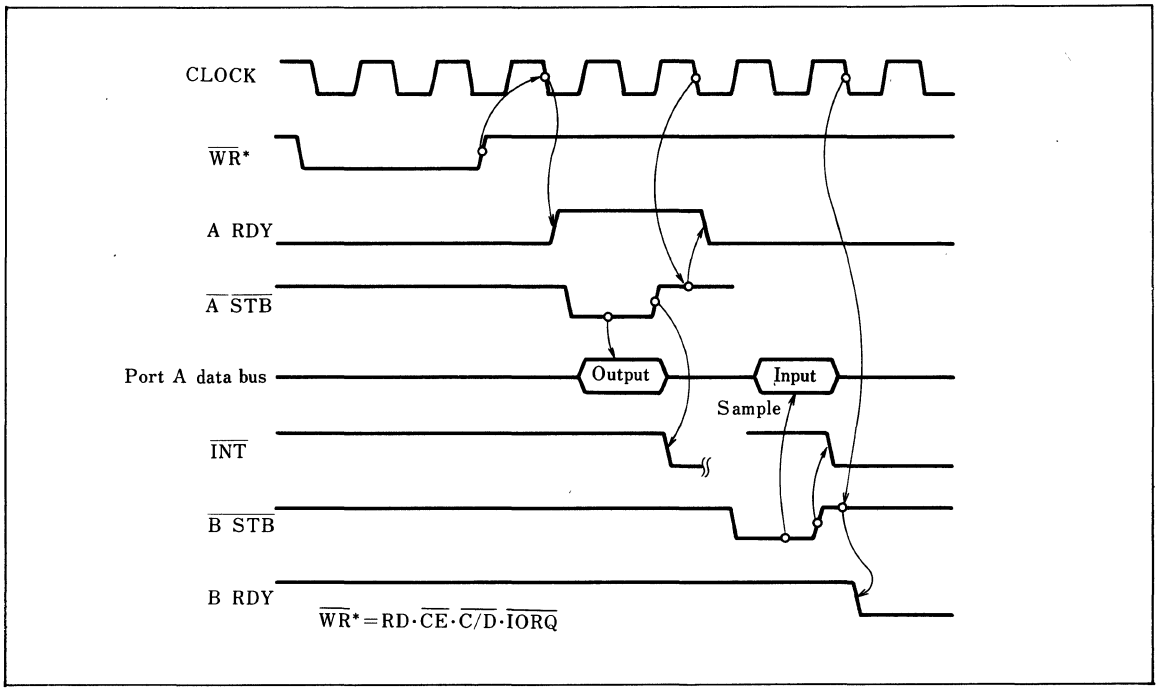
(2) Input mode (Mode 1)

When STROBE goes Low, data is loaded into the selected port input register. The next rising edge of strobe activates INT, if Interrupt Enable is set and this is the highest-priority requesting device. The following falling edge of CLK resets Ready to an inactive state, indicating that the input register is full and cannot accept any more data until the CPU completes a read. When a read is complete, the positive edge of RD sets Ready at the next Low-going transition of CLK. At this time new data can be loaded into the PIO.



(3) Bidirectional mode (Mode 2)

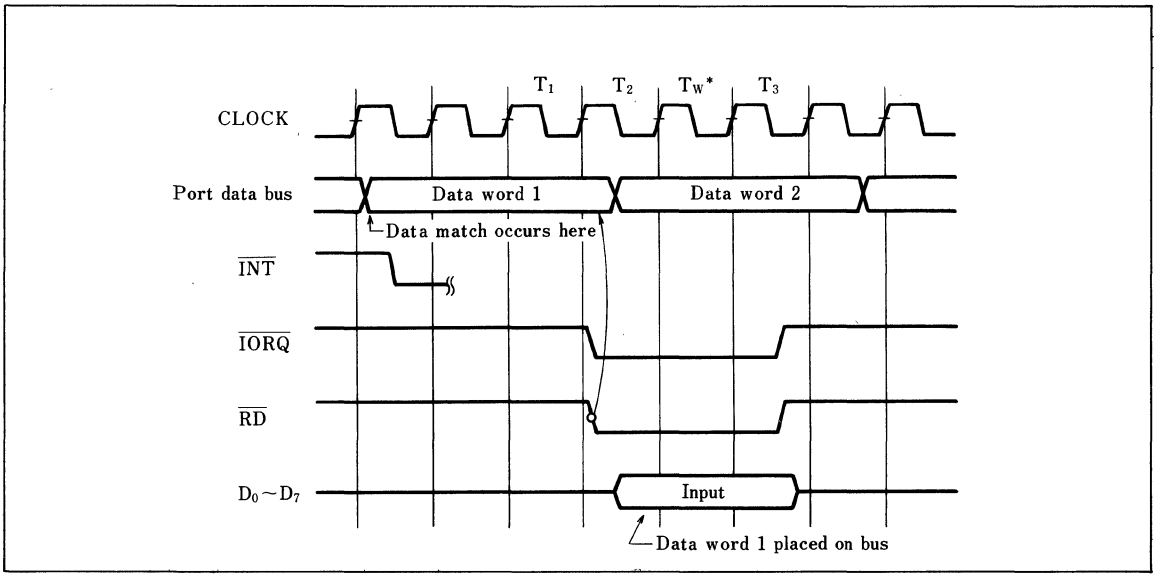
This is a combination of Modes 0 and 1 using all four handshake lines and the eight Port A I/O lines. Port B must be set to the bit mode and its inputs must be masked. The Port A handshake lines are used for output control and the Port B lines are used for input control. If interrupts occur, Port A's vector will be used during port output and Port B's will be used during port input. Data is allowed out onto the Port A bus only when ASTB is Low. The rising edge of this strobe can be used to latch the data into the peripheral.



(4) Bit mode (Mode 3)

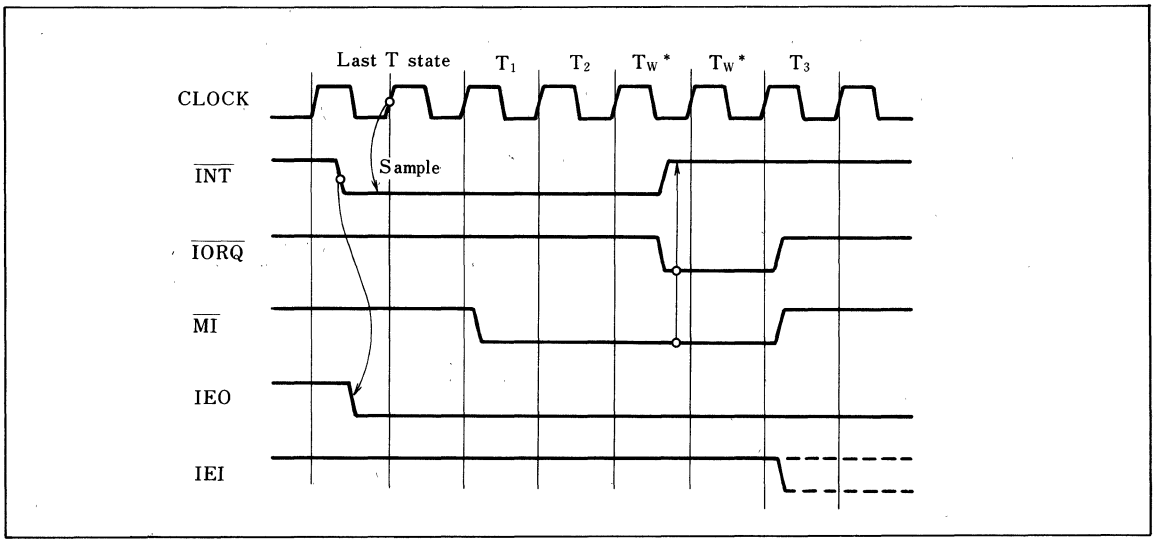
The bit mode does not utilize the handshake signals, and a normal port write or port read can be executed at any time. When writing , the data is latched into the output registers with the same timing as the output mode.

When reading the PIO, the data returned to the CPU is composed of output register data from those port data lines assigned as outputs and input register data from those port data lines assigned as inputs. The input register contains data that was present immediately prior to the falling edge of RD. An interrupt is generated if interrupts from the port are enabled and the data on the port data lines satisfy the logical equation defined by the 8-bit mask and 2-bit mask control registers. However, if Port A is programmed in bidirectional mode, Port B does not issue an interrupt in bit mode and must therefore be polled.



(5) Interrupt acknowledge timing

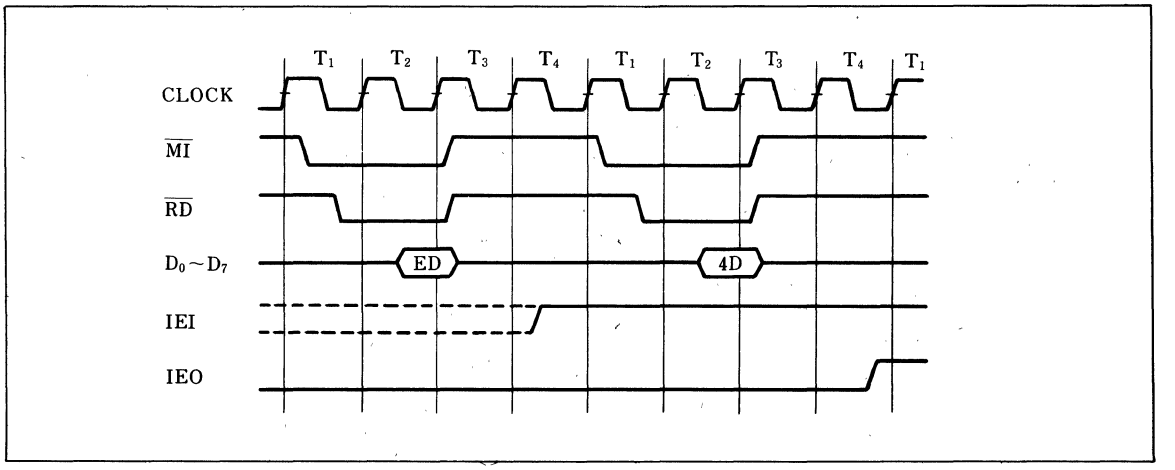
During $\overline{M1}$ time, peripheral controllers are inhibited from changing their interrupt enable status, permitting the Interrupt Enable signal to ripple through the daisy chain. The peripheral with IEI High and IEO Low during $\overline{INTACK}$ places a preprogrammed 8-bit interrupt vector on the data bus at this time. IEO is held Low until a Return From Interrupt (RETI) instruction is executed by the CPU while IEI is High. The 2-byte RETI instruction is decoded internally by the PIO for this purpose.



(6) Return from interrupt cycle

If a Z-80 peripheral has no interrupt pending and is not under service, then its IEO=IEI. If it has an interrupt under service (i.e., it has already interrupted and received an interrupt acknowledge) then its IEO is always Low, inhibiting lower priority devices from interrupting. If it has an interrupt pending which has not yet been acknowledged, IEO is Low unless an "ED" is decoded as the first byte of a 2-byte opcode. In this case, IEO goes High until the next opcode byte is decoded, whereupon it goes Low again. If the second byte of the opcode was a "4D", then the opcode was an RETI instruction.

After an "ED" opcode is decoded, only the peripheral device which has interrupted and is currently under service has its IEI High and its IEO Low. This device is the highest-priority device in the daisy chain that has received an interrupt acknowledge. All other peripherals have IEI = IEO. If the next opcode byte decoded is "4D". this peripheral device resets its "interrupt under service" condition.



LH0082/LH0082A/LH0082B

Z80/Z80A/Z80B Counter Timer Circuit

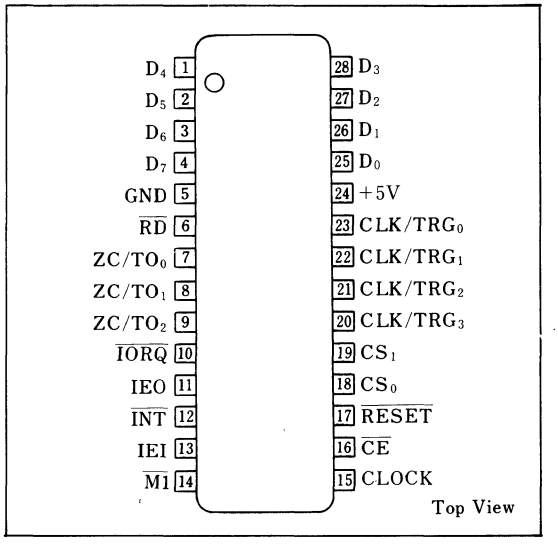
■ Description

The Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

The LH0082 Z80 CTC (Z80 CTC for short below) is a programmable, four channel device that provides counting and timing functions for the Z80 CPU. The Z80 CPU configures the Z80 CTC's four independent channels to operate under various modes and conditions as required.

The LH0082A Z80A and LH0082B Z80B CTC are the high speed version which can operate at the 4MHz and 6MHz system clock, respectively.

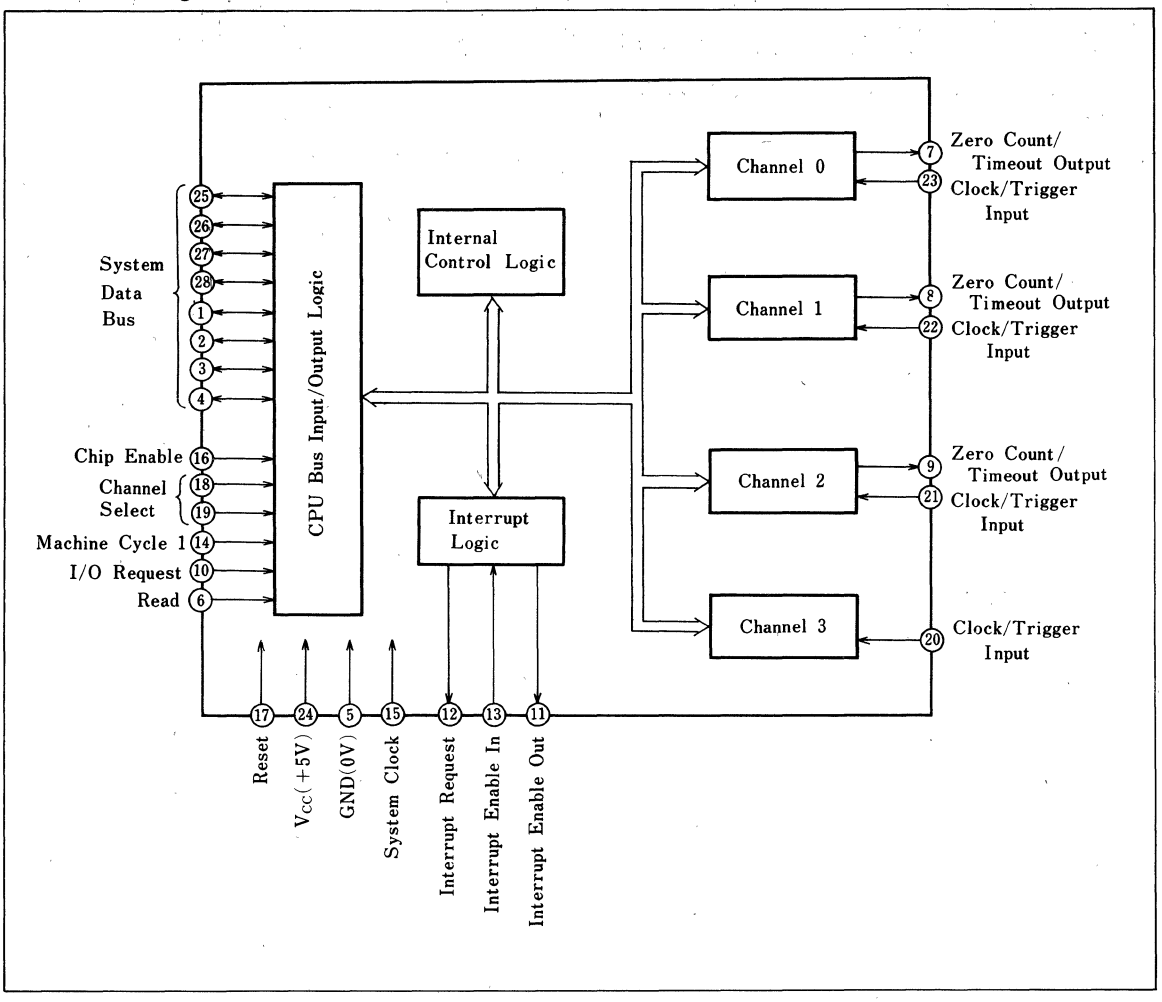
■ Pin Connections



■ Features

1. Four independent programmable 8-bit counter/16-bit timer channels
2. N-channel silicon gate process
3. Each channel may be selected to operate in either a counter mode or timer mode
4. Programmable interrupts on counter or timer states
5. When the down-counter reaches the zero count the CTC reloads its time constant automatically and continues it's channel operation
6. Readable down counter
7. Selectable 16 or 256 clock prescaler for each timer channels
8. Selectable positive or negative trigger may initiate timer or counter operation
9. Three channels have ZC/TO outputs capable of driving Darlington transistors
10. Vectored daisy chain priority interrupt logic included
11. Single +5V power supply and single phase clock
12. All inputs and outputs fully TTL compatible
13. 28-pin dual-in-line package

Block Diagram



Pin Description

Pin	Meaning	I/O	Function
$D_0 \sim D_7$	Data bus	Bidirectional 3-state	System data bus.
CS_0, CS_1	Channel select	I	Selects one of the four independent channels.
$\overline{CE}$	Chip enable	I	Active "Low". A Low enables the CPU to transmit and receive control words and data.
CLOCK	System clock	I	Standard Z80 system clock used for internal synchronization signals.
$\overline{M1}$	Machine cycle one	I	Active "Low". Indicates that the CPU is acknowledging an interrupt, when both $\overline{M1}$ and $\overline{IORQ}$ are active.
$\overline{IORQ}$	I/O request	I	Active "Low". Read operation when RD is active, and write operation when it is not active. Indicates the CPU is acknowledging an interrupt, when both $\overline{IORQ}$ and $\overline{M1}$ are active.
$\overline{RD}$	Read cycle status	I	Active "Low". Read operation when active.

Pin	Meaning	I/O	Function
IEI	Interrupt enable in	I	Active "High". Forms a priority-interrupt daisy-chain.
IEO	Interrupt enable out	O	Active "High". Forms a priority-interrupt daisy-chain.
$\overline{INT}$	Interrupt request	Open drain, O	Active "Low". Active when requesting an interrupt.
$\overline{RESET}$	Reset	I	Active "Low". Resets the interrupt bits.
CLK/TRG_0～ CLK/TRG_3	External clock/timer trigger input	I	Counter/timer input for four independent channels.
ZC/TO_0～ ZC/TO_2	External clock/timer trigger out	O	Active "High". 0/1/2 output for four independent channels. No output terminal at channel 3.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7	V
Output voltage	V_{OUT}	−0.3～+7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock input low voltage	V_{ILC}		−0.3		0.45	V
Clock input high voltage	V_{IHC}		V_{CC}−0.6		V_{CC}+0.3	V
Input low voltage	V_{IL}		−0.3		0.8	V
Input high voltage	V_{IH}		2.0		V_{CC}	V
Output low voltage	V_{OL}	I_{OL}=2mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4			V
Supply current	I_{CC}	t_c=400ns			120	mA
Input leakage current	I_{LI}	$0 \leqq V_{IN} \leqq V_{CC}$			10	μA
3-state output leakage current	$\lvert I_{LOH} \rvert$	$2.4V \leqq V_{OUT} \leqq V_{CC}$			10	μA
3-state output leakage current	$\lvert I_{LOL} \rvert$	V_{OUT}=0.4V			10	μA
Darlington drive current	I_{OHD}	V_{OH}=1.5V, R_{EXT}=390Ω	−1.5			mA

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground			20	pF
Input capacitance	C_{IN}				5	pF
Output capacitance	C_{OUT}				10	pF

■ AC Characteristics

(V_{CC}=5V±5%, Ta=0~+70℃)

No.	Symbol	Parameter	Z80 CTC		Z80A CTC		Z80B CTC		Unit	Note*
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	TcC	Clock cycle time	400	(Note 1)	250	(Note 1)	165	(Note 1)	ns	
2	TwCh	Clock width (high)	170	2000	105	2000	65	2000	ns	
3	TwCl	Clock width (low)	170	2000	105	2000	65	2000	ns	
4	TfC	Clock fall time		30		30		20	ns	
5	TrC	Clock rise time		30		30		20	ns	
6	Th	All hold times	0		0		0		ns	
7	TsCS (C)	$\overline{CS}$ to clock ↑ setup time	250		160		100		ns	
8	TsCE (C)	$\overline{CE}$ to clock ↑ setup time	200		150		100		ns	
9	TsIO (C)	$\overline{IORQ}$ ↑ to clock ↑ setup time	250		115		70		ns	
10	TsRD (C)	$\overline{RD}$ ↓ to clock ↑ setup time	240		115		70		ns	
11	TdC (DO)	Clock ↑ to data out delay		240		200		130	ns	2
12	TdC (DOz)	Clock ↓ to data out float delay		230		110		90	ns	
13	TsDI (C)	Data in to clock ↑ setup time	60		50		40		ns	
14	TsM1 (C)	$\overline{M1}$ to clock ↑ setup time	210		90		70		ns	
15	TdM1 (IEO)	$\overline{M1}$ ↓ to IEO ↓ delay (interrupt immediately preceding $\overline{M1}$)		300		190		130	ns	3
16	TdIO (DOI)	$\overline{IORQ}$ ↓ to data out delay (INTA cycle)		340		160		110	ns	2
17	TdIEI (IEOf)	IEI ↓ to IEO ↓ delay		190		130		100	ns	3
18	TdIEI (IEOr)	IEI ↑ to IEO ↑ delay (after ED decode)		220		160		110	ns	3
19	TdC (INT)	Clock ↑ to $\overline{INT}$ ↓ delay		TcC+200		TcC+140		TcC+120	ns	4
20	TdCLK (INT)	CLK/TRG ↑ to $\overline{INT}$ ↓ delay tsCTR (C) satisfied		TcC+230		TcC+160		TcC+130	ns	5
		CLK/TRG ↑ to $\overline{INT}$ ↓ delay tsCTR (C) not satisfied		2TcC+530		2TcC+370		2TcC+280	ns	5
21	TcCTR	CLK/TRG cycle time	2TcC		2TcC		2TcC		ns	5
22	TrCTR	CLK/TRG rise time		50		50		40	ns	
23	TfCTR	CLK/TRG fall time		50		50		40	ns	
24	TwCTRl	CLK/TRG width (low)	200		200		120		ns	
25	TwCTRh	CLK/TRG width (high)	200		200		120		ns	
26	TsCTR (Cs)	CLK/TRG ↑ to clock ↑ setup time for immediate count	300		210		150		ns	5
27	TsCTR (Ct)	CLK/TRG ↑ to clock ↑ setup time for enabling of prescaler on following clock ↑	210		210		150		ns	4
28	TdC (ZC/TOr)	Clock ↑ to ZC/TO ↑ delay		260		190		140	ns	
29	TdC (ZC/TOf)	Clock ↓ to ZC/TO ↓ delay		190		190		140	ns	

↑ Rising edge, ↓ falling edge

[A] 2.5 TcC > (n-2) TdIEI (IEOf) + TdMI (IEO) + TsIEI (IO) + TTL buffer delay, if any.

[B] $\overline{RESET}$ must be active for a minimum of 3 clock cycles.

Note 1 : TcC=TwCh+TwCl+TrC+TfC.

Note 2 : Increase delay by 10 ns for each 50 pF increase in loading, 200 pF maximum for data lines, and 100 pF for control lines.

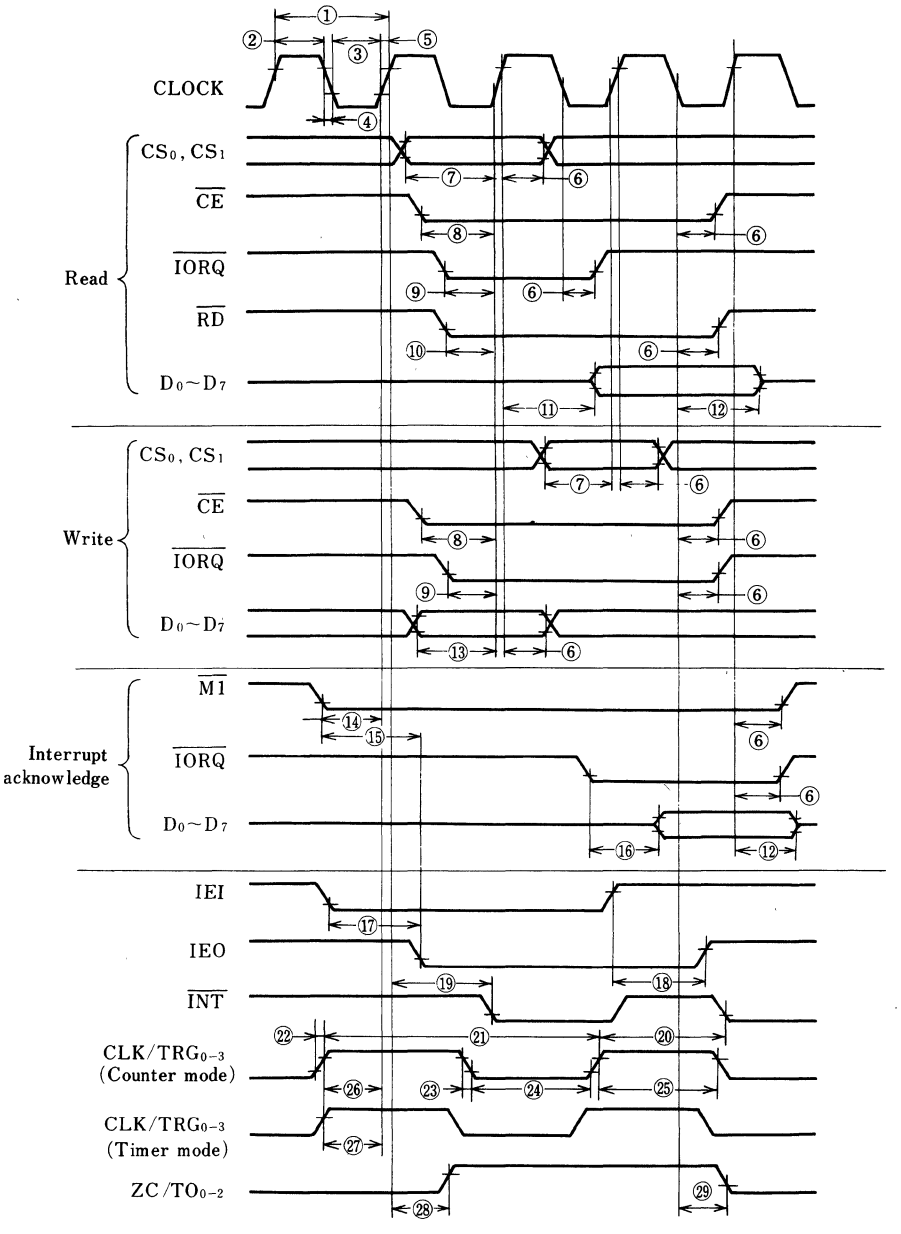
Note 3 : Increase delay by 2 ns for each 10 pF increase in loading, 100 pF maximum.

Note 4 : Timer mode.

Note 5 : Counter mode.

*: All timings are preliminary and subject to change.

AC Timing Chart



■ Programming

(1) Operation mode select

To select a channel operating mode, write a channel control word having bit 0 changed to 1 in the channel control register.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Interrupt enable	Mode	Prescaler value	CLK/TRO edge selection	Trigger mode	Time constant mode	Reset	1

D_3 and D_5 are used in timer mode only.

- Bit 7 = 0: Disables a channel interrupt.
- Bit 7 = 1: Enables a channel interrupt each time the down-counter counts down to zero. No interrupt is produced even with bit 7 as 1, after the counter has counted down to zero with bit 7 as 0.
- Bit 6 = 0: Selects the timer mode, having the prescaler output as the down-counter clock. The timer's period comes in t_C. P. TC. Where t_C represents system clock period, P has 16 or 256 (divisional scale by the prescaler), and TC means an 8-bit programmable time constant (max. 256).
- Bit 6 = 1: Selects the counter mode, having the external clock (CLK input) signal as the down-counter clock. The prescaler is not used.
- Bit 5 = 0: Used for the timer mode only. The prescaler divides the system clock into 16 sections.
- Bit 5 = 1: Used for the timer mode only. The prescaler divides the system clock into 256 sections.
- Bit 4 = 0: Starts the timer operation at the trigger input falling edge in the timer mode. In the counter mode, the down-counter comes on at the clock input rising edge.
- Bit 4 = 1: Starts the timer operation at the trigger input rising edge in the timer mode. In the counter mode, the down-counter comes on at the clock input rising edge.
- Bit 3 = 0: Effective in the timer mode only. With bit 1=1, the timer starts at the rising edge of the machine cycle T_2 which is next to the write cycle of a time constant. With bit 1=0, the timer starts at the rising edge of the machine cycle T_1 which is next to the write cycle of this control information.
- Bit 3 = 1: Effective in the timer mode only. The timer starts by an external trigger input that is given after the rising of the machine cycle T_2 next to the write cycle of a time constant. The operation starts at the second clock rising if the trigger input meets the set-up time, and at the third clock rising if it does not. If an external trigger input is given before writing a time constant the condition of bit 3 = 0 is caused.
- Bit 2 = 0: Indicates that there is no time constant written after the channel control word. This bit cannot be 0 for the channel control word to be immediately given when the channel is reset.
- Bit 2 = 1: Indicates that there is a time constant written after the channel control word. When a time constant is written during a down-counter operation, the new constant is set into the time constant register. But the counter keeps on counting. Once the counter counts zero, the new constant is available to use.
- Bit 1 = 0: The channel acts as a down-counter.
- Bit 1 = 1: Stops the operation as a down-counter. With bit 2 = 1, the operation restarts after a time contant is written.
  With bit 2 = 0, the channel does not act until a new control word is given.

(2) Time constant programming

An 8-bit time constant is written into the time constant register, following the channel control word with bit 2 = 1. "00" (hexadecimal) indicates the time constant 256.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
TC_7	TC_6	TC_5	TC_4	TC_3	TC_2	TC_1	TC_0

(3) Interrupt vector programming

If the Z-80 CTC has one or more interrupts enabled, it can supply interrupt vectors to the Z-80 CPU. To do so, the Z-80 CTC must be pre-programmed with the most-significant five bits of the interrupt vector. Programming consists of writing a vector word to the I/O port corresponding to the Z-80 CTC Channel 0. Note that D_0 of the vector word is always zero, to distinguish the vector from a channel control word. D_1 and D_2 are not used in programming the vector word. These bits are supplied by the interrupt logic to identify the channel requesting interrupt service with a unique interrupt vector. Channel 0 has the highest priority.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

D_2	D_1	Channel
0	0	0
0	1	1
1	0	2
1	1	3

■ Timing

(1) Write cycle timing

Fig. 1 shows write cycle timing for loading control, time constant or vector words.

The CTC does not have a write signal input, so it generates one internally when the read ($\overline{RD}$) input is High during T_1. During T_2 $\overline{IORQ}$ and $\overline{CE}$ inputs are Low. $\overline{M1}$ must be High to distinguish a write cycle from an interrupt acknowledge. A 2-bit binary code at inputs CS_1 and CS_0 selects the channel to be addressed, and the word being written is placed on the Z-80 data bus. The data word is latched into the appropriate register with the rising edge of clock cycle T_3.

(2) Read cycle timing

Fig. 2 shows read cycle timing. This cycle reads the contents of a down-counter without disturbing the count.

During clock cycle T_2, the Z-80 CPU initiates a read cycle by driving the following inputs Low: $\overline{RD}$, $\overline{IORQ}$, and $\overline{CE}$. A 2-bit binary code at inputs CS_1 and CS_0 selects the channel to be read. $\overline{M1}$ must be High to distinguish this cycle from an interrupt acknowledge. No additional wait states are allowed.

(3) Interrupt acknowledge timing

Fig. 3 shows interrupt acknowledge timing. After an interrupt request, the Z-80 CPU sends an interrupt acknowledge ($\overline{M1}$ and $\overline{IORQ}$). All channels are inhibited from changing their interrupt request status when $\overline{M1}$ is active—about two clock cycles earlier than $\overline{IORQ}$. $\overline{RD}$ is High to distinguish this cycle from an instruction fetch.

The CTC interrupt logic determines the highest priority channel requesting an interrupt. If the CTC interrupt enable input. (IEI) is High, the highest proiority interrupting channel within the CTC places its interrupt vector on the data bus when $\overline{IORQ}$ goes Low. Two wait states (T_{WA}) are automatically inserted at this time to allow the daisy chain to stabilize. Additional wait states may be added.

(4) Return from interrupt cycle

If a Z-80 peripheral has no interrupt pending and is not under service, then its IEO = IEI. If it has an interrupt under service (i.e.,it has already interrupted and received an interrupt acknowledge) then its IEO is always Low, inhibiting lower priority devices from interrupting. If it has an interrupt pending which has not yet been acknowledged, IEO is Low unless an "ED" is decoded as the first byte of a 2-byte opcode. In this case, IEO goes High until the next opcode byte is decoded, whereupon it goes Low again. If the second byte of the opcode

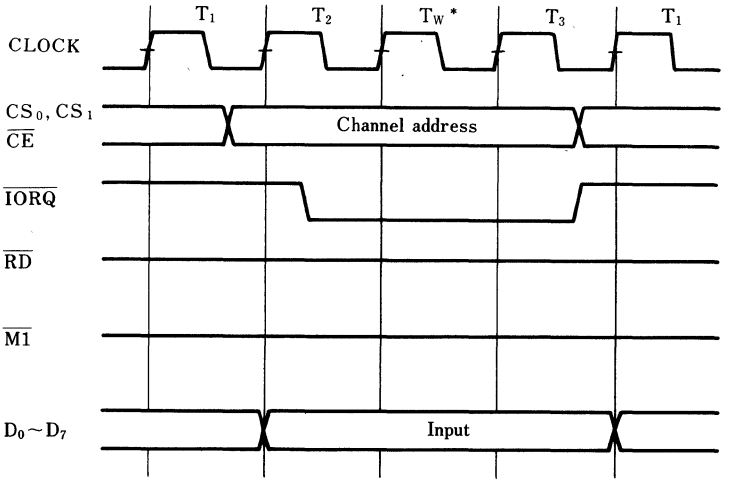


Fig. 1 Write cycle timing

was a "4D," then the opcode was an RETI instruction.

After an "ED" opcode is decoded, only the peripheral device which has interrupted and is currently under service has its IEI High and its IEO Low. This device is the highest-priority device in the daisy chain that has received an interrupt acknowledge. All other peripherals have IEI = IEO. If the next opcode byte decoded is "4D", this peripheral device resets its "interrupt under service" condition.

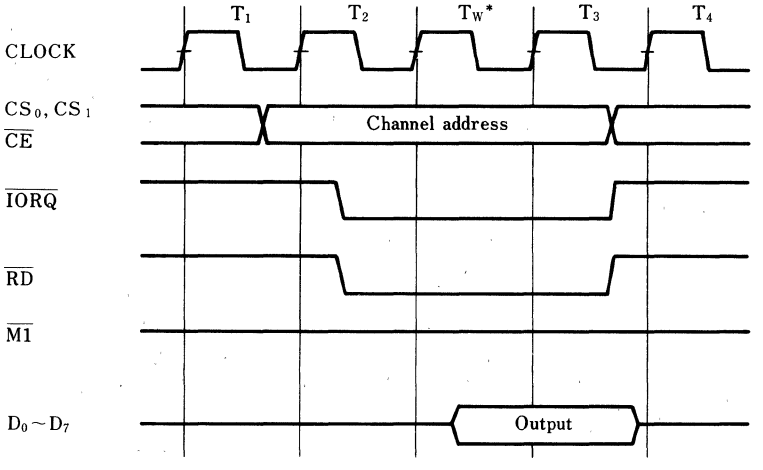


Fig. 2 Read cycle timing

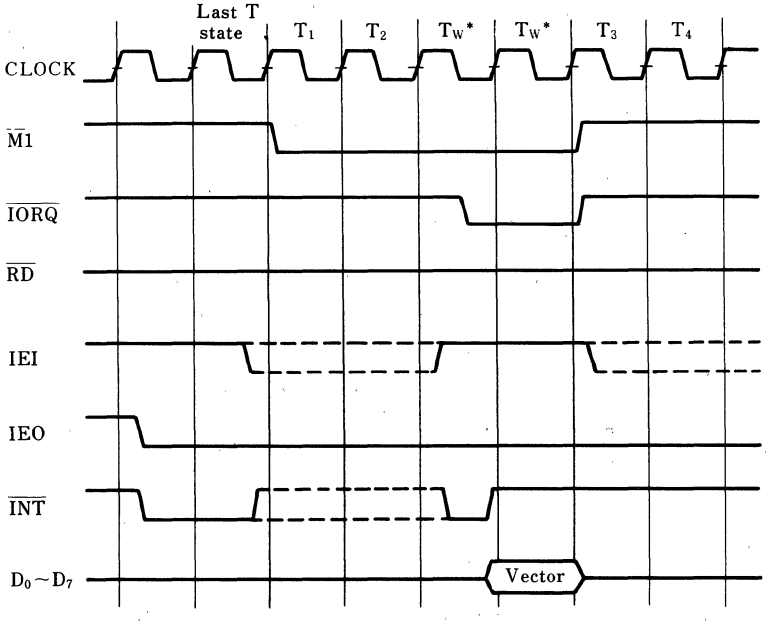


Fig. 3 Interrupt acknowledge timing

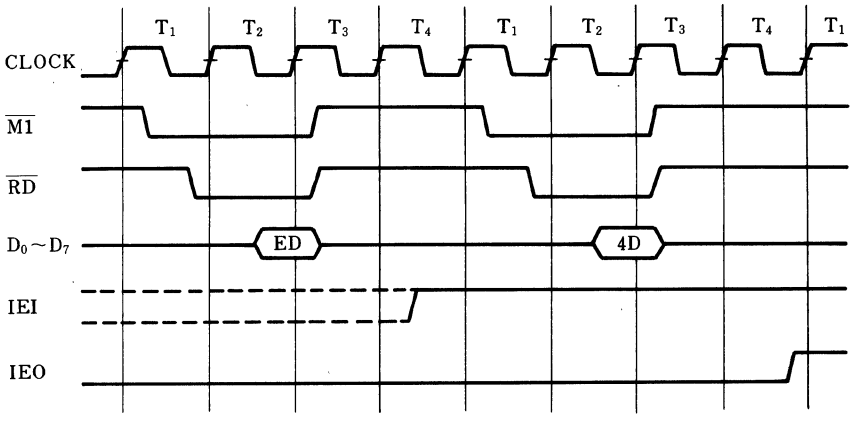
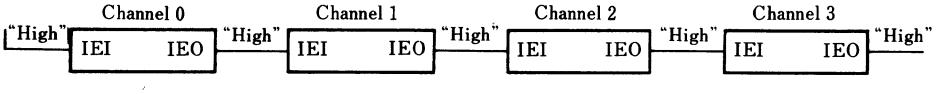
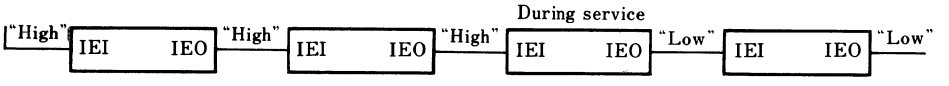


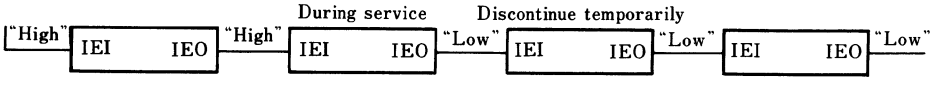
Fig. 4 Return from interrupt cycle



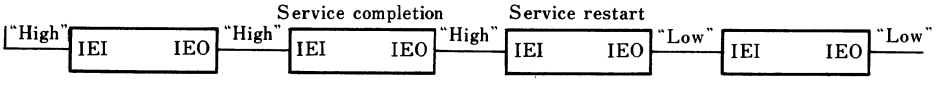
① Daisy chain prior to interrupt



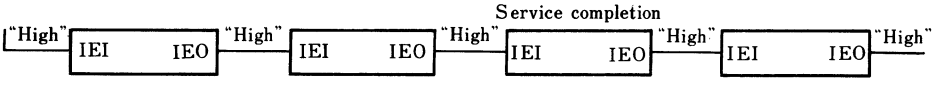
② When Channel 2 requests interrupt and receives acknowledge.



③ When Channel 1 requests interrupt and receives acknowledge.
In this case, Channel 2 service is discontinued temporarily.



④ When Channel 1 service is completed and RETI instruction is executed.
In this case, Channel 2 service is restarted.



⑤ When Channel 2 service is completed and RETI instruction is executed.

Fig. 5 Daisy-chain interrupt service

(5) Daisy-chain interrupt service

Fig. 5 shows a typical nested interrupt order with the CTC. Channel 2 first requests an interrupt to be serviced. If the higher-priority Channel 1 requests an interrupt while Channel 2 is in service, the Channel 2 service is interrupted and Channel 1 is serviced instead. Now the Channel 1 service routine has been completely executed, an RETI instruction can be given to indicate that Channel 1 has been serviced. At this moment, Channel 2 will be in service again.

(6) Counter operation/timer operation

In the counter mode, the CLK/TRG pulse input decrements the down-counter. The trigger is asynchronous, but the count is synchronized with CLK. For the decrement to occur on the next rising edge of CLK, the trigger edge must precede CLK by a minimum lead time. In the timer mode, a CLK/TRG pulse input starts the timer on the second succeeding rising edge of CLK. The trigger pulse is asynchronous, and it must have a minimun width. A minimun lead time (210 ns) is required between the active edge of the CLK/TRG and the next rising edge of CLK to enable the prescaler on the following clock edge.

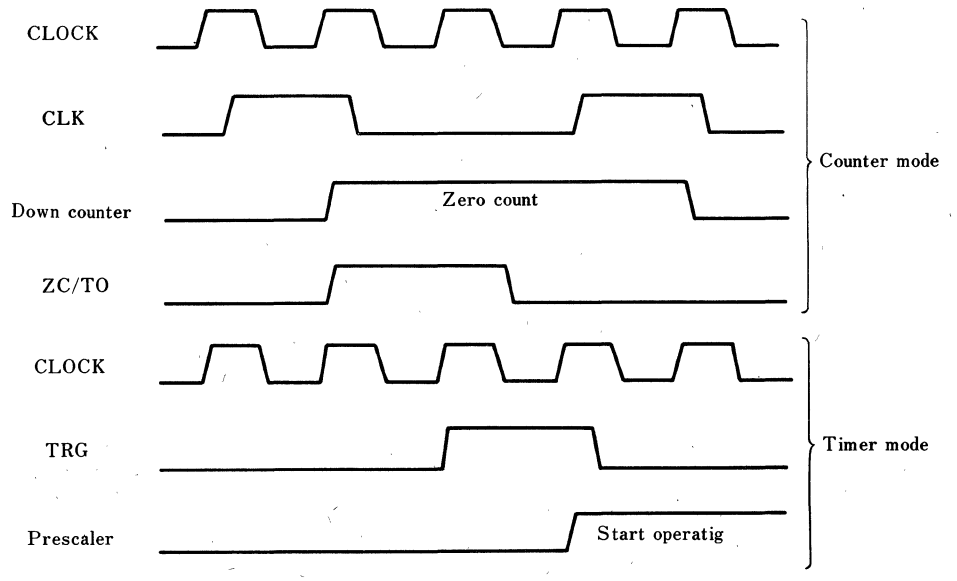


Fig. 6 Counter operation/timer operation

LH0083/LH0083A Z80/Z80A Direct Memory Access

■ Description

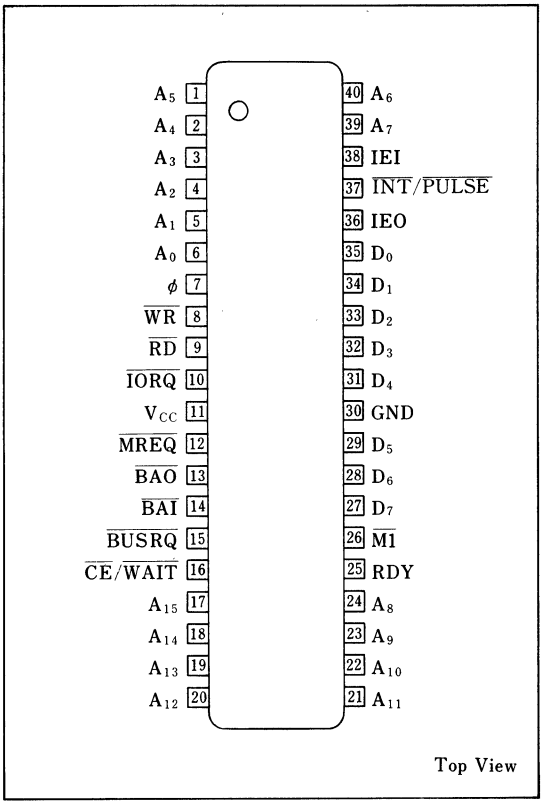
The Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

The LH0083 Z80 DMA (Z80 DMA for short below) is a powerful and versatile device for controlling and processing of data transfers. Its basic function of managing CPU-independent transfers between two ports is augmented by an array of features that optimize transfer speed and control with little or no external logic in systems using an 8-or 16-bit data bus and a 16-bit address bus.

Transfers can be done between any two ports (source and destination), including memory-to-I/O, memory-to-memory, and I/O-to-I/O. Dual port addresses are automatically generated for each transaction and may be either fixed or incrementing/decrementing. In addition, bitmaskable byte searches can be performed either concurrently with transfers or as an operation in itself.

The LH0083A Z80A DMA is a high speed version which can operate at the 4MHz system clock.

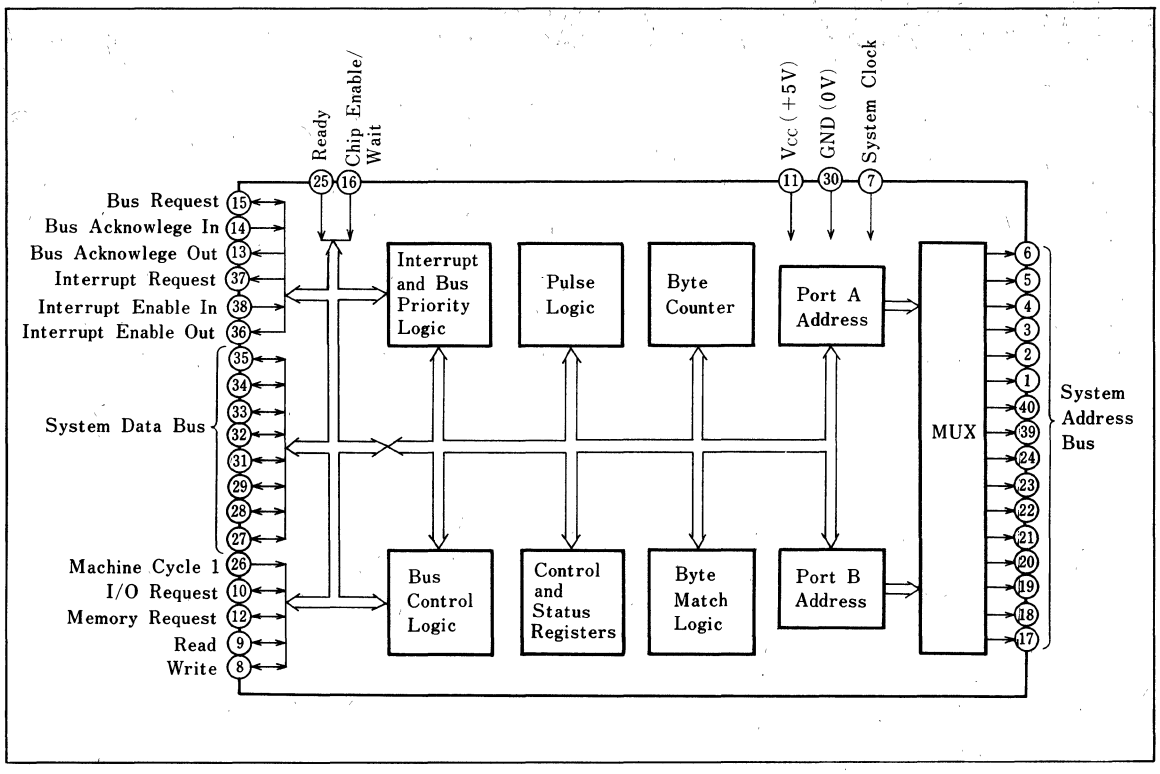
■ Pin Connections



■ Features

1. Transfers, searches and search/transfers in byte-at-a-time, burst or continuous modes
2. Cycle length and edge timing can be programmed
3. Dual port addresses generated for memory-to-I/O, memory-to-memory, or I/O-to-I/O operations Adderess may be fixed or automatically incremented/decremented
4. Next-operation loading without disturbing current operations via buffered starting-address registers and an entire previous sequence can be repeated automatically
5. Extensive programmability of functions CPU can read complete channel status
6. Vectored daisy chain priority interrupt logic
7. Single +5V power supply and single phase clock
8. TTL compatible inputs and outputs
9. 40-pin dual-in-line package
10. N-channel silicon-gate process

■ Block Diagram



■ Pin Description

Pin	Meaning	I/O	Function
$A_0 \sim A_{15}$	Address bus	3-state O	System address bus.
$D_0 \sim D_7$	Data bus	Bidirectional 3-state	System data bus.
$\overline{BAI}$	Bus acknowledge in	I	Active "low". Used to form a bus priority-interrupt daisy-chain.
$\overline{BAO}$	Bus acknowledge out	O	Active "low". Used to form a bus priority-interrupt daisy-chain.
$\overline{BUSRQ}$	Bus request	Open drain, O	Active "low". Active when controlling the bus.
$\overline{CE}/\overline{WAIT}$	Chip enable	I	Active "low". Acts as $\overline{CE}$ when the CPU accesses the DAM, and as $\overline{WAIT}$ when the DAM is the bus master.
CLOCK	System clock	I	Standard Z80 system clock used for internal synchronization signals.
$\overline{M1}$	Machine cycle one	I	Active "low". Indicates that CPU is acknowledging an interrupt, when both $\overline{M1}$ and $\overline{IORQ}$ are active.
$\overline{IORQ}$	Input/output request	Bidirectional 3-state	Active "low". Transmits and receives data from the CPU as an input line. Acts as $\overline{IORQ}$ for another device as an output line. Indicates that the CPU is acknowledging an interrupt, when both $\overline{IORQ}$ and $\overline{M1}$ are active.
$\overline{MREQ}$	Memory request	3-state O	Active "low". Requests a transfer from or to memory with the DMA as a bus master.
IEI	Interrupt enable in	I	Active "high". Used to form a priority-interrupt daisy-chain.
IEO	Interrupt enable out	O	Active "low". Used to form a priority-interrupt daisy-chain.
$\overline{INT}/\overline{PULSE}$	Interrupt request/pulse	Open drain, O	Active "low". Active when requesting an interrupt. Can also generate pulses.
$\overline{RD}$	Read	Bidirectional 3-state	Active "low". Reads data from the CPU as an input line. Acts as $\overline{RD}$ for another device as an output line.
$\overline{WR}$	Write	Bidirectional 3-state	Active "low". Writes data from the CPU as an input line. Acts as $\overline{WR}$ for another device as an output line.
RDY	Ready	I	With the DMA as a bus master, starts DMA operation when active, and stops it when not active.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7	V
Output voltage	V_{OUT}	−0.3～+7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock input low voltage		V_{ILC}		−0.3		0.45	V
Clock input high voltage		V_{IHC}		V_{CC}−0.6		5.5	V
Input low voltage		V_{IL}		−0.3		0.8	V
Input high voltage		V_{IH}		2.0		5.5	V
Output low voltage		V_{OL}	I_{OL}=3.2mA for $\overline{BUSREQ}$ I_{OL}=2.0 mA for all others			0.4	V
Output high voltage		V_{OH}	I_{OH}=−250 μA	2.4			V
Current consumption	Z80 DMA	I_{CC}	t_c=400ns			150	mA
	Z80A DMA		t_c=250ns			200	mA
Input leakage current		$\|I_{LI}\|$	0≦V_{IN}≦V_{CC}			10	μA
3-state output leakage current		$\|I_{LOH}\|$	V_{OUT}=2.4V			10	μA
3-state output leakage current		$\|I_{LOL}\|$	V_{OUT}=0.4V			10	μA
Data bus leakage current in input mode		$\|I_{LD}\|$	0V≦V_{IN}≦V_{CC}			10	μA

■ Capacitance

(f=1MHz, Ta=25℃)

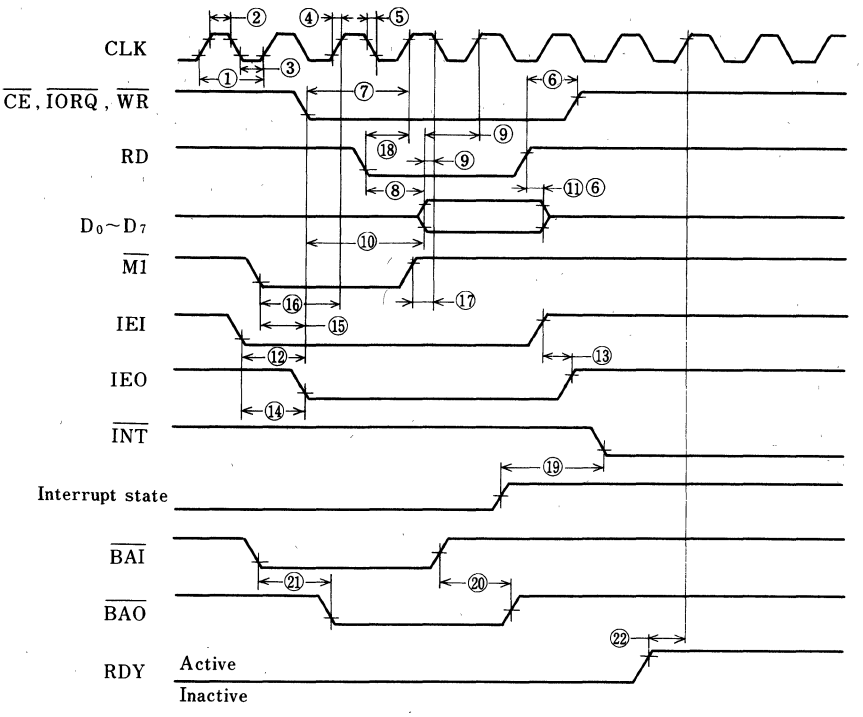
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground			35	pF
Input capacitance	C_{IN}				5	pF
Output capacitance	C_{OUT}				10	pF

■ AC Characteristics

(1) Acting as CPU peripheral (inactive state)

No.	Parameter	Symbol	Z80 DMA		Z80A DMA		Unit
			MIN.	MAX.	MIN.	MAX.	
1	Clock cycle time	TcC	400	4000	250	4000	ns
2	Clock width (high)	TwCh	170	2000	110	2000	ns
3	Clock width (low)	TwCl	170	2000	110	2000	ns
4	Clock rise time	TrC		30		30	ns
5	Clock fall time	TfC		30		30	ns
6	Hold time for any specified setup time	Th	0		0		ns
7	$\overline{IORQ}$, $\overline{WR}$, $\overline{CE}$ ↓ to clock ↑ setup time	TsC(Cr)	280		145		ns
8	$\overline{RD}$ ↓ to data output delay	TdDO(RDf)		500		380	ns
9	Data in to clock ↑ setup ($\overline{WR}$ or $\overline{M1}$)	TsWM(Cr)	50		50		ns
10	$\overline{IORQ}$ ↓ to data out delay (INTA cycle)	TdCf(DO)		340		160	ns
11	$\overline{RD}$ ↑ to data float delay (output buffer disable)	TdRD(DZ)		160		110	ns
12	IEI ↓ to $\overline{IORQ}$ ↓ setup (INTA cycle)	TsIEI(IORQ)	140		140		ns
13	IEI ↑ to IEO ↑ delay	TdIEOr(IEIr)		210		160	ns
14	IEI ↓ to IEO ↓ delay	TdIEOf(IEIf)		190		130	ns
15	$\overline{M1}$ ↓ to IEO ↓ delay (interrupt just prior to $\overline{M1}$ ↓)	TdM1(IEO)		300		190	ns
16	$\overline{M1}$ ↓ to clock ↑ setup	TsMlf(Cr)	210		90		ns
17	$\overline{M1}$ ↑ to clock ↓ setup	TsMlr(Cf)	20		−10		ns
18	$\overline{RD}$ ↓ to clock ↑ setup ($\overline{M1}$ cycle)	TsRD(Cr)	240		115		ns
19	Interrupt cause to $\overline{INT}$ ↓ delay ($\overline{INT}$ generated only when DMA is inactive)	TdI(INT)		500		500	ns
20	$\overline{BAI}$ ↑ to $\overline{BAO}$ ↑ delay	TdBAIr(BAOr)		200		150	ns
21	$\overline{BAI}$ ↓ to $\overline{BAO}$ ↓ delay	TdBAIf(BAOf)		200		150	ns
22	RDY active to clock ↑ setup time	TsRDY(Cr)	150		100		ns

Note : ↑ Rising edge, ↓ Falling edge.
Note 1: Negative minimum setup values mean that the first-mentioned event can come after the second-mentioned event.



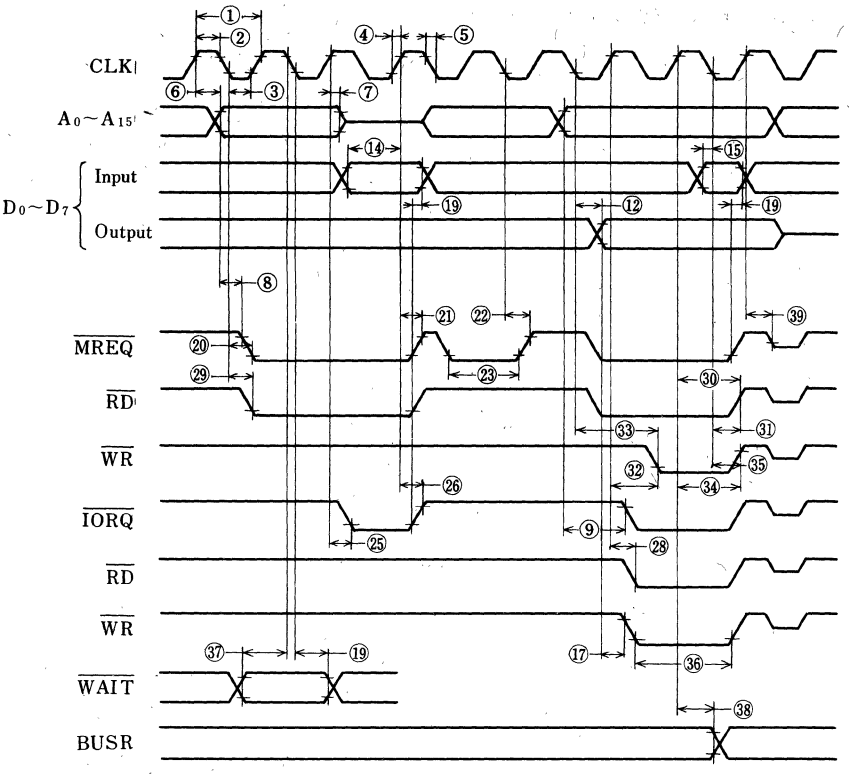
Acting as CPU peripheral (Inactive state)

(2) Acting as bus controller (active state)

(V_{CC}=5V±5%, Ta=0～+70℃)

No.	Parameter	Symbol	Z80 DMA		Z80A DMA		Unit
			MIN.	MAX.	MIN.	MAX.	
1	Clock cycle time	TcC	400		250		ns
2	Clock width (high)	TwCh	180	2000	110	2000	ns
3	Clock width (low)	TwCl	180	2000	110	2000	ns
4	Clock rise time	TrC		30		30	ns
5	Clock fall time	TfC		30		30	ns
6	Address output delay	TdA		145		110	ns
7	Clock ↑ to address float delay	TdC(AZ)		110		90	ns
8	Address to $\overline{MREQ}$ ↓ setup (memory cycle)	TsA(MREQ)	(2)+(5)−75		(2)+(5)−75		ns
9	Address stable to $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$ ↓ setup (I/O cycle)	TsA(IRW)	(1)−80		(1)−70		ns
*10	$\overline{RD}$, $\overline{WR}$ ↑ to addr. stable delay	TdRW(A)	(3)+(4)−40		(3)+(4)−50		ns
*11	$\overline{RD}$, $\overline{WR}$ ↑ to addr. float delay	TdRW(AZ)	(3)+(4)−60		(3)+(4)−45		ns
12	Clock ↓ to data out delay	TdCf(DO)		230		150	ns
*13	Clock ↑ to data float delay (write cycle)	TdCr(Dz)		90		90	ns
14	Data in to clock ↑ setup (read cycle when rising edge ends read)	TsDI(Cf)	50		35		ns
15	Data in to clock ↓ setup (read cycle when falling edge ends read)	TsDO(WfM)	60		50		ns
*16	Data out to $\overline{WR}$ ↓ setup (memory clcle)	TsDO(WPI)	(1)−210		(1)−170		ns
17	Data out to $\overline{WR}$ ↓ setup (I/O cycle)	TsDO(WPI)	100		100		ns
*18	$\overline{WR}$ ↑ to data out hold time	TdWr(DO)	(3)+(4)−80		(3)+(4)−70		ns
19	Hold time for any specified setup time	Th	0		0		ns
20	Clock ↓ to $\overline{MREQ}$ ↓ delay	TdCf(Mf)		100		85	ns
21	Clock ↑ to $\overline{MREQ}$ ↑ delay	TdCf(Mr)		100		85	ns
22	Clock ↓ to $\overline{MREQ}$ ↑ delay	TdCf(Mr)		100		85	ns
23	$\overline{MREQ}$ low pulse width	TwMl	(1)−40		(1)−30		ns
*24	$\overline{MREQ}$ high pulse width	TwMh	(2)+(5)−30		(2)+(3)−20		ns
25	Clock ↑ to $\overline{IORQ}$ ↓ delay	TdCr(If)		90		75	ns
26	Clock ↑ to $\overline{IORQ}$ ↑ delay	TdCr(Ir)		100		85	ns
*27	Clock ↓ to $\overline{IORQ}$ ↑ delay	TdCr(Ir)		110		85	ns
28	Clock ↑ to $\overline{RD}$ ↓ delay	TdCr(Rf)		100		85	ns
29	Clock ↓ to $\overline{RD}$ ↓ delay	TdCr(Rf)		130		95	ns
30	Clock ↑ to $\overline{RD}$ ↑ delay	TdCr(Rr)		100		85	ns
31	Clock ↓ to $\overline{RD}$ ↑ delay	TdCr(Rr)		110		85	ns
32	Clock ↑ to $\overline{WR}$ ↓ delay	TdCr(Wf)		80		65	ns
33	Clock ↓ to $\overline{WR}$ ↓ delay	TdCf(Wf)		90		80	ns
34	Clock ↑ to $\overline{WR}$ ↑ delay	TdCr(Wr)		100		80	ns
35	Clock ↓ to $\overline{WR}$ ↑ delay	TdCf(Wr)		100		80	ns
36	$\overline{WR}$ Low pulse width	TwWl	(1)−40		(1)−30		ns
37	$\overline{WAIT}$ to clock ↓ setup	TsWA(Cf)	70		70		ns
38	Clock ↑ to $\overline{BUSREQ}$ delay	TdCr(B)		150		100	ns
39	Clock ↑ to $\overline{IORQ}$, $\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$ float delay	TdCr(Iz)		100		80	ns

Note : ↑ Rising edge, ↓ Falling edge
Note 1: Numbers in parentheses are other parameter numbers in this table; their values should be substituted in equations.
Note 2: All equations imply DMA default (standard) timing.
Note 3: Data must be enabled onto data bus when RD is active.
Note 4: Asterisk (*) before parameter number means the parameter is not illustrated in the AC Timing Diagrams.



Acting as bus controller (active state)

■ Programming

The Z-80 DMA has two programmable fundamental states.

- an enabled state, in which it can gain control of the system buses and direct the transfer of data between ports, and
- a disabled state, in which it can initiate neither bus requests nor data transfers. When the DMA is powered up or reset by any means, it is automatically placed into the disabled state.

(1) Reading

The Read Registers (RR0-RR6) are read by the CPU by addressing the DMA as an I/O port using an Input instruction. The readable bytes contain DMA status, byte-counter values, and port addresses since the last DMA reset. The registers are always read in a fixed sequence beginning with RR0 and ending with RR6.

● **Read Register 0**

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
×	×	0	0	0	×	0	1	STATUS BYTE

1 = DMA TRANSFER HAS OCCURRED
0 = READY ACTIVE
0 = INTERRUPT PENDING
0 = MATCH FOUND
0 = END OF BLOCK
INTERRUPT PENDING

● **Read Register 1**

BYTE COUNTER (LOW BYTE)

● **Read Register 2**

BYTE COUNTER (HIGH BYTE)

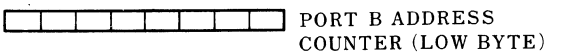
● **Read Register 3**

PORT A ADDRESS COUNTER (LOW BYTE)

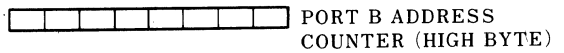
● **Read Register 4**

PORT A ADDRESS COUNTER (HIGH BYTE)

● **Read Register 5**



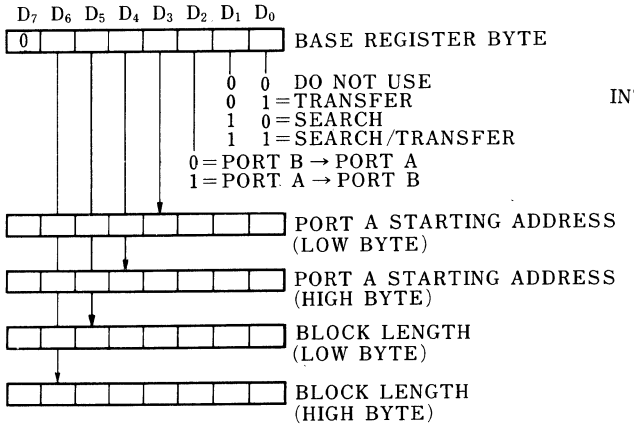
● **Read Register 6**



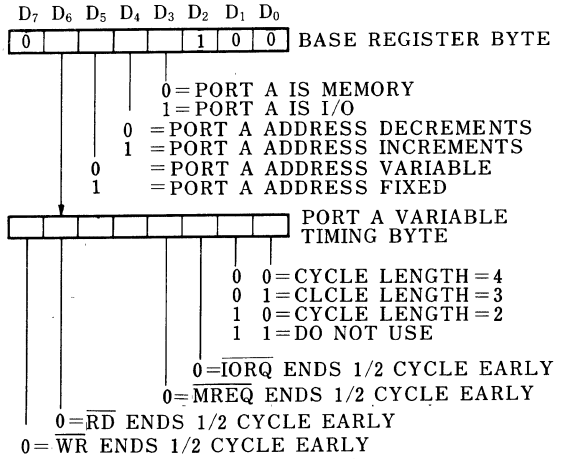
(2) Writing

Control or command bytes are written into one or more of the Write Register groups (WR0-WR6) by first writing to the base register byte in that group. All groups have base registers and most groups have additional associated registers. The associated registers in a group are sequentially accessed by first writing a byte to the base register containing register-group identification and pointer bits (I, s) to one or more of that base register's associated registers.

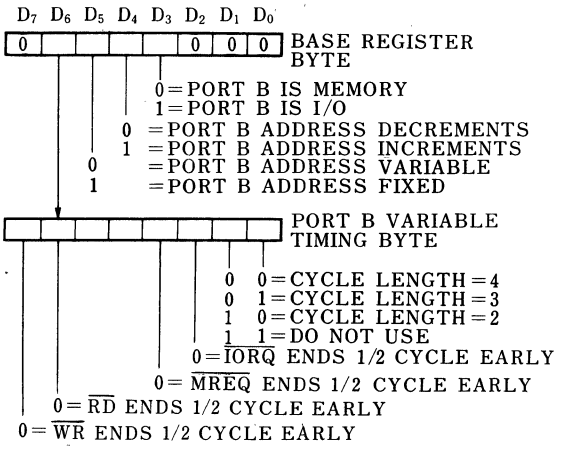
● **Write Register 0**



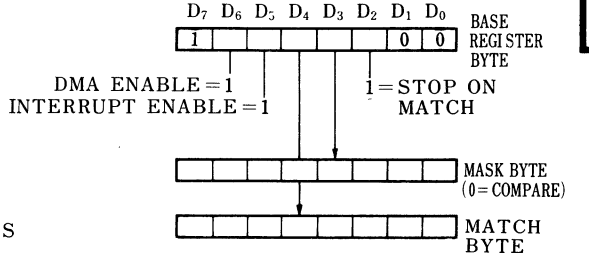
● **Write Register 1**



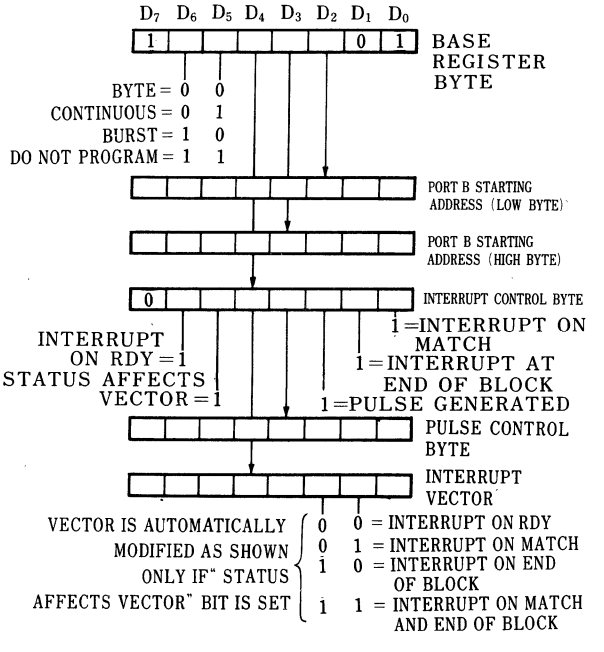
● **Write Register 2**



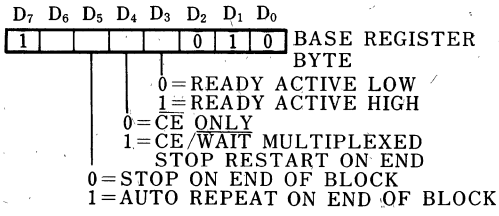
● **Write Register 3**



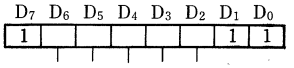
● **Write Register 4**



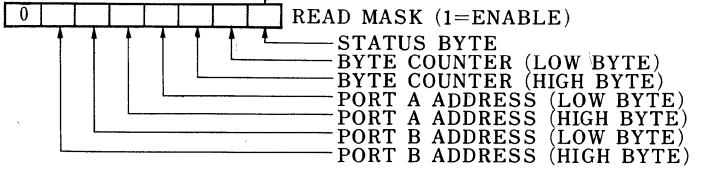
- **Write Register 5**



- **Write Register 6**



C3	1	0	0	0	0	INTERRUPT LINE RESET, INTERRUPT REQUEST AND BUS REQUEST DISABLE, INTERNAL READY STATE CLEAR, CE MULTIPLEX DISABLE, AUTOMATIC REPEAT STOP
C7	1	0	0	0	1	PORT A TIMING TO Z80 STANDARD TIMING
CB	1	0	0	1	0	PORT B TIMING TO Z80 STANDARD TIMING
CF	1	0	0	1	1	BOTH PORTS START ADDRESS LOAD, BYTE CONTER CLEAR
D3	1	0	1	0	0	ADDRESS CONTINUE FROM CURRENT VALUE, BYTE COUNTER CLEAR
AB	0	1	0	1	0	INTERRUPT ENABLE
AF	0	1	0	1	1	INTERRUPT DISABLE
A3	0	1	0	0	0	INTERRUPT CIRCUIT RESET AND DISABLE (SAME AS RETI), INTERNAL READY STATE CLEAR
87	0	0	0	0	1	DMA ENABLE } EFFECTIVE FOR ALL SECTIONS BUT INTERRUPT.
83	0	0	0	0	0	DMA DISABLE } NOT ALL FUNCTIONS RESETTABLE, HOWEVER
A7	0	1	0	0	1	READ SEQUENCE START FOR 1ST REGISTER DESIGNATED BY READ MASTER REGISTER
BF	0	1	1	1	1	STATUS REGISTER READ SETUP. FROM STATUS REGISTER FOR NEXT READ
B3	0	1	1	0	0	INTERNAL READY STATE TO BE FORCEDLY CLEAR OF "RDY" PIN (USED FOR DMA BETWEEN MEMORIES NEEDING NO RDY SIGNAL. NOT OPERATIVE IN "BYTE MODE")
88	0	0	0	1	0	REINITIALIZE. END-OF-BLOCK BIT CLEAR
B7	0	1	1	0	1	ENABLE AFTER RETI. BUS REQUEST ONLY AFTER RETI EXECUTION
BB	0	1	1	1	0	READ MASK FOLLOWS



■ Timing

(1) Inactive state timing (DMA as CPU Peripheral)

In its disabled or inactive state, the DMA is addressed by the CPU as an I/O peripheral for write and read (control and status) operations. Write timing is illustrated in Fig. 1.

Reading of the DMA's status byte, byte counter or port address counters is illustrated in Fig. 2.

(2) Active state timing (DMA as BUS Controller)

(i) Default read and write cycles

By default, and after reset, the DMA's timing of read and write operations is exactly the same as the Z-80 CPU's timing of read and write cycles for memory and I/O peripherals, with one exception: during a read cycle, data is latched on the falling edge of T_3 and held on the data bus across the boundary between read and write cycles, through the end of the following write cycle.

Fig. 3 illustrates the timing for memory to-I/O port transfers and Fig. 4 illustrates I/O-to-memory transfers. Memory-to-memory and I/O-to-I/O transfer timings are simply permutations of these diagrams.

The default timing uses three T-cycles for memory transactions and four T-cycles for I/O transactions, which include one automatically inserted wait cycle between T_2 and T_3. If the $\overline{CE}/\overline{WAIT}$ line is programmed to act as a $\overline{WAIT}$ line during the DMA's active state, it is sampled on the falling edge of T_2 for memory transactions and the falling edge of T_W for I/O transactions. If $\overline{CE}/\overline{WAIT}$ is Low during this time another T-cycle is added, during which the $\overline{CE}/\overline{WAIT}$ line will again be sampled. The duration of transactions can thus be indefinitely extended.

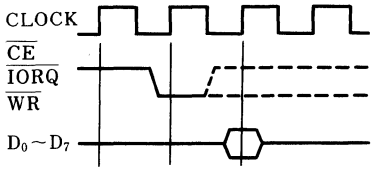


Fig. 1 CPU-DMA write cycle timing

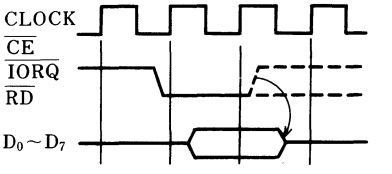


Fig. 2 CPU-DMA read cycle timing

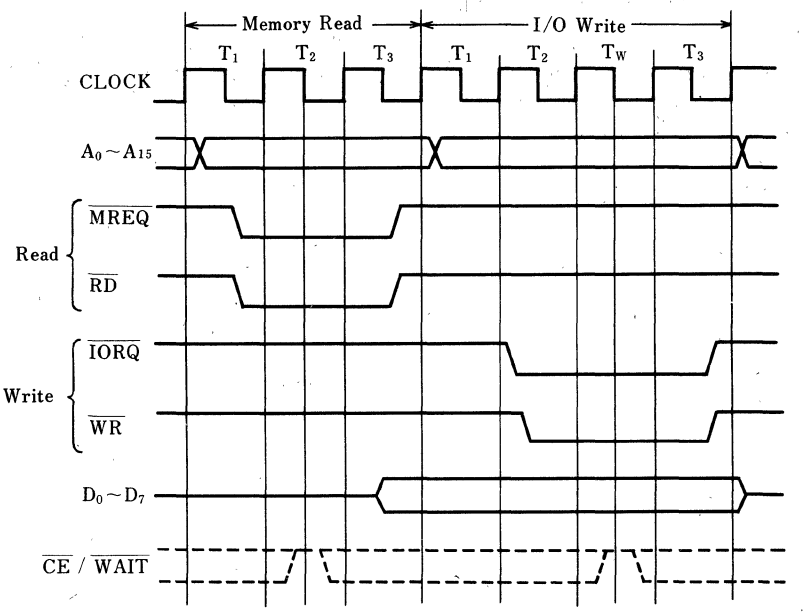


Fig. 3 Transfer from memory to I/O device

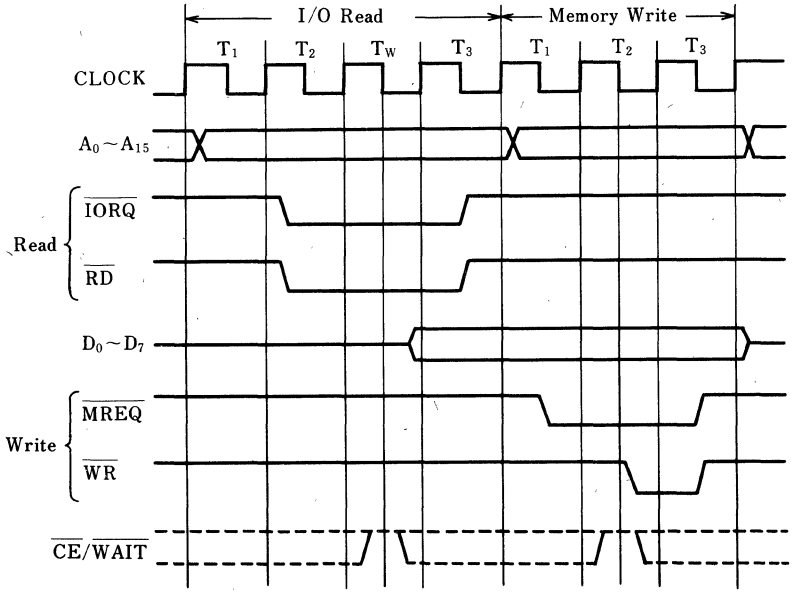


Fig. 4 Transfer from I/O device to memory

(ii) **Variable cycle and edge timing** The Z-80 DMA's default operation-cycle length for the source (read) port and destination (write) port can be independently programmed. This variable-cycle feature allows read or write cycles consisting of two, three or four T-cycles (more if Wait cycles are inserted), thereby increasing or decreasing the speed of all signals generated by the DMA. In addition, the trailing edges of the IORQ, MREQ, RD and WR signals can be independently terminated one-half cycle early. Fig. 5 illustrates this.

In the variable-cycle mode, unlike default timing, IORQ comes active one-half cycle before MREQ, RD and WR. CE/WAIT can be used to extend only the 3 or 4 T-cycle variable memory cycles and only the 4-cycle variable I/O cycle. The CE/WAIT line is sampled at the falling edge of T_2 for 3-or 4-cycle memory cycles, and at the falling edge of T_3 for 4-cycle I/O cycles.

During transfers, data is latched on the clock edge causing the rising edge of RD and held through the end of the write cycle.

(iii) **Bus requests** Fig. 6 illustrates the bus request and acceptance timing. The RDY line, which may be programmed active High or Low, is sampled on every rising edge of CLK.

If it is found to be active, and if the bus is not in use by any other device, the following rising edge of CLK drives BUSREQ low. After receiving BUSREQ the CPU acknowledges on the BAI input either directly or through a multiple-DMA daisy chain. When a Low is detected on BAI for two consecutive rising edges of CLK, the DMA will begin transferring data on the next rising edge of CLK.

(iv) **Bus release byte-at-a-time** In Byte at a Time mode, BUSREQ is brought High on the rising edge of CLK prior to the end of each read cycle (search-only) or write cycle (transfer and transfer/search) as illustrated in Fig. 7. This is done regardless of the state of RDY.

The next bus request for the next byte will come after both BUSREQ and BAI have returned High.

(v) **Bus release at end of block** In Burst and Continuous modes, an end of block causes BUSREQ to go High usually on the same rising edge of CLK in which the DMA completes the transfer of the data block (Fig. 8). The last byte in the block is transferred even if RDY goes inactive before completion of the last byte transfer.

(vi) **Bus release on not ready** In Burst mode, when RDY goes inactive it causes BUSREQ to go High on the next rising edge of CLK after the completion of its current byte operation (Fig. 9). The action on BUSREQ is thus somewhat delayed from action on the RDY line. The DMA always completes its current byte operation in an orderly fashion before releasing the bus.

By contrast, BUSREQ is not released in Continuous mode when RDY goes inactive.

Instead, the DMA idles after completing the current byte operation, awaiting an active RDY again.

(vii) **Bus release on match** If the DMA is programmed to stop on match in Burst or Continuous modes, a match causes BUSREQ to go inactive on the next DMA operation, i.e., at the end of the next read in a search or at the end of the following write in a transfer (Fig. 10). Due to the pipelining scheme, matches are determined while the next DMA read or write is being performed.

The RDY line can go inactive after the matching operation begins without affecting this bus-release timing.

(viii) **Interrupts** Timings for interrupt acknowledge and return from interrupt are the same as timings for these in other Z-80 peripherals. (Refer to the Z80 PIO.)

Interrupt on RDY (interrupt before requesting bus) does not directly affect the BUSREQ line. Instead, the interrupt service routine must handle this by issuing the following commands.

a. Enable after return from interrupt (RETI) (Command code 87_H)

b. Enable DMA (Command code 87_H)

c. An RETI instruction

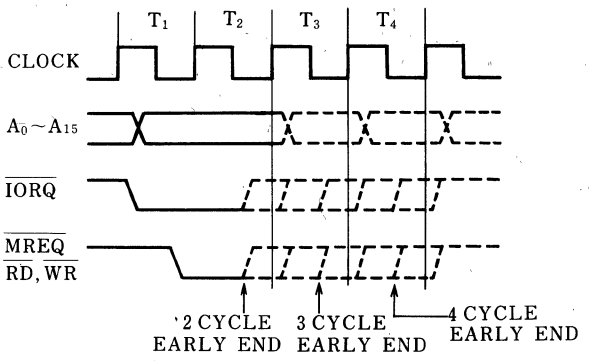


Fig. 5 Variable cycle and edge timing

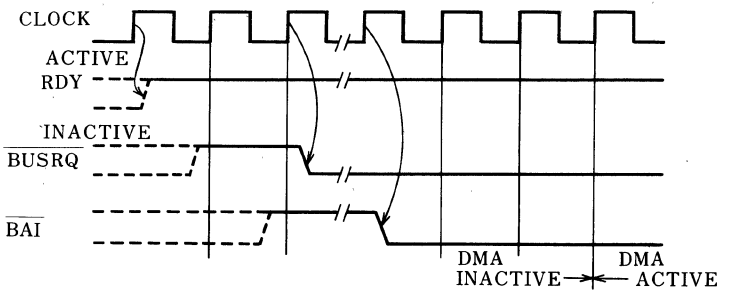


Fig. 6 Bus request and acknowledgement

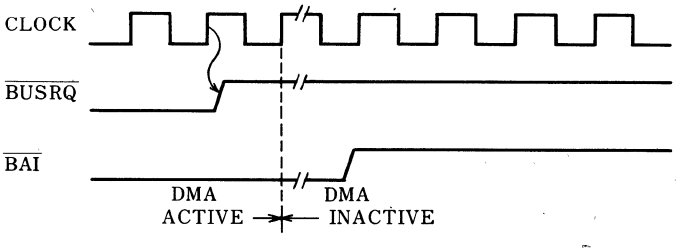


Fig. 7 Bus clear (byte mode)

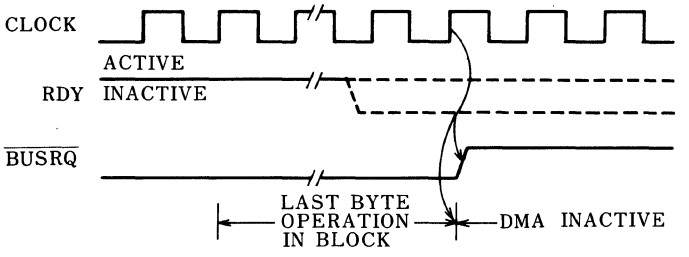


Fig. 8 End of block bus clear (burst, continuous mode)

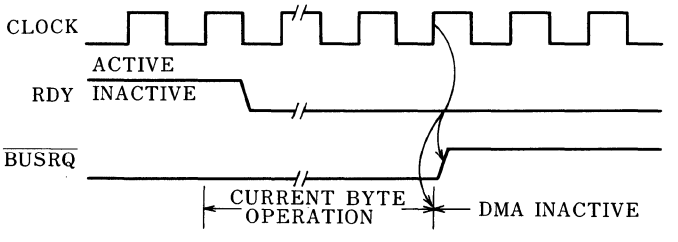


Fig. 9 No READY bus clear (burst mode)

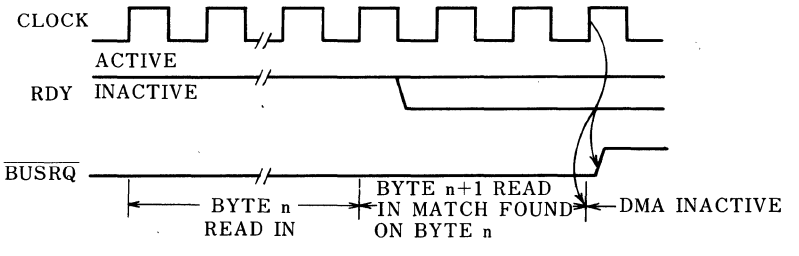


Fig. 10 Mating bus clear (burst, continuous mode)

LH0084/LH0084A/LH0084B
LH0085/LH0085A/LH0085B Z80/Z80A/Z80B Serial
LH0086/LH0086A/LH0086B Input/Output Controller

Description

The Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

The LH0084/85/86, Z80 SIO (Z80 SIO for short below) is a dual-channel multi-function peripheral component designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller, but—within that role—it is configurable by systems software so its "personality" can be optimized for a given serial data communications application.

The Z80 SIO is capable of handling asynchronous and synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device can also be used to support virtually any other serial protocol for applications other than data communications (cassette or floppy disk interfaces, for example).

The Z80 SIO can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

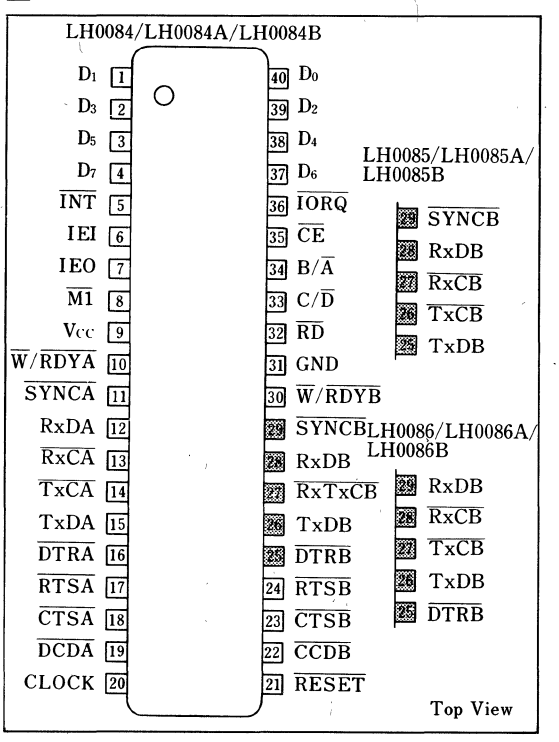
The Z80 SIO has six types as below according it's system clock and bonding option. The Z80A SIO and the Z80B SIO are a high speed version which can operate at the 4MHz and 6MHz system clock, respectively.

- LH0084 Z80 SIO/0
- LH0085 Z80 SIO/1
- LH0086 Z80 SIO/2
- LH0084A Z80A SIO/0
- LH0085A Z80A SIO/1
- LH0086A Z80A SIO/2
- LH0084B Z80B SIO/0
- LH0085B Z80B SIO/1
- LH0086B Z80B SIO/2

Features

1. N-channel silicon-gate process
2. Single +5V power supply and single phase clock
3. Two independent full duplex channels
4. Data rates : 0 to 500K bits/second (at 2.5 MHz system clock)
   : 0 to 800K bits/second (at 4MHz system clock)
   : 0 to 1200K bits/second (at 6MHz system clock)
5. Asynchronous operation
   - 5, 6, 7 or 8 bits/character
   - 1, 1½ or 2 stop bits/character
   - Even, odd or no parity
   - ×1, ×16, ×32 and ×64 clock modes
   - Break generation and detection
   - Parity, Overrun and Framing error detection
6. Binary synchronous operation
   - Internal or external character synchronization
   - One or two Sync characters in separate registers
   - Automatic Sync character insertion
   - CRC generation and checking
7. HDLC or IBM SDLC operation

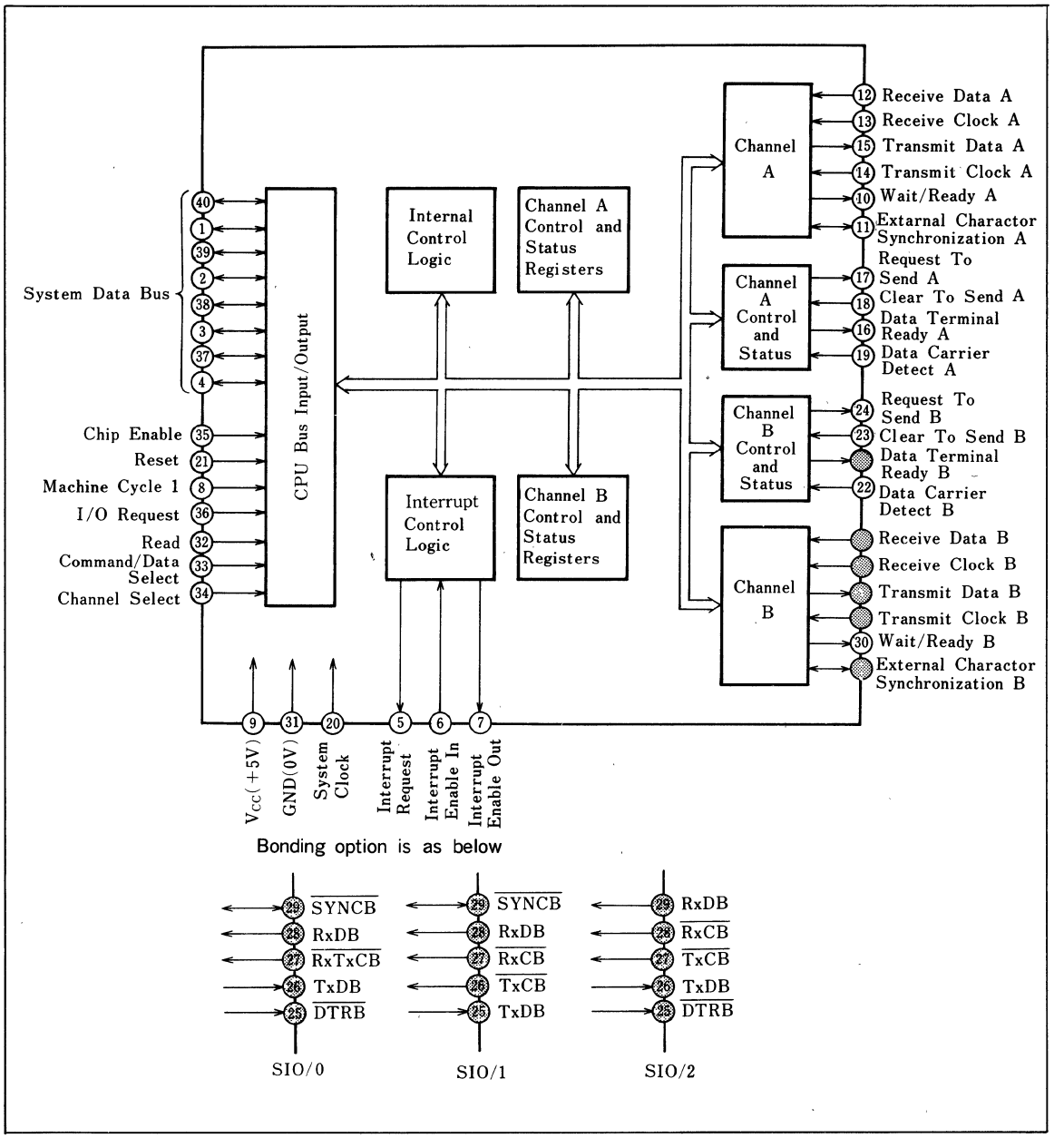
Pin Connections



- Abort sequence generation and detection
- Automatic zero insertion and detection
- Automatic flag insertion
- Address field recognition
- I-field residue handling
- Valid receive messages protected from overrun
- CRC generation and checking

8. Vectored daisy chain priority interrupt logic
9. CRC-16 or CRC-CCITT block check
10. Separate modem control inputs and outputs for both channels
11. Modem status can be monitored
12. 40-pin dual-in-line package

Block Diagram



Pin Description

Pin	Meaning	I/O	Function
$D_0 \sim D_7$	Data bus	Bidirectional 3-state	System data bus
B/$\overline{A}$	Channel A or B select	I	Defines which channel is accessed. Channel B at "High", channel A at "Low".
C/$\overline{D}$	Control or data select	I	Defines the type of information transfer on the data bus. Control word at "High", data at "Low".
$\overline{CE}$	Chip enable	I	Active "Low". A Low enables the CPU to transmit and receive control words and data.
CLOCK	System clock	I	Standard Z80 system clock used for internal synchronization signals.
$\overline{M1}$	Machine cycle one	I	Active "Low". Indicates that the CPU is acknowledging an interrupt, when both $\overline{M1}$ and $\overline{IORQ}$ are active.
$\overline{IORQ}$	Input/output request	I	Active "Low". Read operation when $\overline{RD}$ is active, and write operation when it is not active. Indicates that the CPU is acknowledging an interrupt, when both $\overline{IORQ}$ and $\overline{M1}$ are active.
$\overline{RD}$	Read cycle status	I	Active "Low". Read operation when active.
$\overline{RESET}$	Reset	I	Active "Low". Resets the interrupt bits.
IEI	Interrupt enable in	I	Active "High". Used to form a priority-interrupt daisy chain.
IEO	Interrupt enable out	O	Active "High". Used to form a priority-interrupt daisy chain.
$\overline{INT}$	Interrupt request	Open drain, O	Active "Low". Active when requesting an interrupt.
$\overline{W/RDYA}$ $\overline{W/RDYB}$	Wait/ready	Open drain, O	Active "Low". $\overline{READY}$ when the DMA is a bus master, $\overline{WAIT}$ when the CPU is a bus master.
$\overline{CTSA}$, $\overline{CTSB}$	Clear to send	I	Active "Low". Enables the respective transmitters. Also applicable as general-purpose input pins.
$\overline{DCDA}$, $\overline{DCDB}$	Data carrier detect	I	Active "Low". Enables the respective receivers. Also applicable as general-purpose input pins.
RxDA, RxDB	Receive data	I	Active "Low". Data line for receiving
TxDA, TxDB	Transmit data	O	Active "Low". Data line for transmitting.
$\overline{RxCA}$, $\overline{RxCB}$	Receiver clock	I	Active "Low". Receiving synchronization clock.
$\overline{TxCA}$, $\overline{TxCB}$	Transmitter clock	I	Active "Low". Transmitting synchronization clock.
$\overline{RTSA}$, $\overline{RTSB}$	Request to send	O	Active "Low". Indicates that the transmitter is empty during transfer. Also applicable as general-purpose output pins.
$\overline{DTRA}$, $\overline{DTRB}$	Data terminal ready	O	Active "Low". Also applicable as general-purpose output pins.
$\overline{SYNCA}$, $\overline{SYNCB}$	External character synchronization	I	Active "Low". Acts the same way as $\overline{CTS}$ and $\overline{DCD}$ in the asynchronous mode. Driven "Low" in the synchronous mode when a synchronizing pattern is achieved.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7	V
Output voltage	V_{OUT}	−0.3～+7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock input low voltage	V_{ILC}		−0.3		0.45	V
Clock input high voltage	V_{IEC}		Vcc−0.6		5.5	V
Input low voltage	V_{IL}		−0.3		0.8	V
Input high voltage	V_{IH}		2.0		5.5	V
Output low voltage	V_{OL}	I_{OL}=2.0mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4			V
Input leakage current	$\|I_{LI}\|$	$0<V_{IN}<V_{CC}$			10	μA
3-state output/data bus input leakage curreut	$\|I_Z\|$	$0<V_{IN}<V_{CC}$			10	μA
$\overline{SYNC}$ pin leakage current	$I_{L(SY)}$	$0<V_{IN}<V_{CC}$	−40		10	μA
Current consumption	I_{CC}				100	mA

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground			40	pF
Input capacitance	C_{IN}				5	pF
Output capacitance	C_{OUT}				10	pF

■ AC Characteristics

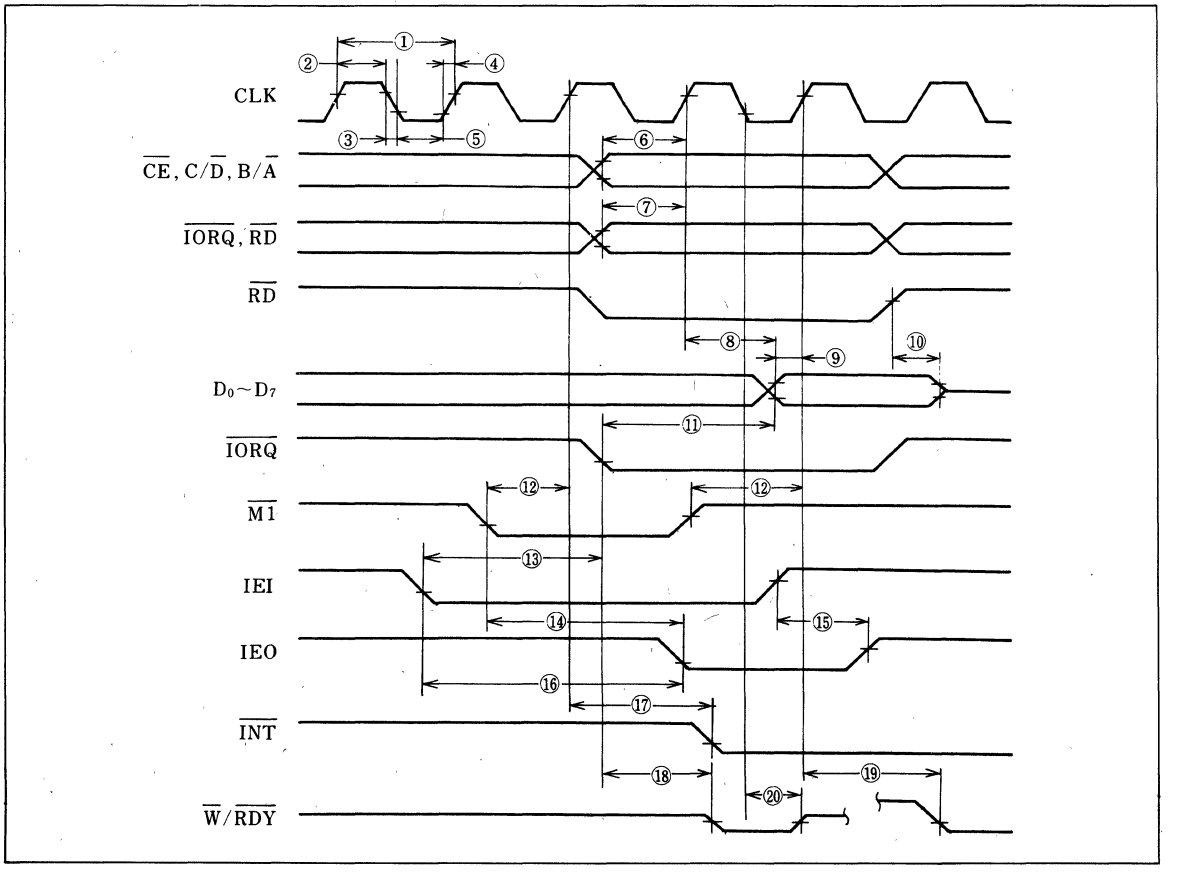
(1) AC characteristics (I)

No.	Parameter	Symbol	Z80 SIO		Z80A SIO		Z80B SIO		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
1	Clock cycle time	TcC	400	4000	250	4000	165	4000	ns
2	Clock width (high)	TwCh	170	2000	105	2000	70	2000	ns
3	Clock fall time	TfC		30		30		15	ns
4	Clock rise time	TrC		30		30		15	ns
5	Clock width (low)	TwCl	170	2000	105	2000	70	2000	ns
6	$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to clock ↑ setup time	TsAD(C)	160		145		60		ns
7	$\overline{IORQ}$, $\overline{RD}$ to clock ↑ setup time	TsCS(C)	240		115		60		ns
8	Clock ↑ to data out delay	TdC(DO)		240		220		150	ns
9	Data in to clock ↑ setup (Write or $\overline{M1}$ cycle)	TsDI(C)	50		50		30		ns
10	$\overline{RD}$ ↑ to data out float delay	TdRD(DOz)		230		110		90	ns
11	$\overline{IORQ}$ ↓ to data out delay (INTACK cycle)	TdIO(DOI)		340		160		100	ns

No.	Parameter	Symbol	Z80 SIO		Z80A SIO		Z80B SIO		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
12	$\overline{M1}$ to clock ↑ setup time	TsM1(C)	210		90		75		ns
13	IEI to $\overline{IORQ}$ ↓ setup time (INTACK cycle)	TsIEI(IO)	200		140		120		ns
14	$\overline{M1}$ ↓ to IEO ↓ delay (interrupt before $\overline{M1}$)	TdM1(IEO)		300		190		160	ns
15	IEI ↑ to IEO ↑ delay (after ED decode)	TdIEI(IEOr)		150		100		70	ns
16	IEI ↓ to $\overline{INT}$ ↓ delay	TdIEI(IEOf)		150		100		70	ns
17	Clock ↑ to $\overline{INT}$ ↓ delay	TdC(INT)		200		200		150	ns
18	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{W}/\overline{RDY}$ ↓ delay (wait mode)	TdIO(W/RWf)		300		210		175	ns
19	Clock ↑ to $\overline{W}/\overline{RDY}$ ↓ delay (ready mode)	TdC(W/PR)		120		120		100	ns
20	Clock ↓ to $\overline{W}/\overline{RDY}$ float delay (wait mode)	TdC(W/RWz)		150		130		110	ns
21	Any unspecified hold when setup is specified	Th	0		0		0		ns

↑ Rising edge, ↓ Falling edge.

(2) AC timing chart (I)



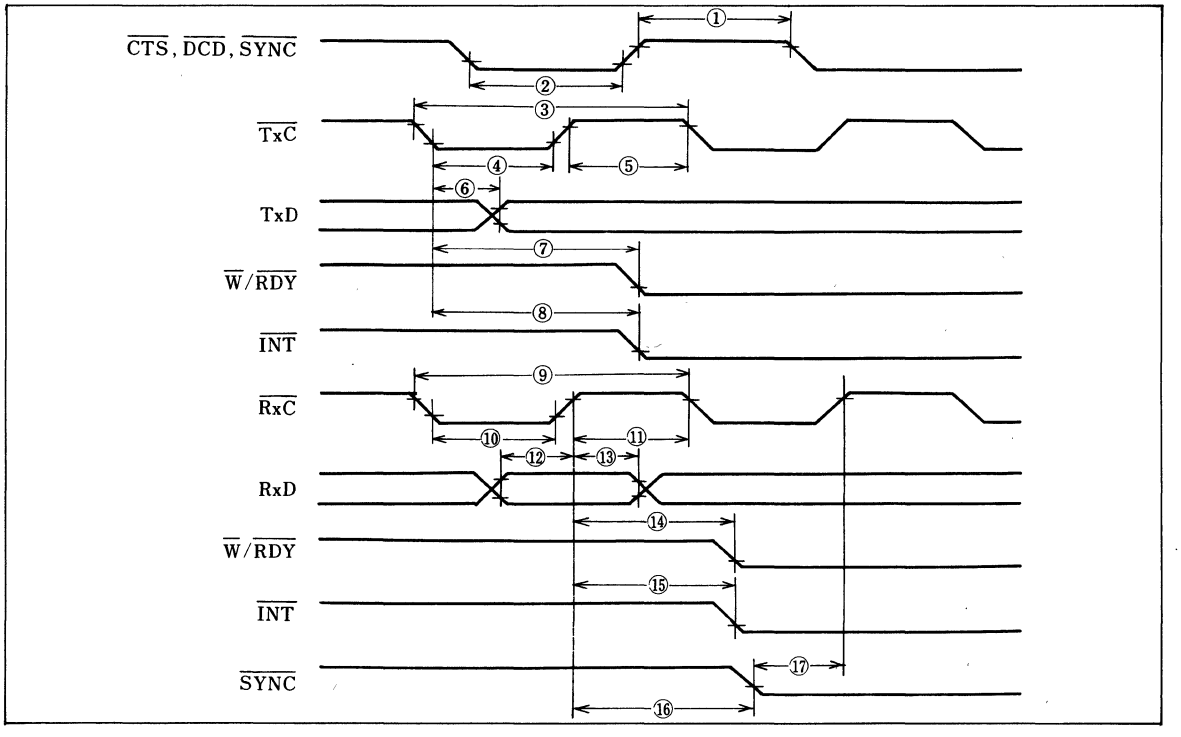
(3) AC characteristics (Ⅱ)

No.	Parameter	Symbol	Z80 SIO		Z80A SIO		Z80B SIO		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
1	Pulse width (high)	TwPh	200		200		200		ns
2	Pulse width (low)	TwPl	200		200		200		ns
3	$\overline{TxC}$ clock time	TcTxC	400	∞	400	∞	330	∞	ns
4	$\overline{TxC}$ width (low)	TwTxCl	180	∞	180	∞	100	∞	ns
5	$\overline{TxC}$width (high)	TwTxCh	180	∞	180	∞	100	∞	ns
6	$\overline{TxC}$ ↓ to TxD delay (xl mode)	TdTxC(TxD)		400		300		220	ns
7	$\overline{TxC}$ ↓ to $\overline{W}/\overline{RDY}$ ↓ delay (ready mode)	TdTxC(W/RRf)	5	9	5	9	5	9	Clock period
8	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ delay	TdTxC(INT)	5	9	5	9	5	9	Clock period
9	$\overline{RxC}$ cycle time	TdRxC	400	∞	400	∞	330	∞	ns
10	$\overline{RxC}$ width (low)	TwRxCl	180	∞	180	∞	100	∞	ns
11	$\overline{RxC}$ width (high)	TwRxCh	180	∞	180	∞	100	∞	ns
12	$\overline{RxD}$ to $\overline{RxC}$ ↑ setup time (xl mode)	TsRxD(RxC)	0		0		0		ns
13	$\overline{RxC}$ ↑ to $\overline{RxD}$ hold time (xl mode)	ThRxD(RxC)	140		140		100		ns
14	$\overline{RxC}$ ↑ to $\overline{W}/\overline{RDY}$ ↓ delay (ready mode)	TdRxC(W/RRf)	10	13	10	13	10	13	Clock period
15	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ delay	TdRxC(INT)	10	13	10	13	10	13	Clock period
16	$\overline{RxC}$ ↑ to $\overline{SYNC}$ ↓ delay (output modes)	TdRxC(SYNC)	4	7	4	7	4	7	Clock period
17	$\overline{SYNC}$ ↓ to $\overline{RxC}$ ↓ setup (external sync modes)	TsSYNC(RxC)	−100		−100		100		ns

↑ Rising edge, ↓ Falling edge

Note: In all mode, the System Clock rate must be at least five times the maximum data rate.

(4) AC timing chart (Ⅱ)



■ Transmit and Receive Data Path

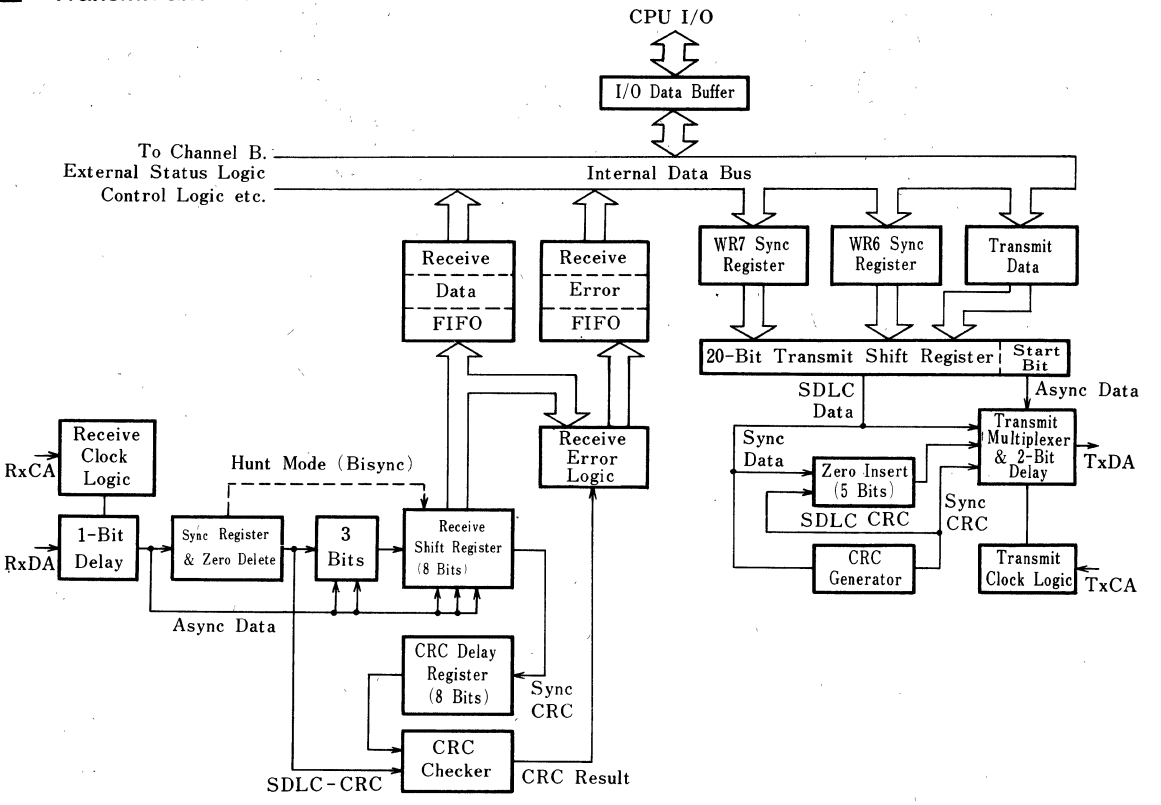


Fig. 1 Transmit and receive data path

■ Programming

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected mode.

Both channels contain registers that must be programmed via the system program prior to operation.

(1) Read Registers

The SIO contains three read registers for Channel B and three read registers for Channel A (RR0-RR2) that can be read to obtain the status information. The status information includes error conditions, interrupt vector and standard communications-interface signals

● **Read Register 0 (RR 0)**

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Break /abort	Tx under-run /EOM	CTS	Sync /hunt	DCD	Tx buffer empty	INT pending (ch.A only)	Rx character available

● **Read Register 1 (RR 1)**

The RR1 contains the status bits for specific receiving coditions as well as the one-field fraction codes for the SDLC receive mode.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
End of frame	CRC/ framing error	Rx overrun error	Parity error	Fraction code 2	Fraction code 1	Fraction code 0	All sent

● **Read Register 2 (RR 2)**

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

Valiable if "status affects vector" is programmed

(2) Write Registers

The SIO contains eight write registers for Channel B and eight write registers for Channel A (WR0-WR7) that are programmed separately to configure the functional personality of the channels.

● Write Register 0 (WR 0)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CRC reset code 1	CRC reset code 0	Command bit 2	Command bit 1	Command bit 0	Pointer bit 2	Pointer bit 1	Pointer bit 0
		Control words			Register pointers		

● Write Register 1 (WR 1)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Wait/ ready enable	Wait/ ready function	Wait/ ready onR/T	Receive inter- rupt mode 1	Receive inter- rupt mode 0	Status affects vector	Tx INT enable	Ext INT enable

● Write Register 2 (WR 2)

The WR2 contains the interrupt vector for both channels and is only in the Channel B. When the status affected vector (WR1, D_2) is 1, the vector from the SIO during the interrupt acknowledge cycle varies (V_3 - V_1) depending on the interrupt conditions. The WR2 contents do not vary then.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

● Write Register 3 (WR 3)

The WR 3 contains the bits and parameters to control the receivers.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Rx bits char- acter 1	Rx bits char- acter 0	Auto enable	Enter hunt phase	Rx CRC enable	Address search mode	Sync charac- ter load inhibit	Rx enable

● Write Register 4 (WR 4)

The WR4 has the bits control both receivers and transmitters.

In initializing for transmitting and receiving, these bits must be set up before the WR1, WR3, WR5, WR6, and WR7.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Clock rate 1	Clock rate 0	Sync mode 1	Sync mode 0	Stop bit 1	Stop bit 0	Parity Even /ODD	Parity enable

● Write Register 5 (WR 5)

The WR5 contains the bits (except for D_2) to control the transmitters.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DTR	Tx bits /char- acter 1	Tx bits /char- acter 0	Send break	Tx enable	CRC16 /SDLC	RTS	Tx CRC enable

● Write Register 6 (WR 6)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SYNC 7	SYNC 6	SYNC 5	SYNC 4	SYNC 3	SYNC 2	SYNC 1	SYNC 0

● Write Register 7 (WR 7)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SYNC 15	SYNC 14	SYNC 13	SYNC 12	SYNC 11	SYNC 10	SYNC 9	SYNC 8

■ Timing

(1) Read cycle

The timing signals generated by a Z-80 CPU input instruction to read a data or status byte from the SIO are illustrated in Fig. 2.

(2) Write cycle

Fig. 3 illustrates the timing and data signals generated by a Z-80 CPU output instruction to write a data or control byte into the SIO.

(3) Interrupt cycle

The interrupt-acknowledging and return-from-interrupt cycles are of the same timing as for other Z80 peripherals. (Refer to the Z80 PIO.)

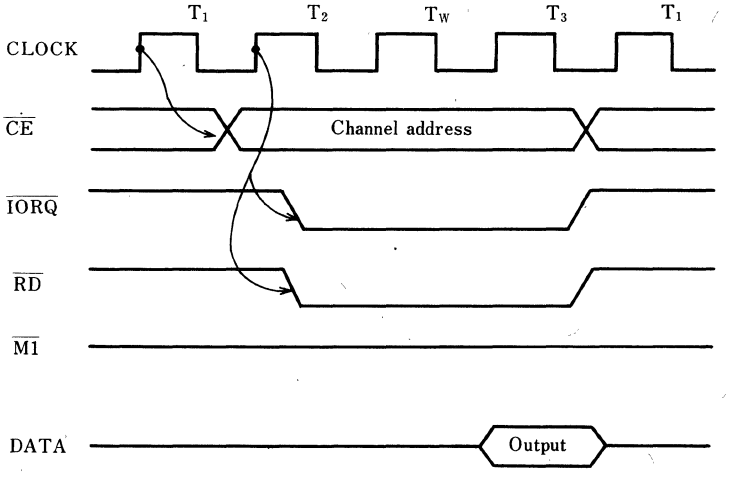


Fig. 2 Read cycle timing

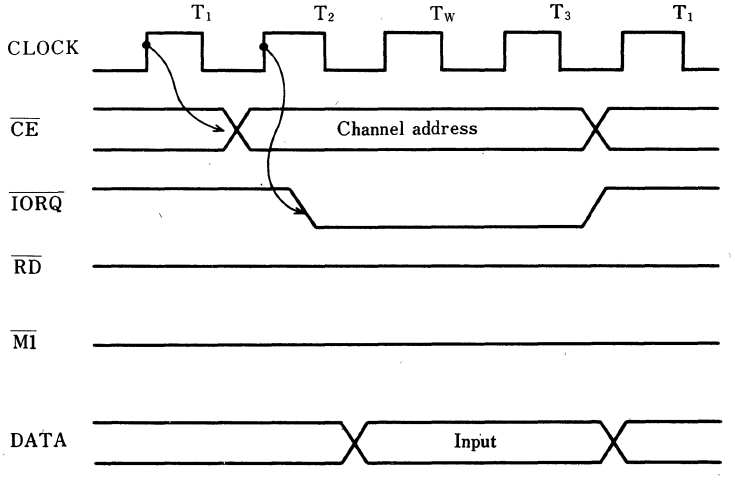


Fig. 3 Write cycle timing

LH0110/LH0110A Floppy Disk Controller

■ Description

The LH0110 is a micro-program controlled Floppy Disk Controller (FDC) designed as one of the Z80 peripherals.

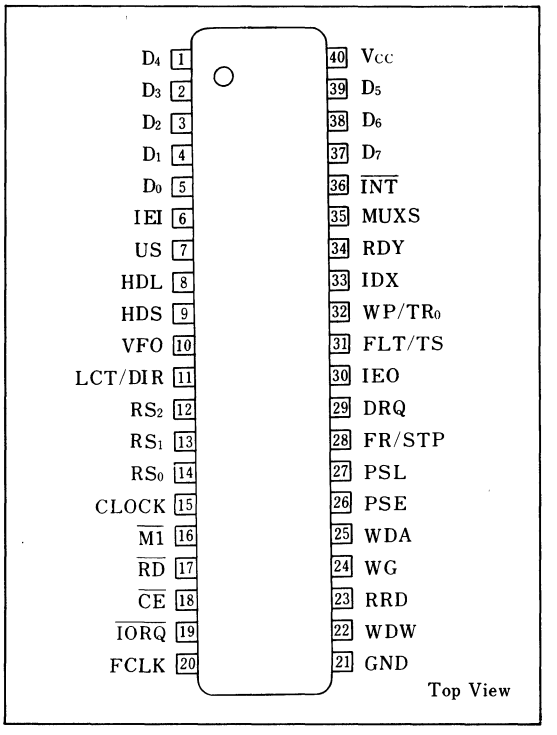
The LH0110 is fabricated with N-channel silicon-gate process technology, and packaged in a 40-pin dual-in-line package.

The LH0110 provides a TTL compatible interface and requires a single +5V power supply.

■ Features

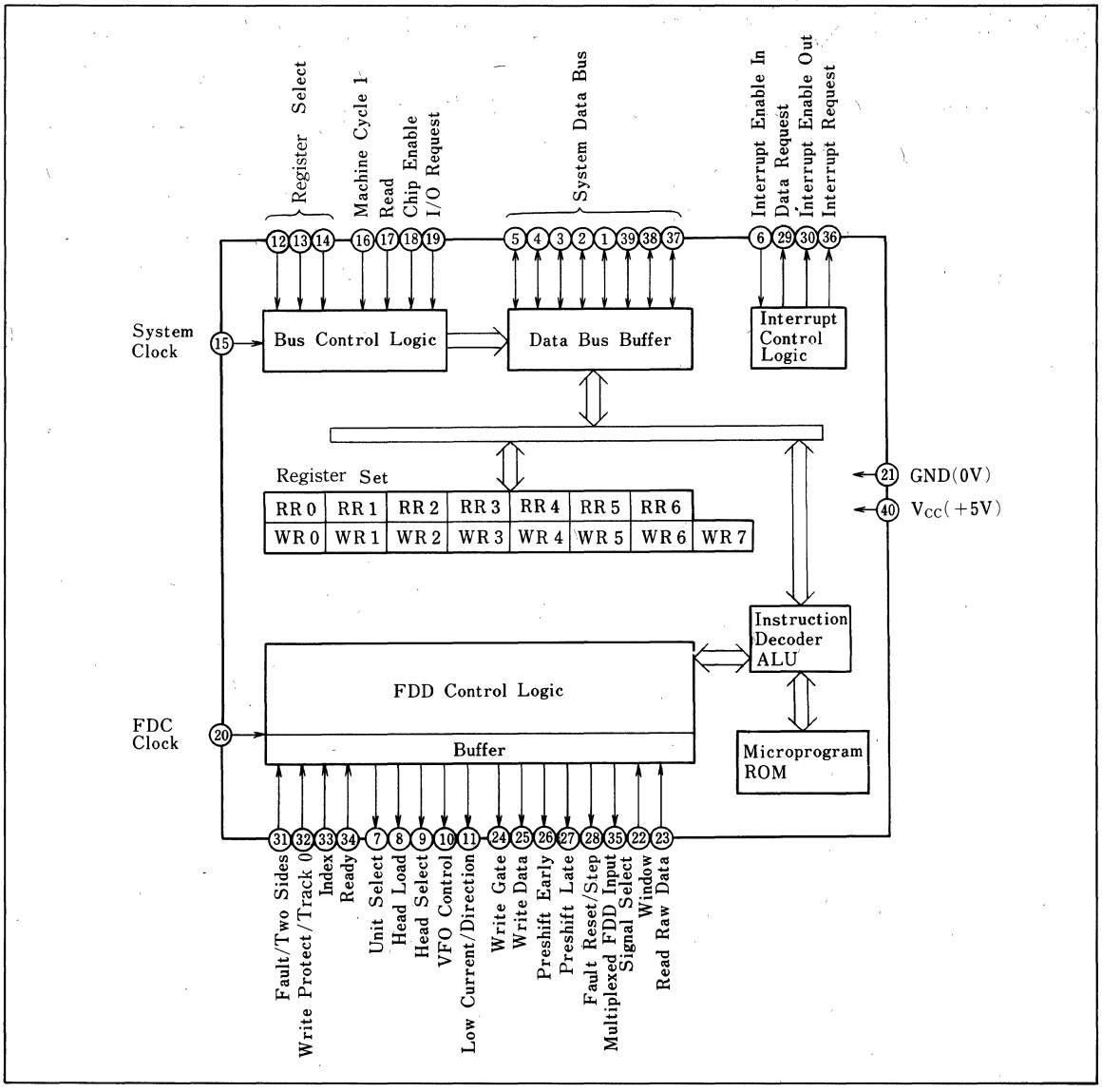
1. Can be connected directly to the Z80 CPU bus
   - Daisy chain interrupt signal
   - Interrupt vector output
   - Recognition of the Z80 CPU RETI instruction
2. DMA or program controlled data transfers
3. Separate clocks for system control and FDD control.
4. Can be connected to other microprocessors
5. IBM format compatible
   - Single-sided, Dual-sided (FM)
     Dual-sided double-density (MFM)
   - FM: 128, 256, 512 bytes/sector
     MFM: 256, 512, 1024 bytes/sector
   - 8, 15, 26 sectors/track
6. Can control minifloppies (change the 2MHz FCLK to a 1MHz clock)
7. Can control 2 dual-sided double-density floppy disk drives (4 single-sided drives)
8. A wealth of commands including VERIFY command
   *Can be specified as head load or head unload
9. A wealth of error status indicators available during command processing
10. CRC generation and checking ($X^{16}+X^{12}+X^5+1$)
11. Deleted data address mark (DDAM) processing capabilities
12. Multi-sector processing capabilities
13. Signals generated for adjusting write data under MFM recording
14. Inner track processing capabilities
15. Stepping speed, head load time and head unload time after command processing are programmable

■ Pin Connections



16. Interrupt enable and disable are programmable
17. Window inversion is programmable
18. Input/Output is TTL compatible (except for clocks)

■ Block Diagram



Pin Description

Pin	Meaning	I/O	Function
$D_0 \sim D_7$	Data bus	Bidirectional 3-state	System data bus
$RS_0 \sim RS_2$	Register select	I	Used to select FDC internal register (RR0-RR6, WR0-WR7).
$\overline{M1}$	Machine cycle 1	I	Active low. Produced by ANDing $\overline{M1}$ and $\overline{RESET}$* of CPU. Active $\overline{M1}$ with $\overline{IORQ}$ causes interrupt.
$\overline{RD}$	Read cycle	I	Active low. Read operations proceed when active.
$\overline{CE}$	Chip enable	I	Active low. Command or data transactions with CPU possible when active.
$\overline{IORQ}$	I/O request	I	Active low. Active $\overline{RD}$ designates read operation ; inactive $\overline{RD}$ designates write operation. Interrupt occurs when $\overline{IORQ}$ and $\overline{M1}$ are simultaneously active.
CLOCK	System clock	I	Standard Z80 system clock is used as internal sync signal.
FCLK	FDC clock	I	2-MHz clock is used for synchronizing FDD control signal(1-MHz clock for mini-floppy control).
IEI	Interrupt enable input	I	Active high. Used to form interrupt priority arbitration loop circuit (daisy chain).
$\overline{IEO}$	Interrupt enable output.	O	Active high. Used with IEI to form daisy chain.
$\overline{INT}$	Interrupt request	Open-drain O	Active low. Active when placing interrupt request.
DRQ	Data request to DMA	O	Active high. Data request signal for transactions between FDC and DMA.
MUXS	Multiplex	O	Multiplexer select signal.
WP/TR_0	Write protect/track zero	I	Active high. WP signal at high MUXS, indicating that mounted diskette is write-protected. TR_0 signal at low MUXS, indicating that the head is positioned at track 0.
FLT/TS	Fault/2-side disk	I	Active high. FLT signal at high MUXS, indicating fault status of FDD. TS signal at low MUXS, indicating that 2-side disk is mounted.
FR/STP	Fault reset/step	O	Active high. FR signal at high MUXS, resetting fault status of FDD. STP signal at low MUXS, indicating seek.
LCT/DIR	Low current/direction	O	Active high. Connected to FDD low current input and direction input. Denotes LCT signal except when seek command is in effect, becoming high when head selects a cylinder above track 44. DIR signal during seek command, becoming high when seek direction is toward disk center (from perimeter).
RDY	Ready	I	Active high. FDD ready signal
IDX	Index	I	Active high. Indicates the physical starting point on the disk track.
HDS	Head select	O	With double-sided FDD, low HDS selects head 0 ; high HDS selects head 1. With single-sided FDD, HDS can be used as FDD select signal.
HDL	Head load	O	Active high. Puts the FDD head in load state.
US	Unit select	O	Active high. Selects FDD unit.
WG	Writing gate	O	Active high. Write command to FDD.
WDA	Write data	O	Active high. Serial data transferred to FDD.
RRD	Read data	I	Active high. Serial data from FDD.
WDW	Window	I	Released by VFO circuit, used in separating RRD data and clock.

Pin	Meaning	I/O	Function
VFO	VFO control	O	Active high. Advises lock timing to VFO circuit.
PSL	Pre-shift	O	Active high. Write correction signal in MFM mode, instructing external write-correction circuit to delay WDA. Maintains active status in FM mode.
PSE	Pre-shift early	O	Active high. Write-correction signal in MEM mode, instructing external write-correction circuit to accelerate WDA. Maintains active status in FM mode.

*Resetting FDC FDC has no reset terminal, but by maintaining $\overline{M1}$ at low for more than 2-clock lengths when both $\overline{IORQ}$ and $\overline{RD}$ are high, the FDC's internal reset flag is set and FDC reset is in effect. Reset status can be released by making access to an FDC register.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7	V
Output voltage	V_{OUT}	−0.3～+7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Clock input low voltage	V_{CL}			−0.3		0.45	V
Clock input high voltage	V_{CH}			V_{CC}−0.6		V_{CC}+0.3	V
Input low voltage	V_{IL}			−0.3		0.8	V
Input high voltage	V_{IH}			2.0		V_{CC}	V
Output low voltage	V_{OL}	I_{OL}=2.0mA				0.4	V
Output high voltage	V_{OH}	I_{OH}=−250 μA		2.4			V
Input leakage current	$\lvert I_{LI} \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$				10	μA
Data bus I/O leakage current	$\lvert I_Z \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$				10	μA
Supply current	I_{CC}		LH0110			170	mA
			LH0110A			180	

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Clock input capacitance	C_{CLOCK}	All pins except the one to be tested should be grounded.		10	pF
Input capacitance	C_{IN}			7	pF
Output capacitance	C_{OUT}			10	pF
Input/Output capacitance	$C_{I/O}$			12	pF

■ AC Characteristics

(1) CPU interface

(V_{CC}=5V±5%, Ta=0~+70℃)

No.	Parameter	Symbol	LH0110		LH0110A		Unit
			MIN.	MAX.	MIN.	MAX.	
1	Clock period	TcC	400	[1]	250	[1]	ns
2	Clock pulse width, high	TwCh	170	2000	105	2000	ns
3	Clock pulse width, low	TwCl	170	2000	105	2000	ns
4	Clock rise time	TfC	0	30	0	30	ns
5	Clock fall time	TrC	0	30	0	30	ns
6	Hold time	Th	0		0		ns
7	Setup time to clock ↑ under read/write cycle.	TsCE(C)	240		145		ns
8	Delay time from $\overline{RD}$ ↓ to data output under read cycle.	TdRI(DO)		500		380	ns
9	Data setup time to clock ↑ under write/M1 cycle.	TsDI(C)	50		50		ns
10	Delay time from $\overline{IORQ}$ ↓ to data output (interrupt cycle).	TdIO(DIO)		340		160	ns
11	Delay time to bus floating.	TdRI(DOs)		160		110	ns
12	IEI setup time to $\overline{IORQ}$ ↓ (interrupt cycle).	TsIEI(IO)	200		140		ns
13	Delay time from IEI ↑ to IEO ↑.	TdIEI(IEOr)		210		160	ns
14	Delay time from IEI ↓ to IEO ↓	TdIEI(IEOf)		190		130	ns
15	Delay time from $\overline{M1}$ ↓ to IEO ↓ (at interrupt before $\overline{M1}$ ↓)	TdM1(IEO)		300		190	ns
16	$\overline{M1}$ ↓ setup time to clock ↑ under INTA/M1 cycle.	TsM1(Cr)	210		90		ns
17	$\overline{RD}$ ↓ setup time to clock ↑ under read/M1 cycle.	TsRI(C)	240		115		ns
18	Delay time from FCLK ↓ to $\overline{INT}$ output	TdC(INT)		300		300	ns
19	$\overline{IORQ}$ ↓ setup time to clock ↑ under I/O cycle.	Ts(IO)	240		115		ns

(1) TcC=TwCh+TwCl+TfC+TrC.
↑ indicates rising edge, ↓ indicates falling edge.

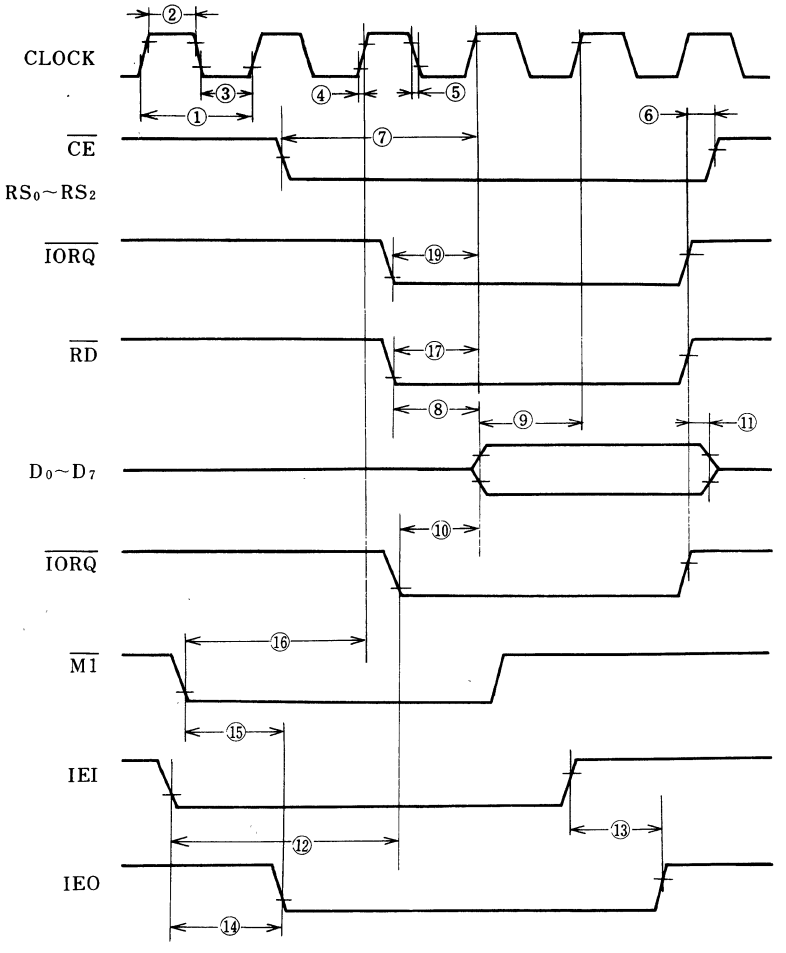
(2) FDD interface

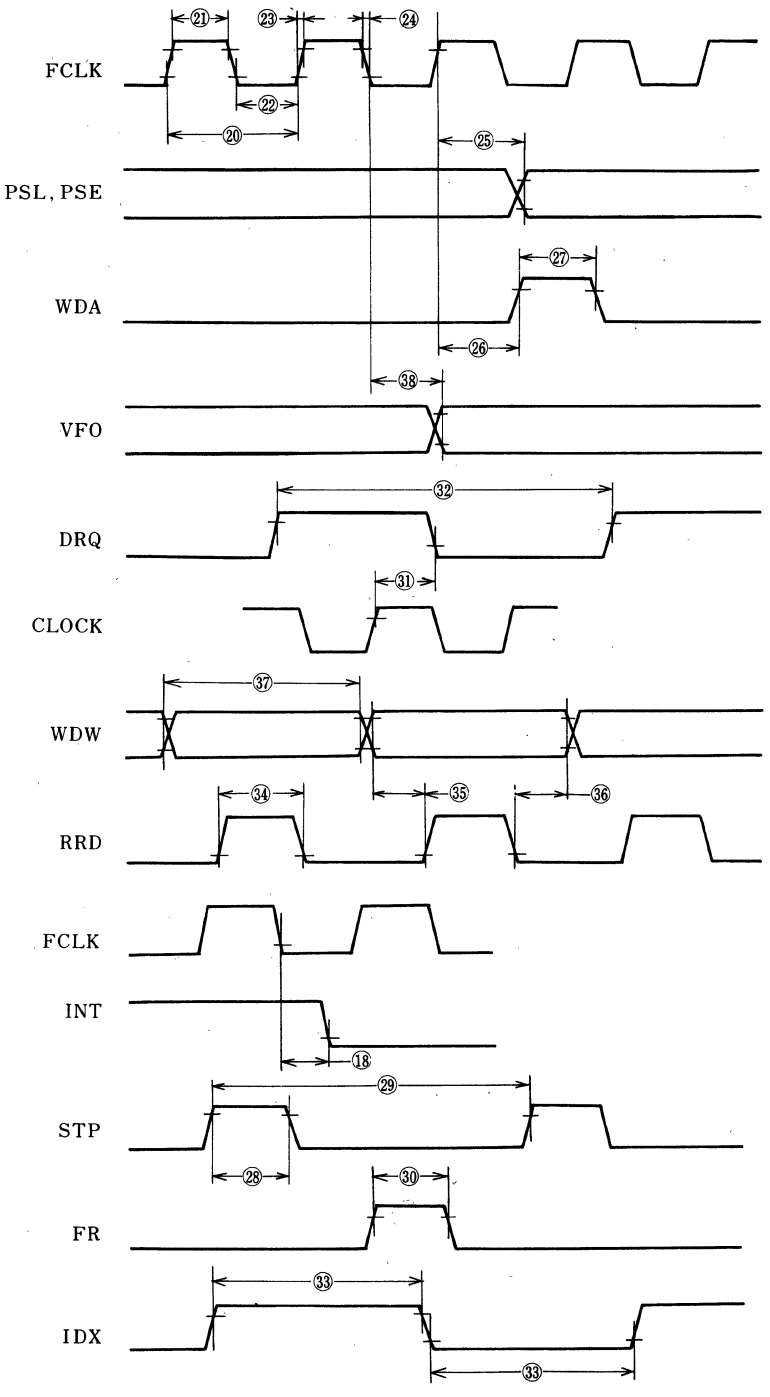
No.	Parameter	Symbol	LH0110/LH0110A			Unit
			MIN.	TYP.	MAX.	
20	FDC clock period, standard floppy disk	TcFC		500		ns
	FDC clock period, mini-floppy disk			1000		ns
21	FDC clock pulse width, high	TwFCh	220			ns
22	FDC clock pulse width, low	TwFCl	220			ns
23	FDC clock rise time	TfFC			30	ns
24	FDC clock fall time	TrFC			30	ns
25	Delay time from FDC clock ↑	TdPS(FC)			280	ns
26	Delay time from FDC clock ↑ (FDC clock ↓, in the case of MFM)	TdWDA(FC)			170	ns
27	Write data pulse width, MFM	TwWDA		250		ns
	Write data pulse width, FM			500		ns
28	Step pulse width	TwSTP		12		μs
29	Step period	TcSTP	1			ms
30	Fault reset pulse width	TwFR		12		μs
31	Delay time from clock ↑ to fulfill $\overline{\text{IORQ}}$ setup time	TdDRQ(FC)			230	ns
32	Data request period, MFM	TcDRQ		16		μs
	Data request period, FM			32		μs
33	Index pulse width	TwIDX	50			μs
34	Read data pulse width	TwRRD	100			ns
35	WDW setup time to read data	TsWDW(RRD)	100			ns
36	WDW hold time from read data	ThWDW(RRD)	100			ns
37	Window cycle time, MFM	TcWDW		1		μs
	Window cycle time, FM			2		μs
38	Delay time from FDC clock ↓ to VFO	TdVFO(FC)			150	ns

↑ indicates rising edge, ↓ indicates falling edge.

■ AC Timing Diagram

		"High"	"Low"
Timing test level :	CLOCK	$V_{CC}-0.6V$	0.45V
	OUTPUT	2.0V	0.8V
	INPUT	2.0V	0.8V
	FLOAT	ΔV	0.5V




FCLK
PSL, PSE
WDA
VFO
DRQ
CLOCK
WDW
RRD
FCLK
INT
STP
FR
IDX
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■ Internal Structure

The FDC consists of a CPU bus interface, internal control circuit (microprogram controlled), interrupt control circuit and floppy disk drive (FDD) control circuit. The interrupt control circuit arbitrates device priority and produces interrupt vectors.

The FDC has the registers:

- Two 8-bit data registers (RR0, WR0)
- Six 8-bit status registers (RR1, RR6)
- Seven 8-bit control registers (WR1-WR7)

■ FDC Registers

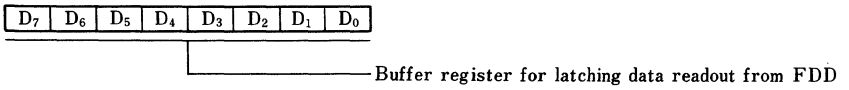
(1) FDC readout registers

Among the seven FDC readout registers RR0-RR6, RR3 and RR4 are cleared at the beginning of each command. The registers have the functions listed in Table 1.

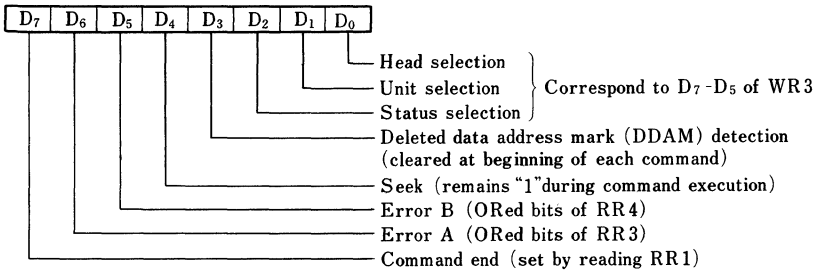
Table 1 FDC readout register functions

Register	Function
RR0	Data buffer
PR1	Control status
RR2	DMA control status; FDD control status
PR3	Error status, A
RR4	Error status, B
PR5	Physical track address
PR6	Sector address

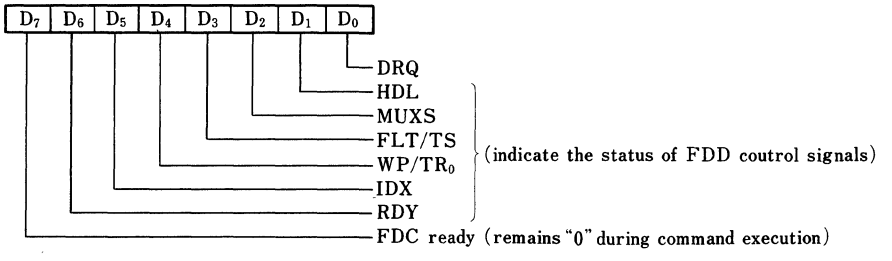
• Read Register 0 (RR0)



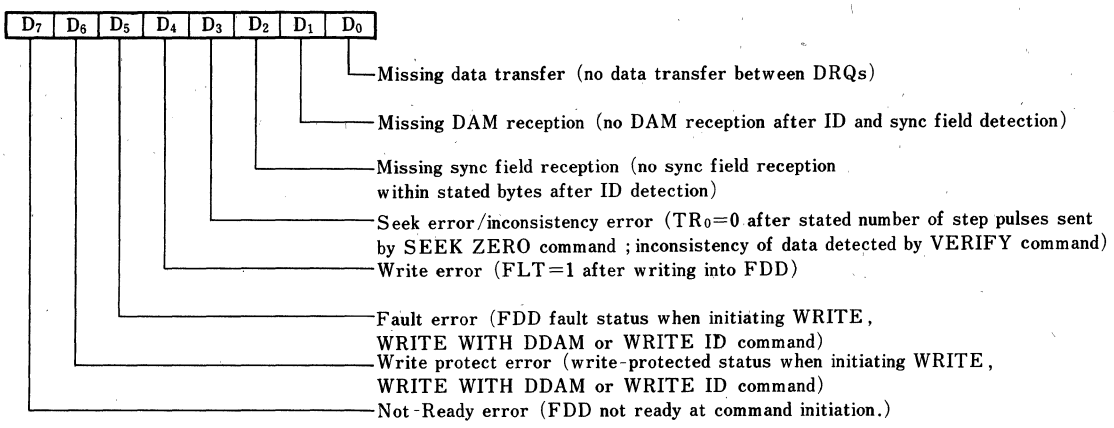
• Read Register 1 (RR1)



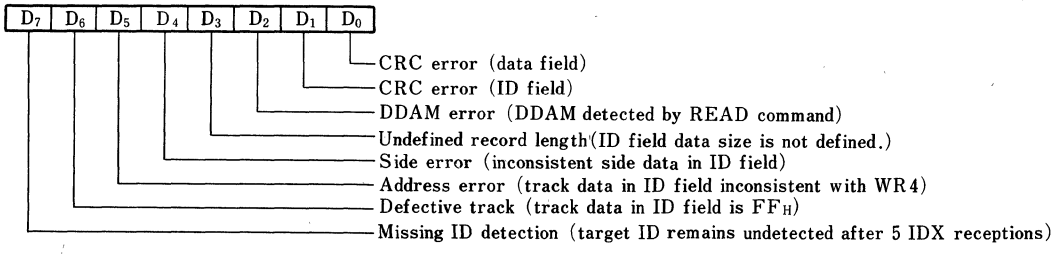
• Read Register 2 (RR2)



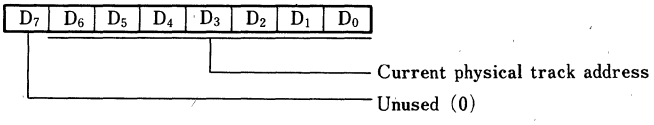
• Read Register 3 (RR3)



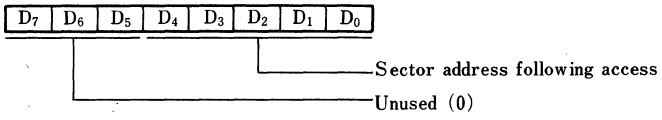
• Read Register 4 (RR4)



• Read Register 5 (RR5)



• Read Register 6 (RR6)



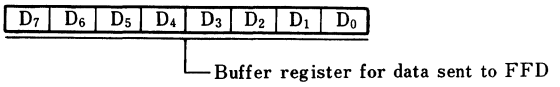
(2) FDC writing registers

Among the eight registers WR0-WR7 written in by CPU, WR1, WR3, WR5 and WR6 do not accept writing when FDC is busy. Tte registers have the functions listed in Table 2.

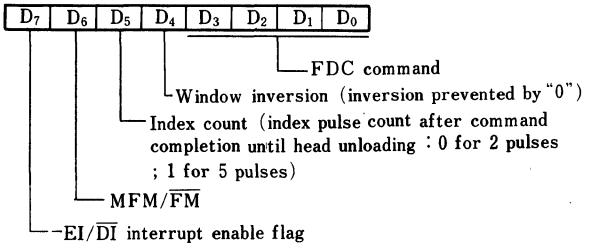
Table 2 FDC write register functions

Register	Function
WR0	Data buffer
WR1	Command designation
WR2	Time setting
WR3	Number-of-sectors designation and pin control
WR4	Logical track address
WR5	Physical track address
WR6	Sector address
WR7	Interrupt vector

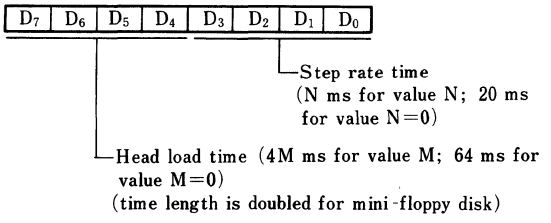
Write Register 0 (WR0)



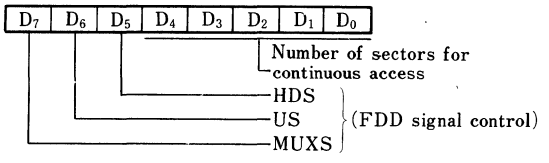
Write Register 1 (WR1)



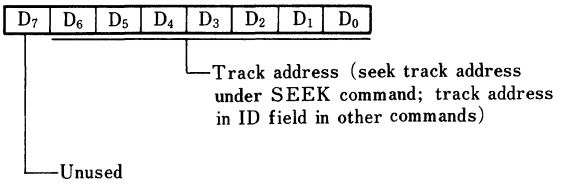
Write Register 2 (WR2)



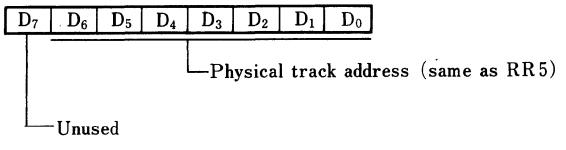
Write Register 3 (WR3)



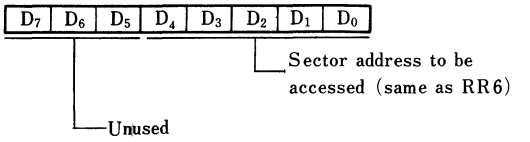
Write Register 4 (WR4)



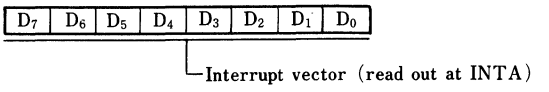
Write Register 5 (WR5)



Write Register 6 (WR6)



Write Register 7 (WR7)



■ Commands

(1) Brief description

① SEEK ZERO (0000/1)

Draw the head up to track 00. With command having LSB=0, task is excuted while retaining the head unload status ; with LSB=1, it is excuted while retaining the head load status.

② SEEK (0010/1)

Move the head to specified track. With LSB=0, task is executed while retaining the head unload status ; with LSB=1, it is executed while retaining head load status.

③ READ (0100)

Read data from specified sector and transfer each byte in data section to main system. When data address mark is DDAM, operation is terminated as DDAM error.

④ READ DDAM (0101)

Same as READ command, except that address DAM causes DDAM error, while DDAM does not cause error.

⑤ READ BOTH (0110)

Same as READ command, except that address mark DDAM does not cause error.

⑥ READ CRC (0111)

Same as READ BOTH, except that data is not transferred to main system.

⑦ VERIFY (1000)

Compare each byte in data section read out from a specified sector with the corresponding byte of data received from main system.

⑧ READ ID (1001)

Read out data in ID section of specified track and transfer each byte to main system.

⑨ WRITE (1010)

Write each byte of data received from main system into specified sector.

⑩ WRITE WITH DDAM (1011)

Same as WRITE command, except that DDAM and not DAM is written as address mark.

⑪ WRITE ID1 (1100)

⑫ WRITE ID2 (1101)

⑬ WRITE ID3 (1110)

Write initialization (ID section) and gaps of specified track. In this command, data section is filled with gaps.

WRITE ID1 26 sectors/track (FM: 128 bytes/sector; MFM: 256 bytes/sector)

WRITE ID2 15 sectors/track (FM: 256 bytes/sector; MFM: 512 bytes/sector)

WRITE ID3 8 sectors/track (FM: 512 bytes/sector; MFM: 1024 bytes/sector)

⑭ RESET STATUS (1111)

Initialize floppy disk drives.

(2) Commands and error status register A

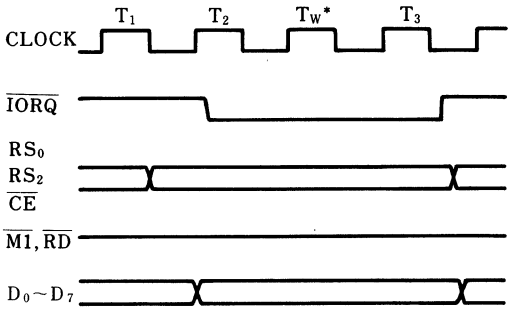
Error status \ Command		SEEK ZERO	SEEK	READ	READ DDAM	READ BOTH	READ CRC	VERIFY	READ ID	WRITE	WRITE WITH DDAM	WRITE ID 1,2,3	RESET STATUS
DB7	Not-ready-error	×	○	○	○	○	○	○	○	○	○	○	×
DB6	Write protect error	×	×	×	×	×	×	×	×	○	○	○	×
DB5	Fault error	×	×	×	×	×	×	×	×	○	○	○	×
DB4	Write error	×	×	×	×	×	×	×	×	○	○	○	×
DB3	Seek error	○	×	×	×	×	×	×	×	×	×	×	×
	Inconsistency error	×	×	×	×	×	×	○	×	×	×	×	×
DB2	Missing sync field reception	×	×	○	○	○	○	○	×	×	×	×	×
DB1	Missing DAM reception	×	×	○	○	○	○	○	×	×	×	×	×
DB0	Missing data transfer	×	×	○	○	○	×	○	○	○	○	○	×

(3) Commands and error status register B

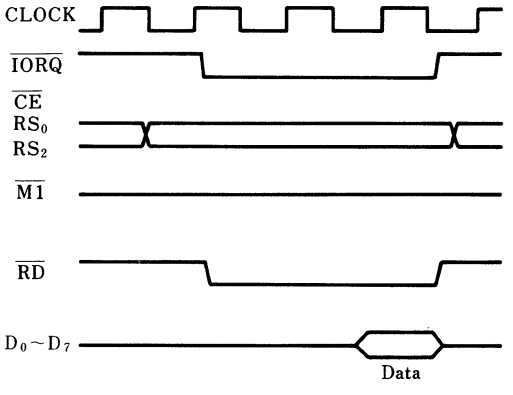
Error status \ Command		SEEK ZERO	SEEK	READ	READ DDAM	READ BOTH	READ CRC	VERIFY	READ ID	WRITE	WRITE WITH DDAM	WRITE ID 1,2,3	RESET STATUS
DB7	Missing ID detection	×	×	○	○	○	○	○	○	○	○	×	×
DB6	Defect track	×	×	○	○	○	○	○	×	○	○	×	×
DB5	Address error	×	×	○	○	○	○	○	×	○	○	×	×
DB4	Side error	×	×	○	○	○	○	○	×	○	○	×	×
DB3	Undefined record length	×	×	○	○	○	○	○	×	○	○	×	×
DB2	DDAM error	×	×	○	○	×	×	×	×	×	×	×	×
DB1	CRC error (ID field)	×	×	○	○	○	○	○	○	○	○	×	×
DB0	CRC error (data field)	×	×	○	○	○	○	○	×	×	×	×	×

■ CPU Interface Timing

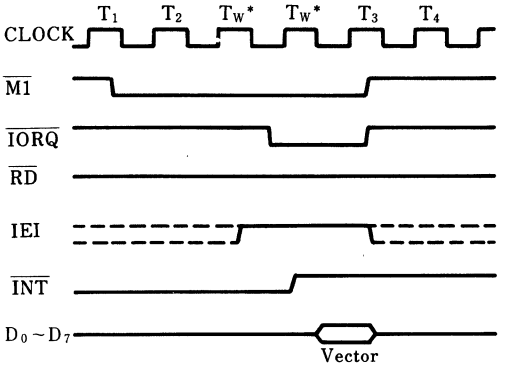
(1) FDC write cycle



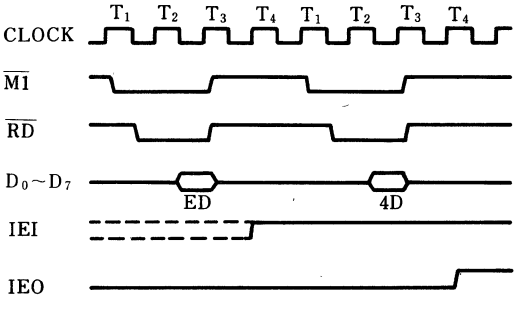
(2) FDC read cycle



(3) Interrupt acknowledge cycle

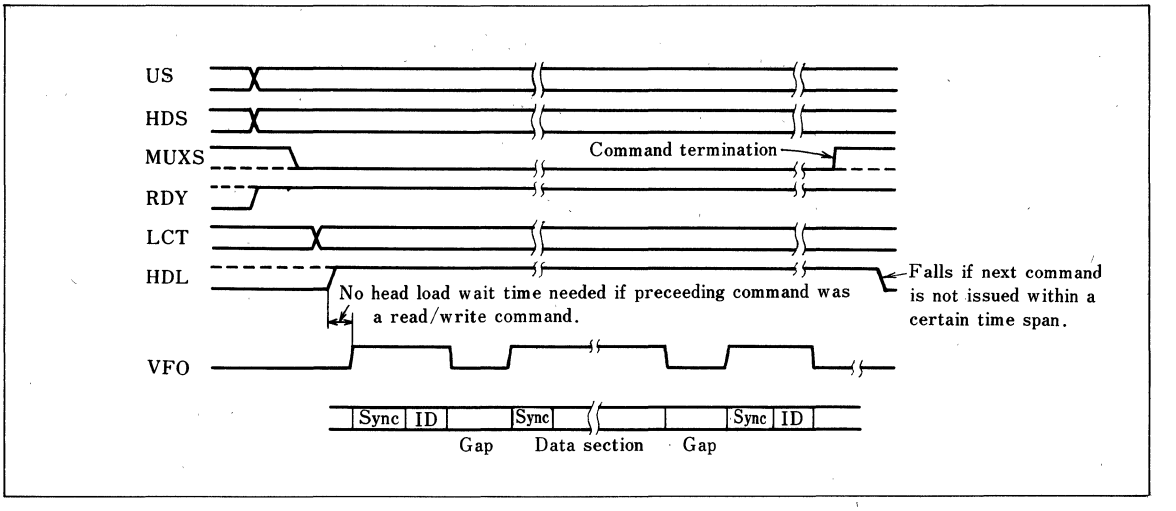


(4) Interrupt return cycle

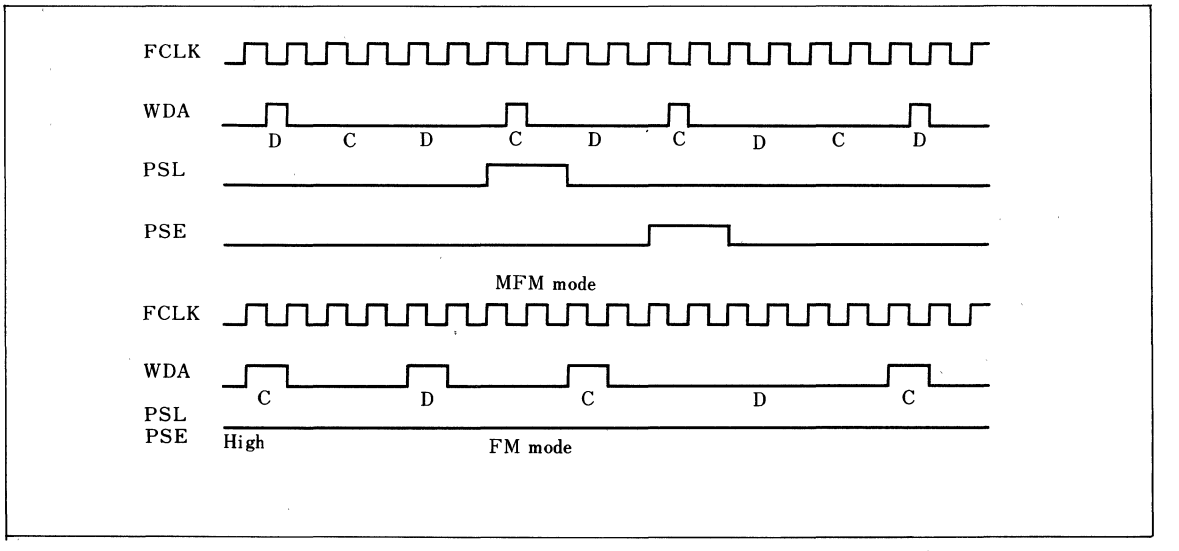


■ FDD Interface Timing

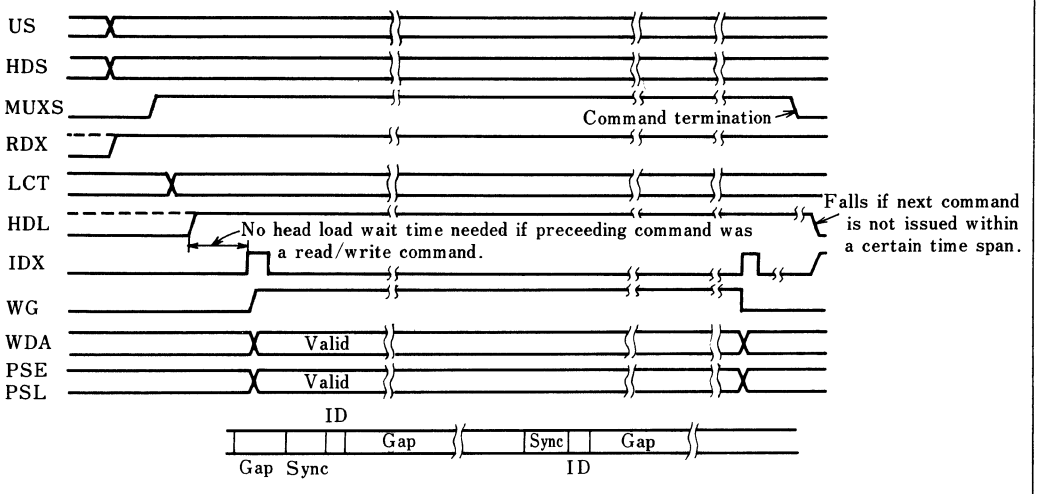
(1) READ, READ DDAM, READ BOTH, READ CYC, VERIFY, READ ID command timing



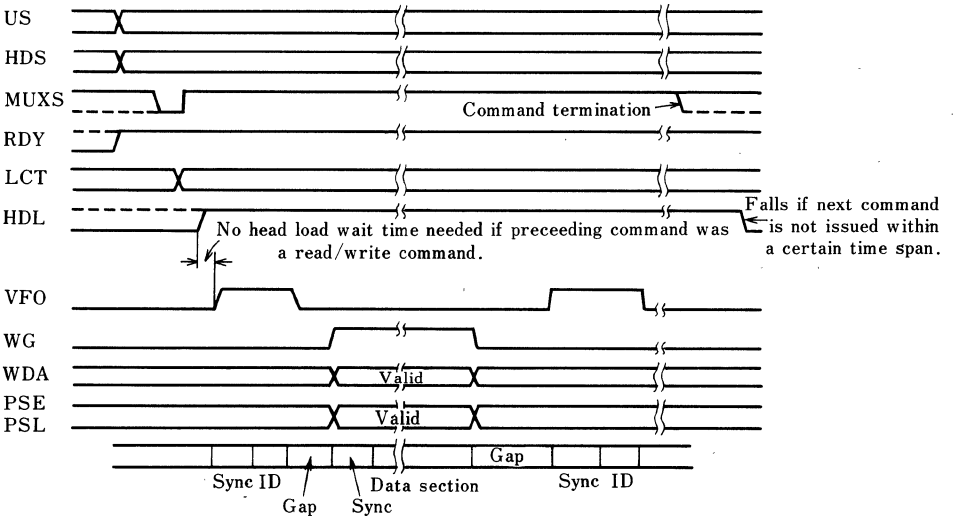
(2) PSL and PSE timing



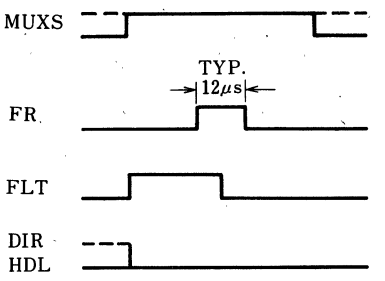
(3) WRITE ID1, WRITE ID2, WRITE ID3 command timing



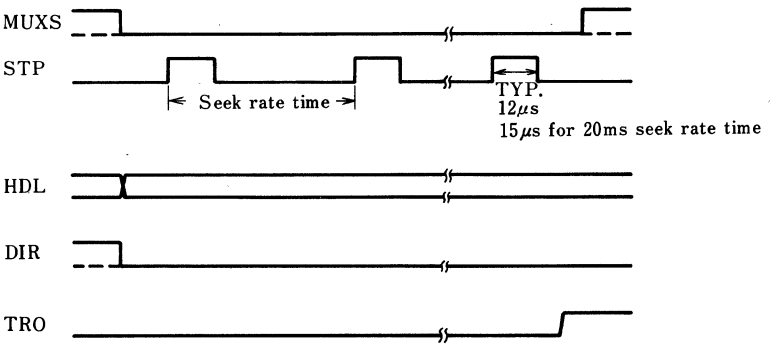
(4) WRITE, WRITE WITH DDAM command timing



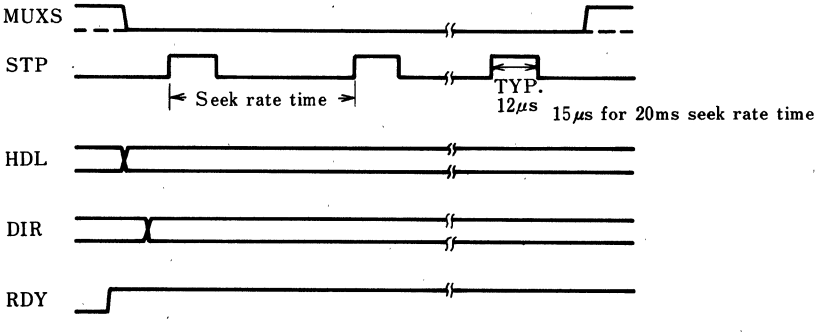
(5) RESET STATUS command timing



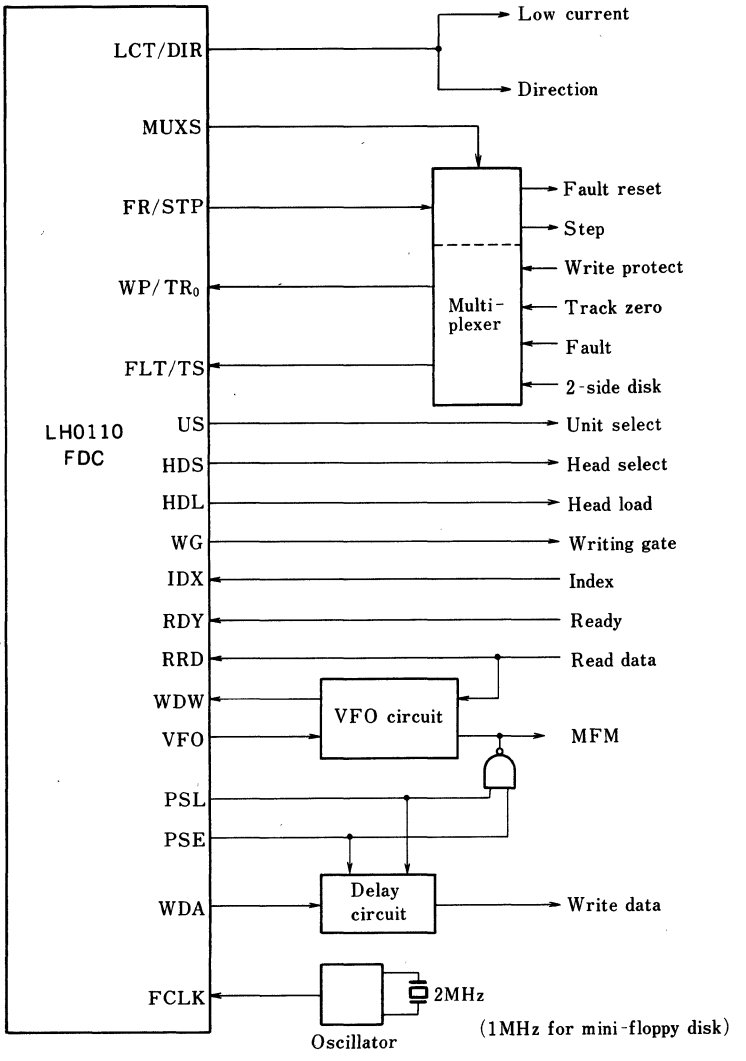
(6) SEEK ZERO command timing



(7) SEEK command timing



■ System Configuration



LH5080/LH5080L/LH5080LM

Z80 CMOS Central Processing Unit

■ Description

The LH5080 is Z80 CPU fabricated with CMOS silicon-gate process technology and is fully compatible with the conventional NMOS Z80 CPU (LH0080).

The LH5080 is designed with CMOS fully static circuits and so provides low power consumption and wide range power supply voltage operation.

The LH5080L/LH5080LM provides power save mode controlled by software.

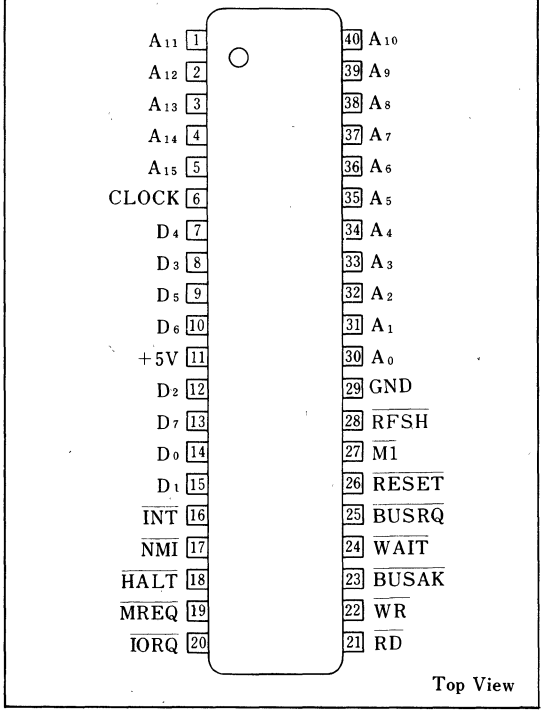
■ Features

1. Z80 CMOS CPU
2. Fully compatible with the NMOS Z80 CPU (LH0080)
3. 158 instructions
4. 22 registers
5. 3 modes of maskable interrupt and a nonmaskable interrupt
6. Instruction fetch cycle 1.6 μs
7. Single +5V power supply and single phase clock
8. All inputs and outputs except clock input fully TTL compatible
9. Fully static operation (DC~2.5MHz)
10. Low power consumption
11. Power save mode (LH5080L/LH5080LM)
12. 40-pin dual-in-line package (LH5080/LH5080L)
13. 44-pin quad-flat package (LH5080LM)

Note: The Z80 CMOS CPU (LH5080/LH5080L/LH5080LM) is compatible with the Z80 NMOS CPU (LH0080). So there is no description here about the pins, CPU registers, architecture, interrupts, basic timings, and instruction sets. Refer back to the Z80 NMOS CPU described earlier.

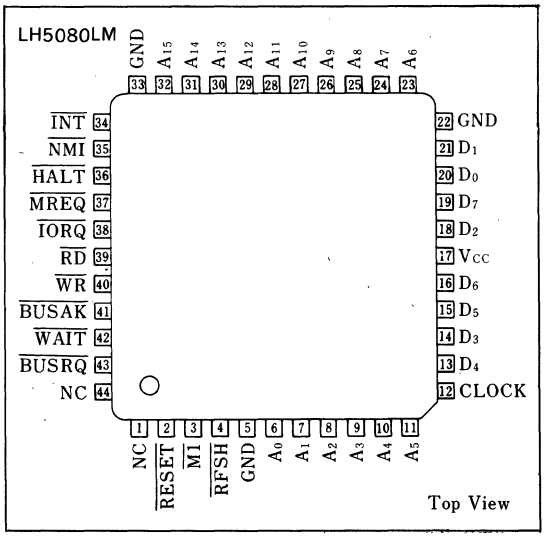
■ Pin Connections

LH5080/LH5080L



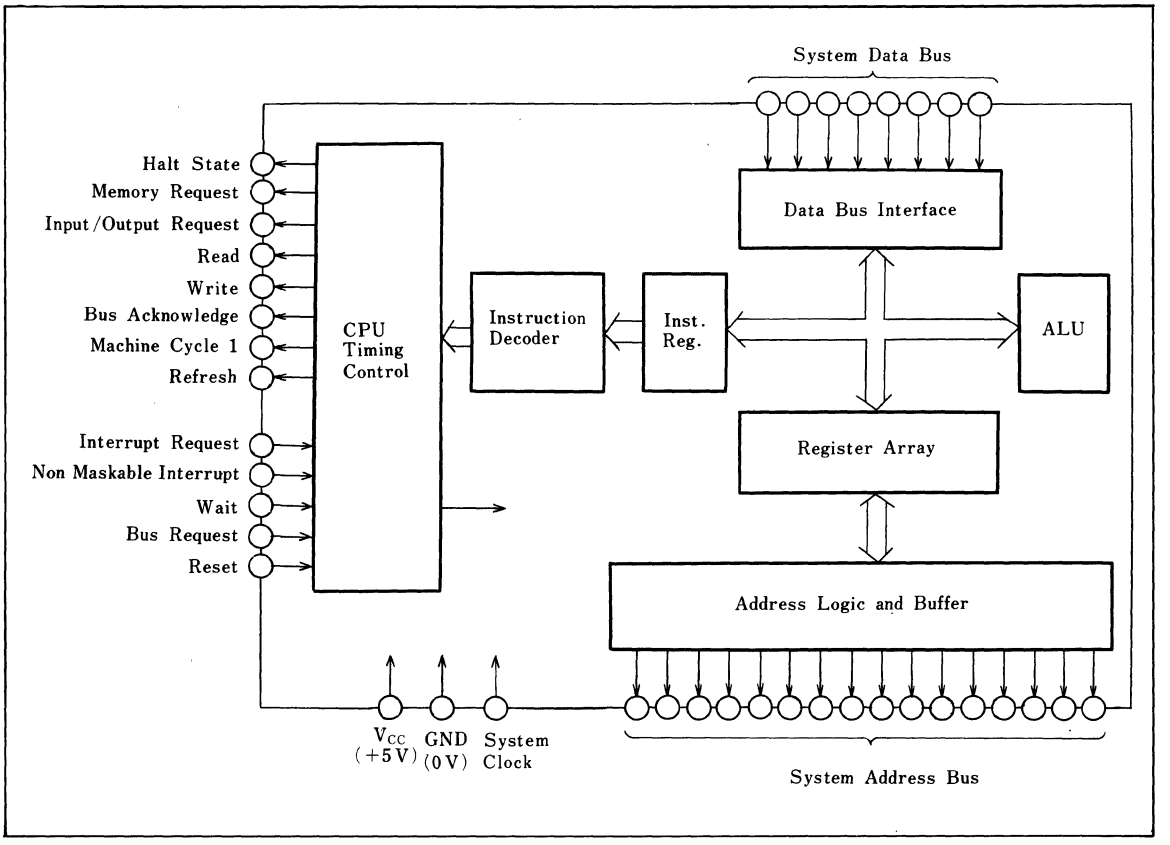
Top View

LH5080LM



Top View

Block Diagram



■ Absolute Maximum Ratings

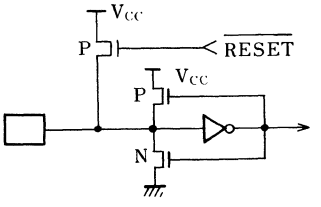
Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7	V
Output voltage	V_{OUT}	−0.3～+7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

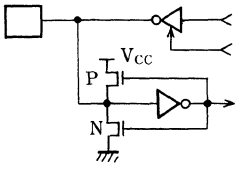
■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

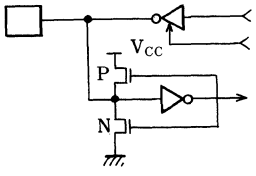
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock input low voltage	V_{ILC}		−0.3		0.45	V	
Clock input high voltage	V_{IHC}		V_{CC}−0.6		V_{CC}+0.3	V	
Input low voltage	V_{IL}		−0.3		0.8	V	
Input high voltage	V_{IH}		2.4		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=1.8mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4			V	
Current consumption	I_{CC}	(Note)		10		mA	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V, V_{CC}			10	μA	1
3-state output leakage current	$\lvert I_{LOH} \rvert$	V_{OUT}=V_{CC}			10	μA	2
3-state output leakage current	$\lvert I_{LOL} \rvert$	V_{OUT}=0V			10	μA	2
Data bus leakage current	$\lvert I_{LD} \rvert$	0≦V_{IN}≦V_{CC}			10	μA	
Current consumption in PS mode (LH5080L/LH5080LM)	I_{CCPS}	V_{IH}=0V, V_{CC} Output pin open		50	150	μA	

Note: TcC=400ns, V_{IL}=0.4V, V_{IH}=V_{CC}−0.4V, output pin open.
Note 1 : The INT , WAIT, NMI and (BUSRQ) pins are arranged as shown below. Note 2: The A_0-A_3 pins are arranged as shown below.





Note 1 and 2 : The D_0～D_7 pins are arranged as shown below.



■ Capacitance

(f=1MHz, Ta=25℃)

Symbol	Parameter	MAX.	Unit	
C_{CLOCK}	Clock capacitance	5	pF	Unmeasured pins returned to ground
C_{IN}	Input capacitance	6	pF	
C_{OUT}	Output capacitance	10	pF	

■ AC Characteristics

(V_{CC}=5V±10%, Ta=0~+70℃)

No.	Parameter	Symbol	MIN.	MAX.	Unit
1	Clock cycle time	TcC	400*		ns
2	Clock pulse width (high)	TwCh	180*		ns
3	Clock pulse width (low)	TwCl	180		ns
4	Clock fall time	TfC		30	ns
5	Clock rise time	TrC		30	ns
6	Clock ↑ to address valid delay	TdCr (A)		145	ns
7	Address valid to $\overline{MREQ}$ ↓ delay	TdA (MREQf)	125*		ns
8	Clock ↓ to $\overline{MREQ}$ ↓ delay	TdCf (MREQf)		100	ns
9	Clock ↑ to $\overline{MREQ}$ ↑ delay	TdCr (MREQr)		100	ns
10	$\overline{MREQ}$ pulse width (high)	TwMREQh	170*		ns
11	$\overline{MREQ}$ pulse width (low)	TwMREQl	360*		ns
12	Clock ↓ to $\overline{MREQ}$ ↑ delay	TdCf (MREQr)		100	ns
13	Clock ↓ to $\overline{RD}$ ↓ delay	TdCf (RDf)		130	ns
14	Clock ↑ to $\overline{RD}$ ↑ delay	TdCr (RDr)		100	ns
15	Data setup time to clock ↑	TsD (Cr)	50		ns
16	Data hold time after $\overline{RD}$ ↑	ThD (RDr)	15		ns
17	$\overline{WAIT}$ setup time to clock ↓	TsWAIT (Cf)	70		ns
18	$\overline{WAIT}$ hold time after clock ↓	ThWAIT (Cf)	15		ns
19	Clock ↑ to $\overline{M1}$ ↓ delay	TdCr (M1f)		130	ns
20	Clock ↑ to $\overline{M1}$ ↑ delay	TdCr (M1r)		130	np
21	Clock ↑ to $\overline{RFSH}$ ↓ delay	TdCr (RFSHf)		180	ns
22	Clock ↑ to $\overline{RFSH}$ ↑ delay	TdCr (RFSHr)		150	ns
23	Clock ↓ to $\overline{RD}$ ↑ delay	TdCf (RDr)		110	ns
24	Clock ↑ to $\overline{RD}$ ↓ delay	TdCr (RDf)		100	ns
25	Data setup to clock ↑ during M_2, M_3, M_4 or M_5 cycles	TsD (Cf)	60		ns
26	Address stable prior to $\overline{IORQ}$ ↓	TdA (IORQf)	320*		ns
27	Clock ↑ to $\overline{IORQ}$ ↓ delay	TdCr (IORQf)		90	ns
28	Clock ↓ to $\overline{IORQ}$ ↑ delay	TdCf (IORQr)		110	ns
29	Data stable prior to $\overline{WR}$ ↓ (memory cycle)	TdDm (WRf)	190*		ns
30	Clock ↓ to $\overline{WR}$ ↓ delay	TdCf (WRf)		90	ns
31	$\overline{WR}$ pulse width	TwWR	360*		ns
32	Clock ↓ to $\overline{WR}$ ↑ delay	TdCf (WRr)		100	ns
33	Data stable prior to $\overline{WR}$ ↓ (I/O cycle)	TdDi (WRf)	20*		ns
34	Clock ↑ to $\overline{WR}$ ↓ delay	TdCr (WRf)		80	ns
35	Data stable from $\overline{WR}$ ↑	TdWRr (D)	120*		ns
36	Clock ↓ to $\overline{HALT}$ ↑	TdCf (HALT)		300	ns
37	$\overline{NM1}$ pulse width	TwNMI	80		ns
38	$\overline{BUSREQ}$ setup time to clock ↑	TsBUSRQ (Cr)	80		ns
39	$\overline{BUSREQ}$ hold time after clock ↑	ThBUSRQ (Cr)	15		ns
40	Clock ↑ to $\overline{BUSACK}$ ↓ delay	TdCr (BUSAKf)		120	ns
41	Clock ↓ to $\overline{BUSACK}$ ↑ delay	TdCf (BUSAKr)		110	ns
42	Clock ↑ data float delay	TdCr (Dz)		90	ns
43	Clock ↑ to control output float delay ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$)	TdCr (CTz)		110	ns

↑ Rising edge, ↓ Falling edge.

No.	Parameter	Symbol	MIN.	MAX.	Unit
44	Clock ↑ to address float delay	TdCr (Az)		110	ns
45	$\overline{MREQ}$ ↑, $\overline{IORQ}$ ↑, $\overline{RD}$ ↑, and $\overline{WR}$ ↑ to address hold time	TdCTr (A)	160*		ns
46	$\overline{RESET}$ to clock ↑ setup time	TsRESET (Cr)	90		ns
47	Clock ↑ to $\overline{RESET}$ hold time	ThRESET (Cr)	15		ns
48	$\overline{INT}$ to clock ↑ setup time	TsINTf (Cr)	80		ns
49	Clock ↑ to $\overline{INT}$ hold time	ThINTr (Cr)	15		ns
50	$\overline{M1}$ ↓ to $\overline{IORQ}$ ↓ delay	TdMIf (IORQf)	920*		ns
51	Clock ↓ to $\overline{IORQ}$ ↓ delay	TdCf (IORQf)		110	ns
52	Clock ↑ to $\overline{IORQ}$ ↑ delay	TdCf (IORQr)		100	ns
53	Clock ↓ to data valid delay	TdCf (D)		230	ns

↑ Rising edge, ↓ Falling edge

* For clock periods other than the minimums shown in the table, calculate parameters using the expressions in the table on the following page.

* All timings are preliminary and subject to change.

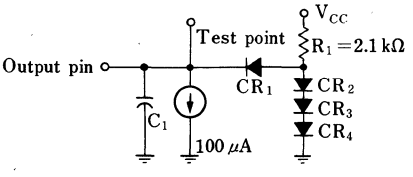
Footnotes to AC Characteristics

No.	Symbol	Formula
1	TcC	TwCh+TwCl+TrC+TfC
2	TwCh	MAX. 200 μs
7	TdA (MREQf)	TwCh+TfC−75
10	TwMREQh	TwCh+TfC−30
11	TwMREQ1	TcC−40
26	TdA (IORQf)	TcC−80
29	TdD (WRf)	TcC−210
31	TwWR	TcC−40
33	TdD (WRf)	TwCl+TrC−180
35	TdWRr (D)	TwCl+TrC−80
45	TdCTr (A)	TwCl+TrC−40
50	TdM1f (IORQf)	2TcC+TwCh+TfC−80

AC Test Conditions

- Input voltage amplitude : 0.4V to 2.8V
- Input signal rise and fall time : 10 ns
- Clock input voltage amplitude : 0.4V to V_{CC}−0.6V
- Input judge level : 0.8V and 2.0V
- Output judge level : 0.8V and 2.0V
- Output load : ITTL+100 pF

Output Pins Measuring Circuit



CR_1~CR_4: IN914 or eguivalent
C_1: 50pF for all pins

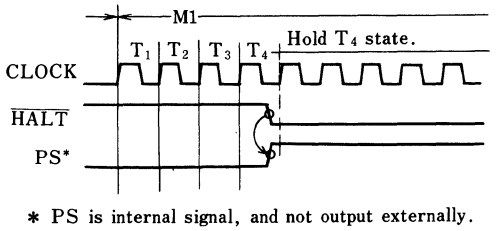
■ Power Save Function

The LH5080L/LH5080LM features the power save (PS) function. After a HALT instruction has been executed, the internal clock signal is automatically cut off to bring the CPU into the halt mode.

(1) PS mode setting

With a HALT instruction executed, the PS mode will be automatically established. In this mode, the internal clock signal is cut off to save the power consumed for the clock signal operation. Cutting an external clock signal does not give any problem inside, therefore, in this mode. To cut off the external clock, it is possible to utilize the rise timing of a $\overline{\text{HALT}}$ signal output. It should be noted, however, that this timing cannot be used to restart the external clock.

In the PS mode, the bus request ($\overline{\text{BUSRQ}}$) is not accepted and the memory refresh is not done, either.



* PS is internal signal, and not output externally.

PS mode setting

(2) PS mode clear

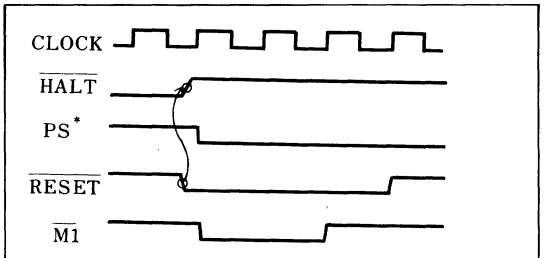
The PS mode is cleared by any of the following; reset (RESET), non-maskable interrupt ($\overline{\text{NMI}}$) and maskable interrupt ($\overline{\text{INT}}$).

When the external clock is shut down in the PS mode, a stable clock signal must be input before clearing the PS mode.

(i) Clearing with RESET: Input the $\overline{\text{RESET}}$ signal for more than 3 clock cycles. The PS mode is then cleared and the reset just as before is carried out.

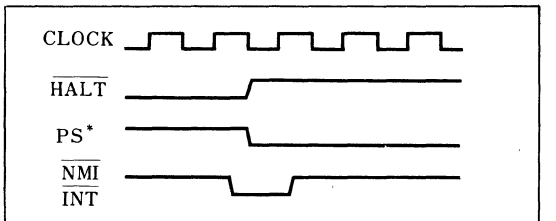
(ii) Clearing with $\overline{\text{NMI}}$: Input the $\overline{\text{NMI}}$ signal (edge trigger) to clear the PS mode and to carry out the instruction next to the HALT. Now the non-maskable interrupt processing routine will be introduced.

(iii) Clearing with $\overline{\text{INT}}$: Input the $\overline{\text{INT}}$ signal (level trigger) regardless of which state the interrupt enable flag is in. The PS mode is now cleared and the HALT instruction executed. If the interrupt enable flag is set up and the $\overline{\text{INT}}$ signal is "Low" at the clock pulse rise timing in the last clock cycle of the HALT instruction, the maskable interrupt processing routine will be introduced as the next machine cycle.



* PS is internal signal, and not output externally.

Halt clear by $\overline{\text{NMI}}$ $\overline{\text{INT}}$



* PS is internal signal, and not output externally.

PS mode clear by $\overline{\text{MI}}$ signal

LH5081/LH5081L/LH5081LM

Z80 CMOS Parallel I/O Controller

■ Description

The LH5081 is Z80 PIO fabricated with CMOS silicon gate process technology and is fully compatible with the conventional NMOS Z80 PIO (LH0081).

The LH5081 is designed with CMOS fully static circuits and so provides low power consumption and wide range power supply voltage operation.

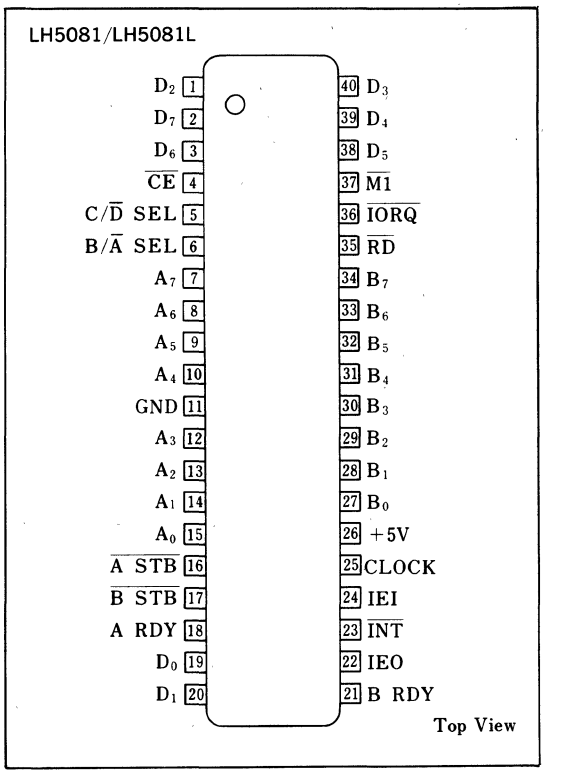
The LH5081L/LH5081LM provides power save mode controlled by softwave.

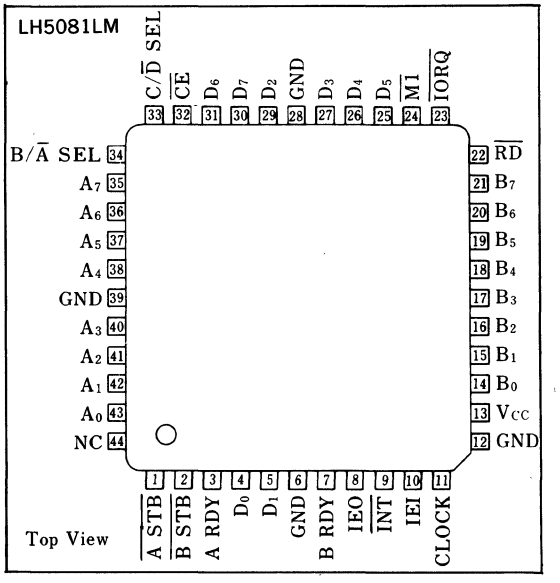
■ Features

1. Z80 CMOS PIO
2. Fully compatible with NMOS Z80 PIO (LH0081)
3. Tow independent 8-bit bidirectional peripheral interface ports with handshake data transfer control
4. 4 programmable operating modes
   - Byte input mode
   - Byte output mode
   - Byte bidirectional bus mode (Port A only)
   - Byte control mode
5. Programmable interrupt on peripheral status conditions
6. Vectored daisy chain priority interrupt
7. Darlington transistor drive capability (Port B output)
8. All inputs and outputs except clock input fully TTL compatible
9. Single +5V power supply and single phase clock
10. Fully static operation (DC~2.5MHz)
11. Low power consumption
12. Power save mode (LH5081L/LH5081LM)
13. Status read mode (LH5081L/LH5081LM)
14. 40-pin dual-in-line package (LH5081/LH5081L)
15. 44-pin quad-flat package (LH5081LM)

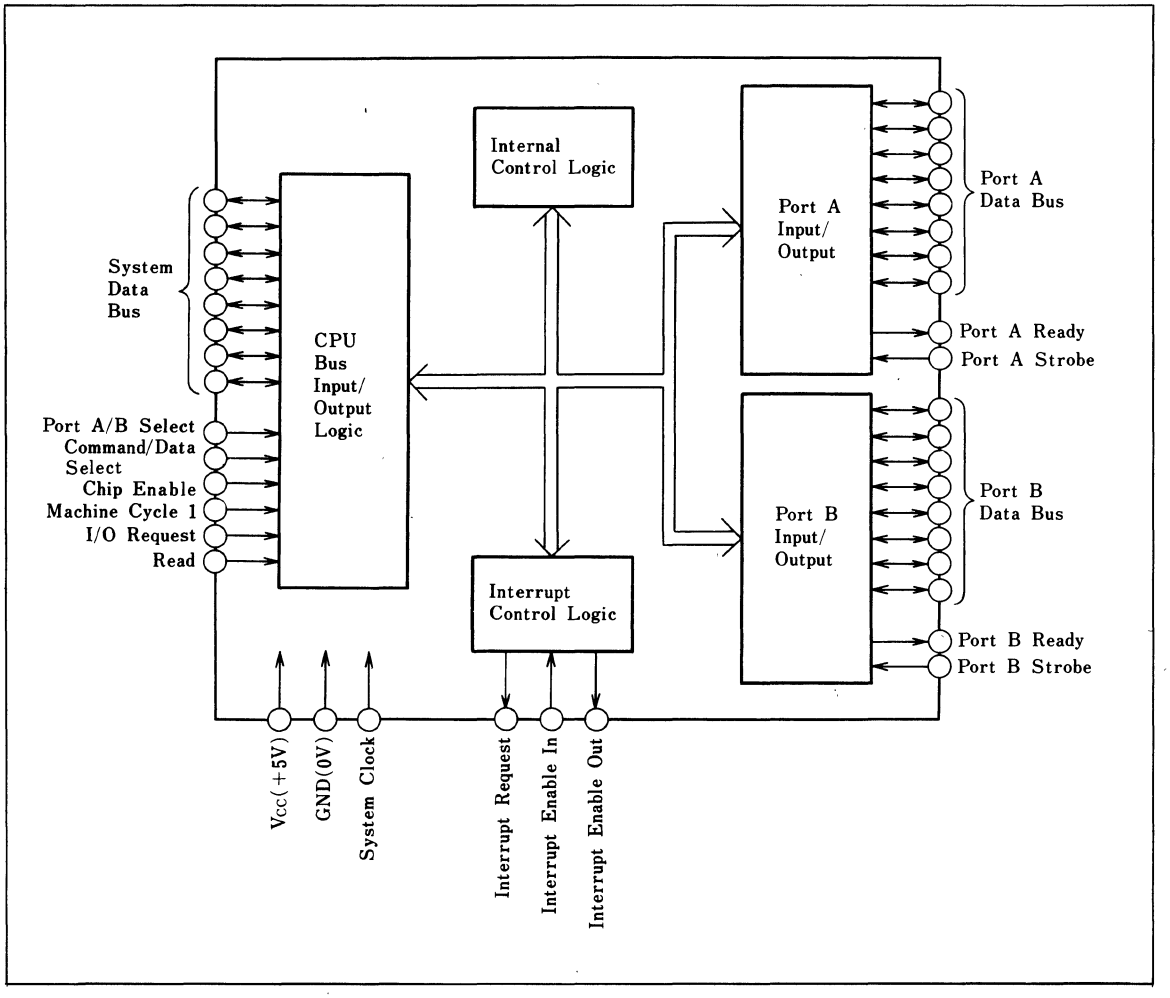
Note: The Z80 CMOS CPU (LH5081/LH5081L) is compatible with the Z80 NMOS PIO (LH0081). So there is no description here about the pins, programming, and basic timings waveforms. Refer back to the Z80 NMOS PIO described earlier.

■ Pin Connections





■ Block Diagram



■ Absolute Maximum Ratings

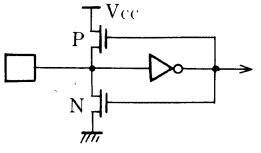
Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	−0.3～7.0	V
Input voltage	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage	V_{OUT}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

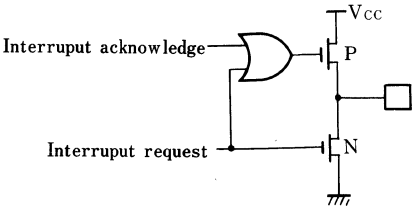
■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

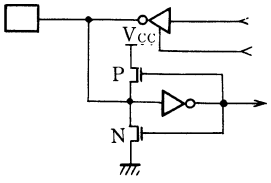
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock input low voltage	V_{ILC}		−0.3		0.45	V	
Clock input high voltage	V_{IHC}		V_{CC}−0.6		V_{CC}+0.3	V	
Input low voltage	V_{IL}		−0.6		0.8	V	
Input high voltage	V_{IH}		2.2		V_{CC}+0.3	V	
Output low voltage	V_{OL}	I_{OL}=2mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=−1.6mA	2.4			V	
		I_{OH}=−250 μA	V_{CC}−0.4V			V	
Current consumption	I_{CC}	(Note)		2	6	mA	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V, V_{CC}			10	μA	1
3-state output leakage current	$\lvert I_{LOH} \rvert$	V_{OUT}=V_{CC}			10	μA	2
3-state output leakage current	$\lvert I_{LOL} \rvert$	V_{OUT}=0V			10	μA	2
Data bus leakage current input	$\lvert I_{LD} \rvert$	0≦V_{IN}≦V_{CC}			10	μA	
Darlington drive current	I_{OHD}	V_{OH}=1.5V, Port only	−1.5			mA	
Current consumption in PS mode (LH5081L/LH5081LM)	I_{CCPS}	Output pin open, V_{IN}=0V, V_{CC}		1	100	μA	

Note TcC=400ns, V_{IL}=0.4V, V_{IH}=V_{CC}−0.4V, output pin open.
Note 1 : The A STB and B STG pins are arranged as shown below. ● The $\overline{INT}$ pin is arraged as shown below.





Note 2: The A_0-A_7 and B_0-B_7 pins are arranged as shown below.



■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground	7	pF
Input capacitance	C_{IN}		7	pF
Output capacitance	C_{OUT}		10	pF

■ AC Characteristics

(V_{CC}=5V±10%, Ta=0~+70℃)

No.	Parameter	Symbol	MIN.	MAX.	Unit	Note
1	Clock cycle time	TcC	400	(Note 1)	ns	
2	Clock width (high)	TwCh	170		ns	
3	Clock width (low)	TwCl	170		ns	
4	Clock fall time	TfC		30	ns	
5	Clock rise time	TrC		30	ns	
6	$\overline{CE}$, B/$\overline{A}$, C/$\overline{D}$ to $\overline{RD}$, $\overline{IORQ}$ ↓ setup time	TsCS (RI)	50		ns	6
7	Any hold times for specified setup time	Th	15		ns	
8	$\overline{RD}$, $\overline{IORQ}$ to clock ↑ setup time	TsRI (C)	115		ns	
9	$\overline{RD}$, $\overline{IORQ}$ ↓ to data output delay	TdRI (DO)		430	ns	2
10	$\overline{RD}$, $\overline{IORQ}$ ↑ to data output float delay	TdRI (DOs)		160	ns	
11	Data in to clock ↑ setup time	TsDI (C)	50		ns	C_L=50pF
12	$\overline{IORQ}$ ↓ to data out delay (INTACK cycle)	TdIO (DOI)	340		ns	3
13	$\overline{M1}$ ↓ to clock ↑ setup time	TsM1 (Cr)	210		ns	
14	$\overline{M1}$ ↑ to clock ↓ setup time ($\overline{M1}$ cycle)	TsM1 (Cf)	0		ns	8
15	$\overline{M1}$ ↓ to IEO ↓ delay (interrupt immediately preceding $\overline{MI}$ ↓)	TdM1 (IEO)		300	ns	5, 7
16	IEI to $\overline{IORQ}$ ↓ setup time (INTACK cycle)	TsIEI (IO)	140		ns	7
17	IEI ↓ to IEO ↓ delay	TdIEI (IEOf)		190	ns	5 C_L=50pF
18	IEI ↑ to IEO ↑ delay (after ED decode)	TdIEI (IEOr)		210	ns	5
19	$\overline{IORQ}$ ↑ to clock ↓ setup time (to activate READY on next clock cycle)	TcIO (C)	220		ns	
20	Clock ↓ to READY ↑ delay	TdC (RDYr)	200		ns	5 C_L=50pF
21	Clock ↓ to READY ↓ delay	TdC (RDYf)	150		ns	5
22	$\overline{STROBE}$ pulse width	TwSTB	150		ns	4
23	$\overline{STROBE}$ ↑ to clock ↓ setup time (to activate READY on next clock cycle)	TsSTB (C)	220		ns	5
24	$\overline{IORQ}$ ↑ to PORT DATA stable delay (mode 0)	TdIO (PD)		200	ns	5
25	PORT DATA to $\overline{STROBE}$ ↑ setup time (mode 1)	TsPD (STB)	260		ns	
26	$\overline{STROBE}$ ↓ to PORT DATA stable (mode 2)	TdSTB (PD)		230	ns	5
27	$\overline{STROBE}$ ↑ to PORT DATA float delay (mode 2)	TdSTB (PDr)		200	ns	C_L=50pF
28	PORT DATA match to $\overline{INT}$ ↓ delay (mode 3)	TdPD (INT)		540	ns	
29	$\overline{STROBE}$ ↑ to $\overline{INT}$ ↓ delay	TdSTB (INT)		490	ns	

↑ Rising edge, ↓ Falling edge

Note 1 : TcC=TwCh+TwCl+TrC+TlC.
Note 2 : Increase TdRI (DO) by 10 ns for each 50 pF increase in load up to 200 pF max.
Note 3 : Increase TdIO (DOI) by 10 ns for each 50 pF, increase in loading up to 200 pF max.
Note 4 : For Mode 2 : TwSTB>TsPD (STB).
Note 5 : Increase these values by 2 ns for each 10 pF increase in loading up to 100 pF max.
Note 6 : TsCS (RI) may be reduced. However, the time substracted from TsCS (RI) will be added to TdRI (DO).
Note 7 : 2.5 TcC > (N-2) TdIEI (IEOf)+TdM1 (IEO)+TsIEI (IO)+TTL Buffer Delay, if any.
Note 8 : $\overline{M1}$ must be active for a minimum of two clock cycles to reset the PIO.

AC Test Conditions :

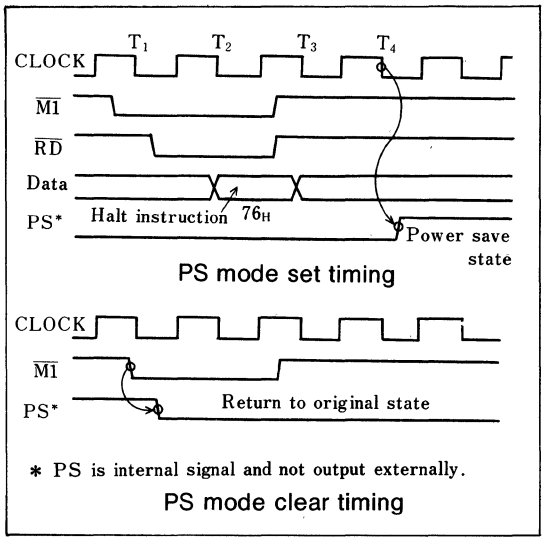
- Input voltage amplitude : 0.4V to 2.8V
- Clock input voltage amplitude : 0.4V to V_{CC}−0.6V
- Input signal rise and fall time : 10ns
- Input judge level : 0.8V and 2.0V
- Output judge level : 0.8V and 2.0V
- Output load : ITTL+100pF (unless otherwise specified)

■ Power Save and Status Information Read Function

Unlike the LH0081/LH5081, the LH5081L/LH5081LM has the power save (PS) and status information read functions.

(1) Power save function

(i) **PS mode setting** When the CPU (LH5080L/LH5080LM) has executed an HALT instruction in the PS mode, the LH5081L/LH5081LM reads this HALT instruction to automatically go into the PS mode. Now the internal clock signal is cut off. Therefore, cutting an external clock input gives no problem inside in this mode.



(ii) **PS mode clear** The PS mode is cleared by detecting the fall of the M1 signal. When the external clock is off in the PS mode, however, a stable clock signal must be input before clearing the PS mode.

When the CPU (LH5080L/LH5080LM) is cleared from the PS mode and comes into the next fetch cycle, therefore, the LH5081L/LH5081LM is also cleared from its PS mode at the fall of the first M1 signal in this cycle.

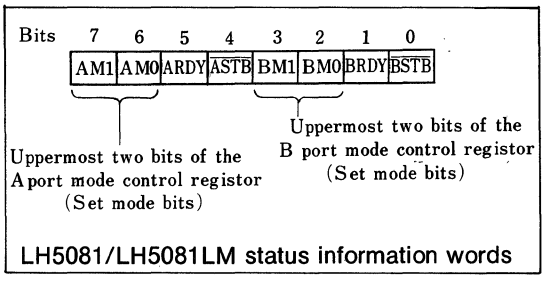
The PS mode clearing can be done by issuing an interrupt request.

Set up the interrupt generate conditions in Mode 3 of the LH5081L/LH5081LM. By this, an interrupt request (INT) is issued even in the PS mode, the CPU (LH5080L/LH5080LM) is cleared from the PS mode, and thus LH5081L/LH5081LM is also cleared.

(2) Status information read

Under the following conditions, the mode setup bits and handshake signals of Port A and Port B are read from the data bus during the read cycle. See the chart below.

Conditions: CE = "Low", RD = "Low", IORQ = "Low", C/D = "High", B/A = X (undefined)



LH5081/LH5081LM status information words

LH5082/LH5082L/LH5082LM

Z80 CMOS Counter Timer Circuit

■ Description

The LH5082 is Z80 CTC fabricated with CMOS silicon-gate process technology and is fully compatible with the conventional NMOS Z80 CTC (LH0082).

The LH5082 is designed with CMOS fully static circuits and so provides low power consumption and wide range power supply voltage operation.

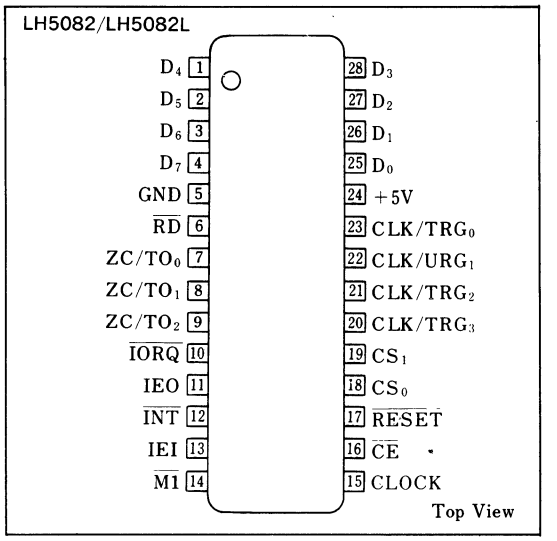
The LH5082L/LH5082LM provides power save mode controlled by software.

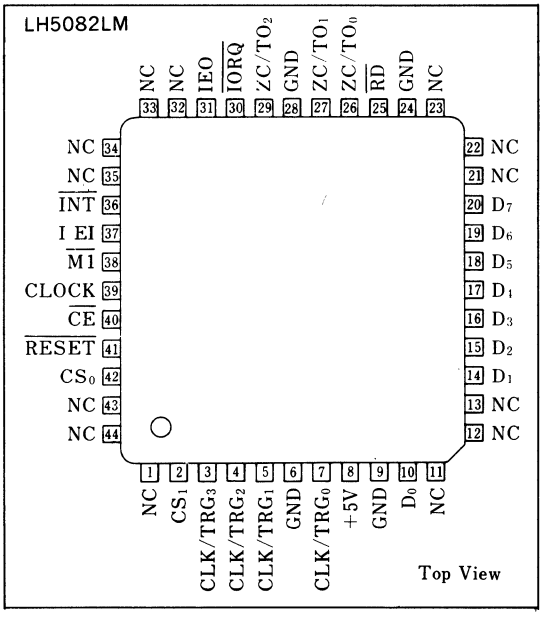
■ Features

1. Z80 CMOS CTC
2. Fully compatible with the NMOS Z80 CTC (LH0082)
3. 4 independent programmable 8-bit counter/16-bit timer channels
4. Selectable counter/timer mode for each channel
5. Programmable interrupt triggered by counter/timer
6. Downcounters reloaded automatically at zero count
7. Readable downcounters
8. Selectable 16 or 256 prescaler (timer mode)
9. Selectable positive or negative triggers for timer and selectable positive or negative clock edge for counter
10. ZC/TO outputs of three channels capable of driving Darlington transistors
11. Vectored and daisy chain piority interrupt
12. Single +5V power supply and single phase clock
13. All inputs and outputs except clock input fully TTL compatible
14. Fully static operation (DC~2.5MHz)
15. Low power consumption
16. Power save mode (LH5082L/LH5082LM)
17. 28-pin dual-in-line package (LH5082/LH5082L)
18. 44-pin quad-flat package (LH5082LM)

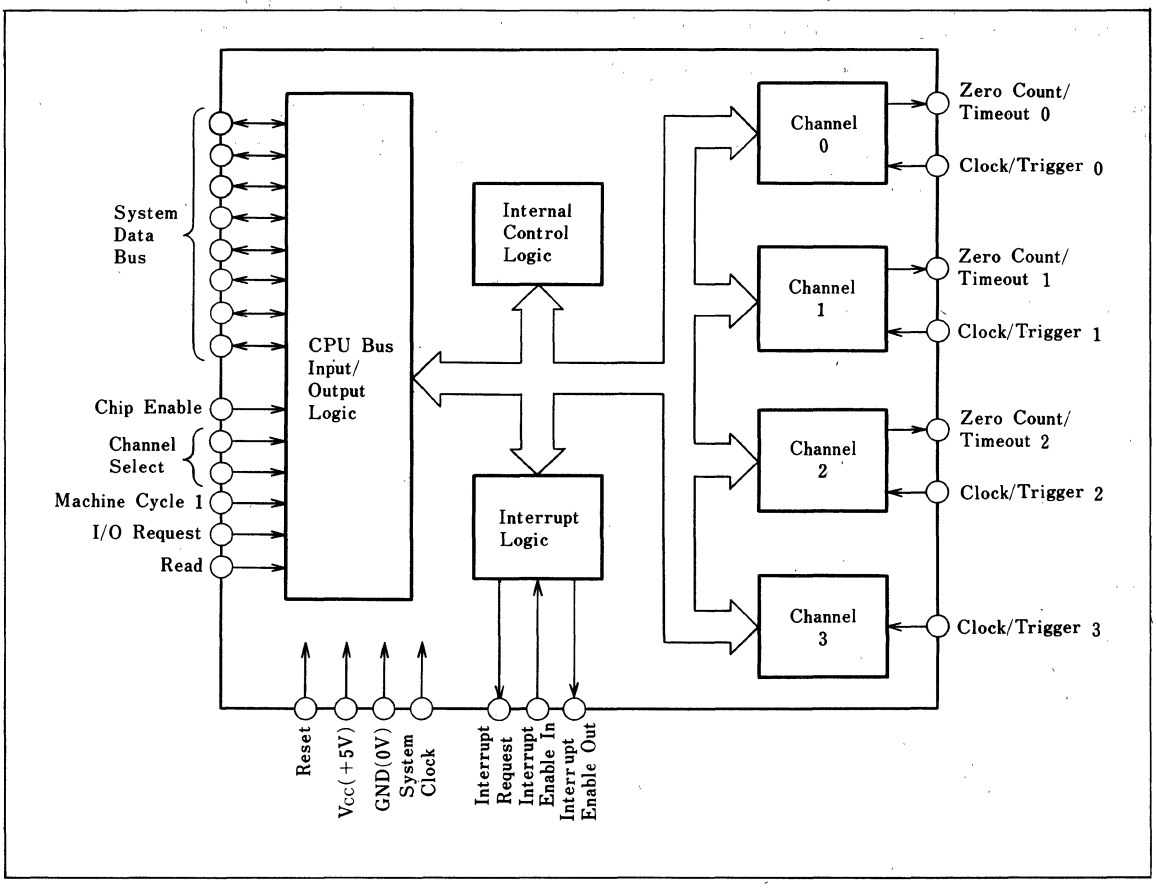
Note: The Z80 CMOS CTC (LH5082/LH5082L/LH5082LM) is compatible with the Z80 NMOS CTC (LH0082). So there is no description here about the pins, programming, and basic timing waveform. Refer back to the Z80 NMOS CTC described earlier.

■ Pin Connections





■ Block Diagram



■ Absolute Maximum Ratings

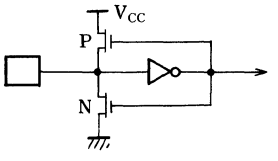
Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	−0.3～+7.0	V
Input voltage	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage	V_{OUT}	−0.3～V_{CC}+0:3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock input low voltage	V_{ILC}		−0.3		0.45	V	
Clock input high voltage	V_{IHC}		V_{CC}−0.6		V_{CC}+0.3	V	
Input low voltage	V_{IL}		−0.3		0.8	V	
Input high voltage	V_{LH}		2.2		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=2mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=−1.6mA	2.4			V	
		I_{OH}=−250 μA	V_{CC}−0.4V			V	
Current consumption	$\|I_{CC}\|$	(Note)		2.5	8	mA	
Input leakage current	$\|I_{LI}\|$	V_{IN}=0V, V_{CC}			10	μA	1
3-state output leakage current	$\|I_{LOH}\|$	V_{OUT}=V_{CC}			10	μA	
3-state output leakage current	$\|I_{IOL}\|$	V_{OUT}=0V			10	μA	
Darlington drive current	I_{OHD}	V_{OH}=1.5V Applicated to ZC/TO_0～ZC/TO_2	−1.5			mA	
Current consumption in PS mode (LH5082L/LH5082LM)	I_{CCPS}	Output pin open, V_{IN}=0V, V_{CC}		1	100	μA	

Note : TcC=400ns, TcCTR=1 μs, V_{IL}=0.4V, V_{IH}=V_{CC}−0.4V, output pin open.
Note 1 : The CLK/TRG_0-CLK/TG_3 pins arranged as shown below.



■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground	5	pF
Input capacitance	C_{IN}		5	pF
Output capacitance	C_{OUT}		10	pF

■ AC Characteristics

(V_{CC}=5V±10%, Ta=0~+70℃)

No.	Parameter	Symbol	MIN.	MAX.	Unit	Note
1	Clock cycle time	TcC	400	(Note 1)	ns	
2	Clock width (high)	TwCh	170		ns	
3	Clock width (low)	TwCl	170		ns	
4	Clock fall time	TfC		30	ns	
5	Clock rise time	TrC		30	ns	
6	All hold times	Th	15		ns	
7	CS to clock ↑ setup time	TsCS (C)	250		ns	
8	$\overline{CE}$ to clock ↑ setup time	TsCE (C)	200		ns	
9	$\overline{IORQ}$ ↓ to clock ↑ setup time	TsIO (C)	250		ns	
10	$\overline{RD}$ ↓ clock ↑ setup time	TsRD (C)	240		ns	
11	Clock ↑ to data out delay	TdC (DO)		240	ns	2
12	Clock ↓ to data out float delay	TdC (DOz)		230	ns	
13	Data In to clock ↑ setup time	TsDI (C)	60		ns	
14	$\overline{M1}$ to clock ↑ setup time	TsM1 (C)	210		ns	
15	$\overline{M1}$ ↓ to IEO ↓ delay (interrupt immediately preceding $\overline{M1}$)	TdM1 (IEO)		300	ns	3
16	$\overline{IORQ}$ ↓ to data out delay (INTA cycle)	TdIO (DOI)		340	ns	2
17	IEI ↓ to IEO ↓ delay	TdIEI (IEOf)		190	ns	3
18	IEI ↑ to IEO ↑ delay (after ED decode)	TdIEI (IEOr)		220	ns	3
19	Clock ↑ to $\overline{INT}$ ↓ delay	TdC (INT)		TcC+200	ns	4
20	CLK/TRG ↑ to $\overline{INT}$ ↓ delay (tsCTR (C) satisfied)	TdCLK (INT)		TcC+230	ns	5
	CLK/TRG ↑ to $\overline{INT}$ ↓ delay (tsCTR (C) not satisfied)	TdCLK (INT)		2TcC+530	ns	5
21	CLK/TRG cycle time	TcCTR	2TcC		ns	5
22	CLK/TRG rise time	TrCTR		50	ns	
23	CLK/TRG fall time	TfCTR		50	ns	
24	CLK/TRG width (low)	TwCTRl	200		ns	
25	CLK/TRG width (high)	TwCTRh	200		ns	
26	CLK/TRG ↑ to clock ↑ setup time for immediate count	TsCTR (Cs)	300		ns	5
27	CLK/TRG ↑ to clock ↑ setup time for enabling of prescaler on following clock ↑	TsCTR (Ct)	210		ns	4
28	Clock ↑ to ZC/TO ↑ delay	TdC (ZC/TOr)		260	ns	
29	Clock ↑ to ZC/TO ↓ delay	TdC(ZC/TOf)		190	ns	
30	IEI setup time to $\overline{IORQ}$ ↓ (INTA cycle)	TsIEI (IO)	140		ns	

↑ Rising edge, ↓ Falling edge

[A] 2.5 TcC>(n-2) TdIEI (IEOf)+TdMI (IEO) +TsIEI (IO)+TTL buffer delay, if any.

[B] $\overline{RESET}$ must be active for minimum of 3 clock cycles

Note 1 : TcC=TwCh+TwCl+TrC+TfC.

Note 2 : Increase delay by 10 ns for each 50 pF increase in loading, 200 pF maximum for data lines, and 100 pF for control lines.

Note 3 : Increase delay by 2 ns for each 10 pF increase in loading, 100 pF maximum.

Note 4 : Timer mode.

Note 5 : Counter mode.

* All timing are preliminary and subject to change.

AC Test Conditions

- Input voltage amplitude: 0.4 V to 2.8 V
- Clock input voltage amplitude: 0.4V to V_{CC}-0.6V
- Input signal rise and fall time: 10 ns
- Input judge level: 0.8 V and 2.0 V
- Output judge level: 0.8 V and 2.0 V
- Output load: ITTL + 100 pF (unless otherwise specified)

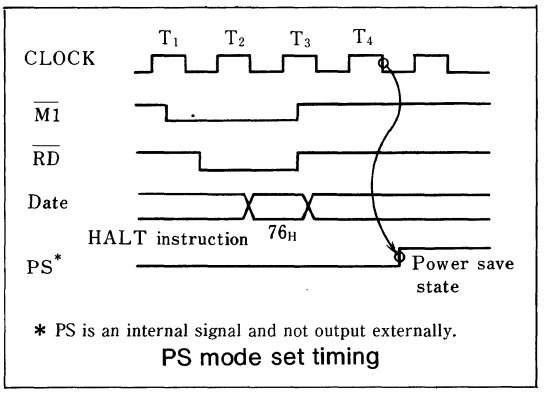
■ Power Save Function

The LH5082L/LH5082LM has the power save (PS) function.

(1) PS mode setting

When the CPU (LH5080L/LH5080LM) has executed a HALT instruction, the LH5082L/LH5082 LM reads this HALT instruction to autmatically go into the PS mode. In this mode, the internal clock signal is cut off. The external clock may be off during the PS mode.

About the external clock stop, the same is true as the power-saving CPU (LH5080L/LH5080LM).



* PS is an internal signal and not output externally.

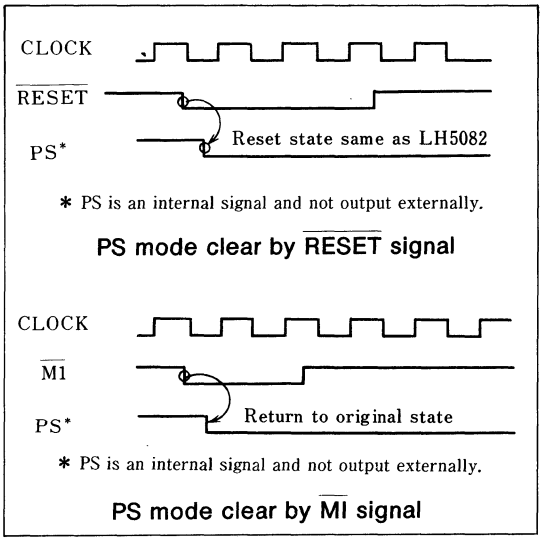
PS mode set timing

(2) PS mode clear

The PS mode is cleared by the fall of $\overline{M1}$ signal or the $\overline{RESET}$ signal.

When the external clock is off the PS mode, however, a stable clock signal must be input before clearing the PS mode.

Once cleared from the PS mode, the power-saving CPU (LH5080L/LH5080LM) comes into the next fetch cycle. At the time when the first $\overline{M1}$ signal during this cycle falls, the LH5082L/LH5082LM is also cleared from the PS mode.



16-Bit Microprocessor and Peripheral LSIs

5

LH8001/LH8001A/LH8002/LH8002A

Z8001/Z8001A/Z8002/Z8002A Central Processing Unit

■ Description

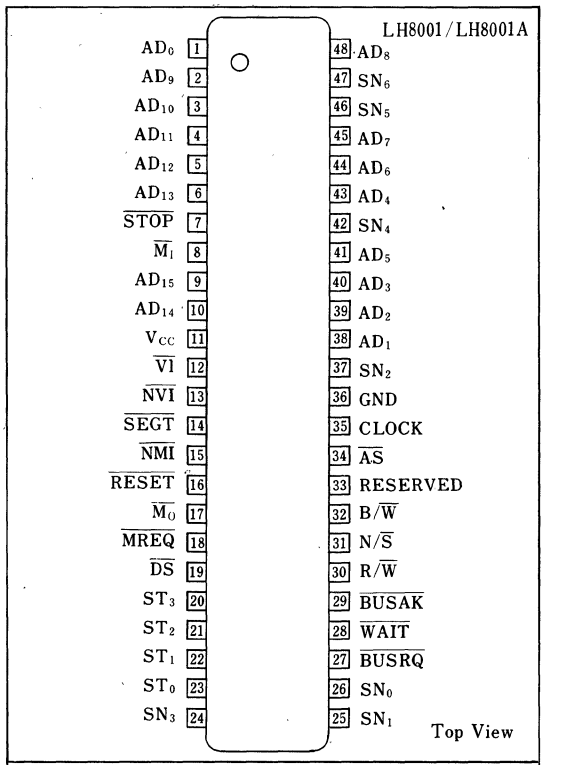
LH8001, Z8001 CPU and LH8002, Z8002 CPU are advanced 16-bit microprocessor that spans a wide variety of applications ranging from simple stand-alone computers to complex parallel-processing unit. Essentially Z8000 CPU is a monolithic minicomputer central processing unit.

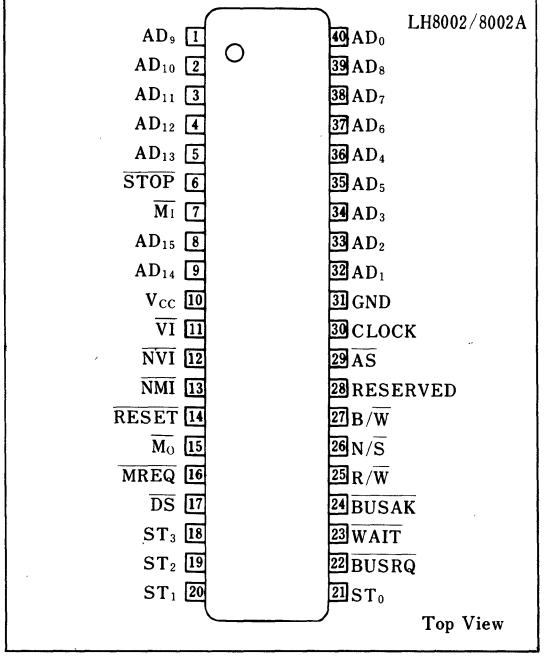
The LH8001A Z8001A and LH8002A Z8002A CPU are the high speed version which can operate at 6MHz system clock.

■ Features

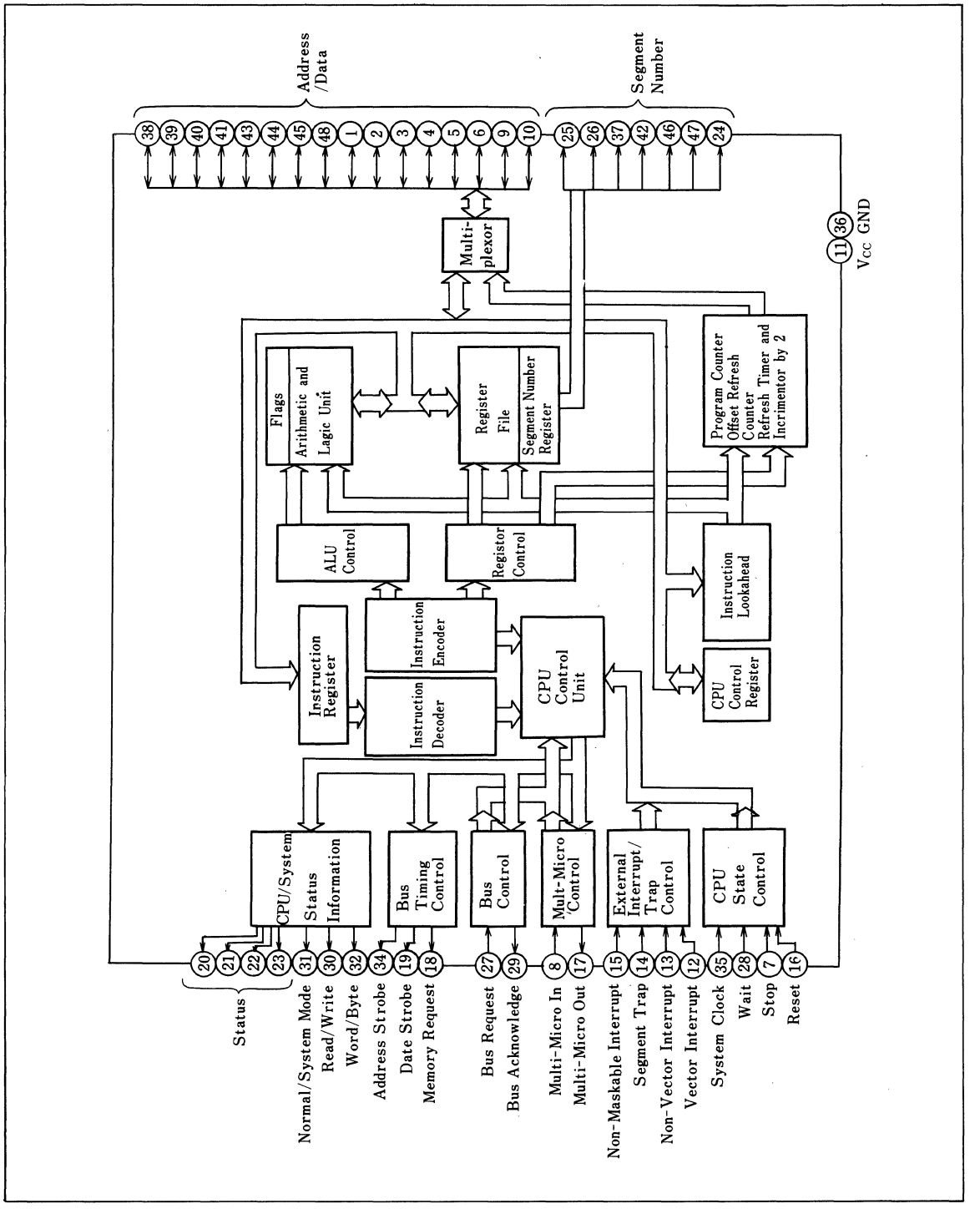
1. Regular, easy-to-use architecture
2. Instruction set more powerful than many minicomputers
3. Directly addresses 8M bytes
4. Eight user-selectable addressing modes
5. Seven data types that range from bits to 32-bit long words and word strings
6. System and Normal operating modes
7. Separate code, data and stack spaces
8. Sophisticated interrupt structure
9. Resource-sharing capabilities for multiprocessing systems
10. Multi-programming support
11. Compiler support
12. Memory management and protection provided by Z8010 Memory Management Unit
13. 32-bit operations, including signed multiply and divide
14. Z-BUS compatible

■ Pin Connections





Block Diagram



■ Pin Description

Pin	Meaning	I/O	Function
$AD_0 \sim AD_{15}$	Address/data bus	Bidirectional 3-state	Multiplexed system address and data bus.
$\overline{AS}$	Address strobe	3-state O	Active "Low". Addresses are valid.
$\overline{DS}$	Data strobe	3-state O	Active "Low". Data are valid.
R/$\overline{W}$	Read/write	3-state O	Read at "High". Write at "Low".
B/$\overline{W}$	Byte/word	3-state O	Byte at "High". Word at "Low".
$\overline{MREQ}$	Memory request	3-state O	Active "Low". For memory access.
$ST_0 \sim ST_3$	Status	3-state O	Specifies CPU status.
N/$\overline{S}$	Normal/system mode	3-state O	Normal mode at "High", System mode at "Low".
$SN_0 \sim SN_6$	Segment number	3-state O	Designates segments to be accessed (for Z8001 CPU only).
$\overline{SEGT}$	Segment trap	I	Active "Low". Detects a segmentation trap from the Z8010 MMU.
$\overline{BUSRQ}$	Bus request	I	Active "Low". Requests the bus line.
$\overline{BUSAK}$	Bus acknowledge	O	Active "Low". Indicates the relinquished control of the bus.
$\overline{RESET}$	Reset	I	Active "Low", Resets the Z8000 CPU.
$\overline{NMI}$	Non-maskable interrupt	I	Active "Low". High-to-low transition not interrupted non-maskable.
$\overline{VI}$	Vectored interrupt	I	Active "Low". Requests a vectored interrupt.
$\overline{NVI}$	Non-vectored Interrupt	I	Active "Low". Requests a non-vectored interrupt.
$\overline{STOP}$	Stop	I	Active "Low". For single-step instruction execution.
$\overline{WAIT}$	Wait	I	Active "Low". For synchronizing with a peripheral device.
$\overline{M_1}$	Multi-micro I	I	Active "Low". Forms a resource-request daisy chain.
$\overline{M_0}$	Multi-micro O	O	Active "Low". Forms a resource-request daisy chain.
CLOCK	System clock	I	Single-phase clock.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7.0	V
Output voltage	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0~+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Clock input high voltage	V_{CH}	Driven by external clock oscillator	$V_{CC}-0.4$	$V_{CC}+0.3$	V
Clock input low voltage	V_{CL}	Driven by external clock oscillator	−0.3	0.45	V
Input high voltage	V_{IH}		2.0	$V_{CC}+0.3$	V
Input low voltage	V_{IL}		−0.3	0.8	V
Output high voltage	V_{OH}	$I_{OH}=-250\,\mu A$	2.4		V
Output low voltage	V_{OL}	$I_{OL}=+2.0mA$		0.4	V
Input leakage current	$\lvert I_{IL} \rvert$	$0.4 \leqq V_{IN} \leqq 2.4V$		10	μA
Output leakage current	$\lvert I_{OL} \rvert$	$0.4 \leqq V_{OUT} \leqq 2.4V$		10	μA
Current consumption	I_{CC}			300	mA

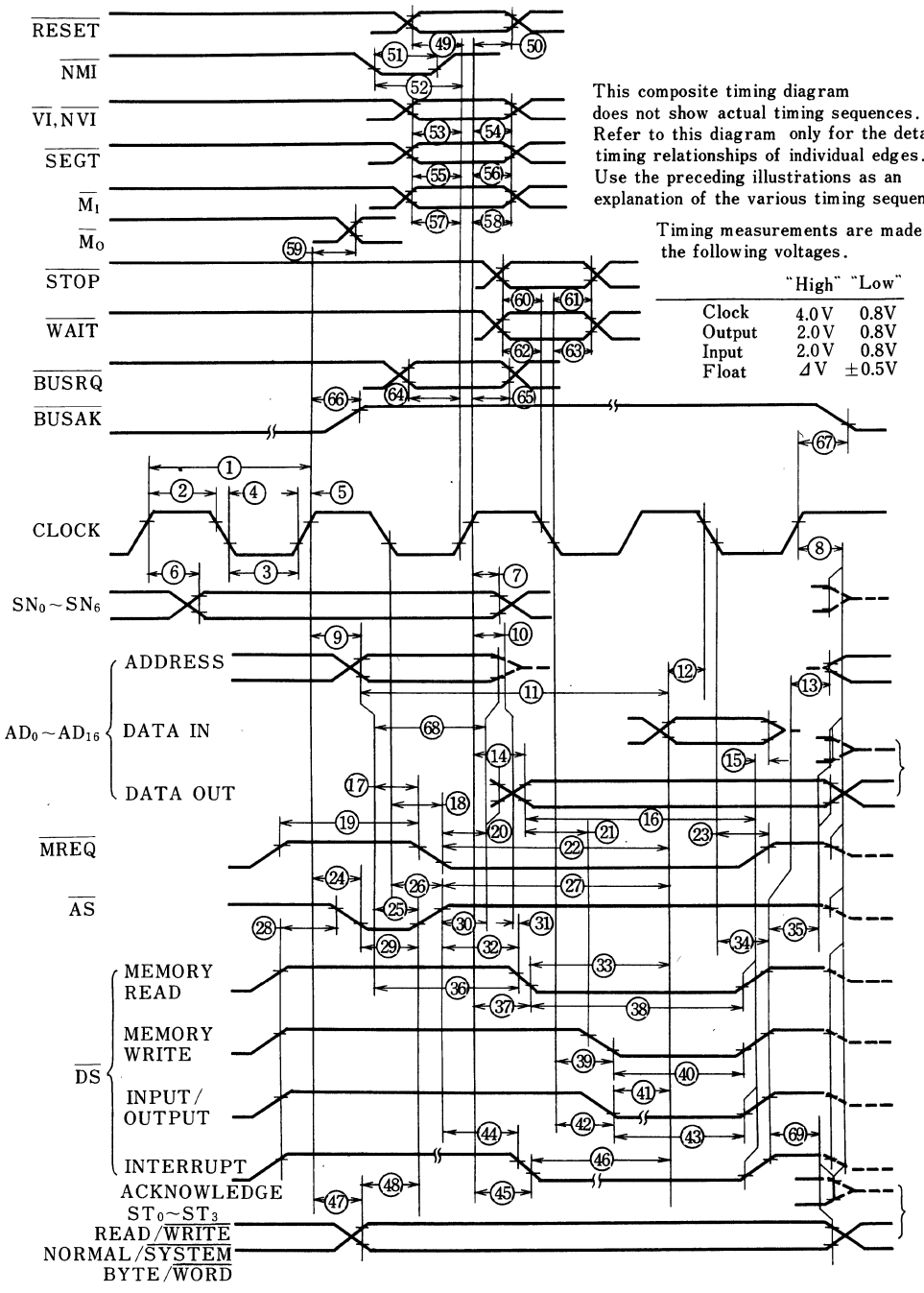
■ AC Characteristics

Number	Symbol	Parameter	LH8001/LH8002(4MHz)		LH8001A/LH8002A(6MHz)		Unit
			MIN.	MAX.	MIN.	MAX.	
1	TcC	Clock cycle time	250	2000	165	2000	ns
2	TwCh	Clock width (high)	105	2000	70	2000	ns
3	TwCl	Clock width (low)	105	2000	70	2000	ns
4	TfC	Clock fall time		20		10	ns
5	TrC	Clock rise time		20		15	ns
6	TdC (SNv)	Clock ↑ to segment number valid (50 pF load)		130		110	ns
7	TdC (SNn)	Clock ↑ to segment number not valid	20		10		ns
8	TdC (Bz)	Clock ↑ to bus float		65		55	ns
9	TdC (A)	Clock ↑ to address valid		100		75	ns
10	TdC (Az)	Clock ↑ to address float		65		55	ns
11	TdA (DR)	Address valid to read data required valid		475*		305	ns
12	TsDI (C)	Read data to clock ↓ setup time	30		20		ns
13	TdDS (A)	$\overline{DS}$ ↑ to address active	80*		45*		ns
14	TdC (DW)	Clock ↑ to write data valid		100		75	ns
15	ThDR (DS)	Read data to $\overline{DS}$ ↑ hold time	0		0		ns
16	TdDW (DS)	Write data valid to $\overline{DS}$ ↑ delay	295*		195*		ns
17	TdA (MR)	Address valid to $\overline{MREQ}$ ↓ delay	55*		35*		ns
18	TdC (MR)	Clock ↓ to $\overline{MREQ}$ ↓ delay		80		70	ns
19	TwMRh	$\overline{MREQ}$ width (high)	210*		135*		ns
20	TdMR (A)	$\overline{MREQ}$ ↓ to address not active	70*		35*		ns
21	TdDW (DSW)	Write data valid to $\overline{DS}$ ↓ (write) delay	55*		35*		ns
22	TdMR (DR)	$\overline{MREQ}$ ↓ to read data required valid	375*		230*		ns
23	TdC (MR)	Clock ↓ $\overline{MREQ}$ ↑ delay		80		60	ns
24	TdC (ASf)	Clock ↑ to $\overline{AS}$ ↓ delay		80		60	ns
25	TdA (AS)	Address valid to $\overline{AS}$ ↑ delay	55*		35*		ns
26	TdC (ASr)	Clock ↓ to $\overline{AS}$ ↑ delay		90		80	ns
27	TdAS (DR)	$\overline{AS}$ ↑ to read data required valid	360*		220*		ns
28	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay	70*		35*		ns
29	TwAS	$\overline{AS}$ width (low)	85*		55*		ns
30	TdAS (A)	$\overline{AS}$ ↑ to address not active delay	70*		45*		ns
31	TdAz (DSR)	Address float to $\overline{DS}$ (read) ↓ delay	0		0		ns
32	TdAS (DSR)	$\overline{AS}$ ↑ to $\overline{DS}$ (read) ↓ delay	80*		55*		ns
33	TdDSR (DR)	$\overline{DS}$ (read) ↓ to read data required valid	205*		130*		ns
34	TdC (DSr)	Clock ↓ to $\overline{DS}$ ↑ delay		70		65	ns
35	TdDS (DW)	$\overline{DS}$ ↑ to write data not valid	75*		45		ns

Number	Symbol	Parameter	LH8001/LH8002(4MHz)		LH8001A/LH8002A(6MHz)		Unit
			MIN.	MAX.	MIN.	MAX.	
36	TdA (DSR)	Address valid to $\overline{DS}$ (read) ↓ delay	180*		110*		ns
37	TdC (DSR)	Clock ↑ to $\overline{DS}$ (read) ↓ delay		120		85	ns
38	TwDSR	$\overline{DS}$ (read) width (low)	275*		185*		ns
39	TdC (DSW)	Clock ↓ to $\overline{DS}$ (write) ↓ delay		95		80	ns
40	TwDSW	$\overline{DS}$ (write) width (low)	185*		110*		ns
41	TdDSI (DI)	$\overline{DS}$ (I/O) ↓ to read data required valid	330*		210*		ns
42	TdC (DSf)	Clock ↓ to $\overline{DS}$ (I/O) ↓ delay		120		90	ns
43	TwDS	$\overline{DS}$ (I/O) width (low)	410*		255*		ns
44	TdAS (DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (acknowledge) ↓ delay	1065*		690*		ns
45	TdC (DSA)	Clock ↑ to $\overline{DS}$ (acknowledge) ↓ delay		120		85	ns
46	TdDSA (DR)	$\overline{DS}$ (acknowledge) ↓ to read data required delay	455*		295*		ns
47	TdC (S)	Clock ↑ to status valid delay		110		85	ns
48	TdS (AS)	Status valid to $\overline{AS}$ ↑ delay	50*		30*		ns
49	TsR (C)	$\overline{RESET}$ to clock ↑ setup time	180		70		ns
50	ThR (C)	$\overline{RESET}$ to clock ↑ hold time	0		0		ns
51	TwNMI	$\overline{NMI}$ width (low)	100		70		ns
52	TsNMI (C)	$\overline{NMI}$ to clock ↑ setup time	140		70		ns
53	TsVI (C)	$\overline{VI}$, $\overline{NVI}$ to clock ↑ setup time	110		50		ns
54	ThVI (C)	$\overline{VI}$, $\overline{NVI}$ to clock ↑ hold time	20		20		ns
55	TsSGT (C)	$\overline{SEGT}$ to clock ↑ setup time	70		55		ns
56	ThSGT (C)	$\overline{SEGT}$ to clock ↑ hold time	0		0		ns
57	TsMI (C)	$\overline{MI}$ to clock ↑ setup time	180		140		ns
58	ThMI (C)	$\overline{MI}$ to clock ↑ hold time	0		0		ns
59	TdC (MO)	Clock ↑ to $\overline{MO}$ delay		120		85	ns
60	TsSTP (C)	$\overline{STOP}$ to clock ↓ setup time	140		100		ns
61	ThSTP (C)	$\overline{STOP}$ to clock ↓ hold time	0		0		ns
62	TsW (C)	$\overline{WAIT}$ to clock ↓ setup time	50		30		ns
63	ThW (C)	$\overline{WAIT}$ to clock ↓ hold time	10		10		ns
64	TsBRQ (C)	$\overline{BUSREQ}$ to clock ↑ setup time	90		80		ns
65	ThBRQ (C)	$\overline{BUSREQ}$ to clock ↑ hold time	10		10		ns
66	TdC (BAKr)	Clock ↑ to $\overline{BUSACK}$ ↑ delay		100		75	ns
67	TdC (BAKf)	Clock ↑ to $\overline{BUSACK}$ ↓ delay		100		75	ns
68	TwA	Address valid width	150*		95*		ns
69	TdDS (S)	$\overline{DS}$ ↑ to STATUS not valid	80*		55*		ns

Note: ↑ Rising, ↓ Falling, (1) 2TcC+TwCh−130ns
* Clock-cycle-time-dependent characteristics.

■ Composite AC Timing Diagram



This composite timing diagram does not show actual timing sequences. Refer to this diagram only for the detailed timing relationships of individual edges. Use the preceding illustrations as an explanation of the various timing sequences.

Timing measurements are made at the following voltages.

	"High"	"Low"
Clock	4.0 V	0.8V
Output	2.0 V	0.8V
Input	2.0 V	0.8V
Float	⊿V	±0.5V

■ Register Organization

The Z8000 CPU is a register-oriented machine that offers sixteen 16-bit general-purpose registers and a set of special system registers.

(1) General-purpose register

All general-purpose registers can be used as accumulators and all but one as index registers or memory pointers.

Register flexibility is created by grouping and overlapping multiple registers (Fig. 1 and 2). For byte operations, the first eight 16-bit registers (R0...R7) are treated as sixteen 8-bit registers (RL0, RH0, ..., RL7, RH7). The sixteen 16-bit registers are grouped in pairs (RR0 ... RR14) to form 32-bit long-word registers. Similarly, the register set is grouped in quadruples (RQ0 ... RQ12) to form 64-bit registers.

(2) Specific -purpose register

The Z8000 CUP has the following specific-purpose registers.

- Refresh counter
- Program status register
- Program status area pointer

The refresh counter can be used to automatically refresh dynamic memory. The refresh counter register consists of a 9-bit row counter, a 6-bit rate counter and an enable bit (Fig. 3).

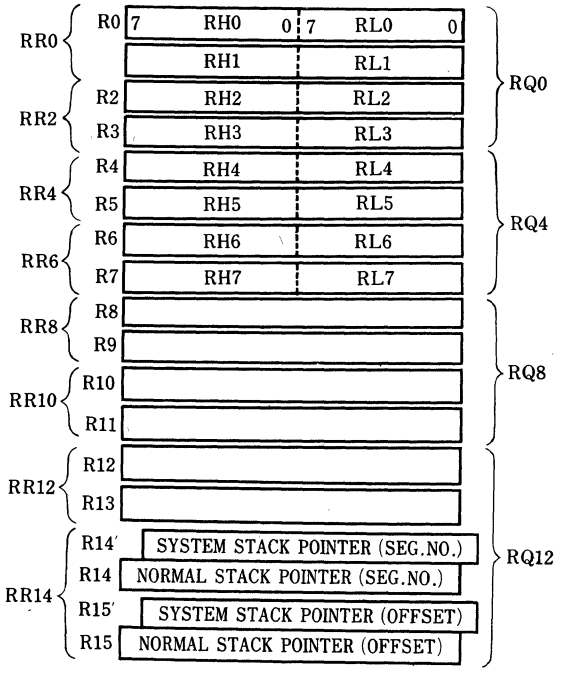


Fig. 1 Z8001 general-purpose register

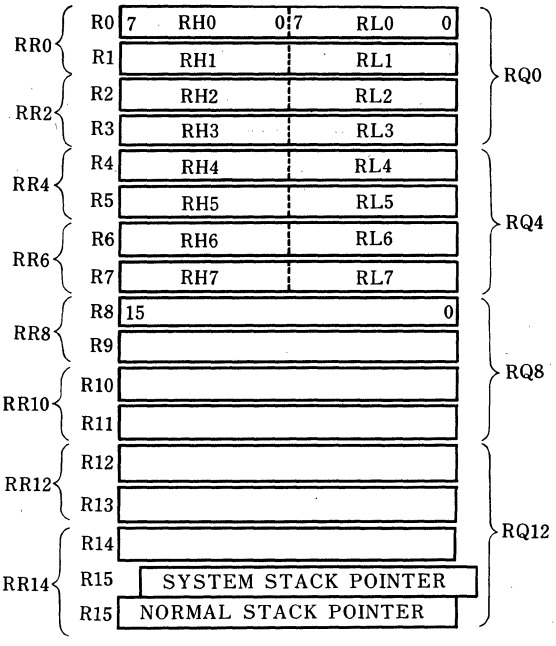


Fig. 2 Z8002 general-purpose register

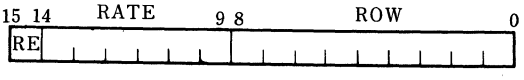


Fig. 3 Refresh counter

This group of status registers contains the program counter, flags and control words. When an interrupt or trap occurs, the entire group is saved and a new program status group is loaded.

Fig. 4 illustrates how the program status groups of the Z8001 and Z8002 differ.

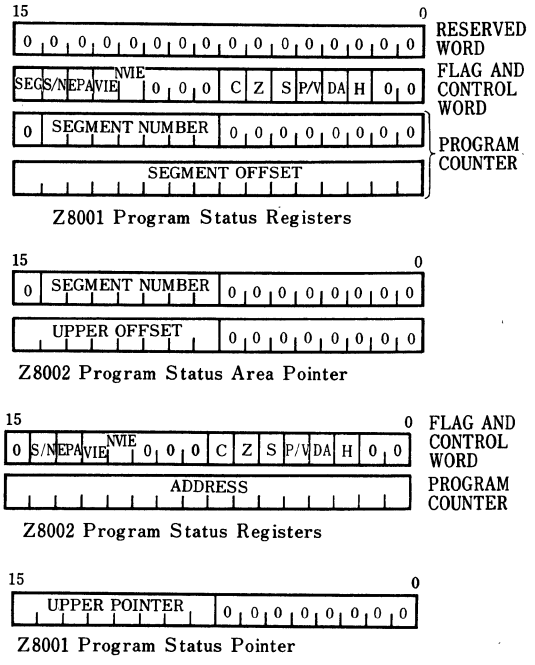


Fig. 4 Z8000 CPU status group

■ Interrupt and Trap Structure

The Z8000 provides a very flexible and powerful interrupt and trap structure. Interrupts are external asynchronous events requiring CPU attention, and are generally triggered by peripherals needing service. Traps are synchronous events resulting from the execution of certain instructions. Both are processes in a similar manner by the CPU.

The CPU supports three types of interrupts (non-maskable, vectored and non-vectored) and four traps (system call, Extended Process Architecture instruction, privileged instructions and segmentation trap). The vectored and non-vectored interrupts are maskable. Of the four traps, the only external one is the segmentation trap, which is generated by the Z8010.

The remaining traps occur when instructions limited to the system mode are used in the normal mode, or as a result of the System Call instruction, or for an EPA instruction. The descending order of priority for traps and interrupts is : internal traps, non-maskable interrupt, segmentation trap, vectored interrupt and non-vectored interrupt.

When an interrupt or trap occurs, the current program status is automatically pushed on the system stack. The program status consists of the processor status (PC and FCW) plus a 16-bit identifier. The indentifier contains the reason or source of the trap or interrupt. For internal traps, the identifier is the first word of the trapped instruction. For external traps or interrupts, the identifier is the vector on the data bus read by the CPU during the interrupt-acknowlege or trap-acknowlege cycle.

After saving the current program status, the new program status is automatically loaded from the program status area in system memory. This area is designated by the program status area pointer (PSAP).

■ Data Type

Z8000 instructions can operate on bits, BCD digits (4bits), bytes (8 bits), words (16 bits), long words (32 bits) and byte strings and word strings (up to 64 kilobytes long). Bits can be set, reset and tested ; digits are used in BCD arithmetic operations ; bytes are used for characters or small integer values ; words are used for integer values, instructions and nonsegmented addresses ; long words are used for long integer values and segmented addresses. All data elements except strings can reside either in registers or momory. Strings are stored in memory only.

The basic data element is the byte. The number of bytes used when manipulating a data element is either implied by the operation or-for strings and multiple register operations-explicitly specified in the instruction.

■ Addressing Modes

Mode	Operand Addressing			Operand Value
	In the Instruction	In a Register	In Memory	
Register (R)		REGISTER ADDRESS → OPERAND		The content of the register
Immediate (IM)	OPERAND			In the instruction
Indirect Register (IR)		REGISTER ADDRESS → ADDRESS	→ OPERAND	The content of the location whose address is in the register
Direct Address (DA)	ADDRESS		→ OPERAND	The content of the location whose address is in the instruction
Index (X)		REGISTER ADDRESS → DISPLACEMENT BASE ADDRESS	→ (+) → OPERAND	The content of the location whose address is the address in the instruction, offset by the content of the register
Relative Address (RA)	DISPLACEMENT	PC VALUE	→ (+) → OPERAND	The content of the location whose address is the content of the program counter, offset by the displacement in the instruction
Base Address (BA)		REGISTER ADDRESS → BASE ADDRESS DISPLACEMENT	→ (+) → OPERAND	The content of the location whose address is the address in the resister, offset by the displacement in the instruction
Base Index (BX)		REGISTER ADDRESS → BASE ADDRESS REGISTER ADDRESS → DISPLACEMENT	→ (+) → OPERAND	The content of the location whose address is the address in the register, offset by the displacement in the register

■ Instruction Set Summary

The Z8000 provides the following types of instructions :

- Load and Exchange
- Arithmetic
- Logical
- Program Control

Instruction Set

- Bit Manipulation
- Rotate and Shift
- Block Transfer and String Manipulation
- Input/Output
- CPU Control

	Mnemonics	Operands	Addr. Modes	Clock Cycles*1 Word Byte NS	SS	SL	Long Word NS	SS	SL	Operation
Load and Exchange	**CLR**	dst	R	7	—	—				Clear
	CLRB		IR	8	—	—				dst ← 0
			DA	11	12	14				
			X	12	12	15				
	EX	R, src	R	6	—	—				Exchange
	EXB		IR	12	—	—				R ↔ src
			DA	15	16	18				
			X	16	16	19				
	LD	R, src	R	3	—	—	5	—	—	Load into Register
	LDB		IM	7	—	—	11	—	—	R ← src
	LDL		IM	5 (Byte only)						
			IR	7	—	—	11	—	—	
			DA	9	10	12	12	13	15	
			X	10	10	13	13	13	16	
			BA	14	—	—	17	—	—	
			BX	14	—	—	17	—	—	
	LD	dst, R	IR	8	—	—	11	—	—	Load into Memory (Store)
	LDB		DA	11	12	14	14	15	17	dst ← R
	LDL		X	12	12	15	15	15	18	
			BA	14	—	—	17	—	—	
			BX	14	—	—	17	—	—	
	LD	dst, IM	IR	11	—	—				Load Immediate into Memory
	LDB		DA	14	15	17				
			X	15	15	18				dst ← IM
	LDA	R, src	DA	12	13	15				Load Address
			X	13	13	16				R ← source address
			BA	15	—	—				
			BX	15	—	—				
	LDAR	R, src	RA	15	—	—				Load Address Relative
										R ← source address
	LDK	R, src	IM	5	—	—				Load Constant
										R ← n (n=0···15)
	LDM	R, src, n	IR	11	—	—	+3n			Load Multiple
			DA	14	15	17				R ← src (n consecutive words)
			X	15	15	18				(n=1...16)
	LDM	dst, R, n	IR	11	—	—	+3n			Load Multiple (Store Multiple)
			DA	14	15	17				dst ← R (n consecutive words)
			X	15	15	18				(n=1...16)
	LDR	R, src	RA	14	—	—	17	—	—	Load Relative
	LDRB									R ← src
	LDRL									(Range −32, 768···+32, 767)

Note

dst :	destination	cc :	flag	PS :	program status
src :	source	b,n :	nemerical value	ⓐ :	indirect register
flag :	flag	SP :	stack pointer		
		PC :	program counter		

*1: NS=Non Segmented SS=Segmented Short Offset SL=Segmented Long Offset

	Mnemonics	Operands	Addr. Modes	Clock Cycles*1 Word Byte NS	SS	SL	Long Word NS	SS	SL	Operation
Load and Exchange (Continued)	**LDR** **LDRB** **LDRL**	dst, R	RA	14	—	—	17	—	—	Load Relative (Store Relative) dst ← R (Range −32, 768…+32, 767)
	POP **POPL**	dst, IR	R	8	—	—	12	—	—	Pop dst ← IR
			IR	12	—	—	19	—	—	
			DA	16	16	18	23	23	25	Autoincrement contents of R
			X	16	16	19	23	23	26	
	PUSH **PUSHL**	IR, src	R	9	—	—	12	—	—	Push Autodecrement contents of R IR ← src
			IM	12	—	—	—	—	—	
			IR	13	—	—	20	—	—	
			DA	14	14	16	21	21	23	
			X	14	14	17	21	21	24	
Arithmetic	**ADC** **ADCB**	R, src	R	5	—	—				Add with Carry R ← R+src+carry
	ADD **ADDB** **ADDL**	R, src	R	4	—	—	8	—	—	Add R ← R+src
			IM	7	—	—	14	—	—	
			IR	7	—	—	14	—	—	
			DA	9	10	12	15	16	18	
			X	10	10	13	16	16	19	
	CP **CPB** **CPL**	R, src	R	4	—	—	8	—	—	Compare with Register R-src
			IM	7	—	—	14	—	—	
			IR	7	—	—	14	—	—	
			DA	9	10	12	15	16	18	
			X	10	10	13	16	16	19	
	CP **CPB**	dst, IM	IR	11	—	—				Compare with Immediate dst-IM
			DA	14	15	17				
			X	15	15	18				
	DAB	dst	R	5	—	—				Decimal Adjust
	DEC **DECB**	dst, n	R	4	—	—				Decrement by n dst←dst-n (n=1…16)
			IR	11	—	—				
			DA	13	14	16				
			X	14	14	17				
	DIV **DIVL**	R, src	R	107	—	—	744	—	—	Divide (signed) Word : R_{n+1} ← $R_{n,n} \div$ src R_n ← remainder Long Word : $R_{n+2,n+3}$ ← $R_{n\cdots n} \div$ src $R_{n,n+1}$ ← remainder
			IM	107	—	—	744	—	—	
			IR	107	—	—	744	—	—	
			DA	108	109	111	745	746	748	
			X	109	109	112	746	746	749	
	EXTS **EXTSB** **EXTSL**	dst	R	11	—	—	11	—	—	Extend Sign Extend sign of low order half of dst through high order half of dst
	INC **INCB**	dst, n	R	4	—	—				Increment by n dst ← dst+n (n=1…16)
			IR	11	—	—				
			DA	13	14	16				
			X	14	14	17				
	MULT **MULTL**	R, src	R	70	—	—	282*2	—	—	Multiply (Signed) Word : $R_{n,n+1}$ ← $R_{n+1} \cdot$ src Long Word : $R_{n\cdots n+3}$ ← $R_{n+2,n+3} \cdot$ src *2: Plus seven cycles for each 1 in the multiplicand
			IM	70	—	—	282*2	—	—	
			IR	70	—	—	282*2	—	—	
			DA	71	72	74	283*2	284*2	286*2	
			X	72	72	75	284*2	284*2	287*2	

	Mnemonics	Operands	Addr. Modes	Clock Cycles*1 Word Byte NS	SS	SL	Long Word NS	SS	SL	Operation
Arithmetic (Continued)	**NEG**	dst	R	7	—	—				Negate
	NEGB		IR	12	—	—				dst ← 0−dst
			DA	15	16	18				
			X	16	16	19				
	SBC	R, src	R	5	—	—				Subtract with Carry
	SBCB									R ← R-src-carry
	SUB	R, src	R	4	—	—	8	—	—	Subtract
	SUBB		IM	7	—	—	14	—	—	R ← R−src
	SUBL		IR	7	—	—	14	—	—	
			DA	9	10	12	15	16	18	
			X	10	10	13	16	16	19	
Logic	**AND**	R, src	R	4	—	—				AND
	ANDB		IM	7	—	—				R ← R AND src
			IR	7	—	—				
			DA	9	10	12				
			X	10	10	13				
	COM	dst	R	7	—	—				Complement
	COMB		IR	12	—	—				dst ← NOT dst
			DA	15	16	18				
			X	16	16	19				
	OR	R, src	R	4	—	—				OR
	ORB		IM	7	—	—				R ← R OR src
			IR	7	—	—				
			DA	9	10	12				
			X	10	10	13				
	TEST	dst	R	7	—	—	13	—	—	Test
	TESTB		IR	8	—	—	13	—	—	dst OR 0
	TESTL		DA	11	12	14	16	17	19	
			X	12	12	15	17	17	20	
	TCC	cc, dst	R	5	—	—				Test Condition Code
	TCCB									Set LSB if cc is true
	XOR	R, src	R	4	—	—				Exclusive OR
	XORB		IM	7	—	—				R ← R XOR src
			IR	7	—	—				
			DA	9	10	12				
			X	10	10	13				
Program Control	**CALL**	dst	IR	10		15				Call Subroutine
			DA	12	18	20				Autodecrement SP
			X	13	18	21				@SP ← PC
										PC ← dst
	CALR	dst	RA	10	—	15				Call Relative
										Autodecrement SP
										@SP ← PC
										PC ← PC+dst (Range −4,094∼+4,096)
	DJNZ	R, dst	RA	11	—	—				Decrement and Jump if Non-Zero
	DBJNZ									R ← R−1
										If R≠ 0 : PC ← PC+dst (Range−254∼0)

	Mnemonics	Operands	Addr. Modes	Clock Cycles*1 Word Byte NS	SS	SL	Long Word NS	SS	SL	Operation
Program Control (Continued)	**IRET***3	—	—	13	—	16				Interrupt Return SP ← SP+2 PS ← @SP Autoincrement SP
	JP	cc, dst	IR	10	—	15	(taken)			Jump Conditional
			IR	7	—	7	(not taken)			If cc is true : PC ← dst
			DA	7	8	10				
			X	8	8	11				
	JR	cc, dst	RA	6	—	—				Jump Conditional Relative If cc is true : PC ← PC+dst (Range −256~+254)
	RET	cc	—	10	—	13	(taken)			Return Conditional
				7	—	7	(not taken)			If cc is true : PC ← @ SP Autoincrement SP
	SC	src	IM	33	—	39				System Call Autodecrement SP @ SP ← old PS Push instruction PS ← System Call PS
Bit Manipulation	**BIT** **BITB**	dst, b	R	4	—	—				Bit Test Static Z flag ← NOT dst bit specified by b
			IR	8	—	—				
			DA	10	11	13				
			X	11	11	14				
	BIT **BITB**	dst, R	R	10	—	—				Bit Test Dynamic Z flag ← NOT dst bit specified by contents of R
	RES **RESB**	dst, b	R	4	—	—				Reset Bit Static Reset dst bit specified by b
			IR	11	—	—				
			DA	13	14	16				
			X	14	14	17				
	RES **RESB**	dst, R	R	10	—	—				Reset Bit Dynamic Reset dst bit specified by contents of R
	SET **SETS**	dst, b	R	4	—	—				Set Bit Static Set dst bit specified by b
			IR	11	—	—				
			DA	13	14	16				
			X	14	14	17				
	SET **SETS**	dst, R	R	10	—	—				Set Bit Dynamic Set dst bit specified by contents of R
	TSET **TSETB**	dst	R	7	—	—				Test and Set S flag ← MSB of dst dst ← all ls
			IR	11	—	—				
			DA	14	15	17				
			X	15	15	18				

*3: Privileged instruction. Executed system mode only.

	Mnemonics	Operands	Addr. Modes	Clock Cycles*1 Word Byte NS	SS	SL	Long Word NS	SS	SL	Operation
Rotate and Shift	**RLDB**	R, src	R	9	—	—				Rotate Digit Left
	RRDB	R, src	R	9	—	—				Rotate Digit Right
	RL	dst, n	R	6 for n=1						Rotate Left
	RLB		R	7 for n=2						by n bits (n=1, 2)
	RLC	dst, n	R	6 for n=1						Rotate Left through Carry
	RLCB		R	7 for n=2						by n bits (n=1, 2)
	RR	dst, n	R	6 for n=1						Rotate Right
	RRB		R	7 for n=2						by n bits (n=1, 2)
	RRC	dst, n	R	6 for n=1						Rotate Right through Carry
	RRCB		R	7 for n=2						by n bits (n=1, 2)
	SDA	dst, R	R	(15+3n)			(15+3n)			Shift Dynamic Arithmetic
	SDAB									Shift dst left or right
	SDAL									by contents of R
	SDL	dst, R	R	(15+3n)			(15+3n)			Shift Dynamic Logical
	SDLB									Shift dst left or right
	SDLL									by contents of R
	SLA	dst, n	R	(13+3n)			(13+3n)			Shift Left Arithmetic
	SLAB									by n bits
	SLAL									
	SLL	dst, n	R	(13+3n)			(13+3n)			Shift Left Logical
	SLLB									by n bits
	SLLL									
	SRA	dst, n	R	(13+3n)			(13+3n)			Shift Right Arithmetic
	SRAB									by n bits
	SRAL									
	SRL	dst, n	R	(13+3n)			(13+3n)			Shift Right Logical
	SRLB									by n bits
	SRLL									
Block Transfer and String Manipulation	**CPD**	R_x, src, R_Y, cc	IR	20	—	—				Compare and Decrement
	CPDB									$R_X - src$
										Autodecrement src address
										$R_Y \leftarrow R_Y - 1$
	CPDR	R_X, src, R_Y, cc	IR	(11+9n)						Compare, Decrement and Repeat
	CPDRB									$R_X - src$
										Autodecrement src address
										$R_Y \leftarrow R_Y - 1$
										Repeat until cc is true or $R_Y = 0$
	CPI	R_X, src, R_Y, cc	IR	20	—	—				Compare and Increment
	CPIB									$R_X - src$
										Autoincrement src address
										$R_Y \leftarrow R_Y - 1$
	CPIR	R_X, src, R_Y, cc	IR	(11+9n)						Compare, Increment and Repeat
	CPIRB									$R_X - src$
										Autoincrement src address
										$R_Y \leftarrow R_Y - 1$
										Repeat until cc is true or $R_Y = 0$
	CPSD	dst, src, R, cc	IR	25	—	—				Compare String and Decrement
	CPSDB									dst − src
										Autodecrement dst and src addresses
										$R \leftarrow R - 1$

	Mnemonics	Operands	Addr. Modes	Clock Cycles*1 Word Byte NS	SS	SL	Long Word NS	SS	SL	Operation
Block Transfer and String Manipulation (Continued)	**CPSDR** **CPSDRB**	dst, src, R, cc	IR	(11+14n)						Compare String, Decr. and Repeat dst−src Autodecrement dst and src addresses R ← R−1 Repeat until cc is true or R=0
	CPSI **CPSIB**	dst, src, R, cc	IR	25	—	—				Compare String and Increment dst−src Autoincrement dst and src addresses R ← R−1
	CPSIR **CPSIRB**	dst, src, R, cc	IR	(11+14n)						Compare String, Incr. and Repeat dst-src Autoincrement dst and src addresses R ← R−1 Repeat until cc is true or R=0
	LDD **LDDB**	dst, src, R	IR	20	—	—				Load and Decrement dst ← src Autodecrement dst and src addresses R ← R−1
	LDDR **LDDRB**	dst, src, R	IR	(11+9n)						Load, Decrement and Repeat dst ← src Autodecrement dst and src addresses R ← R−1 Repeat until R=0
	LDI **LDIB**	dst, src, R	IR	20	—	—				Load and Increment dst ← src Autoincrement dst and src addresses R ← R−1
	LDIR **LDIRB**	dst, src, R	IR	(11+9n)						Load, Increment and Repeat dst ← src Autoincrement dst and src addresses R ← R−1 Repeat until R=0
	TRDB	dst, src, R	IR	25	—	—				Translate and Decrement dst ← src (dst) Autodecrement dst address R ← R−1

	Mnemonics	Operands	Addr. Modes	Clock Cycles *1 Word Byte NS	SS	SL	Long Word NS	SS	SL	Operation
Block Transfer and String Manipulation (Continued)	**TRDRB**	dst, stc, R	IR	(11+14n)						Translate, Decrement and Repeat dst ← stc (dst) Autodecrement dst address R ← R−1 Repeat until R=0
	TRIB	dst, src, R	IR	25	—	—				Translate and Increment dst ← src (dst) Autoincrement dst address R ← R−1
	TRIRB	dst, src, R	IR	(11+14n)						Translate, Increment and Repeat dst ← src (dst) Autoincrement dst address R ← R−1 Repeat until R=0
	TRTDB	src1, src2, R	IR	25	—	—				Translate and Test, Decrement PH1 ← src2 (src 1) Autodecrement src 1 address R ← R−1
	TRTDRB	src1, src2, R	IR	(11+14n)						Translate and Test, Decr. and Repeat RH1 ← src 2 (src 1) Autodecrement src 1 address R ← R−1 Repeat until R=0 or RH1=0
	TRTIB	src1, src2, R	IR	25	—	—				Translate and Test, Increment RH1 ← src2 (src 1) Autoincrement src 1 address R ← R−1
	TRTIRB	src1, src2, R	IR	(11+14n)						Translate and Test, Incr. and Repeat RH1 ← src 2 (src 1) Autoincrement src 1 address R ← R−1 Repeat until R=0 or RH1=0
Input/ Output	**IN***3 **INB***3	R, src	IR DA	10 12	— —	— —				Input R ← src
	IND*3 **INDB***3	dst, src, R	IR	21	—	—				Input and Decrement dst ← src Autodecrement dst address R ← R−1
	INDR*3 **INDRB***3	dst, src, R	IR	(11+10n)						Input, Decrement and Repeat dst ← src Autodecrement dst address R ← R−1 Repeat until R=0
	INI*3 **INIB***3	dst, src, R	IR	21	—	—				Input and Increment dst ← src Autoincrement dst address R ← R−1

*3: Privileged instructions. Executed in system mode only.

	Mnemonics	Operands	Addr. Modes	Clock Cycles*1 Word Byte NS	SS	SL	Long Word NS	SS	SL	Operation
Input/ Output (Continued)	**INIR***3 **INIRB***3	dst, src, R	IR	(11+10n)						Input, Increment and Repeat dst ← src Autoincrement dst address R ← R−1 Repeat until R=0
	OUT*3 **OUTB***3	dst, R	IR DA	10 12	—	—				Output dst ← R
	OUTD*3 **OUTDB***3	dst, src, R	IR	21	—	—				Output and Decrement dst ← src Autoincrement dst address R ← R−1
	OTDR*3 **OTDRB***3	dst, src, R	IR	(11+10n)						Output, Decrement and Repeat dst ← src Autoincrement dst address R ← R−1 Repeat until R=0
	OUTI*3 **OUTIB***3	dst, src, R	IR	21	—	—				Output and Increment dst ← src Autoincrement dst address R ← R−1
	OTIR*3 **OTIRB***3	dst, src, R	IR	(11+10n)						Output, Increment and Repeat dst ← src Autoincrement dst address R ← R−1 Repeat until R=0
	SIN*3 **SINB***3	R, src	DA	12	—	—				Special Input R ← src
	SIND*3 **SINDB***3	dst, src, R	IR	21	—	—				Special Input and Decrement dst ← src Autoincrement dst address R ← R-1
	SINDR*3 **SINDRB***3	dst, src, R	IR	(11+10n)						Special Input, Decrement and Repeat dst ← src Autoincrement dst address R ← R−1 Repeat until R=0
	SINI*3 **SINIB***3	dst, src, R	IR	21	—	—				Special Input and Increment dst ← src Autoincrement dst address R ← R−1
	SINIR*3 **SINIRB***3	dst, src, R	IR	(11+10n)						Special Input, Increment and Repeat dst ← src Autoincrement dst address R ← R−1 Repeat until R=0
	SOUT*3 **SOUTB***3	dst, src	DA	12	—	—				Special Output dst ← src

*3: Privileged instructions. Executed in system mode only.

	Mnemonics	Operands	Addr. Modes	Clock Cycles *1 Word Byte NS	SS	SL	Long Word NS	SS	SL	Operation
Input/ Output (Continued)	**SOUTD***3 **SOUTDB***3	dst, src, R	IR	21	—	—				Special Output and Decrement dst ← src Autoincrement dst address R ← R−1
	SOTDR*3 **SOTDRB***3	dst, src, R	IR	(11+10n)						Special Output, Decr. and Repeat dst ← src Autoincrement dst address R ← R−1 Repeat until R=0
	SOUTI*3 **SOUTIB***3	dst, src, R	IR	21	—	—				Special Output and Increment dst ← src Autoincrement dst address R ← R−1
	SOTIR*3 **SOTIRB***3	dst, src, R	R	(11+10n)						Special Output, Incr. and Repeat dst ← src Autoincrement dst address R ← R−1 Repeat until R=0
CPU Control	**COMFLG**	flags	—	7	—	—				Complement Flag (Any combination of C, Z, S, P/V)
	DI*3	int	—	7	—	—				Disable Interrupt (Any combination of NVI, VI)
	EI*3	int	—	7	—	—				Enable Interrupt (Any combination of NVI, VI)
	HALT*3	—	—	(8+3n)						HALT
	LDCTL*3	CTLR, src	R	7	—	—				Load into Control Register CTLR ← src
	LDCTL*3	dst, CTLR	R	7	—	—				Load from Control Register dst ← CTLR
	LDCTLB	FLGR, src	R	7	—	—				Load into Flag Byte Register FLGR ← src
	LDCTLB	dst, FLGR	R	7	—	—				Load from Flag Byte Register dst ← FLGR
	LDPS*3	src	IR DA X	12 16 17	— 20 20	16 22 23				Load program Status PS ← src
	MBIT*3	—	—	7	—	—				Test Multi-Micro Bit Reset S if $\overline{M_I}$ is Low ; set S if $\overline{M_I}$ is High.
	MREQ*3	dst	R	(12+7n)						Multi-Micro Request
	MRES*3	—	—	5	—	—				Multi-Micro Reset
	MSET*3	—	—	5	—	—				Multi-Micro Set
	NOP	—	—	7	—	—				No Operation
	RESFLG	flag	—	7	—	—				Reset Flag (Any combination of C, Z, S, P/V)
	SETFLG	flag	—	7	—	—				Set Flag (Any combination of C, Z, S, P/V)

*3: Privileged instructions. Executed in system mode only.

LH8010/LH8010A Z8010/Z8010A Memory Management Unit

■ Description

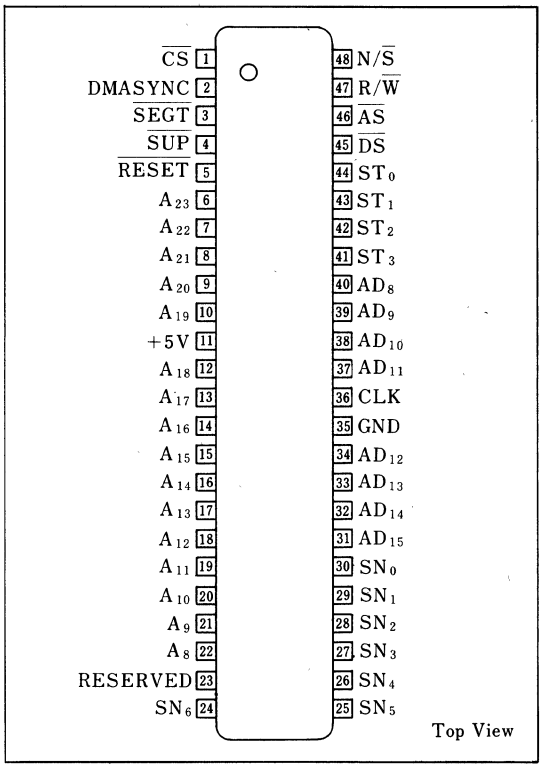
The Z8010 Memory Management Unit (MMU) manages the large 8M byte addressing spaces of the Z8001 CPU. The MMU provides dynamic segment relocation as well as numerous memory protection feature.

Dynamic segment relocation makes user software addresses independent of the physical memory addresses, there by freeing the user from specifying where information is actually located in the physical memory. It also provides a flexible, efficient method for supporting multi-programming systems. The MMU uses a translation table to transform the 23-bit logical address output from the Z8001 CPU into a 24-bit address for the physical memory. (Only logical memory addresses go to an MMU for translation : I/O addresses and data, in general, must bypass this component.)

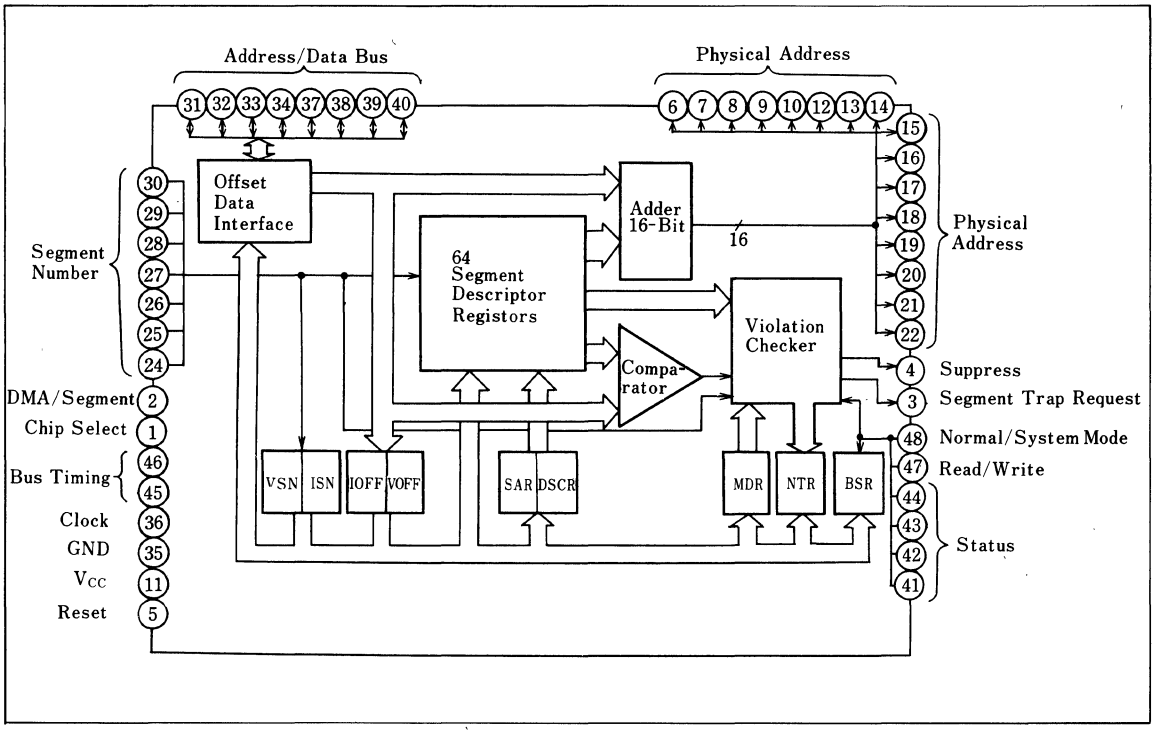
■ Features

1. Dynamic segment relocation makes software addresses independent of physical memory addresses.
2. Sophisticated memory management features include access validation that protects memory areas from unauthorized or unintentional access, and a write-warning indicator that predicts stack overflow.
3. 64 variable-sized segments from 256 to 65,536 bytes can be mapped into a total physical address space of 16M bytes ; all 64 segments are randomly accessible.
4. Multiple MMUs can support several translation tables for each Z8001 address space.
5. MMU architecture supports multiprogramming systems and virtual memory implementations.

■ Pin Connections



■ Block Diagram

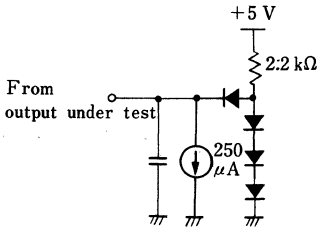


■ Pin Description

Pin	Meaning	I/O	Function
$A_8 \sim A_{23}$	Address bus	3-state O	16 most-significant bits of the physical memory location.
$AD_8 \sim AD_{15}$	Address/data bus	Bidirectional 3-state	8 most-significant bits of the multiplexed system address/data bus.
$\overline{AS}$	Address strobe	I	Active "Low". Addresses are valid.
$\overline{DS}$	Data strobe	I	Active "Low". Data are valid.
$R/\overline{W}$	Read/write	I	Read at "High", Write at "Low".
$N/\overline{S}$	Normal/system	I	Normal mode at "High", System mode at "Low".
$ST_0 \sim ST_3$	Status	I	Specifies Z8001 CPU status.
$SN_0 \sim SN_6$	Segment number	I	Designates segments to be accessed.
$\overline{SUP}$	Suppress	Open drain	Active "Low". Indicates any access violation except write warning.
$\overline{SEGT}$	Segment trap reguest	O	Active "Low". Detects an access violation or write warning.
$\overline{CS}$	Chip select	I	Active "Low". Selects an MMU for a control command.
DMASYNC	DMA/segment number Synchronization strobe	I	Active "High". Segment numbers are valid.
$\overline{RESET}$	Reset	I	Active "Low". Resets the MMU.
CLK	System clock	I	Standard Z8000 system clock used as internal sync signal.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7.0	V
Output voltage	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃



■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Clock input high voltage	V_{CH}	Driven by external clock oscillator	V_{CC}−0.4	V_{CC}+0.3	V
Clock input low voltage	V_{CL}	Driven by external clock oscillator	−0.3	0.45	V
Input high voltage	V_{IH}		2.0	V_{CC}+0.3	V
Input low voltage	V_{IL}		−0.3	0.8	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4		V
Output low voltage	V_{OL}	I_{OL}=+2.0mA		0.4	V
Input leakage current	$\lvert I_{IL} \rvert$	$0.4 \leqq V_{IN} \leqq 2.4V$		10	μA
Output leakage current	$\lvert I_{OL} \rvert$	$0.4 \leqq V_{OUT} \leqq 2.4V$		10	μA
Current consumption	I_{CC}			300	mA

The on-chip back-bias voltage oscillator takes approximately 20 ms to pump the back-bias voltage to −2.5V after the power has been turned on. The performance of the Z8010 Z-MMU is not guaranteed during this period.

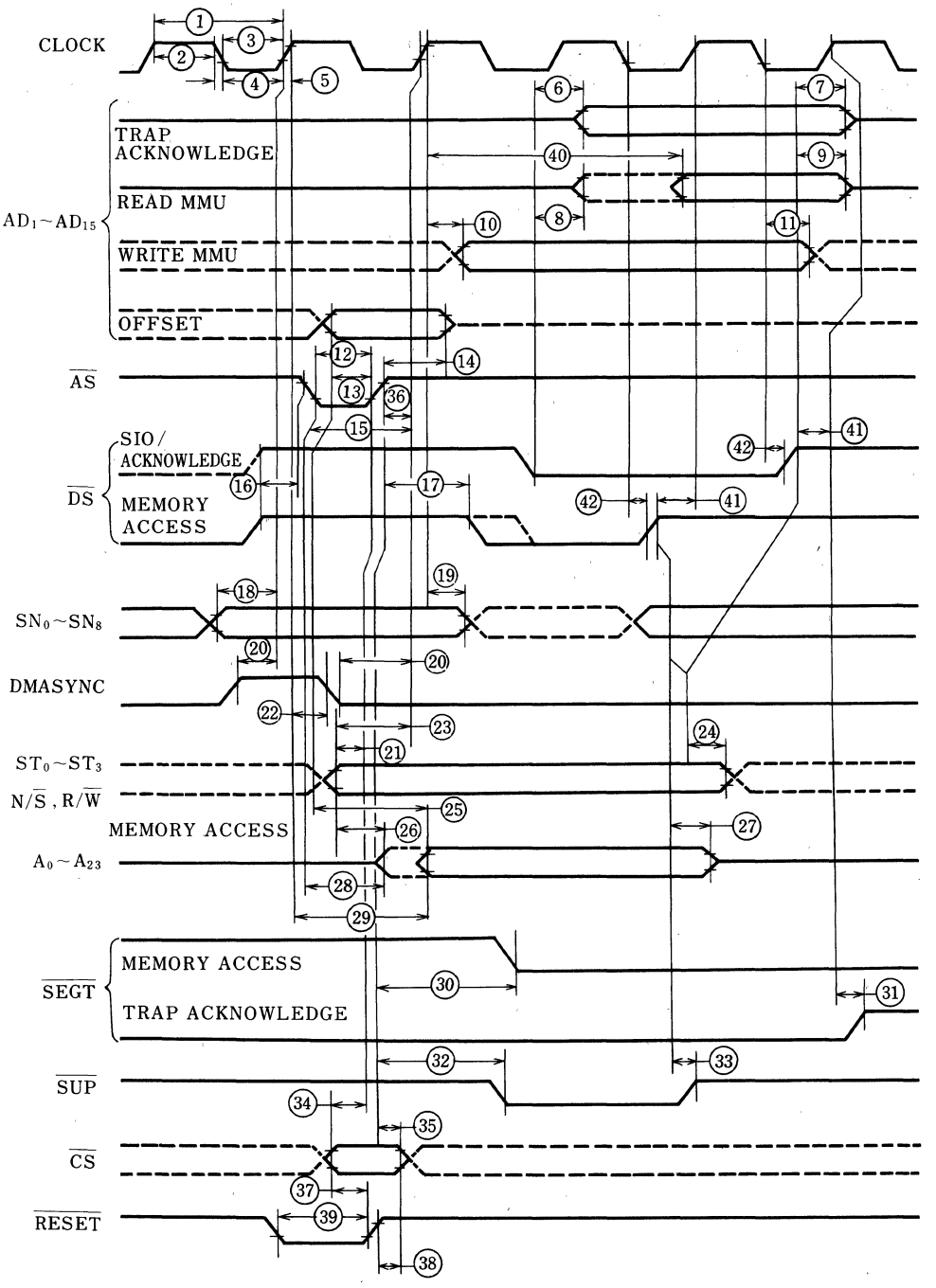
■ AC Characteristics

No.	Symbol	Parameter	LH8010		LH8010A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TcC	Clock cycle time	250		165		ns	
2	TwCh	Clock width (high)	105		70		ns	
3	TwCl	Clock width (low)	105		70		ns	
4	TfC	Clock fall time		20		10	ns	
5	TrC	Clock rise time		20		15	ns	
6	TdDSA (RDv)	$\overline{DS}$ ↓ (acknowledge) to read data valid delay		100		80	ns	1
7	TdDSA (RDf)	$\overline{DS}$ ↑ (acknowledge) to read data float delay		75		60	ns	
8	TdDSR (RDv)	$\overline{DS}$ ↓ (read) to AD output driven delay		100		80	ns	1
9	TdDSR (RDf)	$\overline{DS}$ ↑ (read) to read data float delay		75		60	ns	1
10	TdC (WDv)	CLK ↑ to write data valid delay		125		80	ns	
11	TdC (WDn)	CLK ↓ to write data not valid hold time	30		20		ns	
12	TwAS	Address strobe width	60		50		ns	
13	TsOFF (AS)	Offset valid to $\overline{AS}$ ↑ setup time	45		35		ns	
14	ThAS (OFFn)	$\overline{AS}$ ↑ to offset not valid hold time	60		40		ns	
15	TdAS (C)	$\overline{AS}$ ↓ to CLK ↑ delay	110		90		ns	
16	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay	50		30		ns	

No.	Symbol	Parameter	LH8010		LH8010A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
17	TdAS (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ delay	50		40		ns	
18	TsSN (C)	SN data valid to CLK ↑ setup time	100		40		ns	
19	ThC (SNn)	CLK ↑ to SN data not valid hold time	0		0		ns	
20	TdDMAS (C)	DMASYNC valid to CLK ↑ delay	120		80		ns	
21	TdSTNR (RS)	Status (ST_0-ST_3, N/$\overline{S}$, R/$\overline{W}$) valid to $\overline{AS}$ ↑ delay	50		30		ns	
22	Tdc (DMA)	CLK ↑ to DMASYNC ↓ delay	20		15		ns	
23	TdST (C)	Status (ST_0-ST_3) valid to CLK ↑ delay	100		60		ns	
24	TdDS (STn)	$\overline{DS}$ ↑ to status not valid delay	0		0		ns	
25	TdOFF (Av)	Offset valid to address output valid delay		175		90	ns	1
26	TdST (Ad)	Status valid to address output driven delay		155		75	ns	1
27	TdDS (Af)	$\overline{DS}$ ↑ to address output float delay		160		130	ns	1
28	TdAS (Ad)	$\overline{AS}$ ↓ to addres output driven delay		145		70	ns	1
29	TdC (Av)	CLK ↑ to address output valid delay		255		155	ns	1
30	TdAS (SEGT)	CLK ↑ to $\overline{SEGT}$ ↑ delay		160		100	ns	1, 2
31	TdC (SEGT)	$\overline{AS}$ ↑ to $\overline{SUP}$ ↓ delay		300		200	ns	1, 2
32	TdAS (SUP)	$\overline{DS}$ ↑ to $\overline{SUP}$ ↓ delay		150		90	ns	1, 2
33	TdDS (SUP)	Chip select input valid to $\overline{AS}$ ↑ setup time		155		100	ns	1, 2
34	TsCS (AS)	$\overline{AS}$ ↑ to chip select input not valid hold time	10		10		ns	
35	ThAS (CSn)	$\overline{AS}$ ↑ to CLK ↑ delay	60		40		ns	
36	TdAS (C)	$\overline{AS}$ ↑ to $\overline{SEGT}$ ↑ delay	0		0		ns	
37	TsCS (RST)	Chip select input valid to $\overline{RESET}$ ↑ setup time	150		100		ns	
38	ThRST (CSn)	$\overline{RESET}$ ↑ to chip select input not valid hold time	0		0		ns	
39	TwRST	$\overline{RESET}$ width (low)	2TcC		2TcC		ns	
40	TdC (RDv)	CLK ↑ to read data valid delay		460		300	ns	1
41	TdDS (C)	$\overline{DS}$ ↑ to CLK ↑ delay	30		20		ns	
42	TdC (DS)	CLK ↓ to $\overline{DS}$ ↑ delay	0		0		ns	

↑ Rising edge, ↓ Falling edge.
Note 1: 50pF Load
Note 2: 2.2kΩ Pull-up

■ Composite AC Timing Chart



■ MMU Register Organization

The MMU contains three types of registers : Segment Descriptor, Control and Status. A set of 64 Segment Descriptor Registers supplies the information needed to map logical memory addresses to physical memory locations. The segment number of a logical address determines which Segment Descriptor Register is used in address translation. Each Descriptor Register also contains the necessary information for checking that the segment location referenced is within the bounds of the segment and that the type of reference is permitted. It also indicates whether the segment has been read or written.

In addition to the Segment Descriptor Registers, the Z8010 MMU contains three 8-bit control registers for programming the device and six 8-bit status registers that record information in the event of an access violation.

(1) Segment Descriptor Registers

Each of the 64 Descriptor Registers contains a 16-bit base address field and an 8-bit attribute field (Fig. 1). The base address field is subdivided into high- and low-order bytes that are loaded one byte at a time when the descriptor is initialized. The limit field contains a value N that indicates N + 1 blocks of 256 bytes have been allocated to the segment.

The attribute field contains eight flags (Fig. 2). Five are related to protecting the segment against certain types of access, one indicates the special structure of the segment, and two encode the types of access that have been made to the segment. A flag is set when its value is 1. The following brief descriptions indicate how these flags are used.

	BASE ADDRESS FIELD		LIMIT FIELD	ATTRIBUTE FIELD
	15 8	7 0	7 0	
SDR0	BAH0	BAL0	L0	A0
SDR1	BAH1	BAL1	L1	A1
SDR2	BAH2	BAL2	L2	A2
⋮	⋮	⋮	⋮	⋮
SDR63	BAH63	BAL63	L63	A63

Fig. 1 Segment description registers

7							0
REF	CHG	DIRW	DMAI	EXC	CPUI	SYS	RD

Fig. 2 Attribute field in segment description registers

(i) **Read-Only (RD)** When this flag is set, the segment is read only and is protected against any write access.

(ii) **System-Only (SYS)** When this flag is set, the segment can be accessed only in System mode, and is protected against any access in Normal mode.

(iii) **CPU-Inhibit (CPUI)** When this flag is set, the segment is not accessible to the currently executing process, and is protected against any memory access by the CPU. The segment is, however, accessible under DMA.

(iv) **Execute-Only (EXC)** When this flag is set, the segment can be accessed only during an instruction fetch or access by the relative addressing mode cycle, and thus is protected against any access during other cycles.

(v) **DMA-Inhibit (DMAI)** When this flag is set, the segment can be accessed only by the CPU, and thus is protected against any access under DMA.

(vi) **Direction and Warning (DIRW)** When this flag is set, the segment memory locations are considered to be organized in descending order and each write to the segment is checked for access to the last 256-byte block. Such an access generates a trap to warn of potential segment overflow, but no Suppress signal is generated.

(vii) **Changed (CHG)** When this flag is set, the segment has been changed (written). This bit is set automatically during any write access to this segment if the write access does not cause any violation.

(viii) **Referenced (REF)** When this flag is set, the segment has been referenced (either read or written). This bit is set automatically during any access to the segment if the access does not cause a violation.

(2) Control Registers

The three user-accessible 8-bit control registers in the MMU direct the functioning of the MMU (Fig. 3).The Mode Register provides a sophisticated method for selectively enabling MMUs in multiple-MMU configurations. The Segment Address Register (SAR) selects a particular Segment Descriptior Register to be accessed during a control operation. The Descriptor Selection Counter Register points to a byte within the Segment Descriptor Register to be accessed during a control operation.

The Mode Register contains a 3-bit identification field (ID) that distinguishes among eight enabled MMUs in a multiple-MMU configuration. This field is used during the segment trap acknowledge sequence (refer to the section on Segment Trap and Acknowledge). In addition, the Mode Register contains five flags.

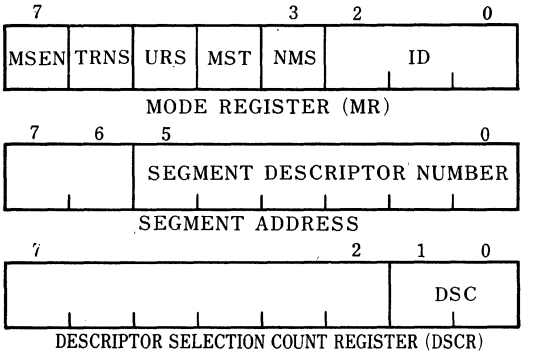


Fig. 3 Countrol registers

(i) **Multiple Segment Table (MST)** This flag indicates whether multiple segment tables are present in the hardware configuration. When this flag is set, more than one table is present and the N/$\overline{S}$ line must be used to determine whether the MMU contains the appropriate table.

(ii) **Normal Mode Select (NMS)** This flag indicates whether the MMU is to translate addresses when the N/$\overline{S}$ line is High or Low. If the MST flag is set, the N/$\overline{S}$ line must match the NMS flag for the MMU to translate segment addresses, otherwise the NMU Address lines remain 3-stated.

(iii) **Upper Range Select (URS)** This flag is used to indicate whether the MMU contains the lower-numbered segment descriptors or the higher-numbered segment descriptors. The most significant bit of the segment number must match the URS flag for the MMU to translate segment addresses, otherwise the MMU Address lines remain 3-stated.

(iv) **Translate (TRNS)** This flag indicates whether the MMU is to translate logical program addresses to physical memory locations or is to pass the logical addresses unchanged to the memory and without protection checking. In the non-translation mode, the most significant byte of the output is the 7-bit segment number and the most significant bit is 0.

When this flag is set, the MMU performs address translation and attribute checking.

(v) **Master Enable (MSEN)** This flag enables or disables the MMU from performing its address translation and memory protection functions. When this flag is set, the MMU performs these tasks ; when the flag is clear the Address lines of the MMU remain 3-stated.

The Segment Address Register (SAR) points to one of the 64 segment descriptors. Control commands to the MMU that access segment descriptors implicitly use this pointer to select one of the descriptors. This register has an auto-incrementing capability so that multiple descriptors can be accessed in a block read/write fashion.

The Descriptor Selection Counter Register holds a 2-bit counter that indicates which byte in the descriptor is being accessed during the reading or writing operation. A value of zero in this counter indicates the high-order byte of the base address field is to be accessed, one indicates the low-order byte of the base address, two indicates the limit field and three indicates the attribute field.

(3) Status Registers

Six 8-bit registers contain information useful in recovering from memory access violations (Fig. 4). The Violation Type Register describes the conditions that generated the trap. The Violation Segment Number and Violation Offset Registers record the most-significant 15 bits of the logical address that causes a trap. The Instruction Segment Number and Offset Registers record the most-significant 15 bits of the logical address of the last instruction fetched before the first accessing violation. These two registers can be used in conjunction with external circuitry that records the low-order offset byte. At the time of the addressing violation, the Bus Cycle Status Register records the bus cycle status (status code, read/write mode and normal/system mode).

The MMU generates a Trap Request for two general reasons : either it detects an access violation, such as an attempt to write into a read-only segment, or it detects a warning condition, which is a write into the lowest 256 bytes of a segment with the DIRW flag set. When a violation or warning condition is detected, the MMU generates a Trap Request and automatically sets the appropriate flags. The eight flags in the Violation Type Register describe the cause of a trap.

Read-Only Violation (RDV) Set when the CPU attempts to access a read-only segment and the R/$\overline{W}$ line is Low.

System Violation (SYSV) Set when the CPU accesses a system-only segment and the $\overline{N}$/S line is High.

CPU-Inhibit Violation (CPUIV) Set when the CPU attempts to access a segment with the CPU-inhibit flag set.

Execute-Only Violation (EXCV) Set when the CPU attempts to access an excute-only segment in other than an instruction fetch or load relative instructions cycle.

Segment Length Violation (SLV) Set when an offset falls outside of the legal range of a segment.

Primary Write Warning (PWW) Set when an access is made to the lowest 256 bytes of a segment with the DIRW flag set.

Secondary Write Warning (SWW) Set when the CPU pushes data into the last 256 bytes of the system stack and EXCV, CPUIV, SLV, SYSV, RDV or PWW is set. Once this flag is set, subsequent write warnings for accessing the system stack do not generate a Segment Trap request.

Fatal Condition (FATL) Set when any other flag in the Violation Type Register is set and either a violation is detected or a write warning condition occurs in Normal mode. This flag is not set during a stack push in System mode that results in a warning condition. This flag indicates a memory access error has occurred in the trap processing routine. Once set, no Trap Request signals are generated on subsequent violations. However, Suppress signals are generated on this and subsequent CPU violations until the FATL flag has been reset.

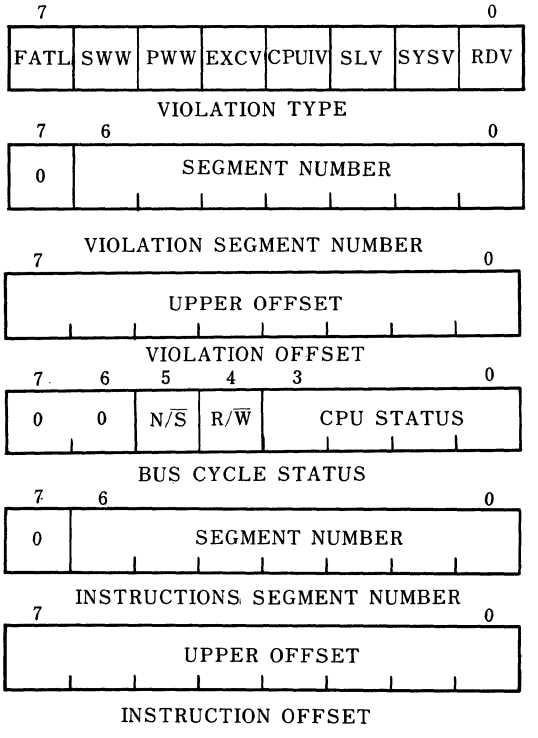


Fig. 4 Status registers

■ Memory Protection

Each memory segment is assigned several attributes that are used to provide memory access protection. A memory request from the Z8001CPU is accompanied by status information that indicates the attributes of the memory request. The MMU compares the memory request attributes with segment attributes and generates a Trap Request whenever it detects an attribute violation. Trap Request informs the Z8001 CPU and the system control program of the violation so that appropriate action can be taken to recover. The MMU also generates the Suppress signal $\overline{SUP}$ in the event of an access violation. Suppress can be used by a memory system to inhibit stores into the memory and thus protect the contents of the memory from erroneous changes.

Five attributes can be associated with each segment. When an attempted access violates any one of the attributes associated with a segment, a Trap Request and a Suppress signal are generated by the MMU. These attributes are read only, execute only, system access only, inhibit CPU accesses and inhibit DMA accesses.

Segments are specified by a base address and a range of legal offsets to this base address. On each access to a segment, the offset is checked against this range to insure that the access falls within the allowed range. If an access that lies outside the segment is attempted, Trap Request and Suppress are generated.

Normally the legal range of offsets within a segment is form 0 to 256N + 255 bytes, where $0 \leqq N \leqq 255$. However, a segment may be specified so that legal offsets range from 256N to 65,535 bytes, where $0 \leqq N \leqq 255$. The later type of segment is useful for stacks since the Z8000 stack manipulation instructions cause stacks to grow towerd lower memory locations. Thus when a stack grows to the limit of its allocated segment, additional memory can be allocated on the correct end of the segment. As an aid in maintaining stacks, the MMU detects when a write is performed to the lowest allocated 256 bytes of these segments and generates a Trap Request. No Suppress signal is generated so the write is allowed to proceed. This write warning can then be used to indicate that more memory should be allocated to the segment.

■ Segmented Addressing

The 8M bytes Z8001 addressing spaces are divided into 128 relocatable segments of up to 64K bytes each. A 23-bit segmented address uses a 7-bit segment address to point to the segment, and a 16-bit offset to address any byte relative to the beginning of the segment. The two parts of the segmented address may be manipulated separately.

The MMU divides the physical memory into 256-byte blocks. Segments consist of physically contiguous blocks. Certain segments may be designated so that writes into the last block generate a warning trap. If such a segment is used as a stack, this warning can be used to increase the segment size and prevent a stack overflow error.

The addresses manipulated by the programmer, used by instructions and output by the Z8001 are called logical addresses. The MMU takes the logical addresses and transforms them into the physical addresses required for accessing the memory (Fig. 4). This address transformation process is called relocation.

The relocation process is transparent to user software. A translation table in the MMU associates the 7-bit segment number with the base address of the physical memory segment. The 16-bit logical address offset is added to the physical base address to obtain the actual physical memory location. Because a base address always has a low byte equal to zero,

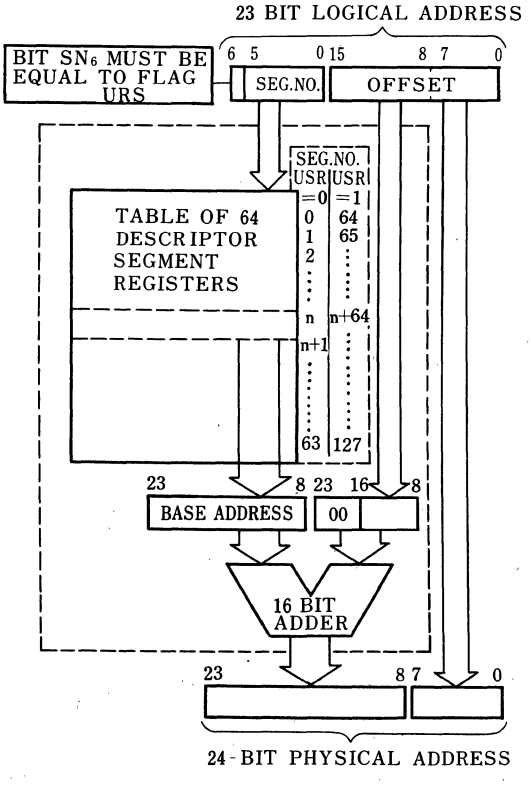


Fig. 5 Logical-to-physical address translation

■ Segment Trap and Acknowledge

The Z8010 MMU generates a Segment Trap when it detects an access violation or a write warning condition. In the case of an access violation, the MMU also activates Suppress, which can be used to inhibit memory writes and to flag special data to be returned on a read access. Segment Trap remains Low until a Trap Acknowlege signal is received. If a CPU-generated violation occurs, Suppress is asserted for that cycle and all subsequent CPU instruction execution cycles until the end of the instruction. Intervening DMA cycles are not suppressed, however, unless they generate a violation. Violations detected during DMA cycles cause Suppress to be asserted during that cycle only-no Segment Trap Requests are ever generated during DMA cycles.

Segment traps to the Z8001 CPU are handled similarly to other types of interrupts. To service a segment trap, the CPU issues a segment trap acknowledge cycle. The acknowledge cycle is always preceded by an instruction fetch cycle that is ignored (the MMU has been designed so that this dummy cycle is ignored). During the acknowledge cycle all enabled MMUs use the Address/Data lines to indicate their status. An MMU that has generated a Segment Trap Request outputs a 1 on the A/D line associated with the number in its ID field ; an MMU that has not generated a segment trap request outputs a 0 on its associated A/D line. A/D lines for which no MMU is associated remain 3-stated.

Note : The ID field is used with multiple MMUs. In the multiple organization one of the 8 ENABLE-state MMUs can be detected. During a segment trap acknowledge cycle, an MMU outputs a 1 on the A/D line associated with this bit, and a 0 on the other associated A/D line. If two or more violations occur while an instruction is being executed, the CPU uses the data (high-order byte) on this A/D line as the distinguishing information, enabling an MMU analysis in the segment trap handling routine.

Following the acknowlege cycle the CPU automatically pushes the Program Status onto the system stack and loads another Program Status from the Program Status Area. The Segment Trap line is reset during the segment trap acknowledge cycle. Suppress is not generated during the stack push. If the store creates a write warning condition, a Segment Trap Request is generated and is serviced at

the end of the Program Status swap. The SWW flag is also set. Servicing this second Segment Trap Request also creates a write warning condition, but because the SWW flag is set, no Segment Trap Request is generated. If a violation rather than a write warning occurs during the Program Status swap, the FATL flag is set rather than the SWW flag. Subsequent violations cause Suppress to be asserted but not Segment Trap Request. Without the SWW and FATL flags, trap processing routines that generate memory violations would repeatedly be interrupted and called to process the trap they created.

The CPU routine to process a trap request should first check the FATL flag to determine if a fatal system error has occurred. If not, the SWW flag should be checked to determine if more memory is required for the system stack. Finally, the trap itself should be processed and the Violation Type Register reset.

■ MMU Commands

Table 1 Segment descriptor register commands

Code (Hex)	Instruction
08	Read/write base field
09	Read/write limit field
0A	Read/write attribute field
0B	Read/write descriptor (all fields)
0C	Read/write base field ; Increment SAR
0D	Read/write limit field ; Increment SAR
0E	Read/write attribute field ; Increment SAR
0F	Read/write descriptor ; Increment SAR
15	Set All CPU-inhibit attribute flags
16	Set All DMAI-inhibit attribute flags

Three commands are used to read and write the control registers.

Table 2 Control register commands

Code (Hex)	Instruction
00	Read/write mode register
01	Read/write segment address register
20	Read/write descriptor selector counter register

The Status Registers are read-only registers, although the Violation Type Register (VTR) can be reset. Nine instructions access these registers.

Table 3 Status register commands

Code (Hex)	Instruction
02	Read violation type register
03	Read violation segment number register
04	Read violation offset (high-byte) register
05	Read bus status register
06	Read instruction segment number register
07	Read instruction offset (high-byte) register
11	Reset violation type register
13	Reset SWW flag in VTR
14	Reset FATL flag in VTR

LH8030/LH8030A Z8030/Z8030A Serial Communications Controller

■ Description

The Z8030 Z-SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with the Zilog Z-Bus. The Z-SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The Z-SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, Digital Phase-Locked Loops, and crystal oscillators that dramatically reduce the need for external logic.

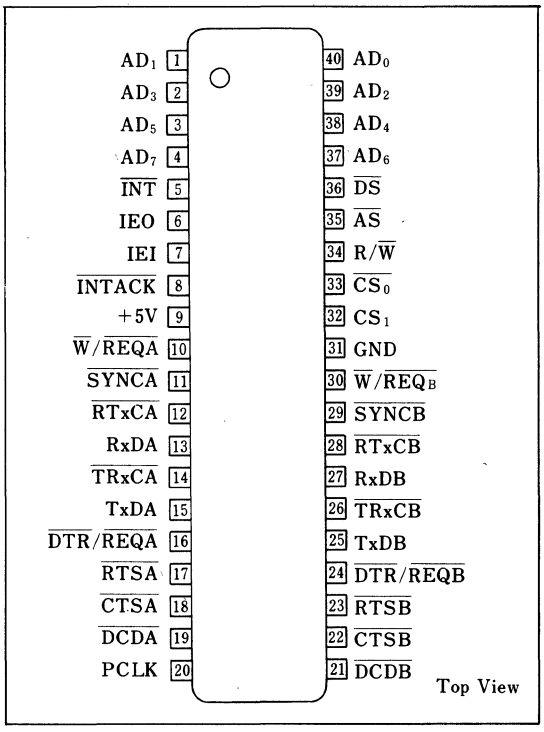
The Z-SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and Synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.).

The device can generate and check CRC codes in any Synchronous mode and can be programmed to check data integrity in various modes. The Z-SCC also has facilities for modem controls in both channels. In applications where these controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The Z-Bus daisy-chain interrupt hierarchy is also supported as is standard for Zilog peripheral components.

The LH8030A Z8030A SCC is the high speed version which can operate at 6MHz system clock.

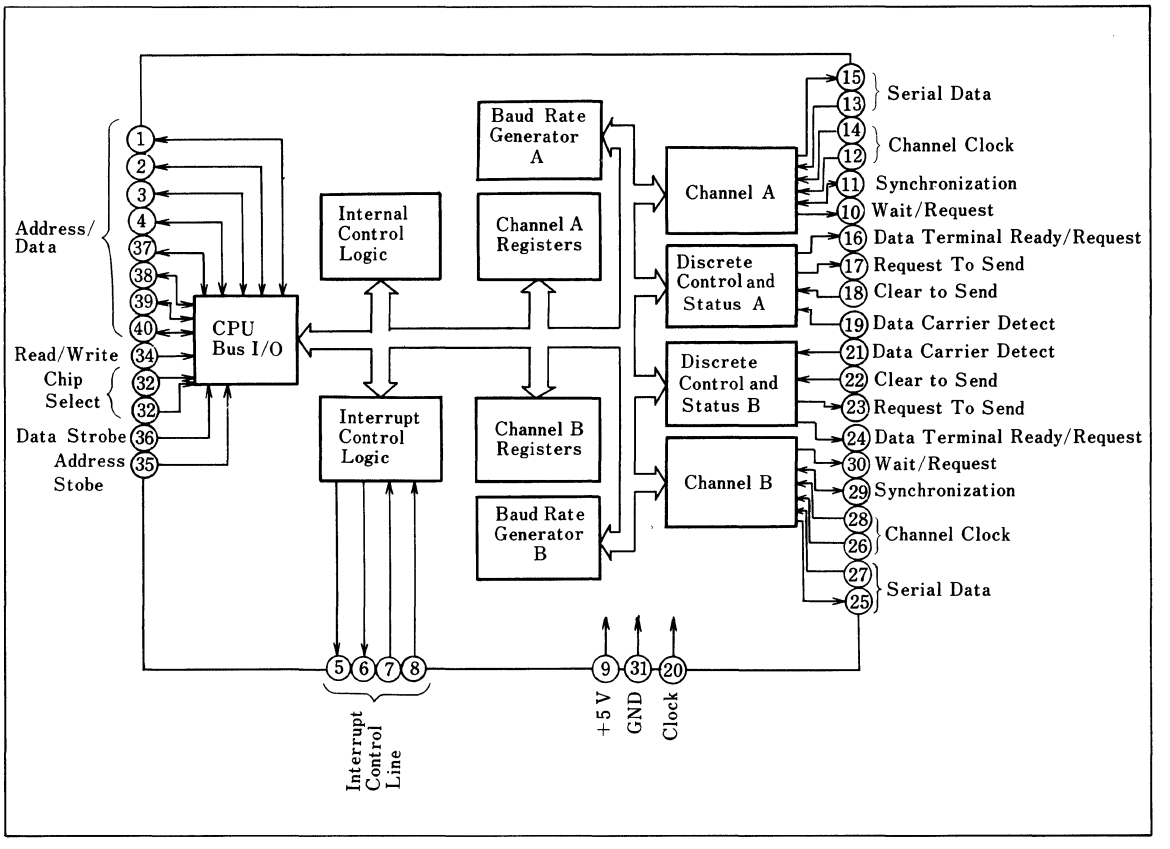
■ Pin Connections



■ Features

1. Two independent, 0 to 1M bit/second, full-duplex channels, each with a separate crystal oscillator, baud rate generator, and Digital Phase-Locked Loop for clock recovery.
2. Multi-protocol operation under program control ; programmable for NRZ, NRZI, or FM data encoding.
3. Asynchronous mode with five to eight bits and one, one and one-half, or two stop bits per character ; programmable clock factor ; break detection and generation ; parity, overrun, and framing error detection
4. Synchronous mode with internal or external character synchronization on one or two synchronous characters and CRC generation and checking with CRC-16 or CRC-CCITT preset to either 1s or 0s.
5. SDLC/HDLC mode with comprehensive frame-level control, automatic zero insertion and delection, I-field residue handing, abort generation and detection, CRC generation and checking, and SDLC Loop mode operation.
6. Local Loopback and Auto Echo modes.

■ Block Diagram



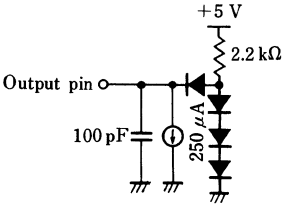
Pin Description

Pin	Meaning	I/O	Function
$AD_0 \sim AD_7$	Address/data bus	Bidirectional 3-state	Multiplexed system address/data bus.
$\overline{AS}$	Address strobe	I	Active "Low". Addresses are valid.
$\overline{DS}$	Data strobe	I	Active "Low". Data are valid.
R/$\overline{W}$	Read/write	I	Read at "High", Write at "Low".
$\overline{CS_0}$	Chip select 0	I	Active "Low". Selects an MMU for a control command.
CS_1	Chip select 1	I	Active "High". Selects an MMU for a control command.
$\overline{INT}$	Interrupt request	O	Active "Low". Requests an interrupt.
$\overline{INTACK}$	Interrupt acknowledge	I	Active "Low". Indicates an active interrupt acknowledge cycle.
IEI	Interrupt enable input	I	Active "High". Forms an interrupt daisy chain to give an interrupt priority.
IEO	Interrupt enable output	O	Active "High". Forms an interrupt daisy chain to give an interrupt priority.
$\overline{W}$/$\overline{REQA}$ $\overline{W}$/$\overline{REQB}$	Wait/request	Open drain	Active "Low". Programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU.
$\overline{CTSA}$ $\overline{STSB}$	Clear to send	I	Active "Low". Enables the respective transmitters to send signals. Can be used as general-purpose input pins.
$\overline{RTSA}$ $\overline{RTSB}$	Request to send	O	Active "Low". Goes High after the transmitter is empty. Can be used as general-purpose output pins.
TxDA, TxDB	Transmit data	I	Transmits data.
$\overline{DCDA}$ $\overline{DCDB}$	Data carrier detect	I	Active "Low". Enables the receiver to receive signals. Can be used as general-purpose input pins.
$\overline{RxDA}$, $\overline{RxDB}$	Receive data	I	Receives data.
$\overline{RTxCA}$, $\overline{RTxCB}$	Recive/transmit clocks	I	Transmission-purpose clocks.
$\overline{TRxCA}$, $\overline{TRxCB}$	Transmit/receive clocks	I/O	Transmission-purpose clocks.
$\overline{DTR}$/$\overline{REQA}$ $\overline{DTR}$/$\overline{REQB}$	Data terminal Ready/request	O	Active "Low". Request lines for a DMA controller. Can be used as general-purpose output pins.
$\overline{SYNCA}$ $\overline{SYNCB}$	Synchronization	I/O	Active "Low". Indicates a synchronization mode. Switches synchronization mode. Switches to input or output depending on modes.
PCLK	Clock	I	Single-phase clock. Not required tobe the same as for the CPU.

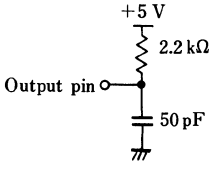
Note : When AS and DS are at "Low" at the same time, the Z-SCC resets.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7.0	V
Output voltage	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃



Standard test load



Open drain test load

DC Characteristics

(V_{CC}=5V±5%, Ta=0~+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input high voltage	V_{IH}		2.0	V_{CC}+0.3	V
Input low voltage	V_{IL}		−0.3	0.8	V
Output high voltage	V_{OH}	I_{OH}=−250μA	2.4		V
Output low voltage	V_{OL}	I_{OL}=+2.0mA		0.4	V
Input leakage current	$\lvert I_{IL} \rvert$	0.4≦V_{IN}≦2.4V		10.0	μA
Output leakage current	$\lvert I_{OL} \rvert$	0.4≦V_{OUT}≦2.4V		10.0	μA
Supply current	I_{CC}			250	mA

Capacitance

(f=1MHz, Ta=0~+70℃)

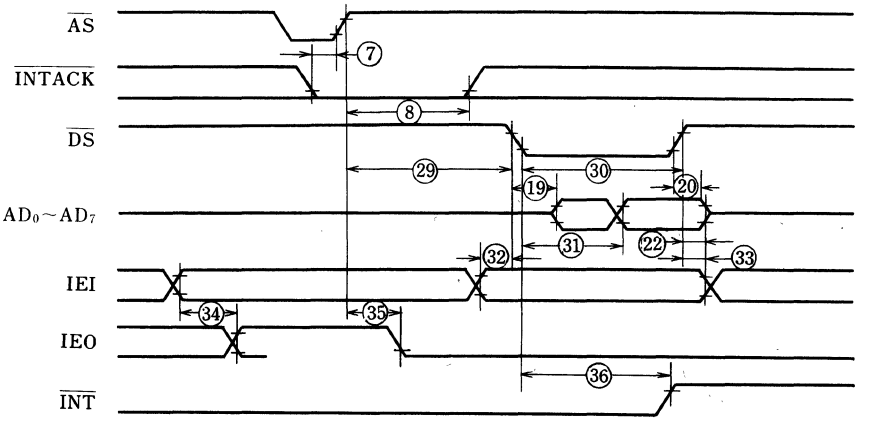
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_{IN}	Unmeasured pins returned to ground		10	pF
Output capacitance	C_{OUT}			15	pF
Bidirectional capacitance	$C_{I/O}$			20	pF

AC Characteristics

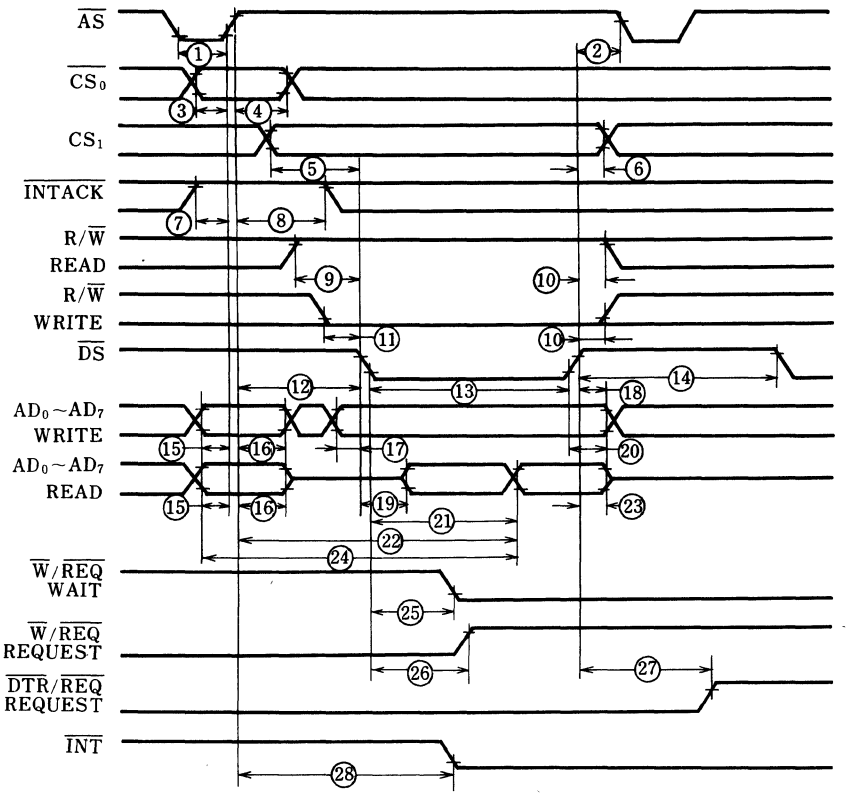
No.	Symbol	Parameter	LH8030		LH8030A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TwAS	AS low width	70		50		ns	
2	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay time	50		25		ns	
3	$TsCS_0$ (AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ setup time	0		0		ns	1
4	$ThCS_0$ (AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ hold time	60		40		ns	1
5	$TsCS_1$ (DS)	CS_1 to $\overline{DS}$ ↓ setup time	100		80		ns	1
6	$ThCS_1$ (DS)	CS_1 to $\overline{DS}$ ↑ hold time	55		40		ns	1
7	TsIA (AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ setup time	0		0		ns	
8	ThIA (AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ hold time	250		250		ns	
9	TsRWR (DS)	R/$\overline{W}$ (read) to $\overline{DS}$ ↓ setup time	100		80		ns	
10	ThRW (DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ hold time	55		40		ns	
11	TsRWW (DS)	R/$\overline{W}$ (write) to $\overline{DS}$ ↓ setup time	0		0		ns	
12	TdAS (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ delay time	60		40		ns	
13	$TwDS_1$	$\overline{DS}$ low width	390		250		ns	
14	TrC	Valid access recovery time	6TcPC+200		6TcPC+130		ns	2
15	TsA (AS)	Address to $\overline{AS}$ ↑ setup time	30		10		ns	1
16	ThA (AS)	Address to $\overline{AS}$ ↑ hold time	50		30		ns	1
17	TsDW (DS)	Write data to $\overline{DS}$ ↓ setup time	30		20		ns	
18	ThDW (DS)	Write data to $\overline{DS}$ ↑ hold time	30		20		ns	
19	TdDS (DA)	$\overline{DS}$ ↓ to data active delay time	0		0		ns	
20	TdDSr (DR)	$\overline{DS}$ ↑ to read data not valid delay	0		0		ns	
21	TdDSf (DR)	$\overline{DS}$ ↓ to read data valid delay time		250		180	ns	
22	TdAS (DR)	$\overline{AS}$ ↑ to read data valid delay time		520		335	ns	
23	TdDS (DRz)	$\overline{DS}$ ↑ to read data float delay time		70		45	ns	3
24	TdA (DR)	Address required valid to read data valid delay		570		420	ns	
25	TdDS (W)	$\overline{DS}$ ↓ to wait valid delay		240		200	ns	4
26	TdDSf (REQ)	$\overline{DS}$ ↓ to W/$\overline{REQ}$ not valid delay		240		200	ns	
27	TdDSr (REQ)	$\overline{DS}$ ↑ to DTR/$\overline{REQ}$ not valid delay		5TcPC+300		5TcPC+250	ns	

No.	Symbol	Parameter	LH8030		LH8030A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
28	TdAS (INT)	$\overline{AS}$ ↑ to $\overline{INT}$ valid delay		500		500	ns	4
29	TdAS (DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (acknowledge) delay					ns	5
30	TwDSA	$\overline{DS}$ (acknowledge) low width	390		250		ns	
31	TdDSA (DR)	$\overline{DS}$ ↓ (acknowledge) to read data valid delay		250		180	ns	
32	TsIEI (DSA)	IEI to $\overline{DS}$ ↓ (acknowledge) setup time	120		100		ns	
33	ThIEI (DSA)	IEI to $\overline{DS}$ ↑ (acknowledge) hold time	0		0		ns	
34	TdIEI (IEO)	IEI to IEO delay		120		100	ns	
35	TdAS (IEO)	$\overline{AS}$ ↑ to IEO delay		250		250	ns	6
36	TdDSA (INT)	$\overline{DS}$ ↓ (acknowledge) to $\overline{INT}$ inactive delay		500		500	ns	4
37	TdDS (ASQ)	$\overline{DS}$ ↑ to AS ↓ delay for no reset	30		15		ns	
38	TdASQ (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ delay for no reset	30		30		ns	
39	TwRES	$\overline{AS}$ and $\overline{DS}$ coincident low for reset	250		250		ns	
40	TwPCI	PCLK low width	105	2000	70	1000	ns	
41	TwPCh	PCLK high width	105	2000	70	1000	ns	
42	TcPC	PCLK cycle time	250	4000	165	2000	ns	
43	TrPC	PCLK rise time		20		15	ns	
44	TfPC	PCLK fall time		20		10	ns	

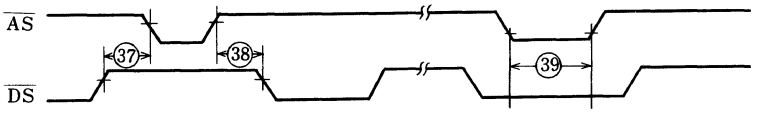
Note : ↑ Rising edge, ↓ falling edge.
Note 1: Parameter does not apply to interrupt acknowledge transactions.
Note 2: Parameter applies only between transactions involving the Z-SCC.
Note 3: Float delay is defined as the time required for a ±0.5 V change in the output with a maximum dc load and minimum ac load.
Note 4: Open-drain output, measured with open-drain test load.
Note 5: Parameter is system dependent. For any Z-SCC in the daisy chain, TdAS (DSA) must be greater than the sum of TdAS (IEO) for the highest priority device in the daisy chain, TsIEI (DSA) for the Z-SCC, and TdIEIf (IEO) for each device separating them in the daisy chain.
Note 6: Parameter applies only to a Z-SCC pulling $\overline{INT}$ Low at the beginning of the Interrupt Acknowledge transaction.



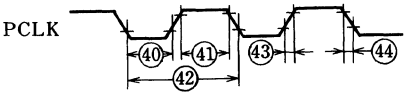
Interrupt acknowledge timing



Read and write timing



Reset timing

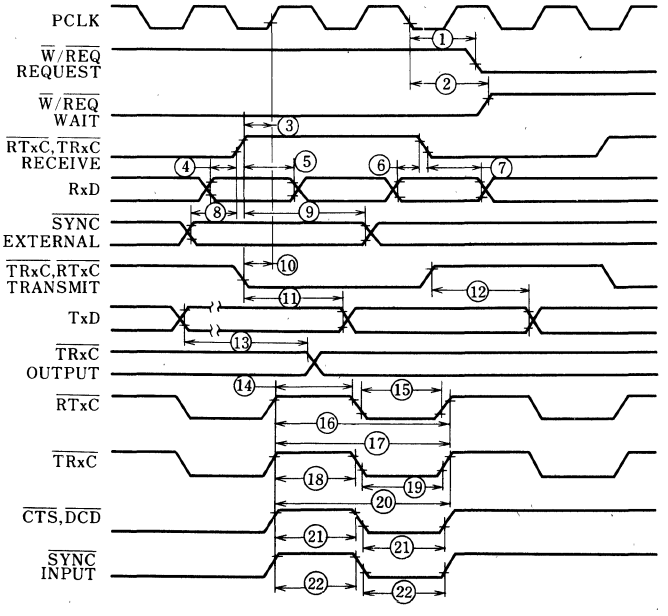


Cycle timing

■ General Timing

No.	Symbol	Parameter	LH8030		LH8030A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TdPC (REQ)	PCLK ↓ to W/REQ valid delay		250		250	ns	
2	TdPC (W)	PCLK ↓ to wait inactive delay		350		350	ns	
3	TsRXC (PC)	RXC ↑ to PCLK ↑ setup time	50		50		ns	1, 4
4	TsRXD (RXCr)	RXD to RXC ↑ setup time (×1 mode)	0		0		ns	1
5	ThRXD (RXCr)	RXD to RXC ↑ hold time (×1 mode)	150		150		ns	1
6	TsRXD (RXCf)	RXD to RXC ↓ setup time (×1 mode)	0		0		ns	1, 5
7	ThRXD (RXCf)	RXD to RXC ↓ hold time (×1 mode)	150		150		ns	1, 5
8	TsSY (RXC)	SYNC to RXC ↑ setup time	−200		−200		ns	1
9	ThSY (RXC)	SYNC to RXC ↑ hold time	3TcPC+200		3TcPC+200		ns	1
10	TsTXC (PC)	TXC ↓ to PCLK ↑ setup time	0		0		ns	2, 4
11	TdTXCf (TXD)	TXC ↓ to TXD delay (×1 mode)		300		300	ns	2
12	TdTXCr (TXD)	TXC ↑ to TXD delay (×1 mode)		300		300	ns	2, 5
13	TdTXD (TRX)	TXD to TRDC delay (send clock echo)					ns	
14	TwRTXh	RTXC high width	180		180		ns	
15	TwRTXl	RTXC low width	180		180		ns	
16	TcRTX	RTXC cycle time	400		400		ns	
17	TcRTXX	Crystal oscillator period	250	1000	250	1000	ns	3
18	TwTRXh	TRXC high width	180		180		ns	
19	TwTRXl	TRXC low width	180		180		ns	
20	TcTRX	TRXC cycle time	400		400		ns	
21	TwEXT	DCD or CTS pulse width	200		200		ns	
22	TwSY	SYNC pulse width	200				ns	

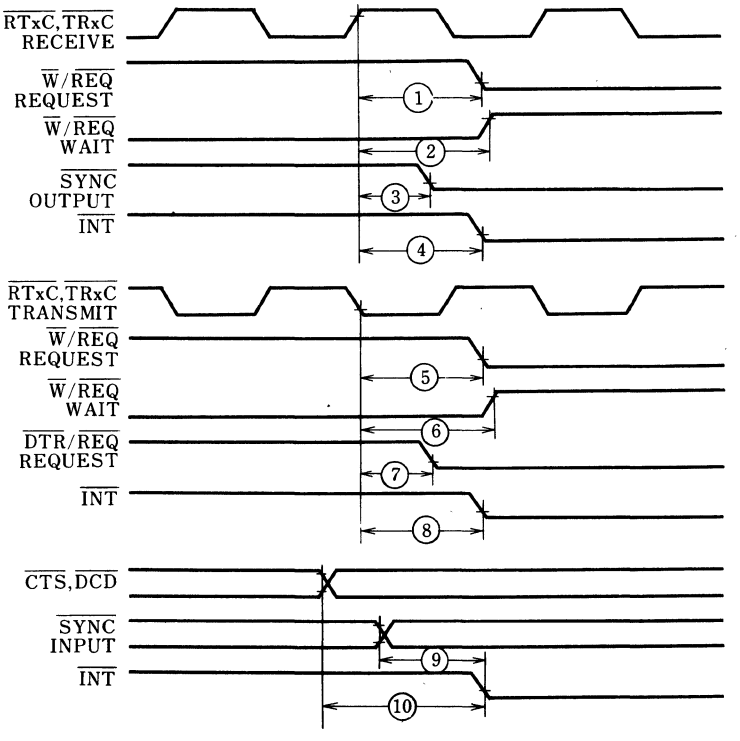
Note : ↑ Rising edge, ↓ Falling edge.
Note 1: RxC is RTxC or TRxC, whichever is supplying the receive clock.
Note 2: TxC is TRxC or RTxC, whichever is supplying the transmit clock.
Note 3: Both RTxC and SYNC have 30 pf capacitors to the ground connected to them.
Note 4: Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
Note 5: Parameter applies only to FM encoding/decoding



System Timing

No.	Symbol	Parameter	LH8030 MIN.	LH8030 MAX.	LH8030A MIN.	LH8030A MAX.	Unit	Note
1	TdRXC (REQ)	$\overline{RxC}$ ↑ to $\overline{W/REQ}$ valid delay	8	12	8	12	TcPC	2
2	TdRXC (W)	$\overline{RxC}$ ↑ to wait inactive delay	8	12	8	12	TcPC	1,2
3	TdRXC (SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ valid delay	4	7	4	7	TcPC	2
4	TdRXC (INT)	$\overline{RxC}$ ↑ $\overline{INT}$ valid delay	8 +2	12 +3	8 +2	12 +3	TcPC $\overline{AS}$ ↑	1,2
5	TdTXC (REQ)	$\overline{TxC}$ ↓ to $\overline{W/REQ}$ valid delay	5	8	5	8	TcPC	3
6	TdTXC (W)	$\overline{TxC}$ ↓ to wait inactive delay	4	8	5	8	TcPC	1,3
7	TdTXC (DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ valid delay	4	7	4	7	TcPC	3
8	TdTXC (INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ valid delay	4 +2	6 +3	4 +2	6 +3	TcPC $\overline{AS}$ ↑	1,3
9	TdSY (INT)	$\overline{SYNC}$ transition to $\overline{INT}$ valid delay	2	3	2	3	$\overline{AS}$ ↑	1
10	TdEXT (INT)	$\overline{DCD}$ or $\overline{CTS}$ transition to $\overline{INT}$ valid delay	2	3	2	3	$\overline{AS}$ ↑	1

Note : ↑ Rising edge, ↓ Falling edge.
Note 1: Open-drain output measured with open-drain test load.
Note 2: $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
Note 3: $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$ whichever is supplying the transmit clock.



■ Data Communications Capabilites

The Z-SCC provides two independent full-duplex channels programmable for use in any common Asynchoronous or Synchronous datacommunication protocol. Fig. 1 illustrates these protocols.

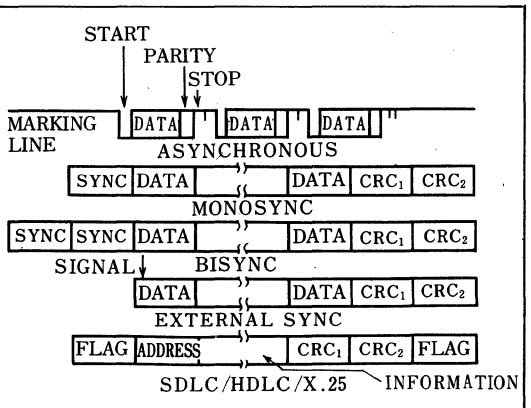


Fig. 1 Some Z-SCC protocols

■ SDLC Loop Mode

The Z-SCC supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow on the loop and any number of secondary stations. In SDLC Loop mode, the Z-SCC performs the functions of a secondary station while a Z-SCC operating in regular SDLC mode can act as a controller (Fig. 2).

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop, and in fact must pass these messages to the rest of the loop by retransmitting them with a one-bit-time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an EOP (End Of Poll), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it chages the last binary 1 of the EOP to a 0 before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit can then append thier messages to the message of the first secondary station by the same process. Any secondary stations without messages to send merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP).

SDLC Loop mode is a programmable option in the Z-SCC. NRZ, NRZI, and FM coding may all be used SDLC Loop mode.

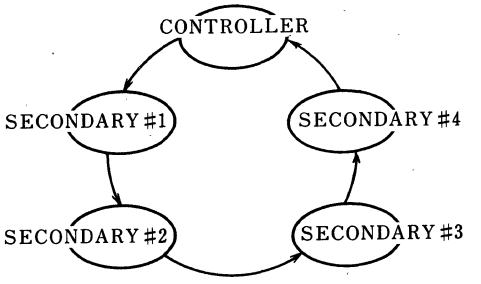


Fig. 2 An SDLC loop

■ Data Encoding

The Z-SCC may be programmed to encode and decode the serial data in four different ways (Fig. 3). In NRZ encoding, a 1 is represented by a High level and a 0 is represented by a Low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level. In FM1 (more properly, bi-phase mark) a transition occurs at the beginning of every bit cell. A 1 is represented by an additional translation at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. FM0 (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the Z-SCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0, the bit is a 1.

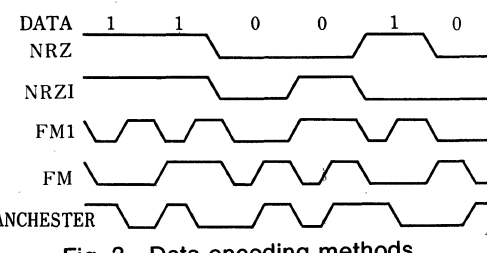


Fig. 3 Data encoding methods

■ Auto Echo and Local Loopback

The Z-SCC is capable of automatically echoing everything it receives. This feature is useful mainly in Asynchronous modes, but works in Synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the $\overline{\text{CTS}}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and $\overline{\text{WAIT/REQUEST}}$ on transmit.

The Z-SCC is also capable of Local Loopback . In this mode TxD is RxD, just as in Auto Echo mode. However, in Local Loopback mode, the internal data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in Asynchronous, Synchronous and SDLC modes with NRZ, NRZI or FM coding of the data stream.

■ Baud Rate Generator

Each channel in the Z-SCC contains a programmable band rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching 0, the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the recieve clock, or both. It can also drive the Digital Phase-Locked Loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{\text{TRxC}}$ pin, the output of the baud rate generator may be echoed out via the $\overline{\text{TRxC}}$ pin.

The following formula relates the time constant to the baud rate (the baud rate is in bits/second and the BR clock period is in seconds) :

$$\text{baud rate} = \frac{1}{2\,(\text{time constant} + 2) \times (\text{BR clock period})}$$

■ Digital Phase-Locked Loop

The Z-SCC contains a Digital Phase-Locked Loop (DPLL) to recover clock information from a data stream with NRZI or FM encodling. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the Z-SCC receive clock, the transmit clock, or both.

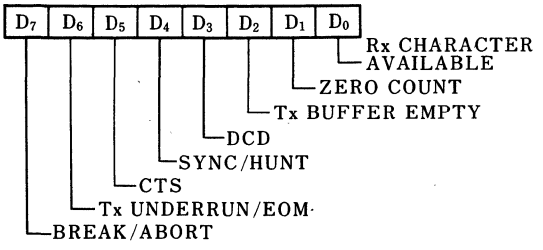
For NRZI encoding, the DPLL counts the 32x clock to create nominal bit times. As the 32x clock is counted, the DPLL is searching the incoming data stream for edges (either 1 to 0 or 0 to 1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15 to 16 counting transition.

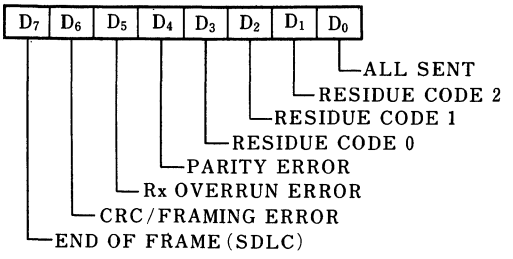
The 32x clock for the DPLL can be programmed to come from either the $\overline{\text{RTxC}}$ input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the Z-SCC via the $\overline{\text{TRxC}}$ pin (if this pin is not being used as an input).

■ Read Registers

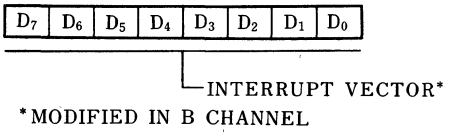
- **Read Register 0**



- **Read Register 1**

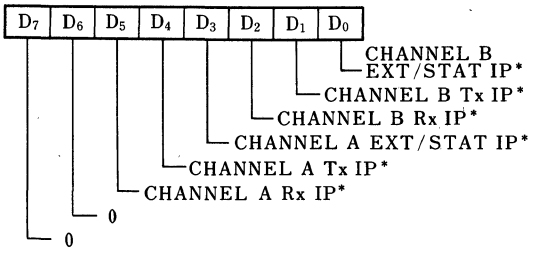


- **Read Register 2**



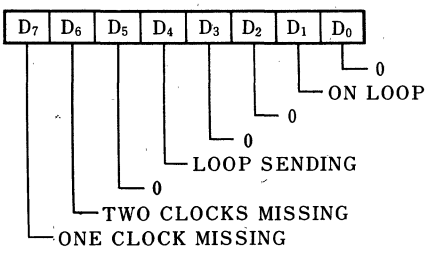
*MODIFIED IN B CHANNEL

- **Read Register 3***

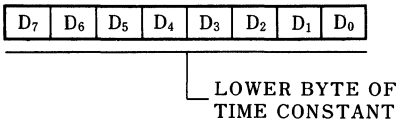


*ALWAYS 0 IN B CHANNEL

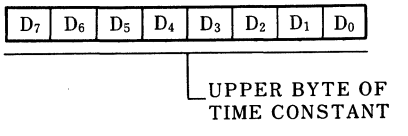
- **Read Register 10**



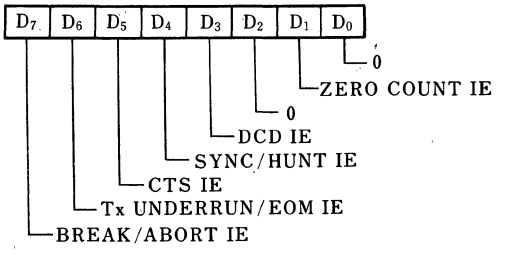
- **Read Register 12**



- **Read Register 13**

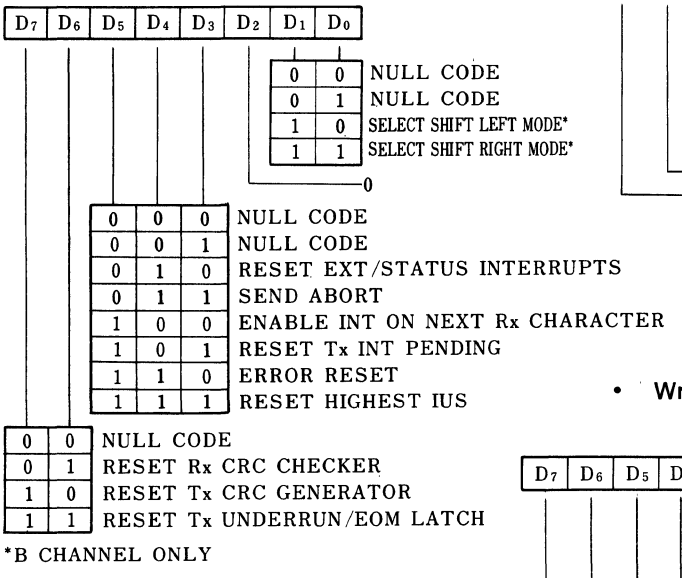


- **Read Register 15**



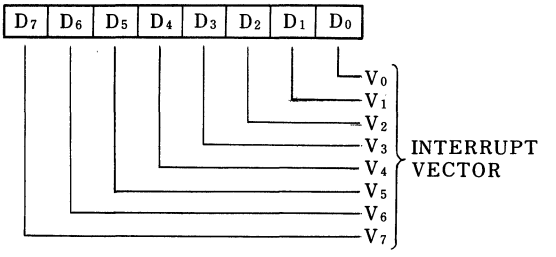
■ Write Registers

• Write Register 0



*B CHANNEL ONLY

• Write Register 2



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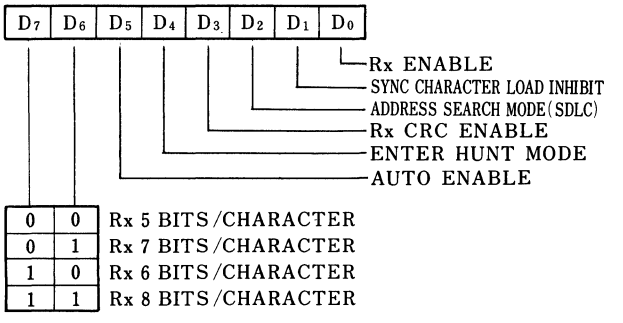

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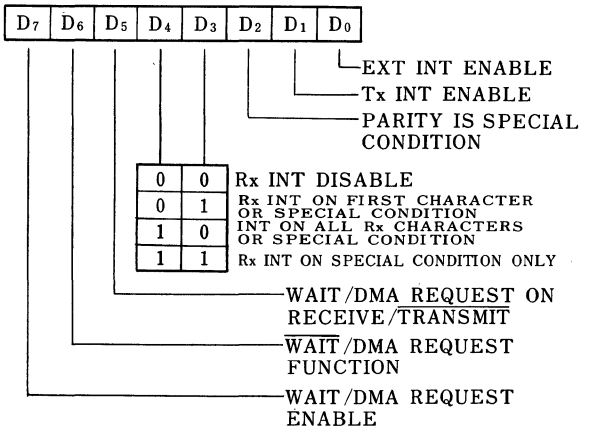

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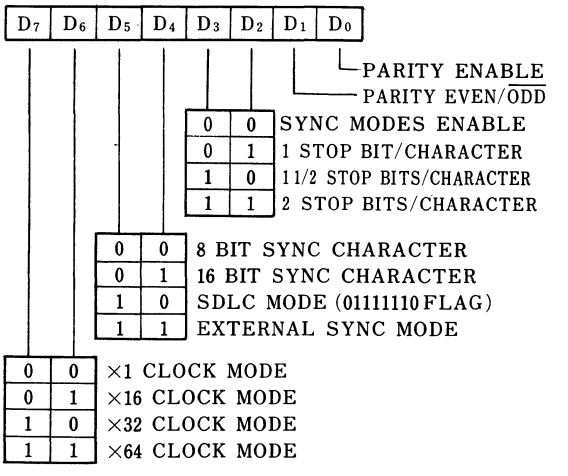

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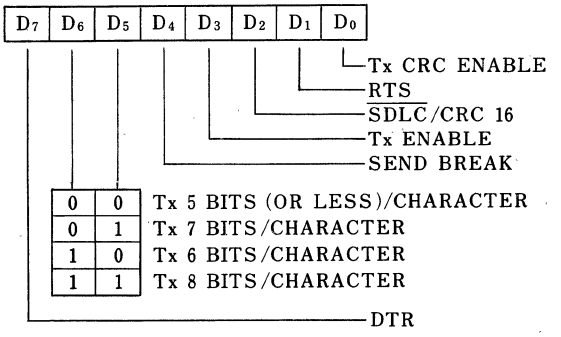

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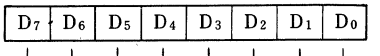
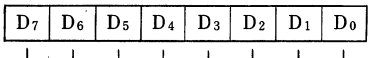


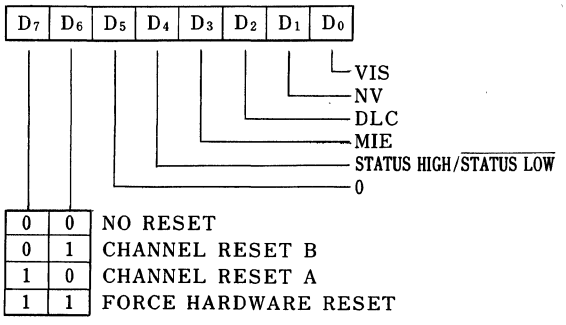
$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	MONOSYNC, 8 BITS
$SYNC_1$	$SYNC_6$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	MONOSYNC, 6 BITS
$SYNC_7$	$SNNC_6$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	BISYNC, 16 BITS
$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	1	1	1	1	BISYNC, 12 BITS
ADR_7	ADR_6	ADR_5	ADR_4	ADR_3	ADR_2	ADR_1	ADR_0	SDLC ADDRESS, 8 BITS
ADR_7	ADR_6	ADR_5	ADR_4	×	×	×	×	SDLC ADDRESS, 4 BITS

- **Write Register 7**



$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	MONOSYNC, 8 BITS
$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	×	×	MONOSYNC, 6 BITS
$SYNC_{15}$	$SYNC_{14}$	$SYNC_{13}$	$SYNC_{12}$	$SYNC_{11}$	$SYNC_{10}$	$SYNC_9$	$SYNC_8$	BISYNC, 16 BITS
$SYNC_{11}$	$SYNC_{10}$	$SYNC_9$	$SYNC_8$	$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$	BISYNC, 12 BITS
0	1	1	1	1	1	1	0	SDLC, FLAG

- **Write Register 9**



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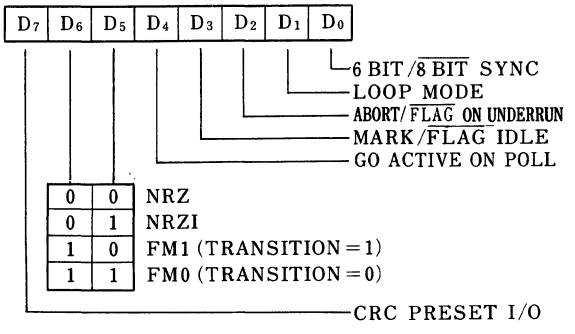

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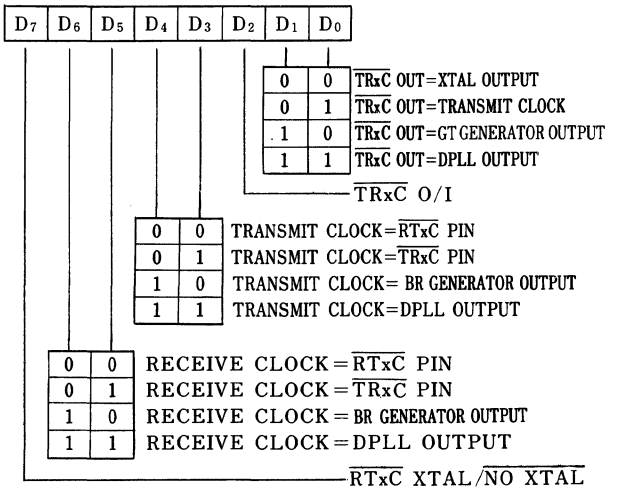

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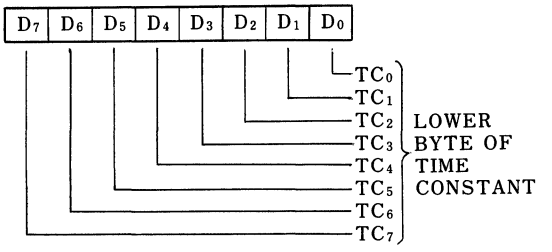
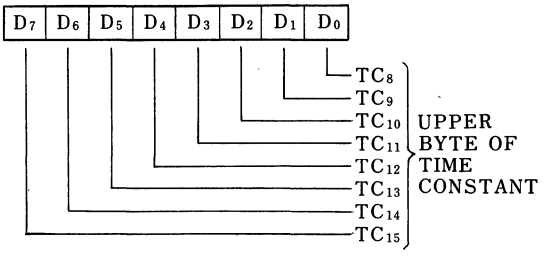
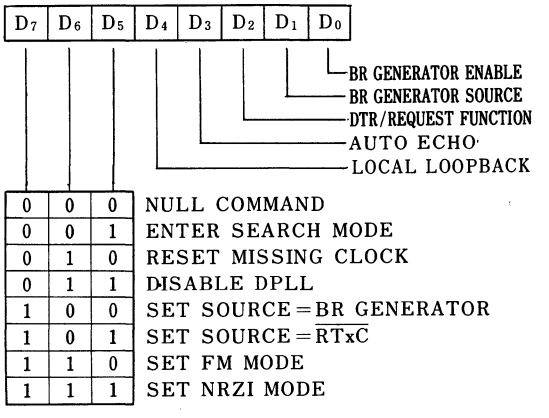


- **Write Register 13**



- **Write Register 14**



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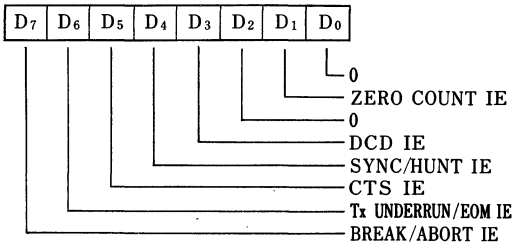


5

LH8036/LH8036A

Z8036/Z8036A Counter/Timer and Parallel I/O Unit

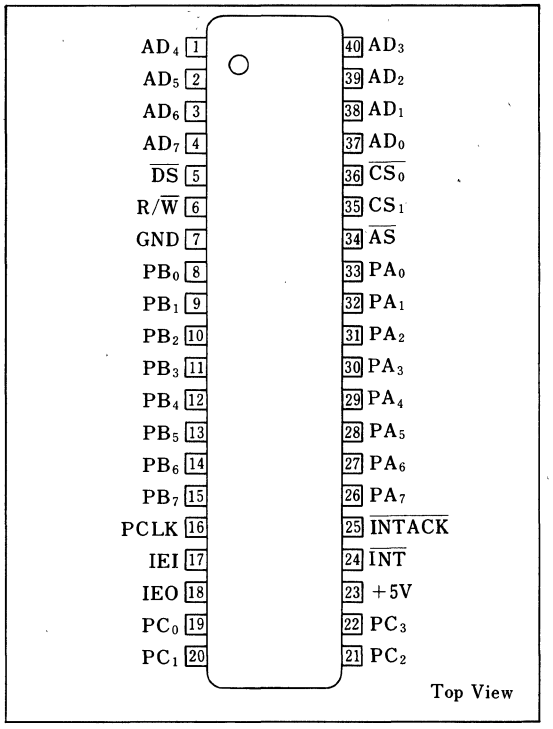
■ Description

The Z8036 Z-CIO Counter/Timer and Parallel I/O element is a general-purpose peripheral circuit, satisfying most counter/timer and parallel I/O needs encountered in system designs. This versatile device contains three I/O ports and three counter/timers. Many programmable options tailor its configuration to specific applications. The use of the device is simplified by making all internal registers (command, status, and data) readable and (except for status bits) writable. In addition, each register is given its own unique address so that it can be accessed directly-no special sequential operations are required. The Z-CIO is directly Z-Bus compatible.

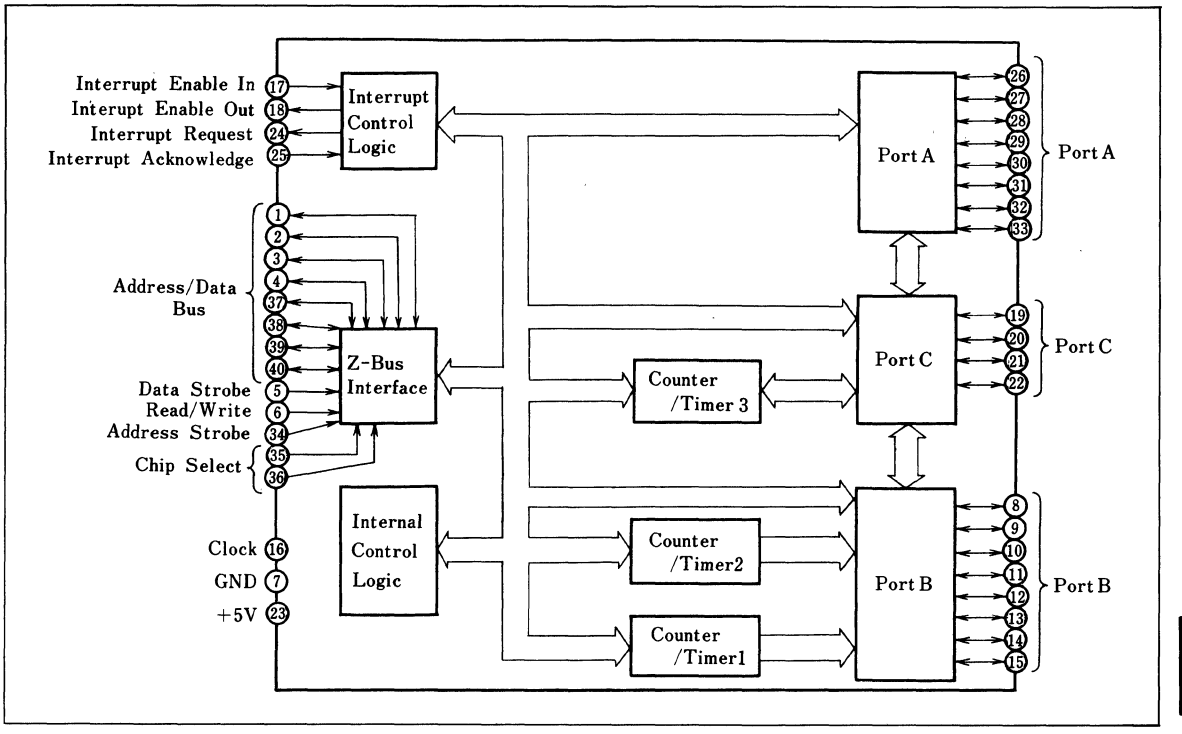
■ Features

1. Two independent 8-bit, double-buffered, bidirectional I/O ports plus a 4-bit special-purpose I/O port. I/O ports feature programmable polarity, programmable direction (Bit mode), "pulse catchers," and programmable opendrain outputs
2. Four handshake modes, including 3-Wire (like the IEEE-488)
3. REQUEST/$\overline{\text{WAIT}}$ signal for high-speed data transfer
4. Flexible pattern-recognition logic, programmable as a 16-vector interrupt controller
5. Three independent 16-bit counter/timers with up to four external access lines per counter/timer (count input, output, gate, and trigger), and three output duty cycles (pulsed, one-shot, and squarewave), programmable as retriggerable or nonretriggerable.
6. Easy to use since all registers are read/write and directly addressable.

■ Pin Connections



Block Diagram



Pin Description

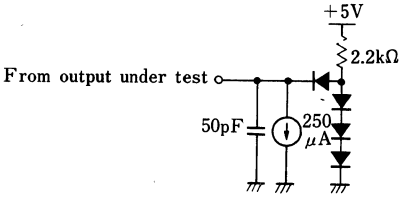
Pin	Meaning	I/O	Function
$AD_0 \sim AD_7$	Address/data bus	Bidirectional 3-state	Multiplexed system address/data bus.
$\overline{AS}$	Address strobe	I	Active low. $\overline{AS}$ determines address while low.
$\overline{DS}$	Data strobe	I	Active low. $\overline{DS}$ providies timing for data transfer while low.
$R/\overline{W}$	Read/write	I	$R/\overline{W}$ indicates that the CPU is reading from (high) or writing to (low) the Z-CIO.
$\overline{CS_0}$	Chip select 0	I	Active low. Chip select signal
CS_1	Chip select 1	I	Active high. Chip select signal
$\overline{INT}$	Interrupt request	Open-drain	Active low. $\overline{INT}$ is pulled low when the Z-CIO requests on interrupt.
$\overline{INTACK}$	Interrupt acknowledge	I	Active low. $\overline{INTACK}$ indicates that an Interrupt acknowledge cycle is in progress.
IEI	Interrupt enable in	I	Acvtive high. IEI is used to form an interrupt daisy chain that determines the priority order of interrupts.
IEO	Interrupt enable out	O	Active high. IEO is used to form an interrupt daisy chain that determines the priority order of interrupts.
$PA_0 \sim PA_7$	Port A I/O lines	Bidirectional 3-state	These eight I/O lines transfer information between the Z-CIO's port A and external devices.
$PB_0 \sim PB_7$	Port B I/O lines	Bidirectional 3-state	These eight I/O lines transfer information between the Z-CIO's port B and external devices.
$PC_0 \sim PC_3$	Port C I/O lines	Bidirectional 3-state	These four I/O lines transfer information between the Z-CIO's port C and external devices.
PCLK	Clock	I	Single-phase clock, need not be same as CPU clock.

Note : When $\overline{AS}$ and $\overline{DS}$ are detected "Low" at the same time, the Z-CIO is reset.

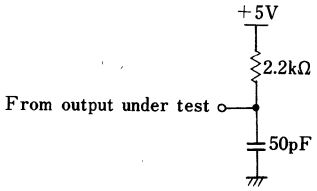
■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Input voltage	V_{IN}	−0.3～+7.0	V	1
Output voltage	V_{OUT}	−0.3～+7.0	V	1
Operating temperature	T_{opr}	0～+70	℃	
Storage temperature	T_{stg}	−65～+150	℃	

Note. 1: The maximum applicable voltage on any pin with respect to GND.



Standard test load



Open drain test load

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input high voltage	V_{IH}		2.0	V_{CC}+0.3	V
Input low voltage	V_{IL}		−0.3	0.8	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4		V
Output low voltage	V_{OL}	I_{OL}=+2.0mA		0.4	V
		I_{OL}=+3.2mA		0.5	V
Input leakage current	$\lvert I_{IL} \rvert$	0.4≦V_{IN}≦2.4V		10.0	μA
Output leakage current	$\lvert I_{OL} \rvert$	0.4≦V_{OUT}≦2.4V		10.0	μA
Supply current	I_{CC}			250	mA

■ Capacitance

(f=1MHz, Ta=0～+70℃)

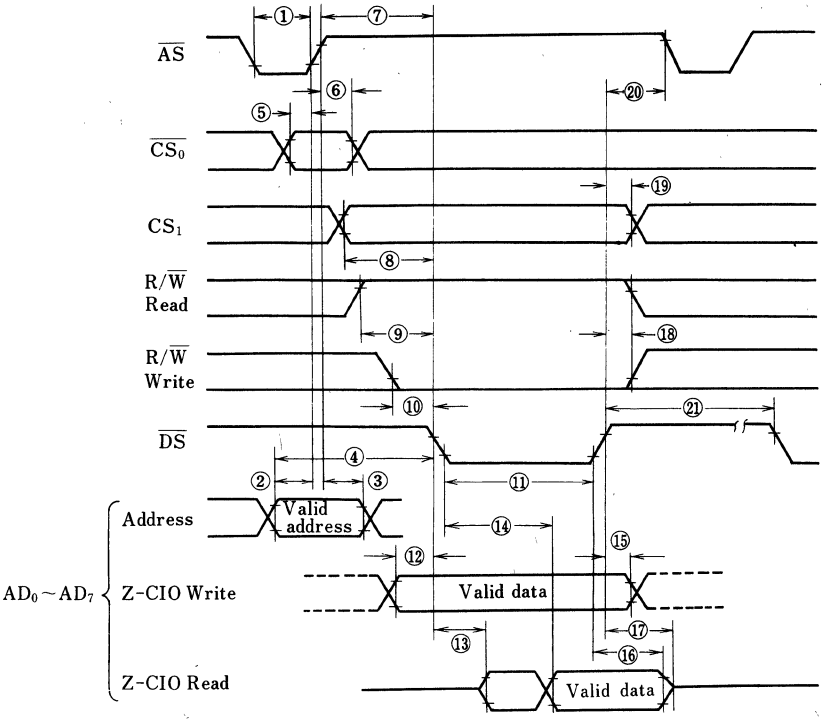
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_{IN}	Unmeasured pins returned to ground		10	pF
Output capacitance	C_{OUT}			15	pF
Bidirectional capacitance	$C_{I/O}$			20	pF

■ AC Characteristics

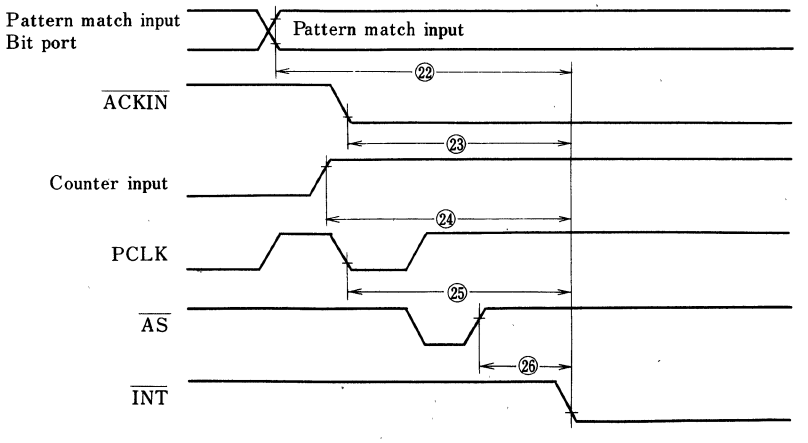
(1) Interface timing

No.	Symbol	Parameter	LH8036		LH8036A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TwAS	$\overline{AS}$ low width	70	2000	50	2000	ns	
2	TsA (AS)	Address to $\overline{AS}$ ↑ setup time	30		10		ns	1
3	ThA (AS)	Address to $\overline{AS}$ ↑ hold time	50		30		ns	1
4	TsA (DS)	Address to $\overline{DS}$ ↓ setup time	130		100		ns	1
5	TsCSO (AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ setup time	0		0		ns	1
6	ThCSO (AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ hold time	60		40		ns	1
7	TdAS (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ delay	60		40		ns	1
8	TsCS1 (DS)	CS_1 to $\overline{DS}$ ↓ setup time	100		80		ns	
9	TsRWR (DS)	R/$\overline{W}$ (read) to $\overline{DS}$ ↓ setup time	100		80		ns	
10	TsRWW (DS)	R/$\overline{W}$ (write) to $\overline{DS}$ ↓ setup time	0		0			
11	TwDS	$\overline{DS}$ low width	390		250		ns	
12	TsDW (DSf)	Write data to $\overline{DS}$ ↓ setup time	30		20		ns	
13	TdDS (DRV)	$\overline{DS}$ (read) ↓ to address data bus driven	0		0			
14	TdDSf (DR)	$\overline{DS}$ ↓ to read data valid delay		250		180	ns	
15	ThDW (DS)	Write data to $\overline{DS}$ ↑ hold time	30		20		ns	
16	TdDSr (DR)	$\overline{DS}$ ↑ to read data not valid delay	0		0			
17	TdDS (DRz)	$\overline{DS}$ ↑ to read data float delay		70		45	ns	2
18	ThRW (DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ hold time	55		40		ns	
19	ThCS1 (DS)	CS_1 to $\overline{DS}$ ↑ hold time	55		40		ns	
20	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay	50		25		ns	
21	Trc	Valid access recovery time	1000		650		ns	3
22	TdPM (INT)	Pattern match to $\overline{INT}$ delay (bit port)		1		1	AS cycle +ns	
23	TdACK (INT)	$\overline{ACKIN}$ to $\overline{INT}$ delay (Port with handshake)		4		4	AS cycle +ns	4
24	TdCI (INT)	Counter input to $\overline{INT}$ delay (Counter mode)		1		1	AS cycle +ns	
25	TdPC (INT)	PCLK to $\overline{INT}$ delay (Timer mode)		1		1	AS cycle +ns	
26	TdAS (INT)	$\overline{AS}$ to $\overline{INT}$ delay					ns	
27	TsIA (AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ setup time	0		0		ns	
28	ThIA (AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ hold time	250		250		ns	
29	TsAS (DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (acknowledge) ↓ setup time	350		250		ns	5
30	TdDSA (DR)	$\overline{DS}$ (acknowledge) ↓ to read data valid delay		250		180	ns	
31	TwDSA	$\overline{DS}$ (acknowledge) low width	390		250		ns	
32	TdAS (IEO)	$\overline{AS}$ ↑ to IEO ↓ delay ($\overline{INTACK}$ cycle)		350		250	ns	5
33	TdIEI (IEO)	IEI to IEO delay		150		100	ns	5
34	TsIEI (DSA)	IEO to $\overline{DS}$ (acknowledge) ↓ setup time	100		70		ns	5
35	ThIEI (DSA)	IEI to $\overline{DS}$ (acknowledge) ↑ hold time	100		70		ns	
36	TdDSA (INT)	$\overline{DS}$ (acknowledge) ↓ to $\overline{INT}$ ↑ delay		600		600	ns	

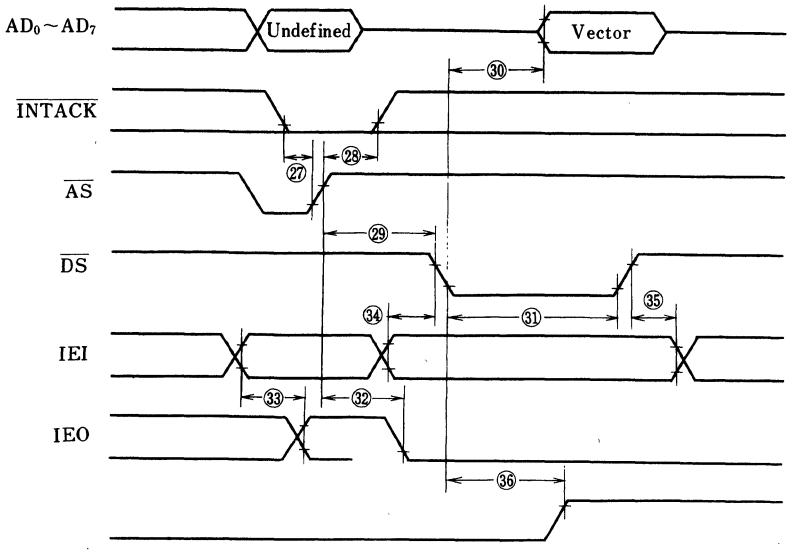
Note : "↑" indicates a rising edge and "↓" a falling edge.
Note 1: Parameter does not apply to Interrupt Acknowledge transactions.
Note 2: Float delay is measured to the time when the output has changed 0.5 V from steady state with minimum ac load and maximum dc load.
Note 3: This is the delay from $\overline{DS}$ ↑ of one CIO access to $\overline{DS}$ ↓ of another CIO access.
Note 4: The delay is from DAV ↓ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wire Output Handshake. One additional AS cycle is required for ports in the Single Buffered mode.
Note 5: The parameters for the devices in any particular daisy chain must meet the following constraint : the delay from $\overline{AS}$ ↑ to $\overline{DS}$ ↓ must be greater than the sum of TdAS (IEO) for the highest priority peripheral, TsIEI (DSA) for the lowest priority peripheral, and TdIEI (IEO) for each peripheral separating them in the chain.



CPU interface timing



Interrupt timing



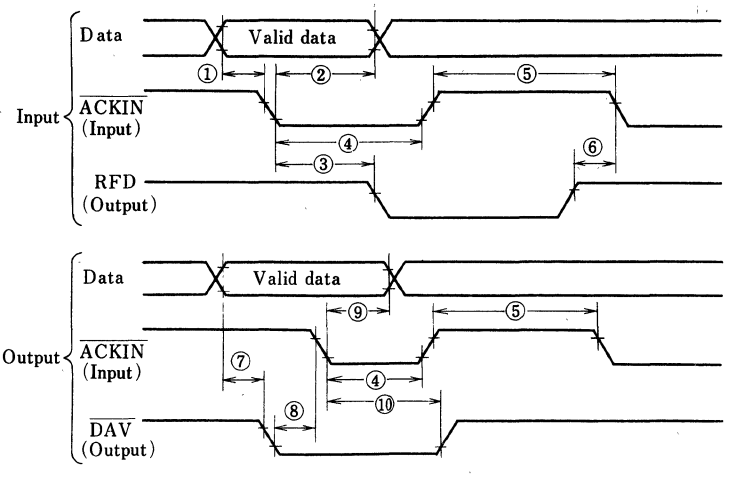
Interrupt acknowledge timing

(2) Handshake timing

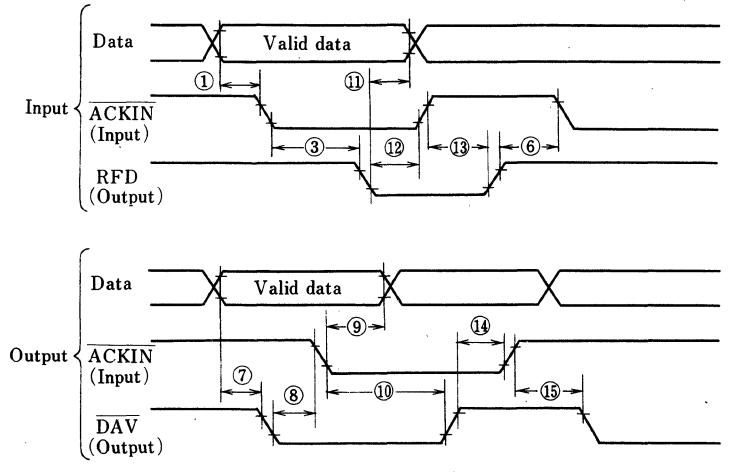
No.	Symbol	Parameter	LH8036		LH8036A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TsDI (ACK)	Data input to $\overline{ACKIN}$ ↓ setup time	0		0		ns	
2	ThDI (ACK)	Data input to $\overline{ACKIN}$ ↓ hold time-strobed handshake					ns	
3	TdACKf(RFD)	$\overline{ACKIN}$ ↓ to RFD ↓ delay	0		0		ns	
4	TwACKI	$\overline{ACKIN}$ low width-strobed handshake					ns	
5	TwACKh	$\overline{ACKIN}$ high width-strobed handshake					ns	
6	TdRFDr(ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ delay	0		0		ns	
7	TsDO (DAV)	Data out to $\overline{DAV}$ ↓ setup time	25		20		ns	1
8	TdDAVf (ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ delay	0		0		ns	
9	ThDO (ACK)	Data out to $\overline{ACKIN}$ ↓ hold time	1		1		AS cycle	
10	TdACK (DAV)	$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ delay	1		1		AS cycle	
11	ThDI (RFD)	Data input to RFD ↓ hold time-interlocked handshake	0		0		ns	
12	TdRFDf(ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ delay-interlocked handshake	0		0		ns	
13	TdACKr(RFD)	$\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ delay-interlocked and 3-wire handshake	0		0		ns	
14	TdDAVr (ACK)	$\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑ (RFD ↑) delay-interlocked and 3-wire handshake	0		0		ns	
15	TdACK (DAV)	$\overline{ACKIN}$ ↑ (RFD ↑) to $\overline{DAV}$ ↓ delay-interlocked and 3-wire handshake	0		0		ns	
16	TdDAVlf (DAC)	$\overline{DAV}$ ↓ to DAC ↑ delay-input 3-wire handshake	0		0		ns	
17	ThDI (DAC)	Data input to DAC ↑ hold time-3-wire handshake	0		0		ns	
18	TdDACOr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ delay-input 3-wire handshake	0		0		ns	
19	TdDAVlr (DAC)	$\overline{DAV}$ ↑ to DAC ↓ delay-input 3-wire handshake	0		0		ns	

No.	Symbol	Parameter	LH8036		LH8036A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
20	TdDAVOf (DAC)	$\overline{DAV}$ ↓ to DAC ↑ delay-output 3-wire handshake	0		0		ns	
21	ThDO (DAC)	Data output to DAC ↑ hold time-3-wire handshake	1		1		AS cycle	
22	TdDAClr (DAV)	DAC ↑ to $\overline{DAV}$ ↑ delay-output 3-wire handshake	1		1		AS cycle	
23	TdDAVOr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ delay-output 3-wire handshake	0		0		ns	

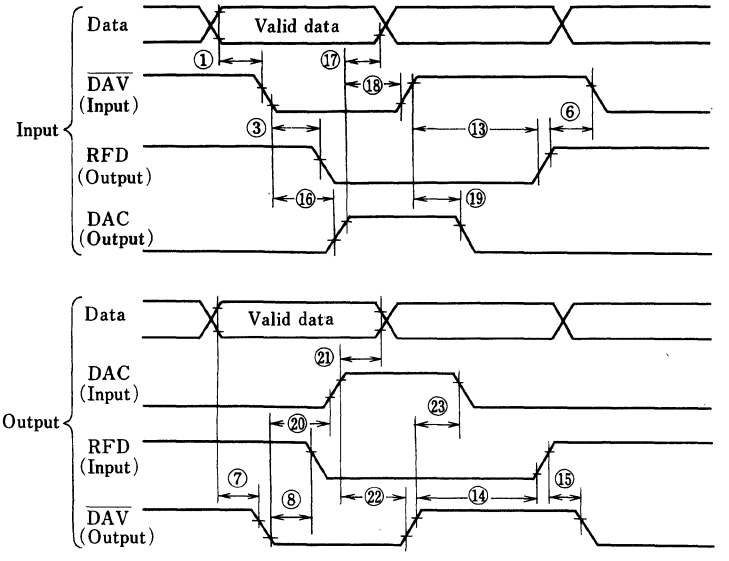
Note 1: This time can be extended through the use of the deskew timers.



Strobe handshake



Interlock handshake

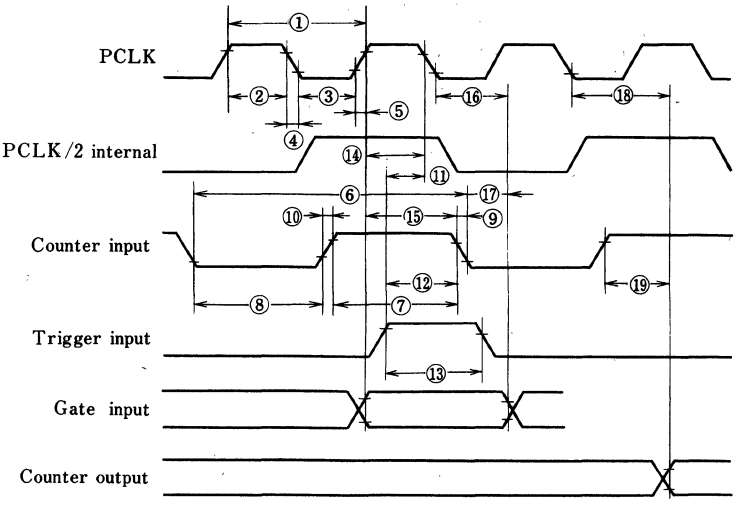


3-Wire handshake

(3) Counter/timer timing

No.	Symbol	Parameter	LH8036		LH8036A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TcPC	PCLK cycle time	250	4000	165	4000	ns	1
2	TwPCh	PCLK high width	105	2000	70	2000	ns	
3	TwPCl	PCLK low width	105	2000	70	2000	ns	
4	TfPC	PCLK fall time		20		10	ns	
5	TrPC	PCLK rise time		20		15	ns	
6	TcCI	Counter input cycle time	500		330		ns	
7	TCIh	Counter input high width	230		150		ns	
8	TwCIl	Counter input low width	230		150		ns	
9	TfCI	Counter input fall time		20		15	ns	
10	TrCI	Counter input rise time		20		15	ns	
11	TsTI (PC)	Trigger input to PCLK ↓ setup time (Timer mode)					ns	2
12	TsTI (CI)	Trigger input to counter input ↓ setup time (Counter mode)					ns	2
13	TwTI	Trigger input pulse width (High or Low)					ns	
14	TsGI (PC)	Gate input to PCLK ↓ setup time (Timer mode)					ns	2
15	TsGI (CI)	Gate input to counter input ↓ setup time (Counter mode)					ns	2
16	ThGI (PC)	Gate input to PCLK ↓ hold time (Timer mode)					ns	2
17	ThGI (CI)	Gate input to counter input ↓ hold time (Counter mode)					ns	2
18	TdPC (CO)	PCLK to counter output delay (Timer mode)					ns	
19	TdCI (CO)	Counter input to counter output delay (Counter mode)					ns	

Note 1: PCLK is only used with the counter/timers (in Timer mode), the deskew timers, and the REQUEST/$\overline{\text{WAIT}}$ logic. If these functions are not used, the PCLK input can be held low.
Note 2: These parameters must be met to guarantee that trigger or gate are valid for the next counter/timer cycle.

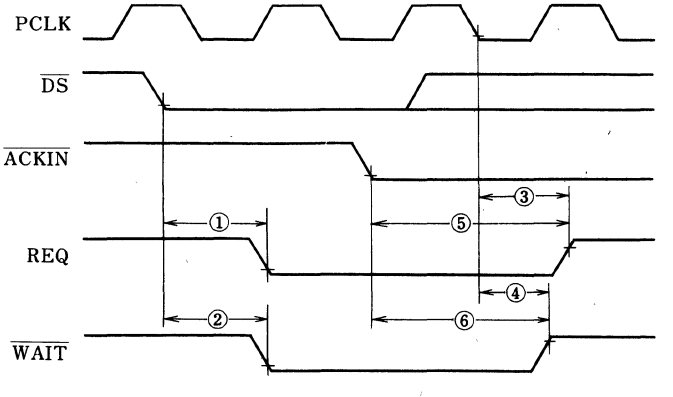


Counter/timer timing

(4) REQUEST/$\overline{\text{WAIT}}$ timing

No.	Symbol	Parameter	LH8036		LH8036A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TdDS (REQ)	$\overline{\text{DS}}$ ↓ to REQ ↓ delay					ns	
2	TdDS (WAIT)	$\overline{\text{DS}}$ ↓ to $\overline{\text{WAIT}}$ ↓ delay					ns	
3	TdPC (REQ)	PCLK ↓ to REQ ↑ delay					ns	
4	TdPC (WAIT)	PCLK ↓ to $\overline{\text{WAIT}}$ ↑ delay					ns	
5	TdACK (REQ)	ACKIN ↓ to REQ ↑ delay					AScycles+ PCLK cycles+ns	1
6	TdACK (WAIT)	ACKIN ↓ to $\overline{\text{WAIT}}$ ↑ delay					PCLK cycles+ns	

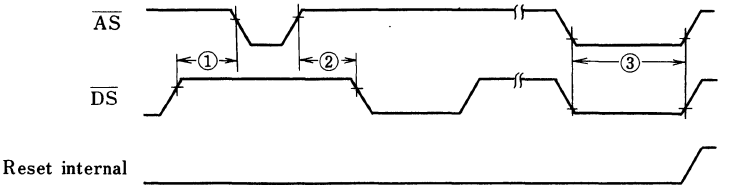
Note 1: The Delay is from DAV ↓ for the 3-wire input handshake. Delay from $\overline{\text{DAC}}$ ↑ for 3-wire handshake output mode.



REQUEST/$\overline{\text{WAIT}}$ timing

(5) Reset timing

No.	Symbol	Parameter	LH8036		LH8036A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TdDSQ (AS)	Delay from $\overline{DS}$ ↑ to $\overline{AS}$ ↓ for no reset	40		15		ns	
2	TdASQ (DS)	Delay from $\overline{AS}$ ↑ to $\overline{DS}$ ↓ for no reset	50		30		ns	
3	TwRES	Minimum width of $\overline{AS}$ and $\overline{DS}$ both low for reset	250		170		ns	

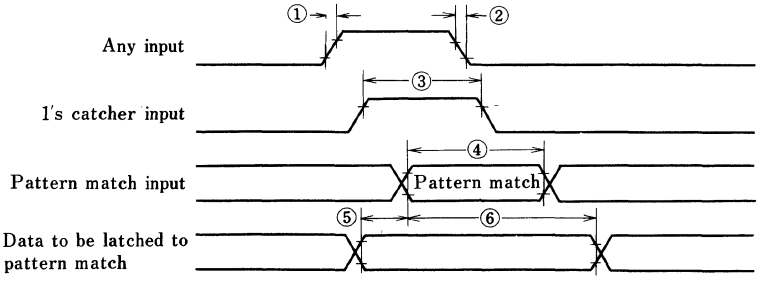


Reset timing

(6) Miscellaneous port timing

No.	Symbol	Parameter	LH8036		LH8036A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	Trl	Any input rise time		100		100	ns	
2	Tfl	Any input fall time		100		100	ns	
3	Twl's	1's catcher high width	250		170		ns	1
4	TwPM	Pattern match input valid (Bit port)	750		500		ns	
5	TsPMD	Data latched on pattern match setup time (Bit port)	0		0		ns	
6	ThPMD	Data latched on pattern match hold time (Bit port)	1000		650		ns	

Note 1: If the input is programmed inverting, a low-going pulse of the same width will be detected.



Miccellaneous port timing

■ Functional Description

(1) I/O port operations

Of the Z-CIO's three I/O ports, two (Ports A and B) are general-purpose, and the third (Port C) is a special-purpose 4-bit port. Ports A and B can be configured as input, output or bidirectional ports with handshake (Four different handshakes are available.). They can also be linked to form a signal 16-bit port. If they are not used as ports with handshake, they provide 16 input or output bits with the data direction programmable on a bit-by-bit basis. Port B also provides access for Counter/Timers 1 and 2. In all configurations, Ports A and B can be programmed to recognize specific data patterns and to generate interrupts when the pattern is encountered.

The four bits of Port C provide the handshake lines for Ports A and B when required. A REQUEST/$\overline{WAIT}$ line can also be provided so that

Z-CIO transfers can be synchronized with DMAs or CPUs. Any Port C bits not used for handshake or REQUEST/WAIT can be used as input or output bits (individually data direction programmable) or external access lines for Counter/Timer3. Port C does not contain any pattern-recognition logic. It is, however, capable of bit-addressable writes. With this feature, any combination of bit can be set and/or cleared while the other bits remain undisturbed without first reading the register.

(2) Bit port operations

In bit port operations, the port's Data Direction register specifies the direction of data flow for each bit. A 1 specifies an input bit, and a 0 specifies an output bit. If bits are used as I/O bits for a counter/timer, they should be set as input or output, as required.

The Data Path Polarity register provides the capability of inverting the data path. A 1 specifies inverting, and a 0 specifies noninverting. All discussions of the port operations assume that the path is noninverting.

The value returned when reading an input bit reflects the state of the input just prior to the read. A 1's catcher can be inserted into the input data path by programming a 1 to the corresponding bit position of the port's Special I/O Control register. When a 1 is detected at the 1's catcher input, its output is set to a 1 until it is cleared. The 1's catcher is cleared by writing a 0 to the bit. In all other cases, attempted writes to input bits are ignored.

When Ports A and B include output bits, reading the Data register returns the value being output. Reads of Port C return the state of the pin. Outputs can be specified as open-drain by writing a 1 to the corresponding bit of the port's Special I/O Control register. Port C has the additional feature of bit-addressable writes. When writing to Port C, the four most significant bits are used as a write protect mask for the least significant bits (0-4, 1-5, 2-6, and 3-7). If the write protect bit is written with a 1, the state of the corresponding output bit is not changed.

(3) Ports with handshake operation

Ports A and B can be specified as 8-bit input, output, or bidirectional ports with handshake. The Z-CIO provides four different handshakes for its ports : Interlocked, Strobed, Pulsed, and 3-Wire. When specified as a port with handshake, the transfer of data into and out of the port and interrupt generation is under control of the handshake logic. Port C provides the handshake lines as shown in Table 1. Any Port C lines not used for handshake can be used as simple I/O lines or as access lines for Counter/Timer 3.

When Ports A and B are configured as ports with handshake, they are double-buffered. This allows for more relaxed interrupt service routine response time. A second byte can be input to or output from the port before the interrupt for the first byte is serviced. Normally, the Interrupt Pending (IP) bit is set and an interrupt is generated when data is shifted into the Input register (input port) or out of the Output register (output port). For input and output ports, the IP is automatically cleared when the data is read or written. In bidirectional ports, IP is cleared only by command. When the Interrupt on Two Bytes (ITB) control bit is set to 1, interrupts are generated only when two bytes of data are available to be read or written. This allows a minimum of 16 bits of information to be transferred on each interrupt. With ITB set, the IP is not automatically cleared until the second byte of data is read or written.

When the Single Buffer (SB) bit is set to 1, the port acts as if it is only single-bufferd. This is useful if the handshake line must be stopped on a byte-by-byte basis.

Ports A and B can be linked to form a 16-bit port by programming a 1 in the Port Link Control (PLC) bit. In this mode, only Port A's Handshake Specification and Command and Status registers are used. Port B must be specified as a bit port. When linked, only Port A has pattern-match capability. Port B's pattern-match capability must be disabled. Also, when the ports are linked, Port B's Data register must be read or written before Port A's.

When a port is specified as a port with handshake, the type of port it is (input, output, or bidirectional) determines the direction of data flow. The data direction for the bidirectional port is determined by a bit in Port C (Table 1). In all cases, the contents of the Data Direction register are ignored. The contents of the Special I/O Control register apply only to output bits (3-state or open-drain). Inputs may not have 1's catchers ; therefore. those bits in the Special I/O Control register are ignored. Port C lines used for handshake should be programmed as inputs. The handshake specification overrides Port C's Data Direction register for bits that must be outputs. The contents of Port C's Data Path Polarity register still apply.

Table 1. Port C bit utilization

Port A/B Configuration	PC_3	PC_2	PC_1	PC_0
Ports A and B : Bit ports	Bit I/O	Bit I/O	Bit I/O	Bit I/O
Port A : Input or output port (Interlocked, strobed, or pulsed handshake)*	RFD or $\overline{DAV}$ (O)	$\overline{ACKIN}$ (I)	REQUEST/$\overline{WAIT}$ or Bit I/O	Bit I/O
Port B : Input or output port (Interlocked, strobed, or pulsed handshake)*	REQUEST/$\overline{WAIT}$ or Bit I/O	Bit I/O	FD or $\overline{DAV}$ (O)	$\overline{ACKIN}$ (I)
Port A or B : Input port (3-wire handshake)	RFD (O)	$\overline{DAV}$ (I)	REQUEST/$\overline{WAIT}$ or Bit I/O	DAC (O)
Port A or B : Output port (3-wire handshake)	$\overline{DAV}$ (O)	DAC (I)	REQUEST/$\overline{WAIT}$ or Bit I/O	RFD (I)
Port A or B : Bidirectional port (Interlocked or strobed handshake)	RFD or DAV (O)	$\overline{ACKIN}$ (I)	REQUEST/$\overline{WAIT}$ or Bit I/O	IN/$\overline{OUT}$

*Both ports A and B can be specified input or output with interlocked, strobed, or pulsed handshake at the same time if neither uses REQUEST/$\overline{WAIT}$.

(4) Interlocked handshake

In the Interlocked Handshake mode, the action of the Z-CIO must be acknowledged by the external device before the next action can take place. Fig. 1 shows timing for Interlocked Handshake. An output port does not indicate that new data is available until the external device indicates it is ready for the data. Similarly, an input port does not indicate that it is ready for new data until the data source indicates that the previous of the data is no loger available, thereby acknowledging the input port's acceptance of the last byte. This allows the Z-CIO to interface directly to the port of a Z8 microcomputer, a UPC, an FIO, an FIFO, or to another Z-CIO port with no external logic.

A 4-bit deskew timer can be inserted in the Data Available ($\overline{DAV}$) output for output ports. As data is transferred to the Buffer register, the deskew timer is triggered. After the number of PCLK cycles specified by the deskew timer time constant pluse one, $\overline{DAV}$ is allowed to go Low. The deskew timer therefore guarantees that the output data is valid for a specified minimum amount of time before $\overline{DAV}$goes Low. Deskew timers are available for output ports independent of the type of handshake employed.

(5) Strobed handshake

In the Strobed Handshake mode, data is "strobed" into or out of the port by the external logic. The falling edge of the Acknowledge Input ($\overline{ACKIN}$) strobes data into or out of the port. Fig. 1 shows timing for the Strobed Handshake. In contrast to the Interlocked Handshake, the signal indicating the port is ready for another data transfer operates independently of the $\overline{ACKIN}$ input. It is up to the external logic to ensure that data overflows or underflows do not occur.

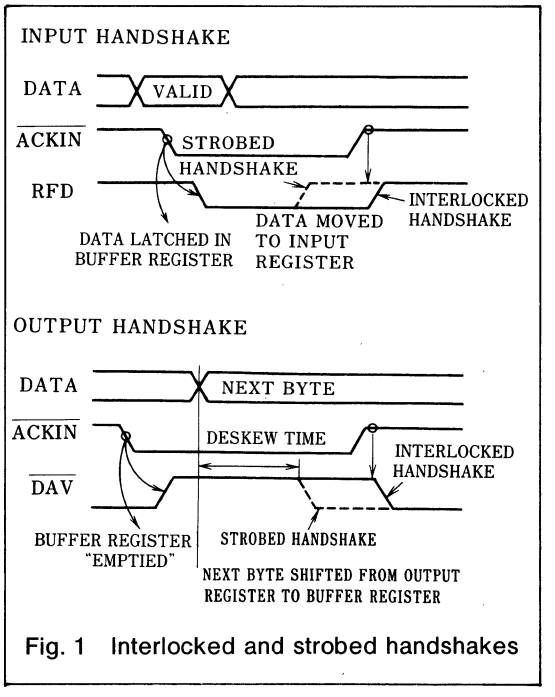


Fig. 1 Interlocked and strobed handshakes

(6) 3-wire handshake

The 3-Wire Handshake is designed for the situation in which one output port is communicating with many input ports simultaneously. It is essentially the same as the Interlocked Handshake, except that two signals are used to indicate if an in-

put port is ready for new data or if it has accepted the present data. In the 3-Wire Handshake (Fig. 2), the rising edge of one status line indicates that the port is ready for data, and the rising edge of another status line indicates that the data has been accepted. With the 3-Wire Handshake, the output lines of many input ports can be bussed together with open-drain drivers ; the output port knows when all the ports have accepted the data and are ready. This is the same handshake as is used on the IEEE-488 bus. Because this handshake requires three lines, only one port (either A or B) can be a 3-Wire Handshake port at a time. The 3-Wire Handshake is not available in the bidirectional mode. Because the port's direction can be changed under software control, however, bidirectional IEEE-488-type transfers can be performed.

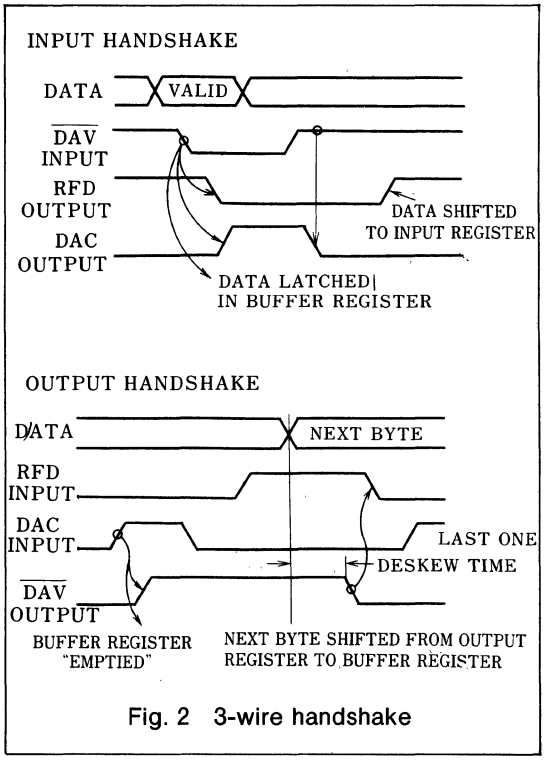


Fig. 2 3-wire handshake

(7) Pulsed handshake

The Pulsed Handshake (Fig. 3) is designed to interface to mechanical-type devices that require data to be held for long periods of time and need relatively wide pulses to gate the data into or out of the device. The logic is the same as the Interlocked Handshake mode, except that an internal counter/timer is linked to the handshake logic. If the port is specified in the input mode, the timer is inserted in the $\overline{\text{ACKIN}}$ path. The external $\overline{\text{ACKIN}}$ input trig-

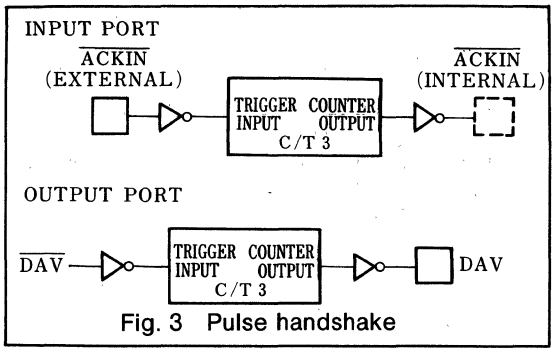


Fig. 3 Pulse handshake

gers the timer and its output used as the Interlocked Handshake's normal acknowledge input. If the port is an output port, the timer is placed in the Data Available ($\overline{\text{DAV}}$) output path. The timer is triggered when the normal Interlocked Handshake $\overline{\text{DAV}}$ output goes Low and the timer output is used as the actual $\overline{\text{DAV}}$ output. The counter/timer maintains all of its normal capabilities. This handshake is not available to bidirectional ports.

(8) REQUEST/WAIT line operation

Port C can be programmed to provide a status signal output in addition to the normal handshake lines for either Port A or B when used as a port with handshake. The additional signal is either a REQUEST or $\overline{\text{WAIT}}$ signal. The REQUEST signal indicates when a port is ready to perform a data transfer via the Z-Bus. It is intended for use with a DMA-type device. The $\overline{\text{WAIT}}$ signal provides synchronization for transfers with a CPU. Three bits in the Port Handshake Specification register provide controls for the REQUEST/$\overline{\text{WAIT}}$ logic. Because the extra Port C line is used, only one port can be specified as a port with a handshake and a REQUEST/$\overline{\text{WAIT}}$ line. The other port must be a bit port.

Operation of the REQUEST line is modified by the state of the port's Interrupt on Two Bytes (ITB) control bit. When ITB is 0, the REQUEST line goes active as soon as the Z-CIO is ready for a data transfer. If ITB is 1, REQUEST does not go active until two bytes can be transferred. REQUEST stays active as long as a byte is available to be read or written.

The SPECIAL REQUEST function is reserved for use with bidirectional ports only. In this case, the REQUEST line indicates the status of the register not being used in the data path at that time. If the IN/$\overline{\text{OUT}}$ line is High, the REQUEST line is High when the Output register is empty. If IN/$\overline{\text{OUT}}$ is Low, the REQUEST line is High when the Input

register is full.

(9) Pattern-recognition logic operation

Both Ports A and B can be programmed to generate interrupts when a specific pattern is recognized at the port. The pattern-recognition logic is independent of the port application, thereby allowing the port to recognize patterns in all of its configurations. The pattern can be independently specified for each bit as 1, 0, rising edge, falling edge, or any transition. Individual bits may be masked off. A pattern-match is defined as the simultaneous satisfaction of all nonmasked bit specifications in the AND mode or the satisfaction of any nonmasked bit specifications in either of the OR or OR-Priority Encoded Vector modes.

The pattern specified in the Pattern Definition register assumes that the data path is programmed to be noninverting. If an input bit in the data path is programmed to be inverting, the pattern detected is the opposite of the one specified. Output bits used in the pattern-match logic are internally sampled before the invert/noninvert logic.

(10) Bit port pattern-recognition operations

During bit port operations, pattern-recognition may be performed on all bits, including those used as I/O for the counter/timers. The input to the pattern-recognition logic follows the value at the pins (through the invert/noninvert logic) in all cases except for simple inputs with 1's catchers. In this case, the output of the 1's catcher is used. When operating in the AND or OR mode, it is the transition from a nomatch to a match state that causes the interrupt. In the "OR" mode, if a second match occurs before the first match goes away, it does not cause an interrupt. Since a match condition only lasts a short time when edges are specified, care must be taken to avoid losing a match condition. Bit ports specified in the OR-Priority Encoded Vector mode generate interrupts as long as any match state exists. A transition from a no-match to a match state is not required.

The pattern-recognition logic of bit ports operates in two basic modes : Transparent and Latched. When the Latch on Pattern Match (LPM) bit is set to 0 (Transparent mode), the interrupt indicates that a specified pattern has occurred, but a read of the Data register does not necessarily indicate the state of the port at the time the interrupt was generated. In the Latched mode (LPM = 1), the state of all the port inputs at the time the interrupt was generated is latched in the input register and held until IP is cleared. In all cases, the PMF indicates the state of the port at the time it is read.

If a match occurs while IP is already set, an error condition exists. If the Interrupt On Error bit (IOE) is 0, the match is ignored. However, if IOE is 1, after the first IP is cleared, it is automatically set to 1 along with the Interrupt Error (ERR) flag. Matches occurring while ERR is set are ignored. ERR is cleared when the corresponding IP is cleared.

When a pattern-match is pressent in the OR-Priority Encoded Vector mode, IP is set to 1. The IP cannot be cleared until a match is no longer present. If the interrupt vector is allowed to include status, the vector returned during Interrupt Acknowledge indicates the highest priority bit matching its specification at the time of the Acknowledge cycle. Bit 7 is the highest priority and bit 0 is the lowest. The bit initially causing the interrupt may not be the one indicated by the vector if a higher priority bit matches before the Acknowledge. Once the Acknowledge cycle is initiated, the vector is frozen until the corresponding IP is cleared. Where inputs that cause interrupts might change before the interrupt is serviced, the 1's catcher can be used to hold the value. Because a no-match to match transition is not required, the source of the interrupt must be cleared before IP is cleared or else a second interrupt is generated. No error detection is performed in this mode and the Interrupt On Error bit should be set to 0.

(11) Ports with handshake pattern-recognition operation

In this mode, the handshake logic normally controls the setting of IP and, therefore, the generation of interrupt requests. The pattern-match logic controls the Pattern Match Flag (PMF). The data is compared with the match pattern when it is shifted from the Buffer register to the Input register (input port) or when it is shifted from the Output register to the Buffer register (output port). The pattern-match logic can override the handshake logic in certain situations. If the port is programmed to interrupt when two bytes of data are available to be read or written, but the first byte matches the specified pattern, the pattern-recognition logic sets IP and generates an interrupt. While PMF is set, IP cannot be cleared by reading or writing the data registers. IP must be cleared by command. The input register is not emptied while IP is set, nor is the output register filled until IP is cleared.

If the Interrupt on Match Only (IMO) bit is set, IP is set only when the data matches the pattern. This is useful in DMA-type applications when interrupts are required only after a block of data is transferred.

(12) Counter/timer operation

The three independent 16-bit counter/timers consist of a presettable 16-bit down counter, a 16-bit Time Constant register, a 16-bit Current Counter register, an 8-bit Mode Specification register, an 8-bit Command and Status register, and the associated control logic that links these registers.

The flexibility of the counter/timers is enhanced by the provision of up to four lines per counter/timer (counter input, gate input, trigger input, and counter/timer output) for direct external control and status. Counter/Timer 1's external I/O lines are provided by the four most significant bits of Port B. Counter/Timer 2's are provided by the four least significant bits of Port B. Counter/Timer 3's external I/O lines are provided by the four bits of Port C. The utilization of these lines (Table 2) is programmable on a bit-by-bit basis via the Counter/Timer Mode Specification registers.

When external counter/timer I/O lines are to be used, the associated port lines must be vacant and programmed in the proper data direction. Lines used for counter/timer I/O have the same characteristics as simple input lines. They can be specified as inverting or noninverting ; they can be read and used with the pattern-recognition logic. They can also include the 1's catcher input.

Counter/Timers 1 and 2 can be be linked internally in three different ways. Counter/Timer 1's output (inverted) can be used as Counter/Timer 2's trigger, gate, or counter input. When linked, the counter/timers have the same capabilities as when used separately. The only restriction is that when Counter/Timer 1 drives Counter/Timer 2's count input, Counter/Timer 2 must be programmed with its external count input disabled.

Table 2 Counter/timer external access

Function	C/T_1	C/T_2	C/T_3
Counter/timer output	PB4	PB0	PC0
Counter input	PB5	PB1	PC1
Trigger input	PB6	PB2	PC2
Gate input	PB7	PB3	PC3

There are three duty cycles available for the timer/counter output: pulse, one-short, and square -wave. Fig. 4 shows the counter/timer waveforms. When tte Pulse mode is specified, the output goes High for one clock cycle, beginning when the down--counter leaves the count of 1. In the One-Shot mode, the output goes High when the counter/timer is triggered and and goes Low when the down-counter reaches 0. When the square -wave output duty cycle is specified, the counter/timer goes through two full sequences for each cycle. The initial trigger causes the down-counter to be loaded and the normal countdown sequence to begin. If a 1 count is detected on the down-counter's clocking edge, the output goes High and the time constant value is reloaded. On the clocking edge, when both the down-counter and the output are 1's, the output is pulled back Low.

The Countinuous/Single Cycle ($C/\overline{SC}$) bit in the Mode Specification register controls operation of the down-counter when it reaches terminal count. If $C/\overline{SC}$ is 0 when a terminal count is reached, the countdown sequence stops. If the $C/\overline{SC}$ bit is 1 each time the countdown counter reaches 1, the next cycle causes the time constant value to be reloaded. The time constant value may be changed by the CPU, and on reload, the new time constant value is loaded.

Counter/timer operations require loading the time constant value in the Time Constant register and initiating the countdown sequence by loading the down-counter with the time constant value. The Time Constant register is accessed as two 8-bit registers. The registers are readable as well as writable, and the access order is irrelevant. A 0 in the Time Constant register specifies a time constant of 65,536. The down-counter is loaded in one of three ways :

(1) By writing a 1 to the Trigger Command Bit (TCB : write-only),
(2) On the rising edge of the external trigger input, or,
(3) For Counter/Timer 2 only, on the rising edge of Counter/Timer 1's internal output if the counters are linked via the trigger input.

Once the down-counter is loaded, the countdown sequence continues toward terminal count as long as all the counter/timers' hardware and software gate inputs are High. If any of the gate inputs goes Low (0), the countdown halts. It resumes when all gate inputs are 1 again.

The reaction to triggers occurring during a countdown sequence is determined by the state of the Retrigger Enable Bit (REB) in the Mode Specification register. If REB is 0, retriggers are ignored and the countdown continues normally. If REB is 1, each trigger causes the down-counter to be reloaded and the count-down sequence starts over again. If the output is programmed in the Square -Wave mode, retrigger causes the sequence to start over from the initial load of the time constant.

The rate at which the down-countor counts is determined by the mode of the counter/timer. In the Timer mode (the External Count Enable [ECE] bit is 0), the down-counter is clocked internally by a signal that is half the frequency of the PCLK input to the chip. In the Counter mode (ECE is 1), the down-counter is decremented on the rising edge of the counter/timer's counter input.

Each time the counter reaches terminal count, its Interrupt Pending (IP) bit is set to 1, and if interrupts are enabled (IE=1), an interrupt is generated. If a terminal count occurs while IP is already set, an internal error flag is set. As soon as IP is cleared, it is forced to a 1 along with the Interrupt Error (ERR) flag. Errors that occur after the internal flag is set are ignored.

The state of the down-counter can determined in two ways :

(1) By reading the contents of the down-counter via the Current Count register, or
(2) By testing the Count In Progress (CIP) status bit in the Command Status register.

The CIP status bit is set when the down-counter is loaded ; it is reset when the down-counter reaches 0. The Current Count register is a 16-bit register, accessible as two 8-bit registers, which mirrors the contents of the down-counter. This register can be read anytime. However, reading the register is asynchronous to the counter's counting, and the value returned is valid only if the counter is stopped. The down-counter can be reliably read "on the fly" by the first writing of a 1 to the Read Counter Control (RCC) bit in the counter/timer's Command and Status register. This freezes the value in the Current Count register until a read of the least significant byte is performed.

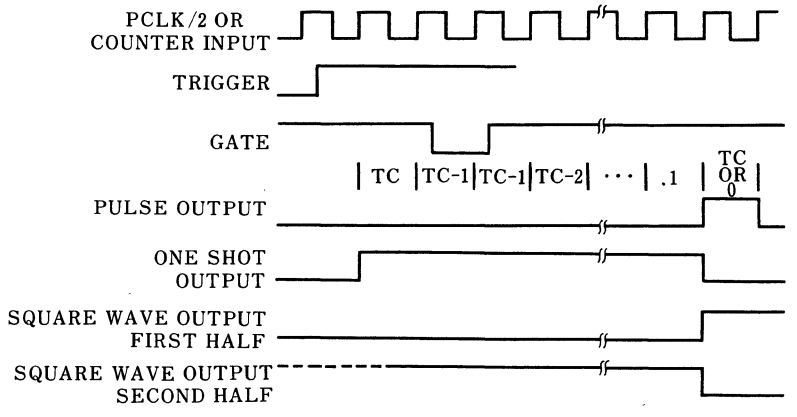
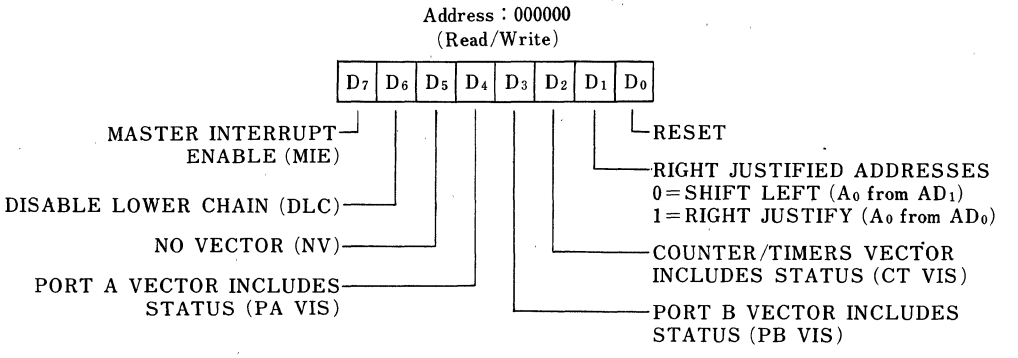


Fig. 4 Counter/timer waveforms

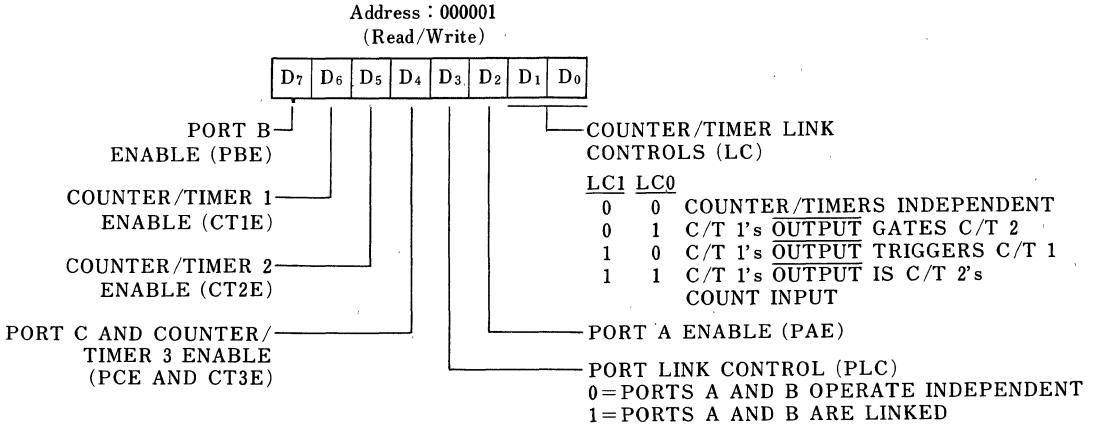
■ Internal Registers

The followings illustrate the contents of the Registers and, in addition, give to register address summary

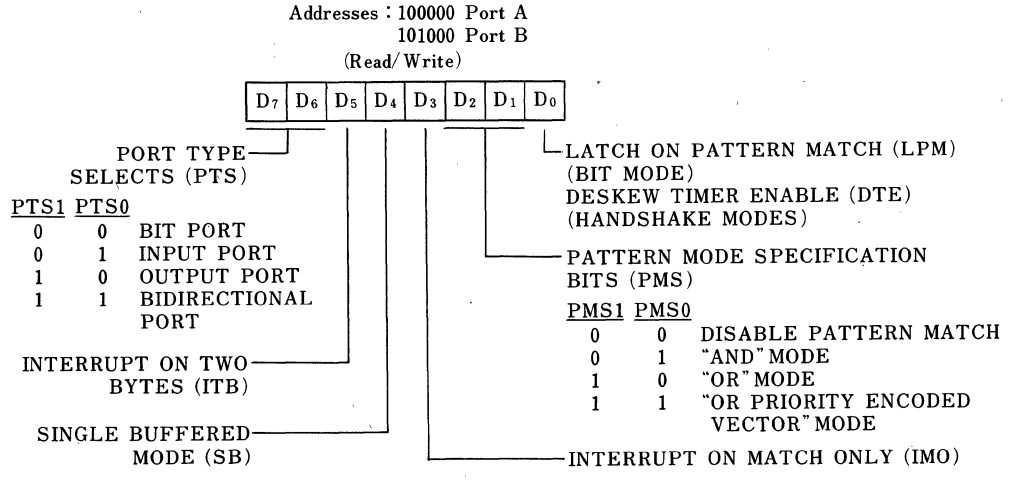
- **Master Interrupt Control Register (MICR)**



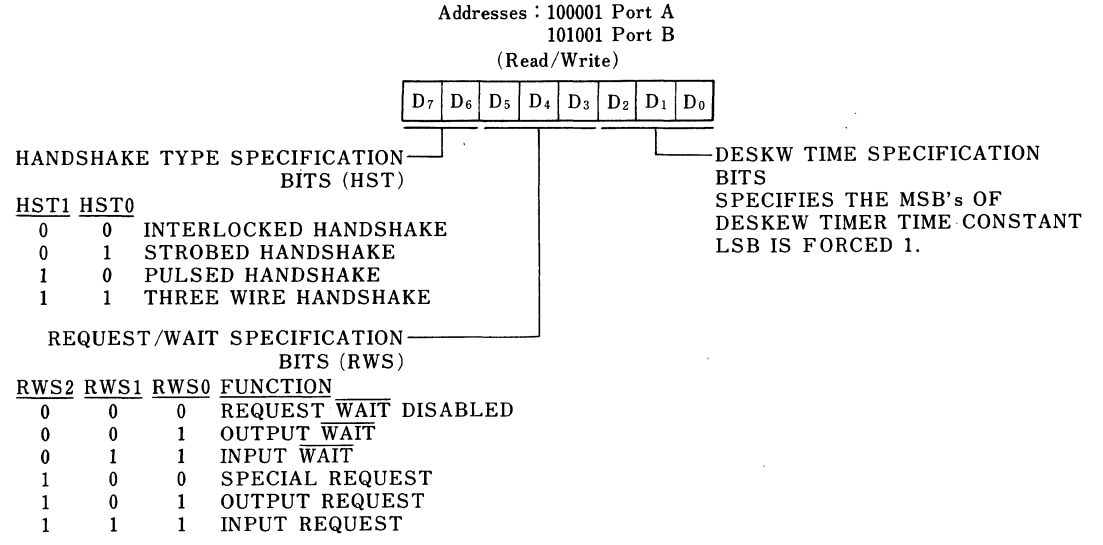
- **Master Configuration Control Register (MCCR)**



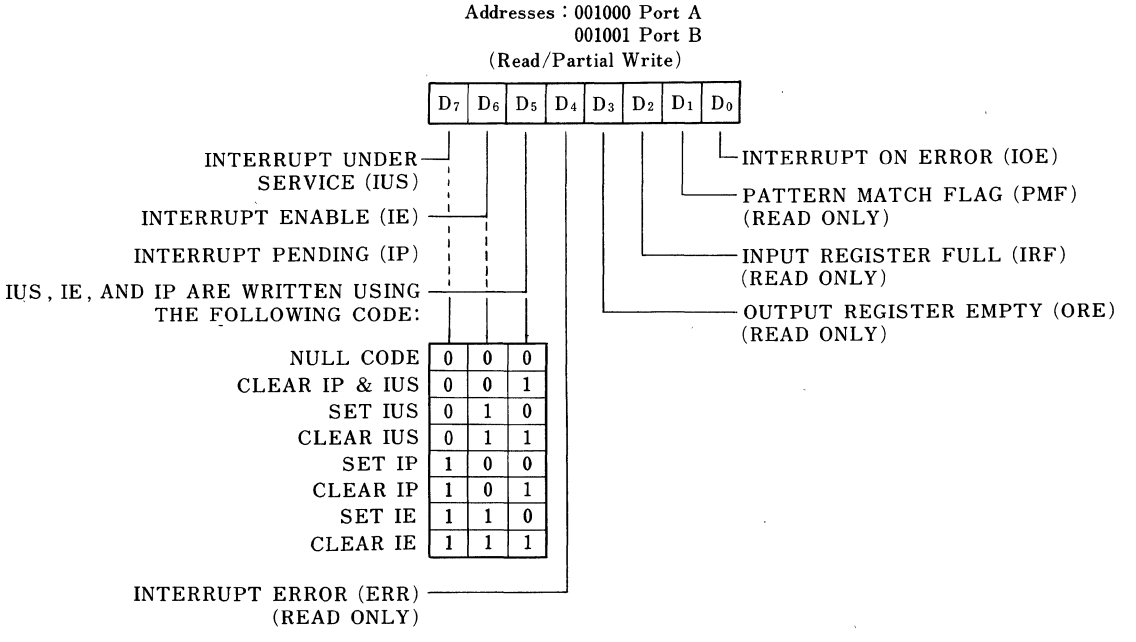
- **Port Mode Specification Registers (PMSR)**



- **Port Handshake Specification Registers (PHSR)**

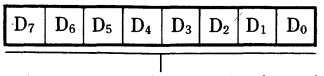


- **Port Command and Status Registers (PCSR)**



● Data Path Polarity Registers (DPPR)

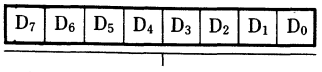
Addresses: 100010 Port A
101010 Port B
000101 Port C (4 LSBs only)
(Read/Write)



DATA PATH POLARITY (DPP)
0 = NON-INVERTING
1 = INVERTING

● Special I/O Control Registers (SIOCR)

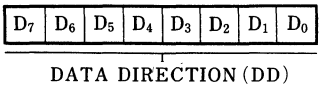
Addresses: 100100 Port A
101100 Port B
000111 Port C (4 LSBs only)
(Read/Write)



SPECIAL INPUT/OUTPUT (SIO)
0 = NORMAL INPUT OR OUTPUT
1 = OUTPUT WITH OPEN DRAIN OR
INPUT WITH 1's CATCHER

● Data Direction Registers (DDR)

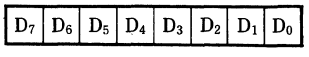
Addresses: 100011 Port A
101011 Port B
000110 Port C (4 LSBs only)
(Read/Write)



DATA DIRECTION (DD)
0 = OUTPUT BIT
1 = INPUT BIT

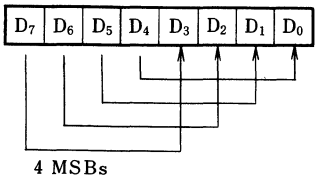
● Port Data Registers (PDR)

Addresses: 001101 Port A
001110 Port B
(Read/Write)



● Port C Data Register (PCDR)

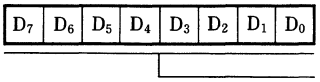
Address: 001111
(Read/Write)



0 = WRITING OF CORRESPONDING LSS ENABLED
1 = WRITING OF CORRESPONDING LSS INHIBITED
(READ RETURNS 1)

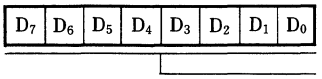
● Pattern Polarity Registers (PPR)

Addresses: 100101 Port A
101101 Port B
(Read/Write)



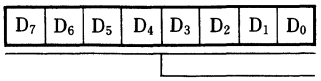
● Pattern Transition Registers (PTR)

Addresses: 100110 Port A
101110 Port B
(Read/Write)



● Pattern Mask Registers (PMR)

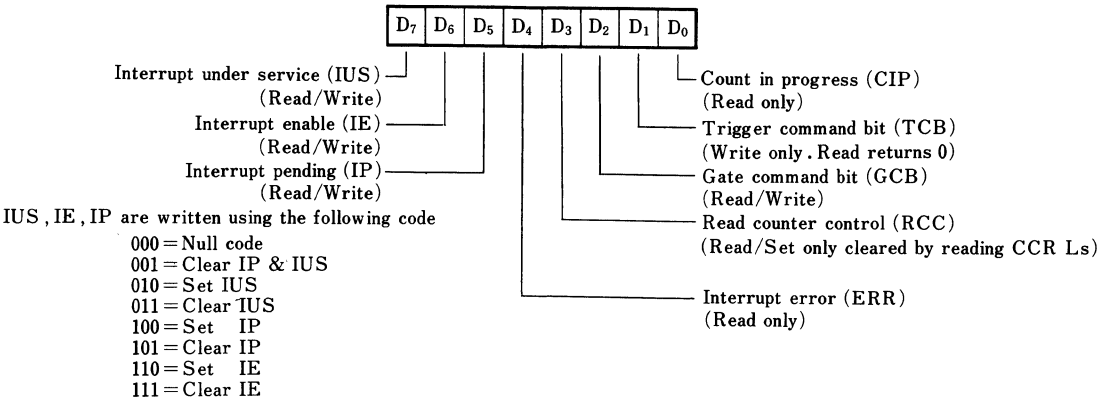
Addresses: 100111 Port A
101111 Port B
(Read/Write)



PM	PT	PP	PATTERN SPECIFICATION
0	0	×	BIT MASKED OFF
0	1	×	ANY TRANSITION
1	0	0	ZERO
1	0	1	ONE
1	1	0	ONE-TO-ZERO TRANSITION (↘)
1	1	1	ZERO-TO-ONE TRANSITION (↗)

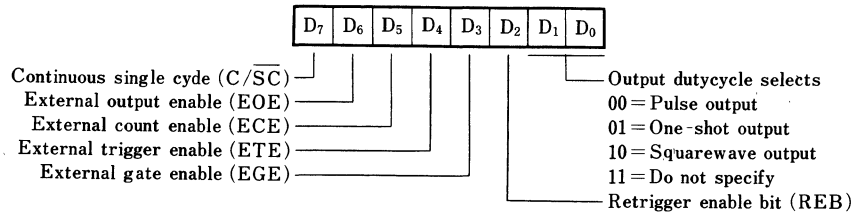
● Counter/Timer Command and Status Registers (CTCSR)

Addresses 0 0 1 0 1 0 Counter/Timer 1
0 0 1 0 1 1 Counter/Timer 2
0 0 1 1 0 0 Counter/Timer 3
(Read/Partial Write)



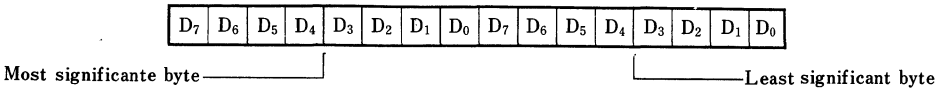
● Counter/Timer Mode Specification Registers (CTMSR)

Addresses 0 1 1 1 0 0 Counter/Timer 1
0 1 1 1 0 1 Counter/Timer 2
0 1 1 1 1 0 Counter/Timer 3
(Read/Write)



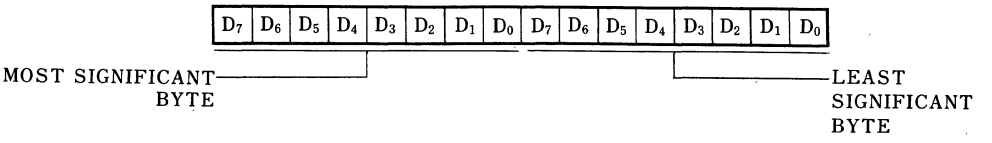
● Counter/Timer Current Count Registers (CTCCR)

Address 0 1 0 0 0 0 Counter/Timer 1's MSB
0 1 0 0 0 1 Counter/Timer 1's LSB
0 1 0 0 1 0 Counter/Timer 2's MSB
0 1 0 0 1 1 Counter/Timer 2's LSB
0 1 0 1 0 0 Counter/Timer 3's MSB
0 1 0 1 0 1 Counter/Timer 3's LSB
(Read only)



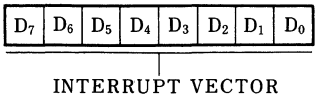
● Counter/Timer Time Constant Registers (CTTCR)

Addresses: 010110 Counter/Timer 1's MSB
010111 Counter/Timer 1's LSB
011000 Counter/Timer 2's MSB
011001 Counter/Timer 2's LSB
011010 Counter/Timer 3's MSB
011011 Counter/Timer 3's LSB
(Read/Write)



● Interrupt Vector Register (IVR)

Addresses: 000010 Port A
000011 Port B
000100 Counter/Timers
(Read/Write)



● Counter/Timer Status

D_2	D_1	
0	0	C/T3
0	1	C/T2
1	0	C/T1
1	1	Error

● Port Vector Status

(1) P encoded vector mode

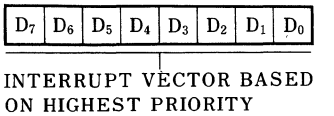
D_3	D_2	D_1	
×	×	×	Number of highest priority bit with a watch

(2) All other modes

D_3	D_2	D_1	
ORE	IRF	PMF	Normal
0	0	0	Error

● Current Vector Register (CVR)

Address: 011111
(Read Only)



INTERRUPT VECTOR BASED ON HIGHEST PRIORITY UNMASKED IP.
IF NO INTERRUPT PENDING ALL 1's OUTPUT.

LH8038/LH8038A Z8038/Z8038A FIO Input/Output Interface Unit

■ Description

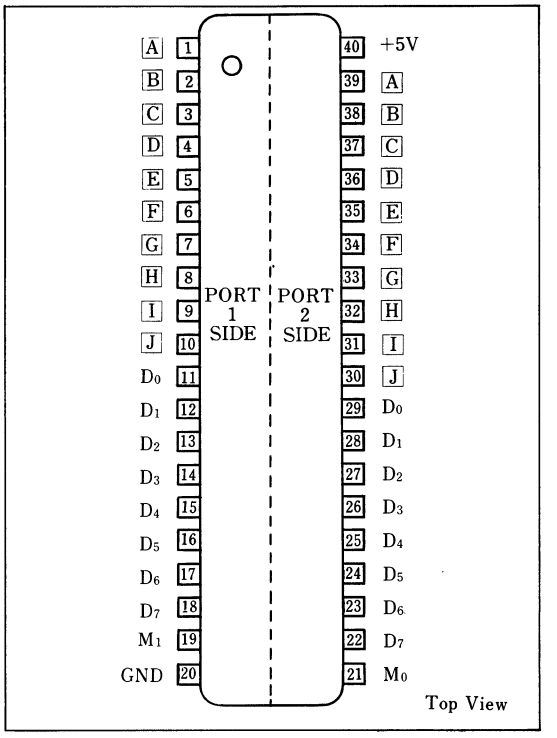
The LH8038 Z8038 FIO provides an asynchronous 128 byte FIFO buffer between two CPUs or between a CPU and a peripheral device. This buffer interface expands to a 16-bit or wider data path and expands in depth to add as many FIFOs (and an additional LH8038) as are needed.

The LH8038 manages data transfers by assuming Z-BUS, non-Z-BUS microprocessor (a generalized microprocessor interface), Interlocked 2-Wire Handshake, and 3-Wire Handshake operating modes. These modes interface dissimilar CPUs or CPUs and peripherals running under differing speeds or protocols, allowing asynchronous data transactions and improving I/O overhead by as much as two orders of magnitude.

The LH8038 supports the Z-BUS interrupt protocols, generating seven sources of interrupts upon any of the following events : a write to a message register, change in data direction, pattern match, status match, over/underflow error, buffer full and buffer empty status. Each interrupt source can be enabled or disabled, and can also place an interrupt vector on the port address/data lines.

The LH8038A Z8038A FIO is the high speed version which can operate at 6MHz system clock.

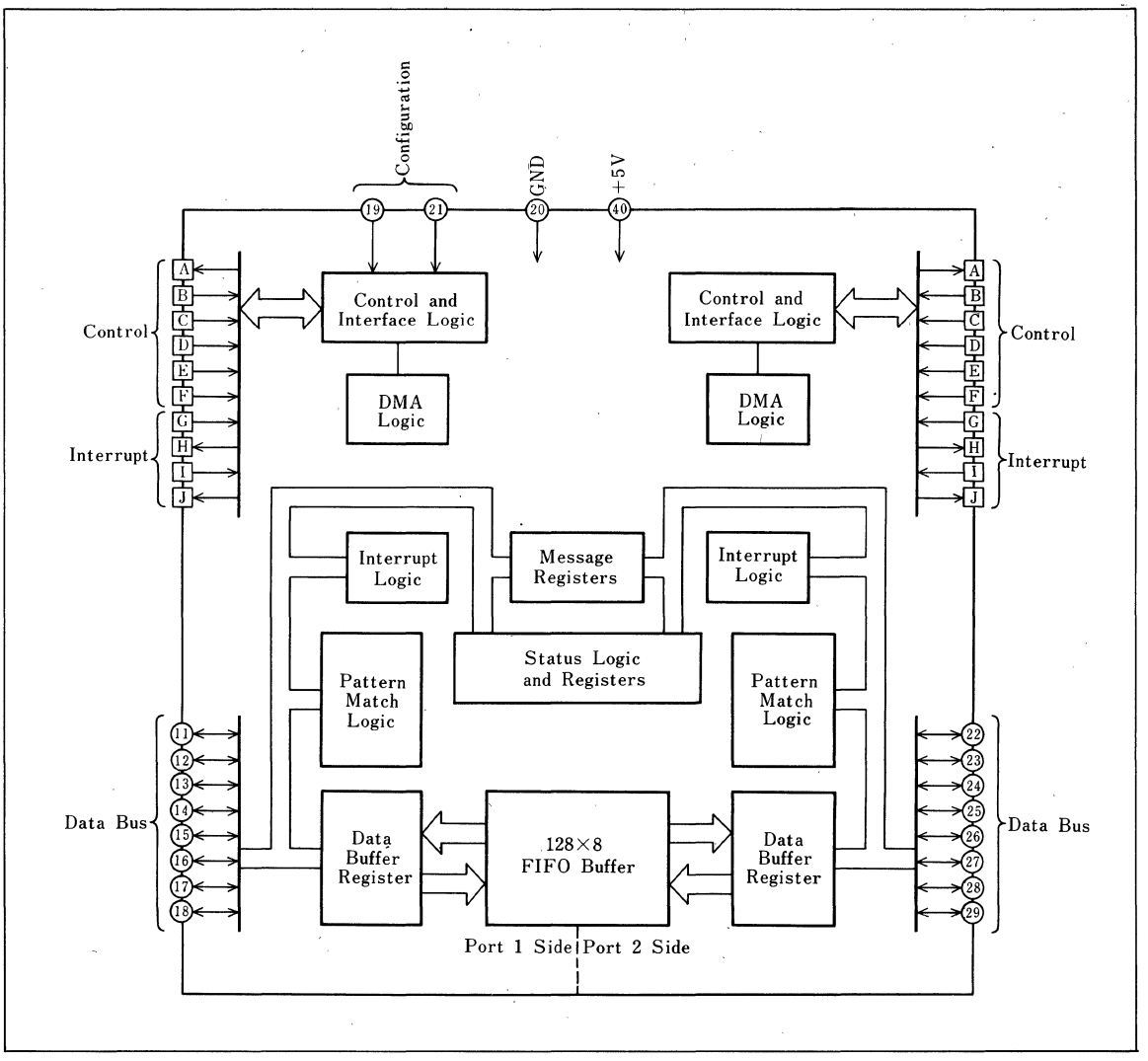
■ Pin Connections



■ Features

1. 128-byte FIFO buffer provides asynchronous bidirectional CPU/CPU or CPU/peripheral interface, expandable to any width in byte increments by use of multiple FIOs.
2. Interlocked 2-Wire or 3-Wire Handshake logic port mode ; Z-BUS or non-Z-BUS interface.
3. Pattern-recognition logic stops DMA transfers and/or interrupts CPU ; preset byte count can initiate variable-length DMA transfers.
4. Seven sources of vectored/nonvectored interrupt which include pattern-match, byte count, empty or full buffer status ; a dedicated "mailbox" register with interrupt capability provides CPU/CPU communication.
5. REQUEST/WAIT lines control high-speed data transfers.
6. All functions are software controlled via directly addressable read/write registers.

■ Block Diagram



■ Pin Description

(1) Pins common to both ports 1 and 2

Pin	Pin signal	Meaning	I/O	Function
M_0	M_0	Multimicro output	O	M_1 and M_0 program Port 1 side
M_1	M_1	Multimicro input	I	CPU interface

(2) Z-bus low byte mode

Pin	Pin signal	Meaning	I/O	Function
$D_0 \sim D_7$	$AD_0 \sim AD_7$	Address/data bus	Bidirectional 3-state	Multiplexed bidirectional bus, Z-BUS compatible
A	$\overline{REQ}/\overline{WAIT}$	Request/wait	O	Active low. open-drain output with $\overline{WAIT}$selected ; REQUEST line for DMA transfer ; $\overline{WAIT}$ line for data transfers to and from CPU.
B	$\overline{DMASTB}$	DMA strobe	I	Active low. Provides timing for data transfer to and from the FIFO buffer.
C	$\overline{DS}$	Data strobe	I	Active low. Provides timing for data transfer to or from Z-FIO.
D	$R/\overline{W}$	Read/write	I	Active high signals CPU to head from Z-FIO ; active Low signals CPU to write to Z-FIO.
E	$\overline{CS}$	Chip select	I	Active low. Enables Z-FIO. Latched on the rising edge of $\overline{AS}$.
F	$\overline{AS}$	Address strobe	I	Active low. Addresses. $\overline{CS}$ and $\overline{INTACK}$ are sampled while $\overline{AS}$ is Low.
G	$\overline{INTACK}$	Interrupt acknowledge	I	Active low. Latched on the rising edge of $\overline{AS}$.
H	IEO	Interrupt enable output	O	Active high. Sends interrupt enable to lower priority device IEI pin.
I	IEI	Interrupt enable input	I	Active high. Receives interrupt enable from higher priority device IEI pin.
J	$\overline{INT}$	Interrupt request	O	Active low, open-drain output. Interrupt request signal to CPU.

(3) Z-bus high byte mode

Pin	Pin signal	Meaning	I/O	Function
$D_0 \sim D_7$	$AD_0 \sim AD_7$	Address/data bus	Bidirectional 3-state I	Multiplexed bidirectional bus, Z-BUS compatible.
A	$\overline{REQ}/\overline{WAIT}$	Request/wait	O	Active low, open-drain output when $\overline{WAIT}$ selected ; REQUEST line for DMA transfer ; $\overline{WAIT}$ line for data transfers to and from CPU.
B	$\overline{DMASTB}$	DMA strobe	I	Active low. Strobes DMA data to and from the FIFO buffer.
C	$\overline{DS}$	Data strobe	I	Active low. Provides timing for data transfer to or from Z-FIO.
D	$R/\overline{W}$	Read/write	I	Active high signals CPU to read from Z-FIO ; active low signal CPU to write to Z-FIO.
E	$\overline{CS}$	Chip select	I	Active low. Enables Z-FIO. Latched on the rising edge of $\overline{AS}$
F	$\overline{AS}$	Address strobl	I	Active low. Addresses, $\overline{CS}$ and $\overline{INTACK}$ are sampled while $\overline{AS}$ is low.
G~J	$A_0 \sim A_3$	Address bits	I	Active high. Specify Z=FIO internal registers.

(4) Non-Z-bus mode

Pin	Pin signal	Meaning	I/O	Function
$D_0 \sim D_7$	$D_0 \sim D_7$	Data bus	Bidirectional 3-state	Bidirectional data bus.
A	$\overline{REQ}/\overline{WAIT}$	Request/wait	O	Active low, open-drain output when $\overline{WAIT}$ is selected ; REQUEST line for DMA transfer ; $\overline{WAIT}$ line for data transfer to and from CPU.
B	$\overline{DACK}$	DMA acknowledge	I	Active low. DMA acknowledge signal.
C	$\overline{RD}$	Read	I	Active low. Timing signal for reading.
D	$\overline{WR}$	Write	I	Active low. Timing signal for writing.
E	$\overline{CE}$	Chip select	I	Active low. Signal that is used to select Z-FIO.
F	$C/\overline{D}$	Control/data	I	Active high identifies control byte on D_0-D_7, active low identifies data byte on D_0-D_7
G	$\overline{INTACK}$	Interrupt acknowledge	I	Active low. acknowledges an interrupt.
H	IEO	Interrupt enable output	O	Active high. Sends interrupt enable to lower priority device IEI pin.
I	IEI	Interrupt enable input	I	Active high. Receives interrupt enable from higher priority device IEO signal.
J	$\overline{INT}$	Interrupt	O	Active low, open drain. Signals Z-FIO interrupt to CPU.

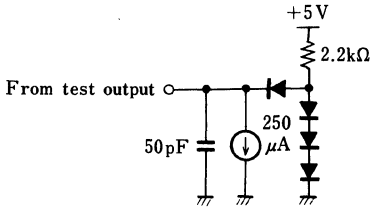
(5) Port 2-I/O port mode

Pin	Pin signal	Meaning	I/O	Function
$D_0 \sim D_7$	$D_0 \sim D_7$	Data bus	Bidirectional 3-state	Bidirectional data bus.
A	RFD/$\overline{DAV}$	Ready for data/ data available	O	For input handshake, RFD (active High) signals that Z-FIO is ready to receive data. For output handshake, $\overline{DAV}$ (active Low) signals that output data is valid
B	$\overline{ACKIN}$	Acknowledge input	I	Active low. Signals that input data is valid in the case of input handshake or that output data is received by peripherals in the case of output handshake.
B	$\overline{DAV}$/DAC	Data available/ data accepted	I	For input handshake, $\overline{DAV}$ (active low) signals that input data is valid. For output handshake, DAC (active high) signals that listener has received data.
C	FULL	Full	O	Active high, open drain. Signals that FIFO buffer is full.
C	DAC/RFD	Data accepted/ ready for data	I/O	Both active high. For input handshake, DAC (an output) signals that data has been received from talker. For output handshake, RFD (an input) signals that the listeners are ready for data.
D	EMPTY	Empty	O	Active high, open drain. Signals that FIFO buffer is empty.
E	$\overline{CLEAR}$	Clear	I/O	Active low. Can clear data from FIFO buffer in the case of input.
F	DATA DIR	Data direction	I/O	Data direction is controllable for input. Active high signals data input to ports 2 ; Low signals data output from Port 2.
G	IN_0	Input	I	Input line to bit 0 (D_0) of control register 3.
H	OUT_1	Output	O	Output line from bit (D_1) of control register 3.
I	$\overline{OE}$	Output enable	O	Active low. When low, enables bus drivers. When high, floats bus drivers at high inpedance.
J	OUT_3	Output	O	Output line from bit 3 (D_3) of control register 3.

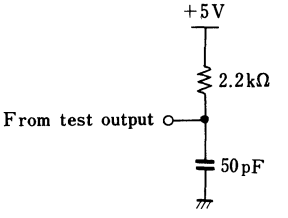
■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage*	V_{IN}	−0.3～+7	V
Output voltage*	V_{OUT}	−0.3～+7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

Note The maximum applicable voltage on any pin with respect to GND.



Standard test load



Open-drain test load

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input high voltage	V_{IH}		2	V_{CC}+0.3	V
Input low voltage	V_{IL}		−0.3	0.8	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4		V
Output low voltage	V_{OL}	I_{OL}=+2mA		0.4	V
		I_{OL}=+3.2mA		0.5	V
Input leakage current	$\lvert I_{IIL} \rvert$	0.4≦V_{IN}<2.4V		10	μA
Output leakage current	$\lvert I_{OL} \rvert$	0.4≦V_{OUT}≦2.4V		10	μA
Mode pins input leakage	I_{LM}	0<V_{IN}<V_{CC}	−100	10	μA
Current consumption	I_{CC}			200	mA

■ Capacitance

(f=1MHz, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_{IN}	Unmeasured pins returned to ground		10	pF
Output capacitance	C_{OUT}			15	pF
Bidirectional capacitance	$C_{I/O}$			20	pF

■ Inputs

(f=1MHz, Ta=0～+70℃)

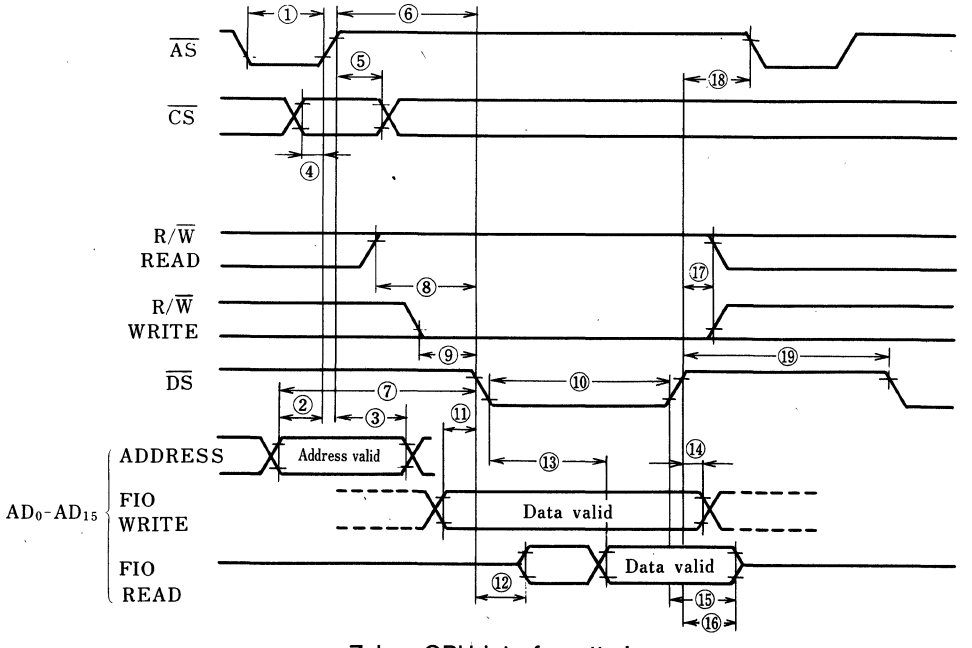
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Any input rise time	t_r			100	ns
Any input fall time	t_f			100	ns

■ AC Characteristics

(1) Z-bus CPU interface timing

No.	Symbol	Parameter	LH8038		LH8038A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TwAS	$\overline{AS}$ low width	70		50		ns	1
2	TsA (AS)	Address to $\overline{AS}$ ↑ setup time	30		10		ns	1
3	ThA (AS)	Address to $\overline{AS}$ ↑ hold time	50		30		ns	1
4	TsCSO (AS)	$\overline{CS}$ to $\overline{AS}$ ↑ setup time	0		0		ns	1
5	ThCSO (AS)	$\overline{CS}$ to $\overline{AS}$ ↑ hold time	60		40		ns	1
6	TdAS (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ delay	60		40		ns	1
7	TsA (DS)	Address to $\overline{DS}$ ↓ setup time (with $\overline{AS}$ ↑ to $\overline{DS}$ ↓ =60ns)	120		100		ns	
8	TsRWR (DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ setup time	100		80		ns	
9	TsRWW (DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ setup time	0		0		ns	
10	TwDS	$\overline{DS}$ low width	390		250		ns	
11	TsDW (DSf)	Write data to $\overline{DS}$ ↓ setup time	30		20		ns	
12	TdDS (DRV)	$\overline{DS}$ (Read) ↓ to address data bus driven delay	0		0		ns	
13	TdDSf (DR)	$\overline{DS}$ ↓ to read data valid delay		250		180	ns	
14	ThDW (DS)	Write data to $\overline{DS}$ ↑ hold time	30		20		ns	
15	TdDSr (DR)	$\overline{DS}$ ↑ to read data not valid delay	0		0		ns	
16	TdDS (DRz)	$\overline{DS}$ ↑ to read data float delay		70		45	ns	2
17	ThRW (DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ hold time	55		40		ns	
18	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay	50		25		ns	
19	Trc	Valid access recovery time	1000		650		ns	3

Note "↑" indicates a rising edge and "↓" a falling edge.
Note 1 Parameter does not apply to interrupt acknowledge transactions.
Note 2 Float delay is measured to the time when the output has changed 0.5 V from steady state with minimum ac load and maximum dc load.
Note 3 This is the delay from $\overline{DS}$ of one CIO access to $\overline{DS}$ of another FIO access (either read or write).

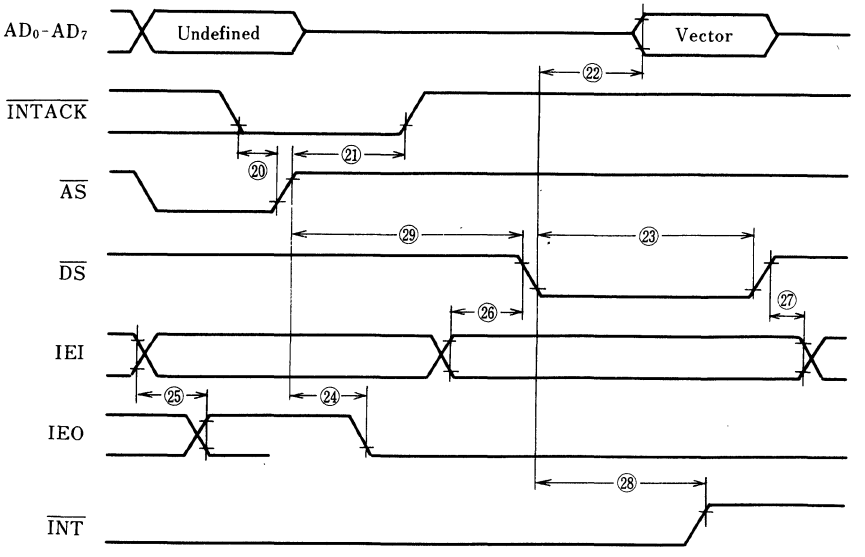


Z-bus CPU interface ttming

(2) Z-bus CPU interrupt acknowledge timing

No.	Symbol	Parameter	LH8038		LH8038A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
20	TsIA (AS)	$\overline{\text{INTACK}}$ low setup time to $\overline{\text{AS}}$ ↑	0		0		ns	
21	ThIA (AS)	$\overline{\text{INTACK}}$ low hold time to $\overline{\text{AS}}$ ↑	250		250		ns	
22	TdDSA (DR)	$\overline{\text{DS}}$ (acknowledge) ↓ to vector valid delay		250		180	ns	
23	TwDSA	$\overline{\text{DS}}$ (acknowledge) low width	390		250		ns	
24	TdAS (IEO)	$\overline{\text{AS}}$ ↑ to IEO ↓ delay ($\overline{\text{INTACK}}$ cycle)		350		250	ns	4
25	TdIEI (IEO)	IEI to $\overline{\text{IEO}}$ delay		150		100	ns	4
26	TsIEI (DSA)	IEI to $\overline{\text{DS}}$ (acknowledge) ↓ setup time	100		70		ns	
27	ThIEI (DSA)	IEI to $\overline{\text{DS}}$ (acknowledge) ↑ hold time	50		30		ns	4
28	TdDS (INT)	$\overline{\text{DS}}$ ($\overline{\text{INTACK}}$ cycle) to $\overline{\text{INT}}$ delay		900		800	ns	
29	TdDCST	Interrupt daisy chain settle time					ns	4

Note 4: The parameters for the devices in any particular daisy chain must meet the following constraint : The delay from $\overline{\text{AS}}$ to $\overline{\text{DS}}$ must be greater than the sum of TdAS (IEO) for the highest priority peripheral, TsIEI (DSA) for the lowest priority peripheral and TdIEI (IEO) for each peripheral, separating them in the chain.

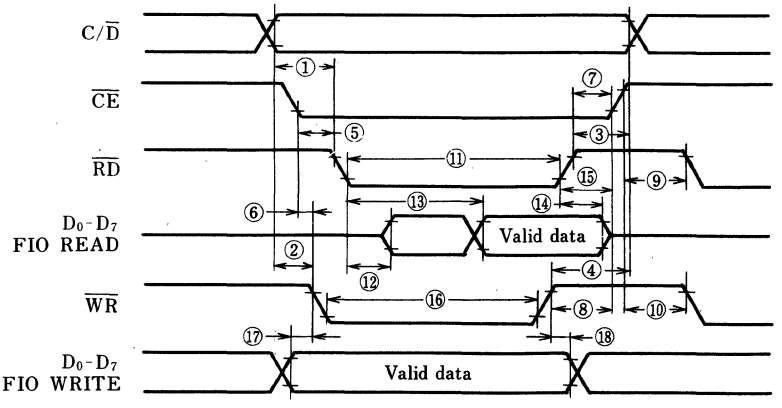


Z-bus CPU interrupt acknowledge timing

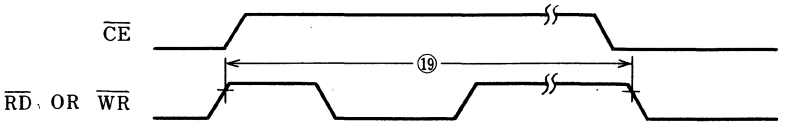
(3) Non-Z-bus CPU interface timing

No.	Symbol	Parameter	LH8038		LH8038A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TsCD (RD)	C/$\overline{D}$ setup time to $\overline{RD}$ ↓	80		80		ns	5
2	TsCD (WR)	C/$\overline{D}$ setup time to $\overline{WR}$ ↓	80		80		ns	
3	ThCD (RD)	C/$\overline{D}$ hold time to $\overline{RD}$ ↑	0		0		ns	5
4	ThCD (WR)	C/$\overline{D}$ hold time to $\overline{WR}$ ↑	0		0		ns	
5	TsCEI (RD)	$\overline{CE}$ low setup time to $\overline{RD}$ ↓	0		0		ns	5
6	TsCEI (WR)	$\overline{CE}$ low setup time to $\overline{WR}$ ↓	0		0		ns	
7	ThCEI (RD)	$\overline{CE}$ low hold time to $\overline{RD}$ ↑	0		0		ns	5
8	ThCEI (WR)	$\overline{CE}$ low hold time to $\overline{WR}$ ↑	0		0		ns	
9	TsCEh (RD)	$\overline{CE}$ high setup time to $\overline{RD}$ ↓	100		70		ns	5
10	TsCEh (WR)	$\overline{CE}$ high setup time to $\overline{WR}$ ↓	100		70		ns	
11	TwRD1	$\overline{RD}$ low width	390		250		ns	
12	TdRD (DRA)	$\overline{RD}$ ↓ to read data active delay	0		0		ns	
13	TdRDf (DR)	$\overline{RD}$ ↓ to valid data delay		250		180	ns	
14	TdRDr (DR)	$\overline{RD}$ ↑ to read data not valid delay	0		0		ns	
15	TdRD (DRz)	$\overline{RD}$ ↑ to data bus float delay		70		45	ns	6
16	TwWR1	$\overline{WR}$ low width	390		250		ns	
17	TsDW (WR)	Data setup time to $\overline{WR}$ ↓	0		0		ns	
18	ThDW (WR)	Data hold time to $\overline{WR}$ ↑	30		20		ns	
19	Trc	Valid access recovery time	1000		650		ns	7

Note 5: Parameter does not apply to interrupt acknowledge transactions.
Note 6: Float delay is measured to the time the output has changed 0.5 V from steady state with minimum ac load and maximum dc load.
Note 7: This is the delay from $\overline{RD}$ ↑ to $\overline{WR}$ ↑ of one FIO access to $\overline{RD}$ ↓ or $\overline{WR}$ ↓ of another FIO access.



Non-Z-bus CPU interface timing

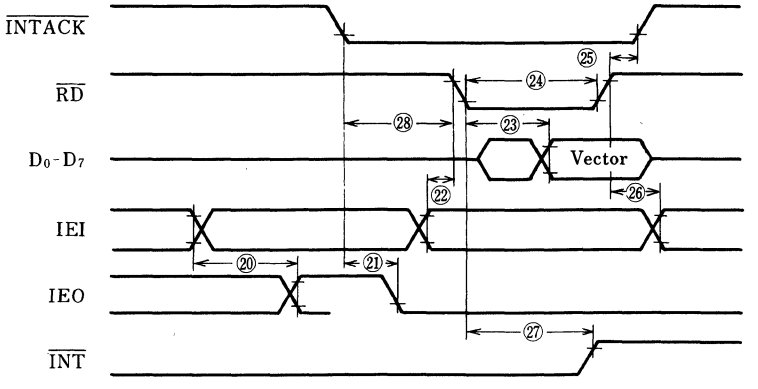


Non-Z-bus interface timing

(4) Non-Z-bus interrupt acknowledge timing

No.	Symbol	Parameter	LH8038		LH8038A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
20	TdIEI (IEO)	IEI to IEO delay		150		100	ns	8
21	TdI (IEO)	$\overline{INTACK}$ ↓ to IEO ↓ delay		350		250	ns	8
22	TsIEI (RDA)	IEI setup time to $\overline{RD}$ (acknowledge) ↓	100		70		ns	8
23	TdRD (DR)	$\overline{RD}$ ↓ to vector valid delay		250		180	ns	
24	TwRDI (IA)	Read low width (interupt acknowledge)	390		250		ns	
25	ThIA (RD)	$\overline{INTACK}$ low hold time to $\overline{RD}$ ↑	30		20		ns	
26	ThIEI (RD)	IEI hold time to $\overline{RD}$ ↑	20		10		ns	
27	TdRD (INT)	$\overline{RD}$ ↑ to $\overline{INT}$ ↑ delay		900		800	ns	
28	TdDCST	Interrupt daisy chain settle time	350		250		ns	8

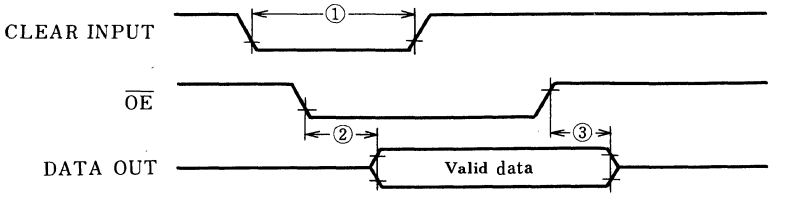
Note 8: The parameter for the devices in any particular daisy chain must meet the following constraint : The delay from $\overline{INTAC}$ ↓ to $\overline{RD}$ ↓ must be greater than the sum of TdINA (IEO) for the highest priority peripheral, TsIEI (RD) for the lowest priority peripheral, and TdIEI (IEO) for each peripheral separating them in the chain.



Non-Z-bus interrupt acknowledge timing

(5) Port 2 side operation

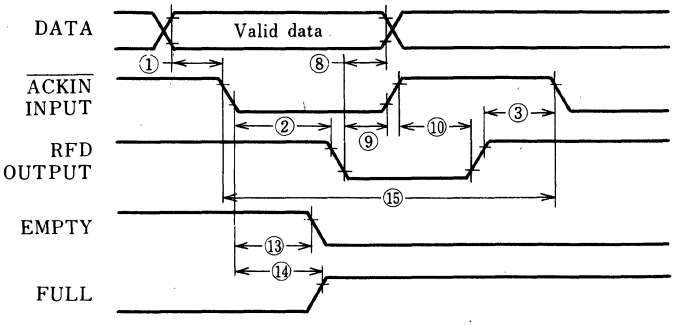
No.	Symbol	Parameter	LH3038		LH3038A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TwCLR	Width clear to reset FIFO	700		700		ns	
2	TdOE (DO)	$\overline{OE}$ ↓ to data bus driven	0		0		ns	
3	TdOE (DRZ)	$\overline{OE}$ ↑ to data bus float					ns	



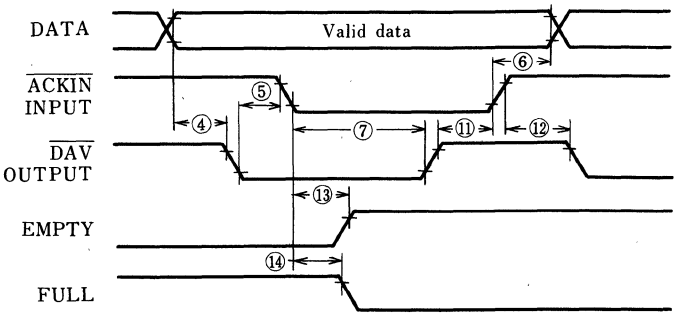
Port 2 side operation

(6) 2-wire handshake (port 2 side only) output

No.	Symbol	Parameter	LH8038		LH8038A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TsDI (ACK)	Data input to $\overline{ACKIN}$ ↓ setup time	50		50		ns	
2	TdACKf (RFD)	$\overline{ACKIN}$ ↓ to RFD ↓ delay	0	500	0	500	ns	
3	TdRFDr (ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ delay	0		0		ns	
4	TsDO (DAV)	Data output to $\overline{DAV}$ ↓ setup time	50		25		ns	
5	TdDAVf (ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ delay	0		0		ns	
6	ThDO (A+K)	Data output t to $\overline{ACKIN}$ hold time	50		50		ns	
7	TdACK (DAV)	$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ delay	0	500	0	500	ns	
8	ThDI (RFD)	Data input from RFD ↓ hold time	0		0		ns	
9	TdRFDf (ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ delay	0		0		ns	
10	TdACKr (RFD)	$\overline{ACKIN}$ ↑ to RFD ↑ delay	0	400	0	400	ns	
11	TdDAVr (ACK)	$\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑ delay	0		0		ns	
12	TdACKr (DAV)	$\overline{ACKIN}$ ↑ to $\overline{DAV}$ ↓ delay	0	800	0	800	ns	
13	TdACKf (EMPTY)	$\overline{ACKIN}$ ↓ to EMPTY ↑ delay	0		0		ns	
14	TdACKf (FULL)	$\overline{ACKIN}$ ↓ to FULL ↓ (FULL ↑) delay	0		0		ns	
15	TcACK	$\overline{ACKIN}$ cycle time	1		1		ns	



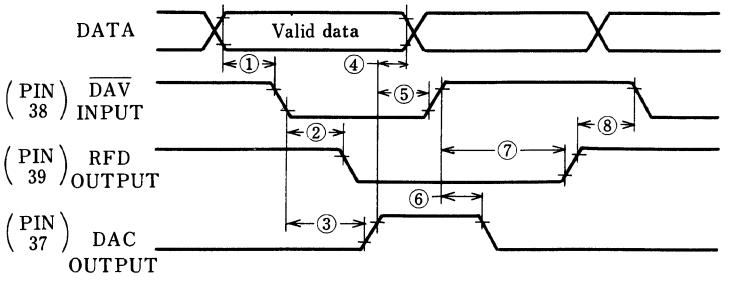
2-wire handshake (Port 2 side only) output



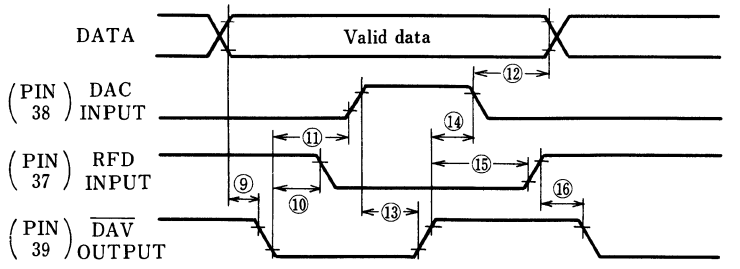
2-wire handshake (Port 2 side only) input

(7) 3-wire handshake timing

No.	Symbol	Parameter	LH3038		LH3038A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TsDI (DAV)	Data input to $\overline{DAV}$ ↓ setup time	50		50		ns	
2	TdDAVIf (RFD)	$\overline{DAV}$ ↓ to RFD ↓ delay	0	500	0	500	ns	
3	TdDAVIf (DAC)	$\overline{DAV}$ ↓ to DAC ↑ delay	0	500	0	500	ns	
4	ThDI (DAC)	Data input from DAC ↑ hold time	0		0		ns	
5	TdDACIr (DAV)	DAC ↑ to $\overline{DAV}$ ↑ delay	0		0		ns	
6	TdDAVIr (DAC)	$\overline{DAV}$ ↑ to DAC ↓ delay	0	500	0	500	ns	
7	TdDAVIr (RFD)	$\overline{DAV}$ ↑ to RFD ↑ delay	0	500	0	500	ns	
8	TdRFDI (DAV)	RFD ↑ to $\overline{DAV}$ ↓ delay	0		0		ns	
9	TsDO (DAC)	Data output to $\overline{DAV}$ ↓ setup time					ns	
10	TdDAVOf (RFD)	$\overline{DAV}$ ↓ to RFD ↓ delay	0		0		ns	
11	TdDAVOf (DAC)	$\overline{DAV}$ ↓ DAC ↑ delay	0		0		ns	
12	ThDO (DAC)	Data output from DAC ↑ hold time					ns	
13	TdDACOr (DAV)	DAC ↑ to $\overline{DAV}$ ↑ delay		400		400	ns	
14	TdDAVOr (DAC)	$\overline{DAV}$ ↑ to DAC ↓ delay	0		0		ns	
15	TdDAVOr (RFD)	$\overline{DAV}$ ↑ to RFD ↑ delay	0		0		ns	
16	TdRFDO (DAV)	RED ↑ to $\overline{DAV}$ ↓ delay	0	800	0	800	ns	



3-wire handshake (Port 2 side only) input



3-wire handshake (Port 2 side only) output

■ Operating Modes

KH 8038 operates in any of twelve combinations of operating modes, listed in Table 1. Port 1 functions in either the Z-bus or non-Z-bus microprocessor modes, while Port 2 functions in Z-BUS, non-Z-bus, Interlocked 2-Wire Handshake, and 3-Wire Handshake modes. Table 2 describes the signals and their corresponding pins in each of these modes.

The pins on the LH8038's Port 1 side are identical to those on the Port 2 side, except for two pins (M_0 and M_1), which select that port's operating mode. Port 2's operating mode is programmed by two bits (B0 and B1) in Port 1's Control register 0.

Table 1 Operating modes

Mode	M_1	M_2	B_1	B_0	Port 1	Port 2
0	0	0	0	0	Z-bus low byte	Z-bus low byte
1	0	0	0	1	Z-bus low byte	Non-Z-bus
2	0	0	1	0	Z-bus low byte	3-wire handshake
3	0	0	1	1	Z-bus low byte	2-wire handshake
4	0	1	0	0	Z-bus high byte	Z-bus high byte
5	0	1	0	1	Z-bus high byte	Non-Z-bus
6	0	1	1	0	Z-bus high byte	3-wire handshake
7	0	1	1	1	Z-bus high byte	2-wire handshake
8	1	0	0	0	Non-Z-bus	Z-bus low byte
9	1	0	0	1	Non-Z-bus	Non-Z-bus
10	1	0	1	0	Non-Z-bus	3-wire handshake
11	1	0	1	1	Non-Z-bus	2-wire handshake

Table 2 Pin assignments

Signal pins	Z-bus low byte	Z-bus high byte	Non-Z-bus	Interlocked HS port*	3-wire HS port*
A	$\overline{\text{REQ/WAIT}}$	$\overline{\text{REQ/WAIT}}$	$\overline{\text{REQ/WAIT}}$	$\overline{\text{RFD/DAV}}$	$\overline{\text{RFD/DAV}}$
B	$\overline{\text{DMASTB}}$	$\overline{\text{DMASTB}}$	$\overline{\text{DACK}}$	$\overline{\text{ACKIN}}$	$\overline{\text{DAV/DAC}}$
C	$\overline{\text{DS}}$	$\overline{\text{DS}}$	$\overline{\text{RD}}$	FULL	DAC/RFD
D	R/$\overline{\text{W}}$	R/$\overline{\text{W}}$	$\overline{\text{WR}}$	EMPTY	EMPTY
E	$\overline{\text{CS}}$	$\overline{\text{CS}}$	$\overline{\text{CE}}$	$\overline{\text{CLEAR}}$	$\overline{\text{CLEAR}}$
F	$\overline{\text{AS}}$	$\overline{\text{AS}}$	C/$\overline{\text{D}}$	DATA DIR	DATA DIR
G	$\overline{\text{INTACK}}$	A_0	$\overline{\text{INTACK}}$	IN_0	IN_0
H	IEO	A_1	IEO	$\overline{\text{OUT}}_1$	$\overline{\text{OUT}}_1$
I	IEI	A_2	IEI	$\overline{\text{OE}}$	$\overline{\text{OE}}$
J	$\overline{\text{INT}}$	A_3	$\overline{\text{INT}}$	OUT_3	OUT_3

Port 2 side only

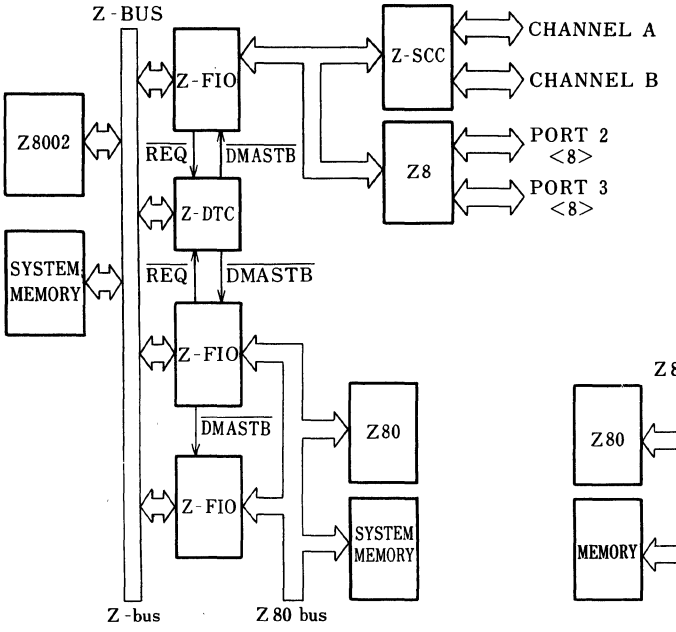


Fig. 1 CPU to CPU configuration

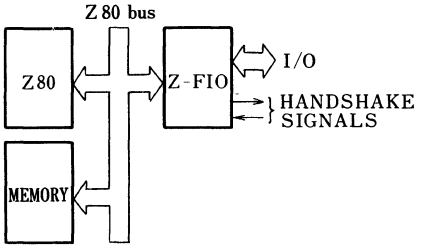


Fig. 2 CPU to I/O configuration

■ CPU Interface

The LH8038 is designed to work with both Z-bus and non-Z-bus-type CPUs on both Port 1 and Port 2. The Z-bus configuration interfaces CPUs with time-multiplexed address and data information on the same pins. The Z8001, Z8002, and Z8 are examples of this type of CPU. The $\overline{AS}$ (Address Strobe) pin is used to latch the address and chip select information sent out by the CPU. The R/$\overline{W}$ (Read/Write) pin and the $\overline{DS}$ (Data Strobe) pin are used for timing reads and writes from the CPU to the LH8038 (Fig. 3 and 4).

The non-Z-bus configuration is used for CPUs where the address and data buses are separate. An Example of this type of CPU is the Z80. The $\overline{RD}$ (Read) and $\overline{WR}$ (Write) pins are used to time reads and writes from the CPU to the FIO (Fig. 5 and 6). The C/$\overline{D}$ (Control/ Data) pin is used to directly access the FIFO buffer (C/$\overline{D}$ = Low) and to access the other register (C/$\overline{D}$ = High).

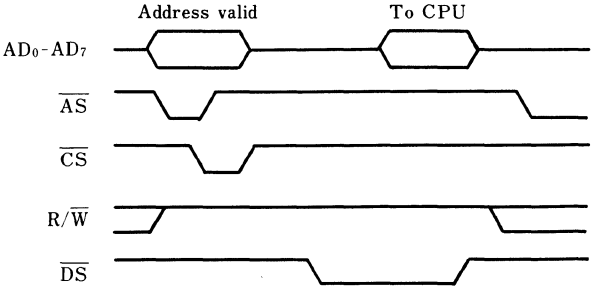


Fig. 3 Z-bus read cycle timing

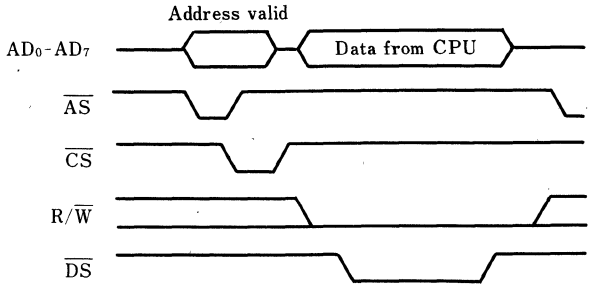


Fig. 4 Z-bus write cycle timing

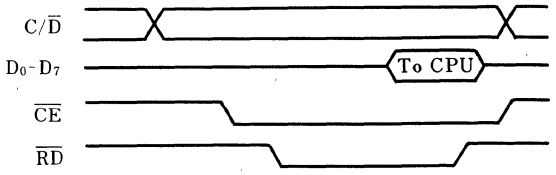


Fig. 5 Non-Z-bus read cycle timing

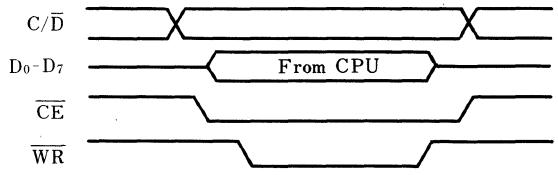


Fig. 6 Non-Z-bus write cycle timing

■ CPU-CPU Operation

(1) DMA operation

The LH8038 is particularly well suited to work with a DMA in both Z-bus and non-Z-bus modes. A data transfer between the LH8038 and system memory can take place durring every machine cycle on both sides of the LH8038 simultaneously.

(2) Message registers

Two CPUs can communicate through a dedicated "mailbox" register without involving the 128 × 8 bit FIFO buffer. This mailbox approach is useful for the transferring control parameters between the interfacing devices on either side of the LH8038 without using the FIFO buffer.

(3) Direction of data transfer operation

The Data Direction bit controls the direction of data transfer in the FIFO buffer. This bit reads correctly when read by either port's CPU. For example, if Port 1's CPU reads a 0 (CPU output) in its Data Direction bit, then Port 2's CPU reads a 1 (input to CPU) in its Data Direction bit.

■ CPU to I/O Operation

When Port 2 is programmed in the Interlocked 2-Wire Handshake mode or the 3-Wire Handshake mode, and Port 1 is programmed in Z-bus or non-Z-bus Microprocessor mode, the LH8038 interfaces a CPU and a peripheral device.

(1) Interlocked 2-wire handshake

In the Interlocked Handshake, the action of the LH8038 must be acknowledged by the other half of the handshake before the next action can take place. In output mode, Port 2 does not indicate that new data is available until the external device indicates it is ready for the data. Similarly, in input mode, Port 2 does not indicate that it is ready for new data until the data source (external device) indicates that the previous byte of the data is no longer available, thereby acknowledging Port 2's acceptance of the last byte by Port 2's Ready for Data Signal (RFD → High).

(2) 3-wire handshake

The 3-Wire Handshake is designed for applications in which one output port is communicating with many input ports simultaneously. It is essentially the same as the Interlocked Handshack, except that two signals are used to indicate that an input port is ready for new data or that it has accepted the present data. With 3-Wire Handshake, these lines (RFD, DAC) of many input ports can be bussed together with open-drain drivers and the output port knows when all of the ports are ready and have accepted the data. This handshake is the same handshake used in the in IEEE-488 Instruments. Since the port's direction can be changed under software control, bidirectional IEEE-488-type transfers can be performed.

(3) Data direction control

In CPU-to-I/O mode, the direction of data transfer can be controlled by the CPU side (Port 1) under software control. The data direction can also be determined by hardware control by defining the Data Direction pin of Port 2 as an input (Control Register 3, bit 5= 1).

For cascading purposes, the Data Direction pin can also be defied as an output (Control Register 3, bit 5 = 0) pin which reflects the current state of the Data Direction bit. It can then be used to control the direction of data transfer for other LH8038s or for external logic.

■ Programming

The programming of the LH 8038 is greatly simplified by the efficient grouping of the various operation modes in the control registers. Since all of the control registers are read/write, the need for maintaining thier image in system memory is eliminated. Also, the read/write feature of the registers aides in system debugging.

Each side of the LH 8038 has 16 registers. All 16 registers are used by the Port 1 side ;

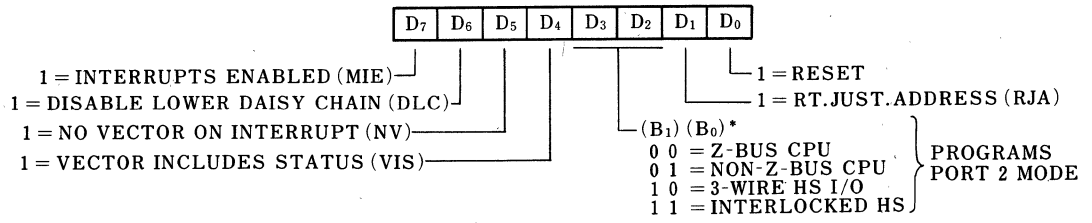
Table 1 Z-FIO register address summary

Non-Z-bus		D_7-D_4	D_3	D_2	D_1	D_0	
Z-bus high			A_3	A_2	A_1	A_0	
Z-bus low	RJA=0	AD_7-AD_5	AD_4	AD_3	AD_2	AD_1	AD_0
	RJA=1	AD_7-AD_4	AD_3	AD_2	AD_1	AD_0	
Register							
Control Register 0		×	0	0	0	0	×
Control Register 1		×	0	0	0	1	×
Interrupt Status Register 0		×	0	0	1	0	×
Interrupt Status Register 1		×	0	0	1	1	×
Interrupt Status Register 2		×	0	1	0	0	×
Interrupt Status Register 3		×	0	1	0	1	×
Interrupt Vector Register		×	0	1	1	0	×
Byte Count Register		×	0	1	1	1	×
Byte Count Comparsion Register		×	1	0	0	0	×
Control Register 2*		×	1	0	0	1	×
Control Register 3		×	1	0	1	0	×
Message Output Register		×	1	0	1	1	×
Message Input Register		×	1	1	0	0	×
Pattern Match Register		×	1	1	0	1	×
Pattern Mask Register		×	1	1	1	0	×
Data Buffer Register		×	1	1	1	1	×

× = Don't Care bit (0, 1)
*Register is only o Port 1 side

● Control Register 0

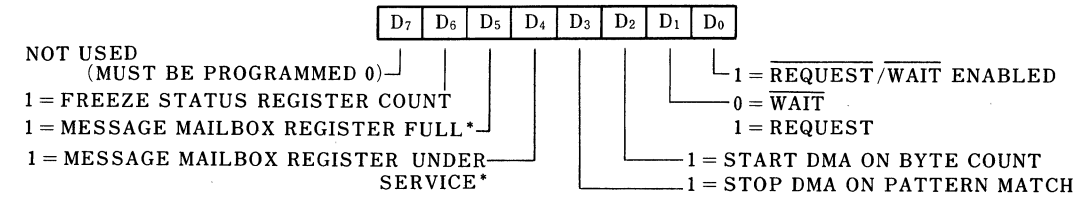
Address: 0000
(Read/Write)



*READ-ONLY FROM PORT 2 SIDE

● Control Register 1

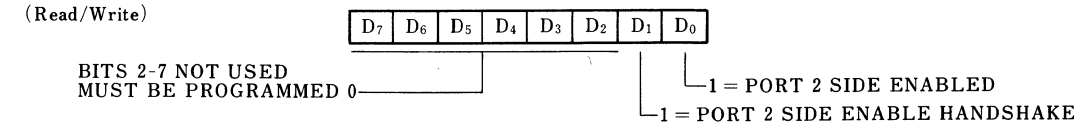
Address: 0001
(Read/Write)



*READ-ONLY BITS

● Control Register 2*

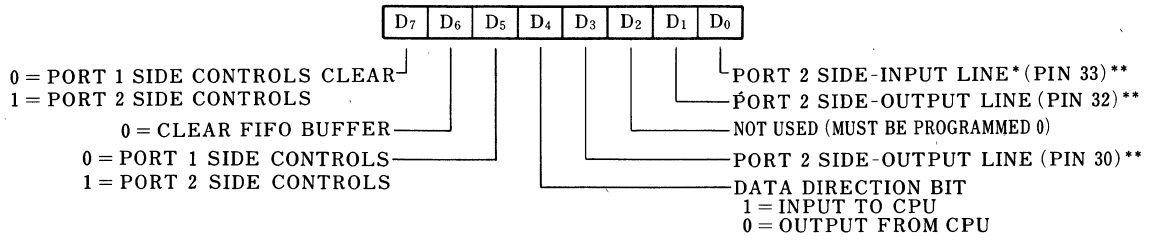
Address: 1001
(Read/Write)



*THIS REGISTER READS ALL 0'S FROM PORT 2 SIDE

● Control Register 3

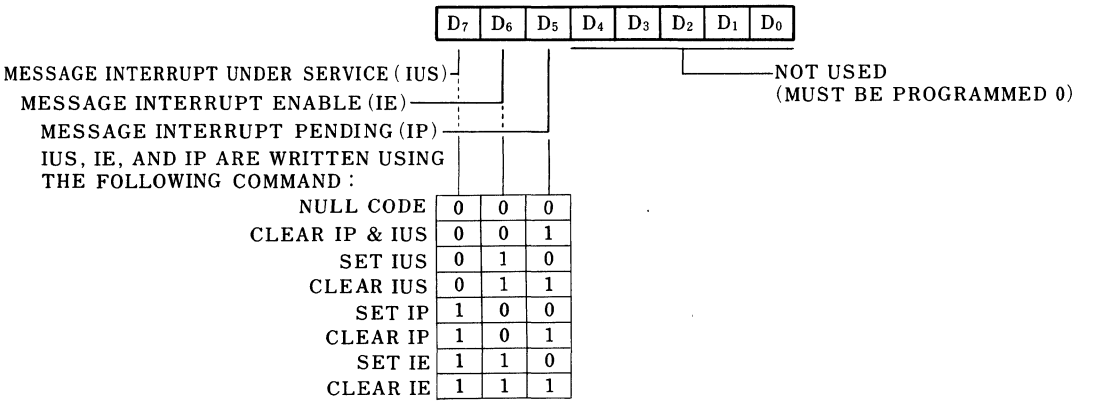
Address: 1010
(Read/Write)



*READ-ONLY BITS
**ONLY WHEN PORT 2 IS AN I/O PORT

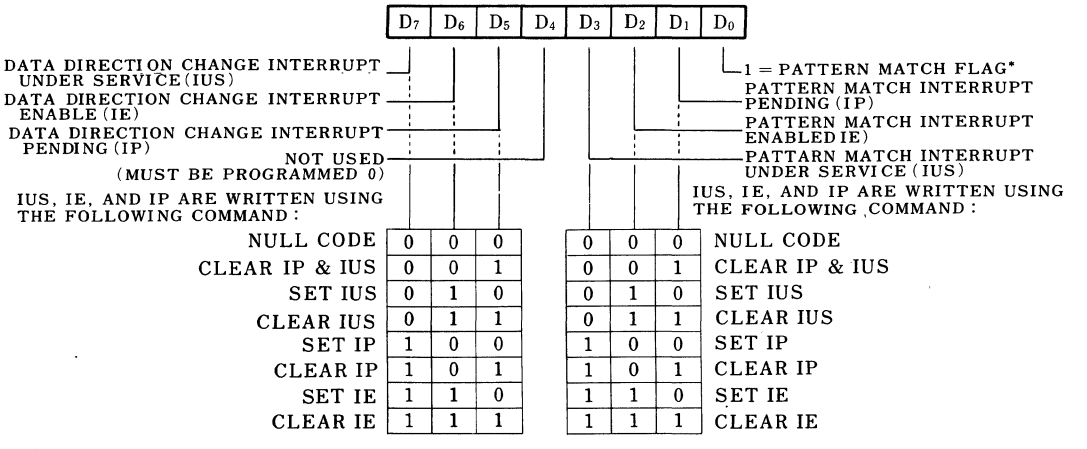
● Interrupt Status Register 0

Address : 0010 (Read/Write)



● Interrupt Status Register 1

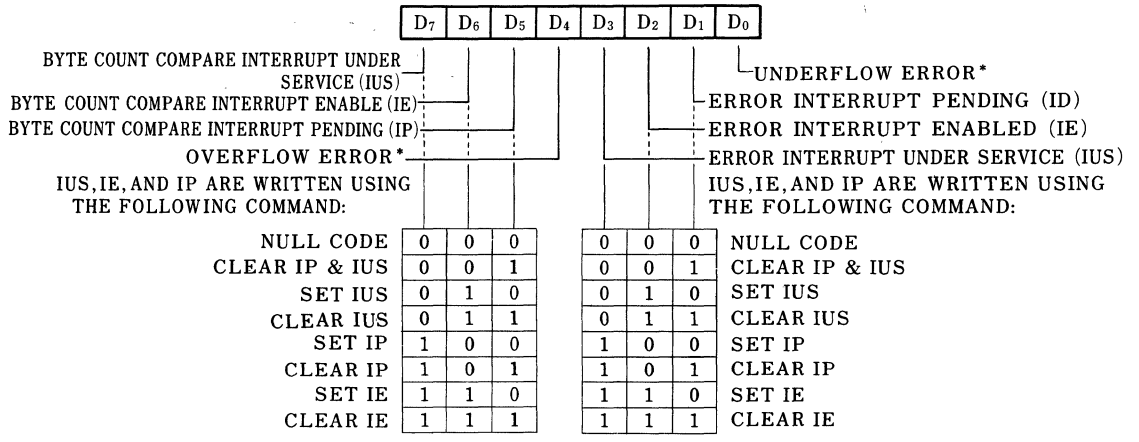
Address : 0011 (Read/Write)



*READ-ONLY BITS

● Interrupt Status Register 2

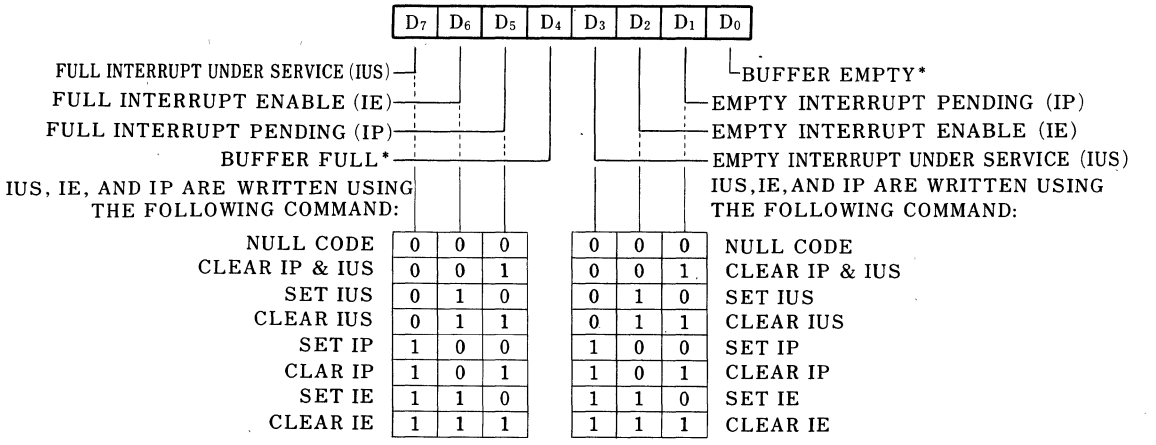
Address: 0100 (Read/Write)



*READ-ONLY BITS

● Interrupt Status Register 3

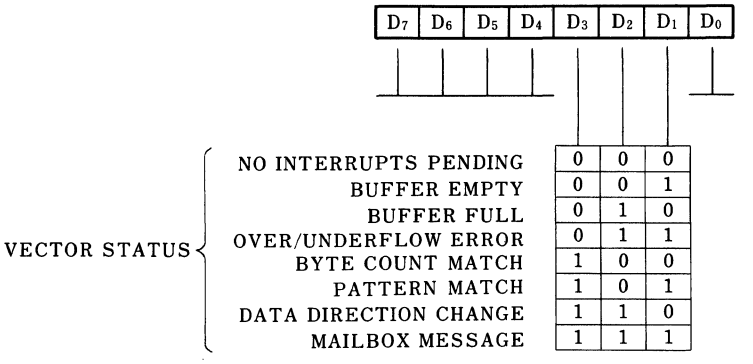
Address: 0101 (Read/Write)



*READ-ONLY BITS

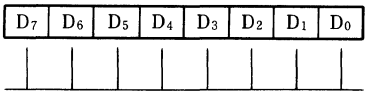
● Interrupt Vector Register

Address: 0110 (Read/Write)



● Byte Count Register

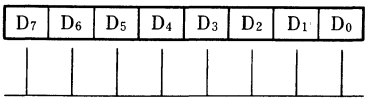
Address: 0111 (Read Only)



REFLECTS NUMBER OF BYTES IN BUFFER

● Byte Count Comparison Register

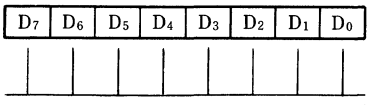
Address: 1000 (Read/Write)



CONTAINS VALUE COMPARED TO BYTE COUNT REGISTER TO ISSUE INTERRUPTS ON MATCH (BIT 7 ALWAYS 0.)

● Message Output Register

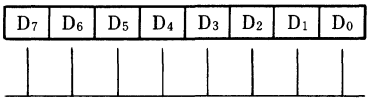
Address: 1011 (Read/Write)



STORES MESSAGE SENT TO MESSAGE IN REGISTER ON OPPOSITE PORT OF FIO

● Message Input Register

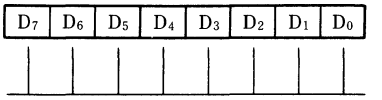
Address: 1100 (Read Only)



STORES MESSAGE RECEIVED FROM MESSAGE OUT REGISTER ON OPPOSITE PORT OF CPU

● Pattern Match Register

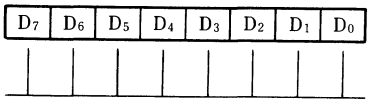
Address: 1101 (Read/Write)



STORES BYTE COMPARED WITH BYTE IN DATA BUFFER REGISTER

● Pattern Mask Register

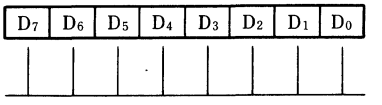
Address: 1110 (Read/Write)



IF SET, BITS 0-7 MASK BITS 0-7 IN PATTERN MATCH REGISTER. MATCH OCCURS WHEN ALL NON-MASKED BITS AGREE.

● Data Buffer Register

Address: 1111 (Read/Write)



CONTAINS THE BYTE TRANSFERRED TO OR FROM FIFO BUFFER RAM

5

LH8060 Z8060 FIFO Buffer Unit and Expander

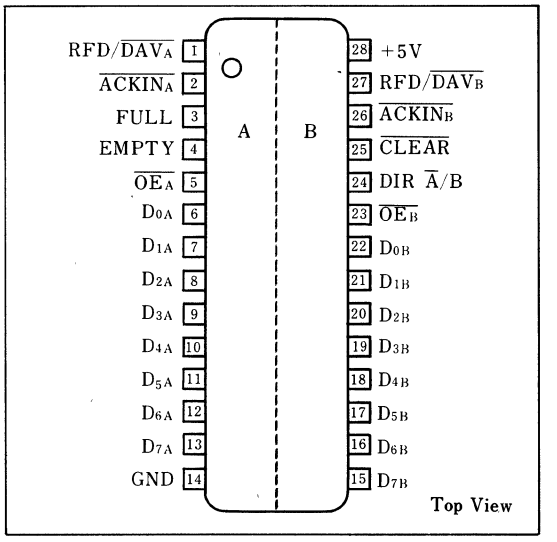
■ Description

The LH8060 First-In, First-Out (FIFO) buffer unit consists of a 128-bit-by-8-bit memory, bidirectional data transfer and handshake logic. The structure of the FIFO unit is similar to that of other available buffer units. LH8060 is a general-purpose unit ; its handshake logic is compatible with that of other members of Z8, Z8000 family and Z8500 family.

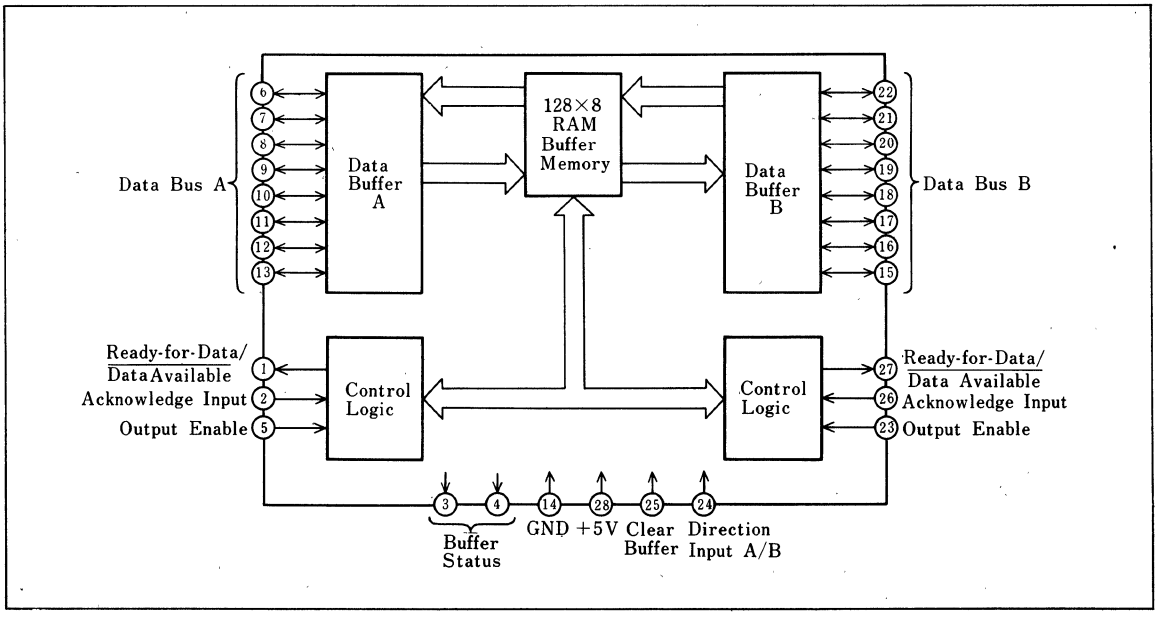
■ Features

1. Bidirectional, asynchronous data transfer capability
2. Large 128-bit-by-8-bit buffer memory
3. Two-wire, interlocked handshake protocol
4. 3-state data outputs
5. Wire-ORing of empty and full output for sensing of multiple-unit buffers
6. Connects any number of LH8060 in series to form buffer of any desired length
7. Connects any number of LH8060 in parallel to form buffer of any desired width

■ Pin Connections



■ Block Diagram



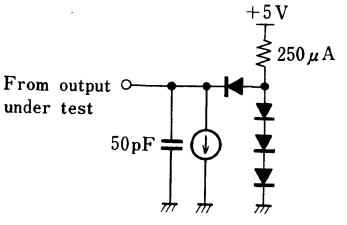
Pin Description

Pin	Meaning	I/O	Function
$D_0 \sim D_7$	Data bus	Bidirectional 3-state	Bidirectional data bus.
$\overline{ACKIN}$	Acknowledge input	I	Active low. Input handshake indicates that input data is valid ; output handshake indicates that output data has been receive by peripherals
RFD/$\overline{DAV}$	Ready-for-data/data valid	O	Input handshake indicates RFD (active High) : Z-FIFO is ready to receive data. Output handshake indicates DAV (active low) : Output data is valid.
$\overline{CLEAR}$	Clear	I	Active low. When set to low, this line causes all to be cleared from the FIFO buffer.
DIR $\overline{A}$/B	Data direction	I	This line allows control of the input data direction. When high, data is to be inputted through port B, when low, data is to be intputted through port A.
EMPTY	Empty	O	Active high, open-drain. Indicates that the FIFO buffer is empty
FULL	Full	O	Active high, open-drain. Indicates that the FIFO buffer is full.
$\overline{OE_A}$, $\overline{OE_B}$	Output enable	I	Active low. $\overline{OE_A}$, when high, causes the bus drivers for port A to float to a high impedance level input. $\overline{OE_B}$ controls the bus drivers for port B in the same manner as $\overline{OE_A}$ controls those for port A

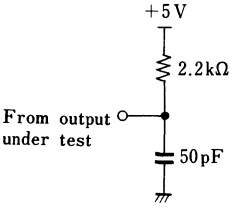
Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Input voltage	V_{IN}	$-0.3 \sim +7$	V	1
Output voltage	V_{OUT}	$-0.3 \sim +7$	V	1
Operating temperature	T_{opr}	$0 \sim +70$	℃	
Storage temperature	T_{stg}	$-65 \sim +150$	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.



Standerd test load



Open-drain test load

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input high voltage	V_{IH}		2		V_{CC}+0.3	V
Input low voltage	V_{IL}		−0.3		0.8	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4			V
Output low voltage	V_{OL}	I_{OL}=+2mA, I_{OL}=+3.2mA			0.4, 0.5	V
Input leakage current	$\lvert I_{IL} \rvert$	$0.4 \leqq V_{IN} < 2.4V$			10	μA
Output leakage current	$\lvert I_{OL} \rvert$	$0.4 \leqq V_{OUT} < 2.4V$			10	μA
Current consumption	I_{CC}				200	mA

■ Capacitance

(f=1MHz, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_{IN}	Unmeasurred pins retured to ground		10	pF
Output capacitance	C_{OUT}			15	pF
Bidirectional capacitance	$C_{I/O}$			20	pF

■ AC Characteristics

(1) Input pin

(f=1MHz, Ta=0～+70℃)

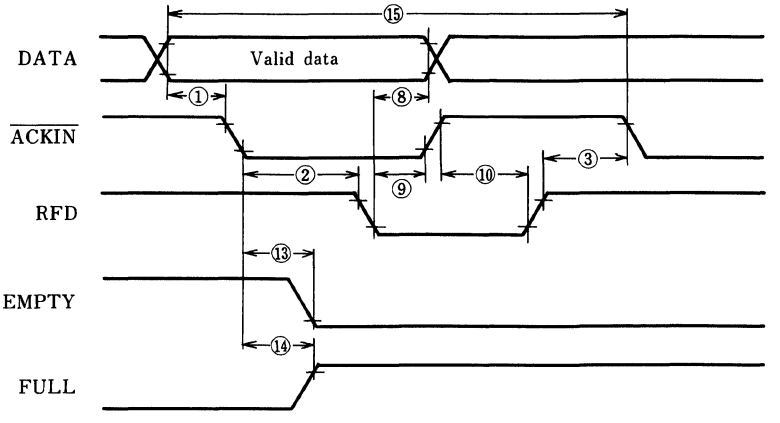
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input rise time	t_r			100	ns
Input fall time	t_f			100	ns

(2) 2-wire interlocked handshake timing

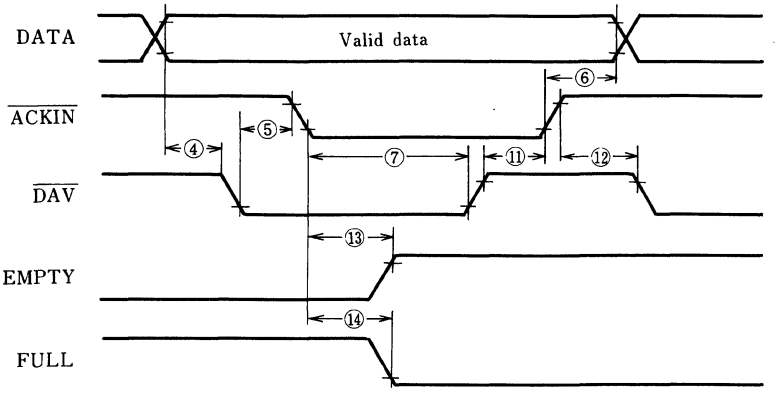
No.	Symbol	Parameter	MIN.	MAX.	Unit
1	TsDI (ACK)	Data input to $\overline{\text{ACKIN}}$ ↓ to setup time			ns
2	TdACKf (RFD)	$\overline{\text{ACKIN}}$ ↓ to RFD ↓ delay	0		ns
3	TdRFDr (ACK)	RFD ↑ to $\overline{\text{ACKIN}}$ ↓ delay	0		ns
4	TsDO (DAV)	Data out to $\overline{\text{DAV}}$ ↓ setup time	25		ns
5	TdDAVf (ACK)	$\overline{\text{DAV}}$ ↓ $\overline{\text{ACKIN}}$ ↓ delay			ns
6	ThDO (ACK)	Data out from $\overline{\text{ACKIN}}$ ↑ hold time			ns
7	TdACK (DAV)	$\overline{\text{ACKIN}}$ ↓ to $\overline{\text{DAV}}$ ↑ delay	0		ns
8	ThDI (RFD)	Data input from RFD ↓ hold time	0		ns
9	TdRFDf (ACK)	RFD ↓ to $\overline{\text{ACKIN}}$ ↑ delay	0		ns
10	TdACKr (RFD)	$\overline{\text{ACKIN}}$ ↑ to RFD ↑ delay	0		ns
11	TdDAVr (ACK)	$\overline{\text{DAV}}$ ↑ to $\overline{\text{ACKIN}}$ ↑ delay	0		ns
12	TdACKr (DAV)	$\overline{\text{ACKIN}}$ ↑ to $\overline{\text{DAV}}$ ↓ delay	0		ns
13	TdACKINf (EMPTY)	(Input) $\overline{\text{ACKIF}}$ ↓ to EMPTY ↓ delay, (Output) $\overline{\text{ACKIN}}$ ↓ to EMPTY ↓ delay			ns
14	TdACKINf (FULL)	(Input) $\overline{\text{ACKIN}}$ ↓ to FULL ↑ delay, (Output) $\overline{\text{ACKIN}}$ ↓ to FULL ↓ delay			ns
15	ACKIN Clock Rate	(Input or Output)	1.0		MHz
16	TdACKINf (DAVf)	$\overline{\text{ACKIN}}$ ↓ to $\overline{\text{DAV}}$ ↓ delay			ns
17	TwCLR	$\overline{\text{CLEAR}}$ "Low" hold time to reset Z-FIFO	700		ns
18	TdOE (DO)	$\overline{\text{OE}}$ ↓ to data bus driven delay	0		ns
19	TdOE (DRZ)	$\overline{\text{OE}}$ ↑ to data bus float delay			ns

Note : All timing references assume 2.0 V for a logic 1 and 0.8 V for a logic 0

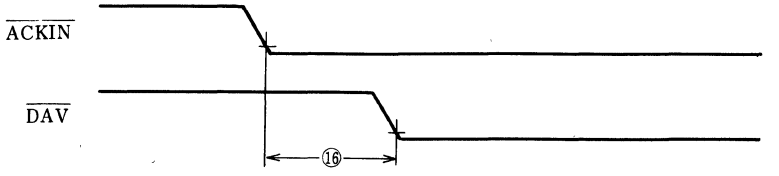
■ AC Timing Diagram



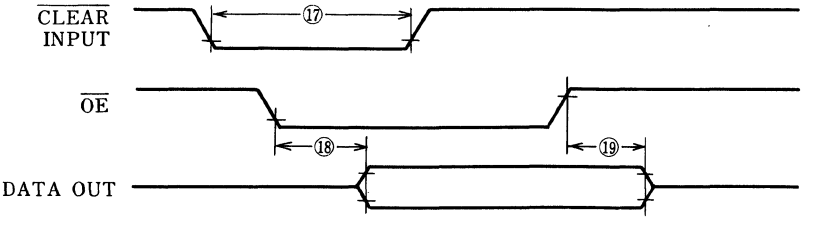
Input timing



Output timing



Time from $\overline{\text{ACKIN}}$ ↓ to $\overline{\text{DAV}}$ ↓



Output enable and clear

■ Interlocked 2-Wire Handshake

The LH8060 uses interlocked handshake operations for data trasfer. In interlocked handshake operation, the action must be acknowledged by the other half of the handshake before the next action can occur. The following describs the handshake timing in input and output modes.

(1) Input mode

In an Input Handshake mode, RFD (output) and $\overline{\text{ACKIN}}$ (input) are used as the handshake control lines. Unless the FIFO buffer is full, RFD is set High and signals to the peripherals involved that the FIFO buffer is ready to receive data. When the acknowledge signal $\overline{\text{ACKIN}}$ from the external device is set Low, the LH8060 takes the input data into the buffer and sets RFD Low to signal to the peripherals that the input signal has been received. This process is repeated until the FIFO is full, RFD is kept low.

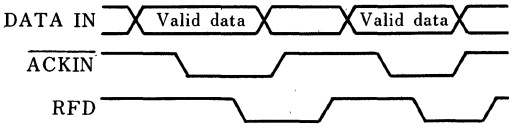


Fig. 1 2-wire interlocked handshake timing (input)

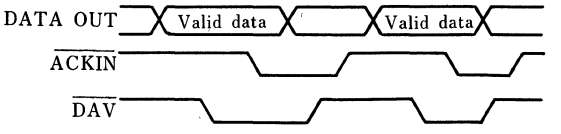


Fig. 2 2-wire interlocked handshake timing (output)

(2) Output mode

In an output handshake mode, $\overline{\text{DAV}}$ (output) and $\overline{\text{ACKIN}}$ are used as the control lines. If the LH8060 has data in the FIFO buffer and if $\overline{\text{ACKIN}}$ is high (indicating that the external device is ready to receive data), it sets $\overline{\text{DAV}}$ Low to signal to the external device that the output data is available.

When the external device sets ACKIN low to indicate that it has received the data, LH8060 sets $\overline{\text{DAV}}$ back to a high level. In response, the external device sets $\overline{\text{ACKIN}}$ high to request the LH8060 for the next data. This process repeats till the FIFO buffer becomes empty. when it becomes empty, $\overline{\text{DAV}}$ is kept high.

This contorol feature allows the LH8060, with no external logic, to directly interface with port of:

- Z8
- Z-CIO
- Z-UPC
- Z-FIO
- Another FIFO

■ Resetting and Clearing the FIFO

The $\overline{\text{CLEAR}}$ input signal is used to reset and clear the LH8060 FIFO. A Low level on this input clears all data from the FIFO buffer and disallows any data transfer.

■ Bidirectional Transfer Control

The LH8060 has bidirectional data transfer capability under control of the DIR $\overline{\text{A}}$/B input. When DIR $\overline{\text{A}}$/B is set Low, data transfers are made from Port A to Port B.

Setting DIR $\overline{\text{A}}$/B High reverses the handshake assignments and the direction of transfer.

Table 1 Bidirectional control function table

DIR $\overline{\text{A}}$/B	Port A handshake	Port B handshake	transfer
0	Input	Output	A to B
1	Output	Input	B to A

■ Empty and Full Operation

The EMPTY and FULL output lines can be wire-ORed with the EMPTY and FULL lines of other LH8060s and LH8038s. This capability enables the user to determine the empty/full status of a buffer consisting of multiple FIFOs, FIOs, or a combination of both.

■ Interconnection Example

Fig. 3 illustrates a simplified block diagram showing the manner in which LH8060s can be interconnected to extend an LH8038 buffer.

Table 2 Signals EMPTY and FULL operation table

Number of bytes in FIFO	EMPTY	FULL
0	High	Low
1~127	Low	Low
128	Low	High

■ Output Enable Operation

The FIFO provides a separate Output Enable (OE) signal for each port of the buffer. An $\overline{OE}$ output is valid only when its port is in the Output Handshake mode. The control of this output function is shown in Table 3-Signal $\overline{OE}$ operates with lines DIR $\overline{A}$/B.

Table 3 Output control function table

DIR $\overline{A}$/B	$\overline{OE}_A$	$\overline{OE}_A$	Function
0	X	0	Disable port A output Enable port B output
0	X	1	Disable port A output Enable port B output
1	0	X	Enable port A output Disable port B output
1	1	X	Disable port A output Disable port B output

Note : X=Don't care

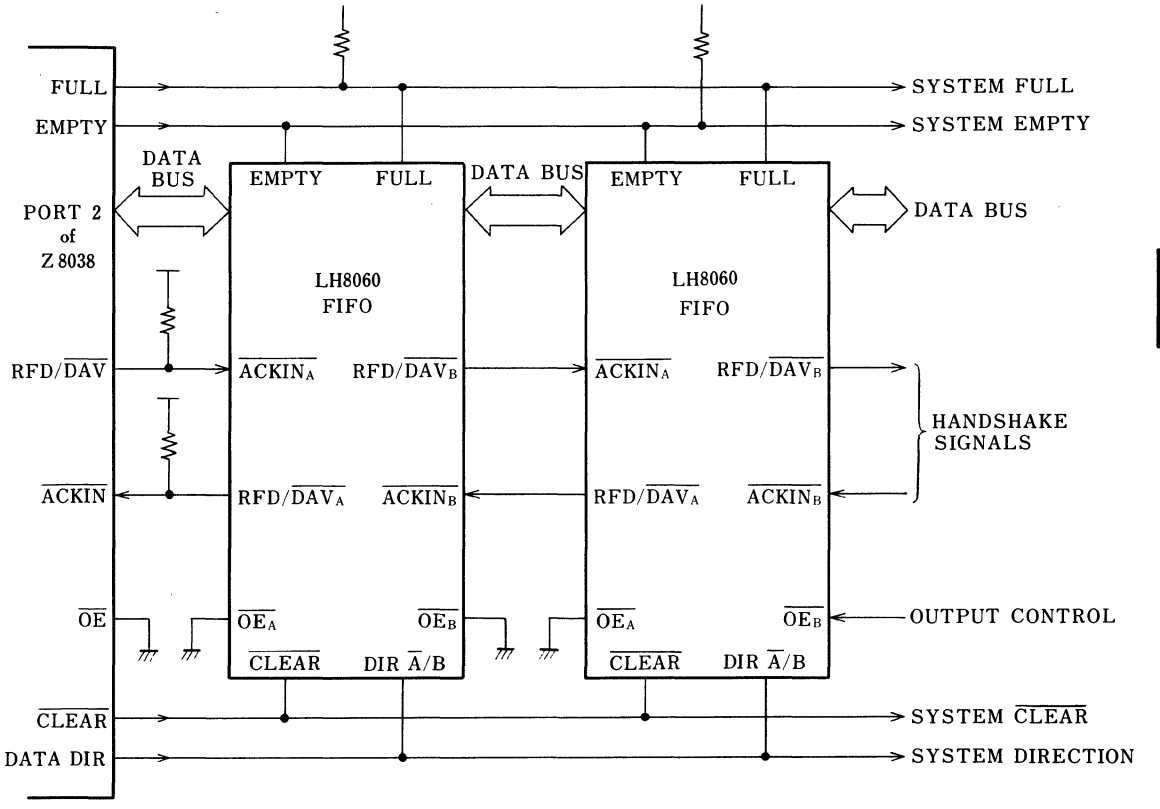


Fig. 3 Connection diagram

LH8071 Serial Parallel Combination Controller

■ Description

The LH8071 (SPCC71) is a peripheral device for general purpose microcomputers, with control functions for RS232C interface and Centronics interface, within a single LSI chip.

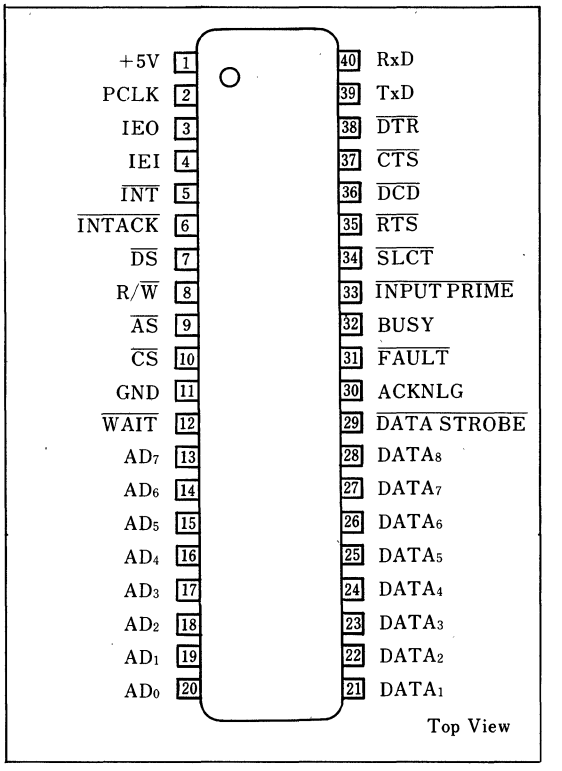
The LH8071 provides a serial port for transferring data in asynchronous mode and also an 8-bit parallel port with handshaking function as a Centronics interface.

The LH8071 has 24 commands for controlling these ports. The commands not only control the operation of RS232C terminal units and printers, but handle various utilities (e.g., code conversion) necessary for these units. Accordingly, the CPU needs merely to specify an operation through the command, thus significantly reducing the CPU's load in handling I/O units through the program, and eventually reducing the amount of memory needed for storing the program.

The LH8071 controls the peripheral unit control lines (e.g., $\overline{RTS}$ and $\overline{CTS}$ of RS232C interface) according to the status of the units, instead of by software control from the CPU. Consequently, the system designer can configure the interface merely by connecting buffer devices and connectors.

In conclusion, the LH8071 not only easily implements the RS232C interface and Centronics interface, but achieves superior performance and space reduction.

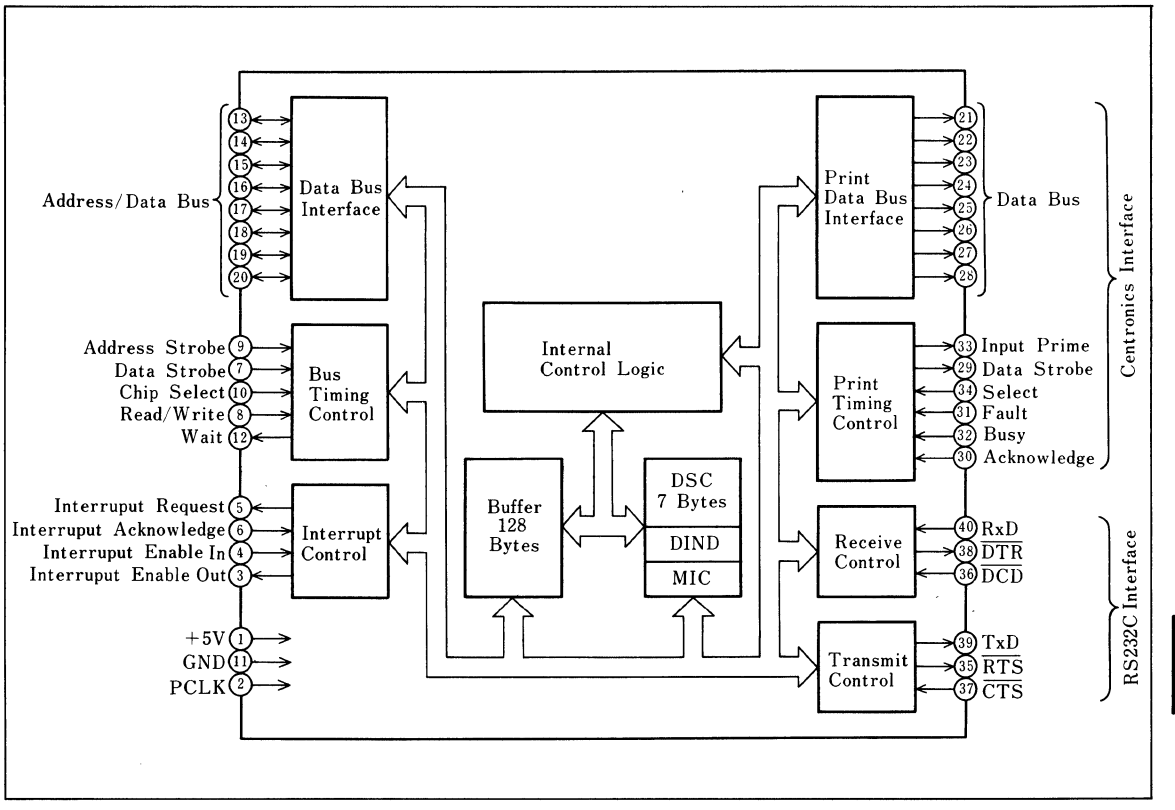
■ Pin Connections



■ Features

1. Asynchronous data transfer serial port
   - RS232C interface can easily be realized
   - Programmable data format and Baud rate
2. Printer control parallel port
   - Centronics interface can easily be realized
3. Data transfer and conversion functions by command
   - 24 commands
4. Data conversion function
   - Serial-parallel conversion
   - Binary-ASCII conversion
   - Intel hex, format acceptable for data input/output
5. 128-byte data transfer buffer
   - Useful for the serial port and parallel port
6. Z-bus interface
7. 40-pin dual-in-line package
8. Single + 5V power supply

■ Block Diagram



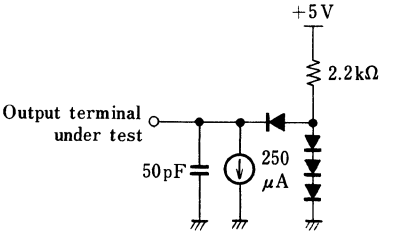
■ Pin Description

Pin	Meaning	I/O	Function
$AD_0 \sim AD_7$	Address/data bus	Bidirectional 3 state	Multiplexed system address/data bus as address.
$\overline{AS}$	Address strobe	I	Active low. Fetch information on address/data bus as address.
$\overline{DS}$	Data strobe	I	Active low. Transact information on address/data bus as data.
R/$\overline{W}$	Read/write	I	High at reading. Output contents of internal register onto address/data bus; Low at writing. Fetch data on address/data bus.
$\overline{CS}$	Chip select	I	Active low. Chip selection signal
$\overline{WAIT}$	Wait	O	Active low, open-drain. Used to synchronize with CPU.
$\overline{INT}$	Interrupt request	O	Active low, open-drain. Indicate interrupt request to CPU.
$\overline{INTACK}$	Interrupt acknowledge	I	Active low. Indicate interrupt acknowledge cycle.
IEI	Interrupt enable input	I	Active high. Used to form interrupt priority arbitration loop circuit (daisy chain).
IEO	Interrupt enable output	O	Active high. Used to form daisy chain.
$DATA_1 \sim DATA_8$	Output data	O	Output data
$\overline{DATA\ STROBE}$	Data strobe	O	Active low. Indicate settlement of data.
BUSY	Busy	I	Active high. Indicate printer in operation.
ACKNLG	Acknowledge	I	Active high. Acknowledge signal from printer.
$\overline{FAULT}$	Fault	I	Active low. Indicate printer inoperable.
$\overline{INPUT\ PRIME}$	Prime input	O	Active low. Printer initializing signal.
$\overline{SLCT}$	Select	I	Active low. Printer selection signal.
RxD	Received data	I	Receiving data line.
TxD	Transmitted data	O	Transmitting data line.
$\overline{RTS}$	Transmission request	O	Active low. Indicate readiness for data transmission.
$\overline{CTS}$	Transmission enable	I	Active low. Indicate data transmission is possible.
$\overline{DTR}$	Data terminal ready	O	Active low. Data transmission request signal.
$\overline{DCD}$	Reception enable	I	Active low. Indicate data reception is possible.
PCLK	Clock	I	Single-phase clock, need not be same as CPU clock.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage*	V_{IN}	−0.3～+7	V
Output voltage*	V_{OUT}	−0.3～+7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

* The maximum applicable voltage on any pin except for V_{BB} with respect to GND.



Standard test load

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0~+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock input high voltage	V_{CH}		2.4		V_{CC}	V
Clock input low voltage	V_{CL}		−0.3		0.8	V
Input high voltage	V_{IH}		2		V_{CC}	V
Input low voltage	V_{IL}		−0.3		0.8	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4			V
Output low voltage	V_{OL}	I_{OL}=2mA			0.4	V
Input leakage current	$\lvert I_{IL} \rvert$	$0 \leqq V_{IN} \leqq 5.25V$			10	μA
Output leakage current	$\lvert I_{OL} \rvert$	$0 \leqq V_{IN} \leqq 5.25V$			10	μA
Current consumption	I_{CC}				250	mA

■ AC Characteristics

(1) CPU interface timing

(V_{CC}=5V±5%, Ta=0~+70℃)

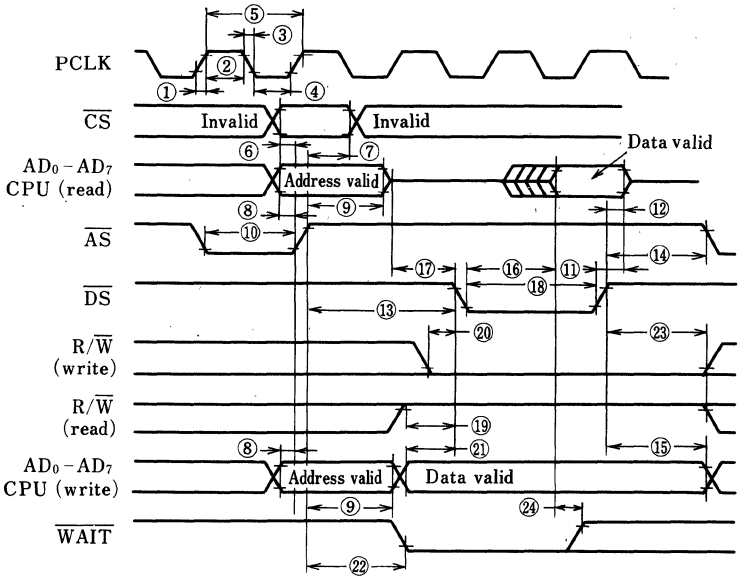
No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TrC	Clock rise time		20	ns	
2	TwCh	DSClock pulse high width	105		ns	
3	TfC	Clock fall time		20	ns	
4	TwCl	Clock pulse low width	105		ns	
5	TpC	Clock period	250		ns	
6	TsCS(AS)	$\overline{CS}$ setup time to $\overline{AS}$ ↑	0		ns	1
7	ThCS(AS)	$\overline{CS}$ hold time from $\overline{AS}$ ↑	60		ns	1
8	TsA(AS)	Address setup time to $\overline{AS}$ ↑	30		ns	1
9	ThA(AS)	Address hold time from $\overline{AS}$ ↑	50		ns	1
10	TwAS	$\overline{AS}$ low pulse width	70		ns	
11	TdDS(DR)	Delay time from $\overline{DS}$ ↑ to invalid readout data	0		ns	
12	TdDS(DRz)	Delay time from $\overline{DS}$ ↑ to readout data floating		70	ns	2
13	TdAS(DS)	Delay time from $\overline{AS}$ ↑ to $\overline{DS}$ ↓	60	2095	ns	
14	TdDS(AS)	Delay time from $\overline{DS}$ ↑ to $\overline{AS}$ ↓	50		ns	
15	ThDW(DS)	Written data hold time from $\overline{DS}$ ↑	30		ns	1
16	TdDS(DR)	Delay time from $\overline{DS}$ ↓ to readout data settlement			ns	3
17	TdAz(DS)	Delay time from address floating to $\overline{DS}$ ↓	0		ns	
18	TwDS	$\overline{DS}$ low pulse width	390		ns	
19	TsRWR(DS)	R/$\overline{W}$ high (read) setup time to $\overline{DS}$ ↓	100		ns	
20	TsRWW(DS)	R/$\overline{W}$ low (write) setup time to $\overline{DS}$ ↓	0		ns	
21	TsDW(DSf)	Written data setup time to $\overline{DS}$ ↓	30		ns	
22	TdAS(W)	Delay time from $\overline{AS}$ ↑ to $\overline{WAIT}$ ↓		195	ns	
23	ThWR(DS)	R/$\overline{W}$ hold time from $\overline{DS}$ ↑	60		ns	
24	TsDR(W)	Time from valid readout data to $\overline{WAIT}$ ↑	0		ns	

↑ indicates rising edge, ↓ indicates falling edge. The reference voltage levels for timing measurement are 2.0 volts for 'high'; 0.8 volts for 'low'.

Note 1: This does not apply to the interrupt acknowledge operation.

Note 2: The Max. value of TdAS (DS) does not apply to the interrupt acknowledge operation.

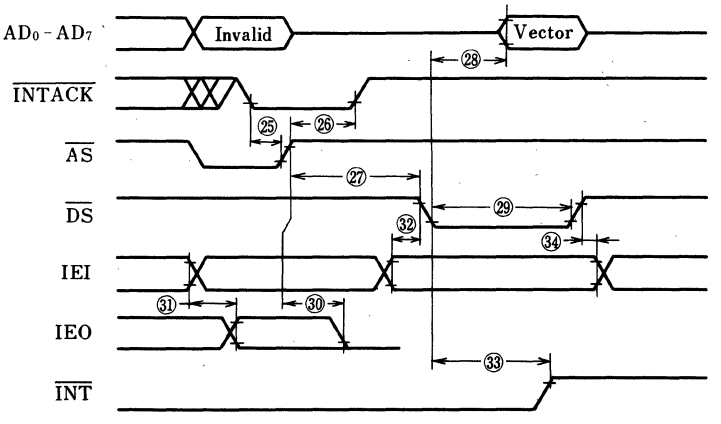
Note 3: The delay time depends on the status of LH8071 at the time of access by CPU.



CPU interface timing

(2) Interrupt acknowledge timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
25	TsIA(AS)	$\overline{\text{INTACK}}$ setup time to $\overline{\text{AS}}$ ↑	0		ns	
26	ThIA(AS)	$\overline{\text{INTACK}}$ low hold time from $\overline{\text{AS}}$ ↑	250		ns	
27	TdAS(DSA)	Delay time from $\overline{\text{AS}}$ ↑ to $\overline{\text{DS}}$ ↓ (acknowledge)	940		ns	
28	TdDSA(DR)	Delay time from $\overline{\text{DS}}$ ↓ (acknowledge) to vector settlement		360	ns	
29	TwDSA	$\overline{\text{DS}}$ (acknowledge) low pulse width	475		ns	
30	TdAS(IEO)	Delay time from $\overline{\text{AS}}$ ↑ to IEO		290	ns	
31	TdIEIf(IEO)	Delay time from IEI to IEO		120	ns	
32	TsIEI(DSA)	IEI setup time to $\overline{\text{DS}}$ ↓ (acknowledge)	150		ns	
33	TdDS(INT)	Delay time from $\overline{\text{DS}}$ ↓ to INT		500	ns	
34	ThIEI(DS)	IEI hold time from $\overline{\text{DS}}$ ↑	100		ns	

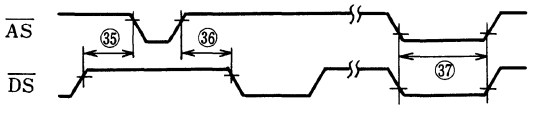


Interrupt acknowledge timing

(3) Reset timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
35	TdRDQ(AS)	Delay time from $\overline{DS}$ ↑ (for suppressing reset) to $\overline{AS}$ ↓	40		ns	
36	TdWRQ(DS)	Delay time from $\overline{AS}$ ↑ (for suppressing reset) to $\overline{DS}$ ↓	50		ns	
37	TwRES	Minimum low width of $\overline{AS}$ and $\overline{DS}$ (for setting)	250		ns	4

Note 4: The internal reset signal lags by 1/2 to 2 clocks behind external reset conditions.

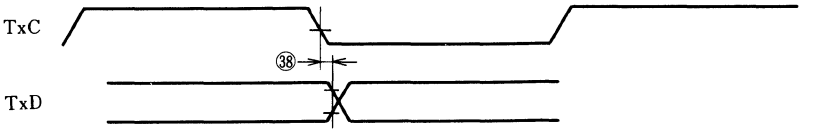


Reset timing

(4) Serial port timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
38	TdTxC(TxD)	Delay time from sending clock transition to output data transition		19000	ns	5

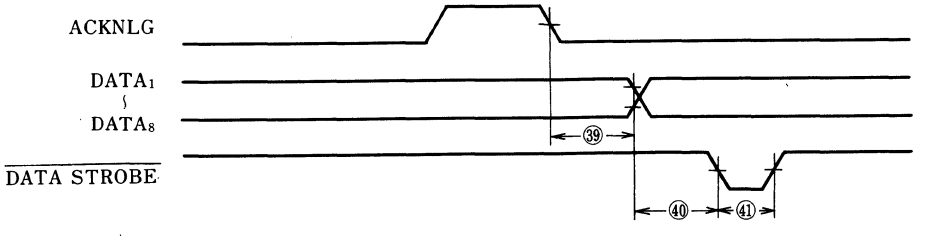
Note 5: Applies to all baud rates (110-9800 B) serial port timing



Serial port timing

(5) Parallel port timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
39	TdACK(D)	Time from ACKNLG ↓ to data output	13000	18000	ns	
40	TdD(DSTR)	Time from data output to $\overline{DATA\ STROBE}$ ↓	6000		ns	
41	TwDSTR	$\overline{DATA\ STROBE}$ pulse width	6000		ns	



Parallel port timing

■ Registers

The LH8071 has the following registers which can be accessed externally (from CPU).

- Master interrupt control register (MIC)
- Data indirect address register (DIND)
- Data status command registers (DSC0, DSC1, DSC2, DSC3, DSC4, DSC5 and DSC8)

Table 1 shows the register addresses assigned to these registers.

The master interrupt control register (MIC) is used to control the interrupt operation (see Fig. 2).

Writing into the MIC register falls into two groups.

Group 2 uses the write code shown in Table 2.

Table 1 Register address

Register	Register address	Register	Register address
DSC0	××00000×	DSC5	××00101×
DSC1	××00001×	DSC8	××01000×
DSC2	××00010×	DIND	××10101×
DSC3	××00011×	MIC	××11110×
DSC4	××00100×		

Note: A_{15}-A_6 is decoded and applied to cs, so that the location in the input/output address space is determined. Bits marked by 'x' are underfined.

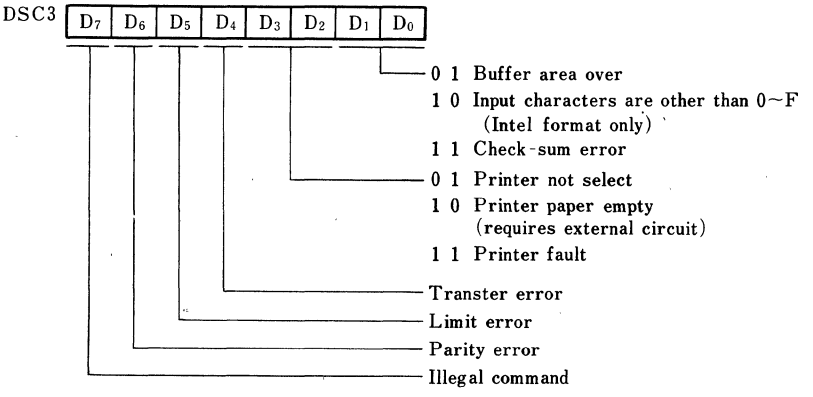


Fig. 1 Error flag (DSC3)

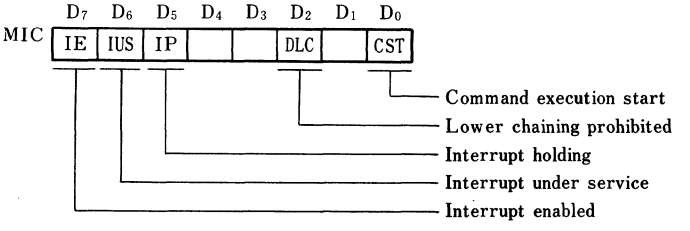


Fig. 2 Master interrupt control register

Table 2 MIC register write code

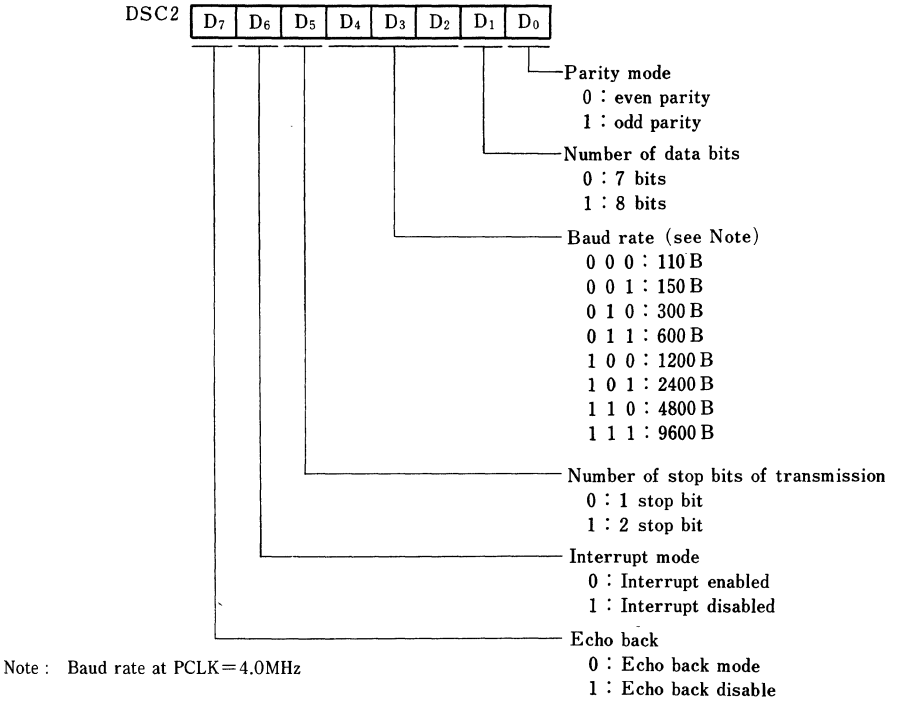
Group 2			Group 1		Function
D_7	D_6	D_5	D_2	D_0	
0	0	0	×	×	Writing to D_0 and D_2
0	0	1	0	0	Reset IP (D_5) and IUS (D_6)
0	1	0	0	0	Set IUS (D_6)
0	1	1	0	0	Reset IUS (D_6)
1	0	0	0	0	Set IP (D_5)
1	0	1	0	0	Reset IP (D_5)
1	1	0	0	0	Set IE (D_7)
1	1	1	0	0	Reset IE (D_7)

■ Programming

Use the registers, DSC0, DSC1, DSC2, DSC3, DSC4, DSC5, and DSC8, to specify operation mode. The 24 types of commands are made valid by first writing a value corresponding to the desired command number into DSC0, then setting the CST bit on MIC. The registers DSC1, DSC2, DSC4, and DSC5 are used to specify parameters for each command. Command 0 is used in specifying serial data format using DSC2 (Fig. 3).

The result of command execution is indicated on DSC0 and DSC3. DSC3 indicates error status as show in Fig. 1. DSC8 is used as a buffer register after command 22 or 23 is executed.

Tables 3 and 4 show command functions versus registers.



Note : Baud rate at PCLK=4.0MHz

Fig. 3 Serial data format (DSC2)

Table 3 Command function and writing register contents

Register / Command	Code	Parameter				Function	Remarks
	DSC0	DSC1	DSC2	DSC4	DSC5		
0	00_H		Transfer format and operating mode			Sepcify transfer format and operating mode.	
1	01_H		Stop character			Output serial-input data to Centronics printer until the stop character arrives.	Stop character is specified by DSC2.
2	02_H	Number of output bytes				Output serial-input data to Centronics printer.	Operation stops upon detection of Control C (hex 03).
3	03_H	Number of output bytes		Load address (high order byte)	Load address (low order byte)	Output buffer area contents to serial port in Intel format.	Address information of data is appended.
4	04_H					Read Intel format data on serial port and store in buffer area.	
5	05_H	Number of bytes of block transfer				Initialize block transfer between master CPU and buffer	
6	06_H	Number of output bytes	Output starting address			Output data in buffer area via serial port.	Operation stops upon detection of Control C (hex 03).
7	07_H	Number of output bytes	Output starting address			Output data in buffer area to printer.	Operation stops upon detection of Control C (hex 03).
8	08_H	Number of output bytes	Output starting address			Convert binary data in buffer area into ASCII and area.	
9	09_H	Number of output bytes	Output starting address	Display address (High order)	Display address (Low order)	Convert binary data in buffer area into ASCII and output via serial port.	Address information of data is appended.
10	$0A_H$	Number of output bytes	Output starting address			Convert binary data in buffer area into ASCII, and output to printer.	
11	$0B_H$	Number of output bytes	Output starting address	Display address (High order)	Display address (Low order)	Convert binary data in buffer area into ASCII, and output to printer.	Address information of data is appended.
12	$0C_H$	Number of input bytes	Output character			Read ASCII data on serial port, and store in buffer area.	
13	$0D_H$					Read Intel format data on serial port and store in buffer area.	Used when reader is connected to serial port.
14	$0E_H$		Output character			Read ASCII data on serial port until arrival of CR code.	After CR reception, CR and LF codes are sent out via serial port.
15	$0F_H$	Number of output bytes		Load address	Load address	Convert data in buffer area into Intel format and output via serial port.	Used when a puncher is connected to serial port.

Register / Command	Code	Parameter				Function	Remarks
	DSC0	DSC1	DSC2	DSC4	DSC5		
16	10_H	Number of input bytes	Output character			Read binary data on serial port into buffer area for storage.	Used when a reader is connected to serial port.
17	11_H	Number of output bytes	Output starting address			Output data in buffer area via serial ports.	Used when a puncher is connected to serial port. Operation stops upon detection of hex 03.
18	12_H					Output null codes via serial port.	256 null codes outputted.
19	13_H					Output EOF in Intel format (:00000001FF) via serial port.	
20	14_H					Output null codes via serial port.	Used when a puncher is connected to serial port.
21	15_H					Output EOF in Intel format (:00000001FF) via serial port.	Used when a puncher is connected to serial port.
22	16_H					Read 1-byte data on serial port.	Data is stored in DSC8.
23	17_H					Output data written in DSC8 by CPU via serial port.	Data needs to be set in DSC8 prior to execution (high order byte)

Table 4 Register contents after command execution (readout register)

Register / Command	Code DSCO 1*	2*	3*	Parameter DSC1	DSC2	DSC3	DSC4	DSC5
0	00_H	80_H	$C0_H$			Error status flag		
1	01_H	81_H	$C1_H$			Error status flag		
2	02_H	82_H	$C2_H$			Error status flag		
3	03_H	83_H	$C3_H$			Error status flag		
4	04_H	84_H	$C4_H$		Number of inputted bytes pluse hex 20	Error status flag	Load address (High order byte)	Load address (Low order byte)
5	05_H	85_H	$C5_H$			Error status flag		
6	06_H	86_H	$C6_H$			Error status flag		
7	07_H	87_H	$C7_H$			Error status flag		
8	08_H	88_H	$C8_H$			Error status flag		
9	09_H	89_H	$C9_H$			Error status flag		
10	$0A_H$	$8A_H$	CA_H			Error status flag		
11	$0B_H$	$8B_H$	CB_H			Error status flag		
12	$0C_H$	$8C_H$	CC_H			Error status flag		
13	$0D_H$	$8D_H$	CD_H		Number of inputted bytes plus hex 20	Error status flag	Load address (High order byte)	Load Adress (Low order byte)
14	$0E_H$	$8E_H$	CE_H			Error status flag	Number of inputted byte pulse hex 20	
15	$0F_H$	$8F_H$	CF_H			Error status flag		
16	10_H	90_H	$D0_H$			Error status flag		
17	11_H	91_H	$D1_H$			Error status flag		
18	12_H	92_H	$D2_H$			Error status flag		
19	13_H	93_H	$D3_H$			Error status flag		
20	14_H	94_H	$D4_H$			Error status flag		
21	15_H	95_H	$D5_H$			Error status flag		
22	16_H	96_H	$D6_H$			Error status flag		
23	17_H	97_H	$D7_H$			Error status flag		

Note 1 1*: Value before command execution (command code value)
2*: Value upon normal completion of command execution.
3*: Value upon abnormal completion (error) of command execution.
These are common to all commands.

Note 2 For error status flag value, see Fig. 1.

Note 3 If FAULT input becomes low (printer error) during command execution, LH8071 suspends operation until FAULT returns to high (error recovery). At this time, DSC0 has bit 6 set and bit 7 reset.

LH8072 Serial Parallel Combination Controller

■ Description

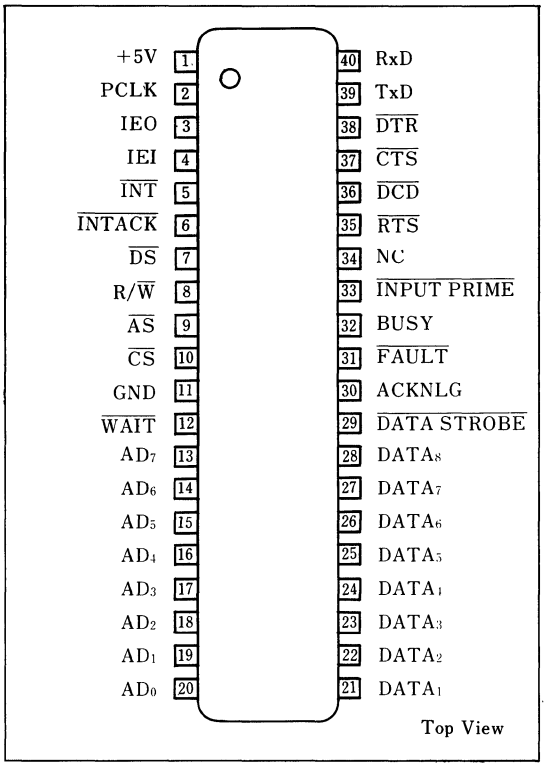
The LH8072 (SPCC72) is a peripheral device for general purpose microcomputer systems to perform asynchronous serial data transfers and control of Centronics compatible printers.

It supports full duplex asynchronous serial data transfers. The transfer conditions such as the baud rate and character length can be set by the program. Further, it is equipped with a control I/O terminal for simple organization of the various types of modem interfaces. The Receive Buffer has a double buffer structure so that the master CPU can easily perform reading and writing of data.

A printer control I/O terminal is available for easy connection to any printer which is Centronics compatible. A handshake line and control for other I/O lines is supported. A 128-byte printer data buffer memory having an FIFO structure is provided within the LH8072. Efficient use of the printer unit by the master CPU is made possible with this buffer.

In this way, the LH8072 peripheral device for Z8000 family, was developed to efficiently perform serial data transfer and printer output control within a compact package. It is suitable for use in small systems such as personal computers which use printer units, RS232C terminal units and modem units.

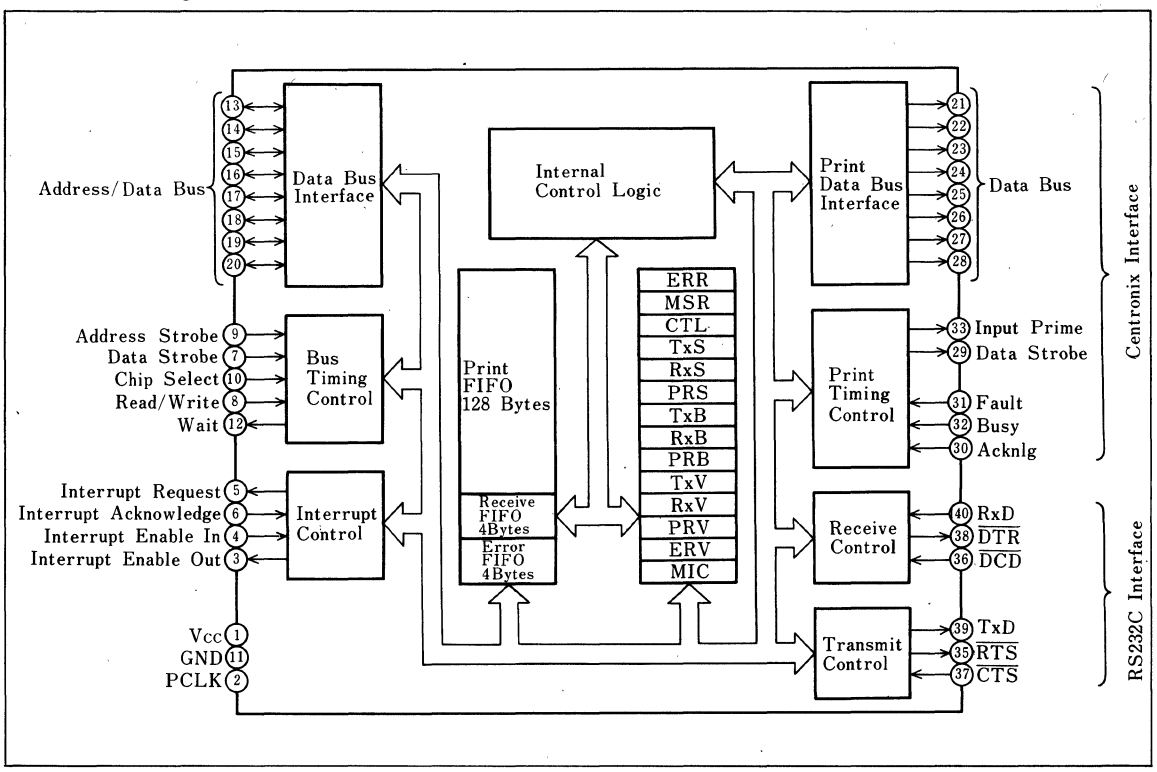
■ Pin Connections



■ Features

1. Asynchronous Full Duplex Data Transfer
   - Character length of 5-8 bits
   - 1 or 2 stop bits
   - No parity bit or odd/even parity
   - False start bit or rejection (rejects spike noise in the mark line to prevent malfunction.)
   - Full duplex
   - Transmit buffer has double buffer structure.
   - Receive buffer has FIFO structure.
   - Error detection function, Parity error detection, Framing error detection, and Overrun error detection
   - Baud rates : 75, 110, 150, 300, 600, 1200, 2400, 4800 baud selectable
2. Centronics Compatible Printer Control
   - Furnishes printer interface signals compatible with Centronics specifications
   - Built-in handshake function for data output
   - Internal buffer : 128-byte FIFO structure
   - Error detection : Printer fault error/Paper empty error
3. Vector Interrupt
   - Able to generate an interrupt on various condition such as Transmit Buffer empty, validity of received character, and printer Output Buffer empty.
   - Interrupt vectors for Transmit, Receive, Printer and Error detection can be set individually.
4. Single + 5V power supply
5. Z-bus interface
6. 40-pin dual-in-line package

Block Diagram



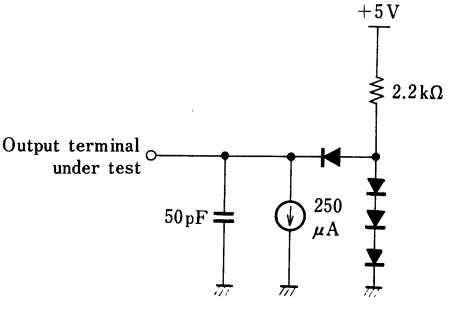
■ Pin Description

Pin	Signal	I/O	Function
$AD_0 \sim AD_7$	Address/data bus	Bidirectional 3-state	Multiplexed system address/data bus
$\overline{AS}$	Address strobe	I	Active low. Fetch information on address/data bus as address.
$\overline{DS}$	Data strobe	I	Active low. Transact information on address/data bus as data.
R/$\overline{W}$	Read /write	I	High at reading. Output contents of internal register onto address/data bus ; Low at writing. Fetch data on address/data bus.
$\overline{CS}$	Chip select	I	Active low. Chip selection signal
$\overline{WAIT}$	wait	O	Active low, open-drain. Used to synchronize with CPU.
$\overline{INT}$	Interrupt request	O	Active low, open-drain. Indicate interrupt request to CPU.
$\overline{INTACK}$	Interrupt acknowledge	I	Active low. Indicate interrupt acknowledge cycle.
IEI	Interrupt enable input	I	Active high. Used to form interupt priority arbitration loop circuit (daisy chain).
IEO	Interrupt enable output	O	Active high. Used to form daisy chain.
$DATA_1 \sim DATA_8$	Output data	O	Output data
$\overline{DATA\ STROBE}$	Data strobe	O	Active low. Indicate settlement of data.
BUSY	Busy	I	Active high. Indicate printer in operation.
ACKNLG	Acknowledge	I	Active high. Acknowledge signal from printer.
$\overline{FAULT}$	Fault	I	Active low. Indicate printer inoperable.
$\overline{INPUT\ PRIME}$	Prime input	O	Active low. Printer initializing signal.
RxD	Receivived data	I	Receiving data line.
TxD	Transmitted data	O	Transmitting data line.
$\overline{RTS}$	Transmission request	O	Active low. Indicate readiness for data transmission.
$\overline{CTS}$	Transmission enable	I	Active low. Indicate data transmission is possible.
$\overline{DTR}$	Data terminal ready	O	Active low. Data transmission request signal.
$\overline{DCD}$	Reception enable	I	Active low. Indicate data reception is possible.
PCLK	Clock	I	Signal-phase clock, need not be same as CPU clock.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage*	V_{IN}	−0.3～+0.7	V
Output voltage*	V_{OUT}	−0.3～+0.7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃

*The maximum applicable voltage on any pin with respect to GND.



Standard test load

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0~+70℃)

Parameter	Symbol	Condition	MIN.	MAX.	Unit	Note
Clock input high voltage	V_{CH}		2.4	V_{CC}	V	
Clock input low voltage	V_{CL}		−0.3	0.8	V	
Input high voltage	V_{IH}		2.0	V_{CC}	V	
Input low voltage	V_{IL}		−0.3	0.8	V	
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4		V	
Output low voltage	V_{OL}	I_{OL}=+2.0mA		0.4	V	
Input leakage current	$\lvert I_{IL} \rvert$	0≦V_{IN}≦5.25V		10	μA	
Output leakage current	$\lvert I_{OL} \rvert$	0≦V_{IN}≦5.25V		10	μA	
Current consumption	I_{CC}			250	mA	

■ AC Characteristics

(1) CPU interface timing

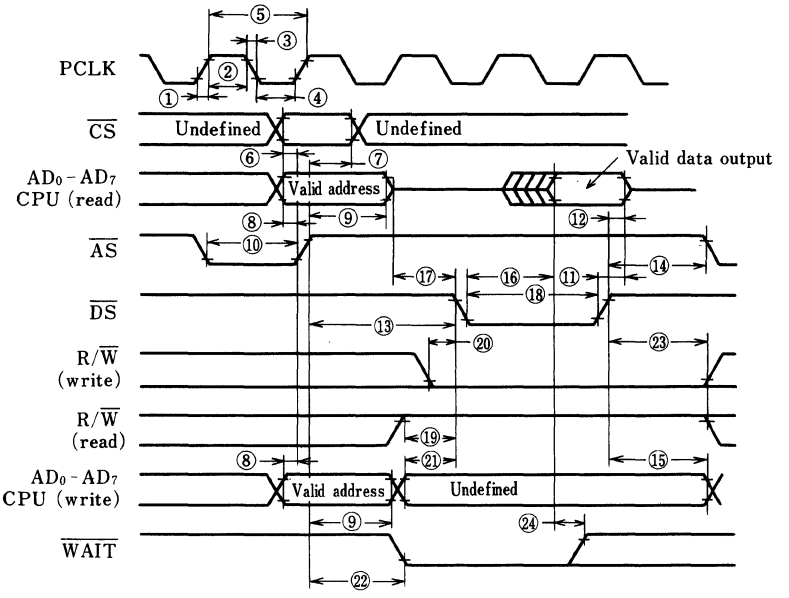
No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TrC	Clock rise time		20	ns	
2	TwCh	Clock pulse width, high	105		ns	
3	TfC	Clock fall time		20	ns	
4	TwCI	Clock pulse width, low	105		ns	
5	TpC	Clock period	250		ns	
6	TsCS (AS)	$\overline{CS}$ setup time to $\overline{AS}$ ↑	0		ns	1
7	ThCS (AS)	$\overline{CS}$ hold time from $\overline{AS}$ ↑	60		ns	1
8	TsA (AS)	Address setup time to $\overline{AS}$ ↑	30		ns	1
9	ThA (AS)	Address hold time from $\overline{AS}$ ↑	50		ns	1
10	TwAS	$\overline{AS}$ low pulse width	70		ns	
11	TdDS (DR)	Delay time from $\overline{DS}$ ↑ to invalid readout data	0		ns	
12	TdDS (DRz)	Delay time from $\overline{DS}$ ↑ to readout data fioating		70	ns	2
13	TdAS (DS)	Delay time from $\overline{AS}$ ↑ to $\overline{DS}$ ↓	60	2095	ns	
14	TdDS (AS)	Delay time from $\overline{DS}$ ↑ to $\overline{AS}$ ↓	50		ns	
15	ThDW (DS)	Written data hold time from $\overline{DS}$ ↑	30		ns	1
16	TdDS (DR)	Delay time from $\overline{DS}$ ↓ to readout data settlement				3
17	TdAz (DS)	Delay time from address floating to $\overline{DS}$	0		ns	
18	TwDS	$\overline{DS}$ low pulse width	390		ns	
19	TsRWR (DS)	R/$\overline{W}$ high (read) setup time to $\overline{DS}$ ↓	100		ns	
20	TsRWW (DS)	R/$\overline{W}$ low (write) setup time to $\overline{DS}$ ↓	0		ns	
21	TsDW (DSf)	Written data setup time to $\overline{DS}$ ↓	30		ns	
22	TdAS (W)	Delay time from $\overline{AS}$ ↑ to $\overline{WAIT}$ ↓		195	ns	
23	ThRW (DS)	R/$\overline{W}$ hold time from $\overline{DS}$ ↑	60		ns	
24	TsDR (W)	Time from vaild readout data to $\overline{WAIT}$	0		ns	

↑ indicates rising edge, ↓ indicates falling edge. The reference voltage levels for timing measurement are 2.0 volts 'high' ; 0.8 volt for 'low'.

Note 1: This does not apply to the interupt acknowledge operation.

Note 2: The Max. value of TdAS (DS) does not apply to the interrupt acknowledge operation.

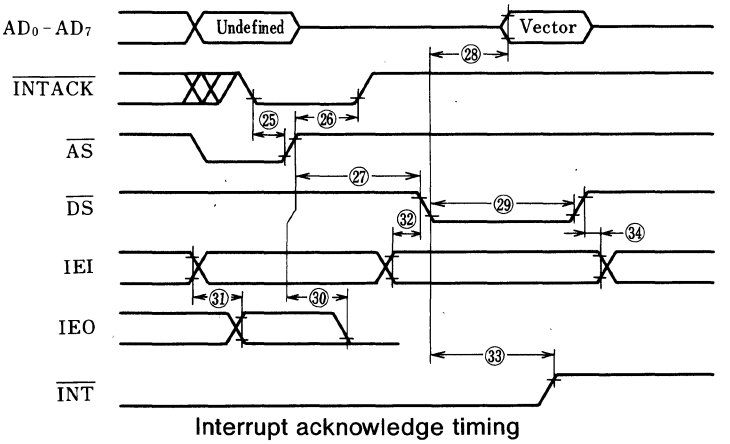
Note 3: The delay time depends on the status of LH8072 at the time of access by CPU.



CPU interface timing

(2) Interrupt acknowledge timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
25	TsIA (AS)	$\overline{INTACK}$ setup time to $\overline{AS}$ ↑	0		ns	
26	ThIA (AS)	$\overline{INTACK}$ low hold time from $\overline{AS}$ ↑	250		ns	
27	TdAS (DSA)	Delay time from $\overline{AS}$ ↑ to $\overline{DS}$ ↓ (acknowledge)	940		ns	
28	TdDSA (DR)	Delay time from $\overline{DS}$ ↓ (acknowledgge) to vector settlement		360	ns	
29	TwDSA	$\overline{DS}$ (acknowledgge) low pulse width	475		ns	
30	TdAS (IEO)	Delay time from $\overline{AS}$ ↑ to IEO		290	ns	
31	$TdIEI_f$ (IEO)	Delay time from IEI to IEO		120	ns	
32	TsIEI (DSA)	IEI setup time to $\overline{DS}$ ↓ (acknowledge)	150		ns	
33	TdDS (INT)	Delay time from $\overline{DS}$ ↓ to $\overline{INT}$		500	ns	
34	ThIEI (DS)	IEI hold time from $\overline{DS}$ ↑	100		ns	

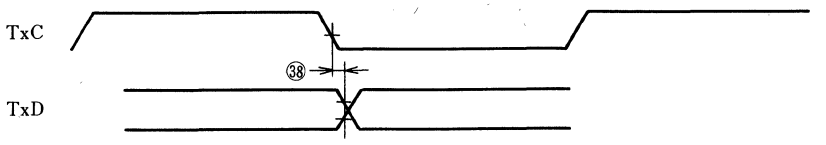


Interrupt acknowledge timing

(3) Serial port timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
38	TdTxC (TxD)	Delay time from sending clock transition to output data transistion		35000	ns	4

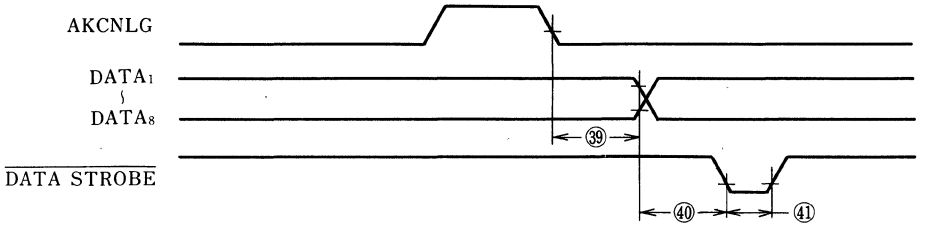
Note 4 : Applies to all baud rates (75-4800 B)



Serial port timing

(4) Parallel port timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
39	TaACK (D)	Time from ACKNLG ↓ to data output	24000		ns	
40	TdD (DSTR)	Time from data output to $\overline{\text{DATA STROBE}}$ ↓	6500		ns	
41	TwDSTR	$\overline{\text{DATA STROBE}}$ pulse width	6500		ns	



Parallel port timing

■ Registers

The LH8072 uses 64 bytes in the system input/output address space. Within this area, 14 bytes are assigned to the 1-byte registers (including data buffer, status, register, control register, etc.) which can directly be accessed by master CPU.

Table 1 lists the registers used for data transaction with the maser CPU and their addresses.

Table 1 Register input/output address

Address	Register
××00000×	Error status register(ERR)
××00001×	Mode setting register (MSR)
××00010×	Control register (CTL)
××00011×	Transmission status register (TxS)
××00100×	Reception status register (RxS)
××00101×	Printer status register (PRS)
××00110×	Transmission buffer (TxB)
××00111×	Reception buffer (RxB)
××01000×	Printer buffer (PRB)
××01001×	Transmission interrupt vector register (TxV)
××01010×	Reception interrupt vector register (RxV)
××01011×	Printer interrupt vector register (PRV)
××01100×	Error interrupt vector register (ERV)
××11110×	Master interrupt control register (MIC)

Note : A_{15}-A_6 is decoded and applied to $\overline{CS}$, so that the location in the input/output address space is determined. Bits marked by 'x' are undefined.

■ Programming

The LH8072 has 14 read/write registers which can be accessed directly by the master CPU.

(1) Initialization

The device is initialized in accordance with the following procedure.

(1) Following power-on reset, or master reset by software, set the mode register is programmed for character format, baud rate, stop bit and parity mode. Subsequently data required by control register* and interrupt vector registers* (transmission, reception and printer error interrupt vector registers) is programmed.
(2) Clear the error status register.
(3) Wait until the data transfer enable bit in the master interrupt control register is set to "1", making the LH8072 operable.

In case interrupt is used, the above polling operation is unnecessary. When transmission, reception and printer output become enable, interupt request is forwarded to the master CPU, indicating that the LH8072 has become operable.

Note: Registers marked by * can be set or revised even during the operation of LH8072.

(2) Data input/output

Data transfer between LH8072 and CPU is carried out in accordance with the following procedure.

(1) Poll the status registers (transmission, reception and printer status register) and wait until they become "1". In case interrupt (transmission, reception and printer interrupt) is used, interrupt occurs as soon as the value of each status register becomes "1", and polling is not necessary.
(2) After the status register has been set to "1" (or after interrupt has occurred), begin data transfer via the buffers (transmission, reception and printer buffers).
(3) Clear the status register. If the above operation is implemented using an interrupt routine, the interrupt-under-service (IUS) bit must be reset immediately before the end of each interupt routine.

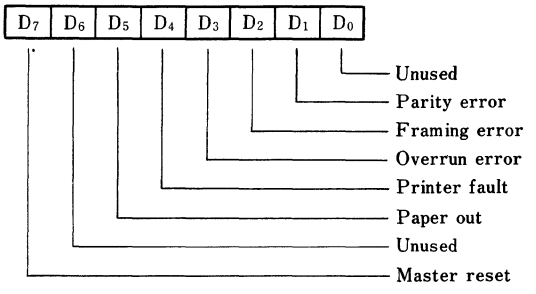


Fig. 1 Error status register (ERR)

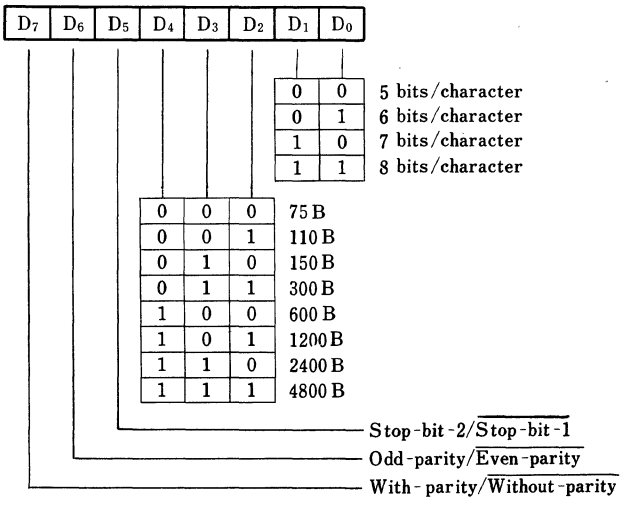


Fig. 2 Mode setting register (MSR)

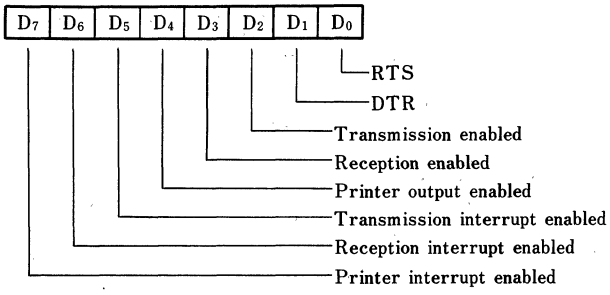


Fig. 3 Control register (CTL)

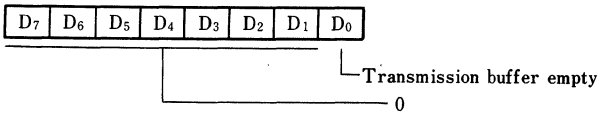


Fig. 4 Transmission status register (TxS)

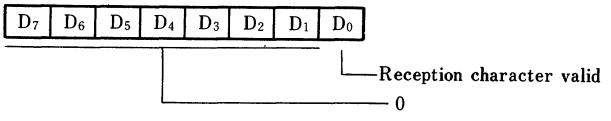


Fig. 5 Reception status register (RxS)

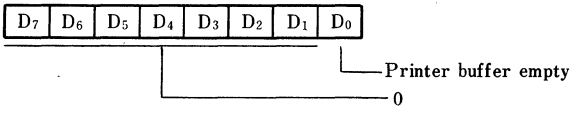


Fig. 6 Printer status register (PRS)

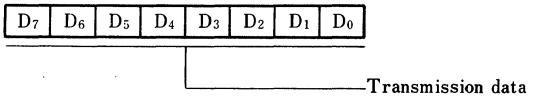


Fig. 7 Transmission buffer (TxB)

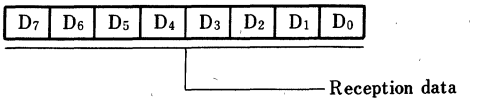


Fig. 8 Reception buffer (RxB)

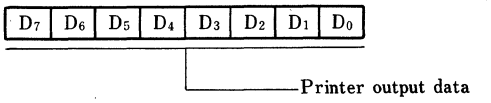


Fig. 9 Printer buffer (PRB)

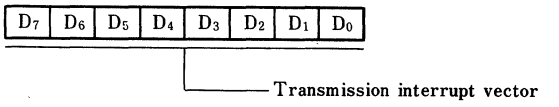


Fig. 10 Transmission interrupt vector register (TxV)

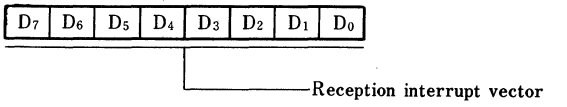


Fig. 11 Reception interrupt vector register (RxV)

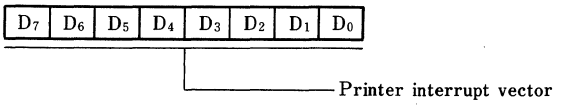


Fig. 12 Printer interrupt register (PRV)

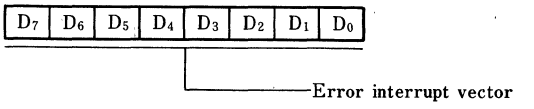


Fig. 13 Error interrupt vector register (ERV)

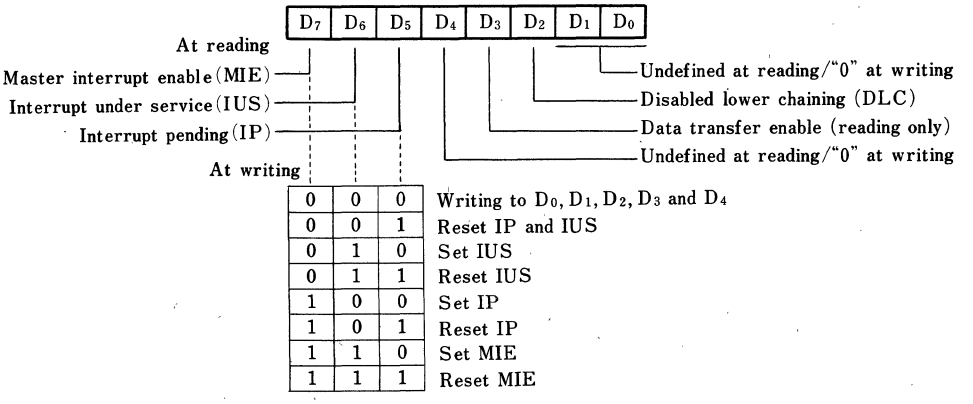


Fig. 14 Master interrupt control register (MIC)

LH8073 General Purpose Interface Bus Controller

Description

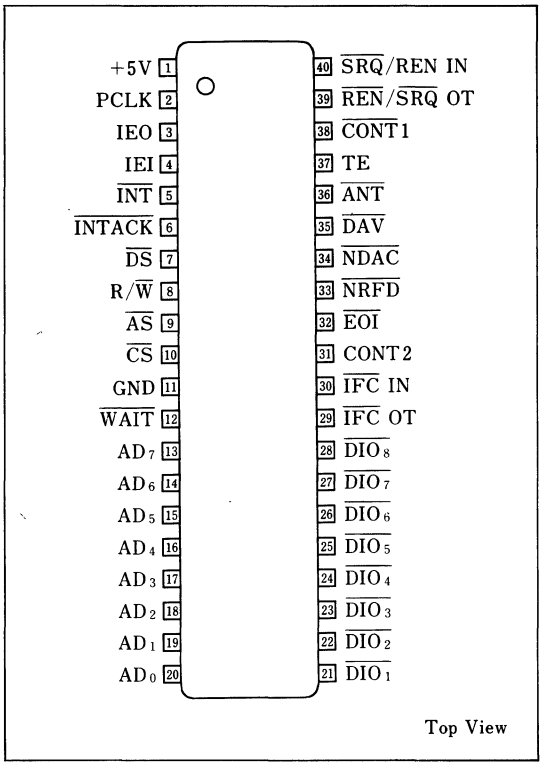
The LH8073 (GPIB73) is a microcomputer peripheral device used to control interface buses conforming to IEEE Std. 488-1978* (will be termed simply "GPIB") The GPIB is used extensively as a linkage bus between data gathering instrumentation devices and a microcomputer system.

The LH8073 incorporates three functions of talker, listener and controller, all integrated in one chip. Using this device, the GPIB interface can be provided for various instrumentation equipment, personal computers and office computers.

The LH8073 is applicable to a CPU bus where address and data are multiplexed. There is a complementary device LH8573 which is applicable for a CPU bus where address and data are not multiplexed.

*Note : The standard disclosed in IEEE Std. 488-1978 "IEEE Standard Digital Interface for Programmable Instrumentation" issued by IEEE, U.S.A.

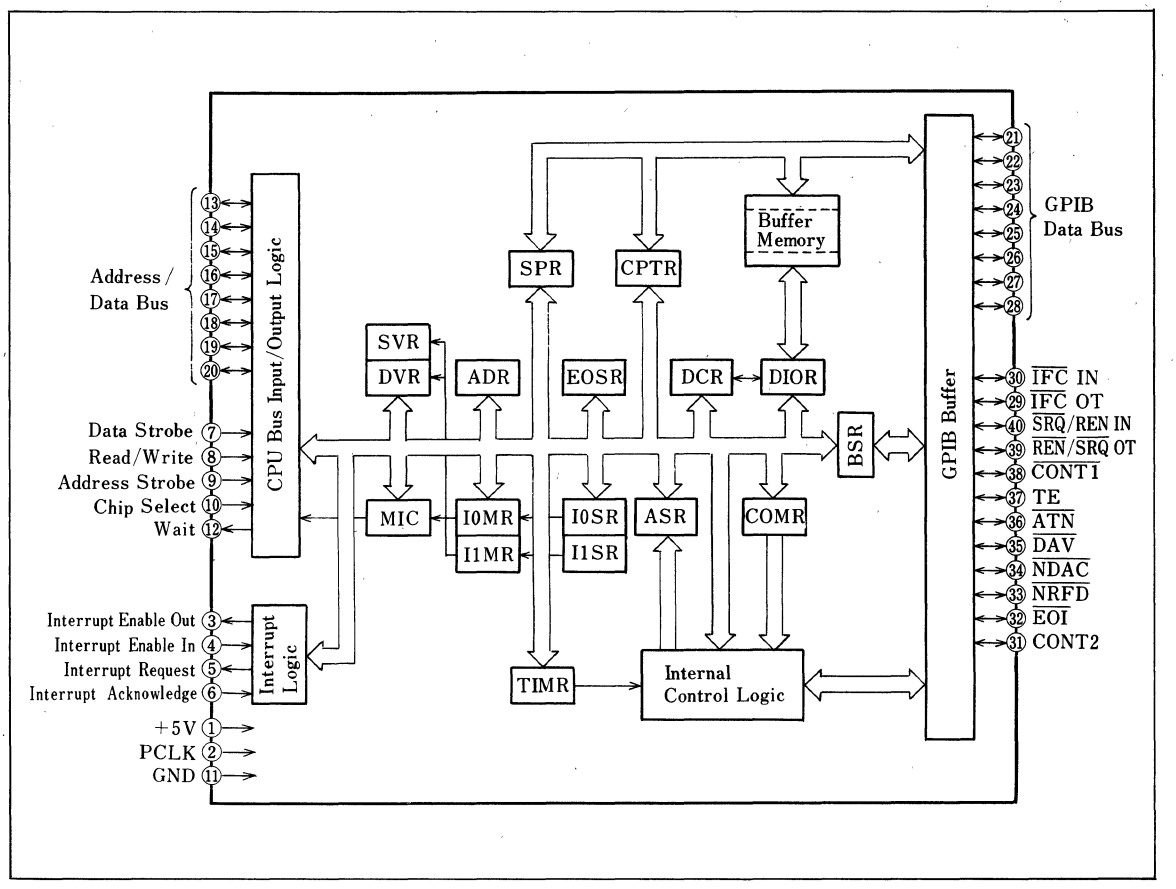
Pin Connections



Features

1. Built-in talker, listener and controller. Talker function, listener function and controller function are integrated in one chip.
2. Built-in buffer memory. Talker or listener can use 160-byte on-chip buffer.
3. EOI automatic transmission. Upon detection of the last byte of or EOS in talker mode, EOI signal is transmitted automatically.
4. EOS automatic detection. Upon reception of EOS in listener mode, the CPU is informed.
5. Built-in timer. The bus time-out period for handshaking can be set by the on-chip timer in the range of 200 μs-12 ms at 50 μs interval.
6. Interrupt function. Daisy-chain type interrupt arbitration facility is provided, allowing vectored interrupt to CPU.
7. Z-bus interface.

■ Block Diagram



LH8075 Multi Task Support Processor

■ Description

The LH8075(MTSP75)is the stand alone type multitask support processor providing multitask capabilities for any simple microcomputer system.

The concept of this multitask processing is similar to a conventional real time OS (operating system).

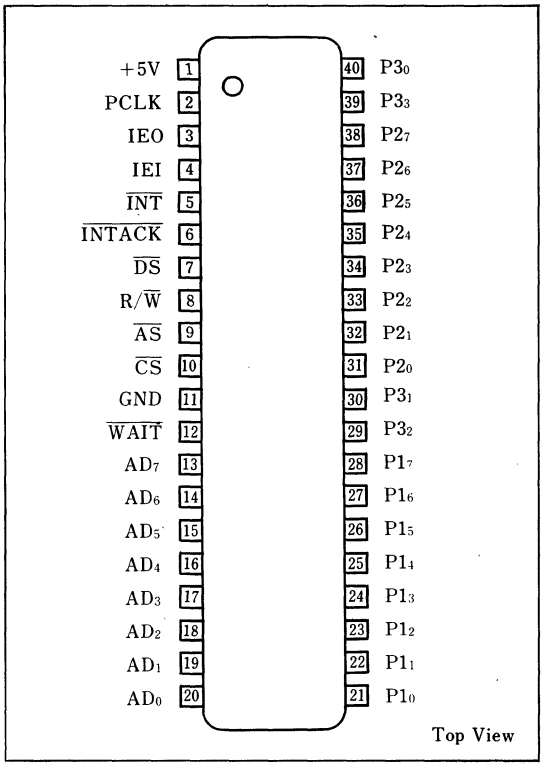
The devices perform task management (creating, deleting, etc.) independently of the master CPU, and carry out multitask processing for systems bus with arbitrary CPU architectures merely by connecting to the system bus.

User's programs are scheduled on a priority or time-sliced basis. Tasks are switched by an interrupt caused by the LH8075, and commands are given to the LH8075 by writing parameters and command numbers in the specified register in the LH8075.

■ Features

1. Task management
   - Up to eight tasks can be controlled concurrently. By using the task creating and deleting technique, a maximum of 255 tasks can be handled.
   - Tasks can be controlled on a priority basis by the assignment of 255 priority levels.
2. Inter-task communication
   - Inter-task communication is possible using the "mail box" provided within the LH8075.
   - Inter-task synchronization is possible using the "mail box".
3. Built-in timer
   - Timers with ranges from 10ms to 255 hours can be used for time-sliced processes and checking I/O wait time.
   - These times can be set independently for each task.
4. Bulit-in clock.Time (hours, minutes and seconds) can be set and read out.
5. 20-bit general-purpose I/O port
   - Two 8-bit ports operable in bit input/output
   - 2-bit input ports and 2-bit output ports.
   - Tasks can be resumed using the 2-bit input ports.
6. Memory assignment
   - Working memory areas can be assigned to each task.

■ Pin Connections



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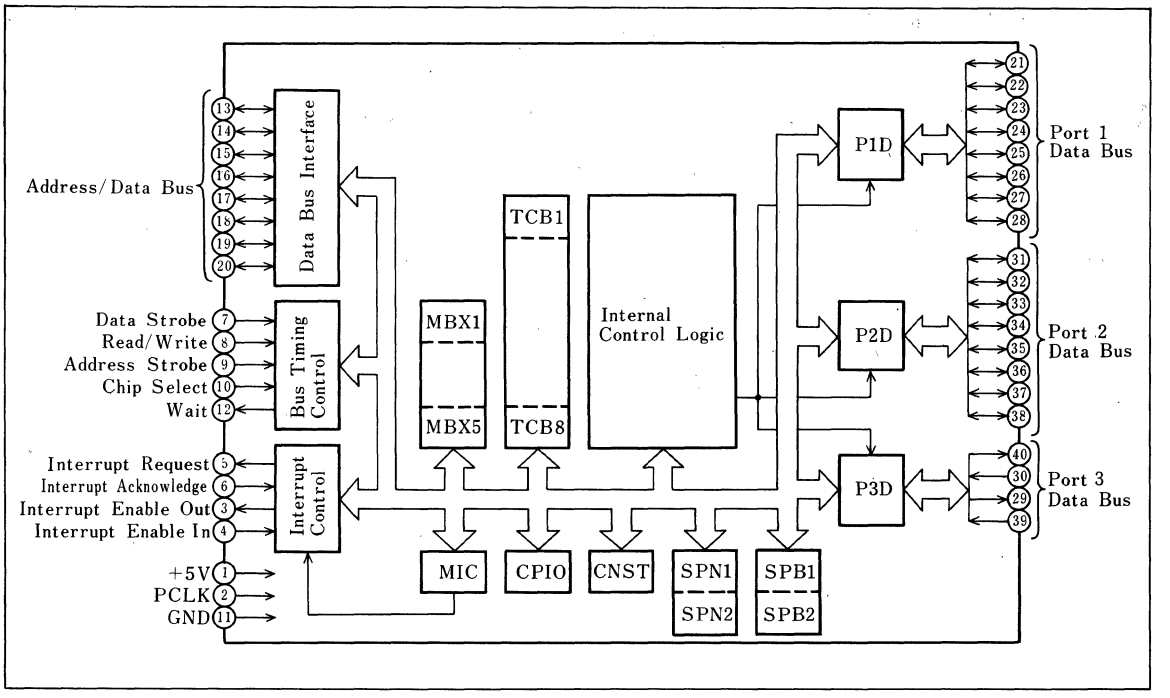
Block Diagram

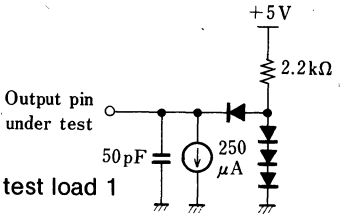


Pin Description

Pin	Meaning	I/O	Function
$AD_0 \sim AD_7$	Address/data bus	Bidirectional 3-state	Multiplexed system address/data bus.
$\overline{AS}$	Address strobe	I	Active low. Fetch information on address/data bus as address.
$\overline{DS}$	Data strobe	I	Active low. Transact information on address/data bus as data.
R/$\overline{W}$	Read/write	I	High at reading. Output contents of internal register on address/data bus ; Low at writing. Fetch data on address/data bus.
$\overline{CS}$	Chip select	I	Active low. Chip selection signal
$\overline{WAIT}$	Wait	O	Active low, open-drain. Used to synchronize CPU.
$\overline{INT}$	Interrupt request	O	Active low, open-drain. Indicate interrupt request to CPU.
$\overline{INTACK}$	Interrupt acknowledge	I	Active low. Indicate interrupt acknowledge cycle
IEI	Interrupt enable input	I	Active high. Used to form interrupt priority arbitration loop circuit (daisy chain).
IEO	Interrupt enable output	O	Active high. Used to form daisy chain.
$P1_0 \sim P1_7$	I/O port lines	I/O	Parallel input/output
$P2_0 \sim P2_7$	I/O port lines	I/O	Parallel input/output
$P3_0 \sim P3_3$	I/O port lines	I/O	Parallel input/output
PCLK	Clock	I	Single-phase clock, need not be same as CPU clock.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3～+7	V
Output voltage	V_{OUT}	−0.3～+7	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−65～+150	℃



Standard test load 1

■ DC Characteristics

(V_{CC}=5V±5%, GND=0V, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Clock input high voltage	V_{CH}		2.4	V_{CC}	V
Clock input low voltage	V_{CL}		−0.3	0.8	V
Input high voltage	V_{IH}		2	V_{CC}	V
Input low voltage	V_{IL}		−0.3	0.8	V
Output low voltage	V_{OH}	I_{OH}=−250 μA	2.4		V
Output low voltage	V_{OL}	I_{OL}=2mA		0.4	V
Inptt leakage current	$\lvert I_{IL} \rvert$	0≦V_{IN}≦5.25V		10	μA
Output leakage current	$\lvert I_{OL} \rvert$	0≦V_{IN}≦5.25V		10	μA
Current consumption	I_{CC}			250	mA

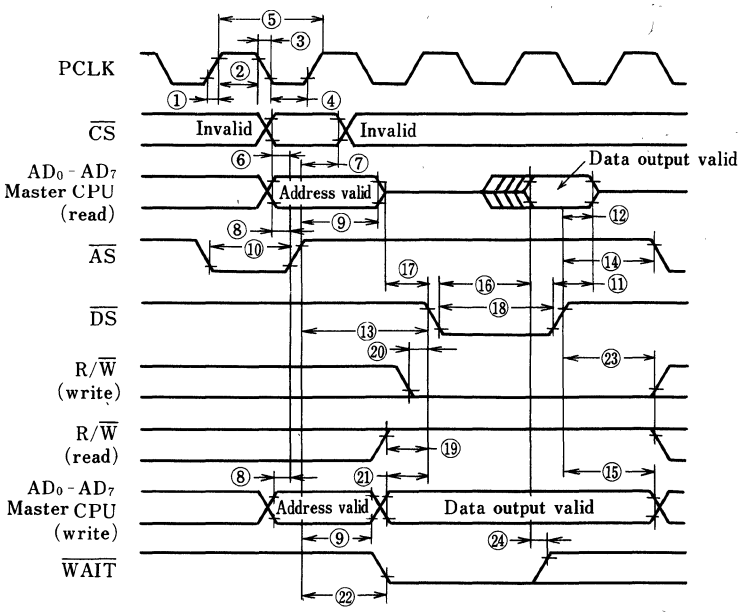
■ AC Characteristics

(1) Master CPU interface timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TrC	Clock rise time		20	ns	
2	TwCh	Clock pulse width, high	105		ns	
3	TfC	Clock fall time		20	ns	
4	TwCl	Clock pulse width, low	105		ns	
5	TpC	Clock period	250		ns	
6	TsCS (AS)	$\overline{CS}$ setup time to $\overline{AS}$ ↑	0		ns	1
7	ThCS (AS)	$\overline{CS}$ hold time from $\overline{AS}$ ↑	60		ns	1
8	TsA (AS)	Address setup time to $\overline{AS}$ ↑	30		ns	1
9	ThA (AS)	Address hold time from $\overline{AS}$ ↑	50		ns	1
10	TwAS	$\overline{AS}$ low pulse width	70		ns	
11	TdDS (DR)	Delay time from $\overline{DS}$ ↑ to invalid readout data	0		ns	
12	TdDS (DRz)	Delay time from $\overline{DS}$ ↑ to readout data floating		70	ns	2
13	TdAS (DS)	Delay time from $\overline{AS}$ ↑ to $\overline{DS}$ ↓	60	2095	ns	
14	TdDS (AS)	Delay time from $\overline{DS}$ ↑ to $\overline{AS}$ ↓	50		ns	
15	ThDW (DS)	Written data hold time from $\overline{DS}$ ↑	30		ns	1
16	TdDS (DR)	Delay time from $\overline{DS}$ ↓ to readout data settlement			ns	3
17	TdAz (DS)	Delay time from address floating to $\overline{DS}$ ↓	0		ns	
18	TwDS	$\overline{DS}$ low pulse width	390		ns	
19	TsRWR (DS)	R/$\overline{W}$ high (read) setup time to $\overline{DS}$ ↓	100		ns	
20	TsRWW (DS)	R/$\overline{W}$ low (write) setup time to $\overline{DS}$ ↓	0		ns	
21	TsDW (DSf)	Written data setup time to $\overline{DS}$ ↓	30		ns	
22	TdAS (W)	Delay time from $\overline{AS}$ ↑ to $\overline{WAIT}$ ↓		195	ns	
23	ThRW (DS)	R/$\overline{W}$ hold time from $\overline{DS}$ ↑	60		ns	
24	TsDR (W)	Time from valid readout data to $\overline{WAIT}$ ↑	0		ns	

The reference voltage levels for timing measurement are 2.0 volts for 'high' ; 0.8 volt for 'low'. All output paramaters are measured under the stated load conditions.

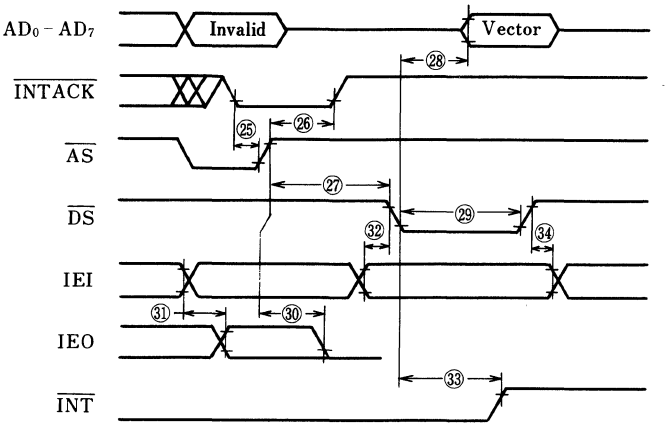
Note 1: This does not apply to the interrupt acknowledge operation.
Note 2: The Max. value of TdAS (DS) does not to the interrupt acknowledge operation.
Note 3: The delay time depends on the status of LH8075 at the time of access by master CPU.



Master CPU interface timing

(2) Interrupt acknowledge timing

No.	Symbol	Parameter	MIN.	MAX.	Unit
25	TsIA (AS)	$\overline{\text{INTACK}}$ setup time to $\overline{\text{AS}}$ ↑	0		ns
26	ThIA (AS)	$\overline{\text{INTACK}}$ low hold time from $\overline{\text{AS}}$ ↑	250		ns
27	TdAS (DSA)	Delay time from $\overline{\text{AS}}$ ↑ to $\overline{\text{DS}}$ ↓ (acknowledge)	940		ns
28	TdDSA (DR)	Delay time from $\overline{\text{DS}}$ ↓ (acknowledge) to vector settlement		360	ns
29	TwDSA	$\overline{\text{DS}}$ (acknowledge low pulse width	475		ns
30	TdAS (IEO)	Delay time from $\overline{\text{AS}}$ ↑ to IEO		290	ns
31	TdIEIf (IEO)	Delay time from IEI to IEO		120	ns
32	TsIEI (DSA)	IEI setup time to $\overline{\text{DS}}$ ↓ (acknowledge)	150		ns
33	TdDS (INT)	Delay time from $\overline{\text{DS}}$ ↓ to $\overline{\text{INT}}$ ↑		500	ns
34	ThIEI (DS)	IEI hold time from $\overline{\text{DS}}$ ↑	100		ns

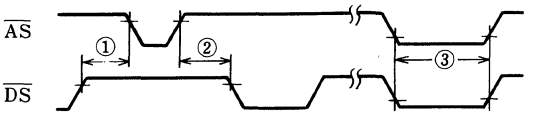


Interrupt acknowledge timing

(3) Reset timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TdRDQ (WR)	Delay time from $\overline{\text{DS}}$ ↑ (for suppressing reset) to $\overline{\text{AS}}$ ↓	40		ns	
2	TdWRQ (RD)	Delay time from $\overline{\text{AS}}$ ↑ (for suppressing reset) to $\overline{\text{DS}}$ ↓	50		ns	
3	TwRES	Minimum low width of $\overline{\text{AS}}$ and $\overline{\text{DS}}$ (for resetting)	250		ns	1

Note 1: The internal reset signal lags 1/2 to 2 clocks behind external reset conditions.

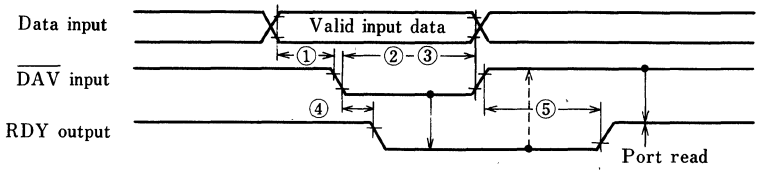


Reset timing

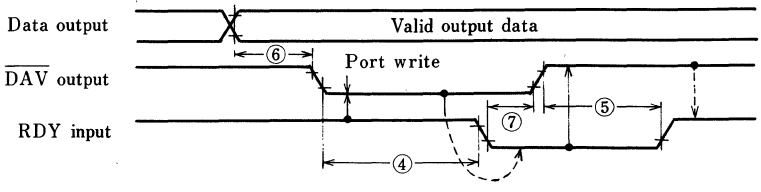
(4) Handshaking timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TsDI (DA)	Data setup time	0		ns	
2	ThDA (DI)	Data hold time	230		ns	
3	TwDA	$\overline{DAV}$ width	175		ns	1,2
4	TdDAL (RY)	Delay time from $\overline{DAV}$ low to RDY	20	175	ns	1,2
			0		ns	2,3
5	TdDAH (RY)	Delay time from $\overline{DAV}$ high to RDY		150	ns	1,2
			0		ns	2,3
6	TdDO (DA)	Delay time from data output to $\overline{DAV}$	50		ns	2
7	TdRY (DA)	Delay time from RDY to $\overline{DAV}$	0	205	ns	2

Note 1: Input handshaking
Note 2: Measured under the stated load conditions.
Note 3: Output handshaking



Input handshaking timing



Serial port timing

■ Basic Specifications

Table 1 LH8075 basic specifications

Parameter	Performance
Task control function	
Number of tasks registered	Max. 255; task number: hex 01-FF
Number of tasks controlled simultaneously	Max. 8
Priority level	Max. 255; priority level: hex 01-FF
Mail box	Max. 5; mail box number: hex 01-05
Unit clock	10 ms
Scheduling	Priority order or time division; Task is switched by interrupt from LH8075.
Memory allocation	User's RAM is segmented in units of hex 100 bytes; Arbitrary area ranging hex 0000-FFFF can be controlled.
Clock function	Time (hour, minute, second) setting and readout
Parallel data input/output function	Two 8-bit I/O ports and one 4-bit I/O port

■ Registers

The LH8075 has the following registers which can be accessed externally (from CPU).

(1) Task control

CPIO (Command parameter register)

This register writes the writing parameter previous to command writing. The readout parameter is placed in CPIO upon completion of command execution.

CNST(Command/status register)

This register is used to write a command. Execution information of executed command is placed in CNST upon completion of command execution.

SPN1, SPN2 (New task stack pointer registers)

At occurrence of interrupt for task switching, execution starting address information for the new task is placed in this register.

SPB1, SPB2 (Old task stack pointer registers)

At occurrence of interrupt for task switching, execution end address information for the executed task is written in this register.

MIC (Master CPU interrupt control register)

Interrupt related parameters including interrupt enable (IE), interrupt pending (IP) and interrupt-under-service (IUS) bits are set or reset in this register.

(2) I/O ports

P1D, P2D, P3D (port 1, 2, 3 data registers)

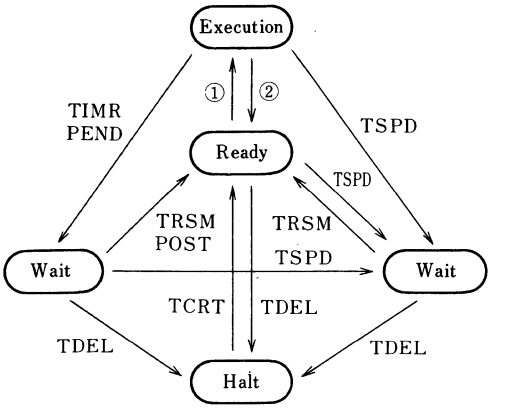
These registers are used to transact data via port 1, port 2, and port 3.

Table 2 lists the register addresses.

Teble 2 Register address

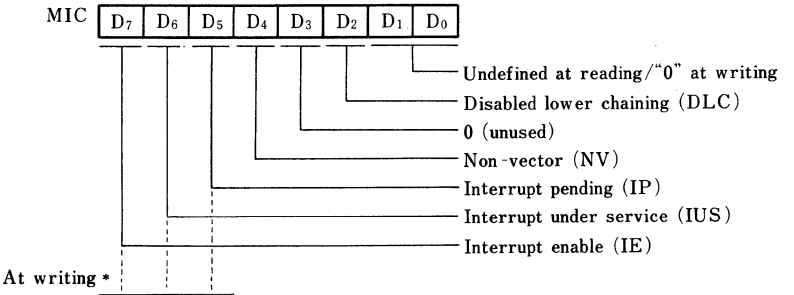
Register	Address
P1D	××00001×
P2D	××00010×
P3D	××00011×
CNST	××00110×
SPN1	××00111×
SPN2	××01000×
SPB1	××01001×
SPB2	××01010×
CPIO	××10101×
MIC	××11110×

Note 1: Bits marked by 'x' may be either '0' or '1'.
Note 2: LH8075 uses 64 input/output address locations.



(1) Task in execution releases CPU.
(2) ○ Higher ranking task becomes ready.
○ Time-up by time division
○ TNXT

Fig. 1 Task status



At writing *

0	0	0	Writing to D_2 and D_4
0	0	1	Reset IP and IUS
0	1	0	Set IUS
0	1	1	Reset IUS
1	0	0	Set IP
1	0	1	Reset IP
1	1	0	Set IE
1	1	1	Reset IE

* : IP, IUS and IE bits are set or reset by writing in these codes.

Fig. 2 MIC bit configuration

■ Programming

The following describes the task control procedure using LH8075.

(1) **Initialization**

(1) The LH8075 causes interrupt for task switching

However, in order to process, a separate interrupt processing routine must be prepared.

(2) Each task is provided with a stack area. Task starting address and initial values for all registers are written at the top of each stack area.

(3) LH8075 is initialized. Table 3 lists the initialization information to be written in LH8075.

(4) When necessary, the clock is set and the port mode is specified.

(5) Initialization completed. To transfer control from the initialization routine to a task, the task execution command (TSTR) must be executed.

Table 3 System information registered at initialization

Order	Item	Contents	
1	Vector	LH8075 interrupt vector for task switching	
2	RAM table	User RAM start address (high order byte)	
3		User RAM end address (high order byte)	
4	Task table	Task 1	Task number (hex 01-FF)
5			Priority level (hex 01-FF)
6			Task stack pointer (high order or low order byte)
7			Task stack pointer (low order or high order byte
⋮		⋮	⋮
4n		Task n	Task number (hex 01-FF)
4n+1			Priority level (hex 01-FF)
4n+2			Task stack pointer (high order or low order byte)
4n+3			Task stack pointer (low order or high order byte)

(2) **Command execution**

Table 4 lists the commands of LH8075, and Table 5 lists the command execution information. In writing commands into LH8075 the following data entry procedure applies.

(1) Write parameters needed in writing command into CPIO in the order shown in Table 4. Commands with blank parameter field in Table 4 do not require writing

(2) Write the command number in CNST.

(3) It is necessary to confirm the completion of command execution by polling D_7 in CNST (D_7 becomes "1" upon completion of command execution). For commands without readout parameter, procedure is completed and the following procedures are unnecessary. Commands with readout parameter (CGET, MALC and PEND) further require the following procedures.

(4) When D_6=1 in CNST (indicating the readout parameter is prepared in CPIO), parameter is read out from CPIO.

(5) Upon completion of parameter readout, PRME command must be executed to notify LH8075 of the parameter readout completion.

(6) Wait until CNST D_7 becomes "1" to confirm the completion of command execution.

Table 4 Command table

No.	Command name	Function	Writing parameter	Readout parameter	Remarks
00_H	INIT	LH8075 initialization	1. Total number of tasks		
01_H	TSTR	Termination of LH8075 initialination and start of task execution			
02_H	TCRT	Task creation	1. Task number 2. Priority level 3. SP (high order or low order byte) 4. SP (low order or high order byte)		
03_H	TDEL	Task deletion	1. Task number		
04_H	TRSM	Task resumption	1. Task number		
05_H	TSPD	Task suspension	1. Task number 2. control switch		See paragraph(1) .
06_H	TPRI	Task priority change	1. Task number 2. New priority		
07_H	TSLI	Task time-slicing process	1. Priority 2. Time base 3. Count		See paragraph(2) .
08_H	TNXK	Swapping of task during time-sliced execution			
09_H	TIMR	Timer setting	1. control code 2. Count		See paragraph(3) .
OA_H	CSET	Clock setting	1. Hour 2. Minute 3. Second		
OB_H	CGET	Clock readout		1. Hour 2. Minute 3. Second	*
OC_H	MALC	Memory allocation	1. Number of memory blocks required	1. Allocated memory address	*
OD_H	MREL	Memory release			
OE_H	POST	Message transmission	1. Mail box number 2. Message data 1 3. Message data 2 4. Message data 3 5. Message data 4		See paragraph(4) .
OF_H	PEND	Message reception	1. Mail box number	1. Message data 1 2. Message data 2 3. Message data 3 4. Message data 4	*
10_H	PMOD	Port mode setting	1. Port-1 mode 2. Port-2 mode 3. Port-3 mode		See paragraph(5) .
11_H	PRME	End of parameter readout			

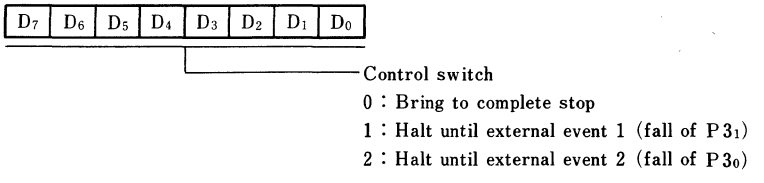
Note 1: Commands marked by '*' require PRME command execution at parameter readout completion.
Note 2: Numerals given in 'writing parameter' and 'readout parameter' indicate the order of writing and reading.
Note 3: Numerals in 'remarks' indicate the reference number of supplementary explanation.

Table 5 Command execution information

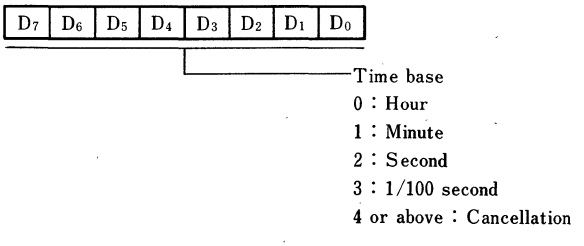
Code	Command name	Execution	Code	Command name	Execution
00_H	INIT	0 Normal termination 1 Task number or priority setting error 2 Double specification of same task number 3 Total number of tasks equal to 0 or larger than 8, Initialized information error, RAM table error	06_H	TPRI	0 Normal termination 1 Task number or priority setting error 2 Specified task not yet created
			07_H	TSLI	0 Normal termination 1 Priority error or data error 5 Cancellation without setting
			08_H	TNXT	0 Normal termination
01_H	TSTR	0 Normal termination 3 Initial information not yet set	09_H	TIMR	0 Normal termination 1 Data error 5 Cancellation without setting 8 Resuming by TRSM
02_H	TCRT	0 Normal termination 1 Task number or priority setting error 2 Already created 3 Control tasks more than 8	$0A_H$	CSET	0 Normal termination 1 Data error
03_H	TDEL	0 Normal termination 1 Task number error 2 Specified task not yet created 4 Specify self	$0B_H$	CGET	0 Normal termination
			$0C_H$	MALC	0 Normal termination 6 Allocation disabled
			$0D_H$	MREL	0 Normal termination 5 Memory not yet allocated
04_H	TRSM	0 Normal termination 1 Task number error 2 Specified task not yet created 4 Specify self 5 Specification of task in ready status	$0E_H$	POST	0 Normal termination 1 Mail box number error or message data error 7 Mail box busy
05_H	TSPD	0 Normal termination 1 Task number or control switch number error 2 Specified task not yet created 3 Control switch setting error 5 Specification of task in halt staus	$0F_H$	PEND	0 Normal termination 1 Mail box number error 8 TRSM command issued by other task or time out
			10_H	PMOD	0 Normal termination
			11_H	PRME	0 Normal termination

■ Supplement for writing parameter

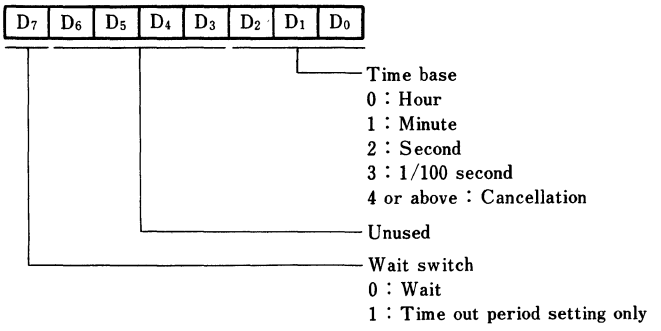
〔1〕 2. Control switch



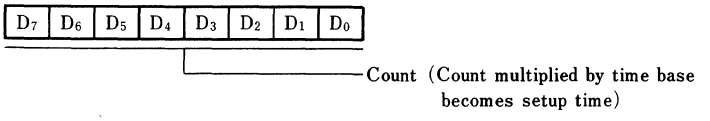
〔2〕 2. Time base



〔3〕 1. Control code

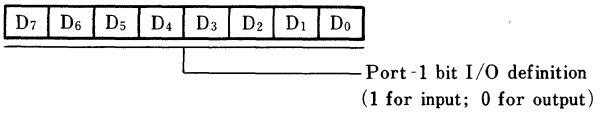


2. Count

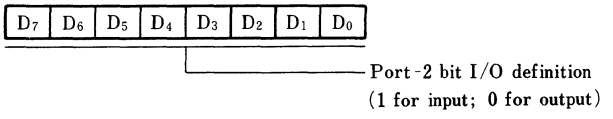


〔4〕 2. Only in message data 1, '0' is not allowed.

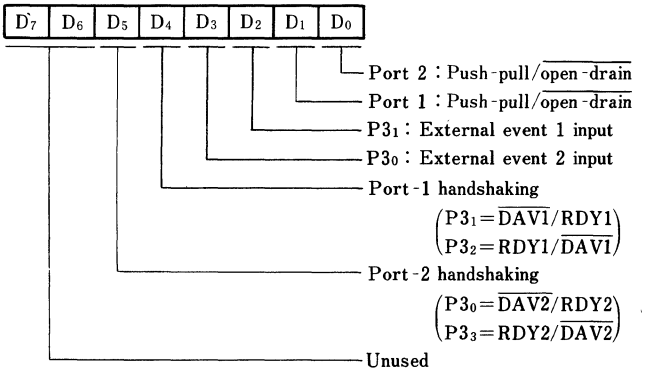
〔5〕 1. Port-1 mode



2. Port-2 mode



3. Port-3 mode



LH8090/LH8090A Z8090/Z8090A Universal Peripheral Controller

Description

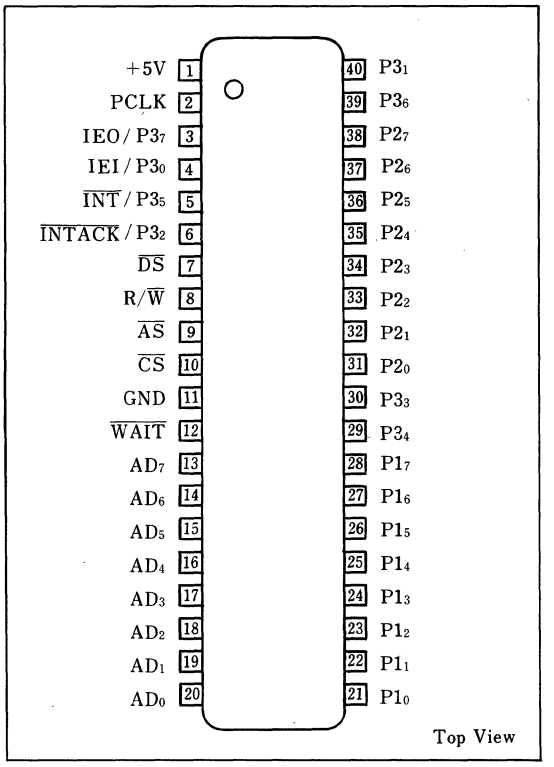
The LH8090 Universal Peripheral Controller (UPC) is an intelligent peripheral controller for distributed processing applications. The LH8090 unburdens the host processor by assuming tasks traditionally done by the host (or by added hardware), such as performing arithmetic, translating or formatting data, and controlling I/O devices. Based on the Z8 microcomputer architecture and instruction set, the LH8090 contains 2K bytes of internal program ROM, a 256-byte register file, three 8-bit I/O ports, and two counter/timers.

The LH8090 offers fast execution time; an effective use of memory; and sophisticated interrupt, I/O, and bit manipulation. Using a powerful and extensive instruction set combined with an efficient internal addressing scheme, the LH8090 speeds program execution and efficiently packs program code into the on-chip ROM.

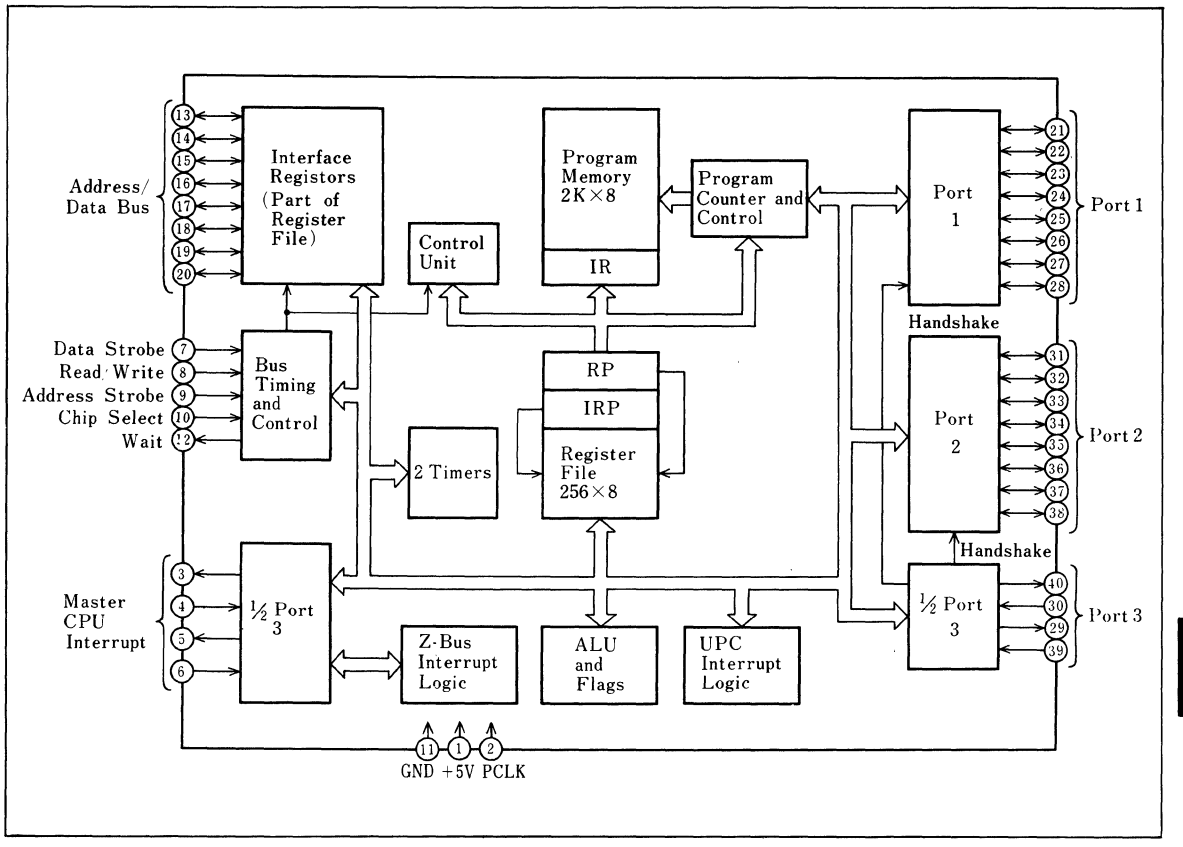
Features

1. Complete slave microcomputer, for distributed processing Z-bus use
2. Unmatched power of Z8 architecture and instruction set
3. Three programmable I/O ports, two with optional 2-Wire Handshake
4. Six levels of priority interrupts from eight sources: six from external sources and two from internal sources
5. Two programmable 8-bit counter/timers each with a 6-bit prescaler. Counter/Timer T0 is driven by an internal source, and Counter/Timer T1 can be driven by internal or external sources. Both counter/timers are independent of program execution
6. 256-byte register file, accessible by both the master CPU and LH8090, as allocated in the LH8090 program
7. 2K bytes of on-chip ROM for efficiency and versatility

Pin Connections



Block Diagram



Pin Description

Pin	Meaning	I/O	Function
$AD_0 \sim AD_7$	Address data bus	Bidirectional	Multiplexed system address/data bus.
$\overline{AS}$	Address strobe	I	Active low. Causes information on the address/data bus to be fatched as address
$\overline{DS}$	Data strobe	I	Active low. Causes information on the address/data bus to be sent/received as data
R/$\overline{W}$	Read/write	I	A high level indicates a read cycle : Data is output from the internal register to the address/data bus. A low level indicates a write cycle : Data is fetched from the address/data bus.
$\overline{CS}$	Chip select	I	Active low, Chip select signal.
$\overline{WAIT}$	Wait	O	Active low, open-drain. For synchronizaion with the CPU.
$P1_0 \sim P1_7$	I/O port lines	I/O	Parallel I/O
$P2_0 \sim P2_7$	I/O port lines	I/O	Parallel I/O
$P3_0 \sim P3_7$	I/O port lines	I/O	Parallel I/O (4-bit input, 4-bit output)
PCKL	Clock	I	Signal-phase clock, not need to be related to the CPU clock.

■ Absolute Maximum Ratings

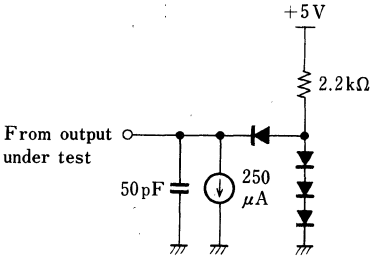
Parameter	Symbol	Ratings	Unit
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	°C
Storage temperature	T_{stg}	−65～+150	°C

* The maximum applicable voltage on any pin except for V_{BB}, with respect to GND.

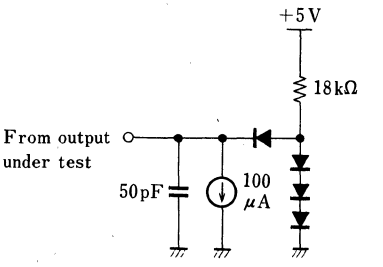
■ Standared Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as followes .

$4.75V \leqq V_{CC} \leqq 5.25V$
$V_{SS} = GND = 0V$
$0°C \leqq Ta \leqq +70°C$



Standard test load 1



Standard test load 2

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP	MAX.	Unit	Note
Clock input high voltage	V_{CH}		2.4		V_{CC}	V	
Clock input low voltage	V_{CL}		−0.3		0.8	V	
Input high voltage	V_{IH}		2.0		V_{CC}	V	
Input low voltage	V_{IL}		−0.3		0.8	V	
Output high voltage	V_{OH}	I_{OH} = −250μA	2.4			V	1
Output low voltage	V_{OL}	I_{O2} = +2.0mA			0.4	V	1
Input leakage current	$\|I_{IL}\|$	$0 \leqq V_{IN} \leqq 5.25V$			10	μA	
Output leakage current	$\|I_{OL}\|$	$0 \leqq V_{IN} \leqq 5.25V$			10	μA	
V_{CC} supply current	I_{CC}				250	mA	

Note 1: For A_0-A_{11}, D_0-D_7, $\overline{MDS}$, $\overline{SYNC}$, $\overline{MAS}$, and MR/$\overline{W}$/IACK of the device for 64-pin development, I_{OH}=100 μA and I_{OL} 1mA

■ AC Characteristics

(1) Master CPU interface timing

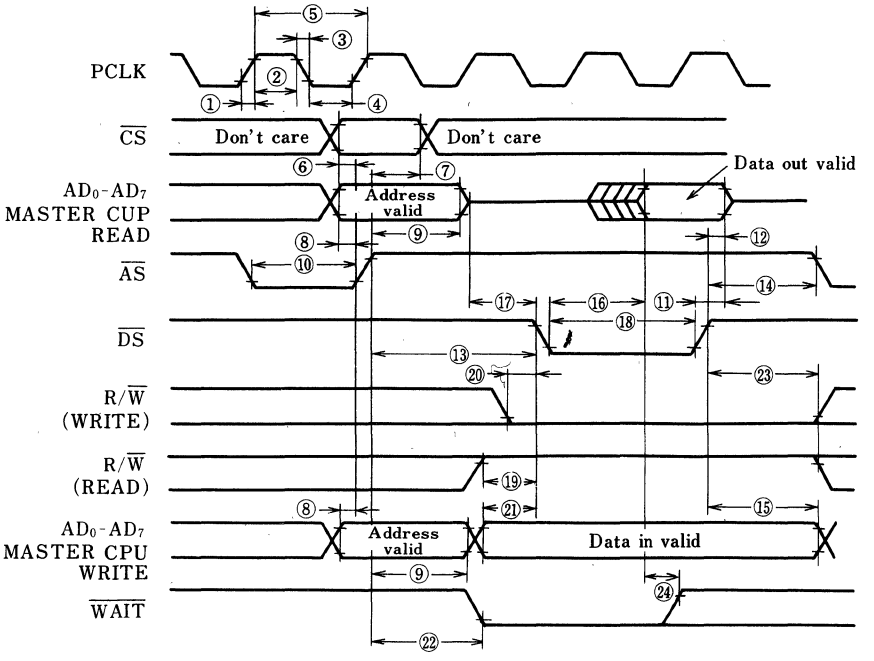
No.	Symbol	Parameter	LH8090		LH8090A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TrC	Clock rise time		20		15	ns	
2	TwCh	Clock high width	105	1855	70	1855	ns	
3	TfC	Clock fall time		20		10	ns	
4	TwCl	Clock low width	105	1855	70	1855	ns	
5	TpC	Clock period	250	2000	165	2000	ns	
6	TsCS(AS)	$\overline{CS}$ to $\overline{AS}$ ↑ setup time	0		0		ns	1
7	ThCS(AS)	$\overline{CS}$ to $\overline{AS}$ ↑ hold time	60		40		ns	1
8	TsA(AS)	Address to $\overline{AS}$ ↑ setup time	30		10		ns	1
9	ThA(AS)	Address to $\overline{AS}$ ↑ hold time	50		30		ns	1
10	TwAS	$\overline{AS}$ low width	70		50		ns	
11	TdDS(DR)	$\overline{DS}$ ↑ to read data not valid	0		0		ns	
12	TdDs(DRz)	$\overline{DS}$ ↑ to read data float delay		70		45	ns	2
13	TdAS(DS)	$\overline{AS}$ ↑ $\overline{DS}$ ↓ delay	60	2095	40	2095	ns	
14	TdDS(AS)	$\overline{DS}$ ↑ $\overline{AS}$ ↓ delay	50		35		ns	
15	ThDW(DS)	Write data to $\overline{DS}$ ↑ hold time	30		20		ns	1
16	TdDS(DR)	$\overline{DS}$ ↓ to read data valid delay					ns	3
17	TdAz(DS)	Address float to $\overline{DS}$ delay	0		0		ns	
18	TwDS	$\overline{DS}$ low width	390		250		ns	
19	TsRWR(DS)	R/$\overline{W}$(read) to $\overline{DS}$ ↓ setup time	100		80		ns	
20	TsRWW(DS)	R/$\overline{W}$(write) to $\overline{DS}$ ↓ setup time	0		0		ns	
21	TsDW(DSf)	Write data to $\overline{DS}$ ↓ setup time	30		20		ns	
22	TdAS(W)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ valid delay		195		160	ns	
23	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ hold time	60		40		ns	
24	TsDR(W)	Read data valid to $\overline{WAIT}$ ↑	0		0		ns	

Note : The timing characteristics given reference 2.0V as High and 0.8V as Low.
All output AC parameters use test load 1.

Note 1: Parameter does apply to interrupt acknowledge transactions.

Note 2: The maximum value for TdAS (DS) does not apply to interrupt acknowledge transcations.

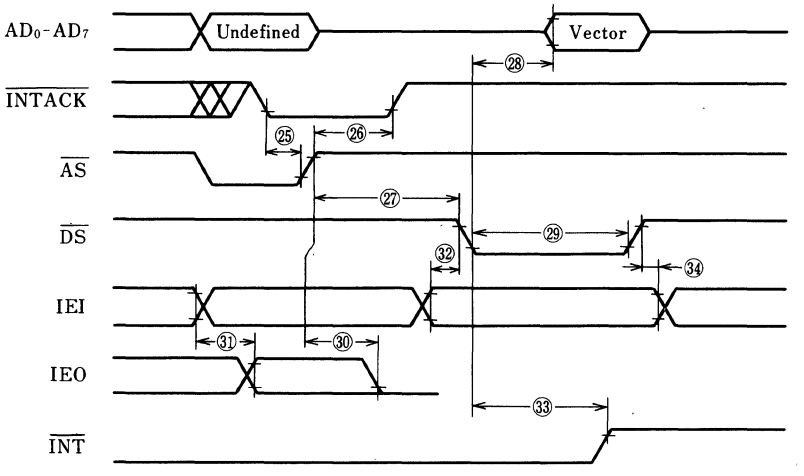
Note 3: This parameter is dependent on the state of UPC at the time of master CPU access.



Master CPU interface timing

(2) Interrupt acknowledge timing

No.	Symbol	Parameter	LH8090		LH8090A		Unit
			MIN.	MAX.	MIN.	MAX.	
25	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ setup time	0		0		ns
26	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ hold time	250		250		ns
27	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (acknowledge) delay	940		200		ns
28	TdDSA(DR)	$\overline{DS}$ ↓ (acknowledge) to read data valid delay		360		180	ns
29	TwDSA	$\overline{DS}$ ↓ (acknowledge) low width	475		250		ns
30	TdAS(IEO)	$\overline{AS}$ ↑ to IEO delay		290		250	ns
31	TdIEIf(IEO)	IEI to IEO delay		120		100	ns
32	TsIEI(DSA)	IEI to $\overline{DS}$ ↓ (acknowledge) setup time	150		120		ns
33	TdDS(INT)	$\overline{DS}$ ↓ to $\overline{INT}$ delay		500		500	ns
34	ThIEI(DS)	IEI to $\overline{DS}$ ↑ hold time	100		100		ns

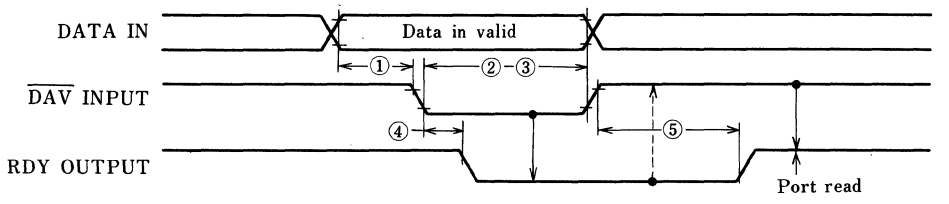


Interrupt acknowledge timing

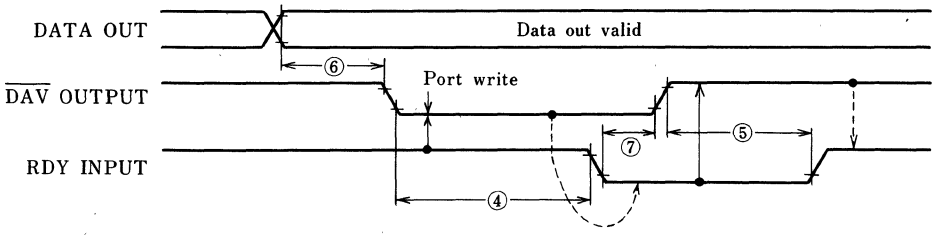
(3) Handshake timing

No.	Symbol	Parameter	LH8090		LH8090A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TsDI(DA)	Data in setup time	0		0		ns	
2	ThDA(DI)	Data in hold time	230		230		ns	
3	TwDA	Data available width	175		175		ns	1,2
4	TdDAL(RY)	Data available low to ready delay time	20	175	20	175	ns	1,2
			0		0		ns	2,3
5	TdDAH(RY)	Data available high to ready delay time		150		150	ns	1,2
			0		0		ns	2,3
6	TdDO(DA)	Data out to data available delay time	50		50		ns	2
7	TdRY(DA)	Ready to data available delay time	0	205	0	205	ns	2

Note 1: Input handshake Note 2: Test load 1 Note 3: Output handshake



Input handshake timing



Output handshake timing

■ Functional Description

(1) Address space

On the 40-pin UPC, all address space is committed to on-chip memory. There are 2048 bytes of mask programmed ROM and 256 bytes of register file. I/O is memory-mapped to three registers in the register file. Only the Protopack version of the UPC can access external program memory. See the section entitled "Special Configurations" for a complete description of the Protopack version.

Program memory: Fig. 1 is a map of the 2K on-chip program ROM. The first 12 bytes of program memory are reserved for the LH8590 interrupt vectors. In the RAM version addresses 0CH through 2FH are reserved for on-chip ROM.

Register file: This 256-byte file includes three I/O port registers (1-3H), 234 general-purpose registers (6H-EFH), and 19 control, Status and special I/O registers (0H,4H,5H and F0-FFH). The functions and mnemonics assigned to these register address locations are shown in Fig. 1. Of the 256 UPC registers, 19 can be directly accessed by the master CPU; the others are accessed indirectly via the block transfer mechanism.

The I/O port and control registers are included in the register file without differentiation. This allows any UPC instruction to process I/O or control information, thereby eliminating the need for special I/O and control instructions. All general-purpose registers can function as accumulators, address pointers, or index registers. In instruction execution, the registers are read when are defined as sources and written when defined as destinations.

UPC instructions may access registers directly or indirectly using an 8-bit address mode or a 4-bit address mode and a Register Pointet. For the 4-bit addressing mode, the file is divided into 16 working register groups, each occupying 16 contiguous locations (Fig. 3). The Register Pointer (RP) addresses the starting point of the active working-register group, and the 4-bit register designator supplied by the instruction specifies the register within the group. Any instruction altering the contents of the register file can also alter the Register Pointer. The UPC instruction set has a special Set Register

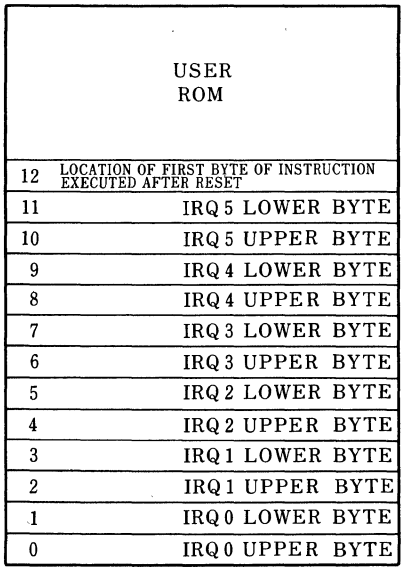


Fig 1 Program memory map

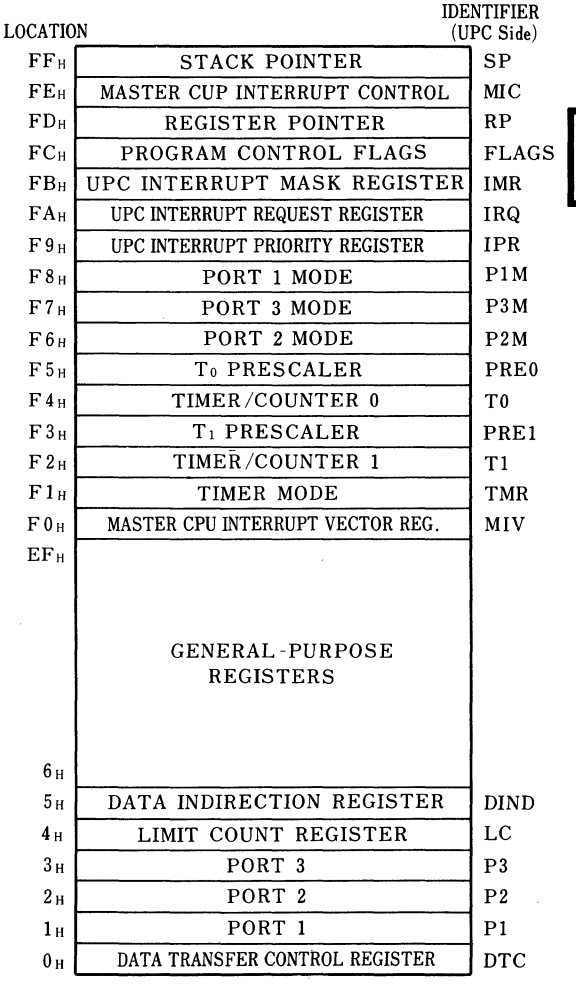
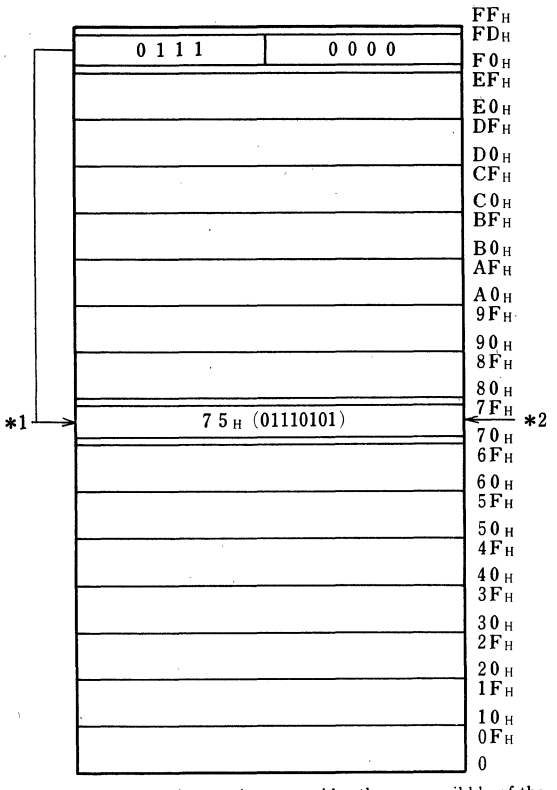


Fig 2 Register file organization



*1 : The 4-bit register pointer provides the upper nibble of the register file address for the 4-bit address mode.
*2 : The lower nibble of the register file address (0101) is provided by the instruction.

Fig. 3 Register pointer mechanism

Pointer (SRP) instruction for initializing or altering the pointer contents.

Stacks : An 8-bit stack Pointer (SP), register R255, is used for addressing the stack, residing within the 234 general-purpose regisgers, address location 6H through EFH.

PUSH and POP instructions can save and restore any register in the register file on the stack. During CALL instructions, the Program Counter is automatically saved on the stack. During UPC interrupt cycles, the Program Counter and the Flag register are automatically saved on the stack. The RET and IRET instructions pop the saved values of the Program Counter and Flag register.

(2) Ports

The LH8090 has 24 lines dedicated to input and output. These are grouped into three ports eight lines each and can be configured under software control as inputs, outputs or special control signals.

They can be programmed to provide Parallel I/O with or without handshake and timing signals.

All outputs can have active pullups and pull-downs, compatible with TTL loads. In addition, Port 1 and Port 2 may be configured as opendrain outputs. Data in each port can be known by reading a corresponding Port Mode register in the same way as accessing the register.

Port 1: Individual bits of port 1 can be configured as input or output. This port can also be programmed as I/O Handshake Line. This port is accessed as general register 1H. It is written by specifying address 1H as the destination of any instruction used to store data in the output registers. The port is read by specifying address 1H as the source of an instruction.

Port 2: Individual bits of Port 2 can be configured as inputs or outputs. This port is accessed as general register 2H, and its functions and methods of programming are the same as those or Port 1.

Port 3: This port can be configured as I/O or control lines. Port 3 is accessed as general register 3H. The directions of the eight data lines are fixed. Four lines, $P3_0$ through $P3_3$, are inputs, and the other four, $P3_4$ through $P3_7$, are outputs. The control functions performed by Port 3 are listed in Table 1.

Table 1 Port 3 control functions

Function	Line	I/O	signal
Handshake	$P3_1$	I	$\overline{DAV_2}/RDY_2$
	$P3_3$	I	$\overline{DAV_1}/RDY_1$
	$P3_4$	O	$RDY_1/\overline{DAV_1}$
	$P3_6$	O	$RDY_2/\overline{DAV_2}$
UPC Interrupt Request*	$P3_0$	I	IRQ_3
	$P3_1$	I	IRQ_2
	$P3_3$	I	IRQ_1
Counter/Timer	$P3_1$	I	T_{IN}
	$P3_6$	O	T_{OUT}
Master CPU	$P3_5$	O	$\overline{INT}$
	$P3_2$	I	$\overline{INTACK}$
	$P3_0$	I	IEI
	$P3_7$	O	IEO

* $P3_0$, $P3_1$, and $P3_3$ can always be used as UPC interrupt request inputs, regardless of the configuration programmed.

(3) Counter/timers

The LH8090 contains two 8-bit programmable counter/timers, each driven by an internal 6-bit programmable prescaler.

The T1 prescaler can be driven by internal or external clock sources. The T0 prescaler is driven by an internal clock source. Both counter/timers operate independently of the processor instruction sequence to relieve the program from time-critical operations like event counting or elapsed-time calculation.

The counters can be started, stopped, restarted to continue, or restarted from the initial value. They can be programmed to stop upon reaching end-of-count (Single-Pass mode) or to automatically reload the initial value and continue counting (Modulo-n Continuous mode).

(4) Interrupts

The LH8090 allows six interrupts from eight different sources as follows:

- Port 3 lines $P3_0$, $P3_1$, and $P3_3$.
- The master CPU (3).
- The two counter/timers.

These interrupts can be masked and globally enabled or disabled. The order of their priority can be specified. All interrupts are vectored.

Table 2 lists the LH8090's interrupt sources, their types, and their vector locations in program ROM.

The LH8090 also supports polled systems.

To acommodate a polled structure, any or all of the interrupt inputs can be masked and the interrupt request register polled to determine which of the interrupt request needs service.

(5) Master CPU register file access

There are two ways in which the master CPU can access the LH8590 register file: direct access and block access.

Direst Access: Three LH8090 registers — the Data transfer Control, the Master Interrupt Vector, and the Master Interrupt Control — are mapped directly into the master CPU address space.

The registers can directly be accessed in 16 bytes.

Block Access: The master CPU may be transmit or receive blocks of data via address ×××10101 (××10101×for shift address). When the master CPU accesses this address, the LH8090 register pointed to by the Data Indirection register (DIND) is read or written.

The number of bytes is set in the Limit Count register (LC). The LH8090 controls everything in the block transfer and is therefore allowed to protect itself from master CPU errors.

Table 2 Interrupt types, sources, and vector locations

Name	Source	Vector Location	Comments
IRQ0	EOM, XERR, LERR	0, 1	Internal (R0 Bits 0, 1, 2)
IRQ1	$\overline{DAV1}$, IRQ1	2, 3	External ($P3_3$) ↓ edge triggerd
IRQ2	$\overline{DAV2}$, IRQ2, T_{IN}	4, 5	External ($P3_1$) ↓ edge triggerd
IRQ3	IRQ3, IEI	6, 7	External ($P3_0$) ↓ edge triggerd
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

■ Instruction

(1) Addressing modes

The following notation is used to describe the addressing modes and instrucion operations.

IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working-register pair address

(2) Symbol

dst	Destination location or contents
src	Source location or contents
cc	Condition code (see list)
@	Indirect address prefix
PC	Program Counter
SP	Stack Pointer (control register FFH)
FLAGS	Flag register (control register FCH)
RP	Register Pointer (control register FDH)
IMR	Interrupt mask register (control register FBH)

Assignment of a value is indicated by the symbol "←". For example,

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr(n)" is used to refer to bit "n" of a given location. For example,

dst (7)

refers to bit 7 of the destination operand.

(3) Flags

Control Register FCH contains the following six flags:

C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Cleared to zero
1	Set to one
*	Set or cleared according to operation
—	Unaffected
×	Undefined

(4) Condition codes

Table 3. shows condition codes.

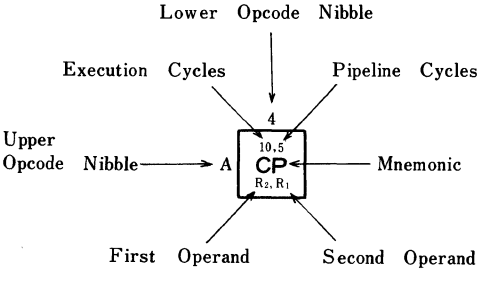
Table 3 Condition codes

Value	Mnemonic	Meaning	Flags set
1000		Always true	.....
0111	C	Carry	C=1
1111	NC	No carry	C=0
0110	Z	Zero	Z=1
1110	NZ	Not zero	Z=0
1101	PL	Plus	S=0
0101	MI	Minus	S=1
0100	OV	Overflow	V=1
1100	NOV	No overflow	V=0
0110	EQ	Equal	Z=1
1110	NE	Not equal	Z=0
1001	GE	Greater than or equal	(S XOR V)=0
0001	LT	Less than	(S XOR V)=1
1010	GT	Greater than	[Z OR(S XOR V)]=0
0010	LE	Less than or equal	[Z OR(S XOR V)]=1
1111	UGE	Unsigned greater than or equal	C=0
0111	ULT	Unsigned less than	C=1
1011	UGT	Unsigned greater than	(C=0 AND Z=0)=1
0011	ULE	Unsigned less than or equal	(C OR Z)=1
0000		Never true	.....

(5) Opcode Map

Lower Nibble (Hex)

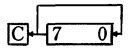
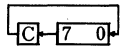
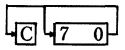
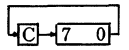
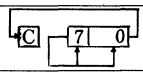
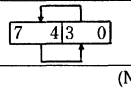
Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6,5 DEC R1	6,5 DEC IR1	6,5 ADD r1, r2	6,5 ADD r1, Ir2	10,5 ADD R2, R1	10,5 ADD IR2, R1	10,5 ADD R1, IM	10,5 ADD IR1, IM	6,5 LD r1, R2	6,5 LD r2, R1	12/10,5 DJNZ r1, RA	12/10,0 JR cc, RA	6,5 LD r1, IM	12/10,0 JP cc, DA	6,5 INC r1	
1	6,5 RLC R1	6,5 RLC IR1	6,5 ADC r1, r2	6,5 ADC r1, Ir2	10,5 ADC R2, R1	10,5 ADC IR2, R1	10,5 ADC R1, IM	10,5 ADC IR1, IM								
2	6,5 INC R1	6,5 INC IR1	6,5 SUB r1, r2	6,5 SUB r1, Ir2	10,5 SUB R2, R1	10,5 SUB IR2, R1	10,5 SUB R1, IM	10,5 SUB IR1, IM								
3	8,0 JP IRR1	6,1 SRP IM	6,5 SBC r1, r2	6,5 SBC r1, Ir2	10,5 SBC R2, R1	10,5 SBC IR2, R1	10,5 SBC R1, IM	10,5 SBC IR1, IM								
4	8,5 DA R1	8,5 DA IR1	6,5 OR r1, r2	6,5 OR r1, Ir2	10,5 OR R2, R1	10,5 OR IR2, R1	10,5 OR R1, IM	10,5 OR IR1, IM								
5	10,5 POP R1	10,5 POP IR1	6,5 AND r1, r2	6,5 AND r1, Ir2	10,5 AND R2, R1	10,5 AND IR2, R1	10,5 AND R1, IM	10,5 AND IR1, IM								
6	6,5 COM R1	6,5 COM IR1	6,5 TCM r1, r2	6,5 TCM r1, Ir2	10,5 TCM R2, R1	10,5 TCM IR2, R1	10,5 TCM R1, IM	10,5 TCM IR1, IM								
7	10/12,1 PUSH R2	12/14,1 PUSH IR2	6,5 TM r1, r2	6,5 TM r1, Ir2	10,5 TM R2, R1	10,5 TM IR2, R1	10,5 TM R1, IM	10,5 TM IR1, IM								
8	10,5 DECW RR1	10,5 DECW IR1	12,0 LDE r1, Irr2	18,0 LDEI Ir1, Irr2												6,1 DI
9	6,5 RL R1	6,5 RL IR 1	12,0 LDE r2, Irr1	18,0 LDEI Ir2, Irr1												6,1 EI
A	10,5 INCW RR1	10,5 INCW IR1	6,5 CP r1, r2	6,5 CP r1, Ir2	10,5 CP R2, R1	10,5 CP IR2, R1	10,5 CP R1, IM	10,5 CP IR1, IM								14,0 RET
B	6,5 CLR R1	6,5 CLR IR1	6,5 XOR r1, r2	6,5 XOR r1, Ir2	10,5 XOR R2, R1	10,5 XOR IR2, R1	10,5 XOR R1, IM	10,5 XOR IR1, IM								16,0 IRET
C	6,5 RRC R1	6,5 RRC IR1	12,0 LDC r1, Irr2	18,0 LDCI Ir1, Irr2				10,5 LD r1, x, R2								6,5 RCF
D	6,5 SRA R1	6,5 SRA IR1	12,0 LDC r2, Irr1	18,0 LDCI Ir2, Irr1	20,0 CALL* IRR1		20,0 CALL DA	10,5 LD r2, x, R1								6,5 SCF
E	6,5 RR R1	6,5 RR IR1		6,5 LD r1, Ir2	10,5 LD R2, R1	10,5 LD IR2, R1	10,5 LD R1, IM	10,5 LD IR1, IM								6,5 CCF
F	8,5 SWAP R1	8,5 SWAP IR1		6,5 LD Ir1, r2		10,5 LD R2, IR1										6,0 NOP
Bytes per Instruction	2				3				2					3	1	



Legend:
R = 8-Bit Address
r = 4-Bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address
Sequence:
Opcode, First Operand, Second Operand
Note: The blank areas are not defined.

Instruction Summary

Instruction and Operation	Addr. mode dst	Addr. mode src	Opcode (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst+src+C		(Note 1)	1□	* * * * 0 *
ADD dst, src dst←dst+src		(Note 1)	0□	* * * * 0 *
AND dst, src dst←dst AND src		(Note 1)	5□	− * * 0 − −
CALL dst SP←SP−2 @SP←PC; PC←dst	DA IRR		D6 D4	− − − − − −
CCF C←NOT C			EF	* − − − − −
CLR dst dst←0	R IR		B0 B1	− − − − − −
COM dst dst←NOT dst	R IR		60 61	− * * 0 − −
CP dst, src dst←src		(Note 1)	A□	* * * * − −
DA dst dst←DA dst	R IR		40 41	* * * X − −
DEC dst dst←dst−1	R IR		00 01	− * * * − −
DECW dst dst←dst−1	RR IR		80 81	− * * * − −
DI IMR(7)←0			8F	− − − − − −
DJNZ r,dst r←r−1 if r≠0 PC←PC+dst Range: +127∼−128	RA		rA r=0−F	− − − − − −
EI IMR(7)←1			9F	− − − − − −
INC dst dst←dst+1	r R IR		rE r=0−F 20 21	− * * * − −
INCW dst dst←dst+1	RR IR		A0 A1	− * * * − −
IRET FLAGS←@SP;SP←SP+1 PC←@SP;SP←SP+2;IMR(7)←1			BF	* * * * * *
JP cc, dst if cc is true PC←dst	DA IRR		cD c=0−F 30	− − − − − −
JR cc, dst if cc is true, PC←PC+dst Range: +127∼−128	RA		cB c=0−F	− − − − − −
LD dst, src dst←src	r r R r X r Ir R R R R IR IR	IM R r X r Ir r R IR IM IM R	rC r8 r9 r=0−F C7 D7 E3 F3 E4 E5 E6 E7 F5	− − − − − −
LDC dst, src dst←src	r Irr	Irr r	C2 D2	− − − − − −
LDCI dst, src dst←src r←r+1; rr←rr+1	Ir Irr	Irr r	C3 D3	− − − − − −
LDE dst, src dst←src	r Irr	Irr r	82 92	− − − − − −

Instruction and Operation	Addr. mode dst	Addr. mode src	Opcode (Hex)	Flags Affected C Z S V D H
LDEI dst, src dst←src r←r+1; rr←rr+1	Ir Irr	Irr Ir	83 93	− − − − − −
NOP			FF	− − − − − −
OR dst, src dst←dst OR src		(Note 1)	4□	− * * 0 − −
POP dst dst←@SP SP←SP+1	R IR		50 51	− − − − − −
PUSH src SP←SP−1; @SP←src		R IR	70 71	− − − − − −
RCF C←0			CF	0 − − − − −
PET PC←@SP; SP←SP+2			AF	− − − − − −
4RL dst		R IR	90 91	* * * * − −
RLC dst		R IR	10 11	* * * * − −
RR dst		R IR	E0 E1	* * * * − −
RRC dst		R IR	C0 C1	* * * * − −
SBC dst, src dst←dst−src−C		(Note 1)	3□	* * * * 1 *
SCF C←1			DF	1 − − − − −
SRA dst			D0 D1	* * * 0 − −
SRP src RP←src		IM	31	− − − − − −
SUB dst, src dst←dst−src		(Note 1)	2□	* * * * 1 *
SWAP dst		R IR	F0 F1	X * * X − −
TCM dst,src (NOT dst) AND src		(Note 1)	6□	− * * 0 − −
TM dst,src dst AND src		(Note 1)	7□	− * * 0 − −
XOR dst,src dst←dst XOR src		(Note 1)	B□	− * * 0 − −

Note 1: These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a □ in this table, and its value is found in the following table to the left of the applicable addressing mode paie.

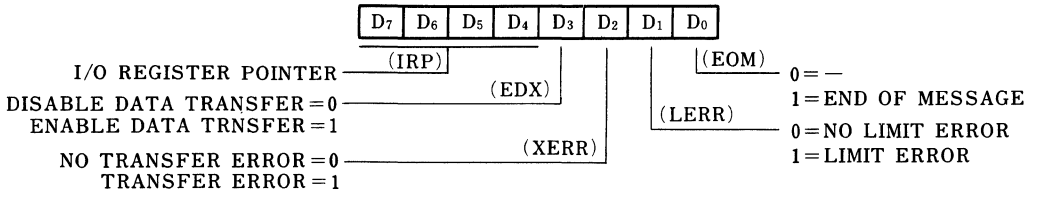
For example, to determine the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Addr Mode dst	Addr Mode src	Lower Opcode Nibble
r	r	2
r	Ir	3
R	R	4
R	IR	5
R	IM	6
IR	IM	7

■ Register

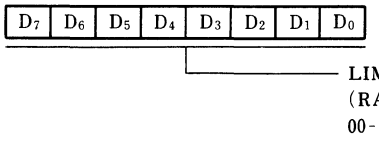
R0 (DTC)

UPC Register Address (Hex): 00



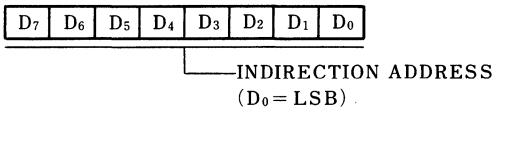
R4 (LC)

UPC Register Address (Hex): 04



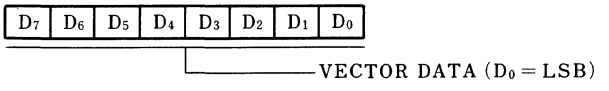
R5 (DIND)

UPC Register Address (Hex): 05



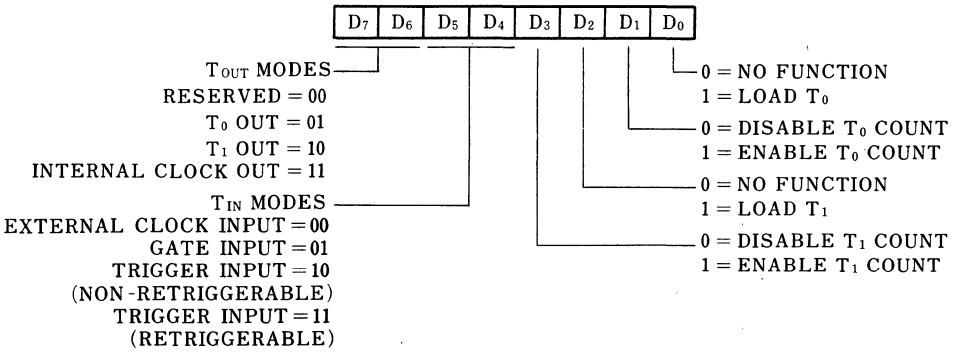
R240 (MIV)

UPC Register Address (Hex): F1



R241 (TMR)

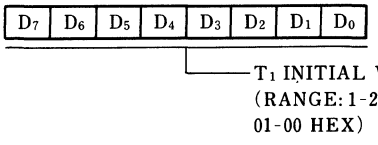
UPC register address (Hex): F1



R242 (T1)

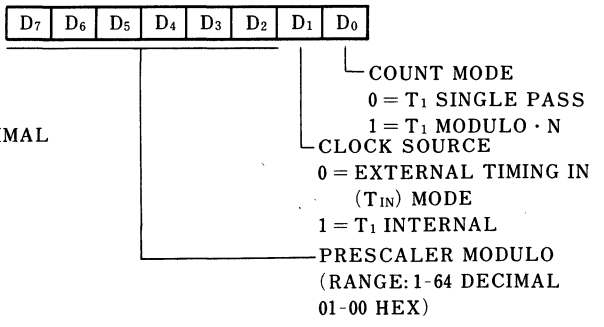
Counter/Timer 1 Register

UPC Register Address (Hex): F2

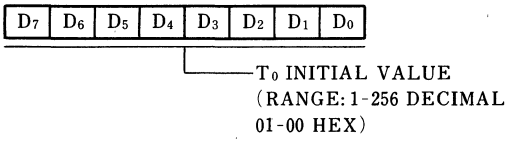


R243 (PRE1)

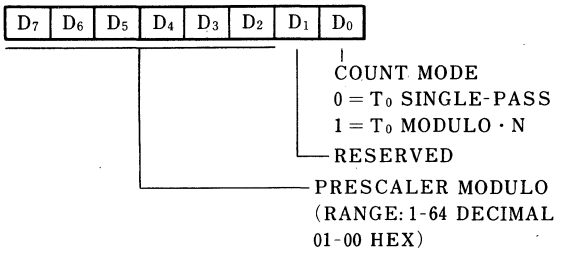
UPC Register Address (Hex): F3



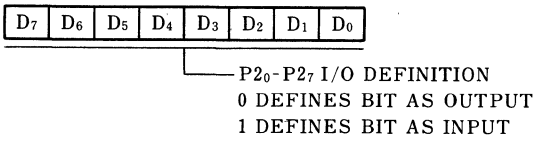
R244 (T0)
Counter/Timer 0 Register
UPC Register Address (Hex): F4



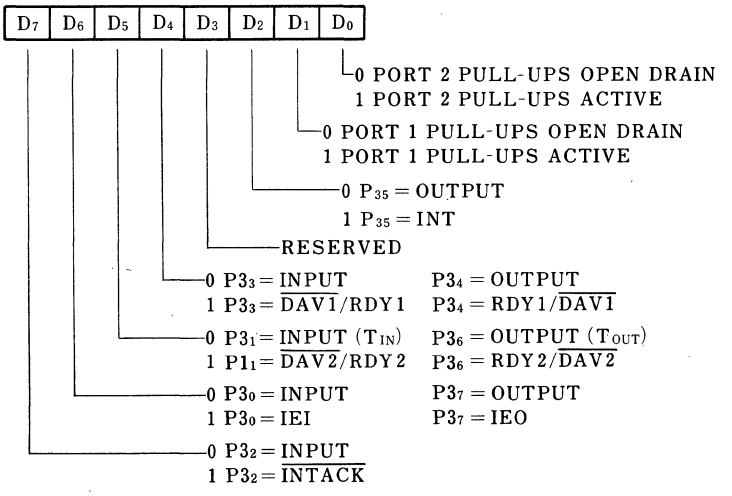
R245 (PRE0)
Prescaler 0 Register
UPC Register Address (Hex): F5



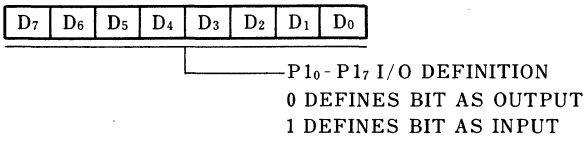
R246 (P2M)
Port 2 Mode Register
UPC Register Address (Hex): F6



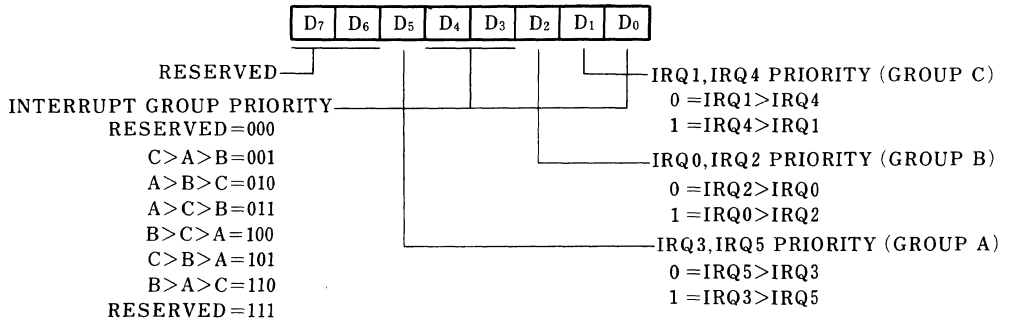
R247 (P3M)
Port 3 Mode Register
UPC Register Address (Hex): F7



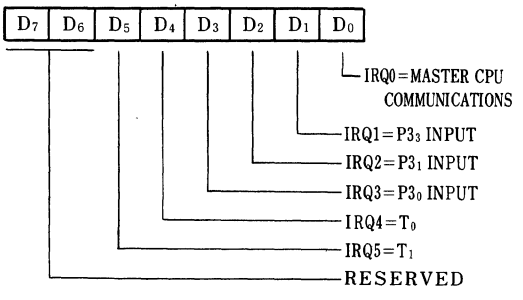
R248 (P1M)
Port 1 Mode Register
UPC Register Address (Hex): F5



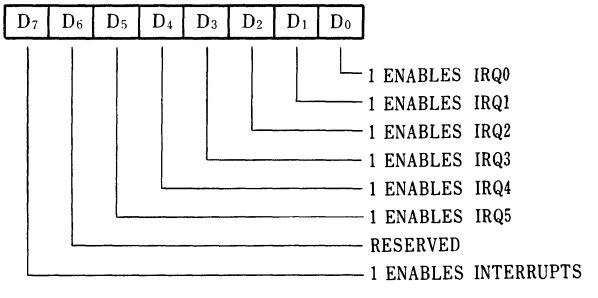
R249 (IPR)
Interrupt Priority Register
UPC Register Address (Hex): F9 (write only)



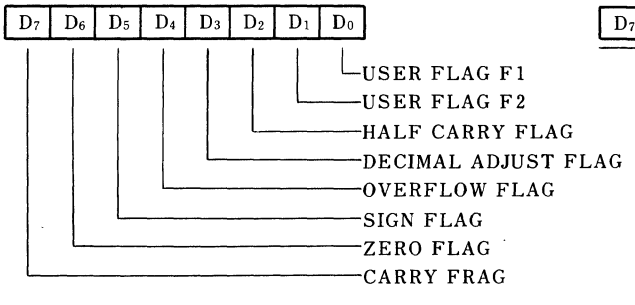
R250 (IRQ)
Interrupt Request Register
UPC Register Address (Hex): FA



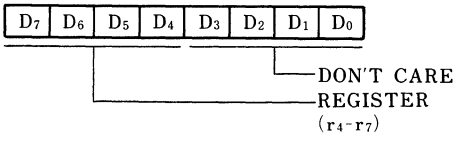
R251 (IMR)
Interrupt Mask Register
UPC Register Address (Hex): FB



R252 (FLAGS)
Flag Register
UPC Register Address (Hex): FC



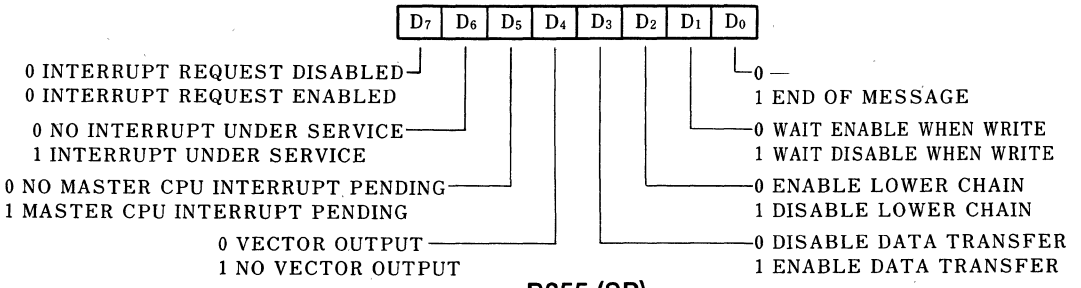
R253 (RP)
Register Pointer
UPC Register Address (Hex): FD



R254 (MIC)

Master CPU Interrupt Control Register

UPC Register Address (Hex): FE



R255 (SP)

Stack Pointer

UPC Register Address (Hex): FF

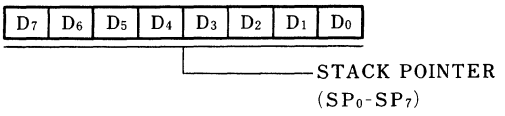


Table 4. Control register reset conditions

Control Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Comments
00_H Data transfer control register	X	X	X	X	0	0	0	0	Disable data transfer from master CPU
04_H Limit count register	Not defined								
05_H Data indirection register	Not defined								
$F0_H$ Interrupt vector register	Not defined								
$F1_H$ Timer mode	0	0	0	0	0	0	0	0	Stops T0 and T1
$F2_H$ T1 register	Not defined								
$F3_H$ T1 prescaler	X	X	X	X	X	X	0	0	Single-pass mode
$F4_H$ T0 register	Not defined								
$F5_H$ T0 prescaler	X	X	X	X	X	X	0	0	Single-pass mode external clock source
$F6_H$ Port 2 mode	1	1	1	1	1	1	1	1	Port 2 lines defined as inputs
$F7_H$ port 3 mode	0	0	0	0	X	1	0	0	Port 1, 2 open drain output $P3_5 = \overline{INT}$ $P3_0$, $P3_1$, $P3_2$, $P3_3$ defined as input $P3_4$, $P3_6$, $P3_7$ defined as output
$F8_H$ port 1 mode	1	1	1	1	1	1	1	1	Port 1 lines defined as inputs
$F9_H$ Interrupt priority	Not defined								
FA_H Interrupt request	X	X	0	0	0	0	0	0	Reset interrupt request
EB_H Interrupt mask	0	X	X	X	X	X	X	X	Interrupts disabled
FC_H Flag register	Not defined								
FD_H Register pointer	Not defined								
FE_H Master CPU interrupt control register	0	0	0	0	0	0	0	0	Master CPU interrupt disabled: wait enable when write: lower chain enabled
FF_H Stack pointer	Not defined								

Note: X means not defined.

LH8091/LH8091A Z8091/Z8091A Development Device

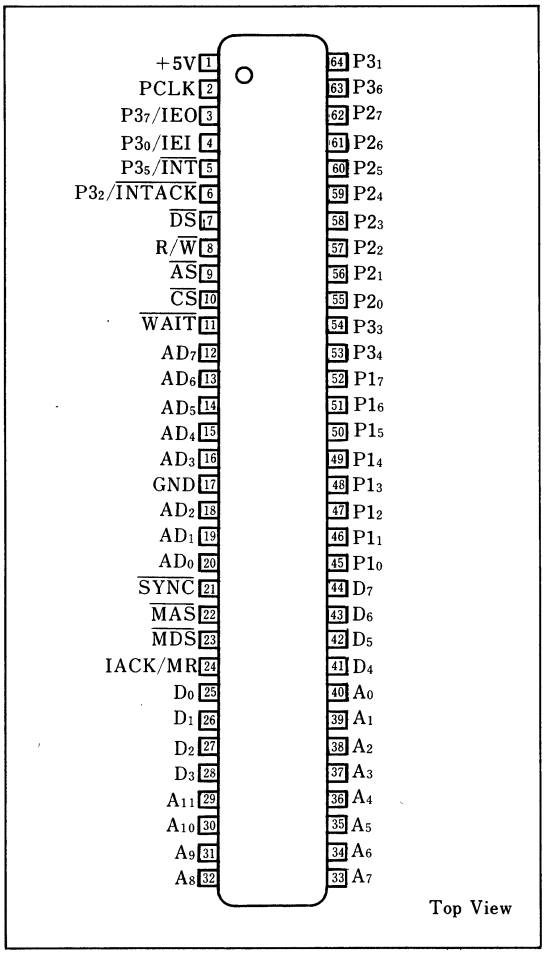
■ Description

The 64-pin LH8091 is the development version of LH8090 (Z8090) UPC with internal mask-programmed ROM. This device allows the user to the prototype systems in hardware without an actual device and to develop the code that is eventually mask-programmed into the on-chip ROM of the LH8090.

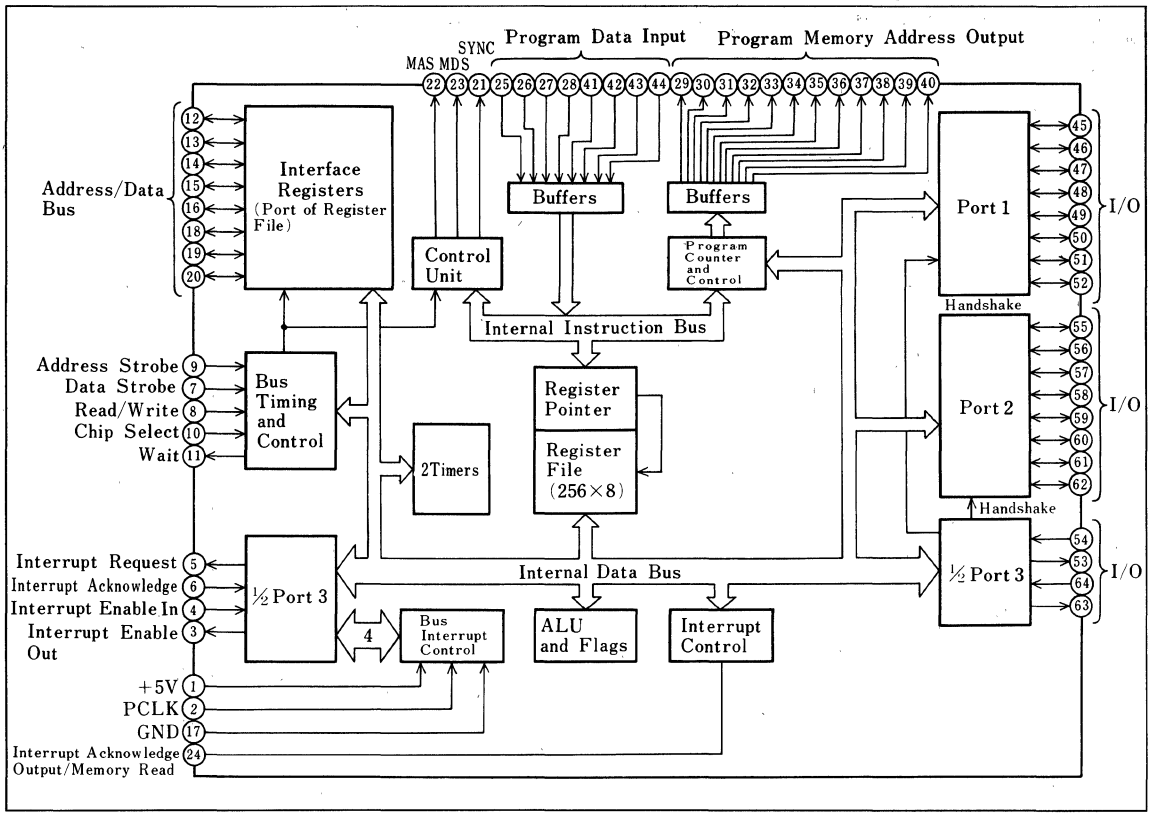
The LH8091 is identical to the LH8090 with the following exceptions.

- The internal ROM has been removed.
- The ROM address lines and data lines are buffered and brought out to external pins.
- Control lines for the memory have been added. The LH8091A is the high speed version which can operate at 6MHz system clock.

■ Pin Connections



■ Block Diagram



■ Pin Description

LH8091 has the same functions as those of a 40-pin device LH8090, and the functions of the additional 24 pins are as follows.

Symbol	Meaning	I/O	Function
A_0~A_{11}	Program memory address	O	Used for the access to the external memory of 4K bytes.
D_0~D_7	Program data	I	Reads the data through these lines from the external memory.
IACK/MR	Interrupt acknowledge /memory read	O	Active high. This signal becomes high during interrupt or instruction fetch cycle of LH8591.
$\overline{MAS}$	Memory address strobe	O	Active low. This signal is output every memory fetch cycle for the interface with the external ROM.
$\overline{MDS}$	Memory data strobe	O	Active low. This signal becomes low during instruction fetch cycle or write cycle.
$\overline{SYNC}$	Synchronization	O	Active low. This signal becomes low at the clock cycle just before Op-code fetching.

LH8092/LH8092A Z8092/Z8092A Development Device

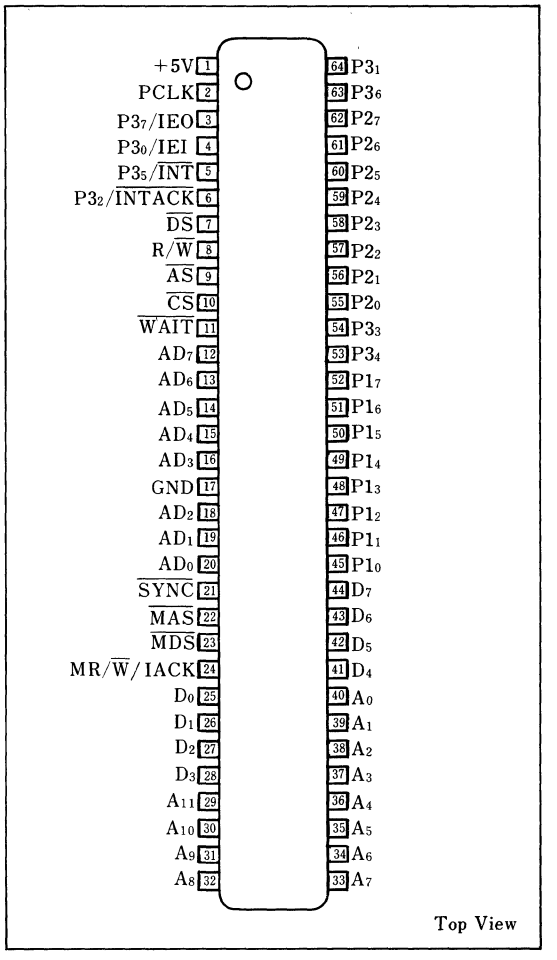
Description

The 64-pin LH8092 is the development version of LH8090 (Z8090 UPC) with internal mask-programmed ROM. This device allows the user to the prototype systems in hardware with an actual device and to develop the code that is eventually mask-programmed into the on-chip ROM of the LH8090.

The LH8092 is identical to the LH8090 with the following exceptions.

- The internal ROM has been removed (But there are 36 bytes of internal ROM for a bootstrap program).
- The ROM address lines and data lines are buffered and brought out to external pins.
- Control lines for the memory have been added. The LH8092A is the high speed version which can operate at 6MHz system clock.

Pin Connections



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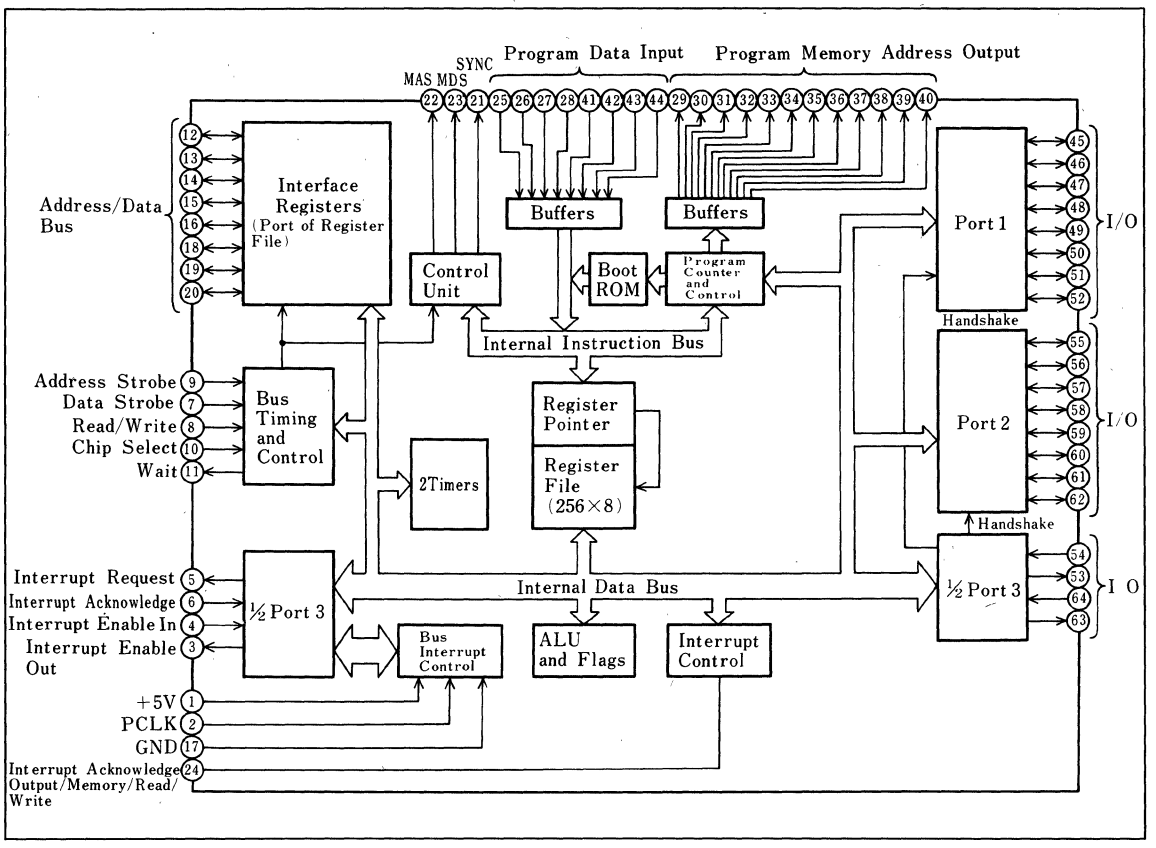
■ Block Diagran



■ Pin Description

LH8092 has the same functions as those of a 40-pin device LH8090, and the functions of additional 24 pins are as follows.

Symbol	Meaning	I/O	Function
A_0~A_{11}	Program memory address	O	Used for the access to the external memory of 4K bytes.
D_0~D_7	Program data	I	Reads for data through these lines from the external memory. And it is possible to write into an external RAM through these lines.
LACK	Interrupt acknowledge	O	Active high. This signal is always active during interrupt cycle of LH8092.
$\overline{MAS}$	Memory address strobe	O	Active low. This signal is output every memory fetch cyclefor interfacing with the external RAM.
$\overline{MDS}$	Memory data strobe	O	Active low. This signal is outptt eyery memory fetch cycle for cycle or write cycle.
MR/$\overline{W}$	Memory read/write	O	This signal is high during instruction fetching by LH8092, or low while writing into the external memory.
$\overline{SYNC}$	Synchronization	O	Active low. This signal becomes low during clock cycle just before OP code fetching.

LH8093/LH8093A Z8093/Z8093A Protopack Emulator

■ Description

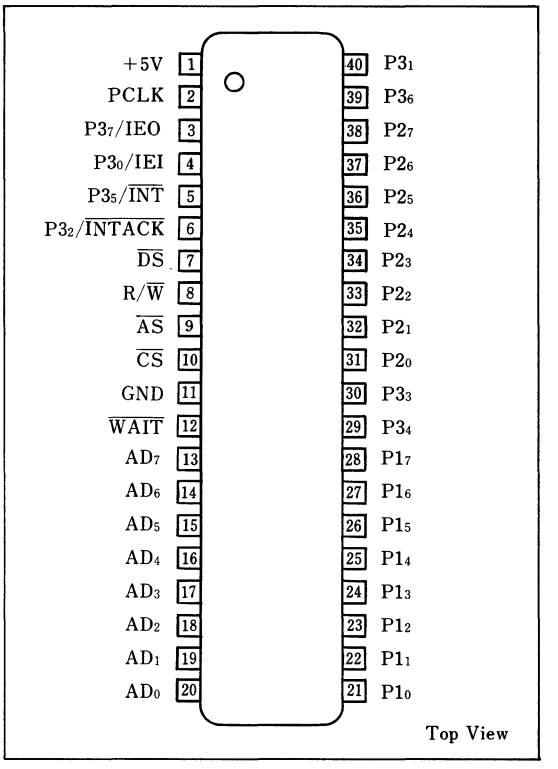
The LH8093 (Z8093) is a ROMless version of the standard LH8090, housed in a pin compatible 40-pin package.

The LH8093 carries a 40-pin soket for a direct interface to program memory. 2716 type EPROM can be used for program memory.

The LH8093 allows the user to build the prototype and pilot production units. When the final program is established, the user can then switch over the LH8090.

The LH8093A is the high speed version which can operate at 6MHz system clock.

■ Pin Connections



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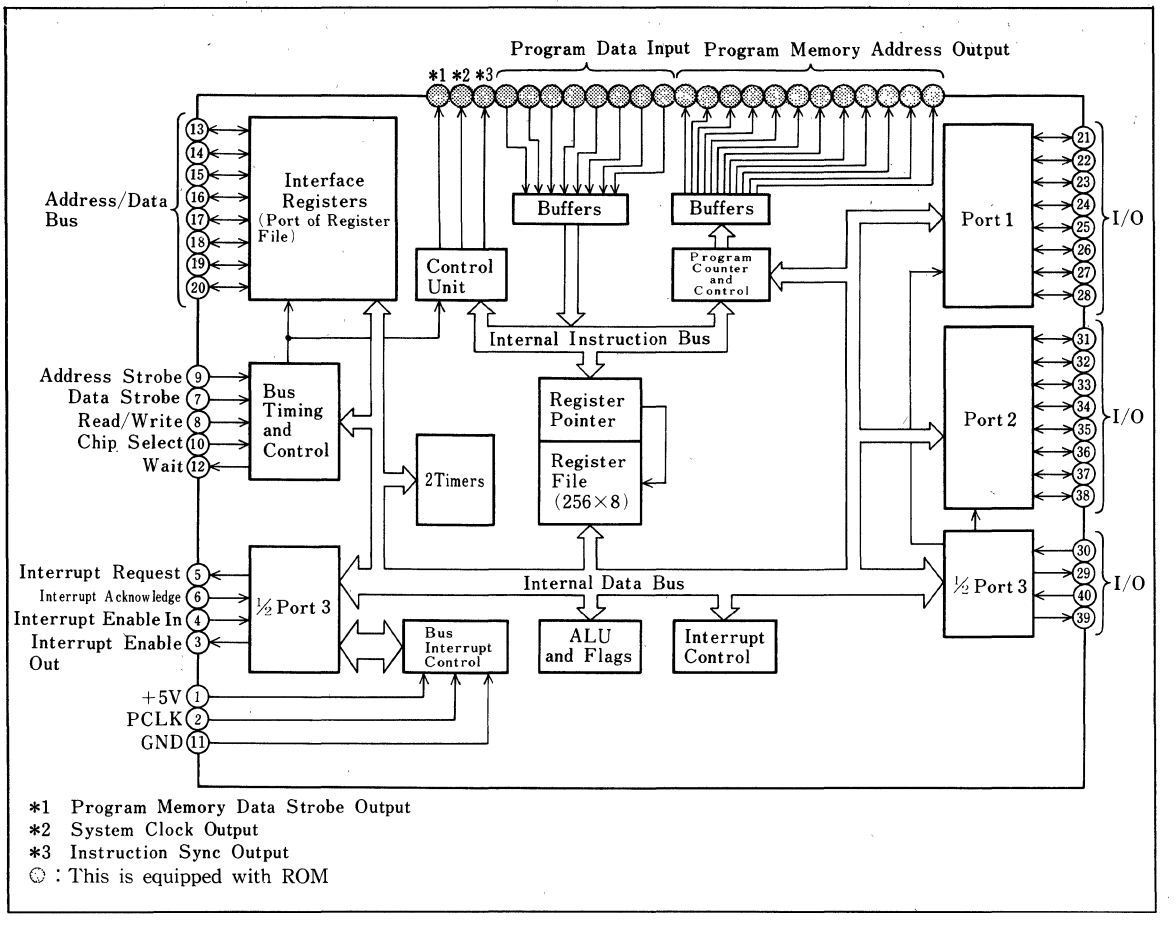
■ Block Diagram



*1 Program Memory Data Strobe Output
*2 System Clock Output
*3 Instruction Sync Output
◎ : This is equipped with ROM

■ Pin Description

LH8093 pins are compatible with those of LH8090. For pin descriptions of LH8093, refer to those of LH8090.

LH8094/LH8094A Z8094/Z8094A Protopack Emulator

■ Description

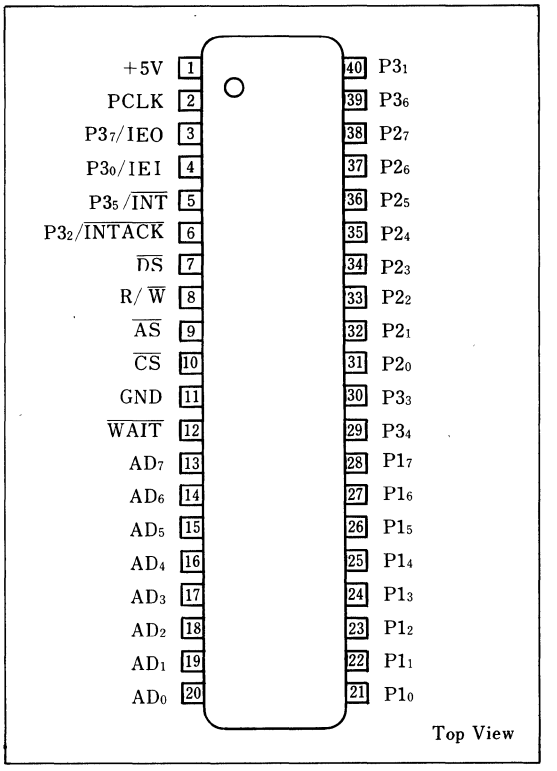
The LH8094 (Z8094) is a RAM version (16K bits RAM) of the standard LH8090, housed in a pin compatible 40-pin package.

The LH8094 carries a 24-pin soket for a direct interface to program memory, and has 36 bytes of internal ROM for a bootstrap program.

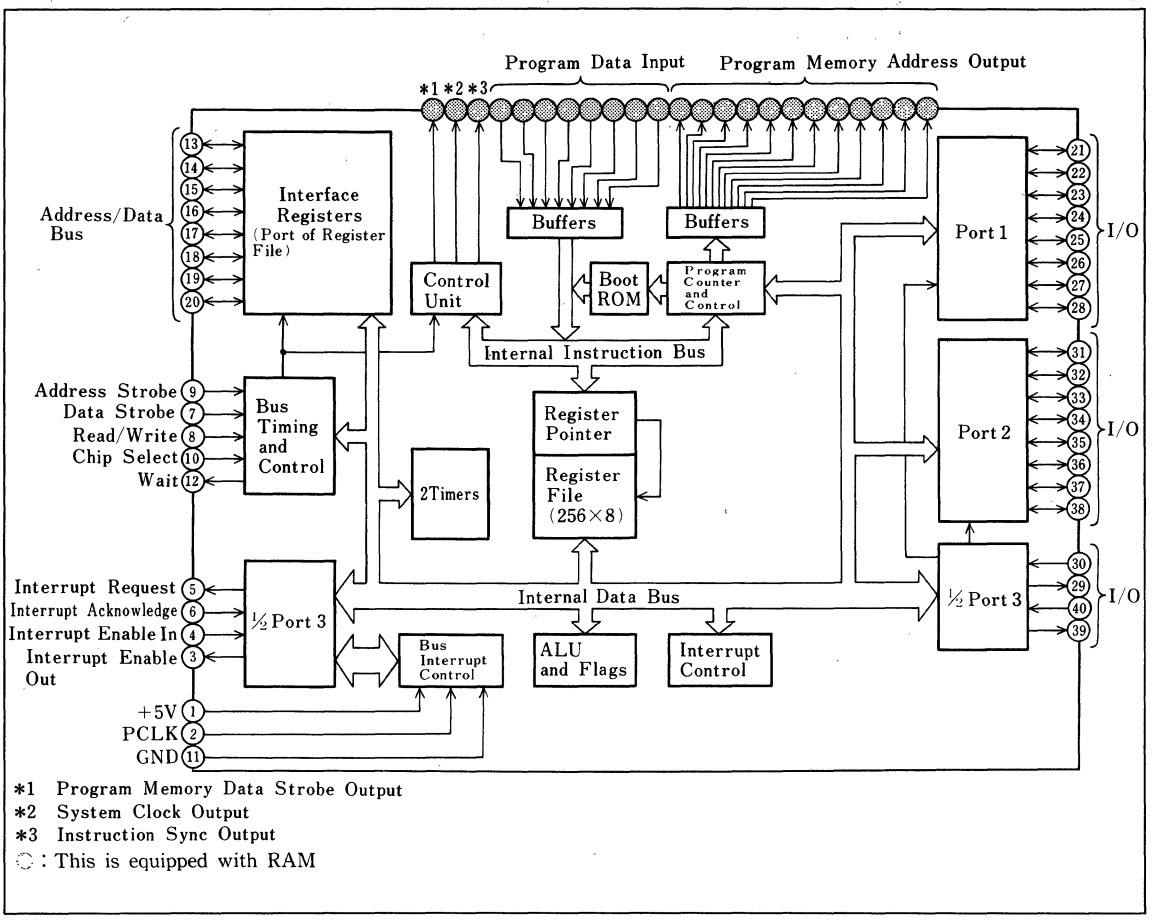
The LH8094 allows the user to build the prototype and when the final program is established, the user can then switch over the LH8090.

The LH8094A is the high speed version which can operate at 6MHz system clock.

■ Pin Connections



■ Block Diagram



■ Pin Description

LH8094 pins are compatible with those of LH8090. For pin descriptions of LH8094, refer to those of LH8090.

Peripheral LSIs for Microcomputers

LH8530/LH8530A

Z8530/Z8530A Serial Communications Controller

■ Description

The LH8530 Z8530 SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with conventional non-multiplexed buses. The LH8530 functions as a serial-to-parallel, parallel-to-serial converter controller. The LH8530 can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, Digital Phase-Locked Loops, and crystal oscillators that dramatically reduce the need for external logic.

The LH8530 handles asynchronous formats, Synchronous byte-oriented protocols such as IBM Bisync, and Synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial date transfer application (cassette, disk tape drives, etc).

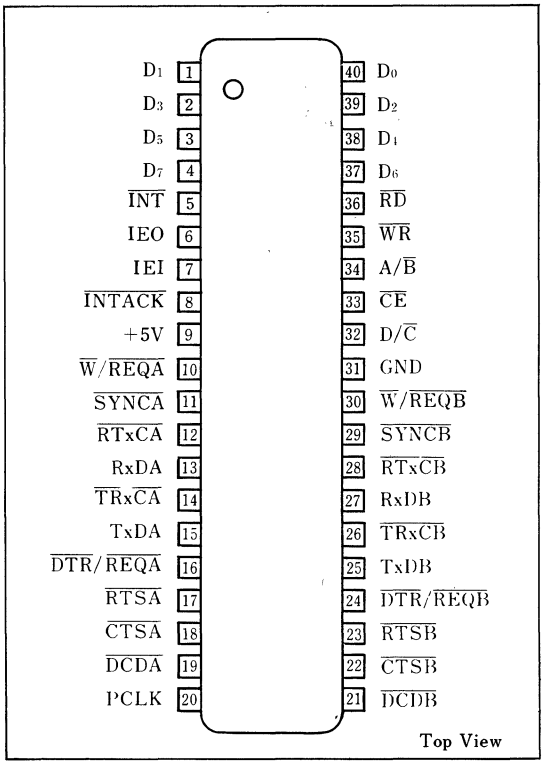
The device can generate and check CRC codes in any Synchronous mode and can be programmed to check data integrity in various modes. The LH8530 also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The daisy-chain interrupt hierarchy is also supported by the LH8530.

The LH8530 is packaged in a 40-pin ceramic DIP and uses a single+5V power supply.

The LH8530A Z8530A SCC is the high speed version which can operate at 6MHz system clock.

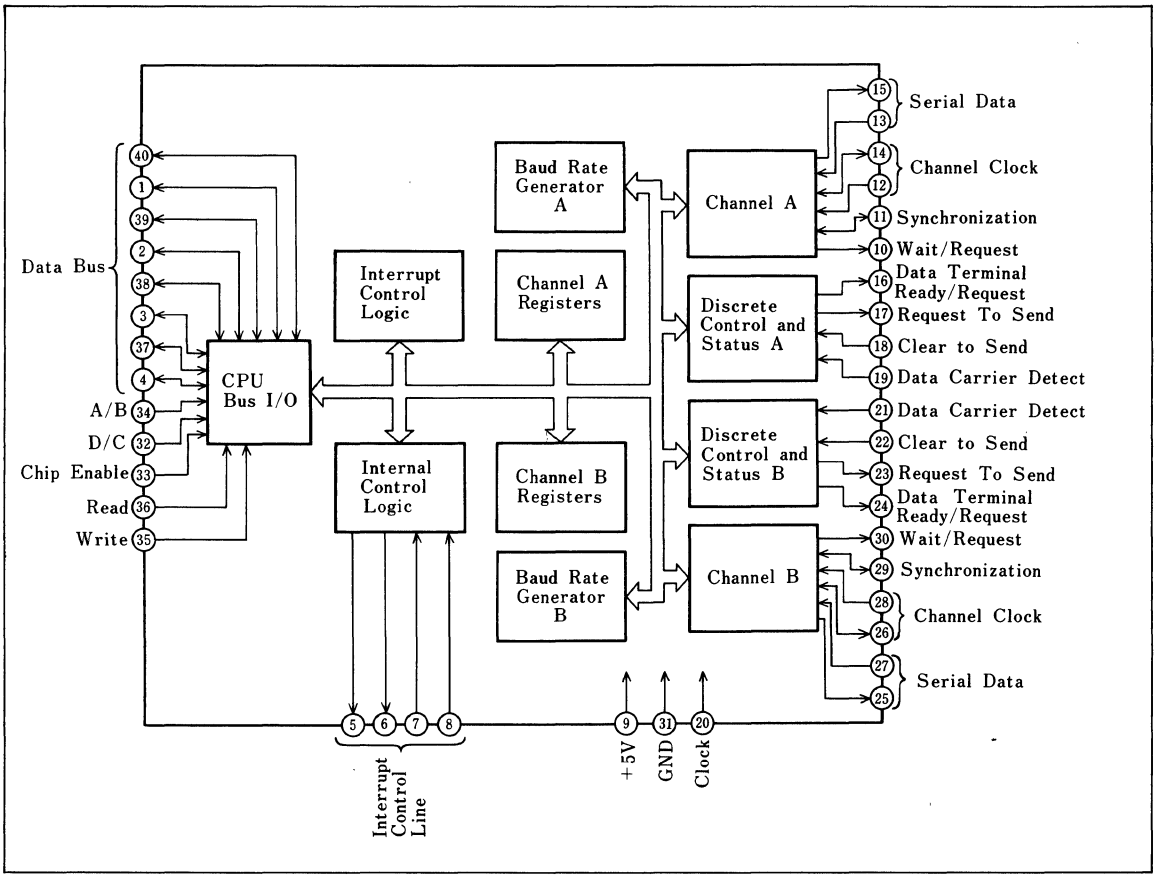
■ Pin Connections



■ Features

1. Two independent, 0 to 1.5M bit/second, full-duplex channels, each with a separate crystal oscillator, baud rate generator, and Digital Phase-Locked Loop for clock recovery.
2. Multi-protocol operation under program control; programmable for NRZ, NRZI, or FM data encoding.
3. Asychronous mode with five to eight bits and one, one and one-half, or two stop bits per character; programmable clock factor, break detection and generation; parity, overrun, and framing error detection.
4. Synchronous mode with internal or external character synchronization on one or two synchronous characters and CRC generation and checking with CRC-16 or CRC-CCITT preset to either 1s or 0s.
5. SDLC/HDLC mode with comprehensive frame-level control, automatic zero insertion and deletion. I-field residue handling, abort generation and detection, CRC generation and checking, and SDLC Loop mode operation.
6. Local Loopback and Auto Echo modes.

■ Block Diagram

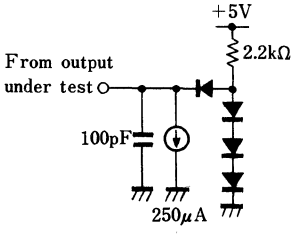


Pin Description

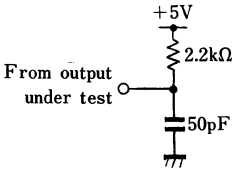
Pin	Meaning	I/O	Function
A/$\overline{B}$	Channel A/ Channel B select	I	Channel select signal.
$\overline{CE}$	Chip enable	I	Active low. Enables the CPU to transmit and receive command and data when low.
$\overline{CTSA}$ $\overline{CTSB}$	Clear to send	I	Active low. Enables the respective transmitters.
D/$\overline{C}$	Data/control select	I	This signal defines the type of information on the data bus. High means data ; Low indicates a command.
$\overline{DCDA}$ $\overline{DCDB}$	Data carrier detect	I	Active low. Enables the respective receivers.
D_0~D_7	Data bus	Bidirectional 3-state	System data bus.
$\overline{DTR}$/$\overline{REQA}$ $\overline{DTR}$/$\overline{REQB}$	Data terminal ready/request	O	Active low. These outputs follow the state programmed into the DTR bit.
IEI	Interrupt enable input	I	Active high. IEI is used to form a daisy chain that determines the interrupt priority order.
IEO	Interrupt enable output	O	Active high. IEO is used to form a daisy chain that determines the interrupt priority order.
$\overline{INT}$	Interrupt request	Open-drain	Active low, open-drain. Indicates an interrupt request to the CPU.
$\overline{INTACK}$	Interrupt acknowledge	I	Active low. This signal indicates an active interrupt acknowledge cycle.
$\overline{RD}$	Read	I	Active low. This signal indicates a read operation.
R×DA R×DB	Receive data	I	Active high. These are receive data lines.
$\overline{RT}$×$\overline{CA}$ $\overline{RT}$×$\overline{CB}$	Receive/transmit clocks	I	Active low. These are communication clock lines.
$\overline{RTSA}$ $\overline{RTSB}$	Request to send	O	Active low. Goes high after the transmitter is empty.
$\overline{SYNCA}$ $\overline{SYNCB}$	Synchronization	I/O	Active low. Indicates that a synchronization pattern has been recognized.
T×DA T×DB	Transmit data	O	Active high. These are transmit data lines.
$\overline{TR}$×$\overline{CA}$ $\overline{TR}$×$\overline{CB}$	Transmit/receive clocks	I/O	These are communication clocks.
$\overline{WR}$	Write	I	Active low. This signal indicates a write operation.
$\overline{W}$/$\overline{REQA}$ $\overline{W}$/$\overline{REQB}$	Wait/request	Open-drain	Active low. Operate as request lines when the DMA is the bus master or as wait lines when the CPU is the bus master.
PCLK	Clock	I	Single-phase clock. It does not have to be the CPU clock.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3~+7	V
Output voltage	V_{OUT}	−0.3~+7	V
Operating temperature	T_{opr}	0~+70	℃
Storage temperature	T_{stg}	−65~+150	℃



Standard test load



Open-drain test load

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input high voltage	V_{IH}		2	V_{CC}+0.3	V
Input low voltage	V_{IL}		−0.3	0.8	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4		V
Output low voltage	V_{OL}	I_{OL}=+2mA		0.4	V
Input leakage current	$\lvert I_{IL} \rvert$	0.4 ≦ V_{IN} ≦ 2.4V		10	μA
Output leakage current	$\lvert I_{OL} \rvert$	0.4 ≦ V_{OUT} ≦ 2.4V		10	μA
Current consumption	I_{CC}			250	mA

■ Capacitance

(f=1MHz. Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_{IN}	Unmeasured Pins Returned to Ground		10	pF
Output capacitance	C_{OUT}			15	pF
Bidirectional capacitance	$C_{I/O}$			20	pF

■ AC Characteristics

(1) CPU interface timing, interrupt timing, and interrupt acknowledge timing

No.	Symbol	Parameter	LH8530		LH8530A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TwPCl	PCLK low width	105	2000	70	1000	ns	
2	TwPCh	PCLK high width	105	2000	70	1000	ns	
3	TfPC	PCLK fall time		20		10	ns	
4	TrPC	PCLK rise time		20		15	ns	
5	TcPC	PCLK cycle time	250	4000	165	2000	ns	
6	TsA(WR)	Address to $\overline{WR}$ ↓ setup time	80		80		ns	
7	ThA(WR)	Address to $\overline{WR}$ ↑ hold time	0		0		ns	
8	TsA(RD)	Address to $\overline{RD}$ ↓ setup time	80		80		ns	
9	ThA(RD)	Address to $\overline{RD}$ ↑ hold time	0		0		ns	
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ setup time	0		0		ns	
11	TsIAi(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ setup time	200		200		ns	1
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ hold time	0		0		ns	
13	TsIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ setup time	200		200		ns	1
14	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ hold time	0		0		ns	
15	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ hold time	100		100		ns	
16	TsCEl(WR)	$\overline{CE}$ low to $\overline{WR}$ ↓ setup time	0		0		ns	
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ hold time	0		0		ns	
18	TsCEh(WR)	$\overline{CE}$ high to $\overline{WR}$ ↓ setup time	100		70		ns	
19	TsCEl(RD)	$\overline{CE}$ low to $\overline{RD}$ ↓ setup time	0		0		ns	1
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ hold time	0		0		ns	1
21	TsCEh(RD)	$\overline{CE}$ high to $\overline{RD}$ ↓ setup time	100		70		ns	1
22	TwRDl	$\overline{RD}$ low width	390		250		ns	1
23	TdRD(DRA)	$\overline{RD}$ ↓ to read data active delay	0		0		ns	
24	TdRDr(DR)	$\overline{RD}$ ↑ to read data not valid delay	0		0		ns	
25	TdRDf(DR)	$\overline{RD}$ ↓ to read data valid delay		250		180	ns	
26	TdRD(DRz)	$\overline{RD}$ ↑ to read data float delay		70		45	ns	2
27	TdA(DR)	Address required valid to read data valid delay		590		420	ns	
28	TwWRl	$\overline{WR}$ low width	390		250		ns	
29	TsDW(WR)	Write data to $\overline{WR}$ ↓ setup time	0		0		ns	

No.	Symbol	Parameter	LH8530		LH8530A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
30	ThDW(WR)	Write data to $\overline{WR}$ ↑ hold time	0		0		ns	
31	TdWR(W)	$\overline{WR}$ ↓ to wait valid delay		240		200	ns	4
32	TdRD(W)	$\overline{RD}$ ↓ to wait valid delay		240		200	ns	4
33	TdWRf(REQ)	$\overline{WR}$ ↓ to $\overline{W/REQ}$ not valid delay		240		200	ns	
34	TdRDf(REQ)	$\overline{RD}$ ↓ to $\overline{W/REQ}$ not valid delay		240		200	ns	
35	TdWRr(REQ)	$\overline{WR}$ ↑ to $\overline{DTR/REQ}$ not valid delay		5TcPC+300		5TcPC+250	ns	
36	TdRDr(REQ)	$\overline{RD}$ ↑ to $\overline{DTR/REQ}$ not valid delay		5TcPC+300		5TcPC+250	ns	
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ valid delay		500		500	ns	4
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (acknowledge) delay					ns	5
39	TwRDA	$\overline{RD}$ (acknowledge) width	285		250		ns	
40	TdRDA(DR)	$\overline{RD}$ ↓ (acknowledge) to read data valid delay		190		180	ns	
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (acknowledge) setup time	120		100		ns	
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (acknowledge) hold time	0		0		ns	
43	TdIEI(IEO)	IEI to IEO delay time		120		100	ns	
44	TdPC(IEO)	PCLK ↑ to IEO delay		250		250	ns	
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ inactive delay		500		500	ns	4
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ delay for no reset	30		15		ns	
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ delay for no reset	30		30		ns	
48	TwRES	$\overline{WR}$ and $\overline{RD}$ coincident low for reset	250		250		ns	
49	Trc	Valid access recovery time	6TcPC+200		6TcPC+130		ns	3

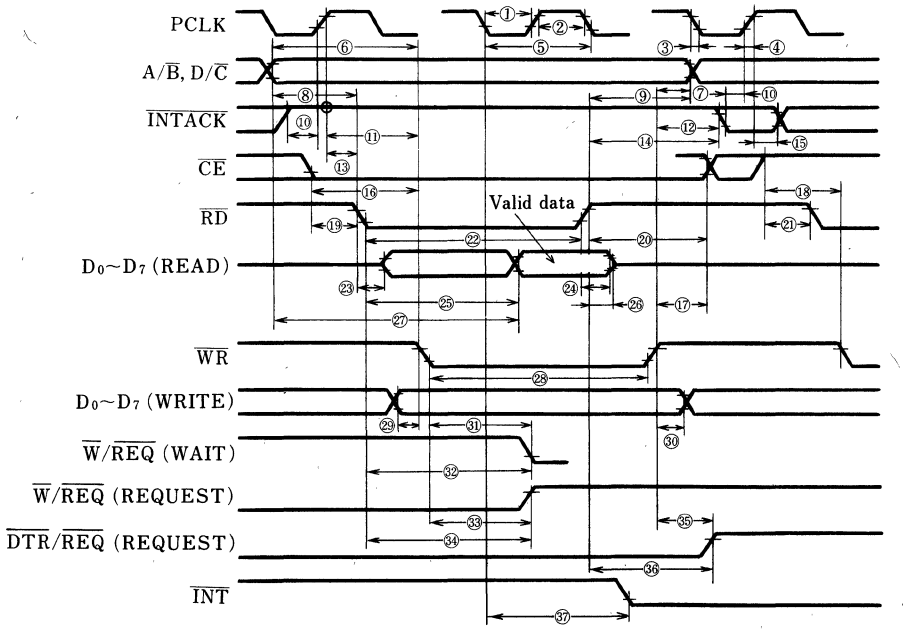
Note 1: Parameter does not apply to Interrupt Acknowledge transactions.

Note 2: Float delay is defined as the time required for a ±0.5V change in the output with a maximum DC load and minimum AC load.

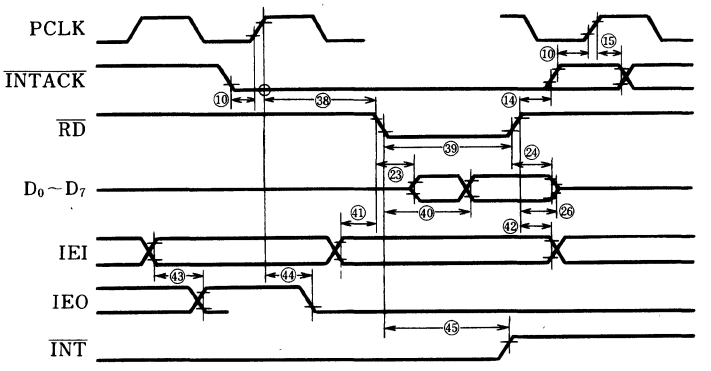
Note 3: Parameter applies only between transactions involving the SCC.

Note 4: Open-drain output, measured with open-drain test load.

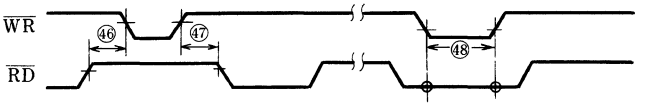
Note 5: Parameter is system dependent. For any SCC in the daisy chain, TdIAi (RD) must be greater than the sum of TdPC (IEO) for the highest priority device in the daisy chain, TsIEI (RDA) for the SCC, and TdIEIf (IEO) for each device separating them in the daisy chain.



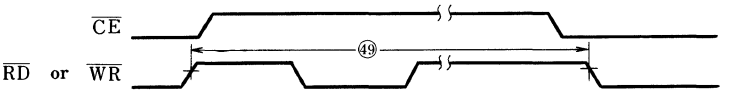
Read and write timing



Interrupt acknowledge timing



Reset timing

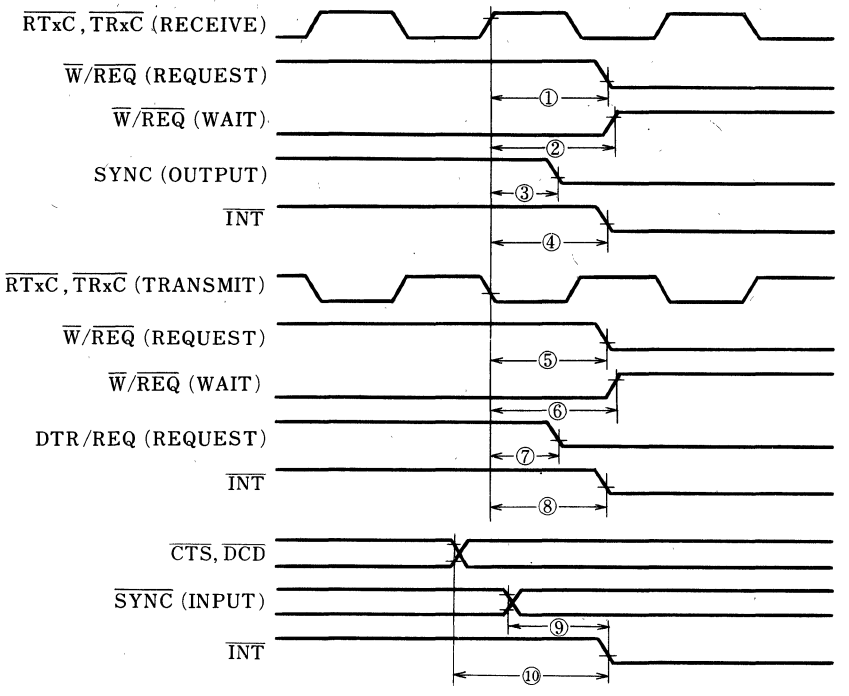


Cycle timing

(2) System timing

No.	Symbol	Parameter	LH8530		LH8530A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TdRxC(REQ)	$\overline{RxC}$ ↑ to $\overline{W}/\overline{REQ}$ valid delay	8	12	8	12	TcPC	2
2	TdRxC(W)	$\overline{RxC}$ ↑ to wait inactive delay	8	12	8	12	TcPC	1,2
3	TdRxC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ valid delay	4	7	4	7	TcPC	2
4	TdRxC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ valid delay	10	16	10	16	TcPC	1,2
5	TdTxC(REQ)	$\overline{TxC}$ ↓ to $\overline{W}/\overline{REQ}$ valid delay	5	8	5	8	TcPC	3
6	TdTxC(W)	$\overline{TxC}$ ↓ to wait inactive delay	5	8	5	8	TcPC	1,3
7	TdTxC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR}/\overline{REQ}$ valid delay	4	7	4	7	TcPC	3
8	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ valid delay	6	10	6	10	TcPC	1,3
9	TdSx(INT)	$\overline{SYNC}$ transition to $\overline{INT}$ valid delay	2	6	2	6	TcPC	1
10	TdExT(INT)	$\overline{DCD}$ or $\overline{CTS}$ transition to $\overline{INT}$ valid delay	2	6	2	6	TcPC	1

Note 1: Open-drain output, measured with open-drain test load.
Note 2: $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
Note 3: $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.



System timing

(3) General timing

No.	Symbol	Parameter	LH8530		LH8530A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TdPC(REQ)	PCLK ↓ to W/REQ valid delay		250		250	ns	
2	TdPC(W)	PCLK ↓ to wait inactive delay		350		350	ns	
3	TsRXC(PC)	RxC ↑ to PCLK ↑ setup time (PCLK ÷ 4 case only)	80		70		ns	1,4
4	TsRXD(RXCr)	RxD to RxC ↑ setup time (X1 mode)	0		0		ns	1
5	ThRXD(RXCr)	RxD to RxC ↑ hold time (X1 mode)	150		150		ns	1
6	TsRXD(RXCf)	RxD to RxC ↓ setup time (X1 mode)	0		0		ns	1,5
7	ThRXD(RXCf)	RxD to RxC ↓ hold time (X1 mode)	150		150		ns	1,5
8	TsSY(RXC)	SYNC to RxC ↑ setup time	−200		−200		ns	1
9	ThSY(RXC)	SYNC to RxC ↑ hold time	3TcPC+200		3TcPC+200		ns	1
10	TsTXC(PC)	TxC ↓ to PCLK ↑ setup time	0		0		ns	2,4
11	TdTXCf(TXD)	TxC ↓ to TxD delay (X1 mode)		300		300	ns	2
12	TdTXCr(TXD)	TxC ↑ to TxD delay (X1 mode)		300		300	ns	2,5
13	TdTXD(TRX)	TxD to TRxC delay (send clock echo)		200		200	ns	
14	TwRTXh	RTxC high width	180		180		ns	6
15	TwRTXl	RTxC low width	180		180		ns	6
16	TcRTX	RTxC cycle time	400		400		ns	6
17	TcRTXX	Crystal oscillator period	250	1000	250	1000	ns	3
18	TwTRXh	TRxC high width	180		180		ns	3
19	TwTRXl	TRxC low width	180		180		ns	6
20	TcTRX	TRxC cycle time	400		400		ns	6
21	TwEXT	DCD or CTS pulse width	200		200		ns	
22	TwSY	SYNC pulse width	200		200		ns	

Note 1: $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.

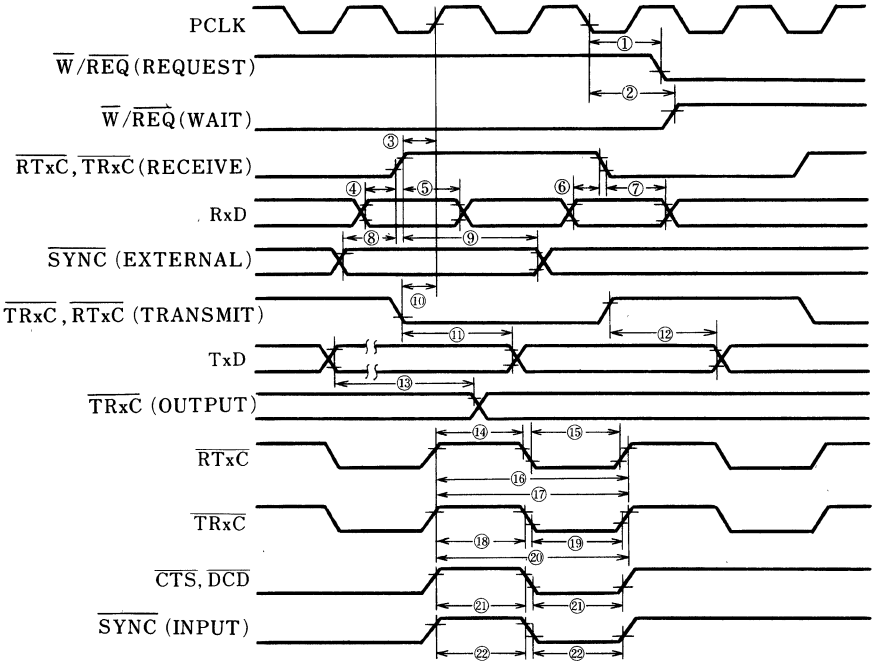
Note 2: $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

Note 3: Both $\overline{RTxC}$ and $\overline{SYNC}$ have 30 pF capacitors to ground connected to them.

Note 4: Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or $\overline{TxC}$ and PCLK is required.

Note 5: Parameter applies only to FM encoding/decoding.

Note 6: Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.



General timing

■ Data Communications Capabilities

The LH8530 provides two independent fullduplex channels programmable for use in any common Asynchronous or Synchronous data communication protocol. Fig. 1 illustrates these protocols.

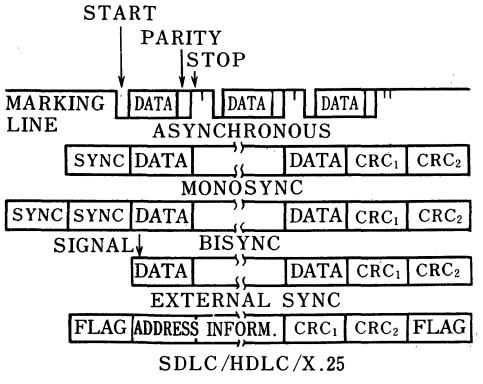


Fig. 1 Some SCC protocols

■ SDLC Loop Mode

The LH8530 supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow on the loop and any number of secondary stations. In SDLC Loop mode, the LH8530 performs the functions of a secondary station while an LH8530 operating in regular SDLC mode can act as a controller (Fig. 2).

A secondary station in an SDLC Loop is alway listening to the messages being sent around the loop, and in fact must pass these messages to the rest of the loop by retransmitting them with a one-bit-time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an EOP (End Of Poll), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary 1 of the EOP to a 0 before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit can then append their messages to the message of the first secondary station by the same process. Any secondary stations without messages to send merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP).

SDLC Loop mode is a programmable option in the LH8530. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

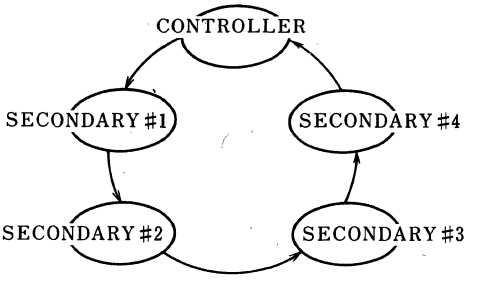


Fig. 2 An SDLC loop

■ Data Encoding

The LH8530 may be programmed to encode and decode the serial data in four different ways (Fig. 3). In NRZ encoding, a 1 is represented by a High level and a 0 is represented by a Low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level. In FM1 (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FM0 (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the LH8530 can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0, the bit is a 1.

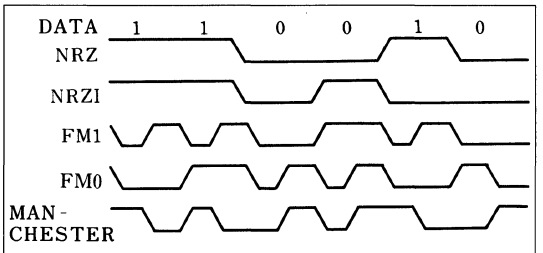


Fig. 3 Data encoding methods

■ Auto Echo and Local Loopback

The LH8530 is capable of automatically echoing everything it receives. This feature is useful mainly in Asynchronous modes, but works in Synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the $\overline{\text{CTS}}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and $\overline{\text{WAIT/REQUEST}}$ on transmit.

The LH8530 is also capable of local loopback. In this mode TxD is RxD, just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in Asynchronous, Synchronous and SDLC modes with NRZ, NRZI or FM coding of the data stream.

■ Baud Rate Generator

Each channel in the LH8530 contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching 0, the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time , but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the Digital Phase-Locked Loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{\text{TRxC}}$ pin, the output of the baud rate generator may be echoed out via the $\overline{\text{TRxC}}$ pin.

The following formula relates the time constant to the baud rate (the baud rate is in bits/second and the BR clock period is in seconds).

$$\text{baud rate} = \frac{1}{2(\text{time constant} + 2) \times (\text{BR clock period})}$$

■ Digital phase-Locked Loop

The LH8530 contains a Digital Phase-Locked Loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the SCC receive clock, the transmit clock, or both.

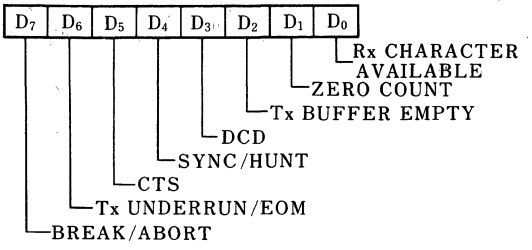
For NRZI encoding, the DPLL counts the 32X clock 60 create nominal bit times. As the 32X clock is counted, the DPLL is searching the incoming data stream for edges (either 1 to 0 or 0 to 1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15 to 16 counting transition.

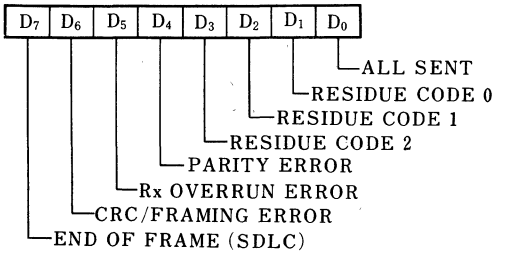
The 32X clock for the DPLL can be programmed to come from either the $\overline{\text{RTxC}}$ input or the output of the baud rate generator. The DPLL output may be programmed to be enchoed out of the LH8530 via the $\overline{\text{TRxC}}$ pin (if this pin is not being used as an input).

■ Read Registers

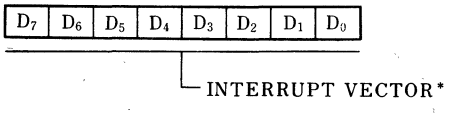
• Read Register 0



• Read Register 1

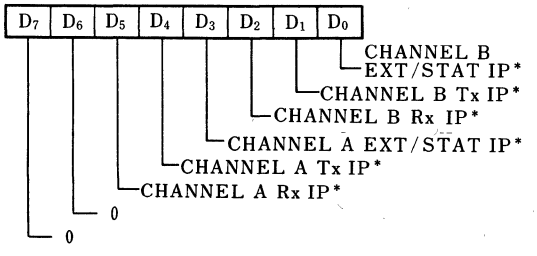


• Read Register 2



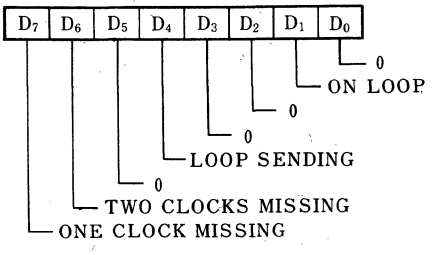
*MODIFIED IN CHANNEL B

• Read Register 3*

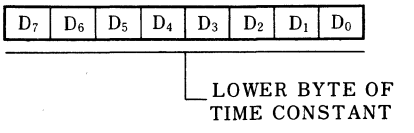


*ALWAYS 0 IN CHANNEL B

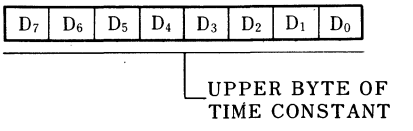
• Read Register 10



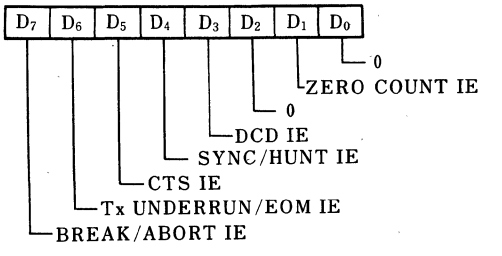
• Read Register 12



• Read Register 13

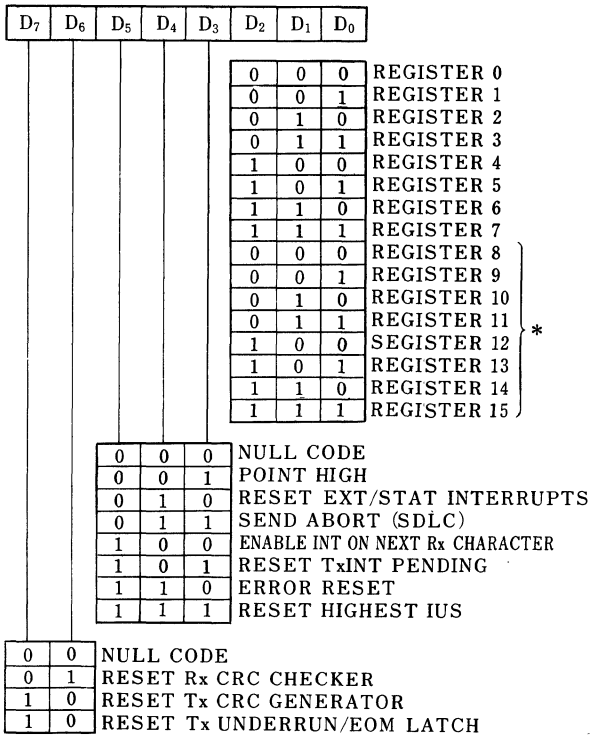


• Read Register 15



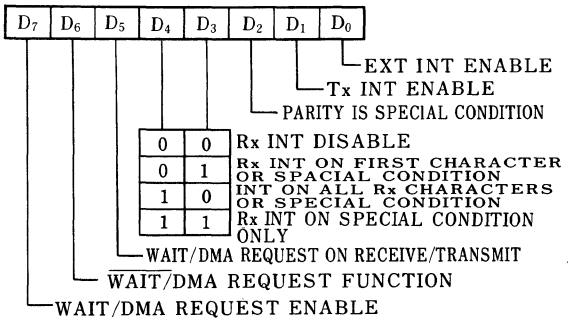
■ Write Registers

• Write Register 0

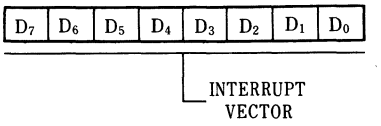


*WITH POINT HIGH COMMAND ($D_5D_4D_3$=001)

• Write Register 1



• Write Register 2



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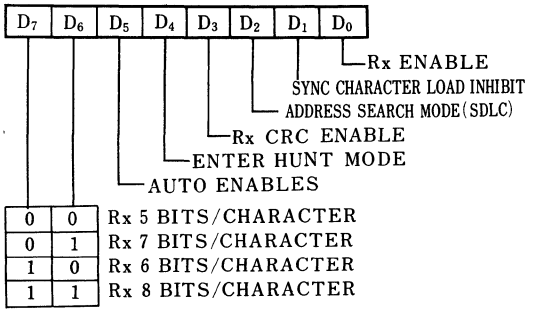

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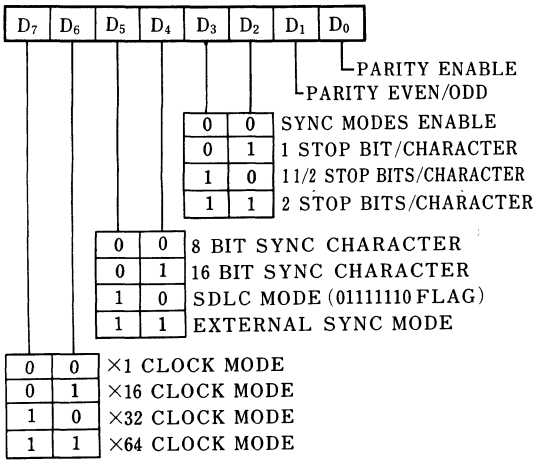
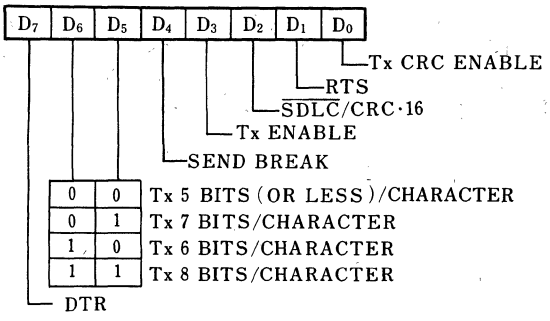


6

- **Write Register 5**



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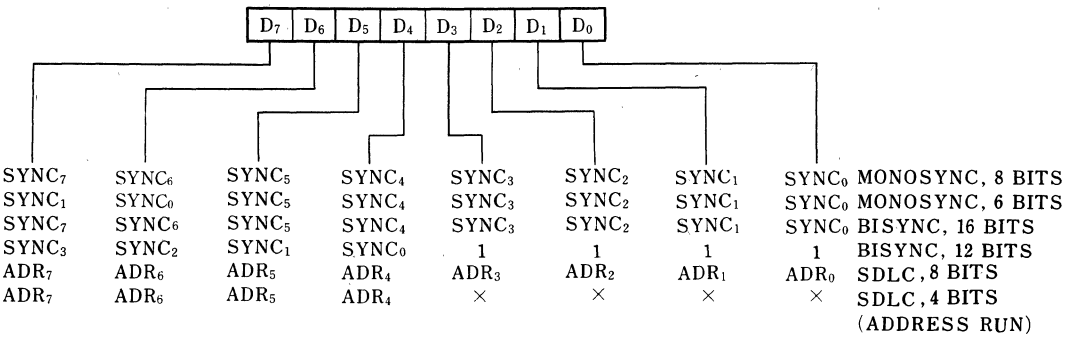

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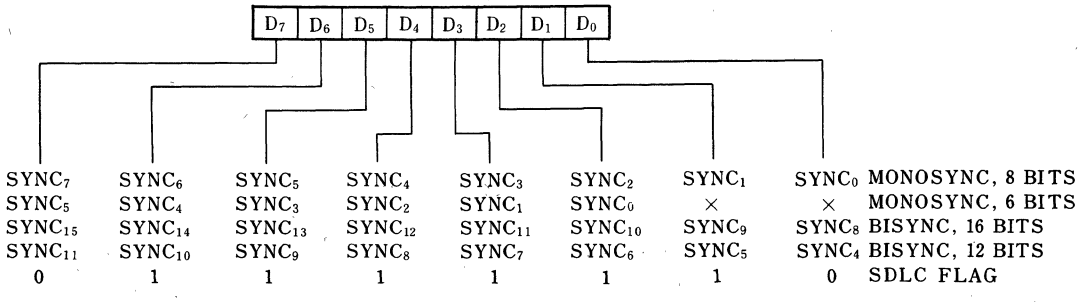

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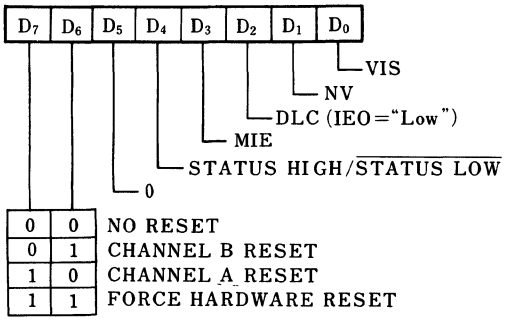

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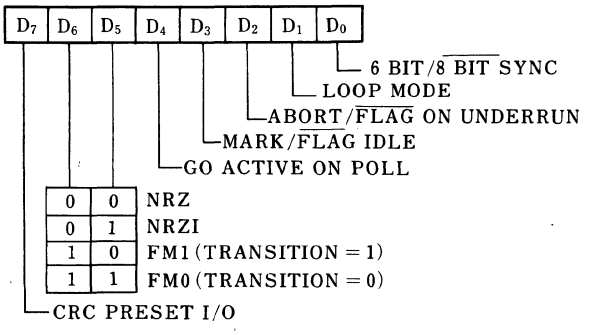

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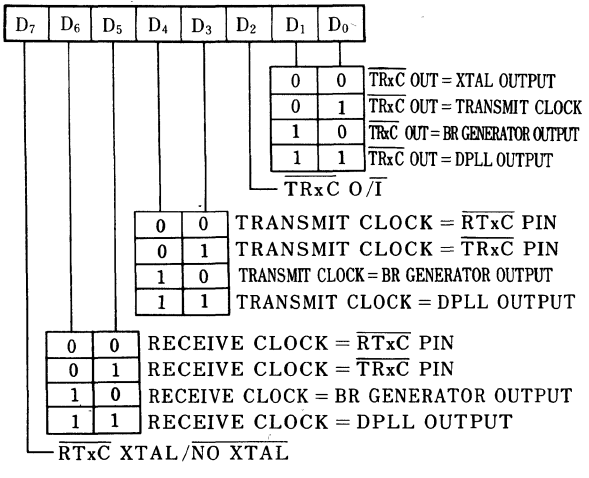
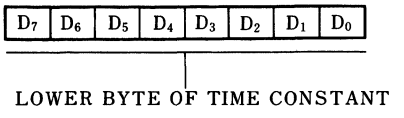
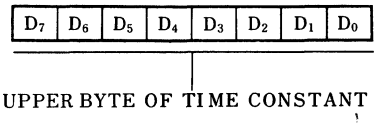


- **Write Register 12**



- **Write Register 13**



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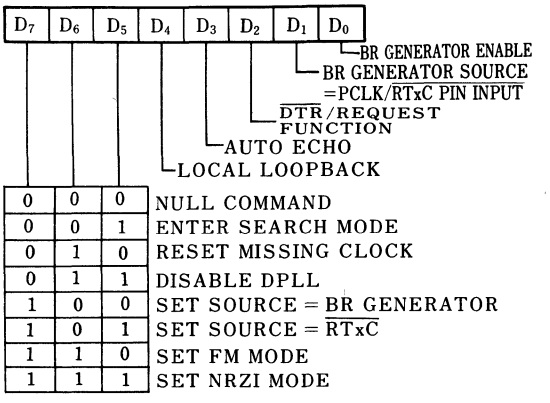

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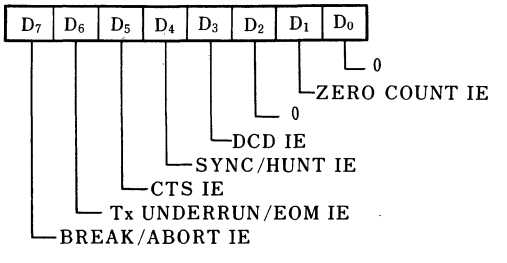


6

LH8536/LH8536A

Z8536/Z8536A Counter/Timer and Parallel I/O Unit

■ Description

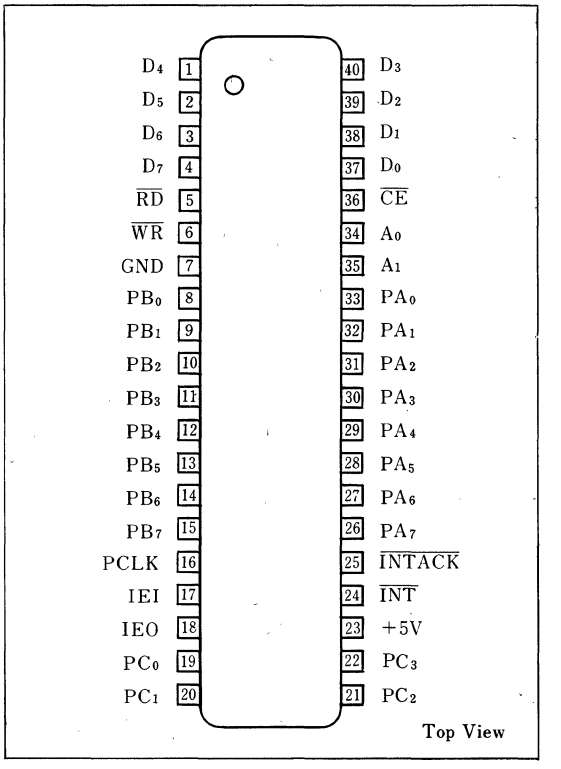
The LH8536 Z8536 CIO Counter/Timer and Parallel I/O element is a general-purpose peripheral circuit, satisfying most counter/timer and parallel I/O needs encountered in system designs. This versatile device contains three I/O ports and three counter/timers. Many programmable options tailor its configuration to specific applications. The use of the device is simplified by making all internal registers (command, status, and data) readable and (except for status bits) writable. In addition, each register is given its own unique internal address, so that any register can be accessed in two operations. All data registers can be directly accessed in a single operation. The LH8536 is easily interfaced to all popular microprocessors.

The LH8536A Z8536A CIO is the high speed version which can operate at 6 MHz system clock.

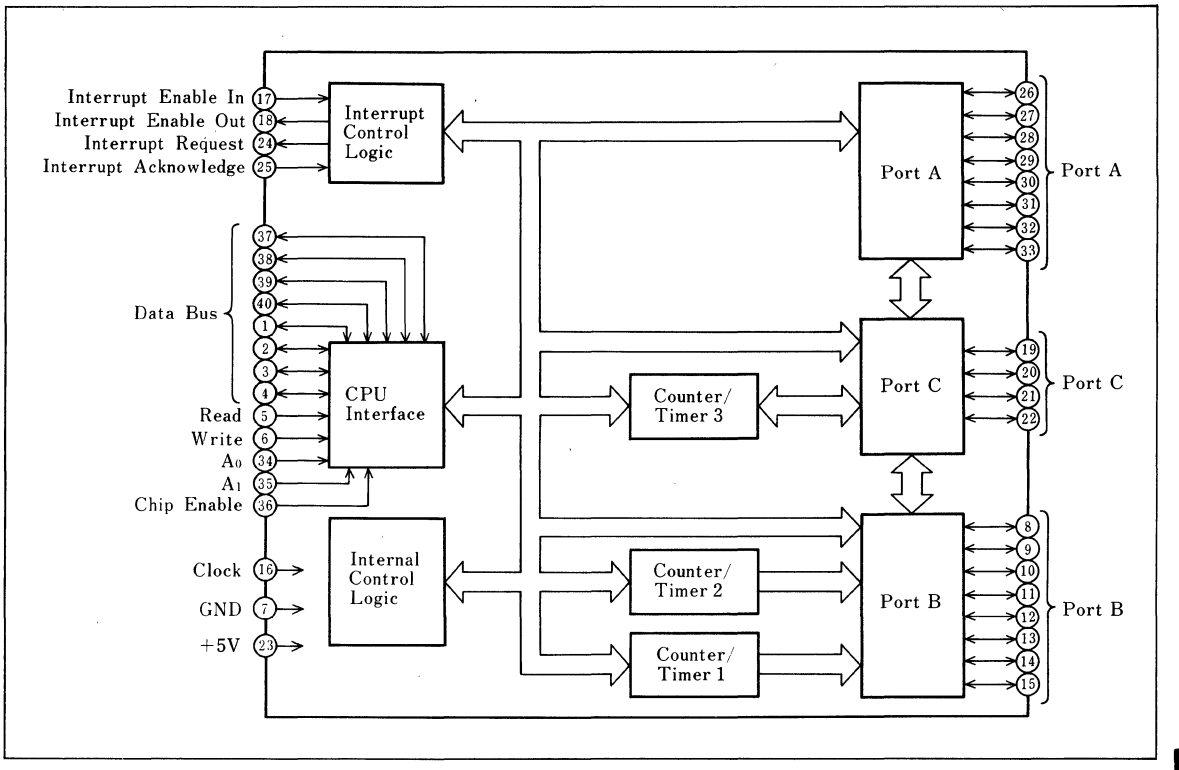
■ Features

1. Two independent 8-bit, double-buffered, bidirectional I/O ports plus a 4-bit special-purpose I/O port. I/O ports feature programmable polarity, programmable direction (Bit mode),"pulse catchers," and programmable open drain outputs.
2. Four handshake modes, including 3-Wire (like the IEEE-488).
3. REQUEST/$\overline{\text{WAIT}}$ signal for high-speed data transfer.
4. Flexible pattern-recognition logic, programmable as a 16-vector interrupt controller.
5. Three independent 16-bit counter/timers with up to four external access lines per counter/timer (count input, output, gate, and trigger), and three output duty cycles (pulsed, one-shot, and squarewave), programmable as retriggerable or nonretriggerable.
6. Easy to use since all registers are read/write.

■ Pin Connections



Block Diagram



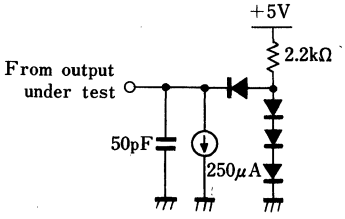
Pin Description

Pin	Meaning	I/O	Function
A_0, A_1	Address select	I	Register select lines
$\overline{CE}$	Chip enable	I	Active low. A low level on this input enables the CIO to be read from or written to.
$D_0 \sim D_7$	Data bus	Bidirectional 3-state	System data bus
IEI	Interrupt enable input	I	Active high. IEI is used to form an interrupt daisy chain which determines the interrupt priority order.
IEO	Interrupt enable output	O	Active high. IEO is used to form an interrupt daisy chain which determines the interrupt priority order.
$\overline{INT}$	Interrupt request	O	Active low, open-drain. Indicates an interrupt to the CPU.
$\overline{INTACK}$	Interrupt acknowledge	I	Active low. Indicates that an interrupt acknowledge cycle is in progress.
$PA_0 \sim PA_7$	I/O port lines	Bidirectional 3-state	Parallel I/O
$PB_0 \sim PB_7$	I/O port lines	Bidirectional 3-state	Parallel I/O
$PC_0 \sim PC_3$	I/O port lines	Bidirectional 3-state	Parallel I/O
$\overline{RD}$	Read	I	Active low. Indicates that a CPU is reading.
$\overline{WD}$	Write	I	Active low. Indicates that a CPU is writing.
PCLK	Clock	I	Single-phase clock. It does not have to be the CPU clock.

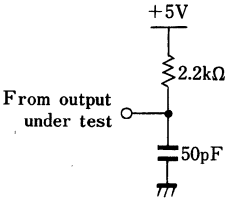
■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Input voltage	V_{IN}	−0.3～+7	V	1
Output voltage	V_{OUT}	−0.3～+7	V	1
Operating temperature	T_{opr}	0～+70	℃	
Storage temperature	T_{stg}	−65～+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.



Standard test load



Open-drain test load

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input high voltage	V_{IH}		2	V_{CC}+0.3	V
Input low voltage	V_{IL}		−0.3	0.8	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4		V
Output low voltage	V_{OL}	I_{OL}=2mA		0.4	V
		I_{OL}=3.2mA		0.5	V
Input leakage current	$\lvert I_{IL} \rvert$	0.4 ≦ V_{IN} ≦ 2.4V		10	μA
Output leakage current	$\lvert I_{OL} \rvert$	0.4 ≦ V_{OUT} ≦ 2.4V		10	μA
Supply current	I_{CC}			200	mA

■ Capacitance

(f=1MHz, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_{IN}	Unmeasured Pins Returned to Ground		10	pF
Output capacitance	C_{OUT}			15	pF
Bidirectional capacitance	$C_{I/O}$			20	pF

■ AC Characteristics

(1) CPU interface timing, interrupt timing, and interrupt acknowledge timing

No.	Symbol	Conditions	LH8536		LH8536A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TcPC	PCLK cycle time	250	4000	165	4000	ns	
2	TwPCh	PCLK width (high)	105	2000	70	2000	ns	
3	TwPCl	PCLK width (low)	105	2000	70	2000	ns	
4	TrPC	PCLK rise time		20		10	ns	
5	TfPC	PCLK fall time		20		15	ns	
6	TsIA(PC)	$\overline{\text{INTACK}}$ to PCLK ↑ setup time	100		100		ns	
7	ThIA(PC)	$\overline{\text{INTACK}}$ to PCLK ↑ hold time	0		0		ns	
8	TsIA(RD)	$\overline{\text{INTACK}}$ to $\overline{\text{RD}}$ ↓ setup time	200		200		ns	
9	ThIA(RD)	$\overline{\text{INTACK}}$ to $\overline{\text{RD}}$ ↑ hold time	0		0		ns	
10	TsIA(WR)	$\overline{\text{INTACK}}$ to $\overline{\text{WR}}$ ↓ setup time	200		200		ns	

No.	Symbol	Parameter	LH8536		LH8536A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
11	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ hold time	0		0		ns	
12	TsA(AD)	Address to $\overline{RD}$ ↓ setup time	80		80		ns	
13	ThA(RD)	Address to $\overline{RD}$ ↑ hold time	0		0		ns	
14	TsA(WR)	Address to $\overline{WR}$ ↓ setup time	80		80		ns	
15	ThA(WR)	Address to $\overline{WR}$ ↑ hold time	0		0		ns	
16	TsCEl(RD)	$\overline{CE}$ low to $\overline{RD}$ ↓ setup time	0		0		ns	1
17	TsCEh(RD)	$\overline{CE}$ high to $\overline{RD}$ ↓ setup time	100		70		ns	1
18	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ hold time	0		0		ns	1
19	TsCEl(WR)	$\overline{CE}$ low to $\overline{WR}$ ↓ setup time	0		0		ns	
20	TsCEh(WR)	$\overline{CE}$ high to $\overline{WR}$ ↓ setup time	100		70		ns	
21	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ hold time	0		0		ns	
22	TwRDl	$\overline{RD}$ low width	390		250		ns	1
23	TdRD(DAR)	$\overline{RD}$ ↓ to read data active delay	0		0		ns	
24	TdRDf(DR)	$\overline{RD}$ ↓ to read data valid delay		255		180	ns	
25	TdRDr(DR)	$\overline{RD}$ ↑ to read data not valid delay	0		0		ns	
26	TdRD(DRz)	$\overline{RD}$ ↑ to read data float delay		70		45	ns	2
27	TwWRl	$\overline{WR}$ low width	390		250		ns	
28	TsDW(WR)	Write data to $\overline{WR}$ ↓ setup time	0		0		ns	
29	ThDW(WR)	Write data to $\overline{WR}$ ↑ hold time	0		0		ns	
30	Trc	Valid access recovery time	1000		650		ns	3
31	TdPM(INT)	Pattern match to $\overline{INT}$ delay(bit port)		2+800		2	ns	6
32	TdACK(INT)	$\overline{ACKIN}$ to $\overline{INT}$ delay(port with handshake)		10+600		10	ns	4,6
33	TdCI(INT)	Counter input to $\overline{INT}$ delay(counter mode)		2+700		2	ns	6
34	TdPC(INT)	PCLK to $\overline{INT}$ delay(time mode)		3+700		3	ns	6
35	TsIA(RDA)	$\overline{INTACK}$ to $\overline{RD}$ ↓(acknowledge)setup time	350		250		ns	5
36	TwRDA	$\overline{RD}$(acknowledge)width	350		250		ns	
37	TdRDA(DR)	$\overline{RD}$ ↓(acknowledge)to read data valid delay		250		180	ns	
38	TdIA(IEO)	$\overline{INTACK}$ ↓ to IEO ↓ delay		350		250	ns	5
39	TdIE(IEO)	IEI to IEO delay		150		100	ns	5
40	TsIEI(RDA)	IEI to $\overline{RD}$ ↓(acknowledge) setup time	100		70		ns	5
41	ThIEI(RDA)	IEI to $\overline{RD}$ ↑(acknowledge) hold time	100		70		ns	
42	TdRDA(INT)	$\overline{RD}$ ↓(acknowledge)to $\overline{INT}$ ↑ delay		600		600	ns	

Note 1: Paramater does not apply to Interrupt Acknowledge transactions.

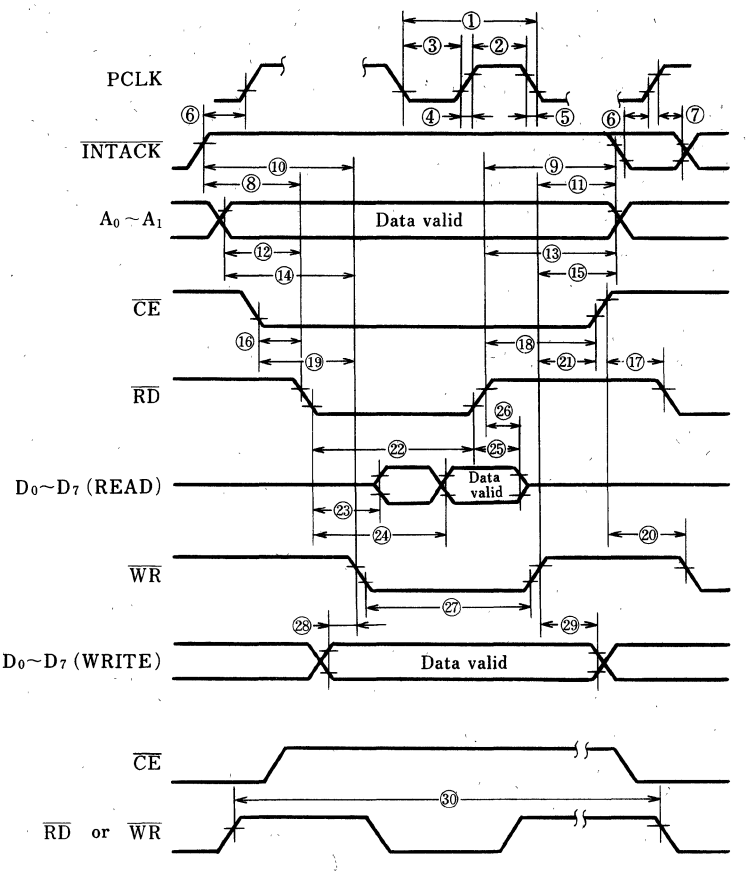
Note 2: Float delay is measured to the time when the output has changed 0.5 V with minimum AC load and maximum DC load.

Note 3: Trc is the specified number or 3 TcPC, whichever is longer.

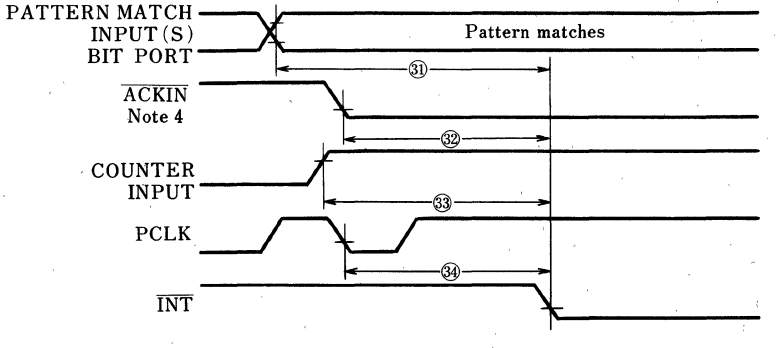
Note 4: The delay is from $\overline{DAV}$ ↓ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wite Output Handshake.

Note 5: The parameters for the devices in any particular daisy chain must meet the following constraint: The delay from $\overline{INTACK}$ ↓ to $\overline{RD}$ ↓ must be greater than the sum of TdIA(IEO)for the highest priority peripheral, TsIEI(RDA)for the lowest priority peripheral, and TdIEI(IEO)for each peripheral separating them in the chain.

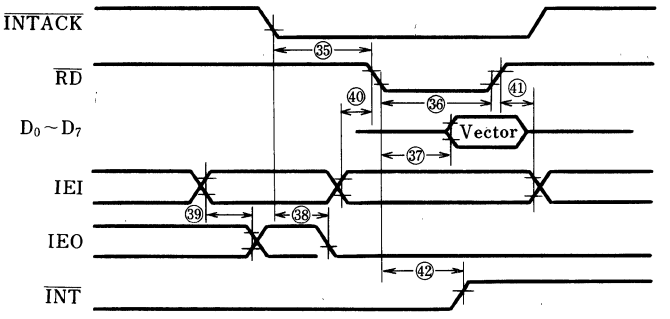
Note 6: Units are equal to TcPC plus ns.



Interface timing



Interrupt timing



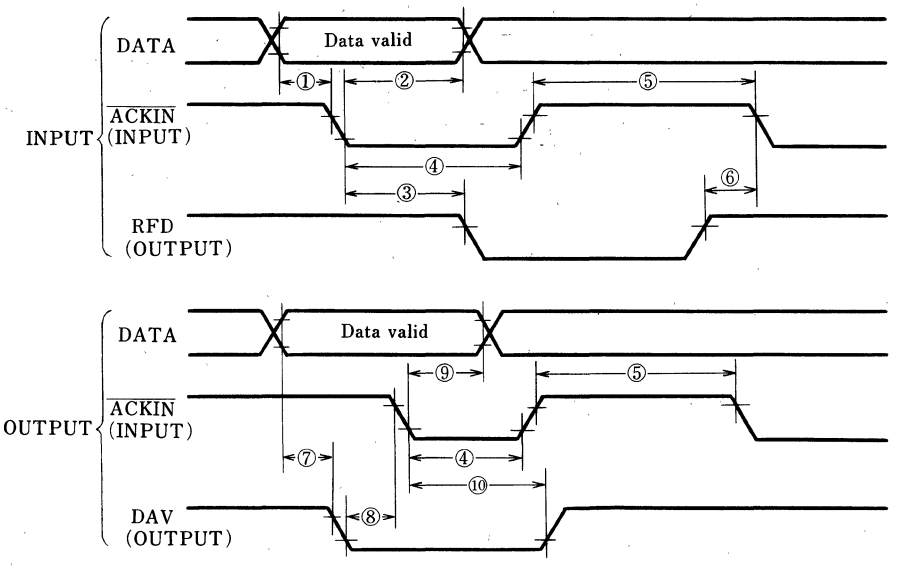
Interrupt acknowledge timing

(2) Handshake timing

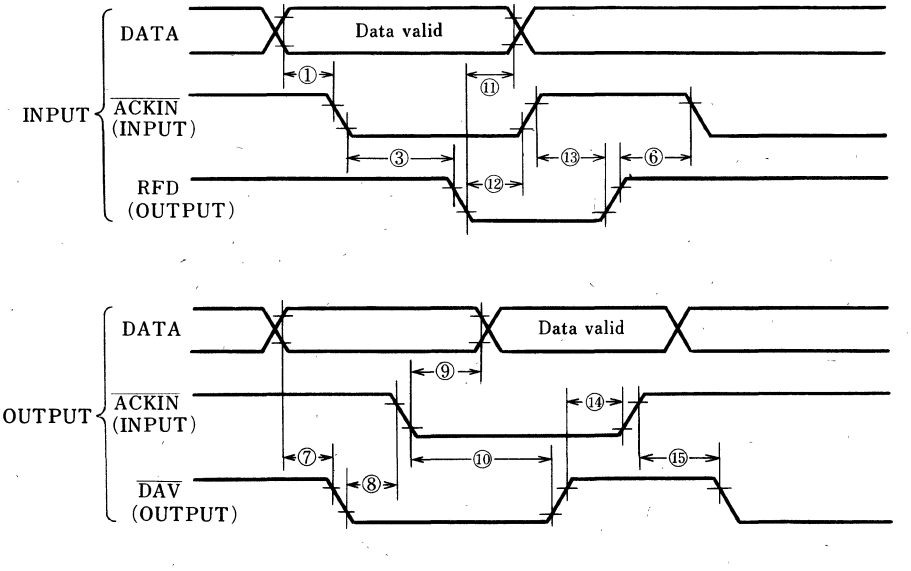
No.	Symbol	Parameter	LH8536		LH8536A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TsDI(ACK)	Data input to $\overline{ACKIN}$ ↓ ($\overline{DAV}$ ↓) setup time	0		0		ns	
2	ThDI(ACK)	Data input to $\overline{ACKIN}$ ↓ hold time strobed handshake					ns	
3	TdACKf(RFD)	$\overline{ACKIN}$ ↓ ($\overline{DAV}$ ↓) to $\overline{RFD}$ ↓ delay	0		0		ns	
4	TwACKl	$\overline{ACKIN}$ low width strobed handshake					ns	
5	TwACKh	$\overline{ACKIN}$ high width strobed handshake					ns	
6	TdRFDr(ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ ($\overline{DAV}$ ↓) delay	0		0		ns	
7	TsDO(DAV)	Data out to $\overline{DAV}$ ↓ setup time	25		20		ns	1
8	TdDAVf(ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ delay	0		0		ns	
9	ThDO(ACK)	Data out to $\overline{ACKIN}$ ↓ hold time	2		2		ns	2
10	TdACK(DAV)	$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ delay	2		2		ns	2
11	ThDI(RFD)	Data input to RFD ↓ hold time interlocked handshake					ns	
12	TdRFDf(ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ delay interlocked handshake	0		0		ns	
13	TdACKr(RFD)	$\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ delay interlocked and 3-wire handshake	0		0		ns	
14	TdDAVr(ACK)	$\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑ (RFD ↑) interlocked and 3-wire handshake	0		0		ns	
15	TdACK(DAV)	$\overline{ACKIN}$ ↑ (RFD ↑) to $\overline{DAV}$ ↓ delay interlocked and 3-wire handshake	0		0		ns	
16	TdDAVIf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ delay input 3-wire handshake	0		0		ns	
17	ThDI(DAC)	Data input to DAC ↑ hold time 3-wire handshake	0		0		ns	
18	TdDACOr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ delay input 3-wire handshake	0		0		ns	
19	TdDAVIr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ delay input 3-wire handshake	0		0		ns	
20	TdDAVOf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ delay output 3-wire handshake	0		0		ns	
21	ThDO(DAC)	Data output to DAC ↑ hold time 3-wire handshake	2		2		ns	2
22	TdDACIr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ delay output 3-wire handshake	2		2		ns	2
23	TdDAVOr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ delay output 3-wire handshake	0		0		ns	

Note 1: This time can be extended through the use of deskew timers.

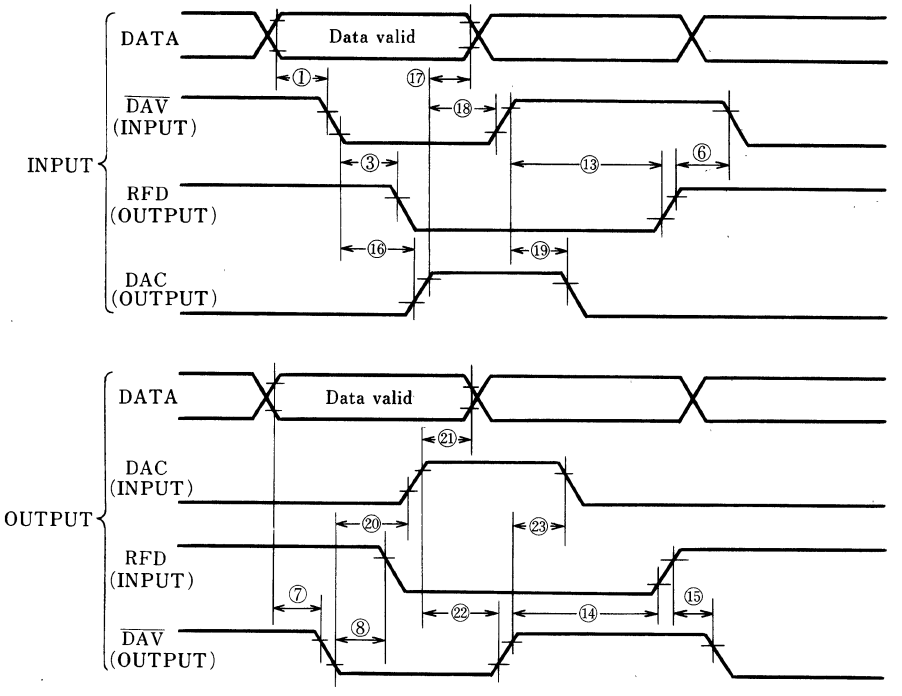
Note 2: Units equal to TcPC.



Strobed handshake



Interlocked handshake

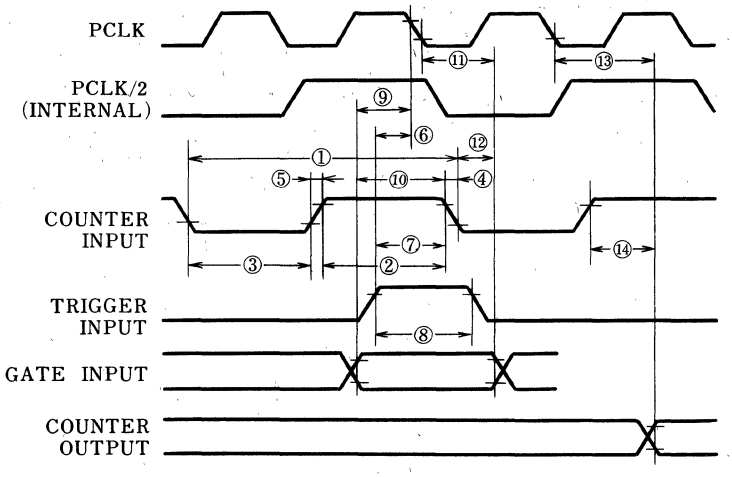


3-wire handshake

(3) Counter/timer timing

No.	Symbol	Parameter	LH8536		LH8536A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TcCI	Counter input cycle time	500		330		ns	
2	TCIh	Counter input high width	230		150		ns	
3	TWCIl	Counter input low width	230		150		ns	
4	TfCI	Counter input fall time		20		15	ns	
5	TrCI	Counter input rise time		20		15	ns	
6	TsTI(PC)	Trigger input to PCLK ↓ setup time (timer mode)					ns	1
7	TsTI(CI)	Trigger input to counter input ↓ setup time (counter mode)					ns	1
8	TwTI	Trigger input pulse width (high or low)					ns	
9	TsGI(PC)	Gate input to PCLK ↓ setup time (timer mode)					ns	1
10	TsGI(CI)	Gate input to counter input ↓ setup time (counter mode)					ns	1
11	ThGI(PC)	Gate input to PCLK ↓ hold time (timer mode)					ns	1
12	ThGI(CI)	Gate input to counter input ↓ hold time (counter mode)					ns	1
13	TdPC(CO)	PCLK to counter output delay (timer mode)					ns	
14	TdCI(CI)	Counter input ↑ to counter output delay (counter mode)					ns	

Note 1: These parameters must be met to guarantee trigger or gate are valid for the next counter/timer cycle.



Counter/timer timing

■ Functional Description

(1) I/O port operations

Of the LH8536 three I/O ports, two (Ports A and B) are general purpose, and the third (Port C) is a special purpose 4-bit port. Ports A and B can be configured as input, output, or bidirectional ports with handshake. (Four different handshakes are available.) They can also be linked to form a single 16-bit port. If they are not used as ports with handshake, they provide 16 input or output bits with the data direction programmable on a bit-by-bit basis. Port B also provides access for Counter/Timers 1 and 2. In all configurations, ports A and B can be programmed to recognize specific data patterns and to generate interrupts when the pattern is encountered.

The four bits of Port C provide the handshake lines for Ports A and B when required. A REQUEST/$\overline{\text{WAIT}}$ line can also be provided so that LH8536 transfers can be synchronized with DMAs or CPUs. Any Port C bits not used for handshake or REQUEST/$\overline{\text{WAIT}}$ can be used as input or output bits (individually data-direction programmable) or external access lines for Counter/Timer 3. Port C does not contain any pattern-recognition logic. It is, however, capable of bit-addressable writes. With this feature, any combination of bits can be set and/or cleared while the other bits remain undisturbed without first reading the register.

(2) Bit port operations

In bit port operations, the port's Data Direction register specifies the direction of data flow for each bit. Port C has the additional feature of bit-addressable writes. When writing to Port C, the four most significant bits are used as write protect mask for the least significant bits (0-4, 1-5, 2-6, and 3-7). If the write protect bit is written with a 1, the state of the corresponding output bit is not changed.

The capability of inverting the data path can be provided, and output can be specified as open-drain.

(3) Ports with handshake operation

Ports A and B can be specified as 8-bit input, output, or bidirectional ports with handshake. The LH8536 provides four different handshakes for its ports: Interlocked, Strobed, Pulsed, and 3-Wire.

The port can be set as if it is only single-buffered. This is useful if the handshake line must be stopped on a byte-by-byte basis.

Ports A and B can be linked to form a 16-bit port.

In this mode, Post A must be specified for handshake, and Port B must be specified as a bit port. When linked, only Port A has pattern-match capability. Port B's pattern match capabiliy must be disabled.

Table 1 Port C bit utilization

Port A/B Configuration	PC_3	PC_2	PC_1	PC_0
Port A and B: Bit port	Bit I/O	Bit I/O	Bit I/O	Bit I/O
Port A: Input or output port (interlocked, strobed, or pulsed handshake)	RFD or $\overline{DAV}$(O)	$\overline{ACKIN}$(I)	REQUEST/$\overline{WAIT}$(O) or Bit I/O	Bit I/O
Port B: Input or output port (interlocked, strobed, or pulsed handshake)	REQUEST/$\overline{WAIT}$(O) or Bit I/O	Bit I/O	RFD or $\overline{DAV}$(O)	$\overline{ACKIN}$ (I)
Port A or B: Input port (3-wire handshake)	RFD(O)	$\overline{DAV}$(I)	REQUEST/$\overline{WAIT}$(O) or Bit I/O	DAC(O)
Port A or B: Output port (3-wire handshake)	$\overline{DAV}$(O)	DAC(I)	REQUEST/$\overline{WAIT}$(O) or Bit I/O	RFD(I)
Port A or B: Bidirectional port (interlocked or strobed handshake)	RFD or $\overline{DAV}$(O)	$\overline{ACKIN}$(I)	REQUEST/$\overline{WAIT}$(O) or Bit I/O	IN/$\overline{OUT}$(I/O)

* Both Ports A and B can be specified input or output with Interlokced, Strobed, Pulsed Handshake at the same time if RFQUEST/$\overline{WAIT}$.

(4) Interlocked handshake

In the Interlocked handshake mode, the action of the LH8536 must be acknowledged by the external device before the next action can take place. Figure 1 shows timing for Interlocked Handshake. An output port does not indicate that new data is available until the external device indicates it is ready for the data. Similarly, an input port does not indicate that it is ready for new data until the data source indicates that the previous byte of the data is no longer available, thereby acknowledging the input port's acceptance of the last byte. This allows the LH8536 to interface directly to the port of a Z8 microcomputer, a UPC, an FIO, an FIFO, or to another CIO port with no external logic.

A 4-bit deskew timer can be inserted in the Data Available ($\overline{DAV}$) output for output ports.

The deskew timer guarantees that the output data is valid for a specified minimum amount of time.

Deskew timers are available for output ports independent of the type of handshake employed.

(5) Strobed handshake.

In the Strobed handshake mode, data is "strobed" into or out of the port by the external logic. Fig. 1 shows timing for the Strobed handshake. IN contrast to the Interlocked handshake, the signal indicating the port is ready for another data transfer operates independently of the $\overline{ACKIN}$ input. It is up to the external logic to ensure that data overflows or underflows do not occur.

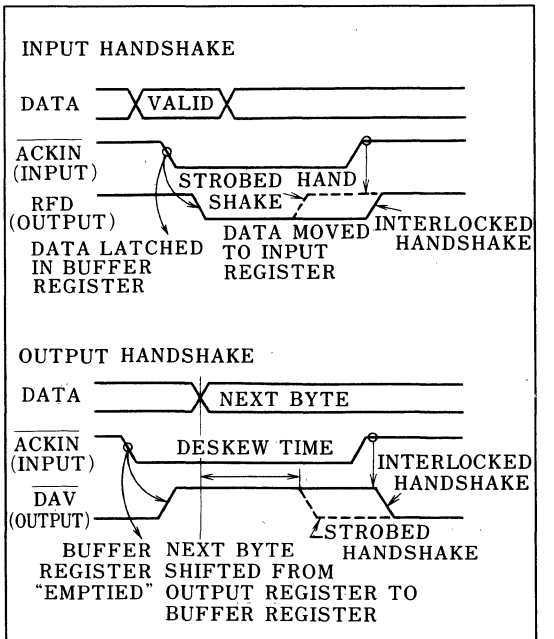


Fig.1 Interlocked and strobed handshakes

(6) 3-wire handshake

The 3-wire handshake is designed for the situation in which one output port is communicating with many input ports simultaneously. It is essentially the same as the Interlocked handshake, except that two signals are used to indicate if an input port is ready for new data or if it has accepted the present data (Fig. 2). With the 3-wire handshake, the output lines of many input ports can be bussed together with open-drain drivers; the output port knows when all the ports have accepted the data and are ready. This is the same handshake as is used on the IEEE-488 bus. Because this handshake requires three lines, only one port (either A or B) can be a 3-wire handshake port at a time. The 3-wire handshake is not available for the bidirectional mode. Because the port's direction can be changed under software control, however, bidirectional IEEE-488-type transfers can be performed.

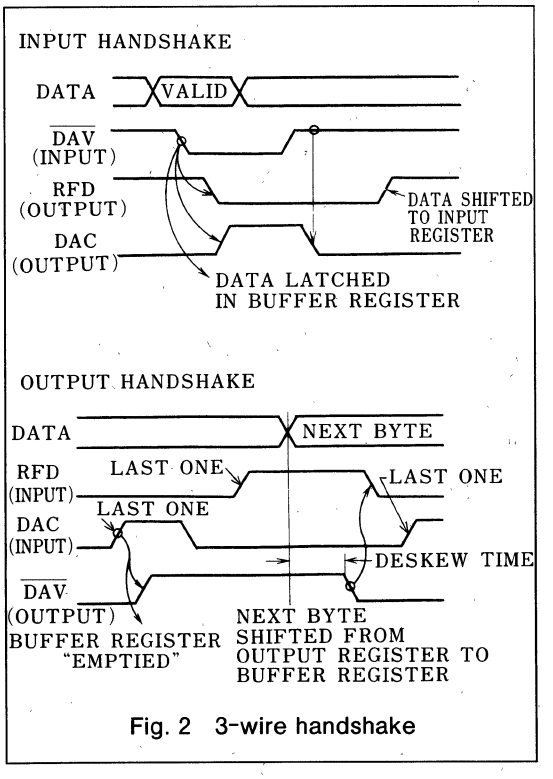


Fig. 2 3-wire handshake

(7) Pulsed handshake

The Pulsed handshake (Fig. 3) is designed to interface to mechanical-type devices that require data to be held for long periods of time and need relatively wide pulses to gate the data into or out of the device. The logic is the same as the Interlocked handshake mode, except that an internal counter/timer is linked to the handshake logic.

The counter/timer maintains all of its normal capabilities. This handshake is not available for bidirectional ports.

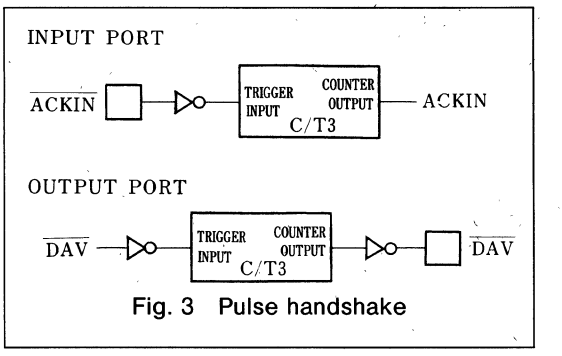


Fig. 3 Pulse handshake

(8) Pattern-recognition logic operation

Both Ports A and B can be programmed to generate interrupts when a specific pattern is recognized at the port. The pattern-recognition logic is independent of the port application, thereby allowing the port to recognize patterns in all of its configurations. The pattern can be independently specified for each bit as 1, 0, rising edge, falling edge, or any transition. Individual bits may be masked off.

(9) Bit port pattern-recognition operations

During bit port operations, pattern-recognition may be performed on all bits, including those used as I/O for the counter/timers.

The pattern-recognition logic of bit ports operates in two basic modes: transparent and latched. In transparent mode, the interrupt indicates that a specified pattern has occurred, but a read of the Data register does not necessarily indicate that state of the port at the time the interrupt was generated. In the Latched mode, the state of all the port inputs at the time the interrupt was generated is latched in the input register and held until IP is cleared.

(10) Counter/timer operation

The three independent 16-bit counter/timers consist of a presettable 16-bit down counter, a 16-bit Time Constant register, a 16-bit Current Counter register, an 8-bit Mode Specification register, an 8-bit Command and Status register, and the associated control logic that links these registers.

The flexibility of the counter/timers is enhanced by the provision of up to four lines per counter/timer (counter input, gate input, trigger input, and counter/timer output) for direct external control and status. Counter/Timer 1's external I/O lines are

provided by the four most significant bits of port B.

Counter/Timer 2's are provided by the four least significant bits of Port B. Counter/Timer 3's external I/O lines are provided by the four bits of Port C. The utilization of these lines (Table 2) is programmable on a bit-by-bit basis via the Counter/Timer Mode Specification registers.

Table 2 Counter/timer external access

Function	C/T1	C/T2	C/T3
Counter/Timer Output	PB_4	PB_0	PC_0
Counter Input	PB_5	PB_1	PC_1
Trigger Input	PB_6	PB_2	PC_2
Gate Input	PB_7	PB_3	PC_3

Lines used for counter/timer I/O have the same characteristics as simple input lines, they can be specified as inverting or noninverting; they can be read and used with the pattern-recognition logic. They can also include the 1's catcher input.

Counter/Timers 1 and 2 can be linked internally in three different ways. Counter/Timer 1's output (inverted) can be used as Counter/Timer 2's trigger, gate, or counter input.

When linked, the counter/timers have the same capabilities as when used separately. The only restriction is that when Counter/Timer 1 drives Counter 2's count input, Counter/Timer 2 must be programmed with its external count input disabled.

There are three duty cycles available for the timer / counter output: pulse, one-shot, and square-wave . Fig. 4 shows the counter/timer waveforms.

Counter/timer operations require loading the time constant value in the Time Constant register and initiating the countdown sequence by loading the down-counter with the time constant value. The Time Constant register is accessed as two 8-bit registers. The registers are readable as well as writable, and the access order is irrelevant.

Once the down-counter is loaded, the countdown sequence continues toward terminal count as long as all the counter/timers' hardware and software gate inputs are High. If any of the gate inputs Low (0), the countdown halts. It resumes when all gate inputs are 1 again.

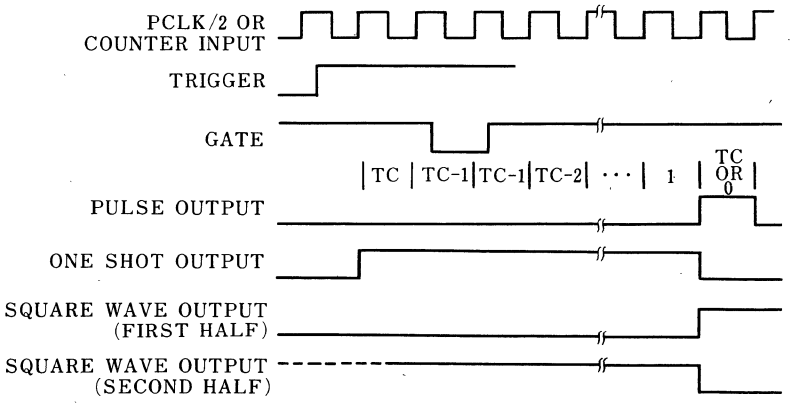


Fig. 4 Counter/timer waveforms

■ Internal Registers

The followings illustrate the contents of the registers and, in addition, given to register address summary.

● Master Interrupt Control Register (MICR)

Address : 000000
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

- D_7 : MASTER INTERRUPT ENABLE (MIE)
- D_6 : DISABLE LOWER CHAIN (DLC)
- D_5 : NO VECTOR (NV)
- D_4 : PORT A VECTOR INCLUDES STATUS (PA VIS)
- D_3 : PORT B VECTOR INCLUDES STATUS (PB VIS)
- D_2 : COUNTER/TIMERS VECTOR INCLUDES STATUS (CT VIS)
- D_1 : RIGHT JUSTIFIED ADDRESSES
  0 = SHIFT LEFT (A_0 from AD_1)
  1 = RIGHT JUSTIFY (A_0 from AD_0)
- D_0 : RESET

● Master Configuration Control Register (MCCR)

Address : 000001
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

- D_7 : PORT B ENABLE (PBE)
- D_6 : COUNTER/TIMER 1 ENABLE (CT1E)
- D_5 : COUNTER/TIMER 2 ENABLE (CT2E)
- D_4 : PORT C AND COUNTER/TIMER 3 ENABLE (PCE AND CT3E)
- D_3 : PORT A ENABLE (PAE)
- D_2 : PORT LINK CONTROL (PLC)
  0 = PORTS A AND B OPERATE INDEPENDENTLY
  1 = PORTS A AND B ARE LINKED
- D_1, D_0 : COUNTER/TIMER LINK CONTROLS (LC)

LC1	LC0	
0	0	COUNTER/TIMERS INDEPENDENT
0	1	C/T 1's $\overline{\text{OUTPUT}}$ GATES C/T 2
1	0	C/T 1's $\overline{\text{OUTPUT}}$ TRIGGERS C/T 2
1	1	C/T 1's $\overline{\text{OUTPUT}}$ IS C/T 2's COUNT INPUT

● Port Mode Specification Register (PMSR)

Addresses : 1100000 Port A
101000 Port B
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

- D_7, D_6 : PORT TYPE SELECTS (PTS)

PTS1	PTS0	
0	0	BIT PORT
0	1	INPUT PORT
1	0	OUTPUT PORT
1	1	BIDIRECTIONAL PORT

- D_5 : INTERRUPT ON TWO BYTES (ITB)
- D_4 : SINGLE BUFFERED MODE (SB)
- D_3 : INTERRUPT ON MATCH ONLY (IMO)
- D_2 : LATCH ON PATTERN MATCH (LPM) (BIT MODE)
  DESKEW TIMER ENABLE (DTE) (HANDSHAKE MODES)
- D_1, D_0 : PATTERN MODE SPECIFICATION BITS (PMS)

PMS1	PMS0	
0	0	DISABLE PATTERN MATCH
0	1	"AND" MODE
1	1	"OR" MODE
1	1	"OR PRIORITY ENCODED VECTOR" MODE

● Port Handshake Specfication Registers (PHSR)

Addressess : 100001 Port A
101001 Port B

(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

HANDSHAKE TYPE SPECIFICATION BITS (HTS)

HTS1	HTS0	
0	0	INTERLOCKED HANDSHAKE
0	1	STROBED HANDSHAKE
1	0	PULSED HANDSHAKE
1	1	THREE-WIRE HANDSHAKE

DESKEW TIME SPECIFICATION BITS
SPECIFIES THE MSB's OF DESKEW TIMER TIME CONSTANT.
LSB IS FORCED 1.

REQUEST/$\overline{\text{WAIT}}$ SPECIFICATION BIT (RWS)

RWS2	RWS1	RWS0	FUNCTION
0	0	0	REQUEST/$\overline{\text{WAIT}}$ DISABLED
0	0	1	OUTPUT $\overline{\text{WAIT}}$
0	1	1	INPUT $\overline{\text{WAIT}}$
1	0	0	SPECIAL REQUEST
1	0	1	OUTPUT REQUEST
1	1	1	INPUT REQUEST

● Port Command and Status Registers (PCSR)

Addresses : 001000 Por A
001001 Por B

(Read/Partial Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

INTERRUPT UNDER SERVICE (IUS)
INTERRUPT ENABLE (IE)
INTERRUPT PENDING (IP)
IUS, IE, AND IP ARE WRITTEN USING THE FOLLOWING CODE :

NULL CODE	0	0	0
CLEAR IP & IUS	0	0	1
SET IUS	0	1	0
CLEAR IUS	0	1	1
SET IP	1	0	0
CLEAR IP	1	0	1
SET IE	1	1	0
CLEAR IE	1	1	1

INTERRUPT ON ERROR (IOE)
PATTERN MATCH FLAG (PMF) (READ ONLY)
INPUT REGISTER FULL (IRF) (READ ONLY)
OUTPUT REGISTER EMPTY (ORE) (READ ONLY)
INTERRUPT ERROR (ERR) (READ ONLY)

● Data Path Polarity Registers (DPPR)

Addresses : 100010 Port A
101010 Port B
000101 Port C (4 LSBs only)
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA PATH POLARITY (DPP)
0 = NON-INVERTING
1 = INVERTING

● Data Direction Registers (DDR)

Addresses : 100011 Port A
101011 Port B
000110 Port C (4 LSBs only)
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA DIRECTION (DD)
0 = OUTPUT BIT
1 = INPUT BIT

*These registers can be addressed directly.

● Special I/O Control Registers (SIOCR)

Addresses : 100100 Port A
101100 Port B
000111 Port C (4 LSBs only)
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

SPECIAL INPUT/OUTPUT (SIO)
0 = NORMAL INPUT OR OUTPUT
1 = OUTPUT WITH OPEN DRAIN OR INPUT WITH 1's CATCHER

● Port Data Registers (PDR)

Addresses : 001101 Port A*
001110 Port B*
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

● Port C Data Registers (PCDR)

Address : 001111*
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

4 MSBs

0 = WRITING OF CORRESPONDING LSB ENABLED
1 = WRITING OF CORRSPONDING LSB INHIBITED
(READ RETURNS 1)

● Pattern Polarity Registers (PPR)

Addresses : 100101 Port A
101101 Port B
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

● Pattern Transition Registers (PTR)

Addresses : 100110 Port A
101110 PortB
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

● Pattern Mask Registers (PMR)

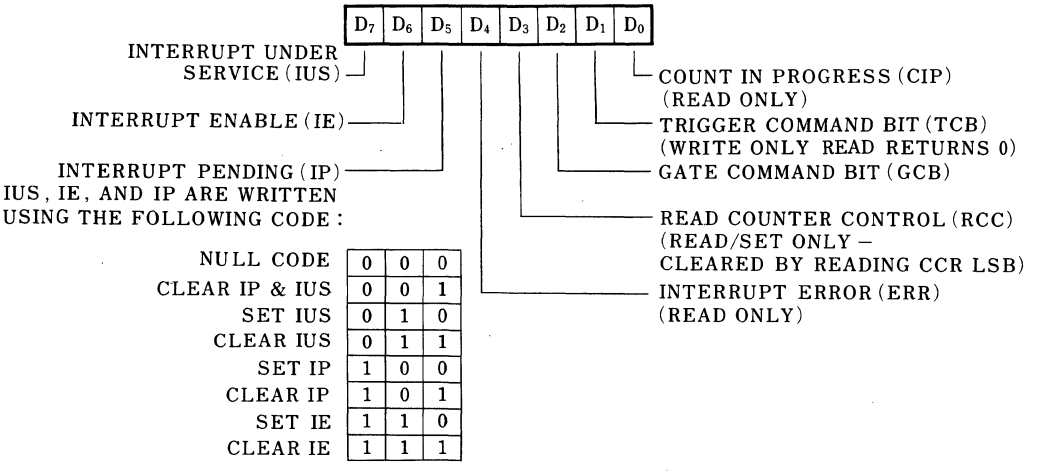
Addresses : 100111 Port A
101111 Port B
(Read/Write)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

PM	PT	PP	PATTERN SPECIFICATION
0	0	×	BIT MASKED OFF
0	1	×	ANY TRANSITION
1	0	0	ZERO
1	0	1	ONE
1	1	0	ONE TO ZERO TRANSITION (↘)
1	1	1	ZERO-TO-ONE TRANSITION (↗)

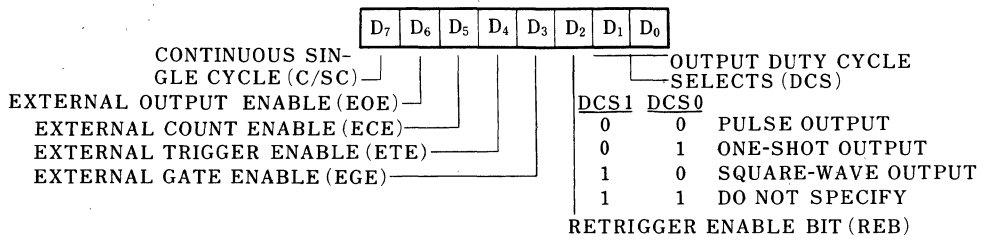
● Counter/Timer Command Status Registers (CTCSR)

Addresses : 001010 Counter/Timer 1
001011 Counter/Timer 2
001100 Counter/Timer 3
(ead/Partial Write)



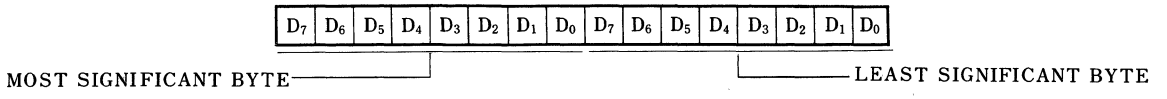
● Counter/Timer Mode Specifications Registers (CTMSR)

Addresses : 011100 Counter/Timer 1
011101 Counter/Timer 2
Counter/Timer 3
(Read/Write)



● Counter/Timer Current Count Registers (CTCCR)

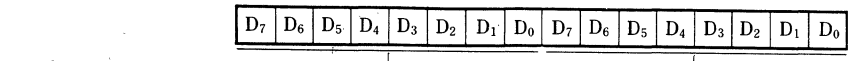
Addresses : 010000 Counter/Timer 1's MSB
010001 Counter/Timer 1's LSB
010010 Counter/Timer 2's MSB
010011 Counter/Timer 2's LSB
010100 Counter/Timer 3's MSB
010101 Counter/Timer 3's LSB
(Read Only)



● Counter/Timer Time Constant Registers (CTTCR)

Addresses : 010110 Counter/Timer 1's MSB
010111 Counter/Timer 1's LSB
011000 Counter/Timer 2's MSB
011001 Counter/Timer 2's LSB
011010 Counter/Timer 3's MSB
011011 Counter/Timer 3's LSB

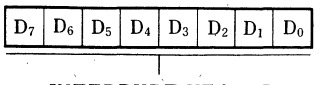
(Read/Write)



● Interrupt Vector Register (IVR)

Addresses : 000010 Port A
000011 Port B
000100 Counter/Timers

(Read/Write)



● Counter/Timer Status

D_2	D_1	
0	0	C/T3
0	1	C/T2
1	0	C/T1
1	1	Error

● Port Vector Status

(1) Priority Encoded Vector Mode

D_3 D_2 D_1	
× × ×	Number of highest priority bit with a match

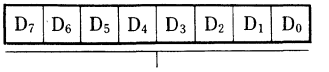
(2) All Other Mode

D_3 D_2 D_1	
ORE IRF PMF	Normal
0 0 0	Error

● Current Vector Register (CVR)

Address : 011111

(Read only)



INTERRUPT VECTOR BASED ON HIGTEST PRIORITY UNMASKED IP.
IF NO INTERRUPT PENDING ALL 1's OUTPUT.

LH8571 Serial Parallel Combination Controller

■ Description

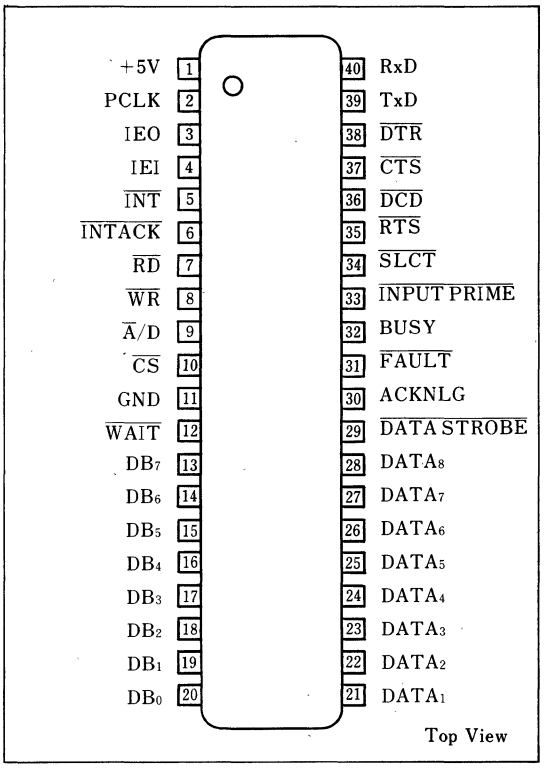
The LH8571 (SPCC71) is a peripheral interface device for general purpose microcomputer systems with two main control functions for an RS232C interface and Centronics interface, all within a single LSI chip.

The LH8571 provides a serial port for transferring data in asynchronous mode and an 8-bit parallel port with handshaking function as a Centronics interface.

The LH8571 has 24 commands for controlling these ports. The commands not only control the operation of RS232C teminal units and printers, but handle various utilities (e.g.,code conversion) necessary for these units. Accordingly, the CPU needs merely to specity an operation through the commands, thus significantly reducing the CPU's load in handling I/O units through the program, and eventually reducing the amount of memory needed for storing the program.

The LH8571 controls the peripheral unit control lines (e.g.,$\overline{RTS}$ and $\overline{CTS}$ of RS232C interface) according to the status of the units, instead of by software control from the CPU. Consequently, the system designer can configure the interface merely by connecting buffer devices and connectors.

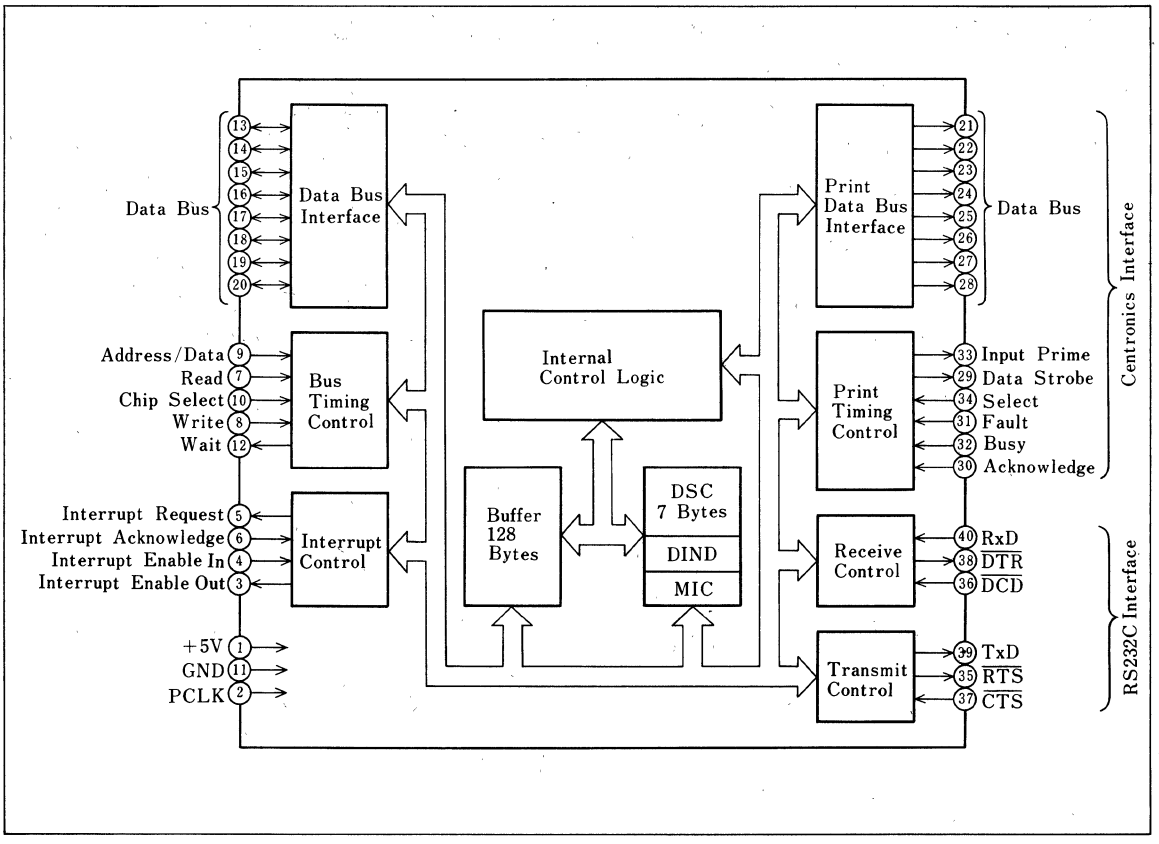
■ Pin Connections



■ Features

1. Asynchronous data transfer serial port
   - RS232C interface can easily be realized.
2. Printer control parallel port
   - Centronics interface can easily be realized.
3. Data transfer and conversion functions by command.
   - 24 commands.
4. Data conversion function.
   - Serial parallel conversion.
   - Binary-ASCII conversion.
   - Intel hex, format acceptable for data input/output.
5. 128-byte data transfer bufter.
   - Useful for the serial port and parallel port.
6. Non-multiplexed bus interface.
7. 40-pin dual-in-line package.
8. Single + 5V power supply.

■ Block Diagram



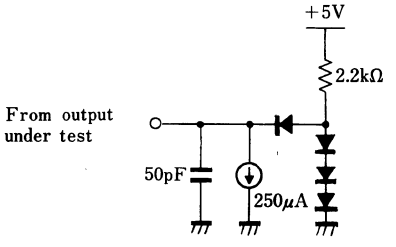
■ Pin Description

Pin	Meaning	I/O	Function
DB_0~DB_7	Data bus	Bidirectional 3-state	System data bus
$\overline{A/D}$	Address/data select	I	Address/data select signal
$\overline{RD}$	Read	I	Active low. Indicate the system in read operation.
$\overline{WR}$	write	I	Active low. Indicate the system in write operation
$\overline{CS}$	Chip select	I	Active low. Chip selection signal
$\overline{WAIT}$	Wait	O	Active low, open-drain. Used to synchronize with CPU.
$\overline{INT}$	Interrupt request	O	Active low, open-drain. Indicate interrupt request to input.
$\overline{INTACK}$	Interrupt acknowledge	I	Active low. Indicate interrupt acknowledge cycle.
IEI	Interrupt enable input	I	Active high. Used to form interrupt priority arbitration loop circuit (daisy chain).
IEO	Interrupt enable output	O	Active high. Used to form daisy chain.
$DATA_1$~$DATA_8$	Output data	O	Output data
$\overline{DATA\ STROBE}$	Data strobe	O	Active low. Indicate settlement of data.
BUSY	Busy	I	Active high. Indicate printer in operation.
ACKNLG	Acknowledge	I	Active high. Acknowledge signal from printer.
$\overline{FAULT}$	Fault	I	Active low. Indicate printer inoperable.
$\overline{INPUT\ PRIME}$	Prime input	O	Active low. Printer initializing signal.
$\overline{SLCT}$	Select	I	Active low. Printer selection signal.
RxD	Received data	I	Receiving data line.
TxD	Transmitted data	O	Transmitting data line.
$\overline{RTS}$	Transmission request	O	Active low. Indicate readiness for data transmission.
$\overline{CTS}$	Transmission enable	I	Active low. Indicate data transmission is possible.
$\overline{DTR}$	Data terminal ready	O	Active low. Data transmission request signal.
$\overline{DCD}$	Reception enable	I	Active low. Indicate data reception is possible.
PCLK	Clock	I	Single-phase clock. Need not be same as CPU clock.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage*	V_{IN}	−0.3~+7	V
Output voltage*	V_{OUT}	−0.3~+7	V
Operating temperature	T_{opr}	0~+70	℃
Storage temperature	T_{stg}	−65~+150	℃

* The maximum applicable voltage on any pin with respect to GND.



Standard test load

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0~+70℃)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Clock input high voltage	V_{CH}		2.4	V_{CC}	V
Clock input low voltage	V_{CL}		−0.3	0.8	V
Input high voltage	V_{IH}		2	V_{CC}	V
Input low voltage	V_{IL}		−0.3	0.8	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4		V
Output low voltage	V_{OL}	I_{OL}=2mA		0.4	V
Input leakage current	$\lvert I_{IL} \rvert$	$0 \leqq V_{IN} \leqq 5.25V$		10	μA
Output leakage current	$\lvert I_{OL} \rvert$	$0 \leqq V_{IN} \leqq 5.25V$		10	μA
Current consumption	I_{CC}			250	mA

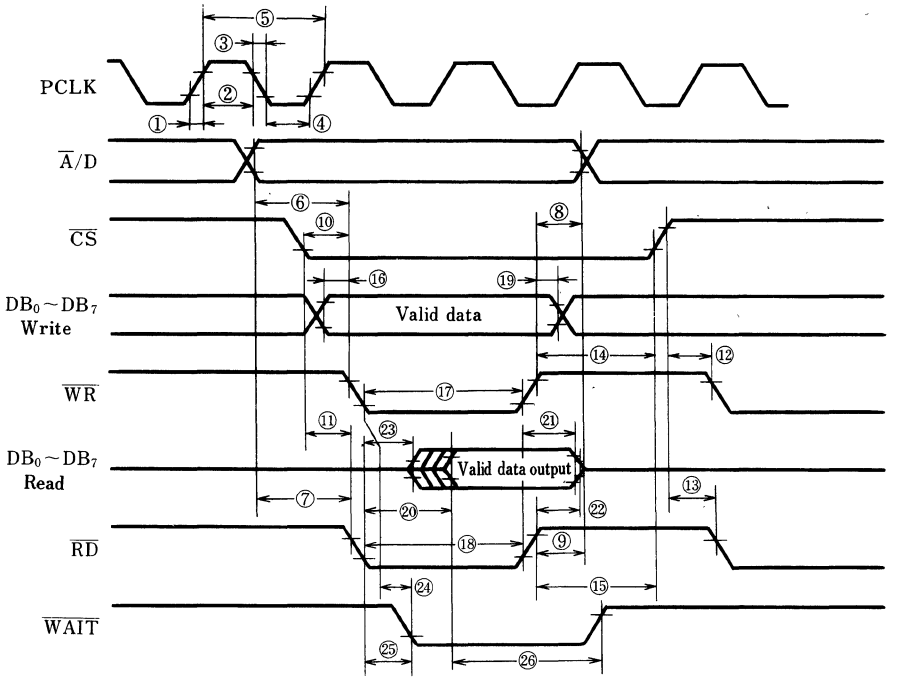
■ AC Characteristics

(1) CPU interface timing

(V_{CC}=5V±5%, Ta=0~+70℃)

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TrC	Clock rise time		20	ns	
2	TwCh	Clock pulse width, high	105		ns	
3	TfC	Clock fall time		20	ns	
4	TwCl	Clock pulse width, low	105		ns	
5	TpC	Clock period	250		ns	
6	TsA/D(WR)	$\overline{A}$/D setup time to $\overline{WR}$ ↓	80		ns	
7	TsA/D(RD)	$\overline{A}$/D setup time to $\overline{RD}$ ↓	80		ns	
8	ThA/D(WR)	$\overline{A}$/D hold time from $\overline{WR}$ ↑	30		ns	
9	ThA/D(RD)	$\overline{A}$/D hold time from $\overline{RD}$ ↑	30		ns	
10	TsCSf(WR)	$\overline{CS}$ low setup time to $\overline{WR}$ ↓	0		ns	
11	TsCSf(RD)	$\overline{CS}$ low setup time to $\overline{RD}$ ↓	0		ns	
12	TsCSr(WR)	$\overline{CS}$ high setup time to $\overline{WR}$ ↓	60		ns	
13	TsCSr(RD)	$\overline{CS}$ high setup time to $\overline{RD}$ ↓	60		ns	
14	ThCS(WR)	$\overline{CS}$ low hold time from $\overline{WR}$ ↑	0		ns	
15	ThCS(RD)	$\overline{CS}$ low hold time from $\overline{RD}$ ↑	0		ns	
16	TsDI(WR)	Written data setup time to $\overline{WR}$ ↓	0		ns	
17	Tw(WR)	$\overline{WR}$ pulse width	390		ns	
18	Tw(RD)	$\overline{RD}$ pulse width	390		ns	
19	ThWR(DI)	Written data hold time from $\overline{WR}$ ↑	0		ns	
20	TdRD(DI)	Delay time from $\overline{RD}$ ↓ to valid data			ns	1
21	ThRD(DI)	Written data hold time from $\overline{RD}$ ↑	0		ns	
22	TdRD(DIz)	Delay time from $\overline{RD}$ ↑ to data bus floating		70	ns	
23	TdRD(DB_A)	Delay time from $\overline{RD}$ ↓ to readout data settlement	0		ns	
24	TdWR(W)	Delay time from $\overline{WR}$ ↓ to $\overline{WAIT}$ ↓		150	ns	
25	TdRD(W)	Delay time from $\overline{RD}$ ↓ to $\overline{WAIT}$ ↓		150	ns	
26	TdDI(W)	Delay time from valid data to $\overline{WAIT}$ ↑	0		ns	

Note : All AC output characteristics are based on the stated load conditions.
Note 1: The delay time depends on the device status at the time of access by CPU.

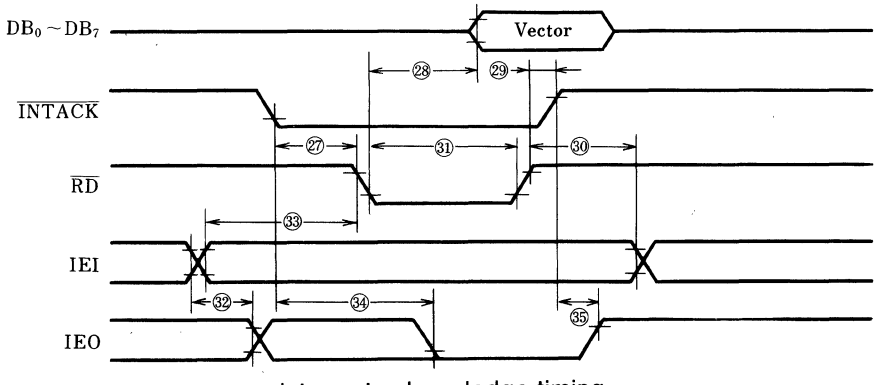


CPU interface timing

(2) Interrupt acknowledge timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
27	TsACK(RD)	$\overline{INTACK}$ low setup time to $\overline{RD}$ ↓	90		ns	2
28	TdRD(DI)	Delay time from $\overline{RD}$ ↓ to valid vector		255	ns	
29	ThRD(ACK)	$\overline{INTACK}$ low hold time from $\overline{RD}$ ↑	0		ns	
30	ThIEI(RD)	IEI hold time from $\overline{RD}$ ↑	100		ns	
31	TwRDI	$\overline{RD}$ (Acknowledge) low pulse width	255		ns	
32	TdIEI(IEO)	Delay time from IEI to IEO		120	ns	
33	TsIEI(RD)	IEI setup time to $\overline{RD}$ ↓	150		ns	
34	TdACK(IEO)	Delay time from $\overline{INTACK}$ ↓ to IEO ↓		250	ns	
35	TdADKr(IEO)	Delay time from $\overline{INTACK}$ ↑ to IEO ↑		250	ns	

Note 2: Interrupt arbitration loop circuit (daisy chain) is not used.

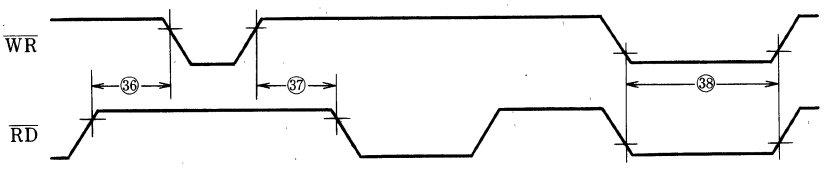


Interrupt acknowledge timing

(3) Reset timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
36	TdRDQ (WR)	Delay time from $\overline{RD}$ ↑ (for suppressing reset) to $\overline{WR}$ ↓	40		ns	
37	TdWRQ (RD)	Delay time from $\overline{WR}$ ↑ (for suppressing reset) to $\overline{RD}$ ↓	50		ns	
38	TwRES	Minimum low width of $\overline{WR}$ and $\overline{RD}$(for resetting)	250		ns	3

Note 3: The internal reset signal lags by 1/2 to 2 clocks behind external reset conditions.

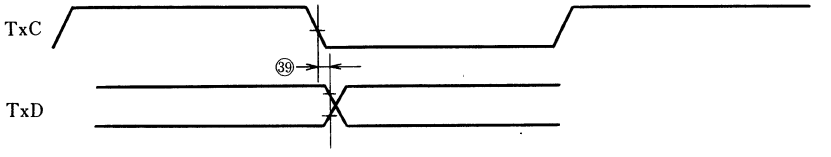


Reset timing

(4) Serial port timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
39	TdTxC(TxD)	Delay time from sending clock transition to output data transition		19000	ns	4

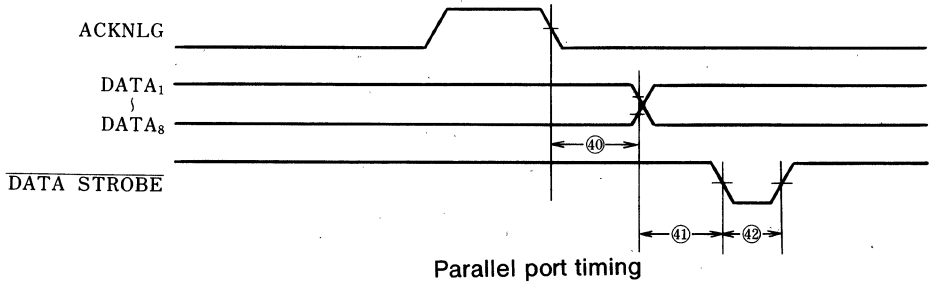
Note 4: Applies to all baud raets (110-9800 B)



Serial port timing

(5) Parallel port timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
40	TdACK (D)	Delay from ACKNLG ↓ to data output	13000	18000	ns	
41	TdD(DSTR)	Delay from data output to $\overline{DATA\ STROBE}$ ↓	6000		ns	
42	TwDSTR	$\overline{DATA\ STROBE}$ pulse width	6000		ns	



Parallel port timing

■ Register

The LH8571 has the following registers which can be accessed externally (from CPU).

- Master interrupt control register (MIC)
- Data indirect register (DIND)
- Data status command registers (DSC0, DSC1, DSC2, DSC3, DSC4, DSC5 and DSC8)

Table 1 Register address

Register	Register address
DSC0	××× 00000
DSC1	××× 00001
DSC2	××× 00010
DSC3	××× 00011
DSC4	××× 00100
DSC5	××× 00101
DSC8	××× 01000
DIND	××× 10101
MIC	××× 11110

Note: A_7–A_1 is decoded and applied to $\overline{CS}$, so that the location in the input/output address space is determined. Bits marked by 'x' are undefined.

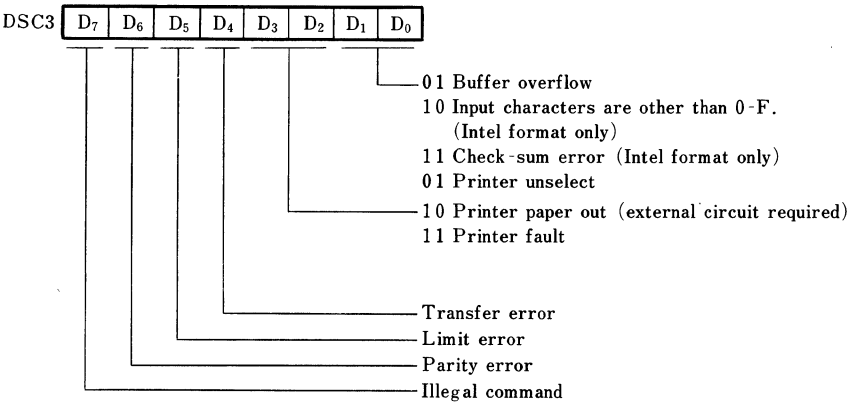


Fig. 1 Error flag (DSC3)

The master interrupt control register (MIC) is used to control the interrupt operation (see Fig. 2). Writing into the MIC register falls into two groups. Group 2 uses the write code shown in Table 2.

Table 2 MIC register write code

Group 2			Group 1		Function
D_7	D_6	D_5	D_2	D_0	
0	0	0	×	×	Writing to D_0 and D_2
0	0	1	0	0	Reset IP (D_5) and IUS (D_6)
0	1	0	0	0	Set IUS (D_6)
0	1	1	0	0	Reset IUS (D_6)
1	0	0	0	0	Set IP (D_5)
1	0	1	0	0	Reset IP (D_5)
1	1	0	0	0	Set IE (D_7)
1	1	1	0	0	Reset IE (D_7)

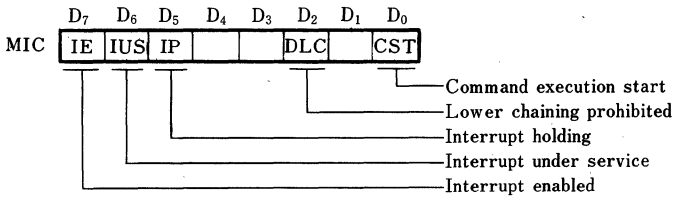


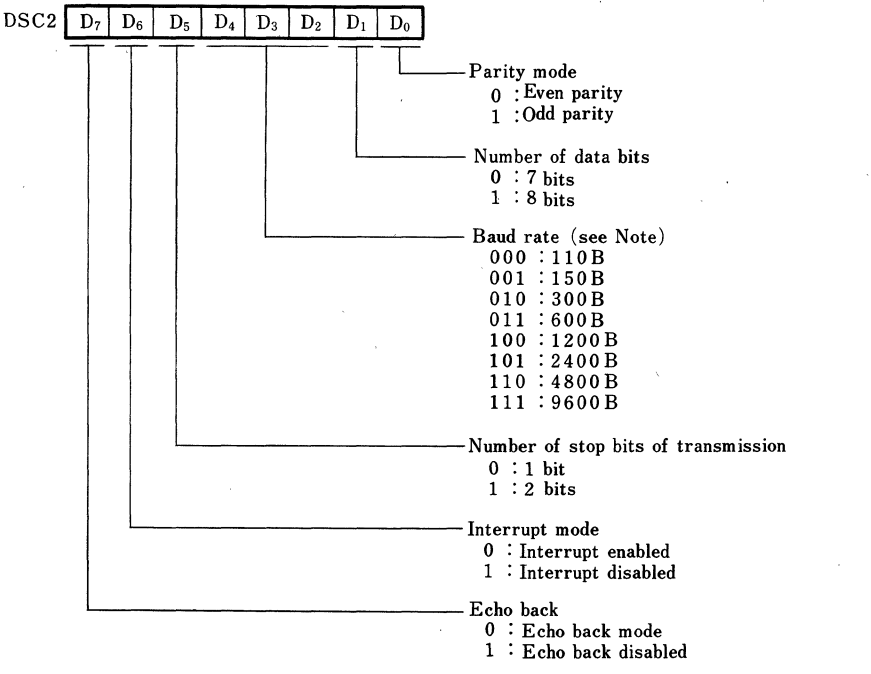
Fig.2 Master interrupt control register

■ Programming

Use the registers, DSC0, DSC1, DSC2, DSC3, DSC4, DSC5, and DSC8, to specify operation mode. The 24 types of commands are made valid by first writing a value corresponding to the desired command number into DSC0, then setting the CST bit on MIC. The registers DSC1, DSC2, DSC4, and DSC5 are used to specify parameters for each command. Command 0 is used inspecifying serial data format using DSC2 (Fig. 3).

The result of command execution is indicated on DSC0 and DSC3. DSC3 indicates error status as shown in Fig. 1. DSC8 is used as a buffer register after command 22 or 23 is executed.

Tables 3 and 4 show command functions versus registers.



Note : The baud rate described above is for PCLK=4.0MHz

Fig. 3 Serial data format (DSC2)

Table 3 Command function and writing register contents

Register / Command	Code	Parameter				Function	Remarks
	DSC0	DSC1	DSC2	DSC4	DSC5		
0	00H		Transfer format and operating mode			Specify transfer format and operating mode.	
1	01H		Stop character			Output serial-input data to Centronics printer until the stop character arrives.	Stop character is specified by DSC2.
2	02H	Number of output bytes				Output serial-input data to Centronics printer.	Operaion stops upon detection of Control C (hex 03).
3	03H	Number of output bytes		Load address (high order byte)	Load address (low order byte)	Output buffer area contents to serial port in Intel format.	Address information of data is appended.
4	04H					Read Intel format data on serial port and store in buffer area.	
5	05H	Number of bytes of block transfer				Initialize block transfer between master CPU and buffer area.	
6	06H	Number of output bytes	Output starting address			Output data in buffer area via serial port.	Operation stops upon detection of Control C (hex 03).
7	07H	Number of output bytes	Output starting address			Output data in buffer area to printer	Operation stops upon detection of Control C (hex 03).
8	08H	Number of output bytes	Output starting address			Convert binary data in buffer area into ASCII and output via serial port.	
9	09H	Number of output bytes	Output starting address	Display address (high order)	Display address (low order)	Convert binary data in buffer area into ASCII and output via serial port.	Address information of data is appended.
10	0AH	Number of output bytes	Output starting address			Convert binary data in buffer area into ASCII, and output to printer.	
11	0BH	Number of output bytes	Output starting address	Display address (high order)	Display address (low order)	Convert binary data in buffer area into ASCII, and output to printer.	Address information of data is appended.
12	0CH	Number of iutput bytes	Nunber of output bytes			Read ASCII data on serial port and store in buffer area.	
13	0DH					Read Intel format data on serial port and store in buffer area.	Used when a reader is connected to serial port.

Register / Command	Code	Parameter				Function	Remarks
	DSC0	DSC1	DSC2	DSC4	DSC5		
14	0EH		Output character			Read ASCII data on serial port until arrival of CR code.	After CR reception, CR and LF codes are sent out via serial port.
15	0FH	Number of output bytes		Load address (low order byte)	Load address (high order byte)	Convert data in buffer area into Intel format, and output via serial port.	Used when a puncher is connected to serial port.
16	10H	Number of input bytes	Output character			Read binary data on serial port into buffer area for storage.	Used when a reader is connected to serial port.
17	11H	Number of output bytes	Output starting address			Output data in buffer area via serial ports.	Used when a puncher is connected to serial port. Opertion stops upon detection of hex 03.
18	12H					Output null codes via serial port.	256 null codes outputted.
19	13H					Output EOF in Intel format (: 00000001FF) via serial port.	
20	14H					Output null codes via serial port.	Used when a puncher is connected to serial port.
21	15H					Output EOF in Intel format (: 00000001FF) via serial port.	Used when a puncher is connected to serial port.
22	16H					Read 1-byte data on serial port.	Data is stored in DSC8.
23	17H					Output data written in DSC8 by CPU via serial port.	Data needs to be set in DSC8 prior to execution.

Table 4 Register contents after command execution (readout register)

Register / Command	Code DSC0 1*	2*	3*	Parameter DSC1	DSC2	DSC3	DSC4	DSC5
0	00	80	C0H			Error status flag		
1	01	81	$C1^{+}_{H}$			Error status flag		
2	02	82	$C2^{+}_{H}$			Error status flag		
3	03	83	C3H			Error status flag		
4	04	84	C4H		Number of bytes input+20H	Error status flag	Load address (high order byte)	Load address (low order byte)
5	05	85	C5H			Error status flag		
6	06	86	C6H			Error status flag		
7	07	87	$C7^{+}_{H}$			Error status flag		
8	08	88	C8H			Error status flag		
9	09	89	C9H			Error status flag		
10	0A	8A	CA^{+}_{H}			Error status flag		
11	0B	8B	CB^{+}_{H}			Error status flag		
12	0C	8C	CCH			Error status flag		
13	0D	8D	CDH		Number of bytes input+20H	Error status flag	Load address (high order byte)	Load address (low order byte)
14	0E	8E	CEH			Error status flag	Number of bytes input+20H	
15	0F	8F	CFH			Error status flag		
16	10	90	D0H			Error status flag		
17	11	91	D1H			Error status flag		
18	12	92	D2H			Error status flag		
19	13	93	D3H			Error status flag		
20	14	94	D4H			Error status flag		
21	15	95	D5H			Error status flag		
22	16	96	D6H			Error status flag		
23	17	97	D7H			Error status flag		

Note 1: 1*: Value before command execution (command code value)
2*: Value upon normal completion of command execution.
3*: Value upon abnormal completion (error) of command execution.
These are common to all commands.

Note 2: For error status flag value, see Fig.1.

Note 3: If $\overline{\text{FAULT}}$ input becomes low (printer error) during command execution, LH8571 suspends operation until $\overline{\text{FAULT}}$ returns to high (error recovery). At this time, DSC0 has bit 6 set and bit 7 reset.

LH8572 Serial Parallel Combination Controller

Description

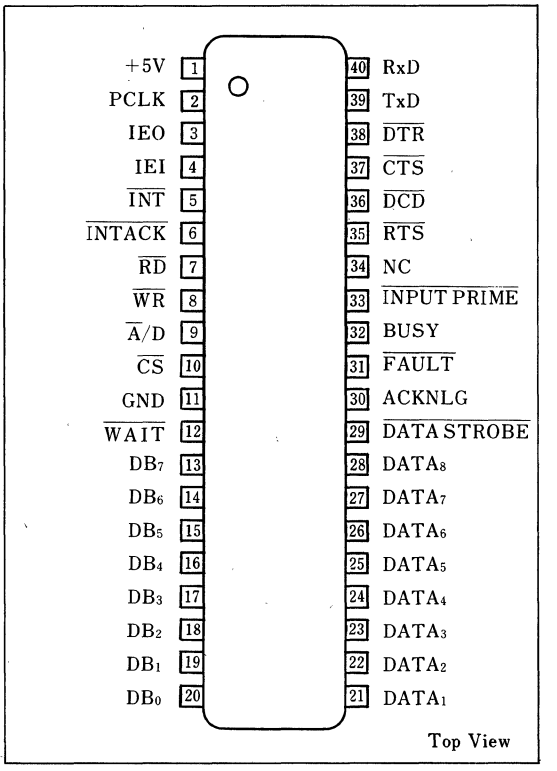
The LH8572 (SPCC72) is a peripheral device for general purpose microcomputer systems to perform asynchronous serial data tansfers and control of Centronics compatible printers.

It supports full duplex asynchronous serial data transfers. The transfer conditions such as the baud rate and character length can be set by the program. Further, it is equipped with a control I/O terminal for simple organization of the various types of modem interfaces. The Receive Buffer has a double buffer structure so that the master CPU can easily perform reading and writing of data.

A printer control I/O terminal is available for easy connection to any printer which is Centronics compatible. A handshake line and control for other I/O lines is supported. A 128-byte printer data buffer memory having an FIFO structure is provided within the LH8572. Efficient use of the printer unit by the master CPU is made possible with this buffer.

In this way, the LH8572 peripheral device for general-purpose microcomputers, was developed to efficiently perform serial data transfer and printer output control within a compact package. It is suitable for use in small systems such as personal computers which use printer units, RS232C terminal units and modem units.

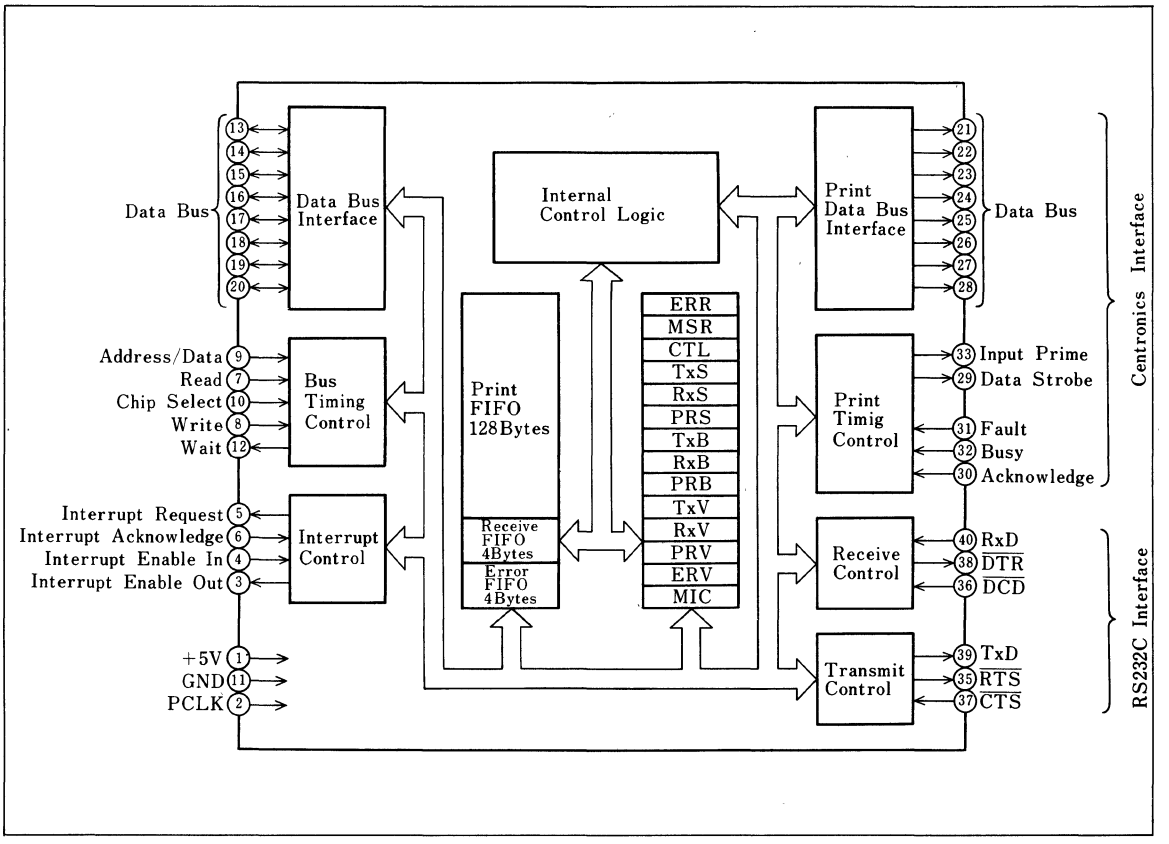
Pin Connections



Features

1. Asynchronous Full Duplex Data Transfer
   - Character length of 5 to 8 bits
   - 1 or 2 stop bits
   - No parity bit or odd/even parity
   - False start bit or rejection (rejects spike noise in the mark line to prevent malfunction.)
   - Full duplex
   - Transmit buffer has double structure.
   - Receive buffer has FIFO structure.
   - Error detection function, Parity error detection, Framing error detection, and Overrun error detection
   - Baud rates: 75, 110, 150, 300, 600, 1200, 2400, 4800 baud selectable
2. Centronics Compatible Printer Control
   - Furnishes printer interface signals compatible with Centronics specifications
   - Built-in handshake function for data output
   - Internal buffer: 128-byte FIFO structure
   - Error detection: Printr fault error/Paper empty error
3. Vector Interrupt
   - Able to generate an interrupt on various conditions such as Transmit Buffer empty, validity of received character, and Printer Output Buffer empty.
   - Interrupt vectors for Transmit, Receive, Printer and Error detection can be set individually.
4. Non-multiplexed bus interface
5. 40-pin dual-in-line package

Block Diagram



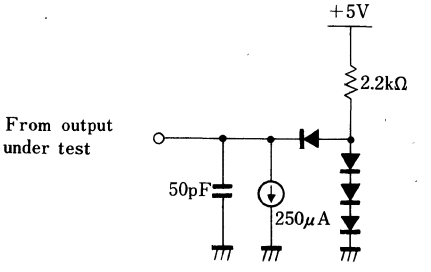
■ Pin Description

Pin	Meaning	I/O	Function
$DB_0 \sim DB_7$	Data bus	Bidirectional 3-state	System data bus
$\overline{A/D}$	Address/data select	I	Address/data select signal
$\overline{RD}$	Read	I	Active low. Indicate the system in read operation.
$\overline{WR}$	Write	I	Active low. Indicate the system in write operation.
$\overline{CS}$	Chip select	I	Active low. Chip selection signal
$\overline{WAIT}$	Wait	O	Active low, open-drain. Used to synchronize with CPU
$\overline{INT}$	Interrupt request	O	Active low, open-drain. Indicate interrupt request to CPU.
$\overline{INTACK}$	Interrupt acknowledge	I	Active low. Indicate interrupt acknowledge cycle.
IEI	Interrupt enable input	I	Active high. Used to form interrupt priority arbitration loop circuit (daisy chain).
IEO	Interrupt enable output	O	Active high. Used to form daisy chain.
$DATA_1 \sim DATA_8$	Output data	O	Output data
$\overline{DATA\ STROBE}$	Data strobe	O	Active low. Indicate settlement of data.
BUSY	Busy	I	Active high. Indicate printer in operation.
ACKNLG	Acknowledge	I	Active high. Acknowledge signal from printer.
$\overline{FAULT}$	Fault	I	Active low. Indicate printer inoperable.
$\overline{INPUT\ PRIME}$	Prime input	O	Active low. Printer initializing signal.
RxD	Receiving data line	I	Receiving data line.
TxD	Transmitted data	O	Transmitting data line
$\overline{RTS}$	Transmission request	O	Active low. Indicate readiness for data transmission.
$\overline{CTS}$	Transmission enable	I	Active low. Indicate data transmission is possible.
$\overline{DTR}$	Data terminal ready	O	Active low. Data transmission request signal.
$\overline{DCD}$	Reception enable	I	Active low. Indicate data reception is possible.
PCLK	Clock	I	Single-phase clock, need not be same as CPU clock.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage*	V_{IN}	−0.3∼+7	V
Output voltage*	V_{OUT}	−0.3∼+7	V
Operating temperature	T_{opr}	0∼+70	℃
Storage temperature	T_{stg}	−65∼+150	℃

* The maximum applicable voltage on any pin with respect to GND.



Standard test load

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

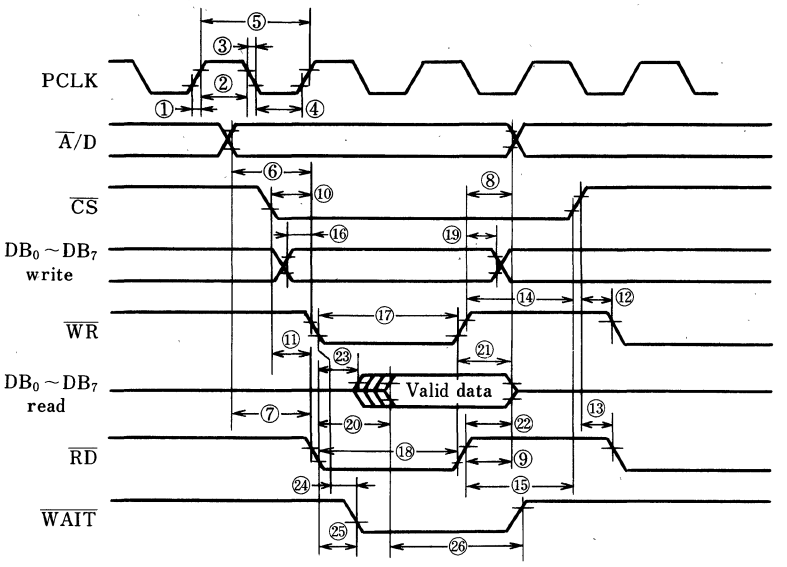
Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Clock input high voltage	V_{CH}		2.4	V_{CC}	V	
Clock input low voltage	V_{CL}		−0.3	0.8	V	
Input high voltage	V_{IH}		2	V_{CC}	V	
Input low voltage	V_{IL}		−0.3	0.8	V	
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4		V	
Output low voltage	V_{OL}	I_{OL}=2mA		0.4	V	
Input leakage current	$\lvert I_{IL} \rvert$	0≦V_{IN}≦5.25V		10	μA	
Output leakage current	$\lvert I_{OL} \rvert$	0≦V_{IN}≦5.25V		10	μA	
Current consumption	I_{CC}			250	mA	

■ AC Characteristics

(1) CPU interface timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TrC	Clock rise time		20	ns	
2	TwCh	Clock pulse width, high	105		ns	
3	TfC	Clock fall time		20	ns	
4	TwCl	Clock pulse width, low	105		ns	
5	TpC	Clock period	250		ns	
6	TsA/D(WR)	A/$\overline{D}$ setup time to $\overline{WR}$ ↑	80		ns	
7	TsA/D(RD)	A/$\overline{D}$ setup time to $\overline{RD}$ ↓	80		ns	
8	ThA/D(WR)	A/$\overline{D}$ hold time from $\overline{WR}$ ↑	30		ns	
9	ThA/D(RD)	A/$\overline{D}$ hold time from $\overline{RD}$ ↑	30		ns	
10	TsCSf(WR)	$\overline{CS}$ low setup time to $\overline{WR}$ ↓	0		ns	
11	TsCSf(RD)	$\overline{CS}$ low setup time to $\overline{RD}$ ↓	0		ns	
12	TsCSr(WR)	$\overline{CS}$ high setup time to $\overline{WR}$ ↓	60		ns	
13	TsCSr(RD)	$\overline{CS}$ high setup time to $\overline{RD}$ ↓	60		ns	
14	ThCS(WR)	$\overline{CS}$ low hold time from $\overline{WR}$ ↑	0		ns	
15	ThCS(RD)	$\overline{CS}$ low hold time from $\overline{RD}$ ↑	0		ns	
16	TsDI(WR)	Data setup time to $\overline{WR}$ ↓	0		ns	
17	Tw(WR)	$\overline{WR}$ pulse width	390		ns	
18	Tw(RD)	$\overline{RD}$ pulse width	390		ns	
19	ThWR(DI)	Data input from $\overline{WR}$ ↑	0		ns	
20	TdRD(DI)	Delay time from $\overline{RD}$ ↓ to valid data			ns	1
21	ThRD(DI)	Data hold time from $\overline{RD}$ ↑	0		ns	
22	TdRD(DIz)	Delay time from $\overline{RD}$ ↑ to data bus floating		70	ns	
23	TdRD(DB_A)	Delay time from $\overline{RD}$ ↓ to readout data settlement	0		ns	
24	TdWR(W)	Delay time from $\overline{WR}$ ↓ to $\overline{WAIT}$ ↓		150	ns	
25	TdRD(W)	Delay time from $\overline{RD}$ ↓ to $\overline{WAIT}$ ↓		150	ns	
26	TdDI(W)	Delay time from valid data to $\overline{WAIT}$ ↑	0		ns	

All AC output characteristics are based on the stated load conditions.
Note 1: The delay time depends on the device status at the time of access by CPU.

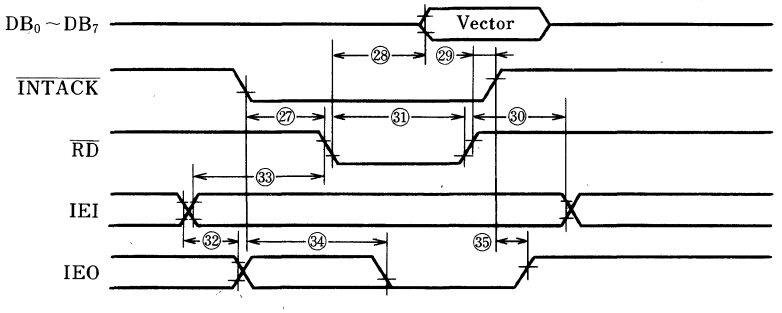


CPU interface timing

(2) Interrupt acknowledge timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
27	TsACK(RD)	$\overline{INTACK}$ low setup time to $\overline{RD}$	90		ns	2
28	TdRD(DI)	Delay time from $\overline{RD}$ ↓ to valid vector		255	ns	
29	ThRD(ACK)	$\overline{INTACK}$ low hold time from $\overline{RD}$ ↑	0		ns	
30	ThIEI(RD)	IEI hold time from $\overline{RD}$ ↑	100		ns	
31	TwRDI	$\overline{RD}$(acknowledge) low pulse width	255		ns	
32	TdIEI(IEO)	Delay time from IEI to IEO		120	ns	
33	TsIEI(RD)	IEI setup time to $\overline{RD}$ ↓	150		ns	
34	TdACK(IEO)	Delay time from $\overline{INTACK}$ ↓ to IEO ↓		250	ns	
35	TdADKr(IEO)	Delay time from $\overline{INTACK}$ ↑ to IEO ↑		250	ns	

Note 2: Interrupt arbitration loop circuit (daisy chain) is not used.

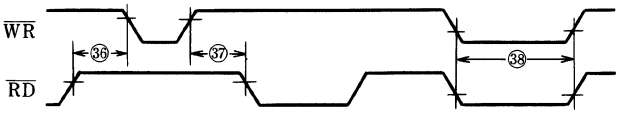


Interrupt acknowledge timing

(3) Reset timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
36	TdRDQ(WR)	Delay time from $\overline{RD}$ ↑ (for suppressing reset) to $\overline{WR}$ ↓	40		ns	
37	TdWRQ(RD)	Delay time from $\overline{WR}$ ↑ (for suppressing reset) to $\overline{RD}$ ↓	50		ns	
38	TwRES	Minimum low width of $\overline{WR}$ and $\overline{RD}$ (for resetting)	250		ns	3

Note 3: The internal reset signal lags by 1/2 to 2 clocks behind external reset conditions.

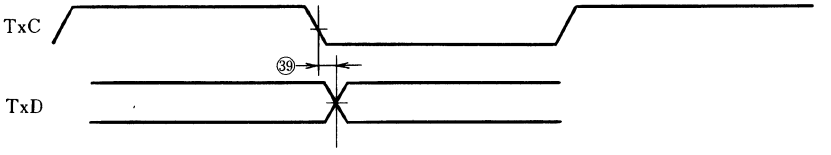


Reset timing

(4) Serial port timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
39	TdTxC(TxD)	Delay time from sending clock transition to output data transition		35000	ns	4

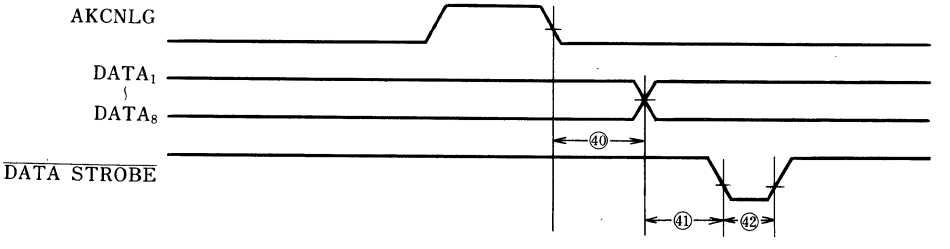
Note 4: Applies to all baud rates (75 -4800 B)



Serial port timing

(5) Parallel port timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
40	TdACK(D)	Time from ACKNLG ↓ to data output	24000		ns	
41	TdD(DSTR)	Time from data output to $\overline{DATA\ STROBE}$ ↓	6500		ns	
42	TwDSTR	$\overline{DATA\ STROBE}$ pulse width	6500		ns	



Parallel port timing

■ Registers

The LH8572 has 14 registers which can be accessed externally (from CPU), and their addresses are listed in Table 1. To make access to these registers, the high order 7 bits of I/O address (A_7-A_1) are decoded and fed to $\overline{CS}$ and the lowest order bit (A_0) is connected to A/D. This connection permits the assignment of 2-byte port addresses (even address and odd address) to the LH8572.

Table 1 Register address

Address	Register
×××00000	Error status register (ERR)
×××00001	Mode setting register (MSR)
×××00010	Control register (CTL)
×××00011	Transmission status register (TxS)
×××00100	Reception status register (RxS)
×××00101	Printer status register (PRS)
×××00110	Transmission buffer (TxB)
×××00111	Reception buffer (RxB)
×××01000	Printer buffer (PRB)
×××01001	Transmission interrupt vector register (TxV)
×××01010	Reception interrupt vector register (RxV)
×××01011	Printer interrupt vector register (PRV)
×××01100	Error interrupt vector register (ERV)
×××11110	Master interrupt control register (MIC)

Note: A_7-A_1 is decoded and applied to $\overline{CS}$, so that the location in the input/output address space is determined. Bits marked by 'x' are undefined.

■ Programming

The LH8572 has 14 read/write registers which can be accessed directly by the master CPU.

(1) Initialization

The device is initialized in accordance with the following procedure.

(1) Following power-on reset, or master reset by software, set the mode register is programmed for character format, baud rate, stop bit and parity mode. Subsequently data required by control register*, master interrupt control register* and interrupt vector registers* (transmission, reception and printer error interrupt vector registers) is programmed.

(2) Clear the error status register.

(3) Wait until the data transfer enable bit in the master interrupt control register is set to "1", making the LH8572 operable.

In case interrupt is used, the above polling operation is unnecessary. When transmission, reception and printer output become enabled, interrupt request is forwarded to the master CPU, indicating that the LH8572 has become operable.

Note: Registers marked by '*' can be set or revised even during the operation of LH8572.

(2) Data input/output

Date transfer between LH8572 and master CPU is carried out in accordance with the following procedure.

(1) Poll the status registers (transmission, reception and printer status registers) and wait until they become "1". In case interrupt (transmission, reception and printer interrupt) is used, interrupt occurs as soon as the value of each status register becomes "1", and polling is not necessary.

(2) After the status register has been set to "1" (or after interrupt has occurred), begin data transfer via the buffers (transmission, reception and printer buffers).

(3) Clear the status register. If the above operation is implemented using an interrupt routine, the interrupt-under-service (IUS) bit must be reset immediately before the end of each interrupt routine.

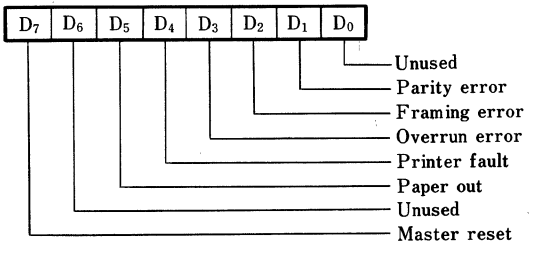


Fig. 1 Error status register (ERR)

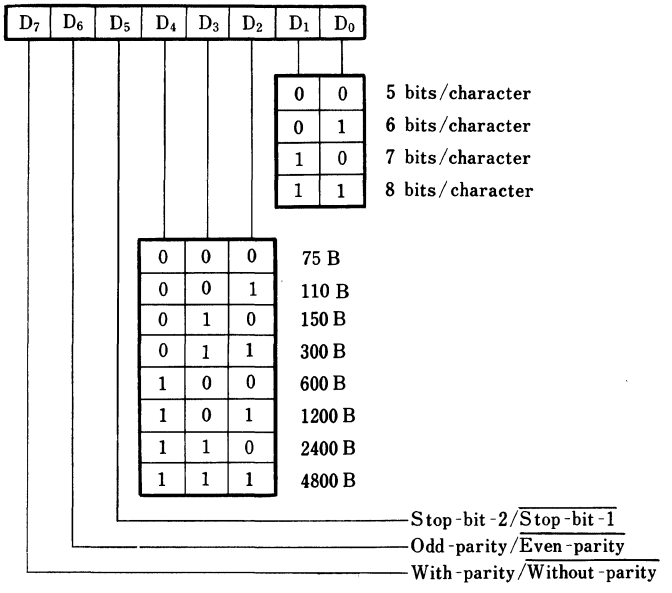


Fig. 2 Mode setting register (MSR)

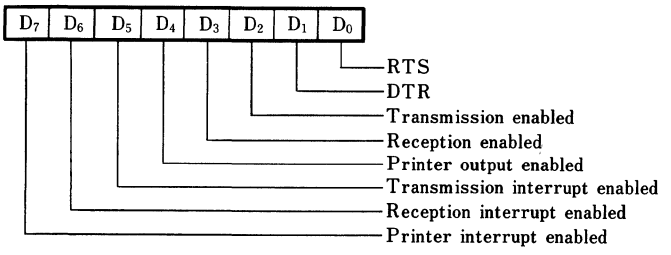
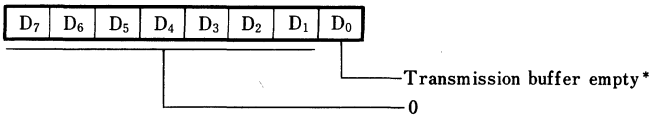
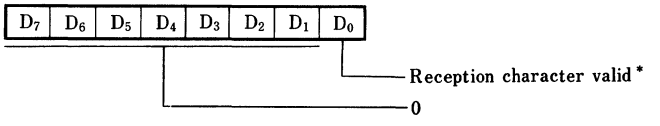


Fig. 3 Control register (CTL)



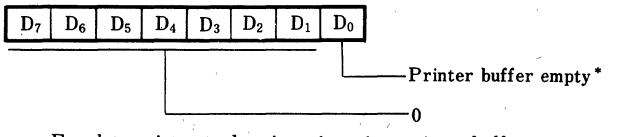
* For data transmission, data is written into transmission buffer upon confirmation that transmission buffer "vacancy" bit is "1", and thereafter that bit is set to "0"

Fig. 4 Transmission status register (TxS)



* For data reception, data is readout from reception buffer upon confirmation that the reception character "validity" bit is "1", and thereafter that bit is set to "0"

Fig. 5 Reception status register (RxS)



* For data print out, data is written into printer buffer upon confirmation that the printer buffer "vacancy" bit is "1", and thereafter that bit is set to "0"

Fig. 6 Printer status register (PRS)

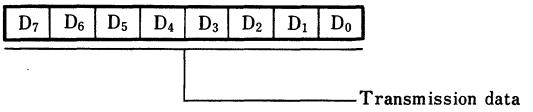


Fig. 7 Transmission buffer (TxB)

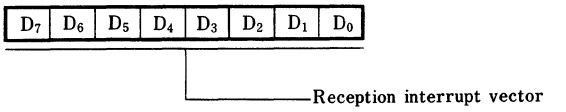


Fig. 11 Reception interrupt vector register (RxV)

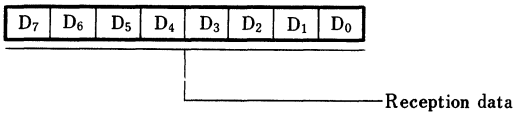


Fig. 8 Reception buffer (RxB)

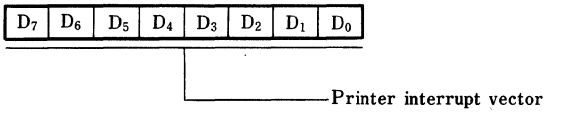


Fig. 12 Printer interrupt vector register (PRV)

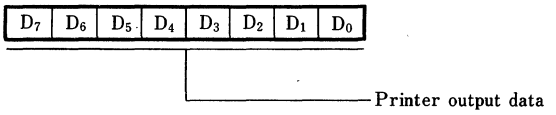


Fig. 9 Printer buffer (PRB)

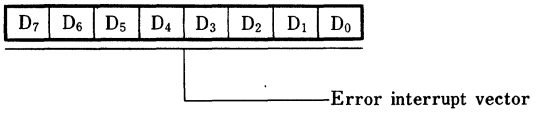


Fig. 13 Error interrupt vector register (ERV)

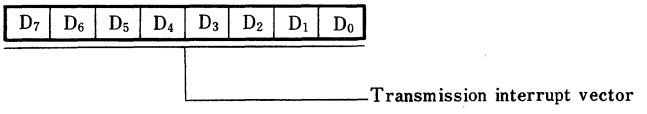
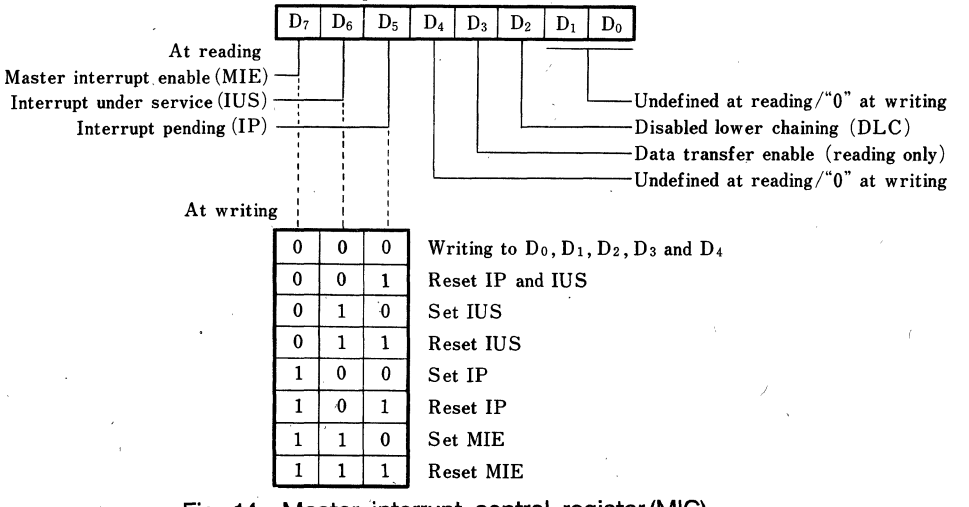


Fig. 10 Transmission interrupt vector register (TxV)



0	0	0	Writing to D_0, D_1, D_2, D_3 and D_4
0	0	1	Reset IP and IUS
0	1	0	Set IUS
0	1	1	Reset IUS
1	0	0	Set IP
1	0	1	Reset IP
1	1	0	Set MIE
1	1	1	Reset MIE

Fig. 14 Master interrupt control register (MIC)

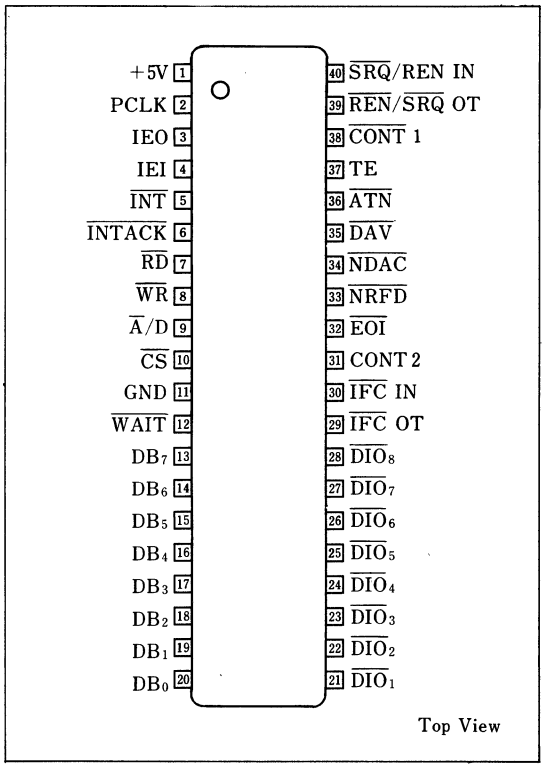
LH8573 General Purpose Interface Bus Controller

■ Description

The LH 8573 (GPIB73) is a microcomputer peripheral device used to control interface buses conforming to IEEE Std. 488-1978* (will be termed simply "GPIB"). The GPIB is extensively used as a linkage bus between data gathering instrumentation devices and a microcomputer system.
The LH8573 incorporates three functions of talker, listener and controller, all integrated in one chip. Using this device, the GPIB interface can be provided for various instrumentation equipment, personal computers and office computers.

*Note : The standard disclosed in IEEE Std. 488-1978 "IEEE Standard Digital Interface for Programmable Instrumentation "issued by IEEE, U.S.A.

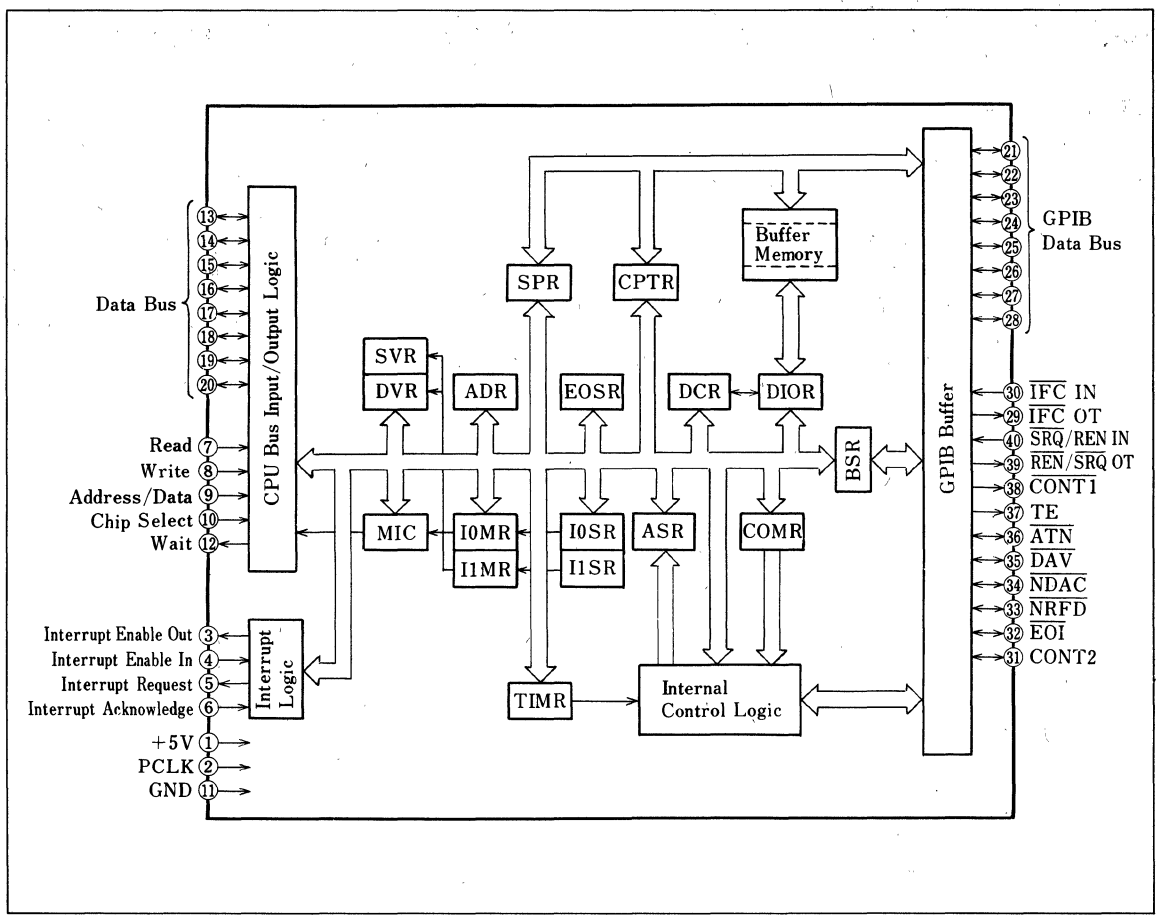
■ Pin Connections



■ Features

1. Built-in talker, listener and controller. Talker function, listener function and controller function are integrated in one chip.
2. Built-in buffer memory. Talker or listener can use 160-byte on-chip buffer.
3. EOI automatic transmission. Upon detection of the last byte of or EOS in talker mode, EOI signal is transmitted automatically.
4. EOS automatic detection. Upon reception of EOS in listener mode, the CPU is informed.
5. Built-in timer. The bus time-out period for handshaking can be set by the on-chip timer in the range of 200 μs to 12ms at 50 μs interval.
6. Interrupt function. Interrupt arbitration facility of daisy-chain type is provided, allowing vectored interrupt to CPU.
7. 40-pin dual-in-line package
8. Single+5V power supply

Block Diagram



LH8575 Multitask Support Processor

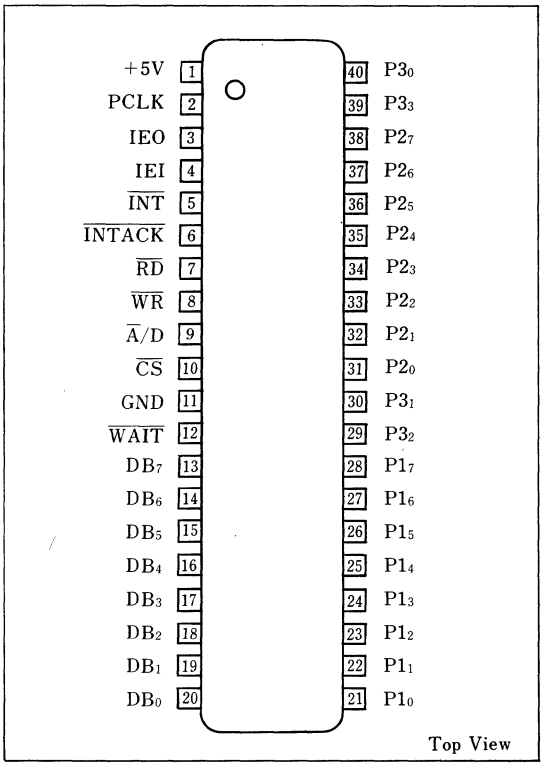
■ Description

The LH8575 is the stand alone type multitask support processor providing the multitask capabilities for any simple microcomputer system.

The concept of this multitask processing is similar to a conventional real time OS (operating system). The devices perform task management (creating, deleting, etc.) independently of the master CPU, and carry out multitask processing for systems bus with arbitrary CPU architectures merely by connecting to the system bus.

User's programs are scheduled on a priority or time sliced basis. Tasks are switched by an interrupt caused by the LH8575, and commands are given to the LH8575 by writing parameters and command numbers in the specified register in the LH8575.

■ Pin Connections

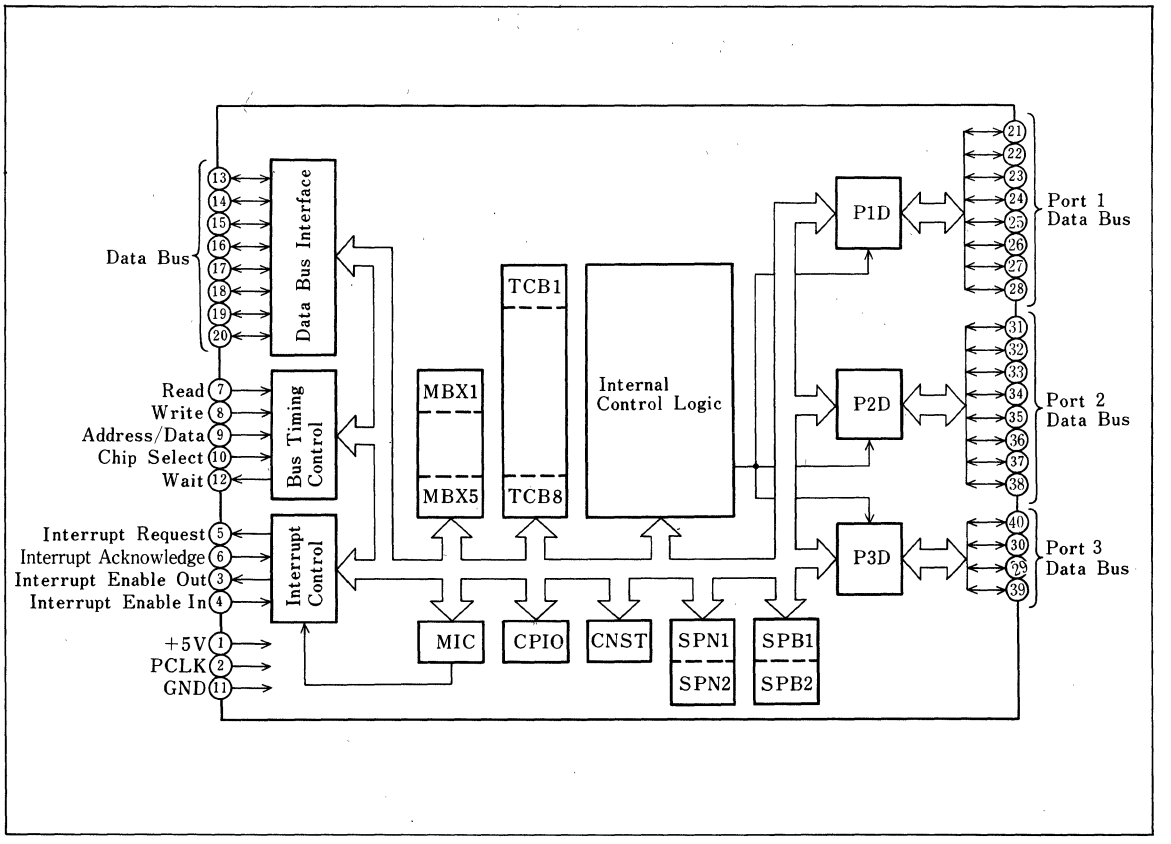


■ Features

1. Matching with any CPU
   - The LH8575 operates only in response to commands which are issued by the main CPU. The system may have any type of CPU provided it is responsive to interrupt access by the LH8575.
2. Task management
   - Up to eight tasks can be controlled concurrently. By using the task creating and deleting technique, a maximum of 255 tasks can be handled.
   - Tasks can be controlled on a priority basis by the assignment of 255 priority levels.
3. Inter-task communication
   - Inter-task communication is possible using the "mail box" provided within the LH8575.
   - Inter-task synchronization is possible using the "mail box."
4. Built-in timer
   - Timers with ranges from 10 ms to 255 hours can be used for time-sliced processes and checking I/O wait time.
   - These timers can be set independently for each task.
5. Built-in clock.
   - Time (hours, minutes and seconds) can be set and read out.
6. 20-bit general-purpose I/O port
   - Two 8-bit ports operable in bit input/output
   - 2-bit input ports and 2-bit output ports
   - Tasks can be resumed using the 2-bit input ports.
7. Memory assignment.
   - Working memory areas can be assigned to each task.

6

■ Block Diagram

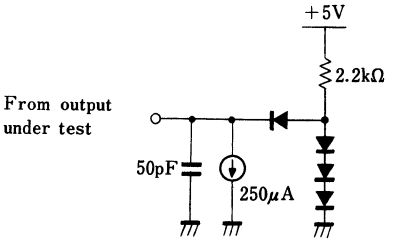


Pin Description

Pin	Meaning	I/O	Function
DB_0~DB_7	Data bus	Bidirectional 3-sate	System data bus
$\overline{A/D}$	Address/data select	I	Address/data select signal
$\overline{RD}$	Read	I	Active low. Indicate the system in read operation.
$\overline{WR}$	Write	I	Active low. Indicate the system in write operation.
$\overline{CS}$	Chip select	I	Active low. Chip selection signal
$\overline{WAIT}$	Wait	O	Active low, open-drain. Used to synchronize with CPU.
$\overline{INT}$	Interrupt request	O	Active low, open-drain. Indicate interrupt request to CPU.
$\overline{INTACK}$	Interrupt acknowledge	I	Active low. Indicate interrupt acknowledge cycle.
IEI	Interrupt enable input	I	Active high. Used to form interrupt priority arbitration loop circuit (daisy-chain).
IEO	Interrupt enable output	O	Active high. Used to form daisy chain.
$P1_0$~$P1_7$	I/O port lines	I/O	Parallel I/O
$P2_0$~$P2_7$	I/O port lines	I/O	Parallel I/O
$P3_0$~$P3_3$	I/O port lines	I/O	Parallel I/O
PCLK	Clock	I	Single-phase clock, need not be same as CPU clock.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3~+7.0	V
Output voltage	V_{OUT}	−0.3~+7.0	V
Operating temperature	T_{opr}	0~+70	°C
Storage temperatuer	T_{stg}	−65~+150	°C



Standard test load

DC Characteristics

(V_{CC}=5V±5%, Ta=0~+70℃)

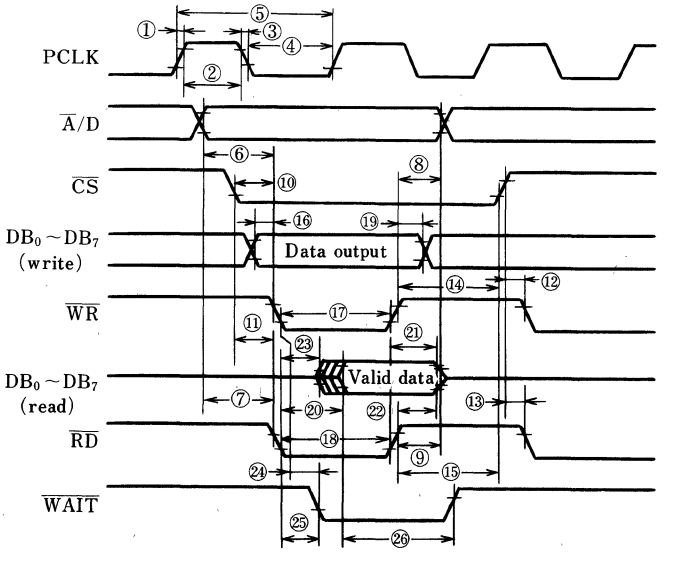
Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Clock input high voltage	V_{CH}		2.4	V_{CC}	V	
Clock input low voltage	V_{CL}		−0.3	0.8	V	
Input high voltage	V_{IH}		2.0	V_{CC}	V	
Input low voltage	V_{IL}		−0.3	0.8	V	
Output high voltage	V_{OH}	I_{OH} = −250 μA	2.4		V	
Output low voltage	V_{OL}	I_{OL} = 2mA		0.4	V	
Input leakage current	$\lvert I_{IL} \rvert$	0 ≦ V_{IN} ≦ +5.25V		10	μA	
Output leakage current	$\lvert I_{OL} \rvert$	0 ≦ V_{IN} ≦ +5.25V		10	μA	
Current consumption	I_{CC}			250	mA	

■ AC Characteristics

(1) Master CPU interface timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TrC	Clock rise time		20	ns	
2	TwCh	Clock pulse width, high	105		ns	
3	TfC	Clock fall time		20	ns	
4	TwCl	Clock pulse width, low	105		ns	
5	TpC	Clock period	250		ns	
6	TsA/D(WR)	$\overline{A}$/D setup time to $\overline{WR}\downarrow$	80		ns	
7	TsA/D(RD)	$\overline{A}$/D setup time to $\overline{RD}\downarrow$	80		ns	
8	ThA/D(WR)	$\overline{A}$/D hold time from $\overline{WR}\uparrow$	30		ns	
9	ThA/D(RD)	$\overline{A}$/D hold time from $\overline{RD}\uparrow$	30		ns	
10	TsCSf(WR)	$\overline{CS}$ low setup time to $\overline{WR}\downarrow$	0		ns	
11	TsCSf(RD)	$\overline{CS}$ low setup time to $\overline{RD}\downarrow$	0		ns	
12	TaCSr(WR)	$\overline{CS}$ high setup time to $\overline{WR}\downarrow$	60		ns	
13	TsCSr(RD)	$\overline{CS}$ high setup time to $\overline{RD}\downarrow$	60		ns	
14	ThCS(WR)	$\overline{CS}$ low hold time from $\overline{WR}\uparrow$	0		ns	
15	ThCS(RD)	$\overline{CS}$ low hold time from $\overline{RD}\uparrow$	0		ns	
16	TsDI(WR)	Data setup time to $\overline{WR}\downarrow$	0		ns	
17	Tw(WR)	$\overline{WR}$ pulse width	390		ns	
18	Tw(RD)	$\overline{RD}$ pulse width	390		ns	
19	ThWR(DI)	Written data hold time from $\overline{WR}\uparrow$	0		ns	
20	TdRD(DI)	Delay time from $\overline{RD}\downarrow$ to valid data			ns	1
21	ThRD(DI)	Readout data hold time from $\overline{RD}\uparrow$	0		ns	
22	TdRD(DIz)	Delay time from $\overline{RD}\uparrow$ to data bus floating		70	ns	
23	TdRD(DB_A)	Delay time from $\overline{RD}\downarrow$ to readout data valid	0		ns	
24	TdWR(W)	Delay time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$		150	ns	
25	TdRD(W)	Delay time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$		150	ns	
26	TdDI(W)	Delay time from valid data to $\overline{WAIT}\uparrow$	0		ns	

Note 1: The delay time depends on device status at the time of access by master CPU.

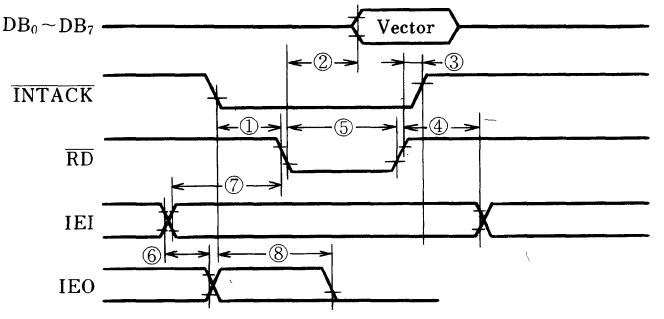


Master CPU interface timing

(2) Interrupt acknowledge timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TsACK(RD)	$\overline{INTACK}$ low setup time to $\overline{RD}$ ↓	90		ns	1
2	TdRD(DI)	Delay time from $\overline{RD}$ ↓ to valid vector		255	ns	
3	ThRD(ACK)	$\overline{INTACK}$ low hold time from $\overline{RD}$ ↑	0		ns	
4	ThIEI(RD)	IEI hold time from $\overline{RD}$ ↑	100		ns	
5	IwRDI	$\overline{RD}$ (acknowledge) pulse width	255		ns	
6	TdIEI(IEO)	Delay time from IEI to IEO		120	ns	
7	TsIEI(RD)	IEI setup time to $\overline{RD}$ ↓	150		ns	
8	TdACKf(IEO)	Delay time from $\overline{INTACK}$ ↓ to IEO ↓		250	ns	

Note 1: Interrupt arbitration loop circuit (daisy-chain) is not used.

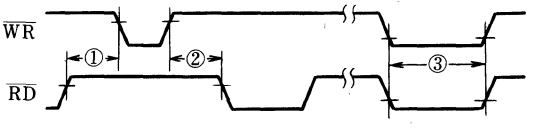


Interrupt acknowledge timing

(3) Reset timing

No.	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TdRDQ(WR)	Delay time from $\overline{RD}$ ↑ (for suppressing reset) to $\overline{WR}$ ↓	40		ns	
2	TdWRQ(RD)	Delay time from $\overline{WR}$ ↑ (for sppressing reset) to $\overline{RD}$ ↓	50		ns	
3	TwRES	Minimum low width of $\overline{WR}$ and $\overline{RD}$ (for resetting)	250		ns	1

Note 1: The internal reset signal lags by 1/2 to 2 clocks behind external reset conditions.

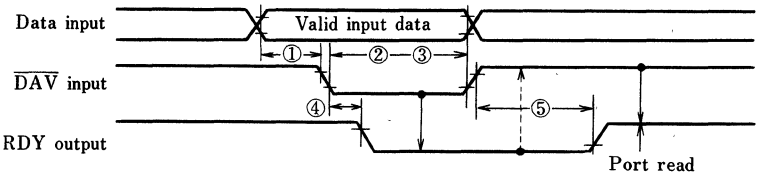


Reset timing

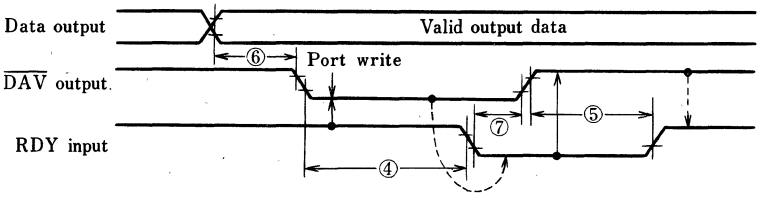
(4) Handshaking timing

No	Symbol	Parameter	MIN.	MAX.	Unit	Note
1	TsDI(DA)	Data setup time	0		ns	
2	ThDA(DI)	Data hold time	230		ns	
3	TwDA	$\overline{DAV}$ width	175		ns	1
4	TdDAL(RY)	Delay time from $\overline{DAV}$ low to RDY	20 0	175	ns	1 2
5	TdDAH(RY)	Delay time from $\overline{DAV}$ high to RDY	 0	150	ns	1 2
6	TdDO(DA)	Delay time from data output to $\overline{DAV}$	50		ns	
7	TdRY(DA)	Delay time from RDY to $\overline{DAV}$	0	205	ns	

Note 1: Input handshaking
Note 2: Output handshaking



Input handshaking timing



Output handshaking timing

■ Registers

(1) Task control

CPIO (Command parameter register)

This register writes the writing perameter previnus to command writing. The readout parameter is placed in CPIO upon completion of command execution.

CNST (Command/status register)

This register is used to write a command. Execution information of executed command is placed in CNST upon completion of command execution.

SPN1, SPN2 (New task stack pointer registers)

At occurrence of interrupt for task switching, execution starting address information for the new task is placed in this register.

SPB1, SPB2 (Old task stack pointer registers)

At occurrence of interrupt for task switching, execution for the executed task is written register.

MIC (Master CPU interrupt control register)

Interrpt related parameters including interrupt enable (IE), interrupt pending (IP) and interrupt-under-service (IUS) bits are set or reset in this register.

Table 1 Register address

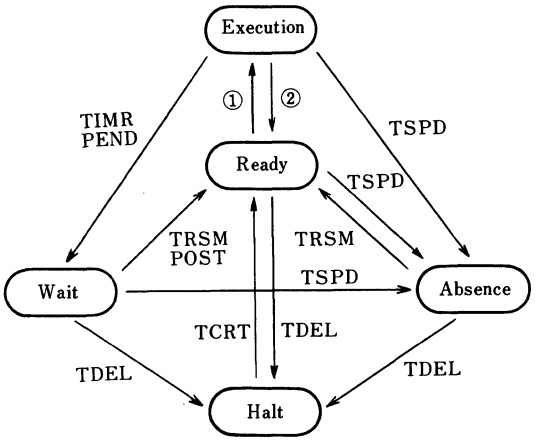
Register	Address
P1D	×××00001
P2D	×××00010
P3D	×××00011
CNST	×××00110
SPN1	×××00111
SPN2	×××01000
SPB1	×××01001
SPB2	×××01010
CPIO	×××10101
MIC	×××11110

Note 1: Bits marked by 'x' may be either '0' or '1'.
Note 2: LH8575 uses 2 input/output address locations.

(2) I/O Ports

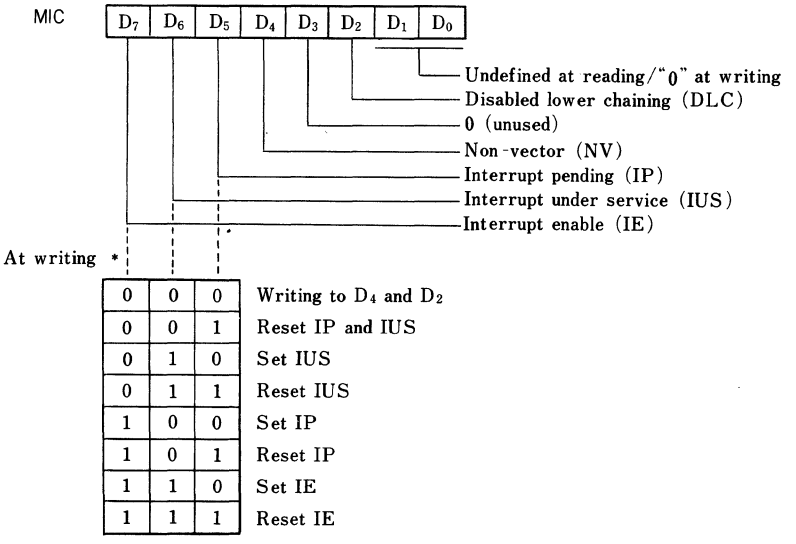
P1D, P2D, P3D (Port 1, 2, 3 data registers)

These registers are used to transact data via port 1, port 2 and port 3.
Table 1 lists the register addresses.



(1) Task in execution releases CPU.
(2)
- Higher ranking task becomes ready.
- Time-up by time division
- TNXT

Fig. 1 Task status



0	0	0	Writing to D_4 and D_2
0	0	1	Reset IP and IUS
0	1	0	Set IUS
0	1	1	Reset IUS
1	0	0	Set IP
1	0	1	Reset IP
1	1	0	Set IE
1	1	1	Reset IE

Note: IP, IUS and IE bits are set or reset by writing in these codes.

Fig. 2 MIC bit configuration

■ Programming

(1) Initialization

The following describes the task control procedure using LH8575.

(1) The LH8575 causes interrupt for task switching. However, in order to process, a separate interrupt processing routine must be prepared.
(2) Each task is provided with a stack area. Task starting address and initial values for all registers are written at the top of each stack area.
(3) LH8575 is initialized. Table 2 lists the initialization information to written in LH8575.
(4) When necessary, the clock is set and the port mode is specified.
(5) Initialization completed. To transfer control from the initialization routine to a task, the task execution command (TSTR) must be executed.

Table 2 System information registered at initialization

Order	Item	Contents	
1	Vector	LH8575 Interrupt vector for task switching	
2	RAM table	User RAM start address (high order byte)	
3		User RAM end address (high order byte)	
4	Task table	Task 1	Task number (hex 01-FF)
5			Priority level (hex 01-FF)
6			Task stack pointer (high order or low order byte)
7			Task stack pointer (low order or high order byte)
⋮		⋮	⋮
4n		Task n	Task number (hex 01-FF)
4n+1			Priority leave (hex 01-FF)
4n+2			Task stack pointer (high order or low order byte)
4n+3			Task stack pointer (low order or high order byte)

(2) Command execution

Table 3 lists the commands of LH8575, and Table 4 lists the command execution information.
In writing command into LH8575 the following data entry procedure applies.

(1) Write parameters needed in writing command into CPIO in the order shown in Table 3. Commands with blank parameter field in Table 3 do not require writing.
(2) Write the command number in CNST.
(3) It is necessary to confirm the completion of command execution by polling D_7 in CNST (D_7 becomes "1" upon completion of command execution). For commands without readout parameter, procedure is completed and the following procedures are unnecessary. Commands with readout parameter (CGET, MALC and PEND) further require the following procedures.
(4) When $D_6 = 1$ in CNST (indicating the readout parameter is prepared in CPIO), parameter is read out from CPIO.
(5) The PRME command must be executed to notify parameter readout completion.
(6) Wait until CNST D_7 becomes "1" to confirm the completion of command execution.

Table 3 Command table

Code	Command name	Function	Writing parameter	Readout parameter	Remarks
00_H	INIT	LH8575 initialization	1. Total number of tasks		
01_H	TSTR	Termination of LH8575 initialization and start of task execution			
02_H	TCRT	Task creation	1. Task number 2. Priority level 3. SP (high order or low order byte) 4. SP (low order or high order byte)		
03_H	TDEL	Task deletion	Task number		
04_H	TRSM	Task resumption	Task number		
05_H	TSPD	Task suspension	1. Task number 2. Control switch		[1]
06_H	TPRI	Task priority change	1. Task number 2. New priority		
07_H	TSLI	Task time-slicing process	1. Priority 2. Time base 3. Count		[2]
08_H	TNXT	Transfer execution right to the next task in time-sliced process.			
09_H	TIMR	Timer setting	1. Control code 2. Count		[3]
$0A_H$	CSET	Clock setting	1. Hour 2. Minute 3. Second		*
$0B_H$	CGET	Clock read out		1. Hour 2. Minute 3. Second	
$0C_H$	MALC	Memory allocation	1. Number of memory blocks required	1. Allocated memory address	*
$0D_H$	MREL	Memory release			
$0E_H$	POST	Message transmission	1. Mail box number 2. Message data 1 3. Message data 2 4. Message data 3 5. Message data 4		[4]
$0F_H$	PEND	Message reception	1. Mail box number	1. Message data 1 2. Message data 2 3. Message data 3 4. Message data 4	*
10_H	PMOD	Port mode setting	1. Port-1 made 2. Port-2 mode 3. port-3 mode		[5]
11_H	PRME	End of parameter readout			

Note 1: Commands marked by "*" require PRME command execution at parameter readout completion.
Note 2: Numerals give in 'writing parameter' and 'readout parameter' indicate the order of writing and reading.
Note 3: Numerals in 'remarks' indicate the reference number of supplementary explanation.

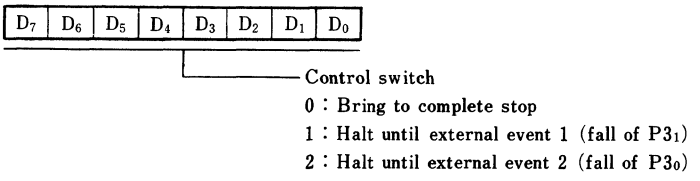
Table 4 Command execution information

Code	Command name	Execution information
00_H	INIT	0 Normal termination 1 Task number or priority setting error 2 Double specification of same task number 3 Total number of tasks equal to 0 or larger than 8; error in the number of system configuration information; RAM table error
01_H	TSTR	0 Nomal termination 3 Initial information not yet set
02_H	TCRT	0 Normal termination 1 Task number or priority setting error 2 Already created 3 Control tasks more than 8
03_H	TDEL	0 Normal termination 1 Task number error 2 Specified task not yet created 4 Specify self
04_H	TRSM	0 Normal termination 1 Task number error 2 Specified task not yet created 4 Specify self 5 Specification of task in ready status
05_H	TSPD	0 Normal termination 1 Task number or control switch number error 2 Specified task not yet created 3 Control switch setting error 5 Specification of task in halt status
06_H	TPRI	0 Normal termination 1 Task number or priority setting error 2 Specified task not yet created
07_H	TSLI	0 Normal termination 1 Priority error or data error 5 Cancellation without setting
08_H	TNXT	0 Normal termination
09_H	TIMR	0 Normal termination 1 Data error 5 Cancellation without setting 8 Resuming by TRSM
$0A_H$	CSET	0 Normal termination 1 Data error
$0B_H$	CGET	0 Normal termination
$0C_H$	MALC	0 Normal termination 6 Allocation disabled
$0D_H$	MREL	0 Normal termination 5 Memory not yet allocated
$0E_H$	POST	0 Normal termination 1 Mail box number error or massage data error 7 Mail box busy
$0F_H$	PEND	0 Normal termination 1 Mail box number error 8 TRSM command issued by other task or time out
10_H	PMOD	0 Normal termination
11_H	PRME	0 Normal termination

■ Supplement for Writing Parameter

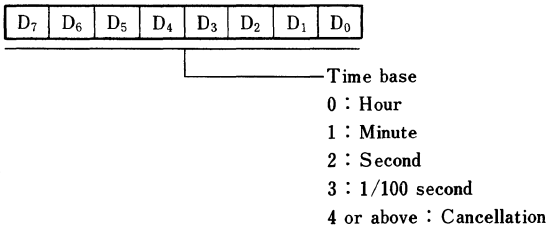
〔1〕

2. Control switch



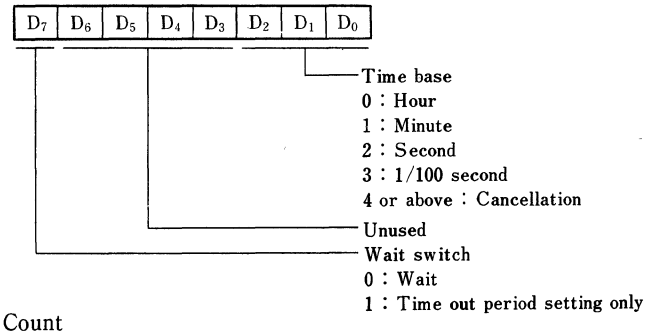
〔2〕

2. Time base

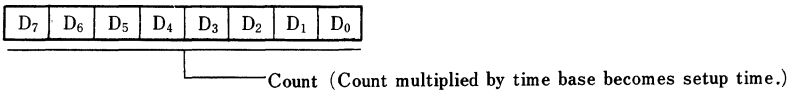


〔3〕

1. Control code



2. Count

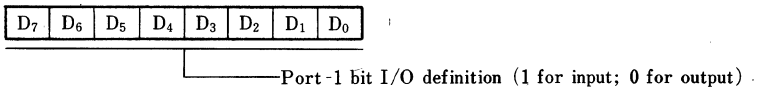


〔4〕

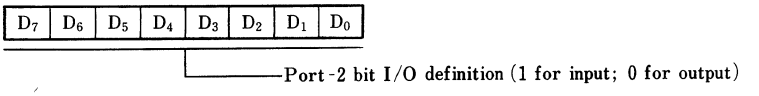
2. Only in message data 1. "0" is not allowed.

〔5〕

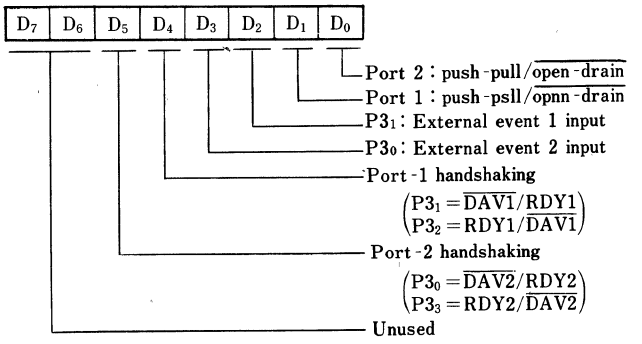
1. Port-1 mode



2. Port-2 mode



3. Port-3 mode



LH8590/LH8590A Z8590/Z8590A Universal Peripheral Controller

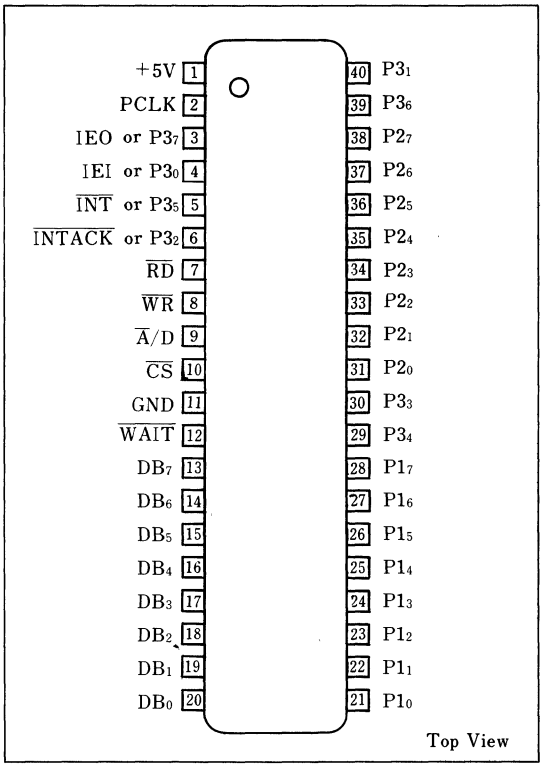
Description

The LH8590 Z8590 Universal Peripheral Controller (UPC) is an intelligent peripheral controller for distributed processing applications (Fig. 3). The LH8590 unburdens the host processor by assuming tasks traditionally done by the host (or by added hardware), such as performing arithmetic, translating or formatting data, and controlling I/O devices. Based on the Z8 microcomputer architecture and instruction set, the LH8590 contains 2K bytes of internal program ROM, a 256-byte register file, three 8-bit I/O ports, and two counter/timers.

The LH8590 offers fast execution time, an effective use of memory, and sophisticated interrupt, I/O, and bit manipulation. Using a powerful and extensive instruction set combined with an efficient internal addressing scheme, the LH8590 speeds program execution and efficiently packs program code into the on-chip ROM.

An important feature of the LH8590 is an internal register file containing I/O port and control registers accessed both by the LH8590 program and indirectly by its associated master CPU. This architecture results in both byte and programming efficiency, because LH8590 instructions can operate directly on I/O data without moving it to and from an accumulator. Such a structure allows the user to allocate as many general purpose registers as the application requires for data buffers between the CPU and peripheral devices. All general-purpose registers can be used as address pointers, index registers, data buffers, or stack space.

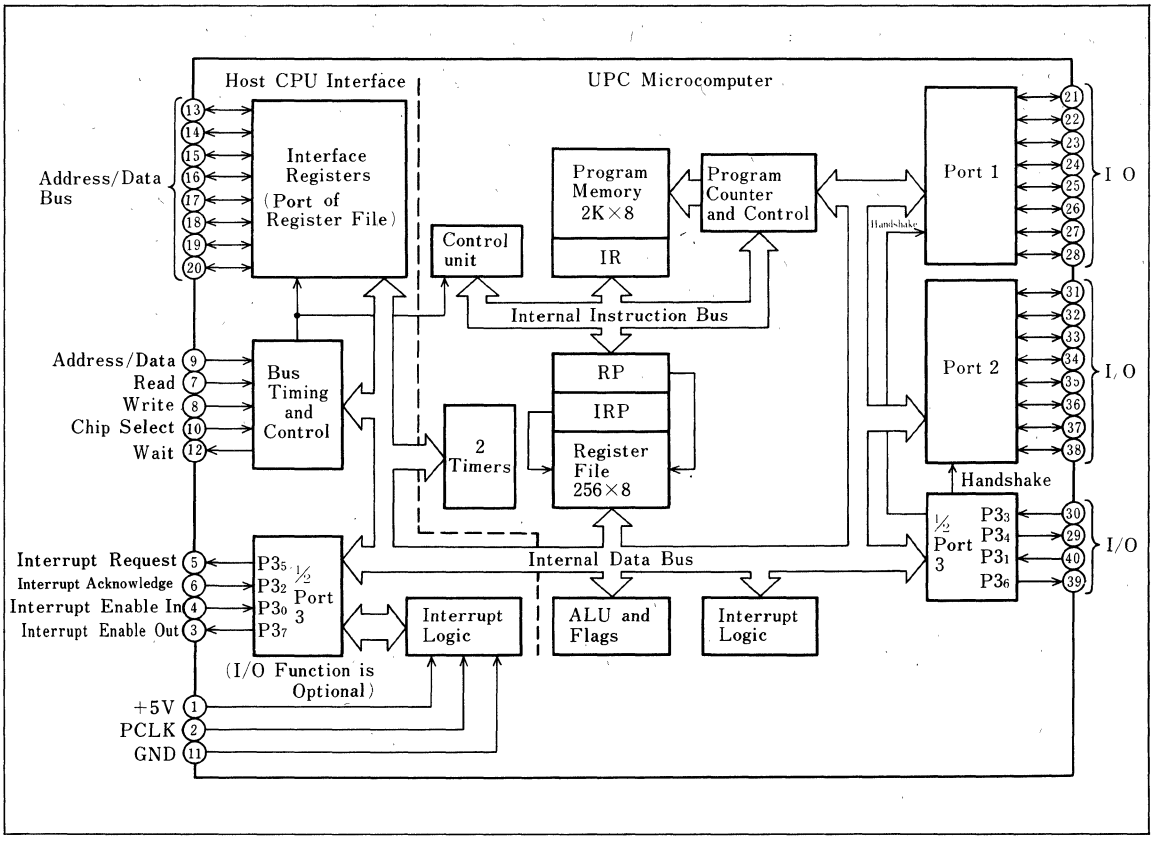
Pin Connections



Features

1. Complete slave microcomputer, for distributed processing use.
2. Unmatched power of Z8 architecture and instruction set.
3. Three programmable I/O Ports, two with optional 2-Wire Handshake.
4. Six levels of priority interrupts from eight sources: six from external sources and two from internal sources.
5. Two programmable 8-bit counter/timers each with a 6-bit prescaler. Counter/Timer T0 is driven by an internal source, and Counter/Timer T1 can be driven by internal or external sources. Both counter/timers are independent of program execution.
6. 256-byte register file, accessible by both the master CPU and LH8590, as allocated in the LH8590 program.
7. 2K bytes of on-chip ROM for efficiency and versatility.

Block Diagram



Pin Description

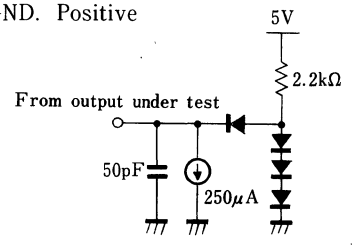
Pin	Meaning	I/O	Function
DB_0-DB_7	Data Bus	Bidirectional 3-state	System data bus
$\overline{A/D}$	Address/Data Select	I	Address/data select signal
$\overline{RD}$	Read	I	Active low. Indicates that reading operation is in progress.
$\overline{WR}$	Write	I	Active low. Indicates that writing operation is in progress.
$\overline{CS}$	Chip Select	I	Active low. Chip select signal
$\overline{WAIT}$	Wait	O	Active low. Open-drain. Used for synchronization with the CPU.
PI_0-PI_7	I/O Port Lines	I/O	Parallel I/O
$P2_0$-$P2_7$	I/O Port Lines	I/O	Parallel I/O
$P3_0$-$P3_7$	I/O Port Lines	I/O	Parallel I/O
PCLK	Clock	I	Single-phase clock. This clock does not need to be related to the CPU clock.

Absolute Maximum Ratings

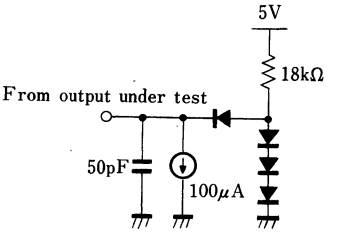
Parameter	Symbol	Ratings	Unit
Input voltage*	V_{IN}	−0.5～+7.0	V
Output voltage*	V_{OUT}	−0.5～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

Standard Test Conditions

All voltages are referenced to GND. Positive current flows into the reference pin.



Standard test load 1



Standerd test load 2

DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Colck input high voltage	V_{CH}		2.4	V_{CC}	V	
Clock input low voltage	V_{CL}		−0.3	0.8	V	
Input high voltage	V_{IH}		2.0	V_{CC}	V	
Input low voltage	V_{IL}		−0.3	0.8	V	
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4		V	1
Output low voltage	V_{OL}	I_{OL}=2mA		0.4	V	1
Input leakage current	I_{IL}	0 ≦ V_{IN} ≦ +5.25V	−10	10	μA	
Output leakage current	I_{OL}	0 ≦ V_{IN} ≦ +5.25V	−10	10	μA	
Current consumption	I_{CC}			250	mA	

Note 1: For A_0-A_{11}, D_0-D_7, $\overline{MDS}$, $\overline{SYNC}$, $\overline{MAS}$, and MR/W/IACK of the device for 64-pin development I_{OH}=−100 μA and I_{OL}=1.0mA.

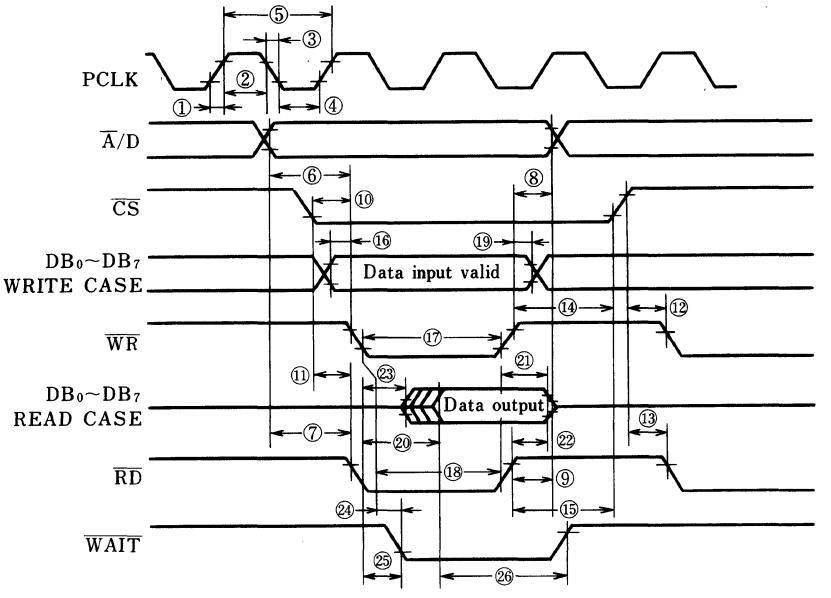
■ AC Characteristics

(1) Master CPU interface timing

(V_{CC}=5V±5%, Ta=0~+70℃)

No.	Symbol	Parameter	LH8090		LH8090A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TrC	Clock rise time		20		15	ns	
2	TwCH	Clock high width	105	1855	70	1855	ns	
3	TfC	Clock fall time		20		10	ns	
4	TwCl	Clock low width	105	1855	70	1855	ns	
5	TpC	Clock period	250	2000	165	2000	ns	
6	TsA/D(WR)	$\overline{A}$/D to $\overline{WR}$ ↓ setup time	80		80		ns	
7	TsA/D(RD)	$\overline{A}$/D to $\overline{RD}$ ↓ setup time	80		80		ns	
8	ThA/D(WR)	$\overline{WR}$ to $\overline{A}$/D ↑ hold time	30		25		ns	
9	ThA/D(RD)	$\overline{RD}$ to $\overline{A}$/D ↑ hold time	30		25		ns	
10	TsCSf(WR)	$\overline{CS}$ ↓ to $\overline{WR}$ ↓ setup time	0		0		ns	
11	TsCSf(RD)	$\overline{CS}$ ↓ to $\overline{RD}$ ↓ setup time	0		0		ns	
12	TsCSr(WR)	$\overline{CS}$ ↑ to $\overline{WR}$ ↓ setup time	60		60		ns	
13	TsCSr(RD)	$\overline{CS}$ ↑ to $\overline{RD}$ ↓ setup time	60		60		ns	
14	ThCS(WR)	$\overline{WR}$ to $\overline{CS}$ ↓ hold time	0		0		ns	
15	ThCS(RD)	$\overline{RD}$ to $\overline{CS}$ ↓ hold time	0		0		ns	
16	TsDI(WR)	Data in to $\overline{WR}$ ↓ setup time	0		0		ns	
17	Tw(WR)	$\overline{WR}$ low width	390		250		ns	
18	Tw(RD)	$\overline{RD}$ low width	390		250		ns	
19	ThWR(DI)	Data in to $\overline{WR}$ ↑ hold time	0		0		ns	
20	TdRD(DI)	Data valid from $\overline{RD}$ ↓ delay					ns	1
21	ThRD(DI)	Data valid to $\overline{RD}$ ↑ hold time	0		0		ns	
22	TdRD(DIz)	Data bus float from $\overline{RD}$ ↑ delay		70		45	ns	
23	TdRD(DBA)	$\overline{RD}$ ↓ to read data active delay	0		0		ns	
24	TdWR(W)	$\overline{WR}$ ↓ to $\overline{WAIT}$ ↓ delay		150		150	ns	
25	TdRD(W)	$\overline{RD}$ ↓ to $\overline{WAIT}$ ↓ delay		150		150	ns	
26	TdDI(W)	Data valid to $\overline{WAIT}$ ↑ delay	0		0		ns	

Note: The timing characteristics given reference 2.0V as High and 0.8V as Low. All output ac parameters use test load 1.
Note 1: This parameter is dependent on the state of LH8590 at the time of master CPU access.

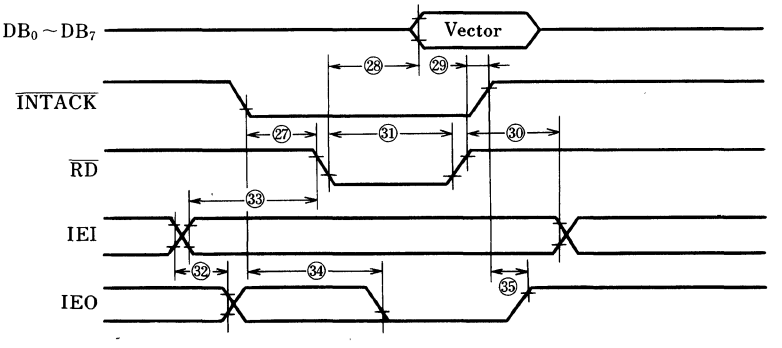


Master CPU interface timing

(2) Interrupt acknowledge timing

No.	Symbol	Parameter	LH8590		LH8590A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
27	TsACK(RD)	$\overline{INTACK}$ ↓ to $\overline{RD}$ ↓ setup time	90		80		ns	1
28	TdRD(DI)	$\overline{RD}$ ↓ to vector valid delary		255		180	ns	
29	ThRD(ACK)	$\overline{RD}$ ↑ to $\overline{INTACK}$ ↑ hold time	0		0		ns	
30	ThIEI(RD)	$\overline{RD}$ to IEI ↑ hold time	100		100		ns	
31	TwRDl	$\overline{RD}$ (acknowledge) low width	255		250		ns	
32	TdIEI(IEO)	IEI to IEO delay		120		100	ns	
33	TsIEI(RD)	IEI to $\overline{RD}$ ↓ setup time	150		120		ns	
34	TdACK(IEO)	$\overline{INTACK}$ ↓ to IEO ↓ delay		250		250	ns	
35	TdADKr(IEO)	$\overline{INTACK}$ ↑ to IEO ↑ delay		250		250	ns	

Note: The timing charcteristics given reference 2.0V as High and 0.8V as Low. All output ac parameters use test load 1.
Note 1: In case where daisy chain is not used.

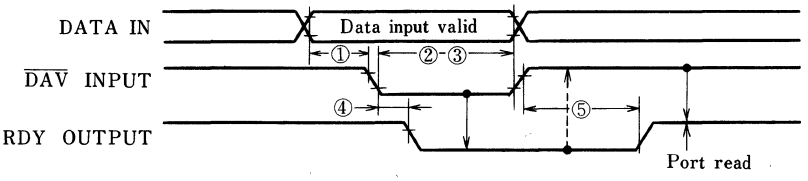


Interrupt acknowledge timing

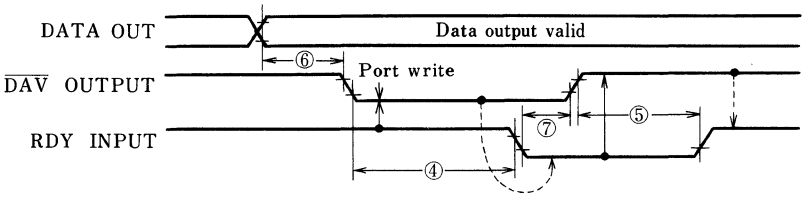
(3) Handshake timing

No.	Symbol	Parameter	LH8590		LH8590A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TsDI(DA)	Data in setup time	0		0		ns	
2	ThDA(DI)	Data in hold time	230		230		ns	
3	TwDA	Data available width	175		175		ns	1,2
4	TdDAL(RY)	Data available low to ready	20	175	20	175	ns	1,2
		delay time	0		0		ns	2,3
5	TdDAH(RY)	Data available high to ready		150		150	ns	1,2
		delay time	0		0		ns	2,3
6	TdDO(DA)	Data out to available delay time	50		50		ns	2
7	TdRY(DA)	Ready to data available delay time	0	205	0	205	ns	2

Note 1: Input handshake
Note 2: Test Load 1
Note 3: Output Handshake



Input handshake timing

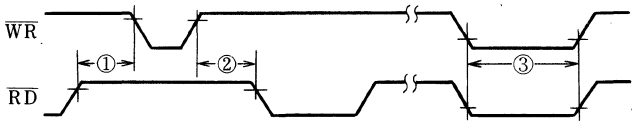


Output handshake timing

(4) Reset timing

No.	Symbol	Parameter	LH8590		LH8590A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TdRDQ(WR)	Delay from $\overline{RD}$ ↑ to $\overline{WR}$ ↓ for no reset	40		35		ns	
2	TdWRQ(RD)	Delay from $\overline{WR}$ ↑ to $\overline{RD}$ ↓ for no reset	50		35		ns	
3	TwRES	Minimum width of $\overline{WR}$ and $\overline{RD}$ both low for reset	250		250		ns	1

Note 1: Internal reset signal is $^1/_2$ to 2 clock delays from external reset condition.



Reset timing

(5) RAM version program memory timing

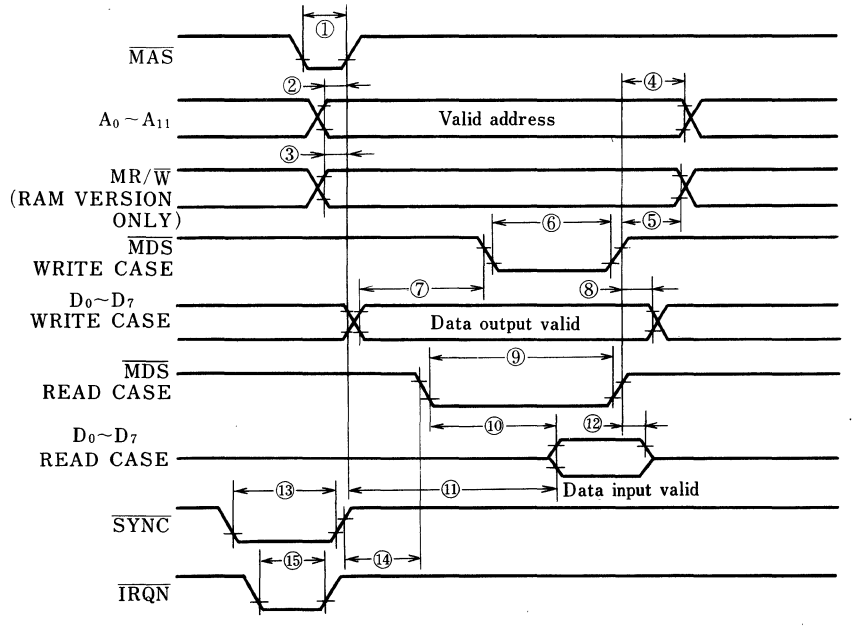
No.	Symbol	Parameter	LH8590		LH8590A		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
1	TwMAS	Memory address strobe width	60		55		ns	1
2	TdA(MAS)	Address valid to memory address strobe ↑ delay	30		30		ns	1
3	TdMR/W(MAS)	Memory read/write to memory address strobe ↑ delay	30		30		ns	1
4	TdMDS(A)	Memory data strobe ↑ to address change delay	60		60		ns	
5	TdMDS(MR/W)	Memory data strobe ↑ to memory read/write not valid delay	80		75		ns	
6	Tw(MDS)	Memory data strobe width (write case)	160		110		ns	2
7	TdDO(MDS)	Data out valid to memory data strobe ↓ delay	30		30		ns	1
8	TdMDS(DO)	Memory data strobe ↑ to data change delay	30		30		ns	1
9	Tw(MDS)	Memory data strobe width (read case)	230		230		ns	2
10	TdMDS(DI)	Memory data strobe ↓ to data in valid delay		160		130	ns	3
11	TdMAS(DI)	Memory address strobe ↑ to data in valid delay		280		220	ns	3
12	ThMDS(DI)	Memory data strobe ↑ to data in hold time	0		0		ns	
13	TwSY	Instruction sync out width	160		100		ns	
14	TdSY(MDS)	Instruction sync out ↑ to memory data strobe ↓ delay	200		160		ns	
15	TwI	Interrupt request via port 3 input width	100		100		ns	

Note: All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0". All output ac parameters use test load 2. Timings are preliminary and subject to change.

Note 1: Delay time are specified for an input clock frequency of 4 MHz. When operating at a lower frequency, the increase in input clock period must be added to the specified delay time.

Note 2: Data strobe width is specified for an input clock frequency of 4 MHz. When operating at a lower frequency, the increase in three input clock periods must be added to the specified width.Data strobe width varies according to instruction being executed.

Note 3: Address strobe and data strobe to data in valid delay times represent memory system access times and are given for a 4 MHz input frequency.



RAM version program memory timing

■ Functional Description

(1) Address space.

On the 40-pin UPC, all address space is committed to on-chip memory. There are 2048 bytes of maskprogrammed ROM and 256 bytes of register file. I/O is memory-mapped to three registers in the register file.

Program Memory Fig. 1 is a map of the 2K on-chip program ROM.The first 12 bytes of program memory are reserved for the LH8590 interrupt vectors.

Register File This 256-byte file includes three I/O port registers (1_H-3_H), 234 general-purpose reginters (6_H-EF_H), and 19 control, status and specical I/O registers (0_H, 4_H, 5_H, and $F0_H$-FF_H). The functions and mnemonics assigned to these register address locations are shown in Fig. 2. Of the 256 UPC registers, 19 can be directly accessed by the master CPU; the others are accessed indirecly via the block transfer mechanism.

UPC instructions may access registers directly or indirectly using an 8-bit address mode or a 4-bit address mode and a Register Pointer. For the 4-bit addressing mode, the file is divided into 16 working register groups, each occupying 16 contiguous locations (Fig.3).

Stacks An 8-bit Stack Pointer (SP), register R255, is used for addressing the stack, residing within the 234 general-purpose registers, address location 6H through EFH.

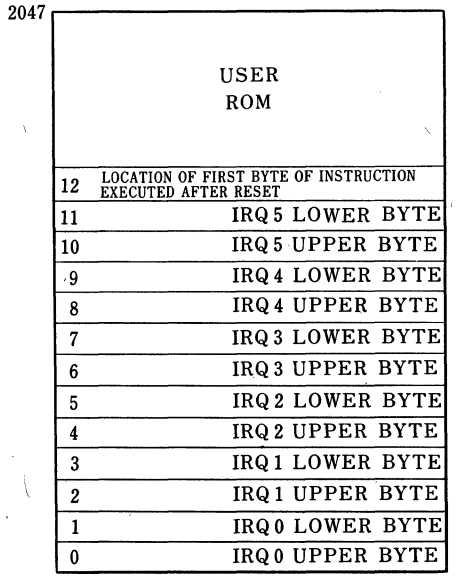


Fig.1 Program memory map

LOCATION		IDENTIFIER (UPC Side)
FF_H	STACK POINTER	SP
FE_H	MASTER CPU INTERRUPT CONTROL	MIC
FD_H	REGISTER POINTER	RP
FC_H	PROGRAM CONTROL FLAGS	FLAGS
FB_H	UPC INTERRUPT MASK REGISTER	IMR
FA_H	UPC INTERRUPT REQUEST REGISTER	IRQ
$F9_H$	UPC INTERRUPT PRIORITY REGISTER	IPR
$F8_H$	PORT 1 MODE	P1M
$F7_H$	PORT 3 MODE	P3M
$F6_H$	PORT 2 MODE	P2M
$F5_H$	T_0 PRESCALER	PRE0
$F4_H$	TIMER/COUNTER 0	T0
$F3_H$	T_1 PRESCALER	PRE1
$F2_H$	TIMER/COUNTER 1	T1
$F1_H$	TIMER MODE	TMR
$F0_H$	MASTER CPU INTERRUPT VECTOR REG.	MIV
EF_H	GENERAL-PURPOSE REGISTERS	
6_H		
5_H	DATA INDIRECTION REGISTER	DIND
4_H	LIMIT COUNT REGISTER	LC
3_H	PORT 3	P3
2_H	PORT 2	P2
1_H	PORT 1	P1
0_H	DATA TRANSFER CONTROL REGISTER	DTC

Fig.2 Register file orgranization

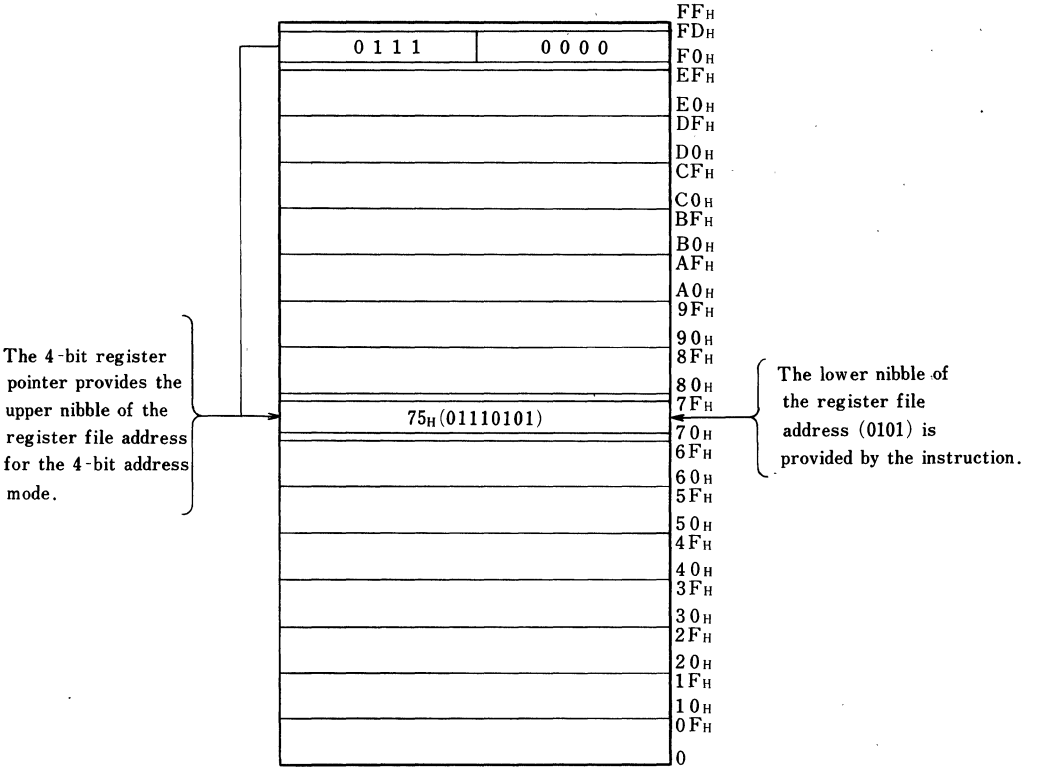


Fig. 3 Register pointer mechanism

(2) Ports

The LH8590 has 24 lines dedicated to input and output. These are grouped into three ports of eight lines each and can be configured under software control as inputs, outputs, or special control signals. They can be programmed to provide Parallel I/O with or without handshake and timing signals. All outputs can have active pullups and pulldowns, compatible with TTL loads. In addition, Port 1 and 2 may be configured as open-drain outputs.

Port 1 Individual bits of Port 1 can be configured as input or output by programming Port 1 Mode register (P1M) F8H. This port is accessed by the UPC program as general register 1H.

Port 1 may be placed under handshake control by programming Port 3 Mode register (P3M) F7H.

Port 2 Individual bits of Port 2 can be configured as inputs or outputs by programming Port 2 Mode register (P2M) F6H. This port is accessed by the UPC program as general register 2H, and its functions and methods of programming are the same as those of Port 1.

Port 3 This port can be configured as I/O or control lines by programming the Port 3 Mode register. Port 3 is accessed as general register 3H. The directions of the eight data lines are fixed. Four lines, $P3_0$ through $P3_3$, are inputs, and the other four, $P3_4$ through $P3_7$, are outputs. The control functions performed by Port 3 are listed in Table 1.

Table 1 Port 3 control functions

Function	Line	I/O	Signal
Handshake	$P3_1$	I	$\overline{DAV_2}/RDY_2$
	$P3_3$	I	$\overline{DAV_1}/RDY_1$
	$P3_4$	O	$RDY_1/\overline{DAV_1}$
	$P3_6$	O	$RDY_2/\overline{DAV_2}$
LH8590 Iterrupt Request*	$P3_0$	I	IRQ_3
	$P3_1$	I	IRQ_2
	$P3_3$	I	IRQ_1
Counter/Timer	$P3_1$	I	TIN
	$P3_6$	O	TOUT
Master CPU	$P3_5$	O	$\overline{INT}$
	$P3_2$	I	$\overline{INTACK}$
	$P3_0$	I	IEI
	$P3_7$	O	IEO

* $P3_0$, $P3_1$, and $P3_3$ can always be used as UPC interrupt request inputs, regardless of the configuration programmed.

(3) Counter/Timers

The LH8590 contains two 8-bit programmable counter/timers, each driven by an internal 6-bit programmable prescaler.

The T1 prescaler can be driven by internal or external clock sources. The T0 prescaler is driven by an internal clock source. Both counter/timers operate indpendently of the processor instruction sequence to relieve the program from time-critical operations like event counting or elapsed-time calculation. T0 Prescaler register (PRE0) F5H and T1 Pre-scaler register (PRE1) F3H can be programmed to divide the input frequency of the source being counted by any number from 1 to 64. A Counter register ($F2_H$ or $F4_H$) is loaded with a number from 1 to 256. The corresponding counter is decremented from this number each time the prescaler reaches end-of-count. When the count is complete, the counter issues a timer interrupt request; IRQ_4 for T0 or IRQ_5 for T1.

(4) Interrupts

The LH8590 allows six interrupts from eight different sources as follows:

- Port 3 lines $P3_0$, $P3_2$, and $P3_3$.
- The master CPU(3).
- The two counter/timers.

These interrupts can be masked and globally enabled or disabled using Interrupt Mask Register (IMR) FBH. Interrupt Priority Register (IPR) F9H specifies the order of their priority. All UPC interrupts are vectored.

Table 2 lists the UPC's interrupt sourcers, their types, and their vector locations in program ROM.

The LH8590 also supports polled systems. To accommodate a polled structure, any or all of the interrupt inputs can be masked and the Interrupt Request register polled to determine which of the interrupt requests needs service.

(5) Master CPU Register File Access

There are two ways in which the master CPU can acess the LH8590 register file: direct access and block access.

Direct access Three LH8590 registers — the Data Transfer Control, the Master Interrupt Vector, and the Master Interrupt Control — are mapped directly into the master CPU address space.

Block Access The master CPU may transmit or receive blocks of data via address xxx10101. When the master CPU accesses this address, the LH8590 register pointed to by the Data Indirection register is read or written. The Data Indirection register is incremented, and the Limit Count register is decremented.

Table 2 Interrupt types, Sources, and Vector locations

Name	Source	Vector location	Comments
IRQ0	EOM, XESS, LERR	0, 1	Internal (R0 bits 0, 1, 2)
IRQ1	$\overline{DAV}1$, LRQ1	2, 3	External ($P3_3$) ↓ edge triggered
IRQ2	$\overline{DAV}2$, IRQ2, T_{IN}	4, 5	External ($P3_1$) ↓ edge triggered
IRQ3	IRQ3, IEI	6, 7	External ($P3_0$) ↓ edge triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

■ Instructions

(1) Addressing modes

The following notation is used to describe the addressing modes and instruction operations.

IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
x	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working-register pair address

(2) Additional symbols

dst	Destination location or contents
src	Source location or contents
cc	Condition code (see list)
@	Indirect address prefix
PC	Program Counter
SP	Stack Pointer (control register 255)
FLAGS	Flag register (control register 252)
RP	Register Pointer (control register 253)
IMR	Interrupt Mask register (control register 251)

Assignment of a value is indicated by the symbol "←". For example,

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr(n)" is used to refer to bit "n" of a given location. For example to refer to bit"n" of a given location. For example,

dst (7)

refers to bit 7 of the destination operand.

(3) Flags

Control Register 252 contains the following six flags:

C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Cleared to zero
1	Set to one
*	Set or cleared according to operation
–	Unaffected
×	Undefined

(4) Condition codes

Table 3 shows condition code.

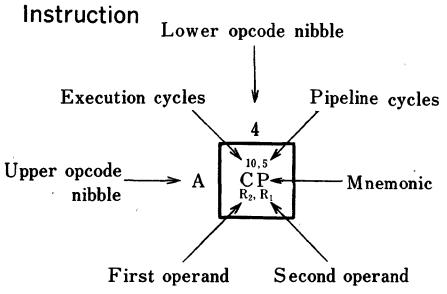
Table 3 Condition codes

Value	Mnemonic	Meaning	Flags set
1000		Always true	.....
0111	C	Carry	C=1
1111	NC	No carry	C=0
0110	Z	Zero	Z=1
1110	NZ	Not zero	Z=0
1101	PL	Plus	S=0
0101	MI	Minus	S=1
0100	OV	Overflow	V=1
1100	NOV	No overflow	V=0
0110	EQ	Equal	Z=1
1110	NE	Not equal	Z=0
1001	GE	Greater than or equal	(S XOR V)=0
0001	LT	Less than	(S XOR V)=1
1010	GT	Greater than	[Z OR (S XOR V)]=0
0010	LE	Less than or equal	[Z OR (S XOR V)]=1
1111	UGE	Unsigned greater than or equal	C=0
0111	ULT	Unsigned less than	C=1
1011	UGT	Unsigned greater than	(C=0 AND Z=0)=1
0011	ULE	Unsigned less than or equal	(C OR Z)=1
0000		Never true	.....

(5) Opcode map

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6,5 DEC R_1	6,5 DEC IR_1	6,5 ADD r_1, r_2	6,5 ADD r_1, Ir_2	10,5 ADD R_2, R_1	10,5 ADD IR_2, R_1	10,5 ADD R_1, IM	10,5 ADD IR_1, IM	6,5 LD r_1, R_2	6,5 LD r_2, R_1	12/10,5 DJNZ r_1, RA	12/10,0 JR cc, RA	6,5 LD r_1, IM	12/10,0 JP cc, DA	6,5 INC r_1	
1	6,5 RLC R_1	6,5 RLC IR_1	6,5 ADC r_1, r_2	6,5 ADC r_1, Ir_2	10,5 ADC R_2, R_1	10,5 ADC IR_2, R_1	10,5 ADC R_1, IM	10,5 ADC IR_1, IM								
2	6,5 INC R_1	6,5 INC IR_1	6,5 SUB r_1, r_2	6,5 SUB r_1, Ir_2	10,5 SUB R_2, R_1	10,5 SUB IR_2, R_1	10,5 SUB R_1, IM	10,5 SUB IR_1, IM								
3	8,0 JP IRR_1	6,1 SRP IM	6,5 SBC r_1, r_2	6,5 SBC r_1, Ir_2	10,5 SBC R_2, R_1	10,5 SBC IR_2, R_1	10,5 SBC R_1, IM	10,5 SBC IR_1, IM								
4	8,5 DA R_1	8,5 DA IR_1	6,5 OR r_1, r_2	6,5 OR r_1, Ir_2	10,5 OR R_2, R_1	10,5 OR IR_2, R_1	10,5 OR R_1, IM	10,5 OR IR_1, IM								
5	10,5 POP R_1	10,5 POP IR_1	6,5 AND r_1, r_2	6,5 AND r_1, Ir_2	10,5 AND R_2, R_1	10,5 AND IR_2, R_1	10,5 AND R_1, IM	10,5 AND IR_1, IM								
6	6,5 COM R_1	6,5 COM IR_1	6,5 TCM r_1, r_2	6,5 TCM r_1, Ir_2	10,5 TCM R_2, R_1	10,5 TCM IR_2, R_1	10,5 TCM R_1, IM	10,5 TCM IR_1, IM								
7	10/12,1 PUSH R_2	12/14,1 PUSH IR_2	6,5 TM r_1, r_2	6,5 TM r_1, Ir_2	10,5 TM R_2, R_1	10,5 TM IR_2, R_1	10,5 TM R_1, IM	10,5 TM IR_1, IM								
8	10,5 DECW RR_1	10,5 DECW IR_1	12,0 LDE r_1, Irr_2	18,0 LDEI Ir_1, Irr_2												6,1 DI
9	6,5 RL R_1	6,5 RL IR_1	12,0 LDE r_2, Irr_1	18,0 LDEI Ir_2, Irr_1												6,1 EI
A	10,5 INCW RR_1	10,5 INCW IR_1	6,5 CP r_1, r_2	6,5 CP r_1, Ir_2	10,5 CP R_2, R_1	10,5 CP IR_2, R_1	10,5 CP R_1, IM	10,5 CP IR_1, IM								14,0 RET
B	6,5 CLR R_1	6,5 CLR IR_1	6,5 XOR r_1, r_2	6,5 XOR r_1, Ir_2	10,5 XOR R_2, R_1	10,5 XOR IR_2, R_1	10,5 XOR R_1, IM	10,5 XOR IR_1, IM								16,0 IRET
C	6,5 RRC R_1	6,5 RRC IR_1	12,0 LDC r_1, Irr_2	18,0 LDCI Ir_1, Irr_2				10,5 LD r_1, x, R_2								6,5 RCF
D	6,5 SRA R_1	6,5 SRA IR_1	12,0 LDC r_2, Irr_1	18,0 LDCI Ir_2, Irr_1	20,0 CALL* IRR_1		20,0 CALL DA	10,5 LD r_2, x, R_1								6,5 SCF
E	6,5 RR R_1	6,5 RR IR_1		6,5 LD r_1, Ir_2	10,5 LD R_2, R_1	10,5 LD IR_2, R_1	10,5 LD R_1, IM	10,5 LD IR_1, IM								6,5 CCF
F	8,5 SWAP R_1	8,5 SWAP IR_1		6,5 LD Ir_1, r_2		10,5 LD R_2, IR_1										6,0 NOP
Bytes per Instruction	2				3				2					3	1	



Legend:
R = 8-Bit Address
r = 4-Bit Address
R_1 or r_1 = Dst address
R_2 or r_2 = Src Address

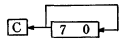
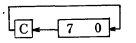
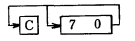
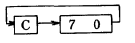
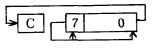
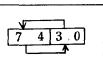
Sequence:
Opcode, First Operand, Second Operand.

Note: The blank areas are not defined.

*2-byte instruction; fatch cycle appears as a 3-byte instruction.

(6) Instruction summary

Instruction and Operation	Addr. mode dst	Addr. mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst+src+C	(Note 1)		1□	* * * * 0 *
ADD dst, src dst←dst+src	(Note 1)		0□	* * * * 0 *
AND dst, src dst←dst AND src	(Note 1)		5□	− * * 0 − −
CALL dst SP←SP−2 @SP←PC; PC←dst	DA IRR		D6 D4	− − − − − −
CCF C←NOT C			EF	* − − − − −
CLR dst dst←0	R IR		B0 B1	− − − − − −
COM dst dst←NOT dst	R IR		60 61	− * * 0 − −
CP dst, src dst←src	(Note 1)		A□	* * * * − −
DA dst dst←DA dst	R IR		40 41	* * * X − −
DEC dst dst←dst−1	R IR		00 01	− * * * − −
DECW dst dst←dst−1	RR IR		80 81	− * * * − −
DI IMR(7)←0			8F	− − − − − −
DJNZ r,dst r←r−1 if r≠0 PC←PC+dst Range: +127∼−128	RA		rA r=0−F	− − − − − −
EI IMR(7)←1			9F	− − − − − −
INC dst dst←dst+1	r R IR		rE r=0−F 20 21	− * * * − −
INCW dst dst←dst+1	RR IR		A0 A1	− * * * − −
IRET FLAGS←@SP;SP←SP+1 PC←@SP;SP←SP+2;IMR(7)←1			BF	* * * * * *
JP cc, dst if cc is true PC←dst	DA IRR		cD c=0−F 30	− − − − − −
JR cc, dst if cc is true, PC←PC+dst Range: +127∼−128	RA		cB c=0−F	− − − − − −
LD dst, src dst←src	r r R r X r Ir R R R IR IR	IM R r X r Ir r R IR IM IM R	rC r8 r9 r=0−F C7 D7 E3 F3 E4 E5 E6 E7 F5	− − − − − −
LDC dst, src dst←src	r Irr	Irr r	C2 D2	− − − − − −
LDCI dst, src dst←src r←r+1; rr←rr+1	Ir Irr	Irr r	C3 D3	− − − − − −
LDE dst, src dst←src	r Irr	Irr r	82 92	− − − − − −

Instruction and Operation	Addr. mode dst	Addr. mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
LDEI dst, src dst←src r←r+1; rr←rr+1	Ir Irr	Irr Ir	83 93	− − − − − −
NOP			FF	− − − − − −
OR dst, src dst←dst OR src	(Note 1)		4□	− * * 0 − −
POP dst dst←@SP SP←SP+1	R IR		50 51	− − − − − −
PUSH src SP←SP−1; @SP←src		R IR	70 71	− − − − − −
RCF C←0			CF	0 − − − − −
RET PC←@SP; SP←SP+2			AF	− − − − − −
RL dst		R IR	90 91	* * * * − −
RLC dst		R IR	10 11	* * * * − −
RR dst		R IR	E0 E1	* * * * − −
RRC dst		R IR	C0 C1	* * * * − −
SBC dst, src dst←dst−src−C	(Note 1)		3□	* * * * 1 *
SCF C←1			DF	1 − − − − −
SRA dst		R IR	D0 D1	* * * 0 − −
SRP src RP←src		IM	31	− − − − − −
SUB dst, src dst←dst−src	(Note 1)		2□	* * * * 1 *
SWAP dst		R IR	F0 F1	X * * X − −
TCM dst,src (NOT dst) AND src	(Note 1)		6□	− * * 0 − −
TM dst,src dst AND src	(Note 1)		7□	− * * 0 − −
XOR dst,src dst←dst XOR src	(Note 1)		B□	− * * 0 − −

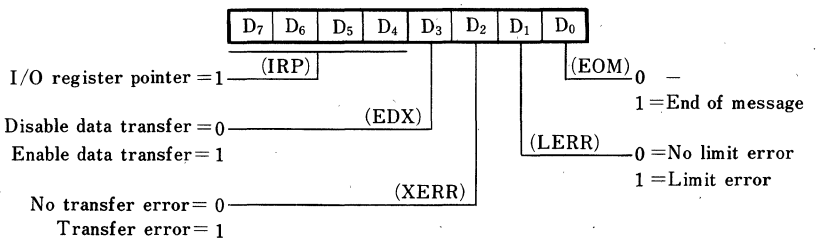
Note 1: These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a □ in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, to determine the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

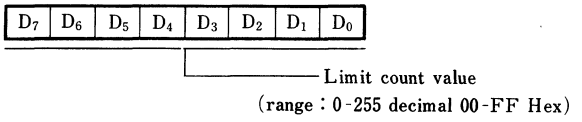
Addr Mode dst	Addr Mode src	Lower Opcode Nibble
r	r	2
r	Ir	3
R	R	4
R	IR	5
R	IM	6
IR	IM	7

■ Register

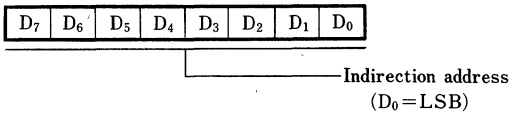
R0 (DTC)
Date Transfer Control Register
UPC register address (Hex): 00



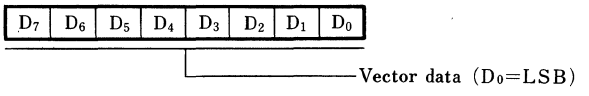
R4 (LC)
Limit Count Register
UPC register address (Hex): 04



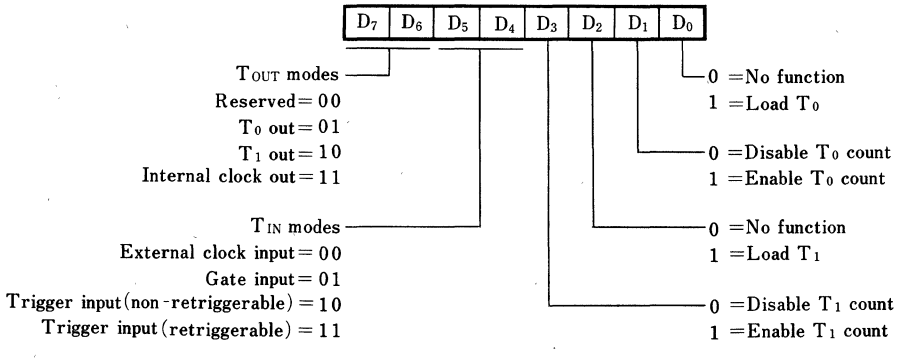
R5 (DIND)
Date Indirect Register
UPC register address (Hex): 05



R240 (MIV)
Master CPU Interrupt Vector Register
UPC register address (Hex): F0

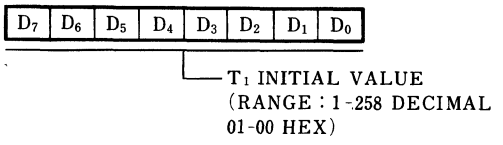


R241 (TMR)
Timer Mode Register
UPC register address (Hex): F1



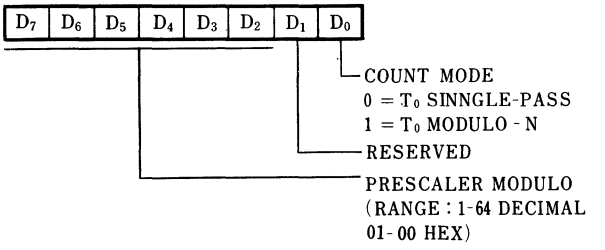
R242 (T1)
Counter/Timer 1 Register

UPC register address (Hex): F2



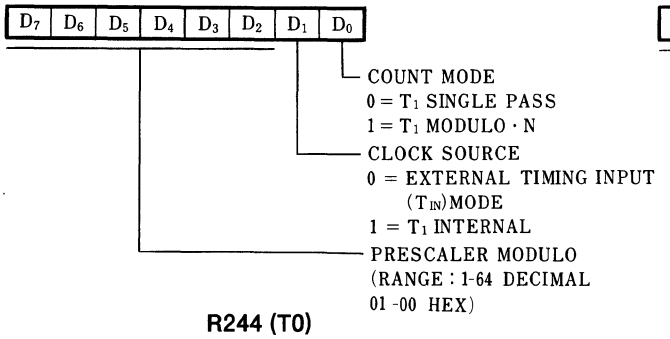
R245 (PRE0)
Prescaler 0 Register

UPC register address (Hex): F5



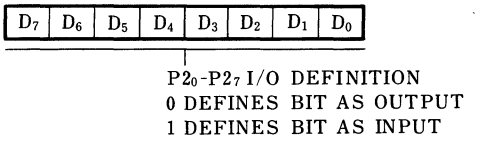
R243 (PRE1)
Prescaler 1 Register

UPC register address (Hex): F3



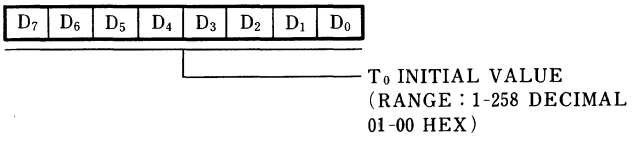
R246 (P2M)
Port 2 Mode Register

UPC register address (Hex): F6



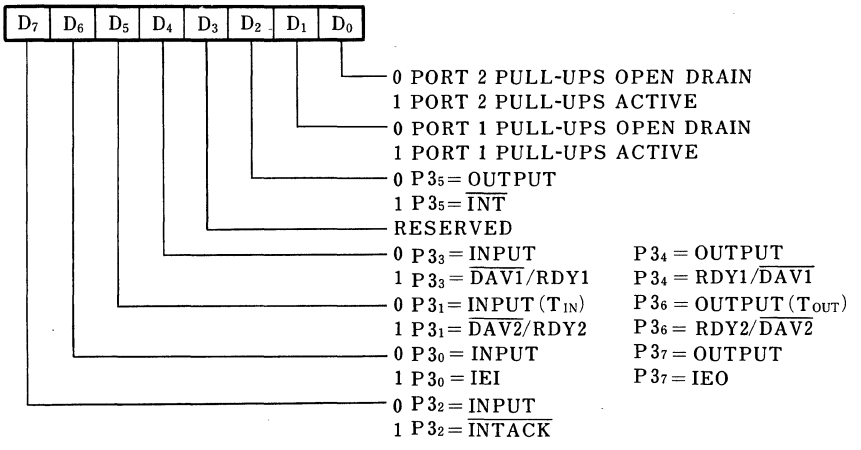
R244 (T0)
Counter/Timer 0 Register

UPC register address (Hex): F4



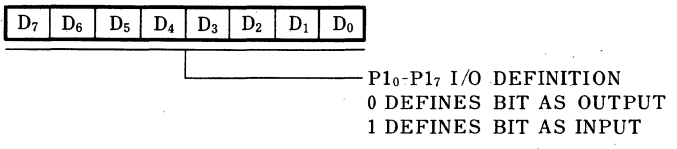
R247 (P3M)
Port 3 Mode Register

UPC register address (Hex): F7



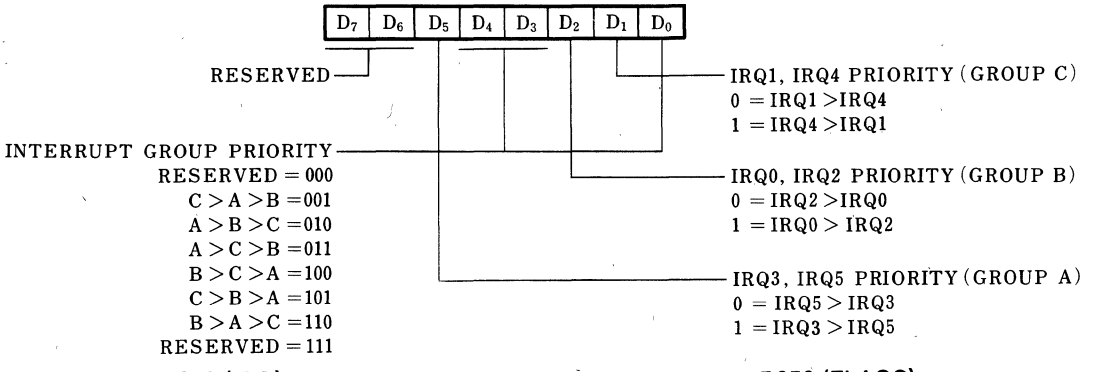
R248 (PIM)
Port 1 Mode Register

UPC register address (Hex): F8



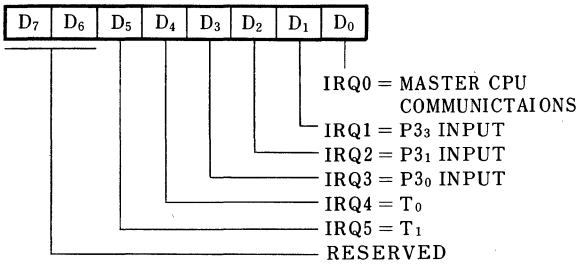
R249 (IPR)
Interrupt Priority Register

UPC register address (Hex): F9 (Write Only)



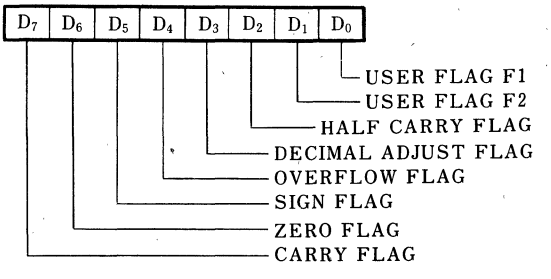
R250 (IRQ)
Interrupt Request Register

UPC register address (Hex): FA



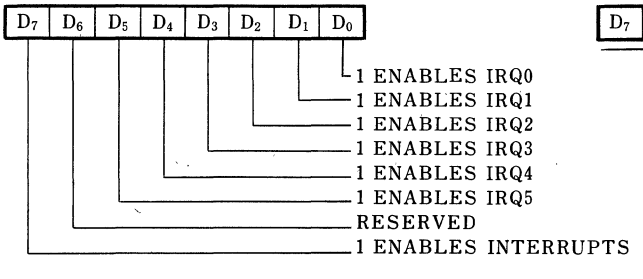
R252 (FLAGS)
Flag Register

UPC register address (Hex): FC



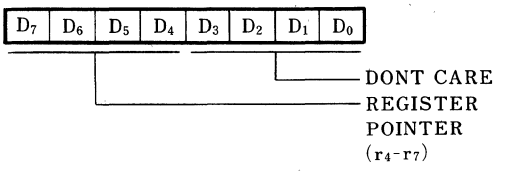
R251 (IMR)
Interrupt Mask Register

UPC register address (Hex): FB

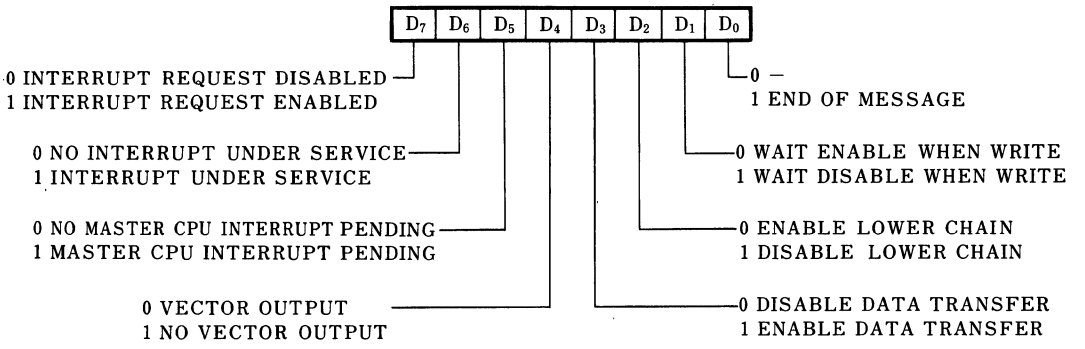


R253 (RP)
Register Pointer

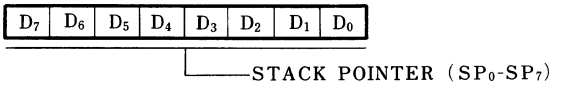
UPC register address (Hex): FD



R254 (MIC)
Master CPU Interrupt Control Register
UPC register address (Hex): FE



R255 (SP)
Stack Pointer
UPC register address (Hex): FF



LH8591/LH8591A Z8591/Z8591A Development Device

Description

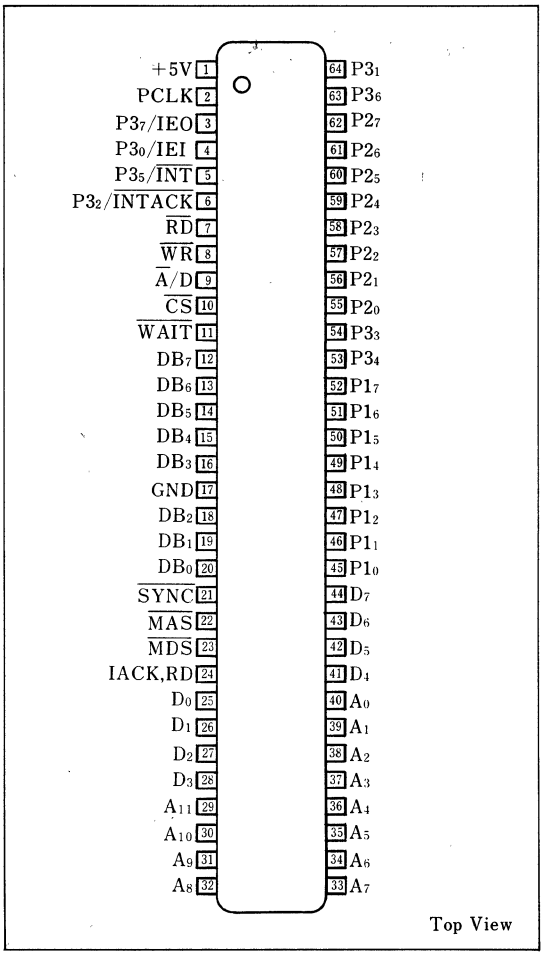
The 64 pin LH8591 (Z8591) is the development version of LH8590 Z8590 UPC with internal mask-programmed ROM. This device allows user to prototype the system in hardware with an actual device and to develop the code that is eventually mask-programmed into the on-chip ROM of the LH8590.

The LH8591 is identical to the LH8590 with the following exceptions.

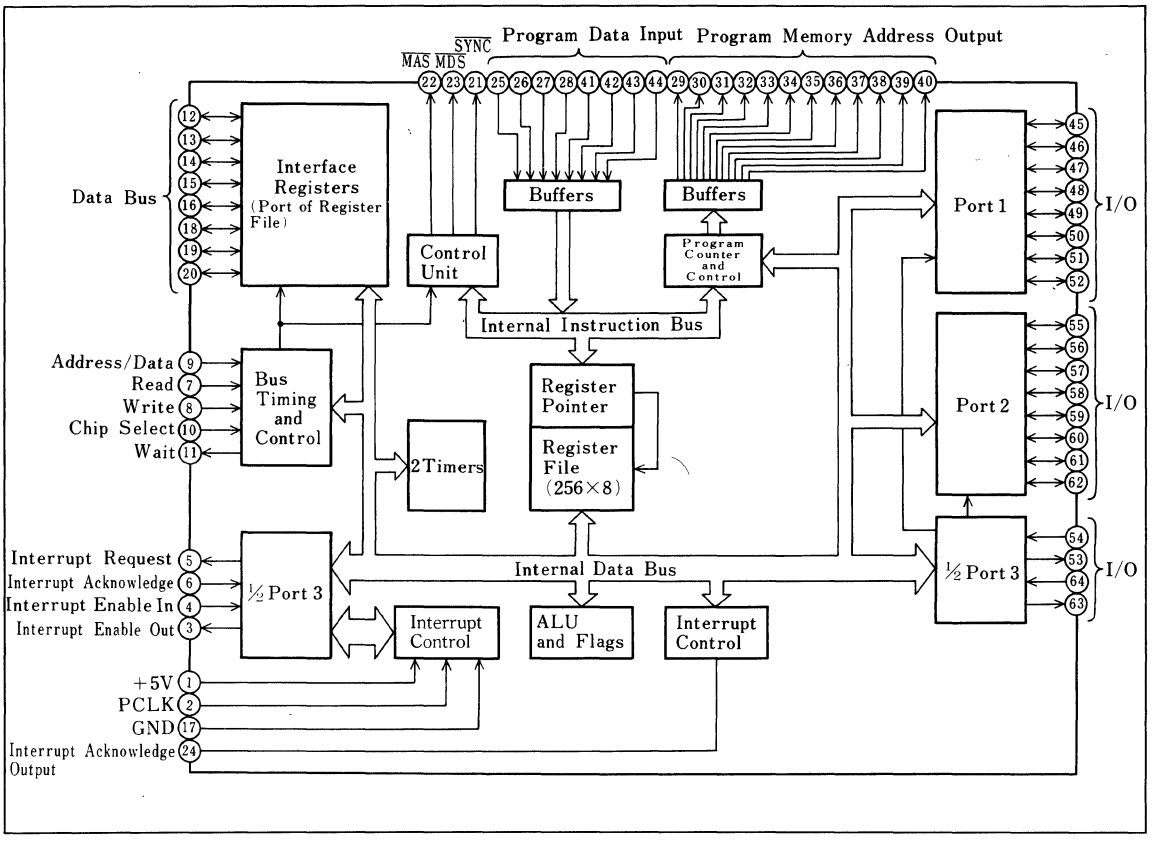
- The internal ROM has been removed.
- The ROM address lines and data lines are buffered and brought out to external pins.
- Control lines for the new memory have been added.

The LH8591A is the high speed version which can operate at 6MHz system clock.

Pin Connections



■ Block Diagram



■ Pin Description

LH8591 has the same functions as those of a 40-pin device LH8590, and the functions of the additional 24 pins are as follows:

Pin	Meaning	I/O	Function
A_0~A_{11}	Program memory address	O	Used for the access to the external memory of 4K bytes.
D_0~D_7	Program data	I	Reads the data through these lines from the external memory.
IACK/MR	Interrupt acknowledge /memory read	O	Active high. This signal becomes high during interrupt or instruction fetch cycle of LH8591.
$\overline{MAS}$	Memory address strobe	O	Active low. This signal is output every memory fetch cycle for the interface with the external ROM.
$\overline{MDS}$	Memory data strobe	O	Active low. This signal becomes low during instruction fetch cycle or write cycle.
$\overline{SYNC}$	Synchronization	O	Active low. This signal becomes low at the clock cycle just before Op-code fetching.

LH8592/LH8592A Z8592/Z8592A Development Device

■ Description

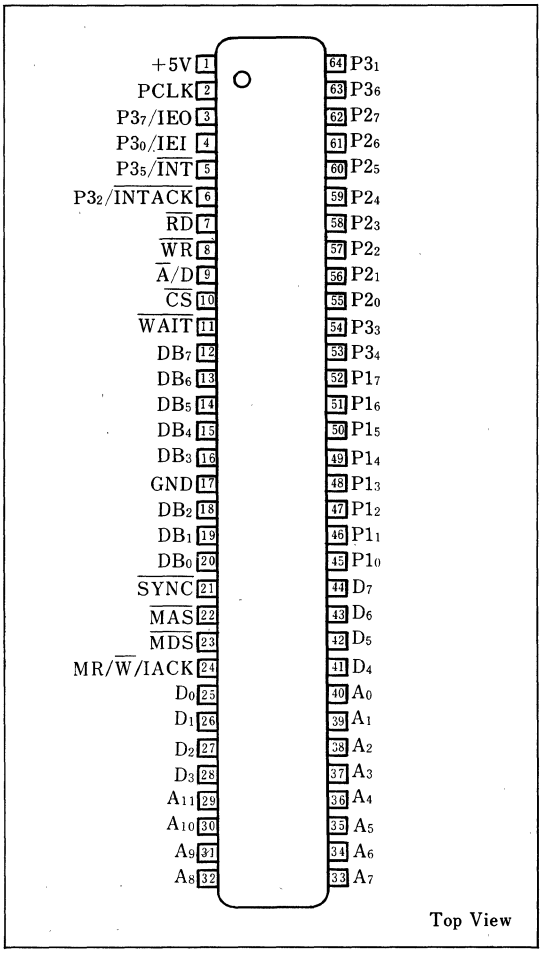
The 64 pin LH8592 (Z8592) is the development version of LH8590 Z8590 UPC with internal mask-programmed ROM. This device allows user to prototype the system in hardware with an actual device and to develop the code that is eventually mask-programmed into the on-chip ROM of the LH8590.

The LH8592 is identical to the LH8590 with the following exceptions.

- The internal ROM has been removed. (But there are 36 bytes internal ROM for a bootstrap program).
- The ROM address lines and data lines are buffered and brought out to external pins.
- Contorl lines for the new memory have been added.

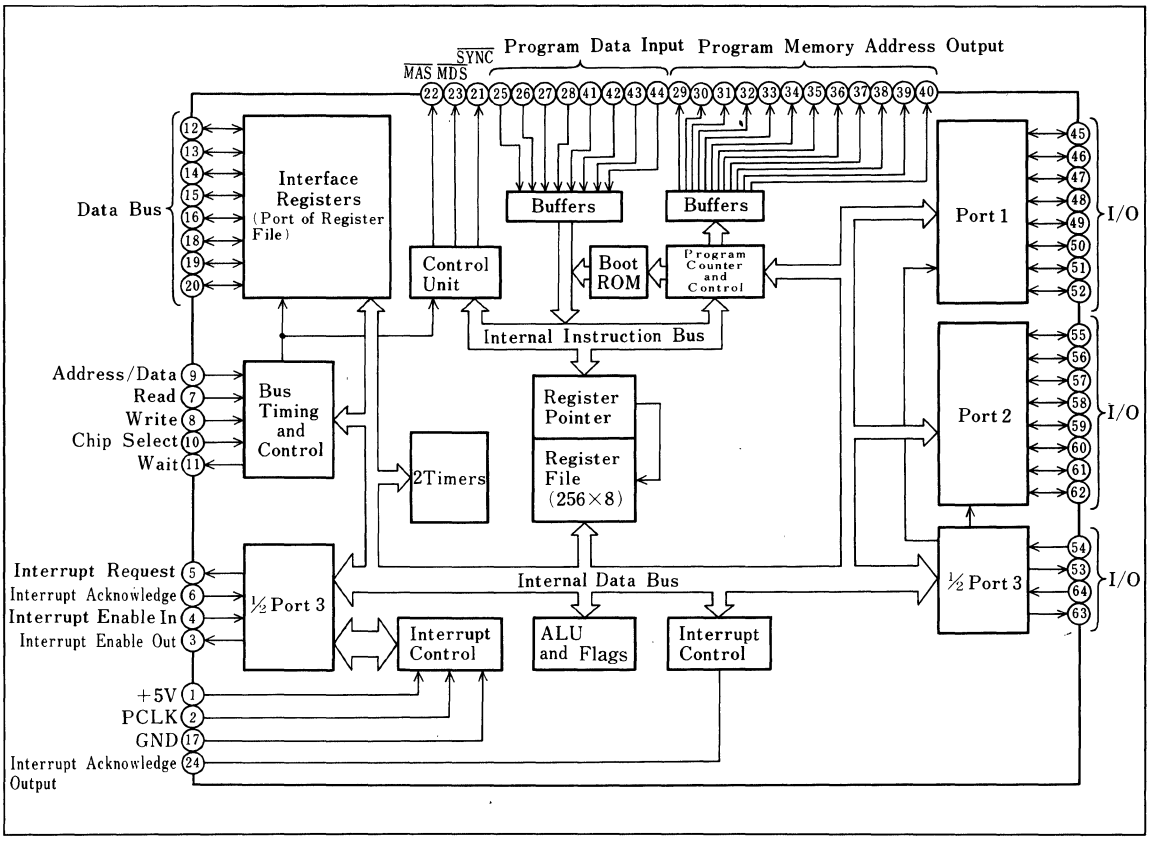
The LH8592A is the high speed version which can operate at 6MHz system clock.

■ Pin Connections



Top View

■ Block Diagram



■ Pin Description

LH8592 has the same functions as those of a 40-pin device LH8590, and the functions of additional 24 pins are as follows:

Pin	Meaning	I/O	Function
$A_0 \sim A_{11}$	Program memory address	O	Used for the access to the external memory of 4K bytes.
$D_0 \sim D_7$	Program data	I	Reads/writes the data through these lines from the external memory.
IACK	Interrupt acknowledge	O	Active high. This signal is always active during interrupt cycle of LH8092.
$\overline{MAS}$	Memory address strobe	O	Active low. This signal is output every memory fetch cycle for interfacing with the external RAM.
$\overline{MDS}$	Memory data strobe	O	Active low. This signal becomes low during instruction fetch cycle or write cycle.
MR/$\overline{W}$	Memory read/write	O	This signal is high during instruction fetching by LH8592, or low while writing into the external memory.
$\overline{SYNC}$	Synchronization	O	Active low. This signal becomes low during clock cycle just before Op-code fetching.

LH8593/LH8593A Z8593/Z8593A Protopack Emulator

■ Description

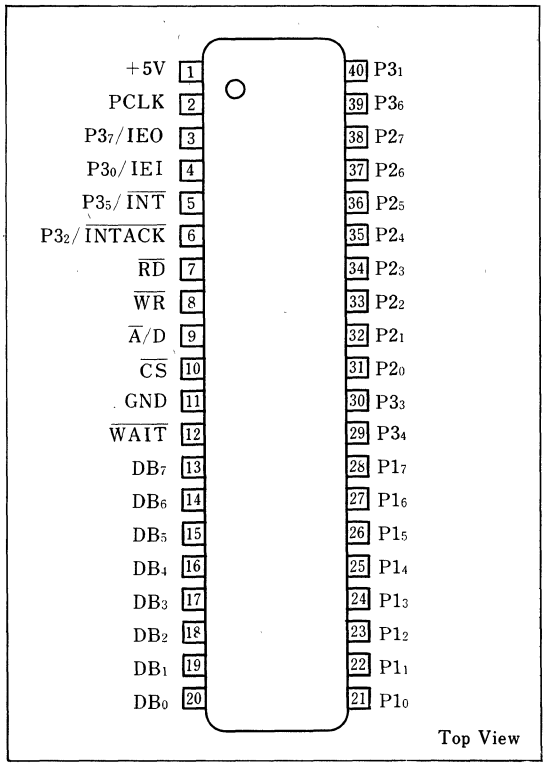
The LH8593 (Z8593) is a ROM less version of the standard LH8590 (Z8590) housed in a pin compatible 40 pin package.

The LH8593 carries a 24-pin soket for a direct interface to program memory. 2716 type EPROM can be used for program memory.

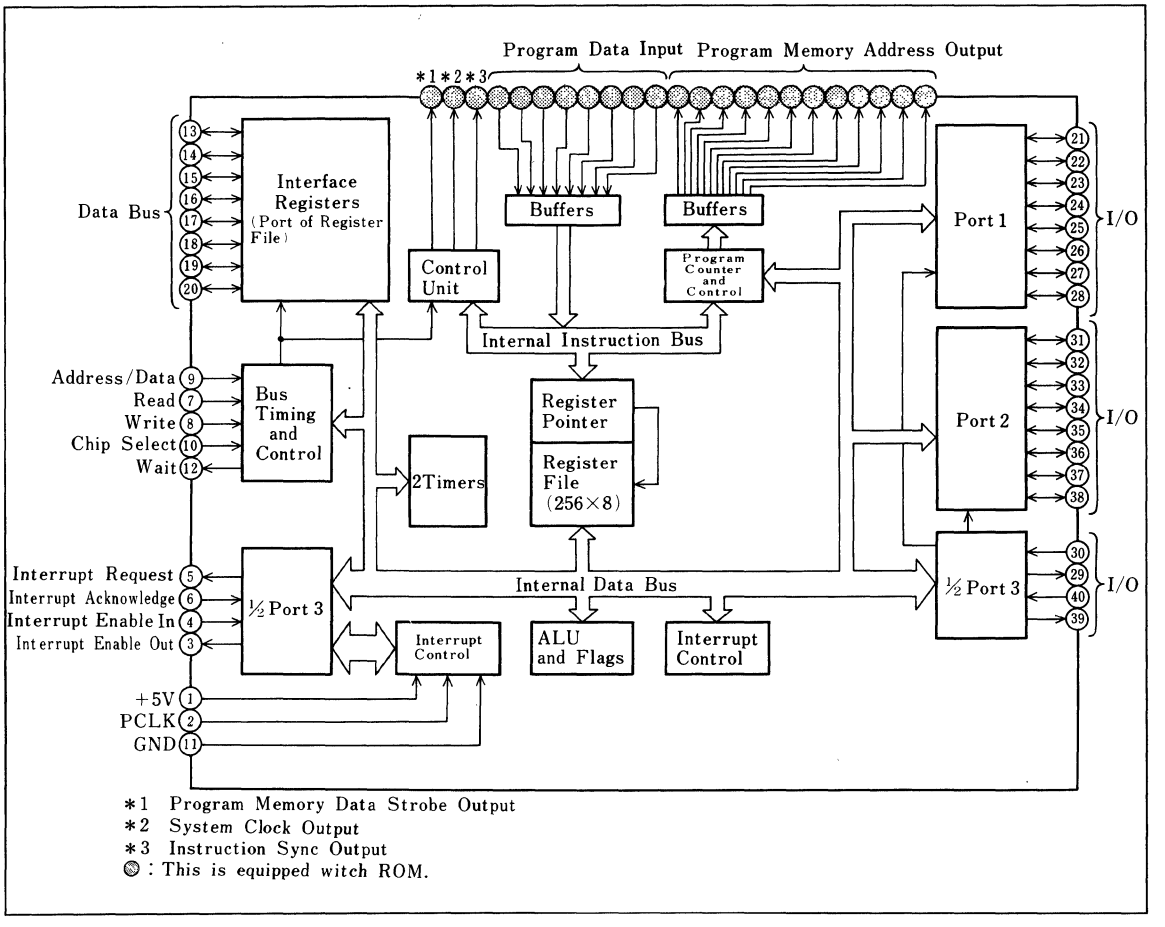
The LH8593 allows the user to build the prototype and pilot production units. When the final program is established, the user can then switch over the LH8590.

The LH8593A is the high speed version which can operate at 6MHz system clock.

■ Pin Connections



■ Block Diagram



■ Pin Description

LH8593 pins are compatible with those of LH8590. For pin description, refer to those of LH8590.

LH8594/LH8594A Z8594/Z8594A Protopack Emulator

■ Description

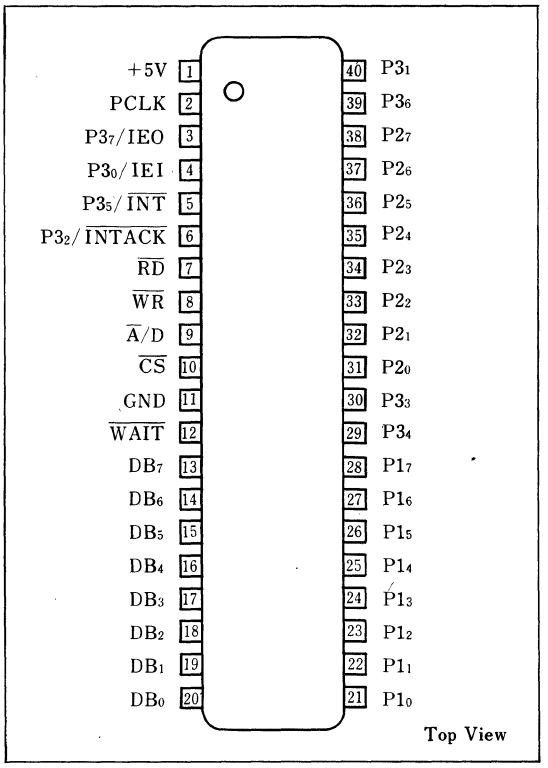
The LH8594(Z8594)is a RAM version(16K bits RAM) of the standard LH8590, housed in a pin compatible 40 pin package.

The LH8594 carries a 24-pin soket for a direct interface to program memory, and has 36 bytes of internal ROM for a bootstrap program.

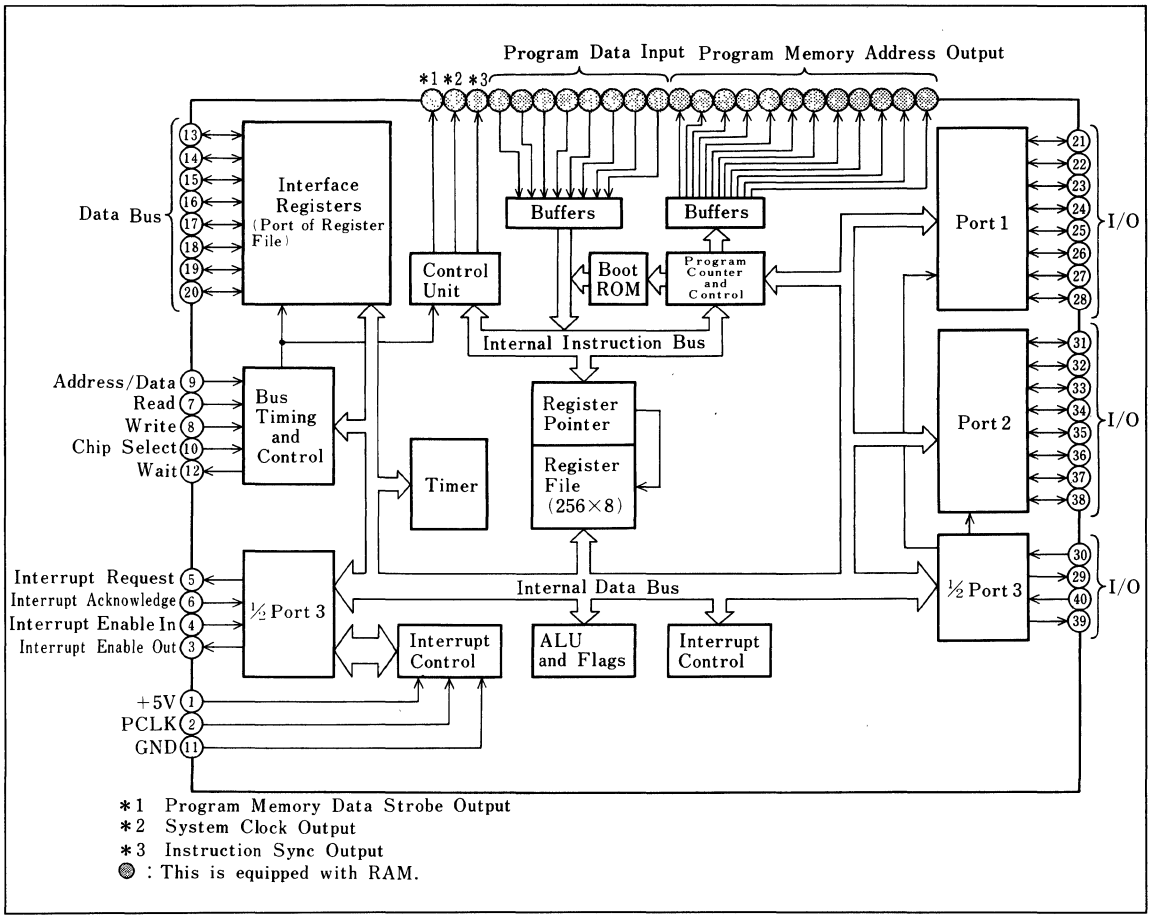
This device allows the user to build the prototype, and when the final program is established, the user can then switch over the LH8590.

The LH8594A is the high speed version which can operate at 6MHz system clock.

■ Pin Connections



■ Block Diagram



■ Pin Description

LH8594 pins are compatible with those of LH8590. For pin description, refer to those of LH8590.

LH8661 Key-encoder and Data Transmitter/Receiver

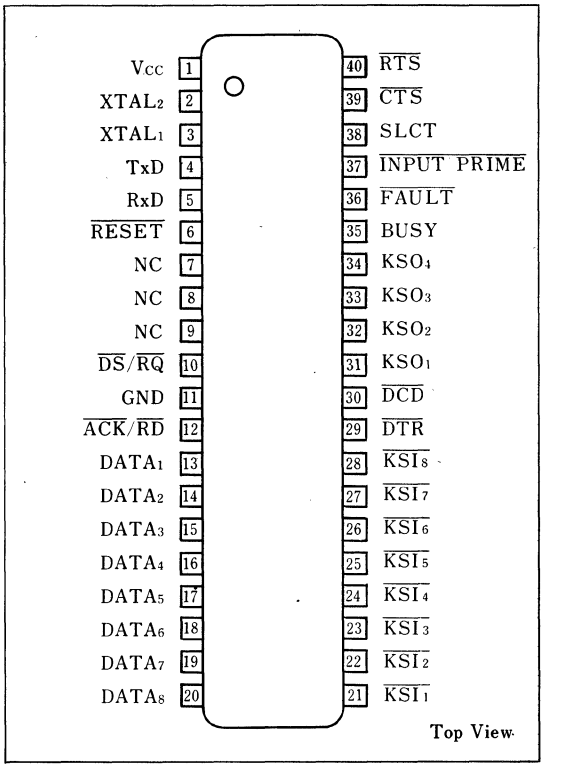
■ Description

The LH8661 is a high performance and multi-purpose interface LSI which has functions such as signal encoding from key matrix circuit, serial data transmission/receiving and parallel data input/output.

The LH8661 can be operated on one of the following five modes:

- Encodes a key matrix signal, and outputs the data to a serial port (Mode 1).
- Encodes a key matrix signal, and outputs the data to a parallel port (Mode 2).
- Encodes a key matrix signal, and outputs the data to both serial and parallel ports (Mode 3).
- Encodes a key matrix signal, and outputs the data to serial port, concurrently, serial input data is converted to parallel and output to a parallel port (Mode 4).
- Parallel input data is converted to serial and output to a serial port (key scanning function is sleep)(Mode 5).

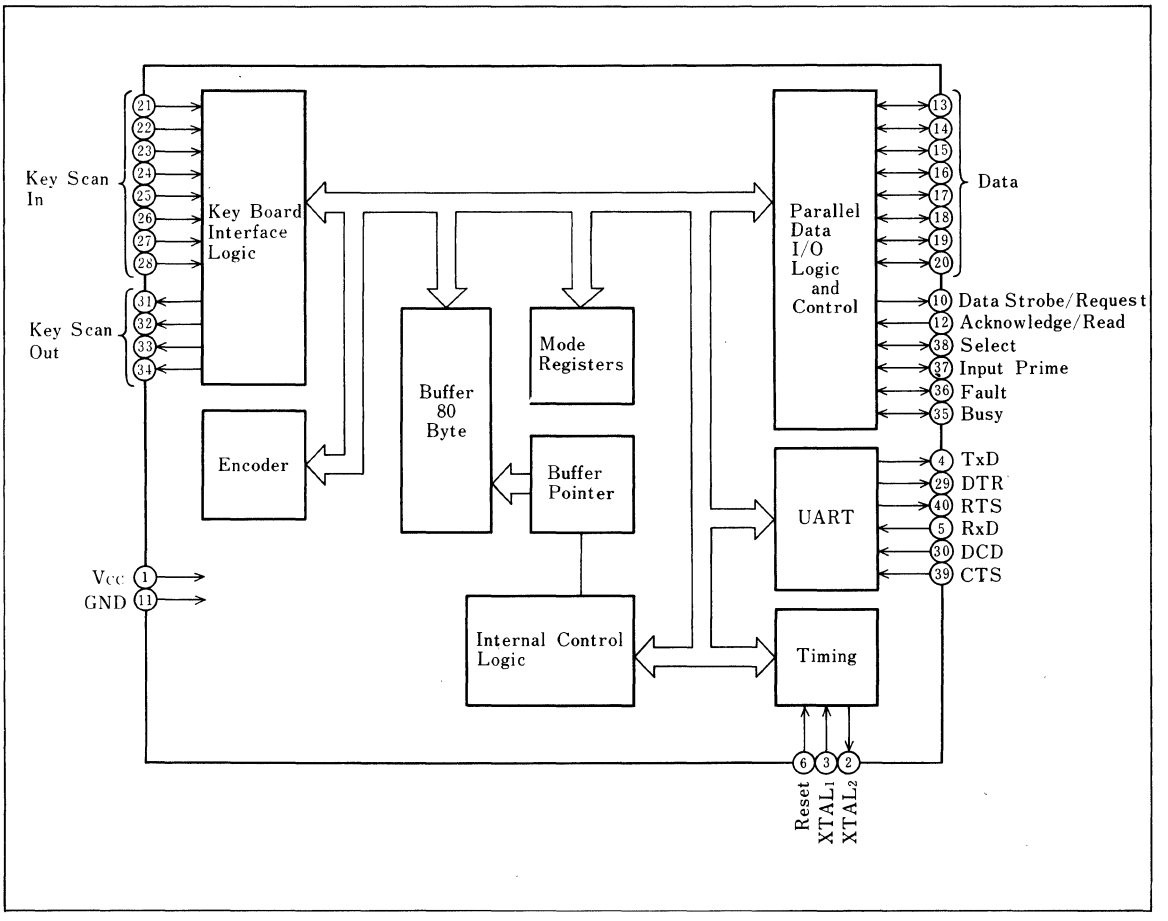
■ Pin Connections



■ Features

1. Key encoding
   - 102 keys compatible with JIS ASCII array can be encoded.
   - Selectable encoding (compatible with JIS 6220-1976 information exchange-code) or no-encoding (native code).
   - Encoded data can be transferred in serial or output in parallel (mono/bi-modes available)
2. Serial data communication
   - Encoded key data can be transferred in asynchronous serial mode.
   - Serial port can be used as an RS232C interface by attaching buffers.
   - Selectable data format (data 7/8, parity, stop bit 1/2).
   - Selectable baud rate (110, 150, 300, 600, 1200, 2400, 4800, 9600, 19200).
3. Parallel data input/output
   - Encoded key data can be output to a parallel port in parallel.
   - Parallel port can be used as a printer interface compatible with Centronics by attaching buffers.
4. Serial/parallel data conversion
   - This device can be used as a serial/parallel data converter with/without a matrix key board.
5. Data buffers 80 bytes×1 or 40 bytes×2.
6. On-chip crystal oscillator circuit.
7. Single+5V power supply
8. 40-pin dual-in-line package

Block Diagram



■ Pin Description

Pin	Meaning	I/O	Function
$\overline{KSI_1}$~$\overline{KSI_8}$	Key scan input	I	Active low. Key scan data signal input
KSO_1~KSO_4	Key scan output	O	Key matrix scanning signal output
$DATA_1$~$DATA_8$	Data bus	Bidirectional 3-State	System data bus
$\overline{DS}/\overline{RQ}$	Data strobe/request	O	Active low. Data strobe signal when mode 1 to 4 is selected; request signal when mode 5 is selected.
$\overline{ACK}/\overline{RD}$	Acknowledge/read	I	Falling edge active. Acknowledge signal when mode 1 to 4 is selected; read signal when mode 5 is selected.
BUSY	Busy	Bidirectional	Active high. Indicate printer busy (input) when mode 1 to 4 is selected; indicate data buffer full (output) when mode 5 is selected.
$\overline{FAULT}$	Fault	Bidirectional	Active low. Indicate printer disable (input) when mode 1 to 4 is selected; indicate data buffer full when mode 5 is selected.
$\overline{INPUT\ PRIME}$	Prime input	Bidirectional	Active low. Output printer initialization signal when in mode 1 to 4; input data buffer pointer initialization signal when in mode 5.
SLCT	Select	Bidirectional	Active high. Input printer select signal when in mode 1 to 4; indicate that parallel data output is available to device when in mode 5.
RxD	Received data	I	Receiving data line.
TxD	Transmitted data	O	Transmitting data line.
$\overline{RTS}$	Transmission request	O	Active Low. Indicate readiness of data transmission.
$\overline{CTS}$	Transmission enable	I	Active Low. Indicate data transmission enabled.
$\overline{DTR}$	Data terminal ready	O	Active Low. Data transmission request signal.
$\overline{DCD}$	Reception enable	I	Active Low. Indicate data reception enabled.
$\overline{RESET}$	Reset input	I	Active Low initialization input.
$XTAL_1$ $XTAL_2$	Crystal	Bidirectional	7.3728 MHz crystal oscillator connected.

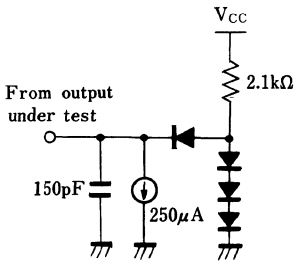
■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V_{IN}	−0.3~+7.0	V
Output voltage	V_{OUT}	−0.3~+7.0	V
Operating temperature	T_{opr}	0~+70	℃
Storage temperature	T_{stg}	−65~+150	℃

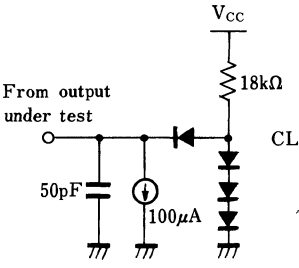
■ DC Characteristics

(V_{CC}=5V±5%, Ta=0~+70℃)

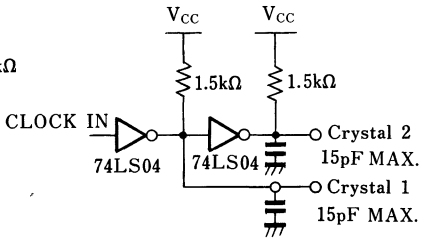
Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Clock input high voltage	V_{CH}	Driven by external clock.	3.8	V_{CC}	V	
Clock input low voltage	V_{CL}	Driven by external clock.	−0.3	0.8	V	
Input high voltage	V_{IH}		2.0	V_{CC}	V	
Input low voltage	V_{IL}		−0.3	0.8	V	
Reset input high voltage	V_{RH}		3.8	V_{CC}	V	
Reset input low voltage	V_{RL}		−0.3	0.8	V	
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4		V	
Output low voltage	V_{OL}	I_{OL}=2mA		0.4	V	
Input leakage current	I_{IL}	$0 \leqq V_{IN} \leqq +5.25V$	−10	10	μA	
Output leakage current	I_{OL}	$0 \leqq V_{IN} \leqq +5.25V$	−10	10	μA	
Reset input current	I_{IR}	V_{CC}=5.25V, V_{RL}=0V		−50	μA	
Supply current	I_{CC}			180	mA	



Test load 1



Test load 2



External C. G. circuit

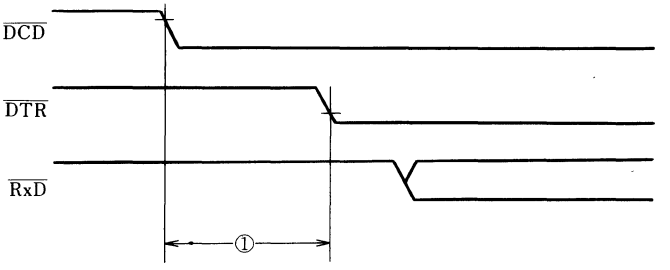
■ AC Characteristics

(1) Serial port timing

(i) Reception

(V_{CC} = 5 V ±5%, OSC freq. = 7.3728 MHz, Ta = 0 to +70°C)

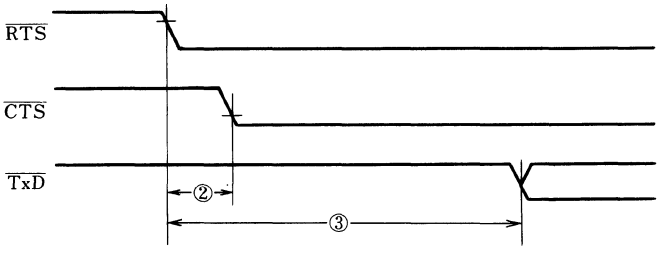
No.	Parameter	Symbol	MIN.	MAX.	Unit	Note
①	Time from $\overline{DCD}$ ↓ to $\overline{DTR}$ signal output	Tb $\overline{DCD}$($\overline{DIR}$)	15		μs	



(ii) Transmission

(V_{CC} = 5 V ±5%, OSC freq. = 7.3728 MHz, Ta = 0 to +70°C)

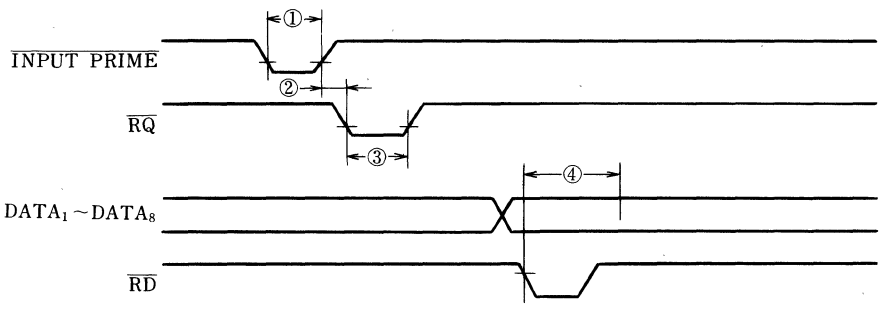
No.	Parameter	Symbol	MIN.		Unit	Note
②	Time from $\overline{RTS}$ ↓ to $\overline{CTS}$ signal acknowledge	Td $\overline{RTS}$($\overline{CTS}$)	2.7		μs	
③	Time from $\overline{RTS}$ ↓ to data (TxD) output	Td $\overline{RTS}$(TxD)	25		μs	



(2) Parallel port timing

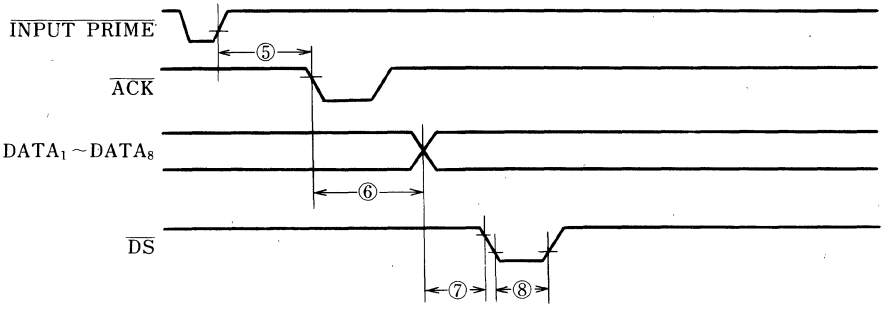
(i) Input (Vcc=5 V ±5%, OSC freq.=7.3728 MHz, Ta=0 to+70°C)

No.	Parameter	Symbol	MIN.	MAX.	Unit	Note
①	$\overline{\text{INPUT PRIME}}$ pulse width	Tw $\overline{\text{IP}}$	7.0		μs	
②	Time from $\overline{\text{INPUT PRIME}}$ ↑ to $\overline{\text{RQ}}$ signal output	Td $\overline{\text{IP}}$ ($\overline{\text{RQ}}$)		13.8	μs	
③	$\overline{\text{RQ}}$ pulse width	Tw $\overline{\text{RQ}}$	4.3		μs	
④	Data settlement time from $\overline{\text{RD}}$ ↓	Tr $\overline{\text{RD}}$ (D)	16		μs	



(ii) Output (Vcc=5 V±5%, OSC freq. =7.3728 MHz, Ta=0 to+70°C)

No.	Parameter	Symbol	MIN.	MAX.	Unit	Note
⑤	Time from $\overline{\text{INPUT PRIME}}$ ↑ to $\overline{\text{ACK}}$ ↓	TdIP($\overline{\text{ACK}}$)	5.0		μs	
⑥	Time from $\overline{\text{ACK}}$ ↓ to data output	Td$\overline{\text{ACK}}$(D)	23		μs	
⑦	Time from data to $\overline{\text{DS}}$ ↓	TdD($\overline{\text{DS}}$)	5.4		μs	
⑧	$\overline{\text{DS}}$ pulse width	Tw$\overline{\text{DS}}$	2.6		μs	



■ Operation Mode Setting

The LH8661 is available in five operation modes which are obtained by combining the key data encode, parallel data transfer, and serial data transfer functions (Fig.1). An Operation mode is selected with mode switches (MODE1-MODE4) which control the scan signal, $\overline{\text{SCAN}}_1$, and key scan input signals, $\overline{\text{KSI}}_5$-$\overline{\text{KSI}}_8$.

■ Key Matrix Configuration

The key matrix consists of key scan input signals ($\overline{\text{KSI}}_1$-$\overline{\text{KSI}}_8$) and scan signals ($\overline{\text{SCAN}}_1$-$\overline{\text{SCAN}}_{16}$). The matrix requires status control circuit (switches plus diodes) in addition to the maximum 102 types of keyboard switches.

The status control circuit should consist of operation mode selector, transmit data format selector, and baud rate selector. The LH8661's operation mode is selected by these settings.

The compatible keyboard types, their configuration and status control switches on the key matrix and shown in Fig. 3. Conformity of key data to the JIS code requires the key arrangement shown in Fig. 2. The status control circuit should consist of the $\overline{\text{SCAN}}_1$-$\overline{\text{SCAN}}_2$ and key scan input signals ($\overline{\text{KSI}}_1$-$\overline{\text{KSI}}_8$). (Note. Shaded sections in the fig. are not usable.)

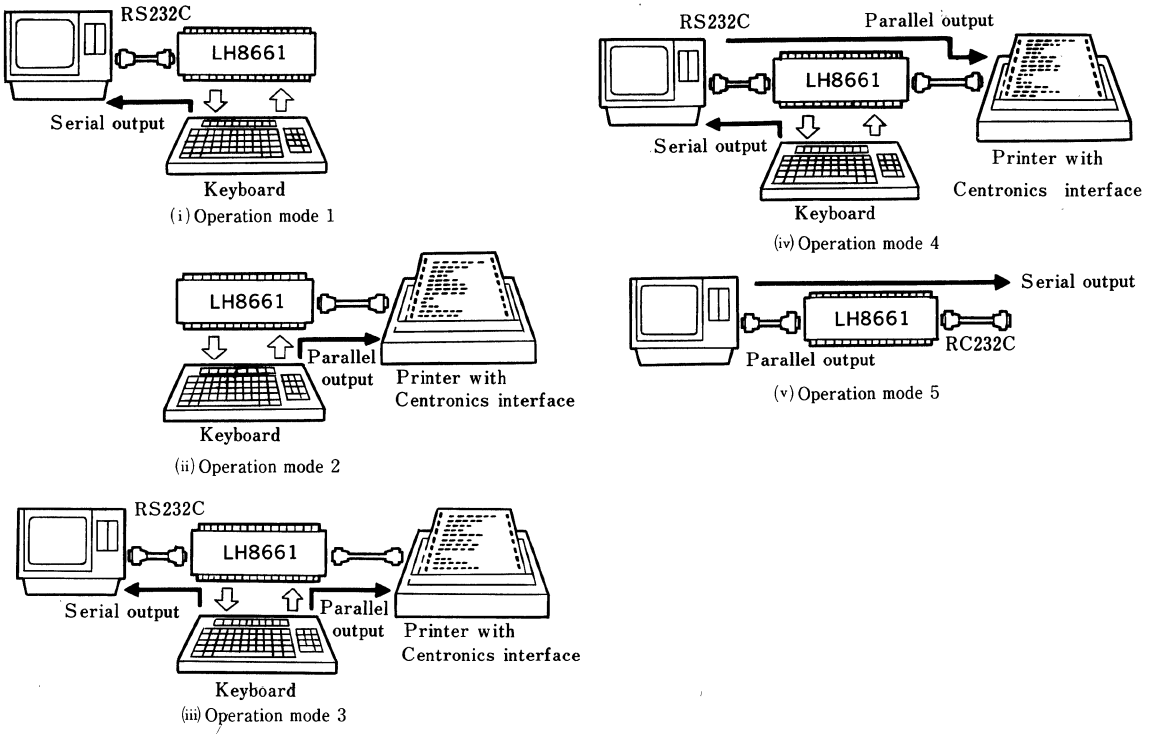
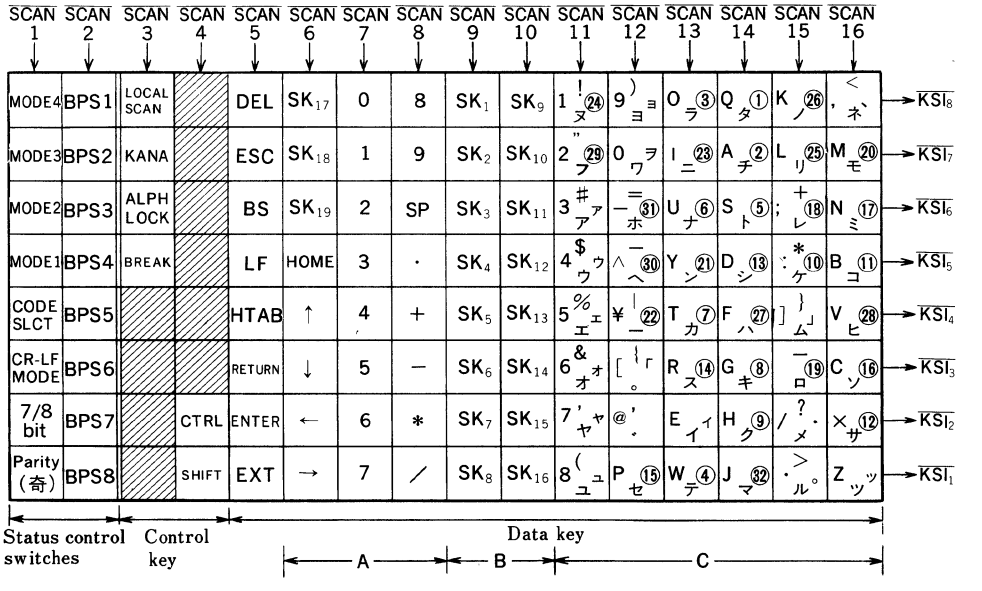


Fig. 1 Description of device operation modes



Note 1 : A, B and C are local scan blocks
Note 2 : Shaded sections in the diagram are not usable

Alphanumeric section (SI) — KANA section (SO)

Fig. 2 Key types and key arrangement

■ Keyboard Matrix

(1) Key types and arrangement

The LH8661 is capable of encoding data from up to 102 types of keys arranged on a key matrix which consists of key scan input signals, $\overline{KSI_1}$-$\overline{KSI_8}$, and scan signals, $\overline{SCAN_3}$-$\overline{SCAN_{16}}$. The 102 types of keys are divided into the following two blocks:

① Data key block: Consists of 96 keys arranged on the matrix composed of scan signals $\overline{SCAN_5}$-$\overline{SCAN_{16}}$ and key scan input signals $\overline{KSI_1}$-$\overline{KSI_8}$. When the JIS code system is selected (code select switch at OFF), key data is encoded into the transmit character codes shown in Fig. 5. In this case the key arrangement shown in Fig. 3 is required. When the native code system is selected (code select switch at ON), key data is encoded into the transmit character codes as shown in Fig. 6.

② Control key block: Consists of six keys on the matrix which is composed of scan lines $\overline{FCAN_3}$-$\overline{SCAN_4}$ and key scan input signals $\overline{KSI_1}$-$\overline{KSI_8}$. These keys are used to control data key encoding and key scanning. The shaded portion of the control key block shown in Fig. 2 is not usable.

(2) Transmit character codes

The LH8661 can encode key data into JIS or native codes. Fig. 4 shows the transmit character codes that conform to the JIS C 6220-1976 Information Exchanging Codes. Fig. 5 shows the native transmit character codes. The following figure shows typical combinations of keyface symbols in the alphanumeric and Kana sections of a key.

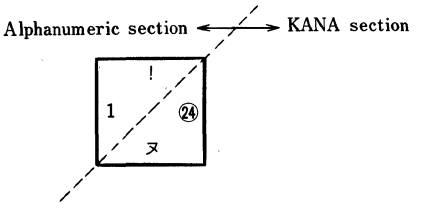


Fig. 3 Keyface symbols

(3) Key entry operations

The LH8661 supports the following key entry features:

- Key contact bounce time of approx. 5 ms.
- Two-key rollover and N-key lockout.
- Typamatic capability

If any data key other than those listed below is

Output code ·····(b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0)

					(S1)								(S0)							
			b_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
			b_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			b_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			b_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
b_3	b_2	b_1	b_0	Col/Row	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0	0			SP	0	@	P	'	p	SK_{16}	SK_1	SP	—	タ	ミ	①	⑰
0	0	0	1	1			!	1	A	Q	a	q		SK_2	。	ア	チ	ム	②	⑱
0	0	1	0	2			"	2	B	R	b	r		SK_3	「	イ	ツ	メ	③	⑲
0	0	1	1	3	ETX		#	3	C	S	c	s		SK_4	」	ウ	テ	モ	④	⑳
0	1	0	0	4			$	4	D	T	d	t		SK_5	、	エ	ト	ヤ	⑤	㉑
0	1	0	1	5			%	5	E	U	e	u		SK_6	・	オ	ナ	ユ	⑥	㉒
0	1	1	0	6			&	6	F	V	f	v		SK_7	ヲ	カ	ニ	ヨ	⑦	㉓
0	1	1	1	7			'	7	G	W	g	w		SK_8	ァ	キ	ヌ	ラ	⑧	㉔
1	0	0	0	8	BS		(	8	H	X	h	x		SK_9	ィ	ク	ネ	リ	⑨	㉕
1	0	0	1	9	HTAB		)	9	I	Y	i	y		SK_{10}	ゥ	ケ	ノ	ル	⑩	㉖
1	0	1	0	A	LF		*	:	J	Z	j	z		SK_{11}	ェ	コ	ハ	レ	⑪	㉗
1	0	1	1	B		ESC	+	;	K	[	k	{			ォ	サ	ヒ	ロ	⑫	㉘
1	1	0	0	C			,	<	L	¥	l	|		SK_{12}	ャ	シ	フ	ワ	⑬	㉙
1	1	0	1	D	CR		−	=	M	]	m	}		SK_{13}	ュ	ス	ヘ	ン	⑭	㉚
1	1	1	0	E	SO		.	>	N	^	n	‾		SK_{14}	ョ	セ	ホ	゛	⑮	㉛
1	1	1	1	F	SI		/	?	O	−	o	DEL		SK_{15}	ッ	ソ	マ	°	⑯	㉜

↑	ESC(1B$_H$)+A(41$_H$)
↓	ESC+B(42$_H$)
→	ESC+C(43$_H$)
←	ESC+D(44$_H$)
HOME	ESC+H(48$_H$)
SK_{17}	ESC+E(45$_H$)
SK_{18}	ESC+J(4A$_H$)
SK_{19}	ESC+K(4B$_H$)

Fig. 4 Transmit character codes (1) ··· JIS codes

Output code ·····(b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0)

				b_3	0	0	0	0	1	1	1	1	1	1	1	1
				b_2	1	1	1	1	0	0	0	0	1	1	1	1
				b_1	0	0	1	1	0	0	1	1	0	0	1	1
				b_0	0	1	0	1	0	1	0	1	0	1	0	1
b_7	b_6	b_5	b_4	Col/ Row	4	5	6	7	8	9	A	B	C	D	E	F
0 1	0	0	0	0	EXT	→	7	/	SK_8	SK_{16}	8 (ュ	P ⑮ セ	W ④ テ	J ㉜ マ	・ > ° ル	Z ッ ツ
0 1	0	0	1	1	ENTER	←	6	*	SK_7	SK_{15}	7 ' ャ ヤ	@ ` ・	E イ ィ	H ⑨ ク	/ ? ・ メ	X ⑫ サ
0 1	0	1	0	2	RETURN	↓	5	−	SK_6	SK_{14}	6 & オ	[｢ ｡	R ⑭ ス	G ⑧ キ	ー ⑲ ロ	C ⑯ ソ
0 1	0	1	1	3	HTAB	↑	4	+	SK_5	SK_{13}	5 % ェ エ	¥ ｜ ㉒ ー	T ⑦ カ	F ㉗ ハ	] ｣ ム	V ㉘ ヒ
0 1	1	0	0	4	LF	HOME	3	·	SK_4	SK_{12}	4 $ ぅ ウ	^ ㉚ ヘ	Y ㉑ ン	D ⑬ シ	: * ⑩ ケ	B ⑪ コ
0 1	1	0	1	5	BS	SK_{19}	2	SP	SK_3	SK_{11}	3 # ァ ア	= ㉛ ホ	U ⑥ ナ	S ⑤ ト	; + ⑱ レ	N ⑰ ミ
0 1	1	1	0	6	ESC	SK_{18}	1	9	SK_2	SK_{10}	2 " ㉙ フ	0 ヲ ワ	1 ㉓ ニ	A ② チ	L ㉕ リ	M ⑳ モ
0 1	1	1	1	7	DEL	SK_{17}	0	8	SK_1	SK_9	1 ! ㉔ ヌ	9) ョ ヨ	O ③ ラ	Q ① タ	K ㉖ ノ	, < 、 ネ

Note : b_7=1 when KANA key is ON, b_7=0 when off.

Fig. 5 Transmit character codes (2)...Native codes

pressed and held for more than 1 second when the JIS code sytem is selected, the corresponding transmit character code is repeatedly entered at a frequency of approx. 20 Hz. When the native code system is selected, all the 96 data keys are effective for the auto repeat function.

DEL ESC BS LF HTAB RETURN ENTER ETX

The above control keys are not effective for the auto repeat function.

■ Serial Data Transfer

The LH8661 transmits serial data via RS232C interface when in modes 1, 3, or 5. It can transmit and receive serial data when in mode 4.

The serial data format can be selected from 7 bits with parity, 7 bits with no parity (b_7 fixed at '0'), and 8 bits with no parity. Selection is executed with bit 7 or 8 and with parity switch (see description of transfer data format setting).
Fig. 6 shows the serial data format.

(1) Transmit mode

The LH8661 automatically adds one start bit and two stop bits to transmit data. It holds TxD at high to maintain mark status between characters.

(2) Receive mode

Receive data must have one start bit, eight data bits, and at least one stop bit. While the receiver has a two-stage buffer, data will not be protected in the event of an overrun.

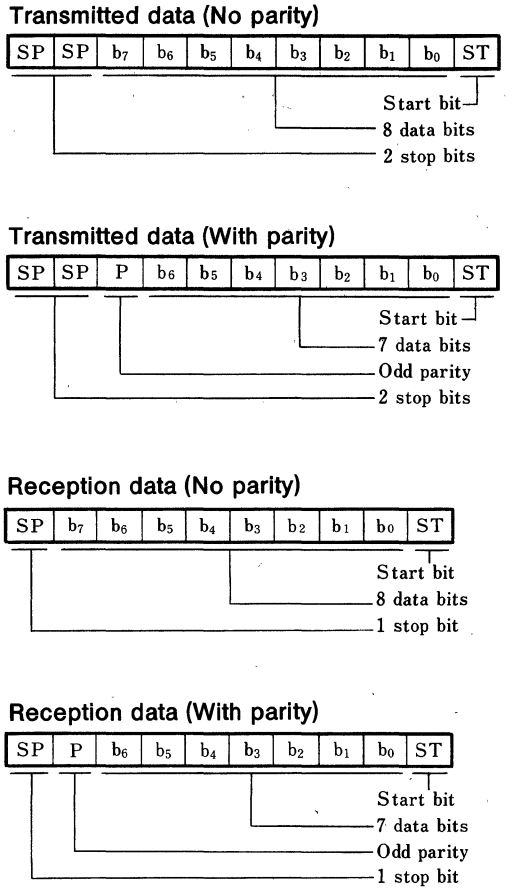


Fig. 6 Serial data format

■ Parallel Data Transfer

When in modes 2, 3, and 4, the LH8661 can transfer parallel data to a printer having Centronics interface. When in mode 5, it can receive parallel data through Centronics interface.

(1) Centronics interface (parallel data transmission)

The LH8661 maintains $\overline{\text{INPUT PRIME}}$ at low for a given time period after being reset. The attached printer usually uses this signal to initialize its internal circuitry. The LH8661 then tests the SLCT and $\overline{\text{FAULT}}$ inputs to see whether or not the printer is ready for operation. When transmitting data, the device also tests for BUSY signals from the printer. When signal is at high, the printer is busy printing and the device waits for the printer to become ready. When the printer returns to the ready status, it resets the BUSY signal to low and sets the ACKNLG signal at high. Seeing that the $\overline{\text{ACK}}$ signal (inverse of ACKLNG) is set to active low, the LH8661 transmits print data. It then sets the $\overline{\text{DS}}$ signal to low a given time period after completing data transmission. The printer uses the $\overline{\text{DS}}$ signal to read the data on the data bus ($DATA_1$-$DATA_8$) and prints it.

The data transmission timing is shown in Fig. 7.

(2) Parallel data reception

When the LH8661 is placed in mode 5, the parallel data port becomes a Centronics input port. Input data received through this port can be output in serial form after being subject to parallel-to-serial conversion. The control signal SLCT is set to high when the LH8661 settles in mode 5.

In receiving parallel data, the $\overline{\text{INPUT PRIME}}$ signal must be set to low for a given time period.

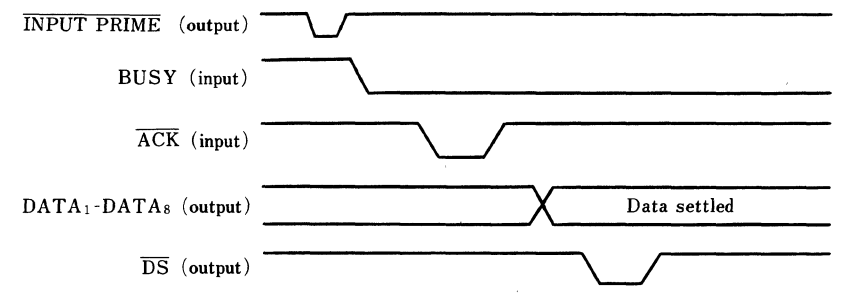


Fig. 7 Parallel port output timing

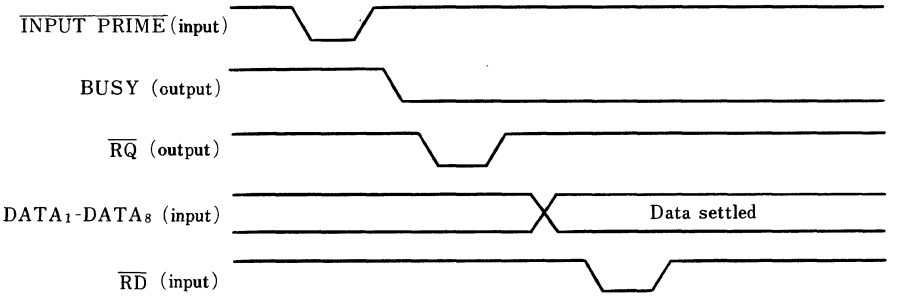


Fig. 8 Parallel port input timing

Receiving this low transition signal , the LH8661 responds by initializing the data buffer pointer and setting both the BUSY and $\overline{RQ}$ signals to low.

Seeing that the ACKLNG signal is set to high, the data output device outputs data, then sets the $\overline{DATA\ STROBE}$ signal to low after a given time period. The LH8661 uses this signal to read data off the data bus ($DATA_1$-$DATA_8$). The LH8661 then sets the $\overline{RQ}$ signal to low to repeat data read operation until the data buffer becomes full.

When the data buffer becomes full, the LH8661 activates the BUSY and $\overline{FAULT}$ signals to inform the output device. The parallel port input timing is shown in Fig. 8.

■ Data Buffer

The LH8661 has a built-in 80-byte RAM for data buffer, which is used to hold key entry data, serial input data or parallel input data.

When the device is in mode 1, 2, or 3, the full 80-byte length of the buffer is used to hold key entry data. When the device is in mode 4, the buffer is divided into a 40-byte segment to hold key entry data and another 40-byte segment to hold serial input data. When in mode 5, the full 80-byte length of the buffer is used to hold parallel input data.

When the buffer becomes full, the LH8661 behaves as follows:

- No longer writes key entry data into the buffer.
- During serial data input, sets the $\overline{DTR}$ signal to high to indicate buffer-full status to the data output device (having RS-232C interface). The LH8661 accepts no serial data transferred while the $\overline{DTR}$ is at high.
- During parallel data input, activates the BUSY and $\overline{FAULT}$ signals to indicate buffer-full status to the parallel data output device. The LH8661 outputs no $\overline{RQ}$ signal while the BUSY and $\overline{FAULT}$ signals are active.

Support Tools for Micrcomputers

LH8DH110 Development Support System SM-D-8000 II

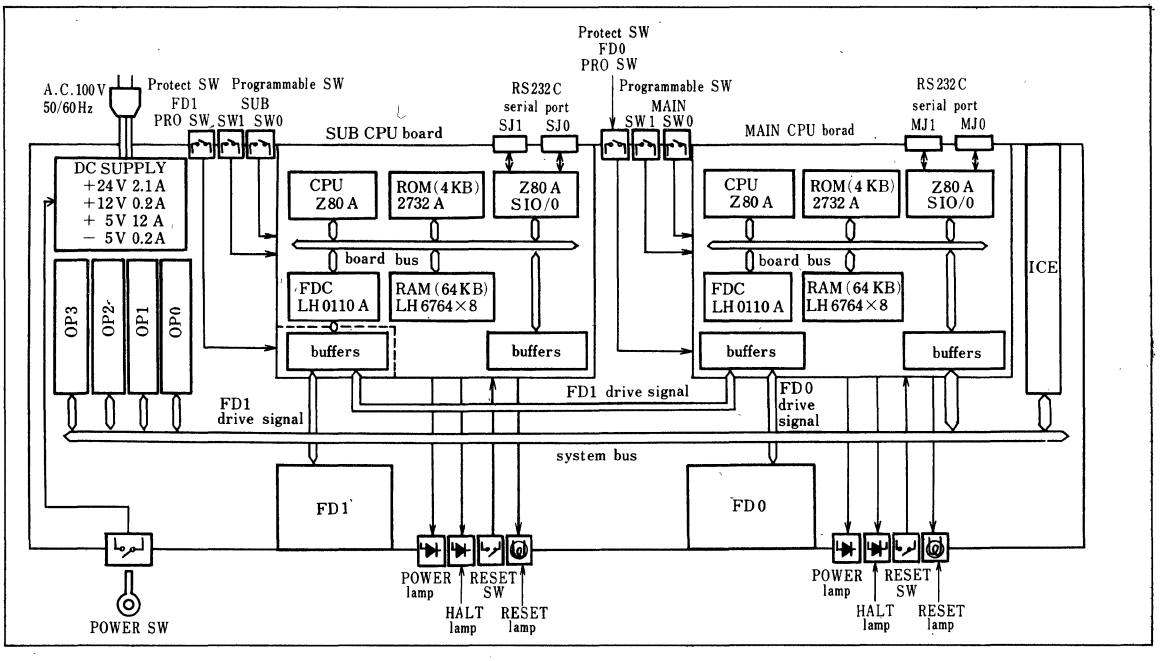
■ Description

This system operates under control of the floppy disk operating system (FDOS), and incorporates software for developing Z80 application programs. The software includes a relocatable macro assembler, a text editor, and a debugger. The system facilitates Z80 software development and minimizes developing time. In addition, program developing software for Z8, Z8000 and SM series can also be used in this system. The system can also be an aid for developing Z80A and Z8 systems by connecting the In-circuit Emulator (Z80A or Z8) to the system. In conjunction with a PROM writer, the system writers EPROMs directly further reducing developing time.

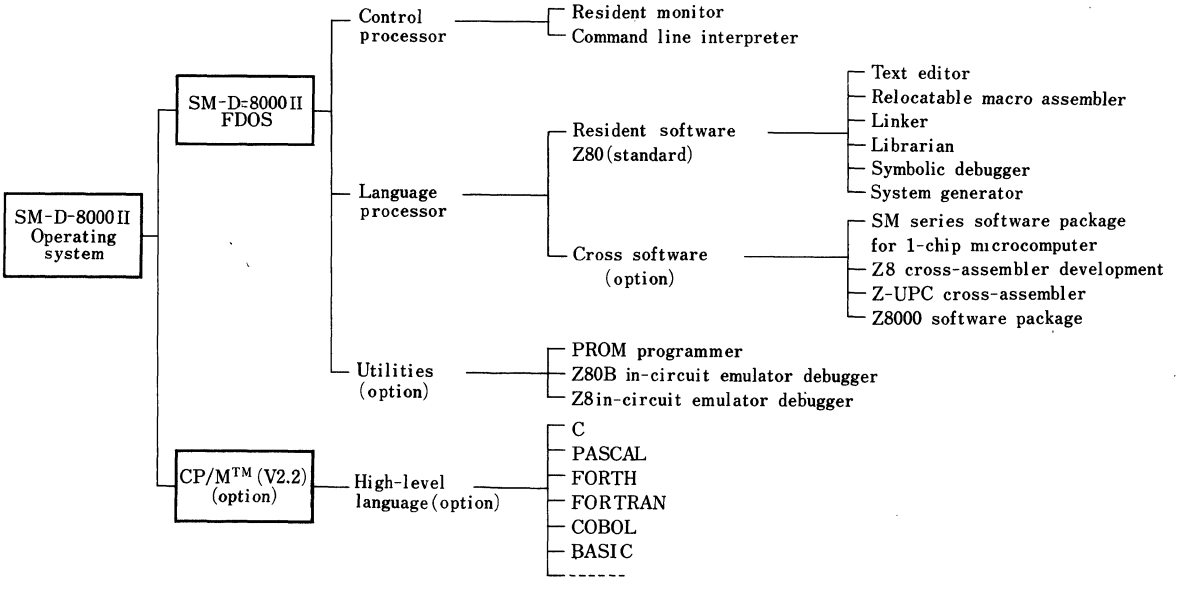
■ Features

1. Z80A CPU (clock frequency : 4MHz)
2. RAM : 64K bytes
3. Two double-sided double-density floppy disk drives in standard (capacity : 2M bytes)
4. RS232C 2ports
   20mA curren loop 1port
   (shared with RS232C port)
   Baud rate 110～19200B
   (9 levels selective)
5. Optional hardware
   PROM writer
   Z8/Z80B In-circuit Emulator etc.

■ Block Diagram



■ Software Organization



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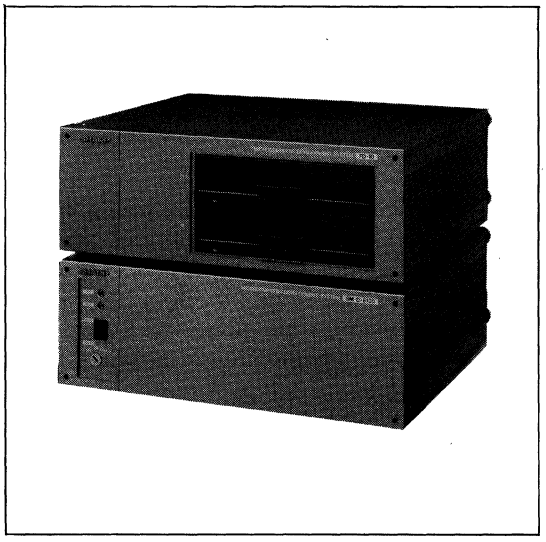
LH8DH130 Development Support System SM-D-8100

■ Description

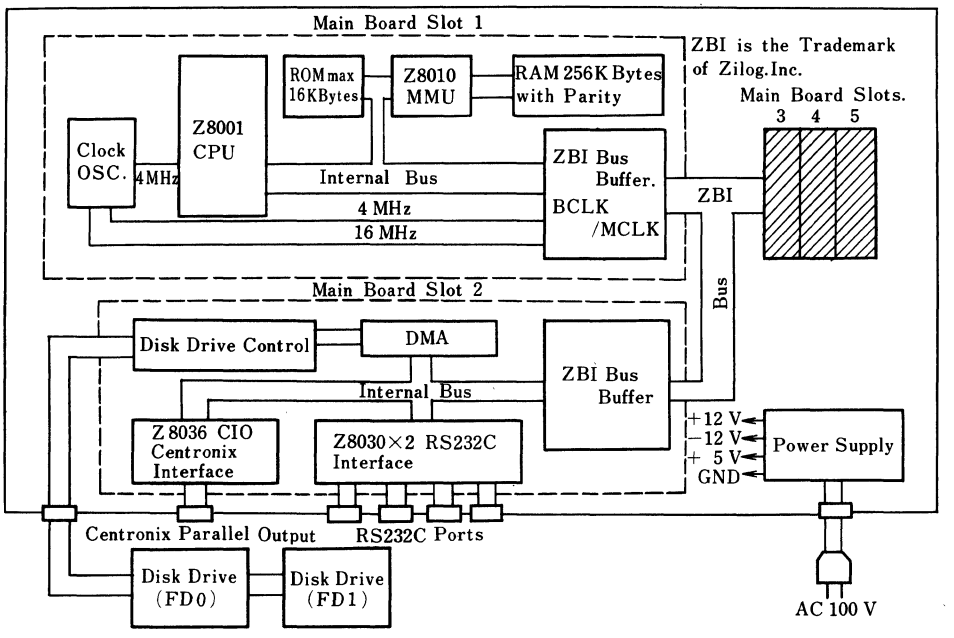
This system in based on the Z8001 CPU and operates under control of the floppy disk operating system (SM-DOS8100). The system provides a standard set of software for developing Z8000 programs. There include C compiler, relocatable macro assembler, text editor and linker for cost effective software development. The SM-D-8100 consists of main unit and a floppy disk drive unit. The main unit is provided with four RS232C ports so that the system can be connected to other devices. The system has 256K-byte of RAM for flexible upgrading in the future.



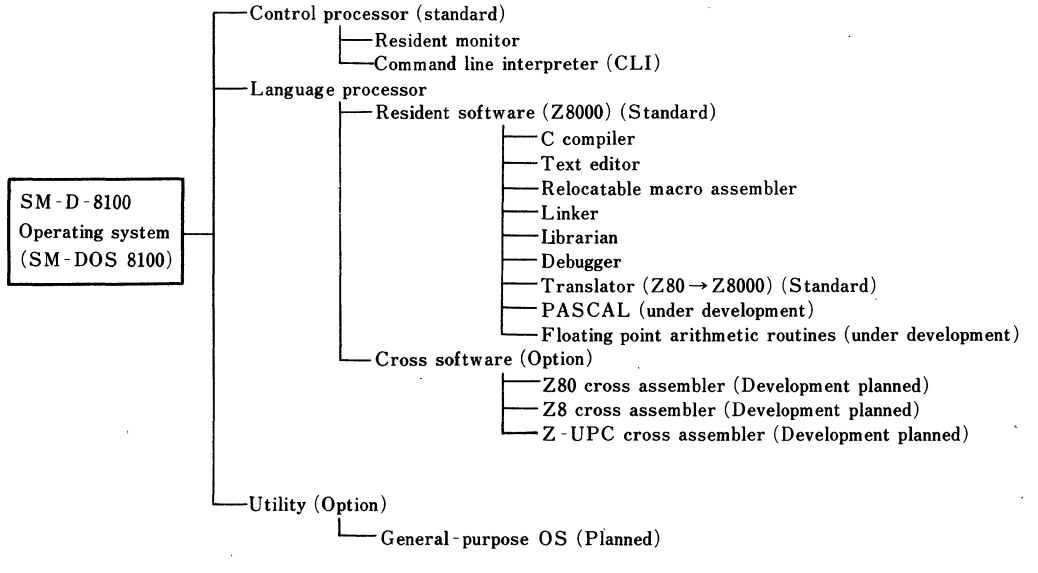
■ Features

1. Z8001 CPU (clock frequency : 4MHz)
2. RAM : 256K bytes (1 parity bit per 8-bit)
3. Two double-sided double-density floppy disk drives in standard (separate unit), (Capacity: 2M bytes)
4. Four RS232C ports Baud rate : 110～19200B (9 levels selective for each port)
5. Centronics parallel output port
6. High-grade language, C compiler in standard
7. Optional hardware :
   SM-E-8100 In-circuit Emulator

■ Block Diagram



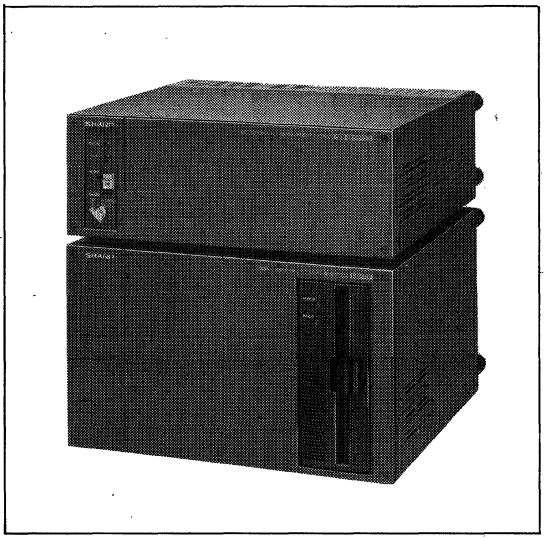
■ Software Organization



LH8DH140 Development Support System SM-D-8200

■ Description

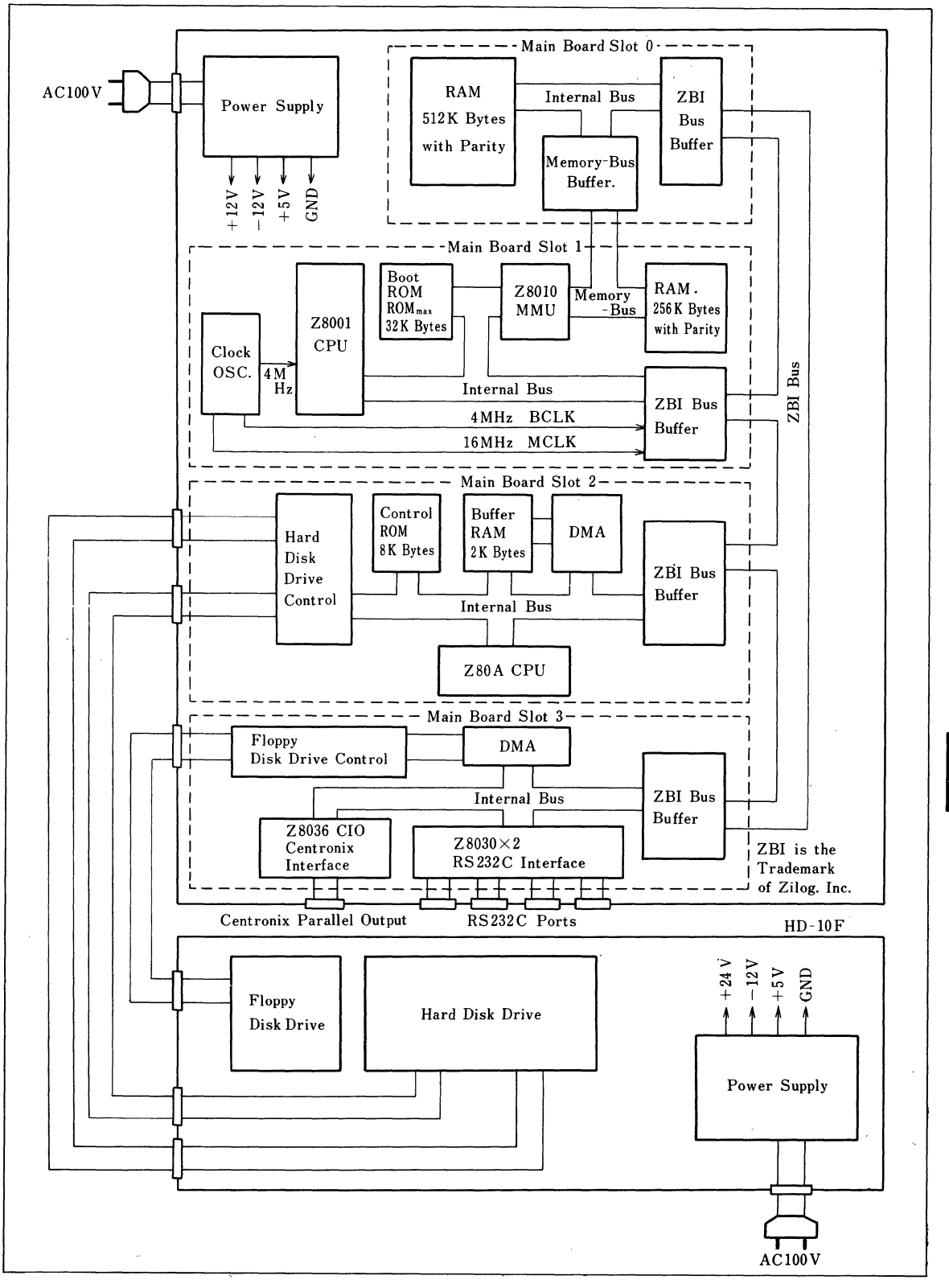
LH8DH140 is a microcomputer system using the Z8001CPU. It is used as the microcomputer development support device or as the general-purpose microcomputer system, with the SM-UX8000 general-purpose operating system mounted, which is based on the system of Bell Laboratories.



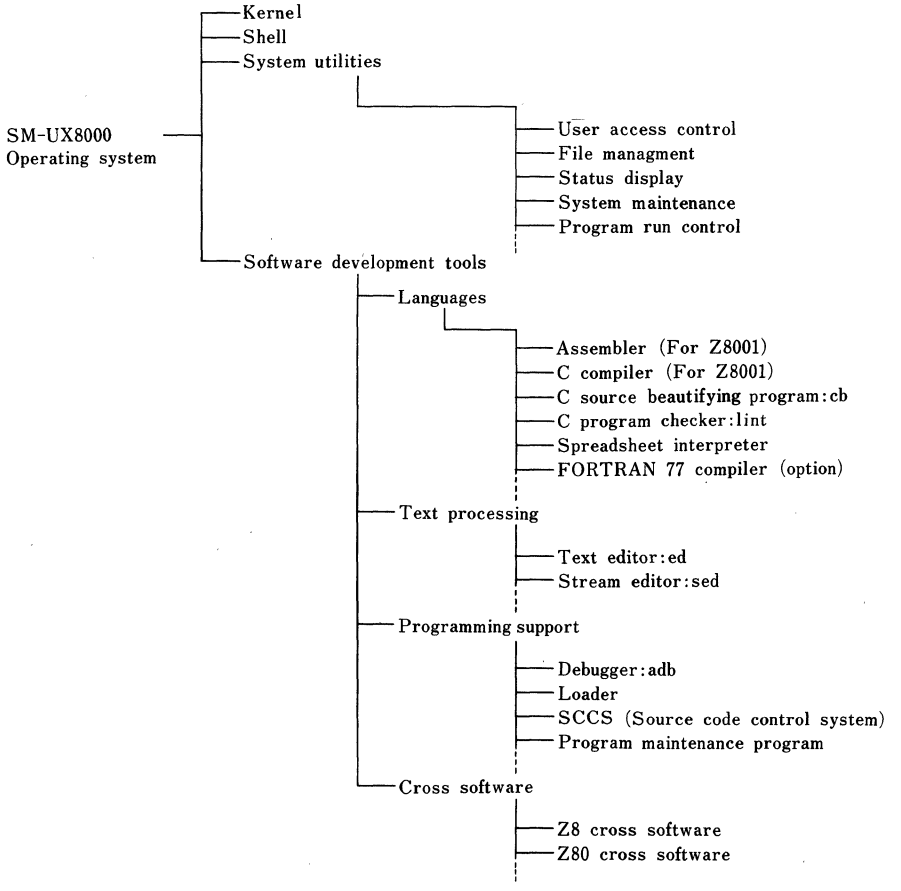
■ Features

1. Main memory function
   - 768K byte RAM
   - 1 parity bit for each 8 bits
   - Memory management function
2. Supplementary memory function
   - Hard disc drive : 1
     Winchester type, 8 inch, 20M bytes
   - Floppy disc drive : 1
     for back up of hard disc equipment
     double-side double-density, 8-inch, 1M bytes
3. I/O interface
   - Serial I/O interface: 4 ports
     RS232C compatible
     Baud rate: 110～9600 for each port
   - Parallel I/O interface : 1-port
     Centronice compatible
4. Optional hardware
   - Z8000 in-circuit emulator (SM-E-8100)
   - Z8000 evaluation board
   - Z8 in-circuit emulator

Block Diagram



Software Organization



LH8DH312 Z80B In-Circuit Emulator

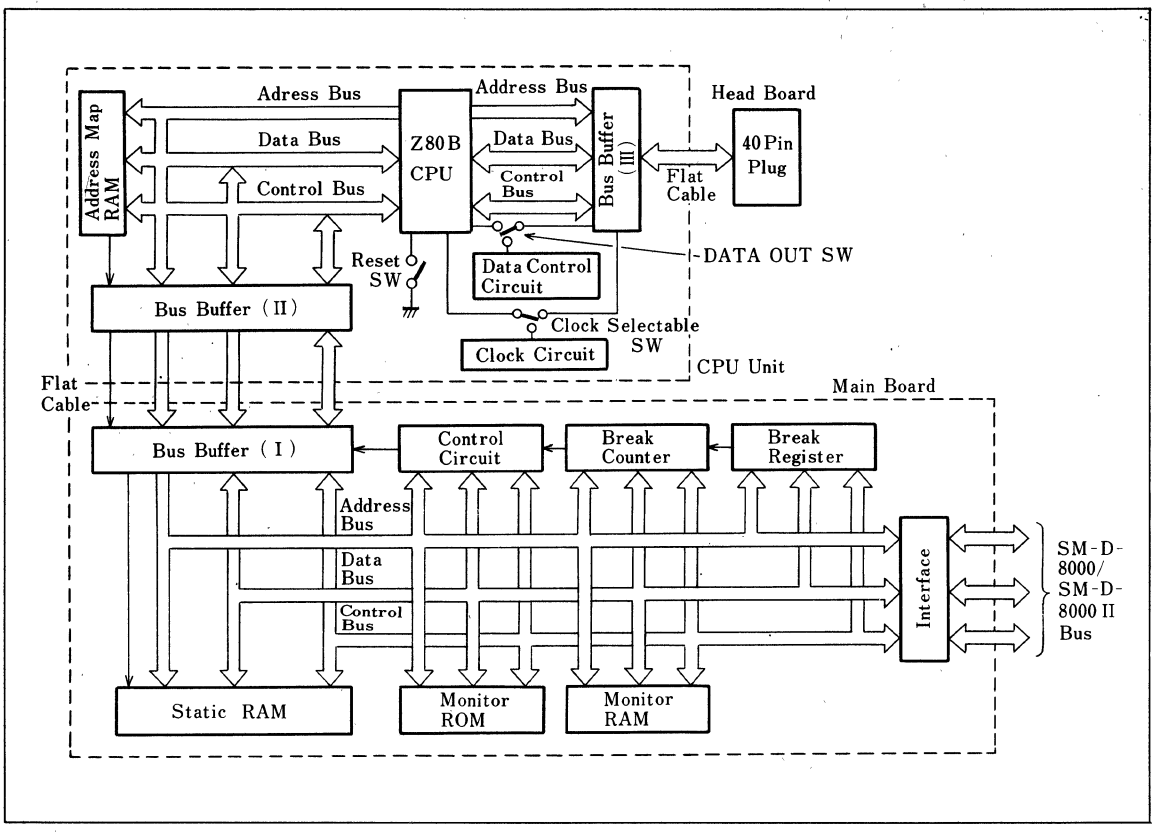
■ Description

This is an SM-D-8000 II option, which provides emulation functions for Z80B systems. The emulator operates under the control of FDOS. It facilitates debugging and reduces development time and costs.

■ Features

1. Support Z80B (6MHz) system
2. Real-time emulation
3. User system memory : 64K bytes
4. User I/O port: 256 ports
5. Memory address mapping function (unit:4K bytes)
6. Hardware break point: 2 (with 16-bit counter)
7. User system RAM: 64K-byte static RAM
8. In-circuit emulator debugger
9. Execution modes of user program
   (i) Real-time
   (ii) 1 step (number of steps can be set)
   (iii) Trace
   (iv) Snapshot
10. Program can be change at mnemonic.
11. I/O device if the user system can read the RETI instruction in the user RAM.
12. All the interrupts (NMI,mode 0,1,2) can be used by the user.

■ Block Diagram



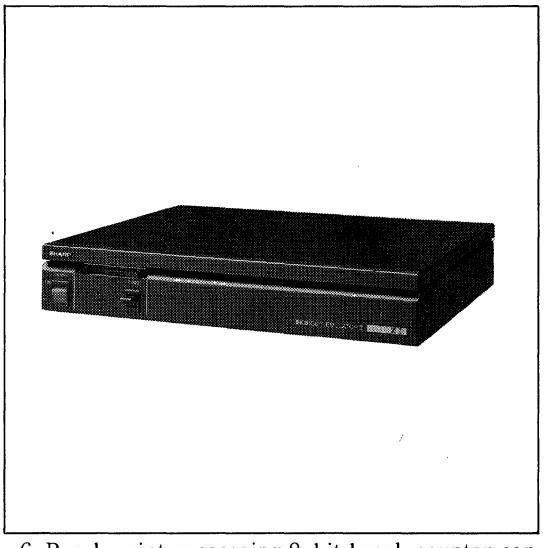
LH8DH321 Z8 In-Circuit Emulator Ⅱ

■ Description

Z8 in-circuit emulator Ⅱ (LH8DH321) is a device which has the function to support the development of the Z8 MCU 8-bit single-chip microcomputer (4Kbytes internal ROM : LH0811/LH0813, 2K bytes internal ROM : LH0801/LH0803). Software developed by the host computer can be downloaded via RS232C into this emulator for program debug purposes.

Prototype Z8 application systems under development and developed systems can be emulated on the real time basis.

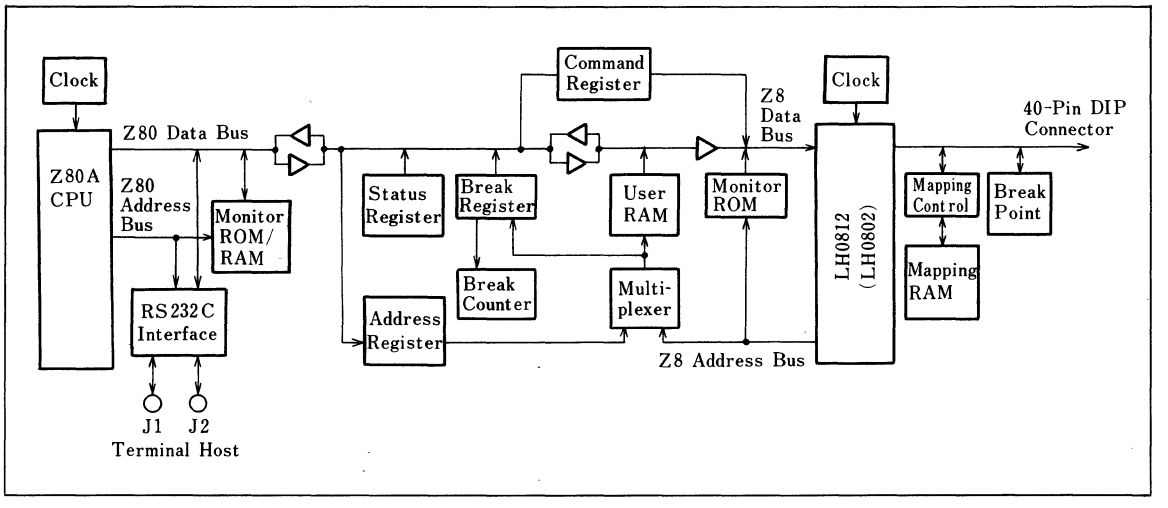
By debugging the user system while emulating, the development term of the user system or maintenance period becomes shorter.



■ Features

1. Usable for 4K and 2K bytes internal ROM
2. Stand-alone type: load the program from the host computer, and save the program to the host computer after debugging.
3. Mapping RAM can be designated for memory area both of program and data.
4. User program in the external ROM can be transferred to the mapping RAM.
5. Possess line assembler and reverse assembler, making debugging effective.
6. Break point possessing 8-bit break counter can be set : up to 4096 in the internal ROM (up to 2048 in the 2K internal ROM) 1 in the external ROM/RAM.
7. Step and trace of user program can be executed.
8. Contents of user program and register can be displayed and changed.
9. I/O ports and register files can all be executed by the user.

■ Block Diagram

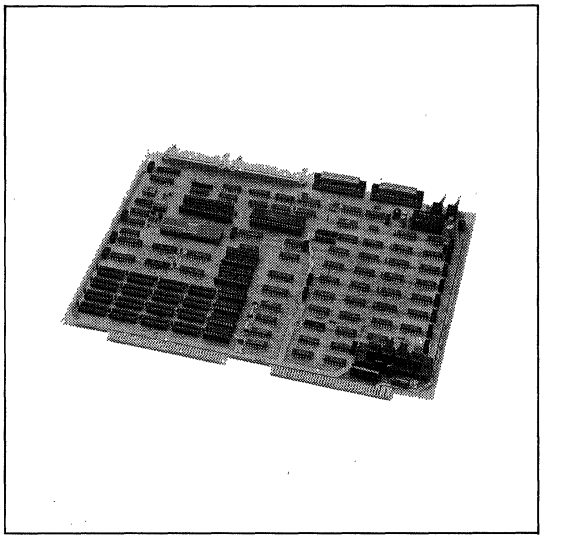


LH8DH330 Z8000 Evaluation Board

■ Description

This board is designed for evaluating application systems using the Z8000 16-bit microprocessor.

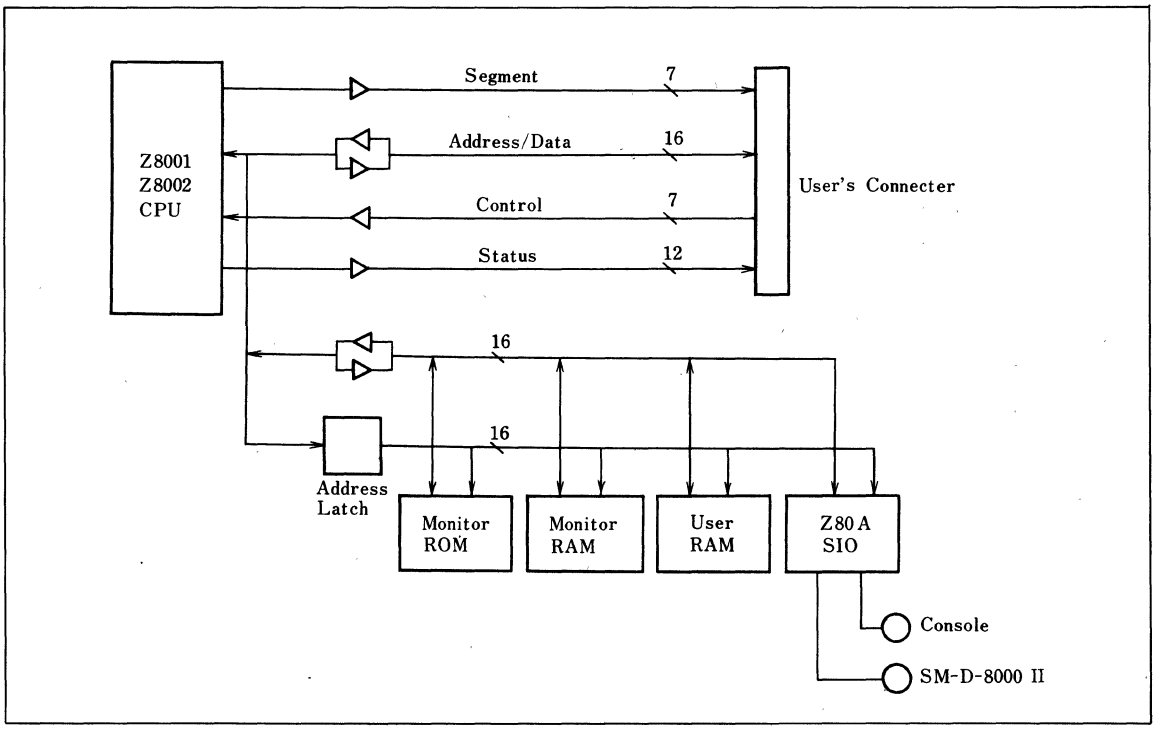
It is also available for a development system due to the emulation function.



■ Features

1. User RAM : 32K bytes
2. Monitor ROM : 8K bytes
3. Break point : 1 point
4. Support for debugging Z8001 CPU Z8002 CPU programs
5. In-circuit emulation functions
6. Object program execution : Real time, single step, and trace
7. Connection with SM-D-8000 II /SM-D-8100 via RS232C interface

■ Block Diagram



LH8DH340 Z8000 In-circuit Emulator SM-E-8100

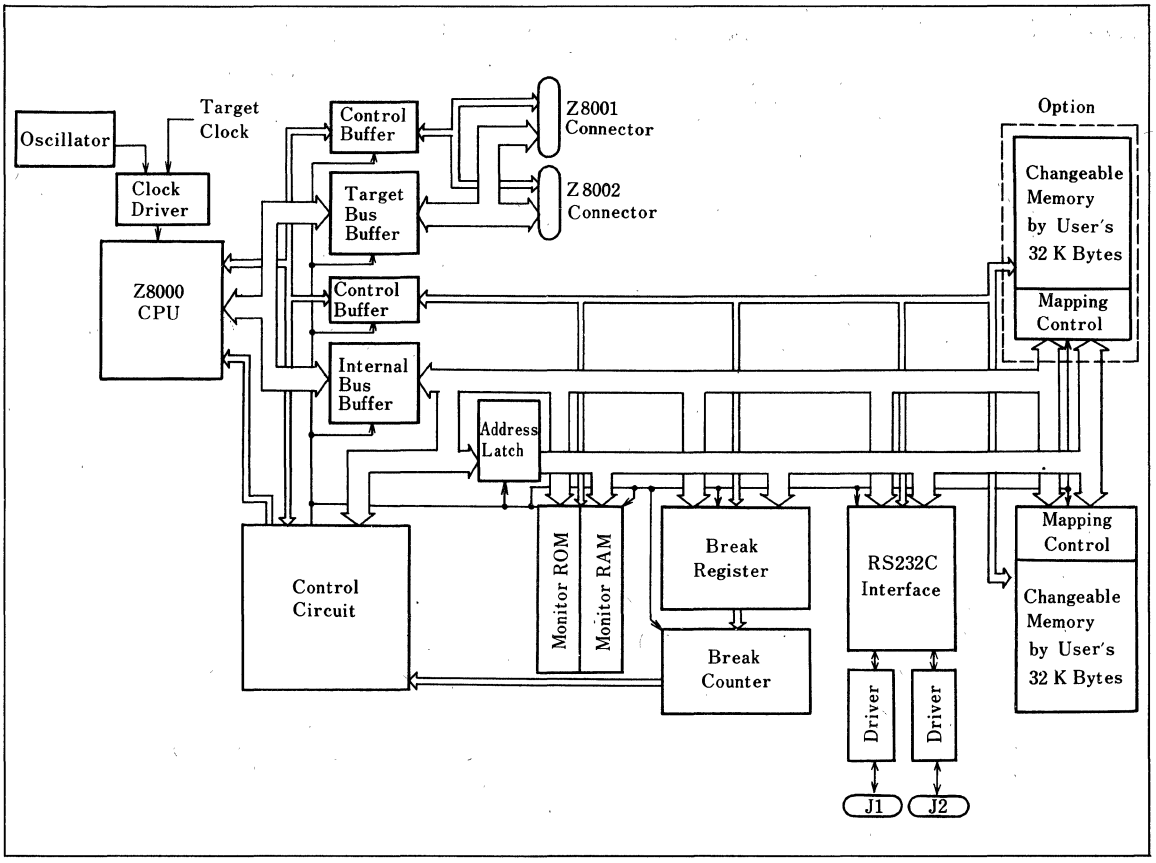
■ Description

The SM-E-8100 supports the development of Z8000 systems based on either the Z8001 or Z8002. A developed program loaded in the user's system memory or the emulator memory (user RAM area) can be executed in real time. The SM-E-8100 can emulate not only programs supplied from a host equipped with RS232C ports such as the SM-D-8000 II or SM-D-8100 but can also operate as a stand alone system.

■ Features

1. Emulation for both Z8001 and Z8002
2. All I/O ports opened for the user
3. User-opened RAM : 32K bytes (expandable)
4. Hardware break points (status, N/$\overline{S}$, R/$\overline{W}$, B/$\overline{W}$ available)
5. Break point counter (16-bit) available
6. Program execution : Real time, single step, trace, and snap shot
7. Down load and up load from a host computer
8. Built-in debugger (with 32 commands)

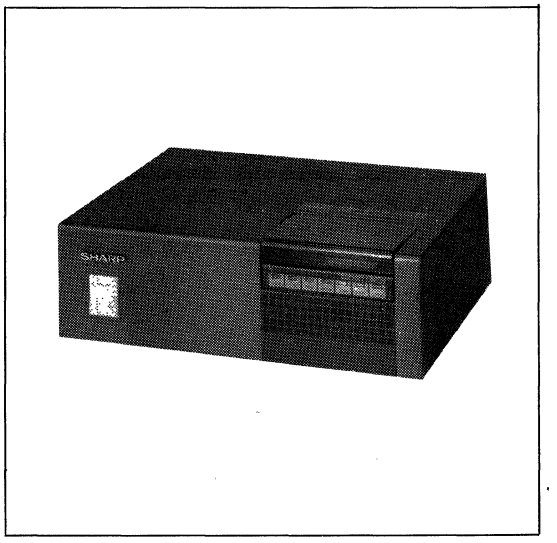
■ Block Diagram



LH8DH403 PROM Writer

■ Description

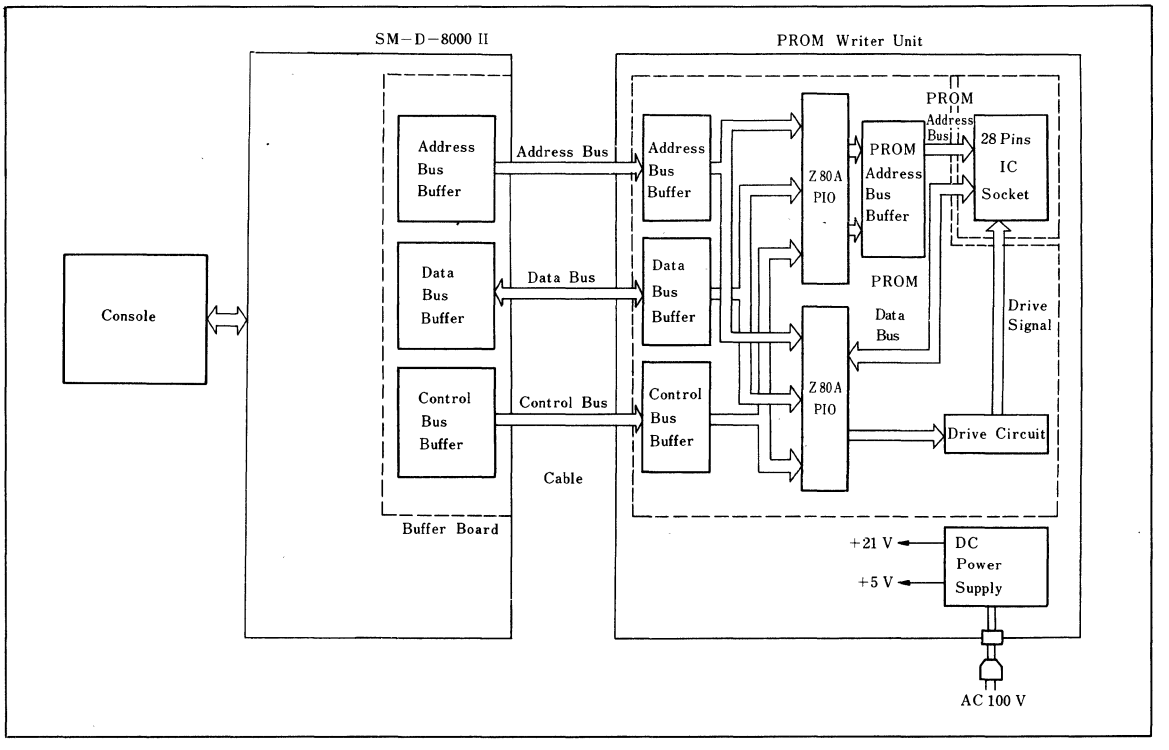
This equipment operates under control of SM-D-8000 II, FDOS. The control program is supplied on the floppy disk. The equipment writes programs that have been developed by using SM-D-8000 II into EPROMs directly, thereby reducing developing time.



■ Features

1. Applicable EPROM 2732A, 2764, 27128, and equivalents
2. Either mnemonic or spelled-out commands acceptable
3. Data management in file from
4. LED indication during command execution

■ Block Diagram



LU4DH200 SM Series Emulator SME-20

■ Description

The LU4DH200 is an emulator designed to support the development of programs for the SM series of 4-bit single-chip microcomputers. It consists of a data input and control key board, LED for display data, PROM writer and interface enabling programs can also be developed in RAM by using the RS232C to connect it to SM-D-8000 II which supports a cross-assembler and other software to facilitate program debugging.

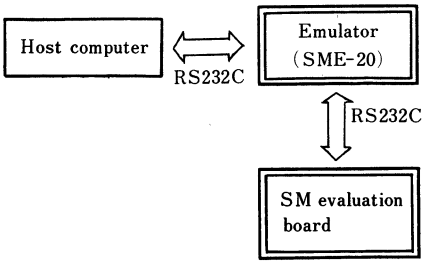
■ Features

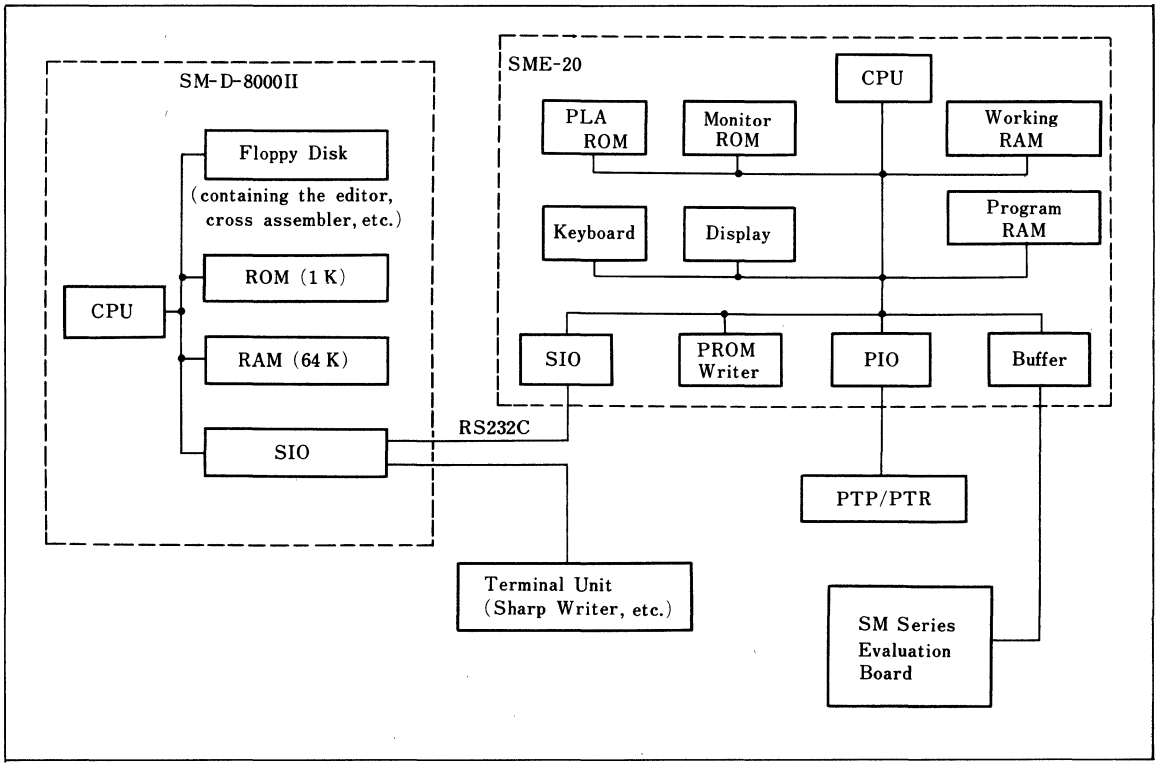
1. PROM writer (2716, 2732) in standard
2. RS232C 1 port
   Baud rate 150～19200B
   (8 levels selective)
3. Paper tape reader interface, Paper tape puncher interface in standard
4. Support all functions of SM series by altering PROM for PLA
5. Function of the emulator
   - Execute/halt program
   - Display/change data
   - One step operation
   - Execute start point of CPU
   - Repair address

■ System Configuration

The SME-20 can be connected through the RS 232C to the SM-D-8000 Ⅱ to allow efficient program debugging.

It can also be connected to other support tools which run under the CP/M operating system and equipped with an RS-232C interface.



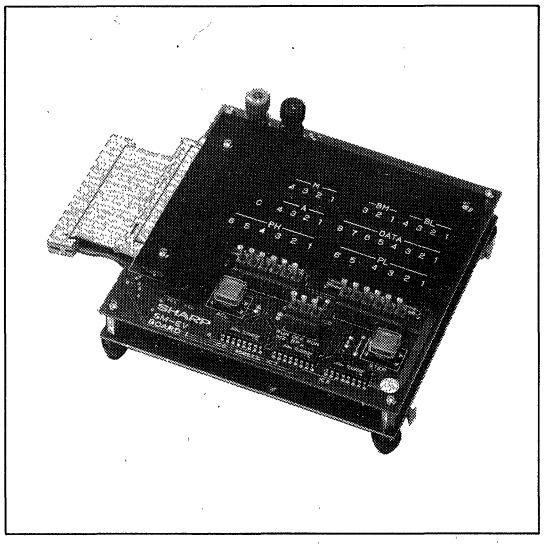


LUXXXH2 SM Series Evaluation Board

■ Description

There are designed for evaluating the SM series of 4-bit 1-chip microcomputers. The boards are functionally and electrically equivalent to the mask ROM version.

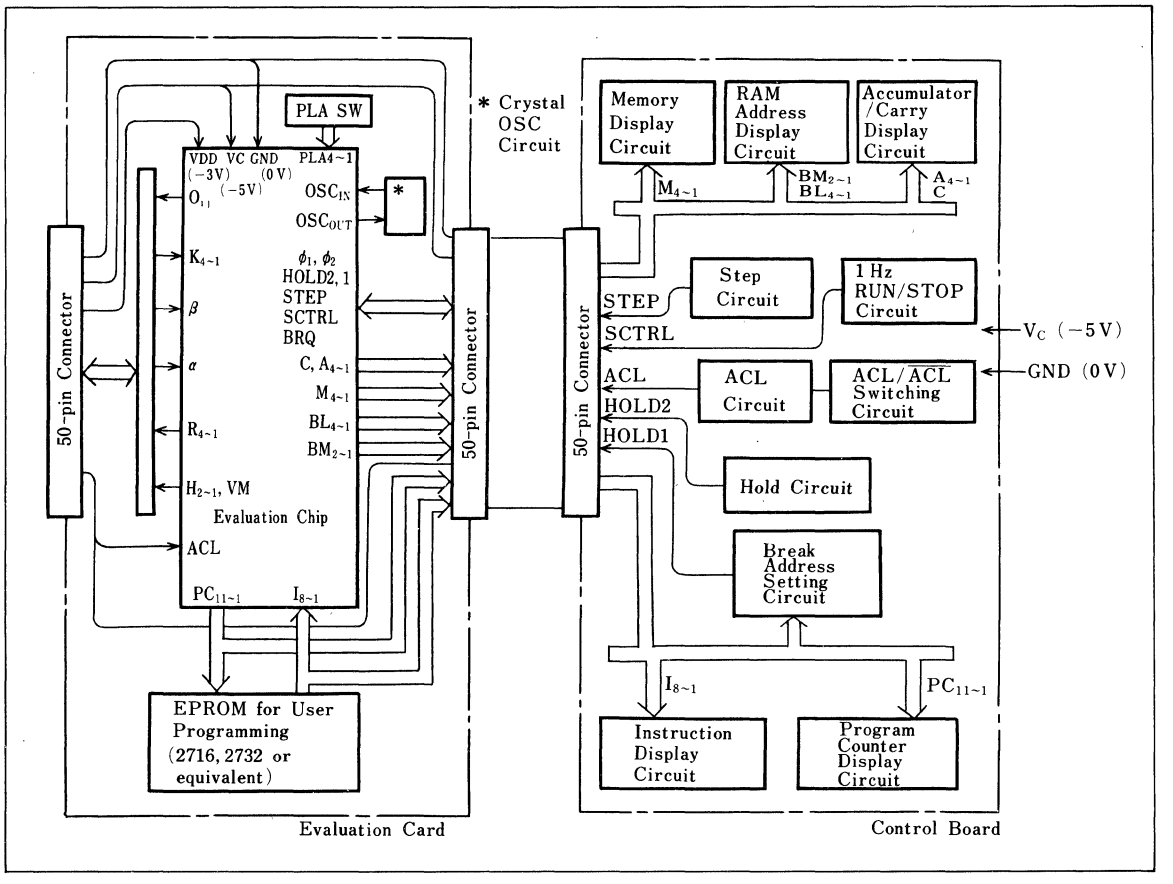
Programs can be developed either at the EPROM level, or when used with any of the SM series support tools (SM-D-80, SM-D-8000 Ⅱ) programs can be developed at the RAM level.



■ Features

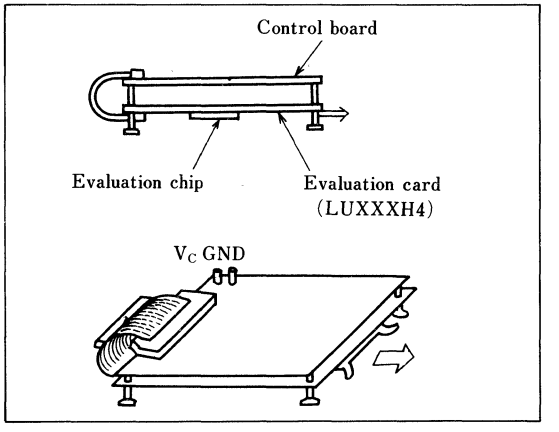
1. System debug with EPROM
2. Debug at RAM base in conjunction with support tool (SM-D-80, SM-D-8000 Ⅱ)
3. Function of the evaluation board
   - Hold function
   - One-step function
   - Auto-stop function
   - Display of the program counter
   - Display of accumlator and carry F/F
   - Display of RAM address, the register and memory
   - Display of instruction code
   - PLA set function

■ Block Diagram



■ SM Series Evaluation Board

The evaluation board consists of two printed circuit boards: the control board and the evaluation card (on which the evaluation chip and EPROM socket installed).



Memories

LH2331/LH2331A

NMOS 32768-Bit Mask Programmable Read Only Memory

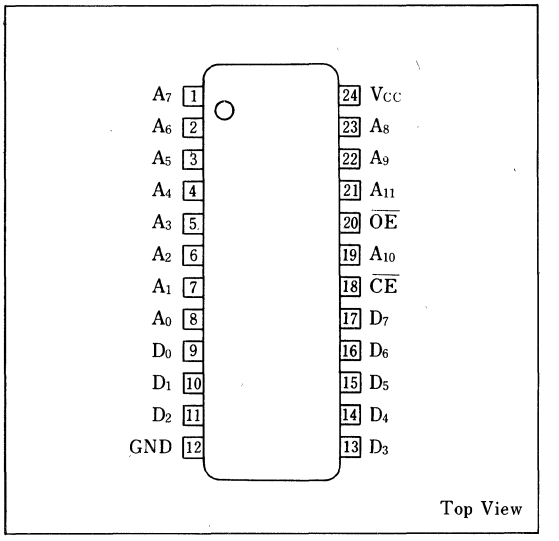
■ Description

The LH2331/LH2331A are fully static mask programmable ROMs organized as 4,096-word-by-8-bit by using silicon-gate NMOS process technology.

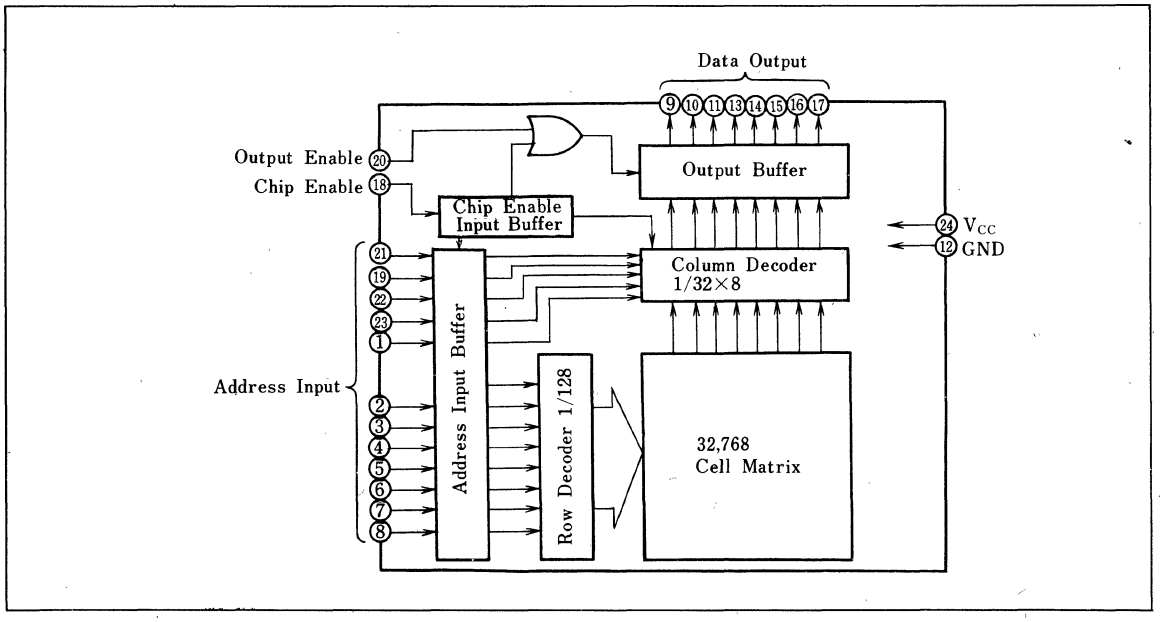
■ Features

1. 4,096-word-by-8-bit organization
2. Single +5V power supply
3. Fully static operation (no clock required)
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.)
   LH2331 : 450ns, LH2331A : 350ns
7. Power-down function
8. 24-pin dual-in-line package (pin compatible with i 2732 type EPROM)

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*	V_{IN}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

* Application voltage on any input pin with respect to ground.

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output low voltage	V_{OL}	I_{OL}=2.0mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=200 μA	2.4			V
Input low voltage	V_{IL}				0.8	V
Input high voltage	V_{IH}		2.0			V
Input leakage current	$\lvert I_{LI} \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$			10	μA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE} \geqq 2V$, $0 \leqq V_{OUT} \leqq V_{CC}$			10	μA
Chip enabled power supply current	I_{CC1}				110	mA
Chip disabled power supply current	I_{CC2}	$\overline{CE} \geqq 2V$			50	mA

■ AC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	LH2331			LH2331A			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Access time	t_{ACC}			450			350	ns
Chip enable setup time	t_{CE}			450			350	ns
Output enable time	t_{OE}			120			120	ns
Output hold time	t_{OH}	0			0			ns
Chip turn-off time	t_{DF}	0		100	0		100	ns

Test conditions of AC characteristics

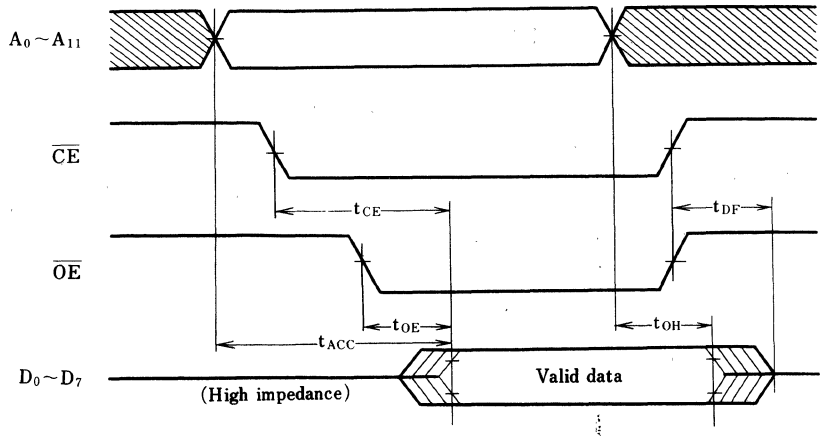
- Input voltage amplitude ····· +0.4～+2.8V
- Input rising/falling time ····· 10ns
- Input threshold level ····· 1.5V
- Output threshold level ····· 0.8V and 2.0V
- Output load condition ····· 1TTL+100pF

■ Capacitance

(f=1MHz, Ta=25℃)

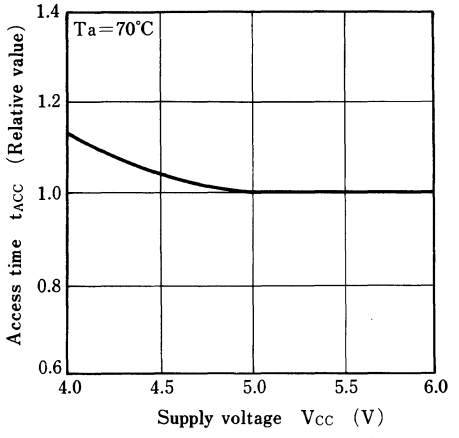
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			15	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			15	pF

■ Timing Diagram

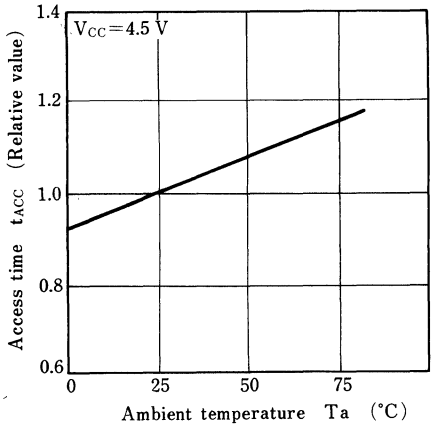


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

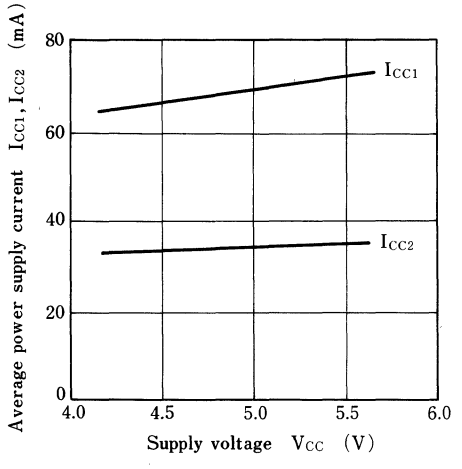
Access time vs. supply voltage



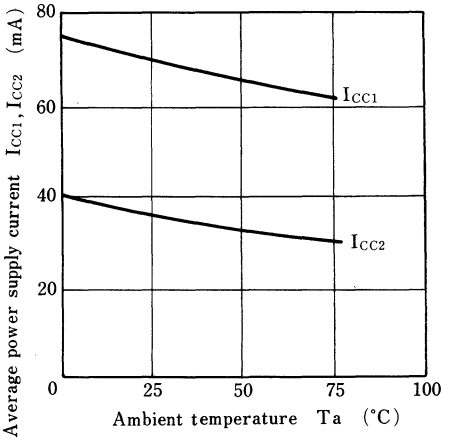
Access time vs. ambient temperature



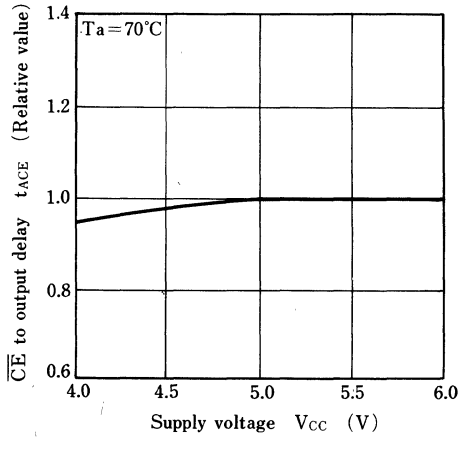
Average supply current vs. supply voltage



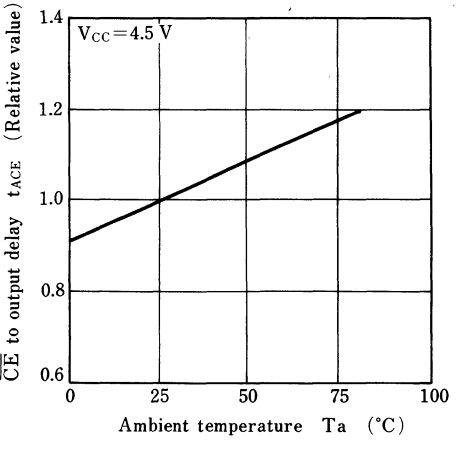
Average supply current vs. ambient temperature



$\overline{CE}$ to output delay vs. supply voltage



$\overline{CE}$ to output delay vs. ambient temperature



8

LH2332/LH2332A

NMOS 32768-Bit Mask Programmable Read Only Memory

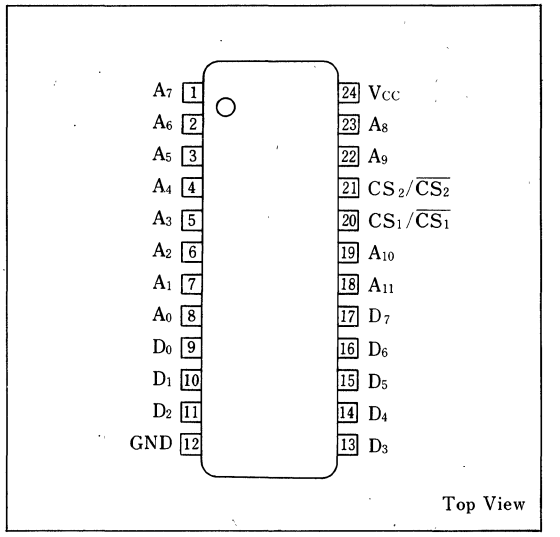
■ Description

The LH2332/LH2332A are fully static mask programmable ROMs organized as 4,096-word-by-8-bit by using silicon-gate NMOS process technology.

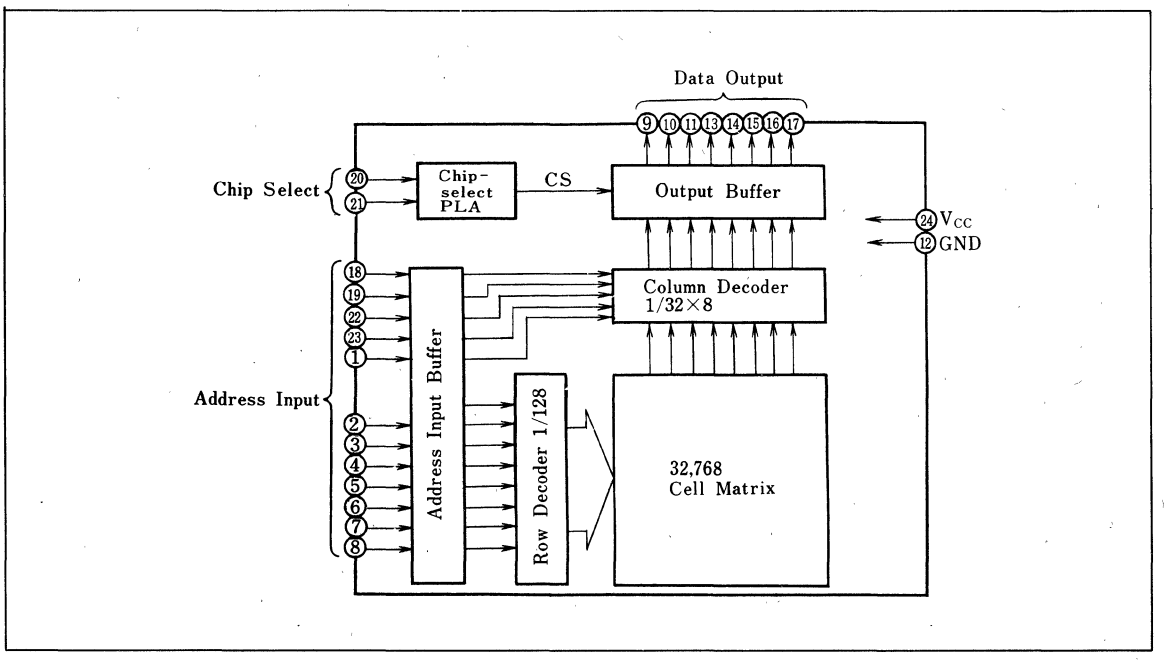
■ Features

1. 4,096-word-by-8-bit organization
2. Single +5V power supply
3. Fully static operation (no clock required)
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.)
   LH2332 : 450ns, LH2332A : 350ns
7. Programmable chip selects ($CS_1/\overline{CS_1}$, $CS_2/\overline{CS_2}$)
8. 24-pin dual-in-line package (JEDEC standard pin configuration)

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions (Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Input voltage	V_{IL}			0.8	V
	V_{IH}	2.0			V

■ DC Characteristics (V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}				0.8	V
Input high voltage	V_{IH}		2.0			V
Output low voltage	V_{OL}	I_{OL}=2.0mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=200 μA	2.4			V
Input leakage current	$\lvert I_{LI} \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$			10	μA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CS} \geqq 2V$, $0 \leqq V_{OUT} \leqq V_{CC}$			10	μA
Current consumption	I_{CC}				110	mA

■ AC Characteristics (V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Access time	t_{ACC}			450	ns
Output hold time	t_{OH}	0			ns
Chip enable setup time	t_{CE}			350	ns
Chip turn-off time	t_{DF}	0		150	ns

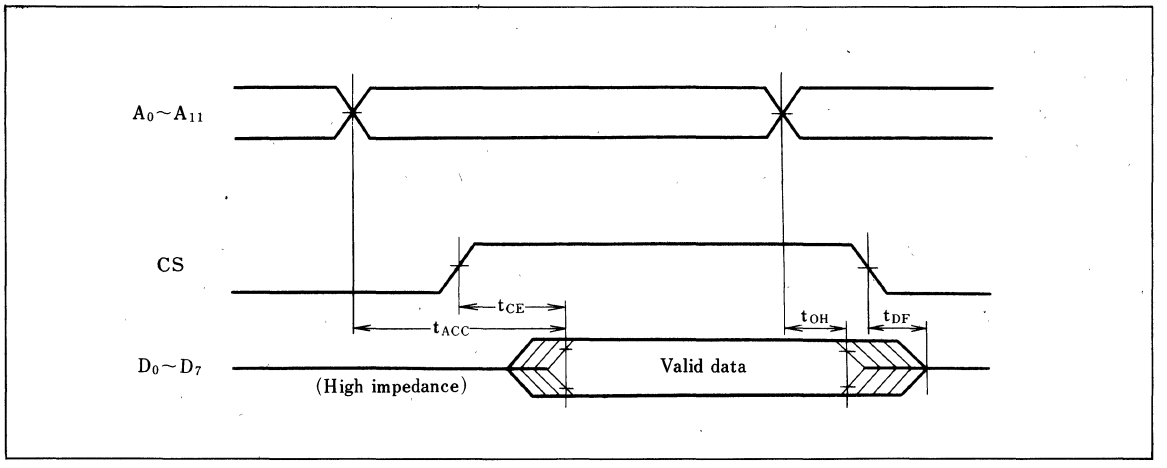
Test conditions of AC characteristics

- Input voltage amplitude ····· +0.4～+2.8V
- Input rising/falling time ····· 10ns
- Input threshold level ····· 1.5V
- Output threshold level ····· 0.8V and 2.0V
- Output load condition ····· 1TTL+100pF

■ Capacitance (f=1MHz, Ta=25℃)

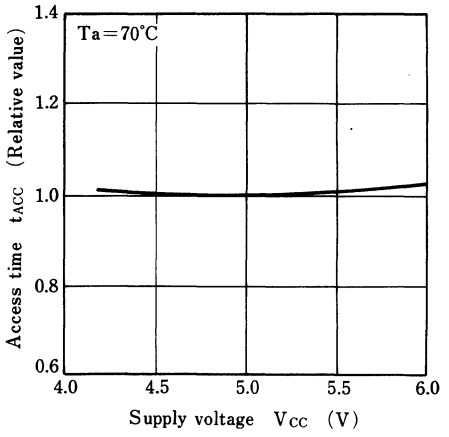
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			15	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			15	pF

■ Timing Diagram

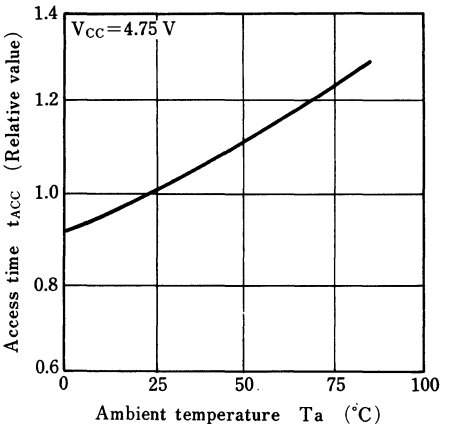


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

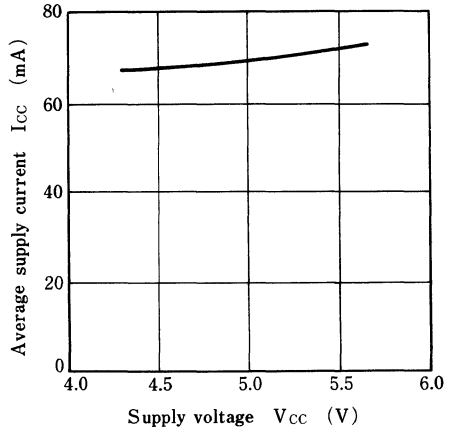
Access time vs. supply voltage



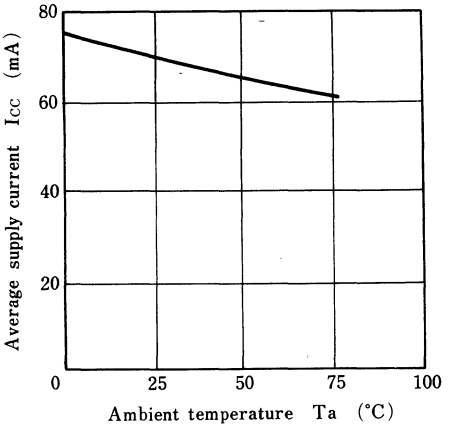
Access time vs. ambient temperature



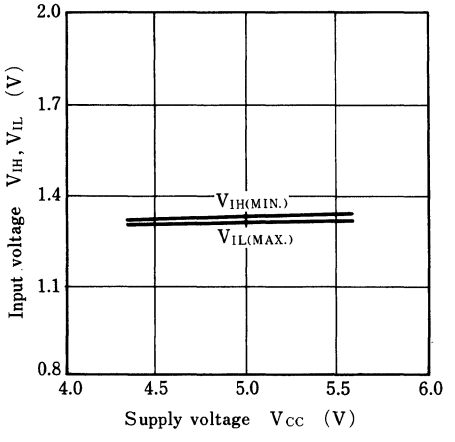
Average supply current vs. supply voltage



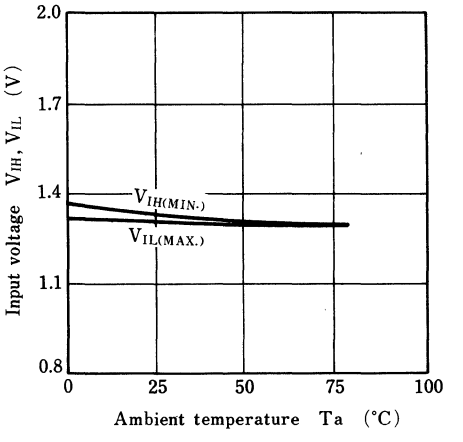
Average supply current vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



8

LH2362B NMOS 65536-Bit Mask Programmable Read Only Memory

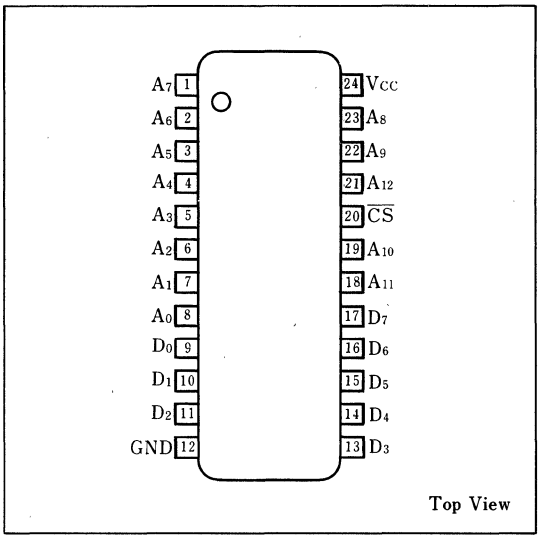
■ Description

The LH2362B is a fully static mask programmable ROM organized as 8,192-word-by-8-bit by using silicon-gate NMOS process technology.

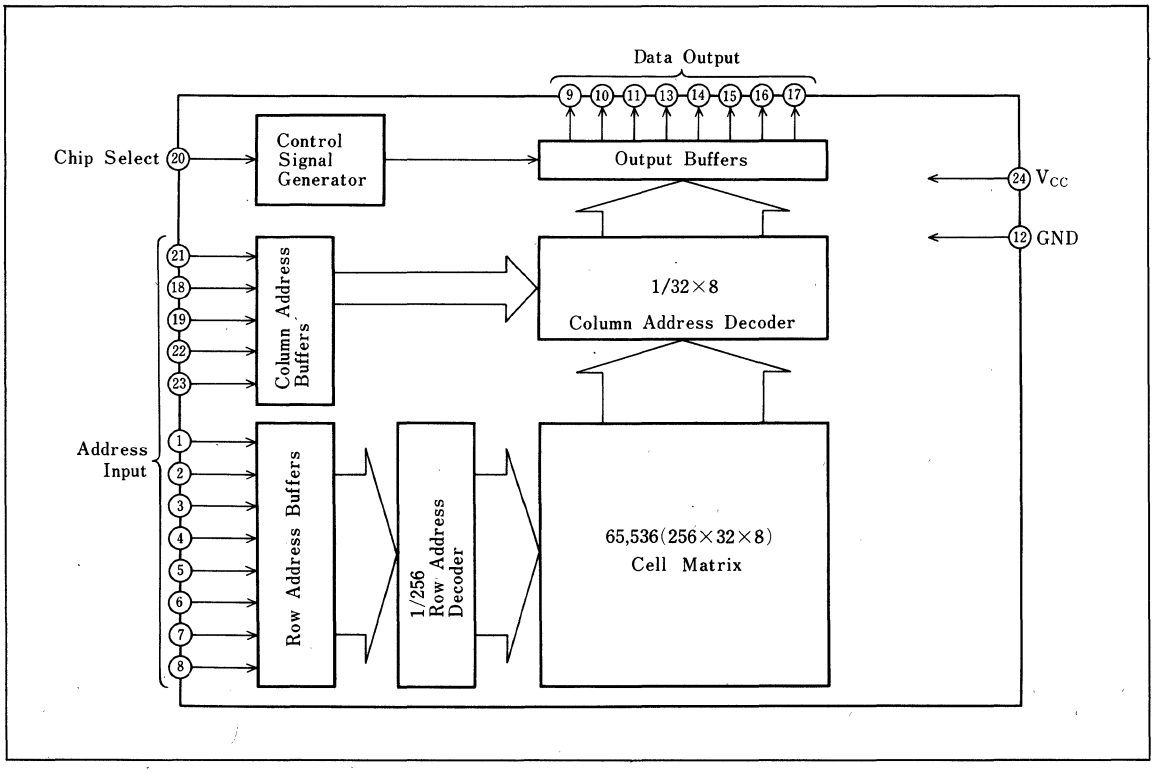
■ Features

1. 8,192-word-by-8-bit organization
2. Single +5V power supply
3. Fully static operation (no clock required)
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.) : 250ns
7. 24-pin dual-in-line package (JEDEC standard pin configuration)

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Input voltage	V_{IL}			0.8	V
	V_{IH}	2.0			V

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}				0.8	V
Input high voltage	V_{IH}		2.0			V
Output low voltage	V_{OL}	I_{OL}=2.0mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=200 μA	2.4			V
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V～V_{CC}			10	μA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CS} \geqq 2V$, V_{OUT}=0V～V_{CC}			10	μA
Current consumption	I_{CC}				160	mA

■ AC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Access time	t_{ACC}			250	ns
Chip enable setup time	t_{CE}			100	ns
Chip turn-off time	t_{DF}			100	ns
Output hold time	t_{OH}	0			ns

Test conditions of AC characteristics

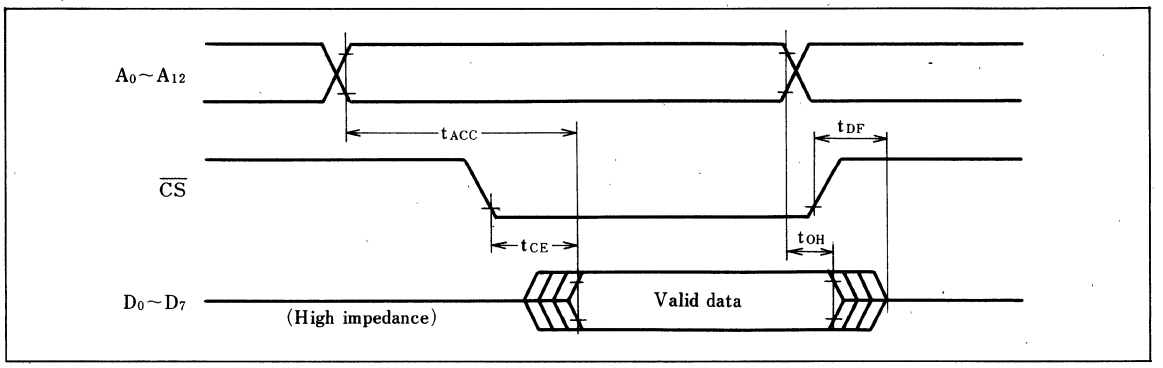
- Input voltage amplitude ····· +0.4～+2.8V
- Input rising/falling time ····· 10ns
- Input threshold level ····· 1.5V
- Output threshold level ····· 0.8V and 2.0V
- Output load condition ····· 1TTL+100pF

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			16	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			13	pF

■ Timing Diagram

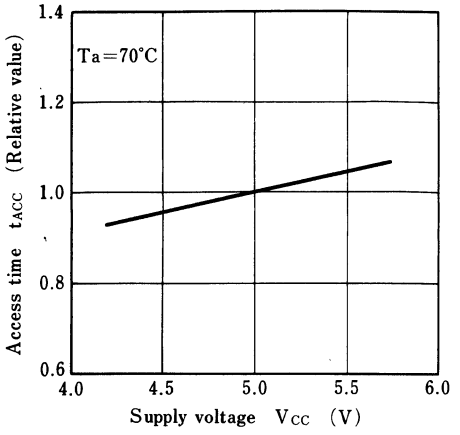


■ Chip Select

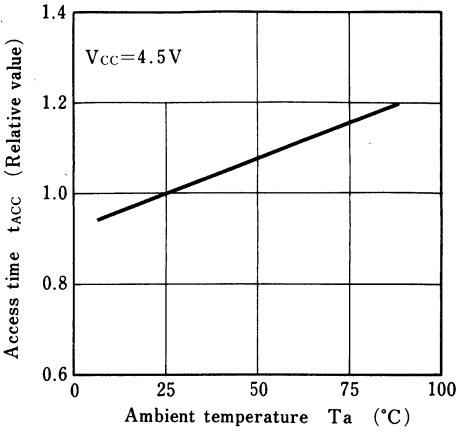
$\overline{CS}$	D0~D7
L	DOUT (Data output)
H	High impedance

■ Electrical Characteristics Curves (Ta=25℃ unless otherwise specified)

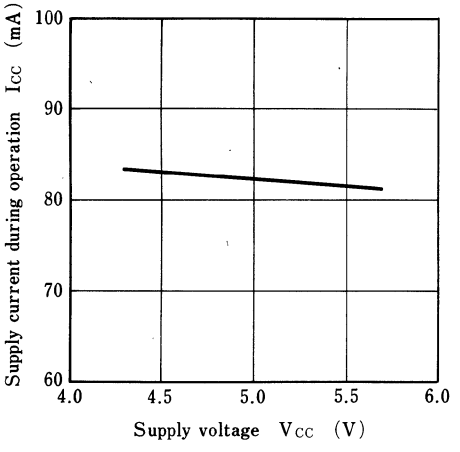
Access time vs. supply voltage



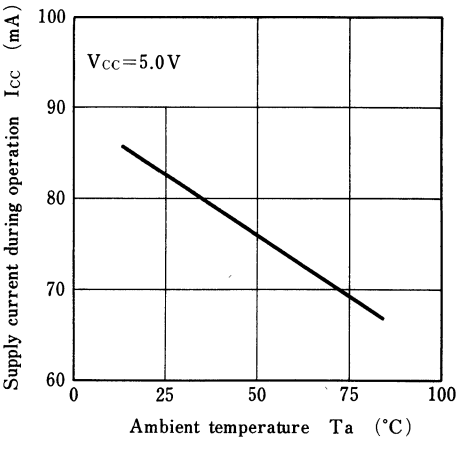
Access time vs. ambient temperature



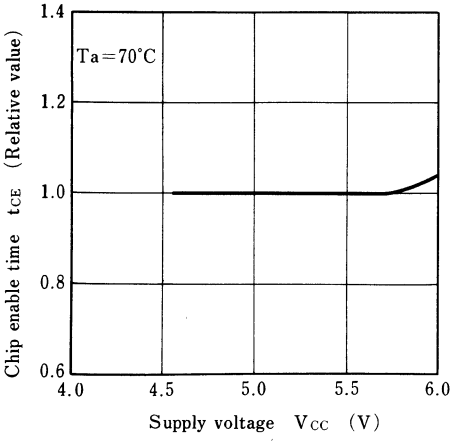
Supply current during operation vs. supply voltage



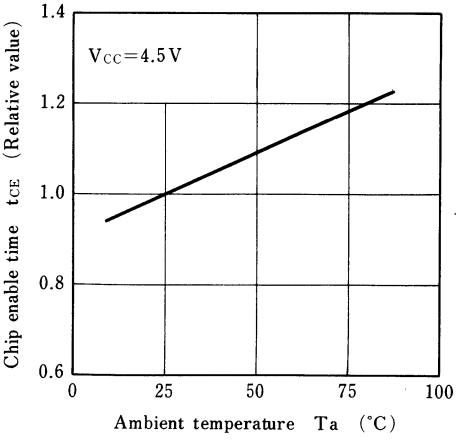
Supply current during operation vs. ambient temperature



Chip enable time vs. supply voltage



Chip enable time vs. ambient temperature



8

LH2367 NMOS 65536-Bit Mask Programmable Read Only Memory

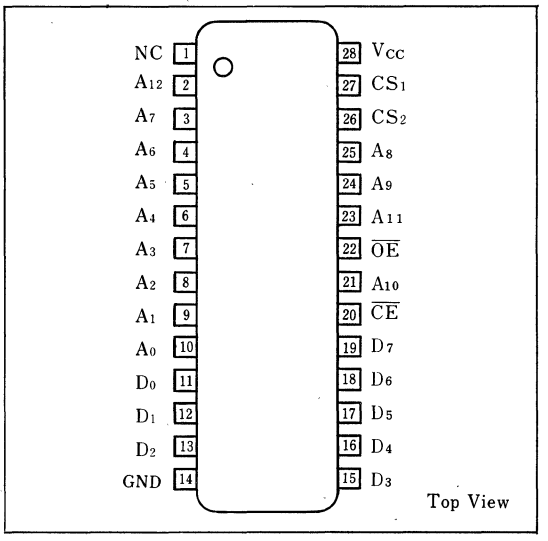
Description

The LH2367 is a fully static mask programmable ROM organized as 8,192-word-by-8-bit by using silicon-gate NMOS process technology.

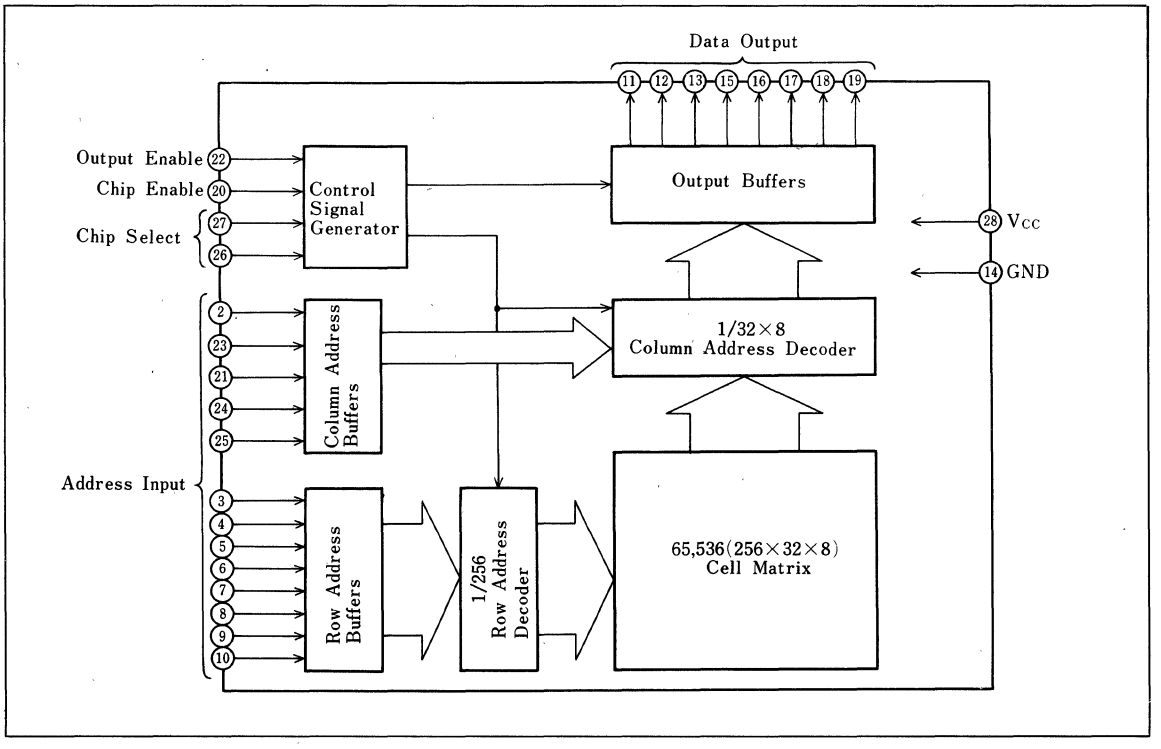
Features

1. 8,192-word-by-8-bit organization
2. Single +5V power supply
3. Fully static operation (no clock required)
4. All inputs and outputs TTL compatible
5. Three-state output
6. Access time (MAX.) : 250ns
7. Programmable chip select (CS_1, CS_2)
8. 28-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Applied voltage *	V	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Input voltage	V_{IL}	−0.5		0.8	V
	V_{IH}	2.0		V_{CC}	V

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}		−0.5		0.8	V
Input high voltage	V_{IH}		2.0		V_{CC}	V
Output low voltage	V_{OL}	I_{OL}=2mA			0.4	V
Output high voltage	V_{OH}	I_{OH}= 200 μA	2.4			V
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V～V_{CC}		0.01	10	μA
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT}=0V～V_{CC} (In non-selection mode)		0.01	10	μA
Chip enabled power supply current	I_{CC1}			50	80	mA
Chip disabled power supply current	I_{CC2}	Note		20	40	mA

Note : $\overline{CE} \geqq 2.0V$ (Non-active) or CS_1 or CS_2 is non-active ($\overline{CE}$ type chip select)

■ AC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

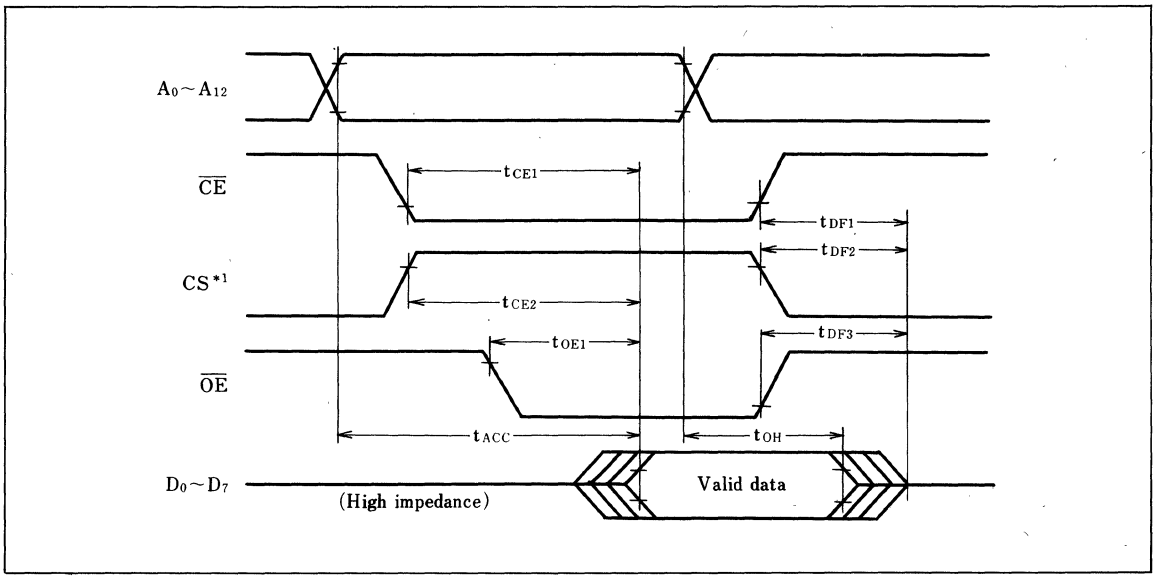
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Access time	t_{ACC}			250	ns
Chip enable time (from $\overline{CE}$)	t_{CE1}			250	ns
Chip enable time (from CS)	t_{CE2}			250	ns
Output enable time (from $\overline{OE}$)	t_{OE1}			100	ns
Output enable time (from CS)	t_{OE2}			100	ns
Output turn-off time (from $\overline{CE}$)	t_{DF1}			100	ns
Output turn-off time (from CS)	t_{DF2}			100	ns
Output turn-off time (from $\overline{OE}$)	t_{DF3}			100	ns
Output hold time	t_{OH}	0			ns

Test conditions of AC characteristics

- Input voltage amplitude ..... +0.4V and +2.8V
- Input rising/falling time 10ns
- Input threshold level 1.5V
- Output threshold level ..... 0.8V and 2.0V
- Output load condition ..... 1TTL+100pF

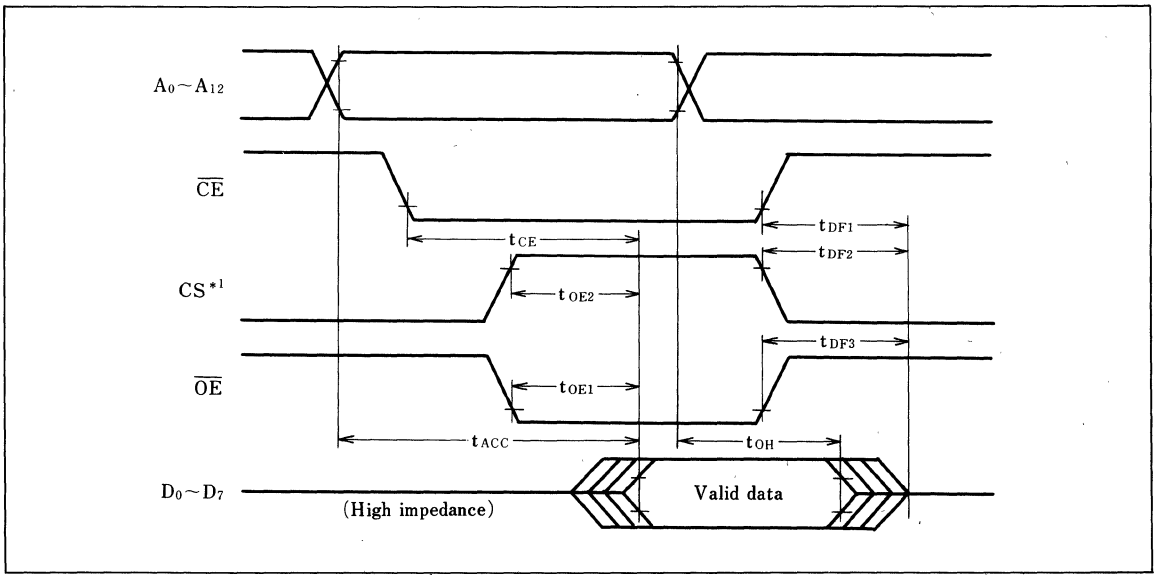
■ Timing Diagram

(1) Type1 (CS_1/CS_2 is CE function type)



* 1 CS is the logical product of CS_1 and CS_2

(2) Type2 (CS_1/CS_2 is OE function type)



* 1 CS is the logical product of CS_1 and CS_2

■ Chip Select

$\overline{OE}$	$\overline{CE}$	CS*1	$D_0 \sim D_7$	Mode
X	H	X	High impedance	Non-select, power down
X	X	L	High impedance	*2
H	X	X	High impedance	Output non-select
L	L	H	D_{OUT}	Read

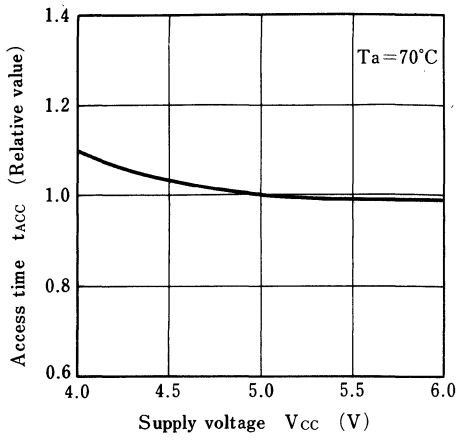
*1 CS is high only when the CS_1 pin and the CS_2 pin are active at the same time and is low at all other times. (Non-connection pins are continuously active.)

*2 Chip select input CS_1 and CS_2 can be programmed into 2 types depending on the ROM pattern (see timing chart).

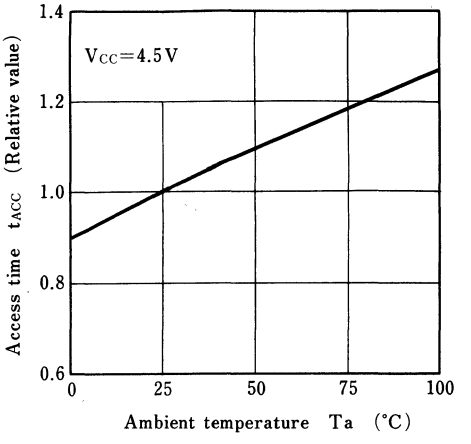
Type	Function of CS_1 pin and CS_2 pin
(1) $\overline{CE}$ function type	Functions at same time as $\overline{CE}$ pin ; when CS = low, non-select power-down mode
(2) $\overline{OE}$ function type	Functions at same time as $\overline{OE}$ pin ; when CS = low, output non-select mode

■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

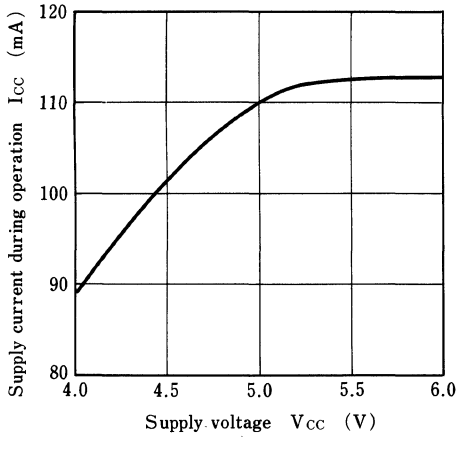
Access time vs. supply voltage



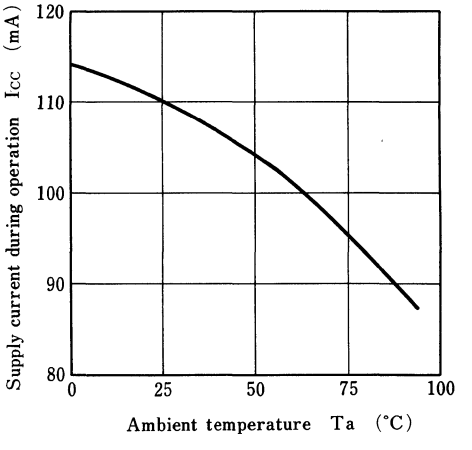
Access time vs. ambient temperature



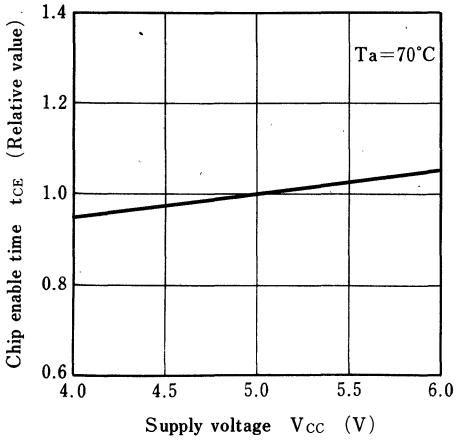
Supply current during operation vs. supply voltage



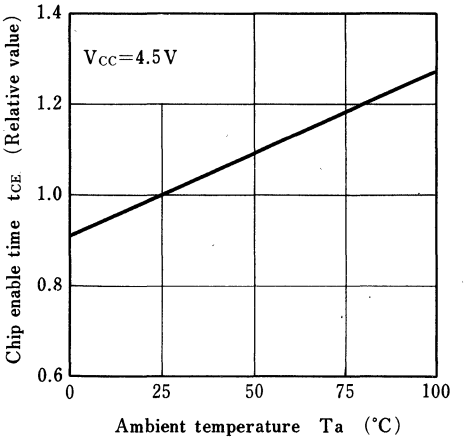
Supply current during operation vs. ambient temperature



Chip enable time vs. supply voltage



Chip enable time vs. ambient temperature



LH5366A CMOS 65536-Bit Mask Programmable Read Only Memory

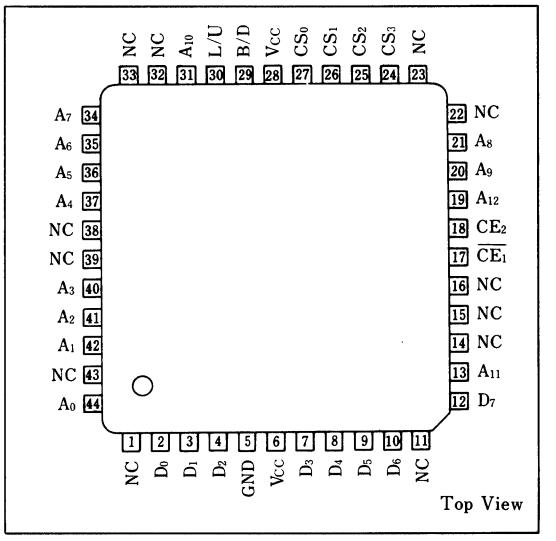
■ Description

The LH5336A is a mask programmable ROM organized as 8,192-word-by-8-bit by using CMOS process technology.

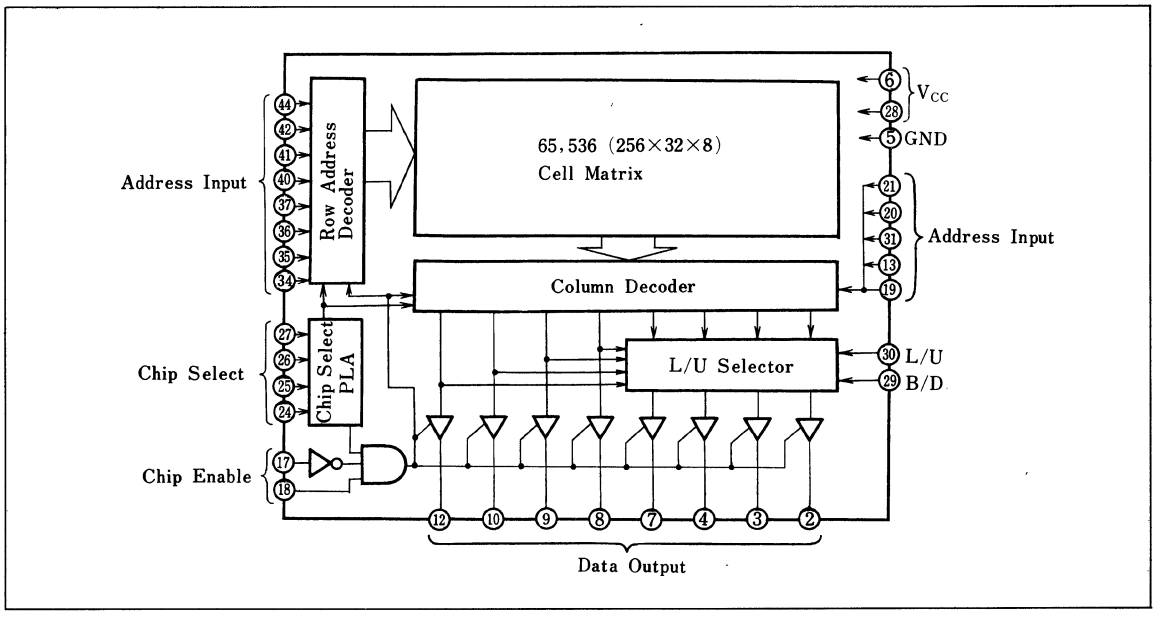
■ Features

1. 8,192-word-by-8-bit organization
2. Single +5V power supply
3. Low power consumption
4. Edge enabled operation ($\overline{CE_1}$, CE_2)
5. Three-state outputs
6. Access time (MAX.) : 2.5 μs
7. Programmable chip select
8. Selectable byte or digit output
9. 44-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	4.5～5.5	V

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input high voltage	V_{IH}		−0.3		0.8	V	
Input low voltage	V_{IL}		V_{CC}−1.0		V_{CC}	V	
Output high voltage	V_{OH}	I_{OH}=100 μA			2.4	V	
Output low voltage	V_{OL}	I_{OL}=1.6mA	0.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V～V_{CC}			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$	In non-selection mode			1.0	μA	
Chip enabled power supply current	I_{CC1}				5	mA	1
Chip disabled power supply current	I_{CC2}	C_3, V_{IN}=0.2V or V_{CC}−0.2V			5	μA	

Note 1: Average current at cycle time of 4 μs with output open and input set to 0V or Vcc.

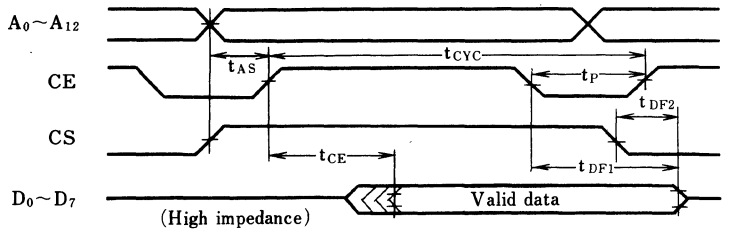
■ AC Characteristics

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}	1			μs
Chip enable setup time	t_{CE}			2.5	μs
Chip enable precharge time	t_p	1.5			μs
Chip turn-off time (CE)	t_{DF1}			1.5	μs
Chip turn-off time (CS)	t_{DF2}			1.5	μs
Cycle time	t_{CYC}	4.0			μs

Test conditions of AC Characteristics

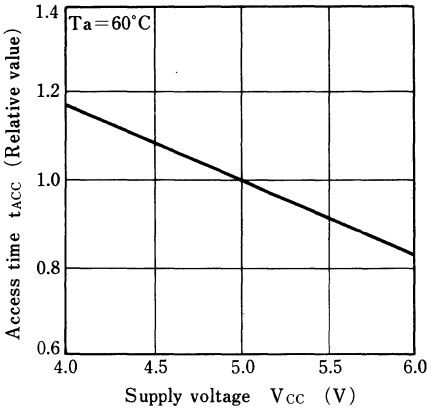
- Input voltage amplitude ····· +0.8V～V_{CC}−1.0V
- Input rising/falling time ····· 20ns
- Input threshold level ····· 1.5V
- Output threshold level ····· 0.4V and 2.4V
- Output load condition ····· 10pF

Timing Diagram

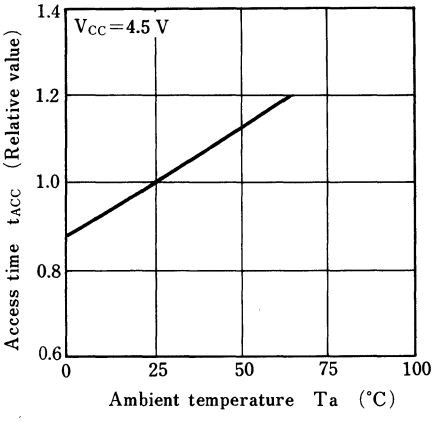


Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

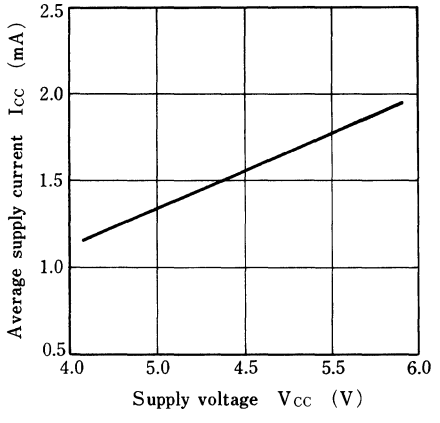
Access time vs. supply voltage



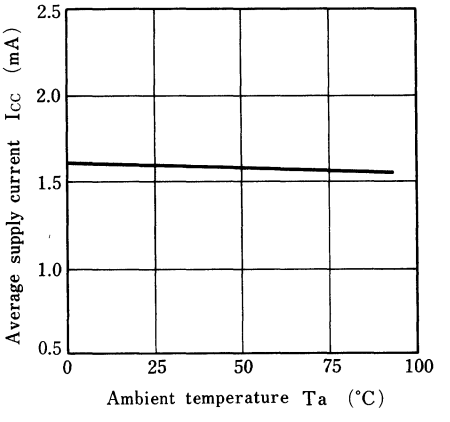
Access time vs. ambient temperature



Average supply current vs. supply voltage



Average supply current vs. ambient temperature



8

LH5366S CMOS 65536-Bit Mask Programmable Read Only Memory

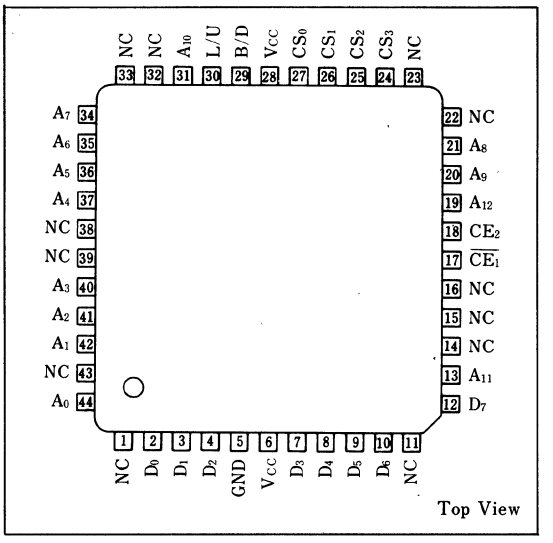
Description

The LH5366S is a mask programmable ROM organized as 8,192-word-by-8-bit by using CMOS process technology.

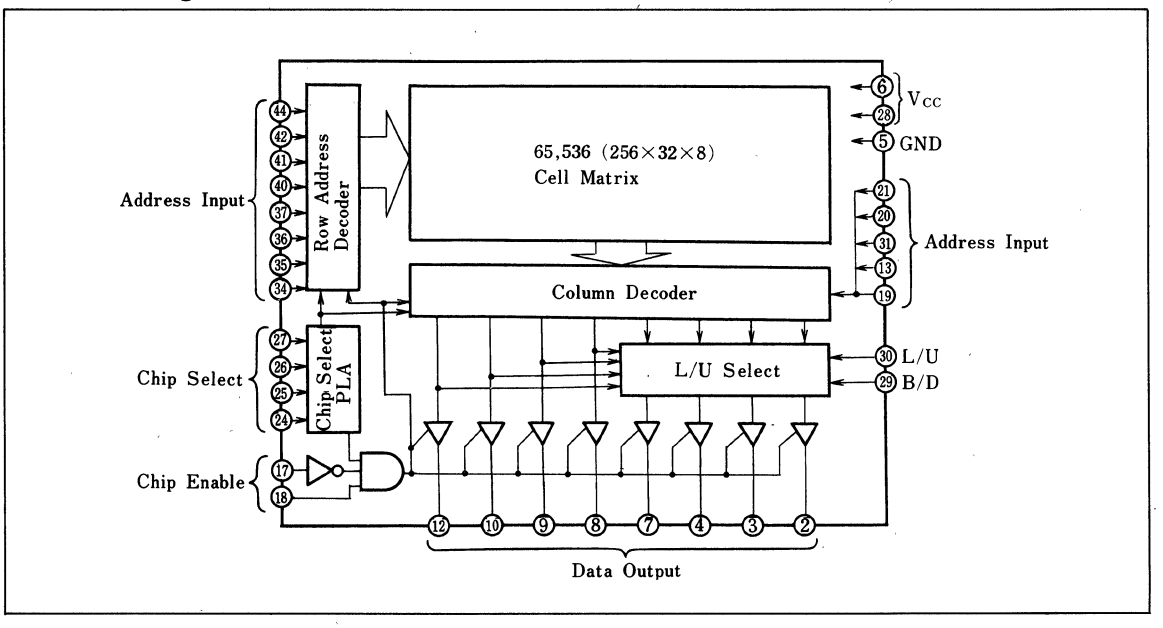
Features

1. 8,192-word-by-8-bit organization
2. Single +3V power supply
3. Low power consumption
4. Edge enabled operation ($\overline{CE_1}$, CE_2)
5. Three-state outputs
6. Access time (MAX.) : 6 μs
7. Programmable chip select
8. Selectable byte or digit output
9. 44-pin quad-flat package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+5.0	V
Input voltage*	V_{IN}	−0.3～+5.0	V
Output voltage*	V_{OUT}	−0.3～+5.0	V
Operating temperature	T_{opr}	0～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	2.5～3.5	V

■ DC Characteristics

(V_{CC}=3.0V, Ta=0～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input high voltage	V_{IH}		V_{CC}−0.6			V	
Input low voltage	V_{IL}				0.6	V	
Output high voltage	V_{OH}	I_{OH}=50 μA	V_{CC}−0.5			V	
Output low voltage	V_{OL}	I_{OL}=50 μA			0.5	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V～V_{CC}			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$	In non-selection mode			1.0	μA	
Chip enabled power supply current	I_{CC1}				1.0	mA	1
Chip disabled power supply current	I_{CC2}	$\overline{CS}$, V_{IN}=0.2V or V_{CC}−0.2V			5.0	μA	

Note 1: Average current at cycle time of 12 μs with output open and input set to 0V or Vcc.

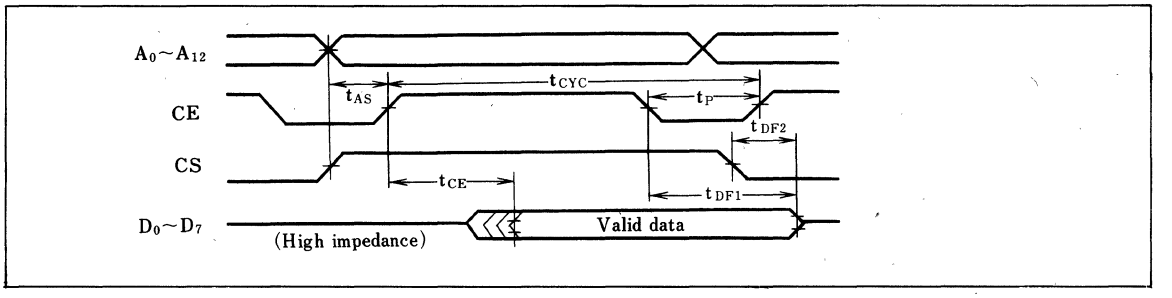
■ AC Characteristics (V_{CC}=2.5～3.5V, Ta=0～+60℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}	1			μs
Chip enable setup time	t_{CE}			6	μs
Chip enable precharge time	t_p	6			μs
Chip turn-off time ($\overline{CE}$)	t_{DF1}			1.5	μs
Chip turn-off time ($\overline{CS}$)	t_{DF2}			1.5	μs
Cycle time	t_{CYC}	12			μs

Test conditions of AC characteristics

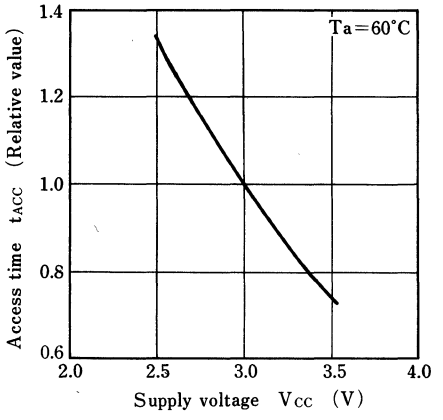
- Input voltage amplitude ····· +0.5V～V_{CC}−0.5V
- Input rising/falling time ····· 20ns
- Input threshold level ····· 0.3V
- Output threshold level ····· V_{CC}−0.3V
- Output load condition ····· 10pF

■ Timing Diagram

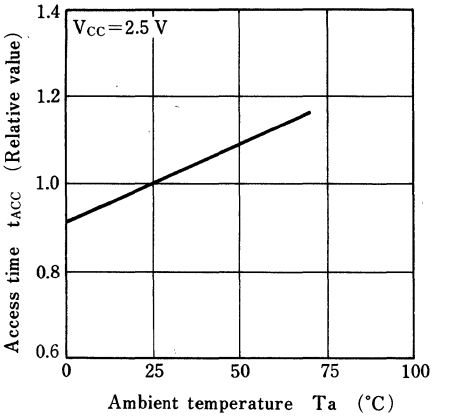


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

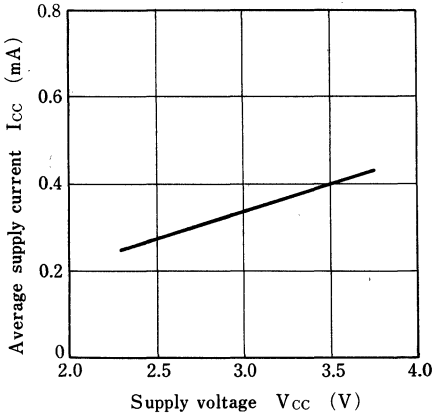
Access time vs. supply voltage



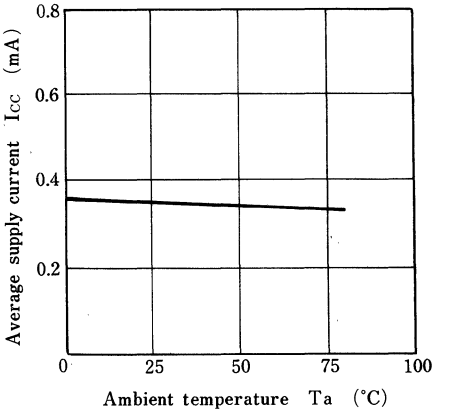
Access time vs. ambient temperature



Average supply current vs. supply voltage



Average supply current vs. ambient temperature



LH5367 CMOS 65536-Bit Mask Programmable Read Only Memory

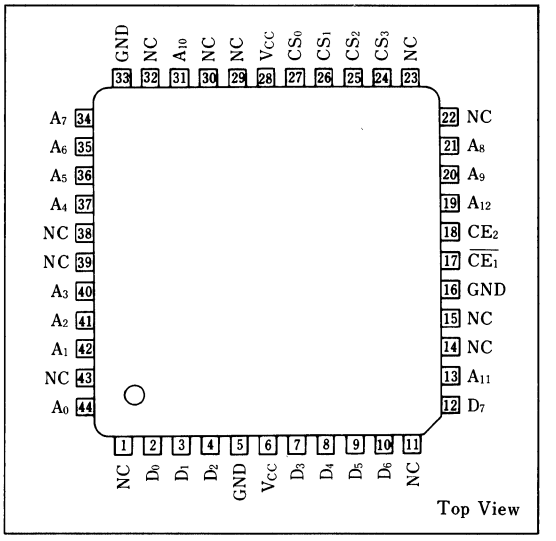
■ Description

The LH5367 is a mask programmable ROM organized as 8,192-word-by-8-bit by using silicon-gate CMOS process technology.

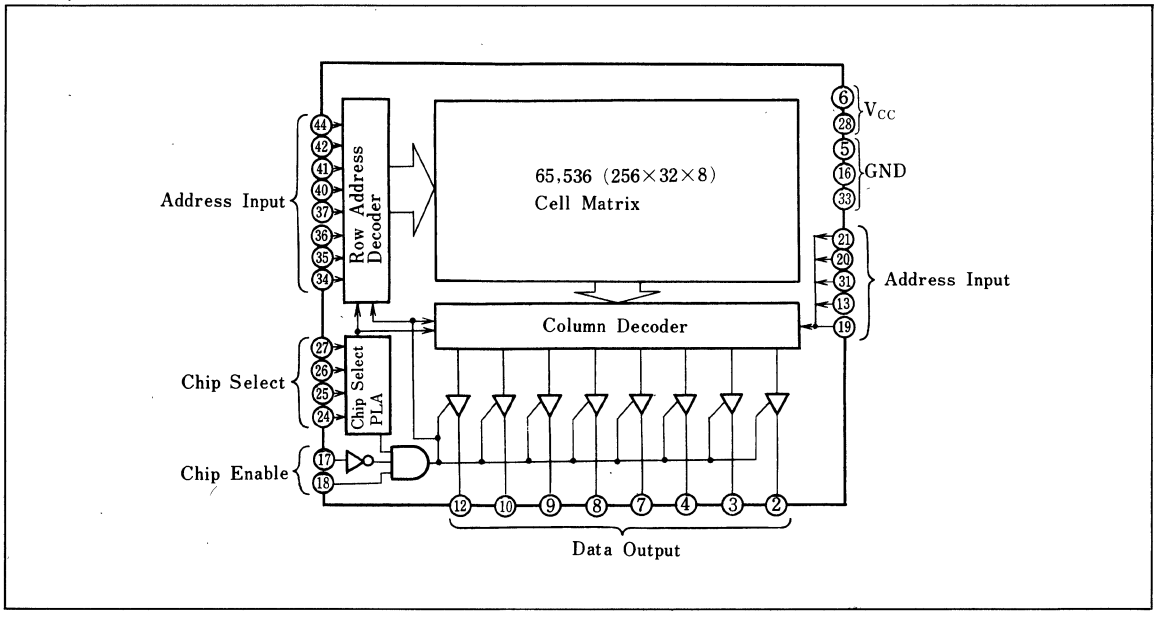
■ Features

1. 8,192-word-by-8-bit organization
2. Single +5V power supply
3. Low power consumption
4. Edge enabled operation ($\overline{CE_1}$, CE_2)
5. Three-state outputs
6. Access time (MAX.) : 450ns
7. Programmable chip select
8. 44-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	4.75～5.25	V

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input high voltage	V_{IH}		V_{CC}−1.0		V_{CC}	V	
Input low voltage	V_{IL}		−0.3		0.8	V	
Output high voltage	V_{OH}	I_{OH}=100 μA	2.4			V	
Output low voltage	V_{OL}	I_{OL}=1.6mA			0.4	V	
Input leakage current	$\|I_{LI}\|$	V_{IN}=0V～V_{CC}			1.0	μA	
Output leakage current	$\|I_{LO}\|$	In non-selection mode			1.0	μA	
Chip enabled power supply current	I_{CC1}				14	mA	1
Chip disabled power supply current	I_{CC2}	C_s, V_{IN}=0.2V or V_{CC}−0.2V			5.0	μA	

Note 1: Average current at cycle time of 750ns with output open and input set to 0V or V_{CC}.

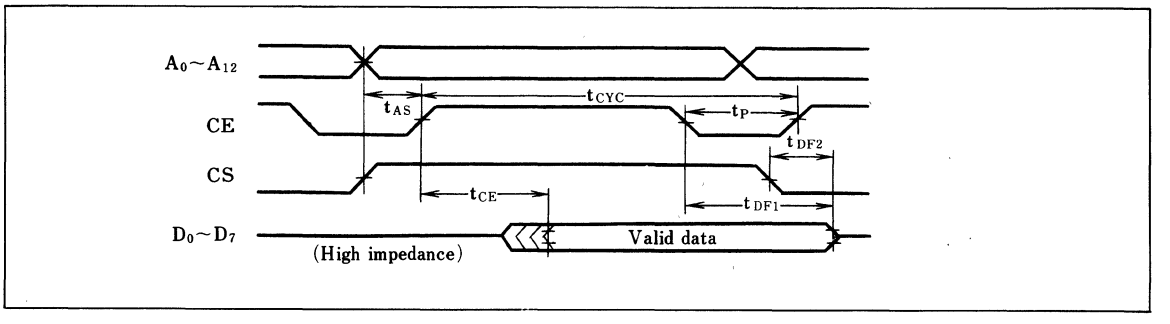
■ AC Characteristics

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}	50			ns
Chip enable setup time	t_{CE}			450	ns
Chip enable precharge time	t_p	300			ns
Chip turn-off time (CE)	t_{DF1}			300	ns
Chip turn-off time (CS)	t_{DF2}			300	ns
Cycle time	t_{CYC}	750			ns

Test conditions of AC characteristics

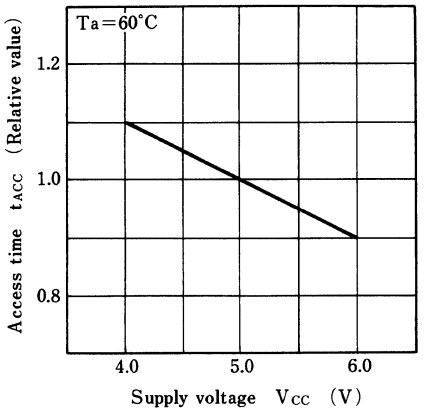
- Input voltage amplitude ····· +0.8V～V_{CC}−1.0V
- Input rising/falling time ····· 10ns
- Input threshold level ····· 1.5V
- Output threshold level ····· 0.4V and 2.4V
- Output load condition ····· 10pF

■ Timing Diagram

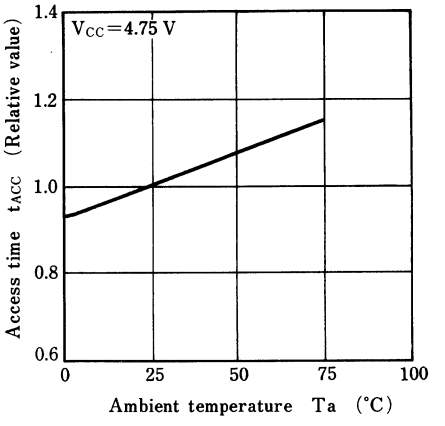


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

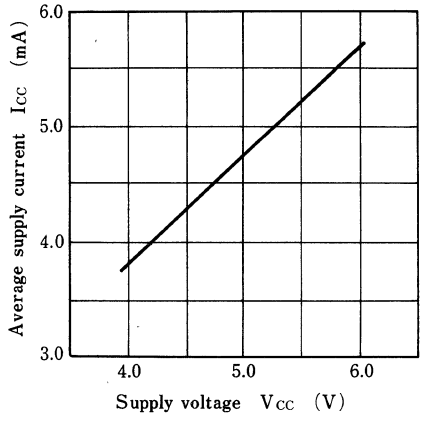
Access time vs. supply voltage



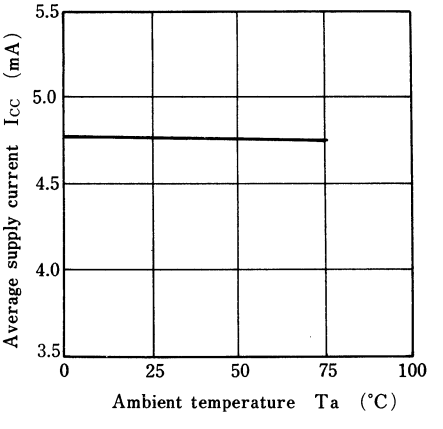
Access time vs. ambient temperature



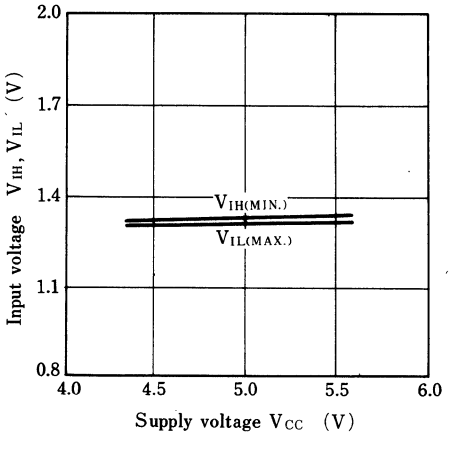
Average supply current vs. supply voltage



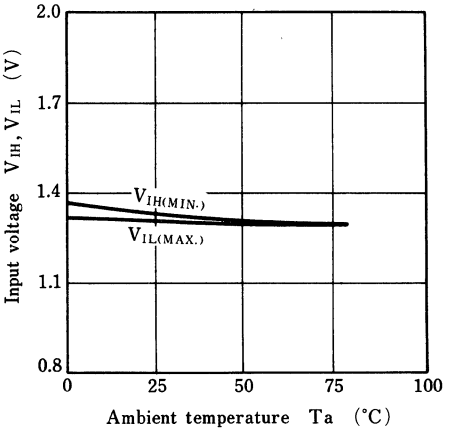
Average supply current vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



LH5396/LH5396A

CMOS 98304-Bit Mask Programmable Read Only Memory

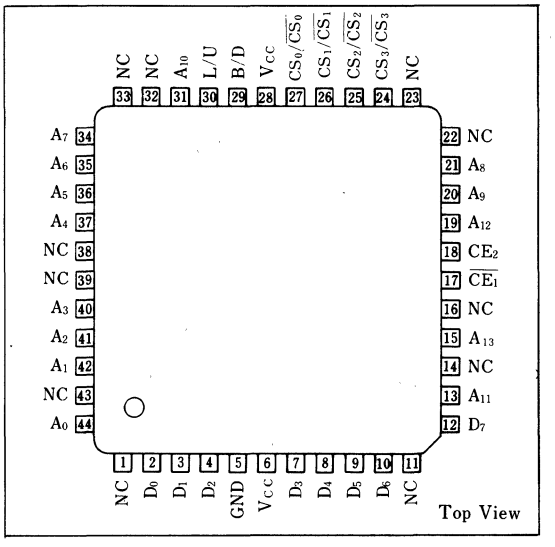
■ Description

The LH5396/LH5396A are mask programmable ROMs organized as 12,288-word-by-8-bit by using silicon-gate CMOS process technology.

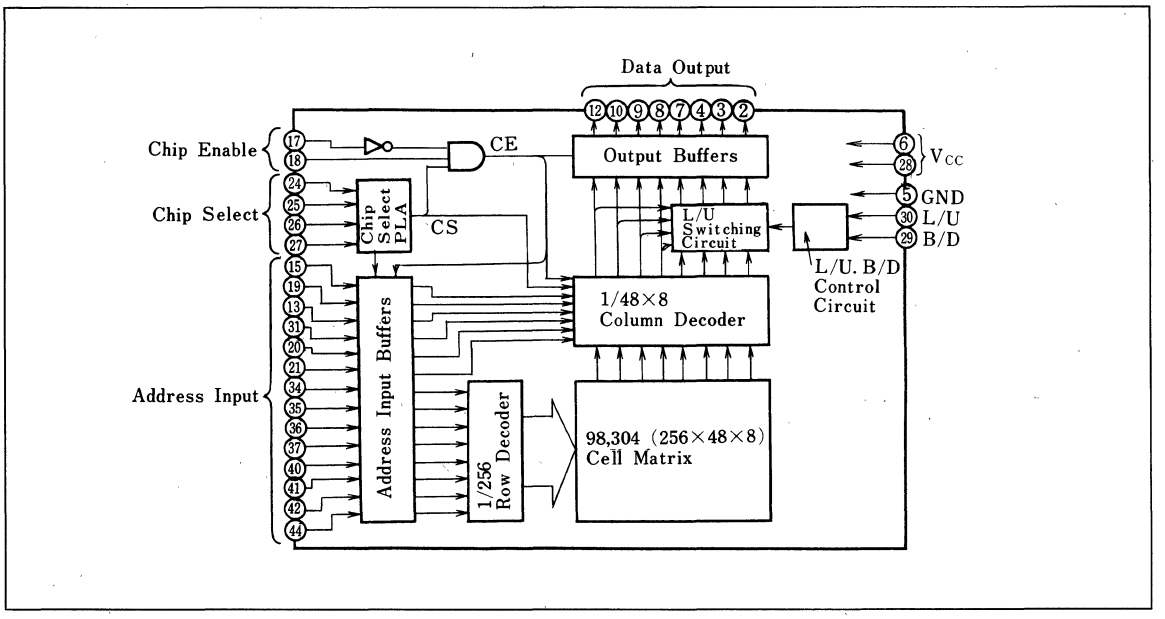
■ Features

1. 12,288-word-by-8-bit organization
2. Single +4.5V power supply
3. Low power consumption
4. Edge enabled operation ($\overline{CE_1}$, CE_2)
5. Three-state outputs
6. Access time (MAX.)
   LH5396 : 6.0 μs, LH5396A : 3.0 μs
7. Programmable chip select
8. Byte/digit output select
9. 44-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.0	4.5	5.0	V
Input voltage	V_{IL}	−0.3		0.8	V
	V_{IH}	V_{CC}−1.0		V_{CC}	V
Operating temperature	T_{opr}	0		60	℃

■ DC Characteristics

(V_{CC}=4.5V±10%, Ta=0～+60℃)

Parameter	Symbol	Conditions	LH5396			LH5396A			Unit	Note
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Input low voltage	V_{IL}		−0.3		0.8	−0.3		0.8	V	
Input high voltage	V_{IH}		V_{CC}−1.0		V_{CC}	V_{CC}−1.0		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=1.6mA			0.4			0.4	V	
Output high voltage	V_{OH}	I_{OH}=100 μA	2.4			2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V or V_{IN}=V_{CC}			1.0			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$	In non-selection mode : V_{OUT}=0V or V_{OUT}=V_{CC}			1.0			1.0	μA	
Chip enabled power supply current	I_{CC1}			3.0	7.0		5.0	12.0	mA	1
Chip disabled power supply current	I_{CC2}				5.0			5.0	μA	2

Note 1: Average current at cycle time of 4.5 μs (LH5396 is 7.5 μs) with output open and input set to 0V or V_{CC}.
Note 2: In chip selection mode : V_{IN}=0.2V or V_{IN}=V_{CC}−0.2V

■ AC Characteristics

(V_{CC}=4.5V±10%, Ta=0～+60℃)

Parameter	Symbol	LH5396			LH5396A			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Address setup time	t_{AS}	1.0			1.0			μs
Chip enable setup time	t_{CE}			6.0			3.0	μs
Chip enable precharge time	t_p	1.5			1.5			μs
Chip turn-off time (CE)	t_{DF1}			1.5			1.0	μs
Chip turn-off time (CS)	t_{DF2}			1.5			1.0	μs
Cycle time	t_{CYC}			10,000			10,000	μs

Test conditions of AC characteristics

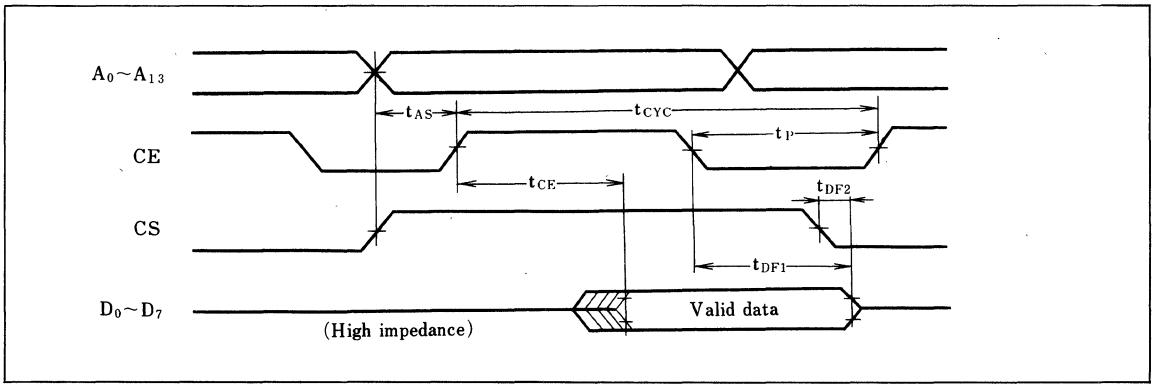
- Input voltage amplitude ····· +0.8V～V_{CC}−1.0V
- Input rising/falling time ····· 20ns
- Input threshold level ····· 1.5V
- Output threshold level ····· 0.4V and 2.4V
- Output load condition ····· 10pF

Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			15	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			15	pF

Timing Diagram



Chip Select

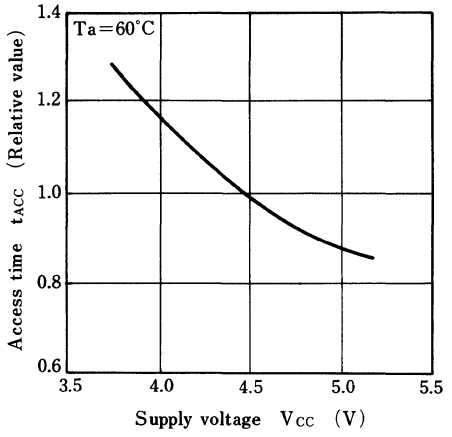
$CS_0/\overline{CS_0}$~$CS_3/\overline{CS_3}$	$\overline{CE_1}$	CE_2	D_0~D_7	Mode
In selection mode	L	H	D_{OUT}	Read
	L	L	High impedance	Non-selection
	H	L		
	H	H		
In non-selection mode	X	X		

Byte/Digit Output Select

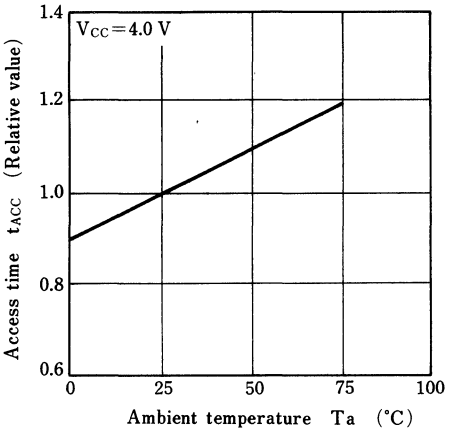
L/U	B/D	Data output pins							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
H	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
H	H	D_7	D_6	D_5	D_4	D_7	D_6	D_5	D_4

Electrical Characteristics Curves (Ta=25℃ unless otherwise specified)

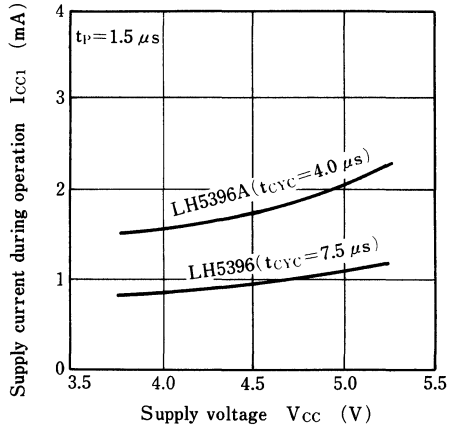
Access time vs. supply voltage



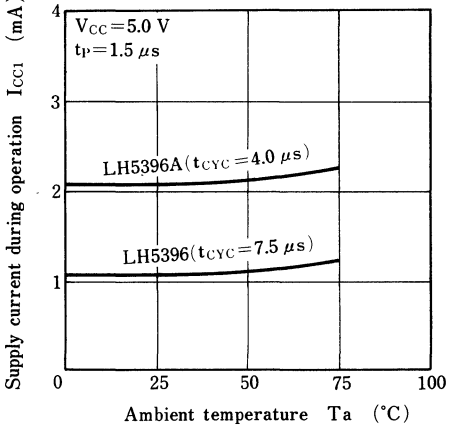
Access time vs. ambient temperature



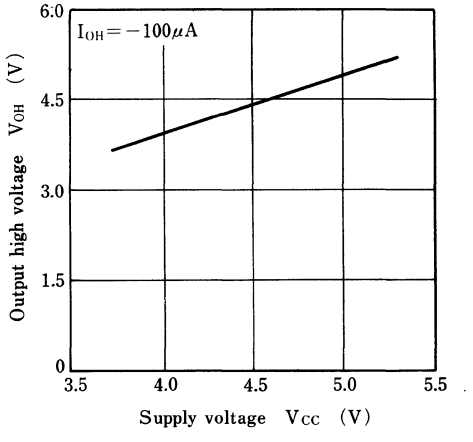
Supply current during operation vs. supply voltage



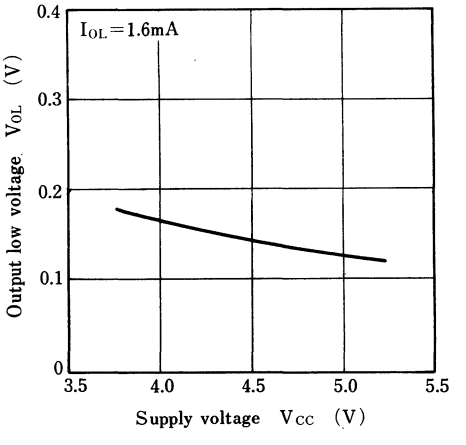
Supply current during operation vs. ambient temperature



Output high voltage vs. supply voltage



Output low voltage vs. supply voltage



LH5396S CMOS 98304-Bit Mask Programmable Read Only Memory

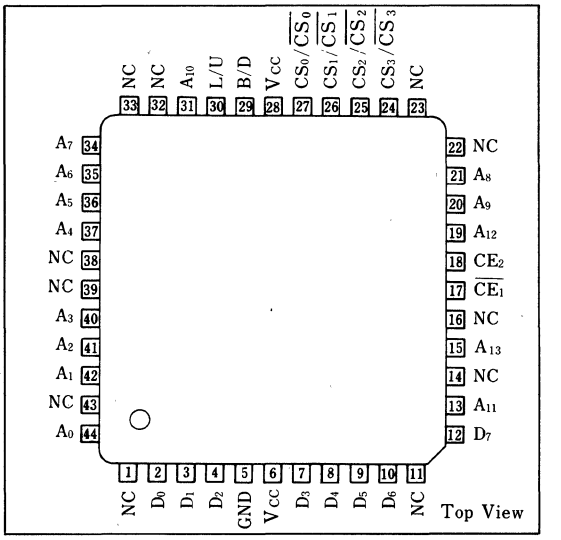
Description

The LH5396S is a mask programmable ROM organized as 12,288-word-by-8-bit by using silicon-gate CMOS process technology.

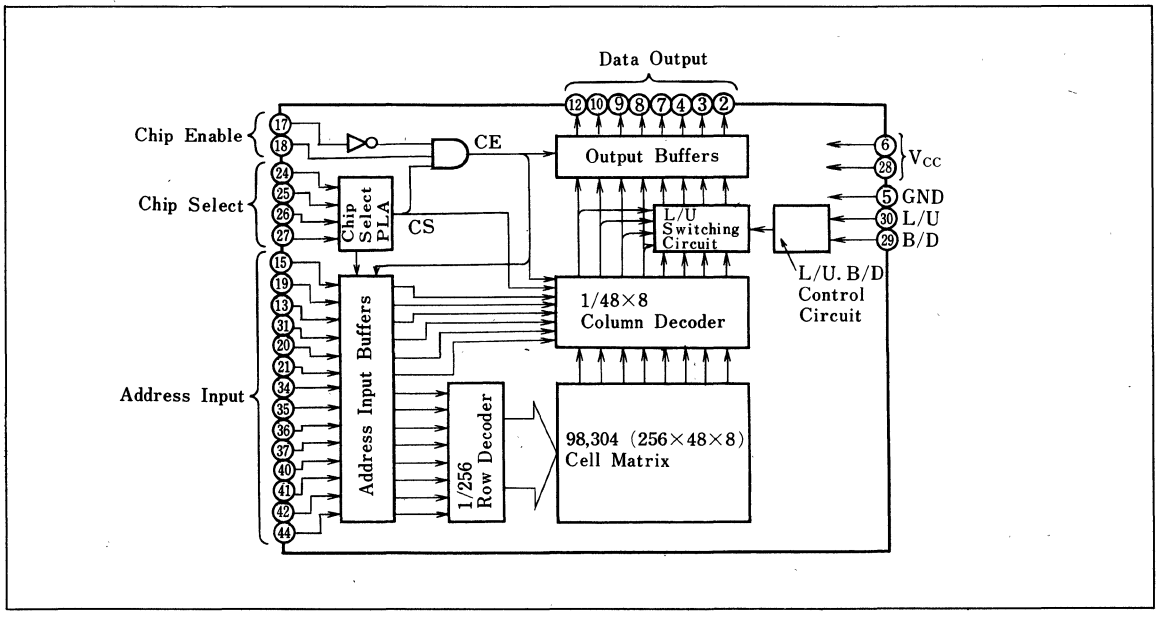
Features

1. 12,288-word-by-8-bit organization
2. Single +3V power supply
3. Low power consumption
4. Edge enabled operation ($\overline{CE_1}$, CE_2)
5. Three-state outputs
6. Access time (MAX.) : 15 μs
7. Programmable chip sclect
8. Byte/digit output select
9. 44-pin quad-flat package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+5.0	V
Input voltage*	V_{IN}	−0.3～+5.0	V
Output voltage*	V_{OUT}	−0.3～+5.0	V
Operating temperature	T_{opr}	0～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	2.6	3	3.4	V
Input voltage	V_{IL}	−0.3		0.5	V
	V_{IH}	V_{CC}−0.5		V_{CC}	
Operating temperature	T_{opr}	0		60	℃

■ DC Characteristics

(V_{CC}=+2.6～+3.4V, Ta=0～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{IL}		−0.3		0.5	V	
Input high voltage	V_{IH}		V_{CC}−0.5		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=300 μA			0.3	V	
Output high voltage	V_{OH}	I_{OH}=30 μA	V_{CC}−0.3			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V or V_{CC}			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$	In non-selection mode : V_{OUT}=0V or V_{CC}			1.0	μA	
Chip enabled power supply current	I_{CC1}			0.8	2.0	mA	1
Chip disabled power supply current	I_{CC2}				2.0	μA	2

Note 1: Average current at cycle time of 18 μs with output open and input set to 0V or V_{CC}.
Note 2: In chip selection mode : V_{IN}=0.2V or V_{IN}=V_{CC}−0.2V

■ AC Characteristics

(V_{CC}=+2.6V～+3.4V, Ta=0～+60℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}	2.0			μs
Chip enable setup time	t_{CE}			15	μs
Chip enable precharge time	t_p	3.0			μs
Chip turn-off time (CE)	t_{DF1}			3.0	μs
Chip turn-off time (CS)	t_{DF2}			3.0	μs
Cycle time	t_{CYC}			10,000	μs

Test conditions of AC characteristics

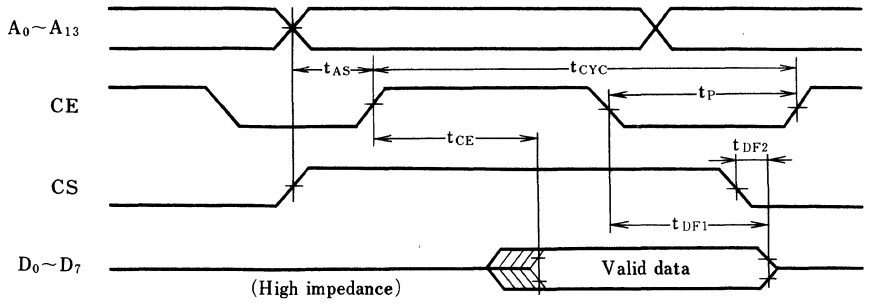
- Input voltage amplitude ····· +0.5V～V_{CC}−0.5V
- Input rising/falling time ····· 20ns
- Input threshold level ····· V_{CC}/2
- Output threshold level ····· 0.3V and V_{CC}−0.3V
- Output load condition ····· Non loading

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			15	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			15	pF

■ Timing Diagram



■ Chip Select

$CS_0/\overline{CS_0}$~$CS_3/\overline{CS_3}$	$\overline{CE_1}$	CE_2	D_0~D_7	Mode
In selection mode	L	H	D_{OUT}	Read
	L	L	High impedance	Non-selection
	H	L		
	H	H		
In non-selection mode	X	X		

■ Byte/Digit Output Select

L/U	B/D	Data output pins							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
H	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
H	H	D_7	D_6	D_5	D_4	D_7	D_6	D_5	D_4

LH23126 NMOS 131072-Bit Mask Programmable Read Only Memory

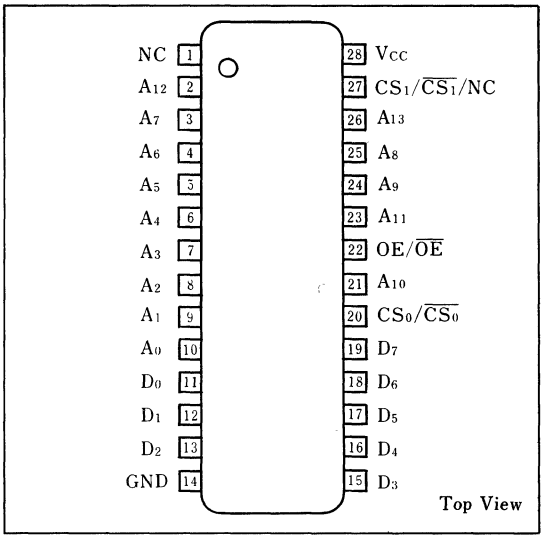
■ Description

The LH23126 is a fully static mask programmable ROM organized as 16,384-word-by-8-bit by using NMOS process technology.

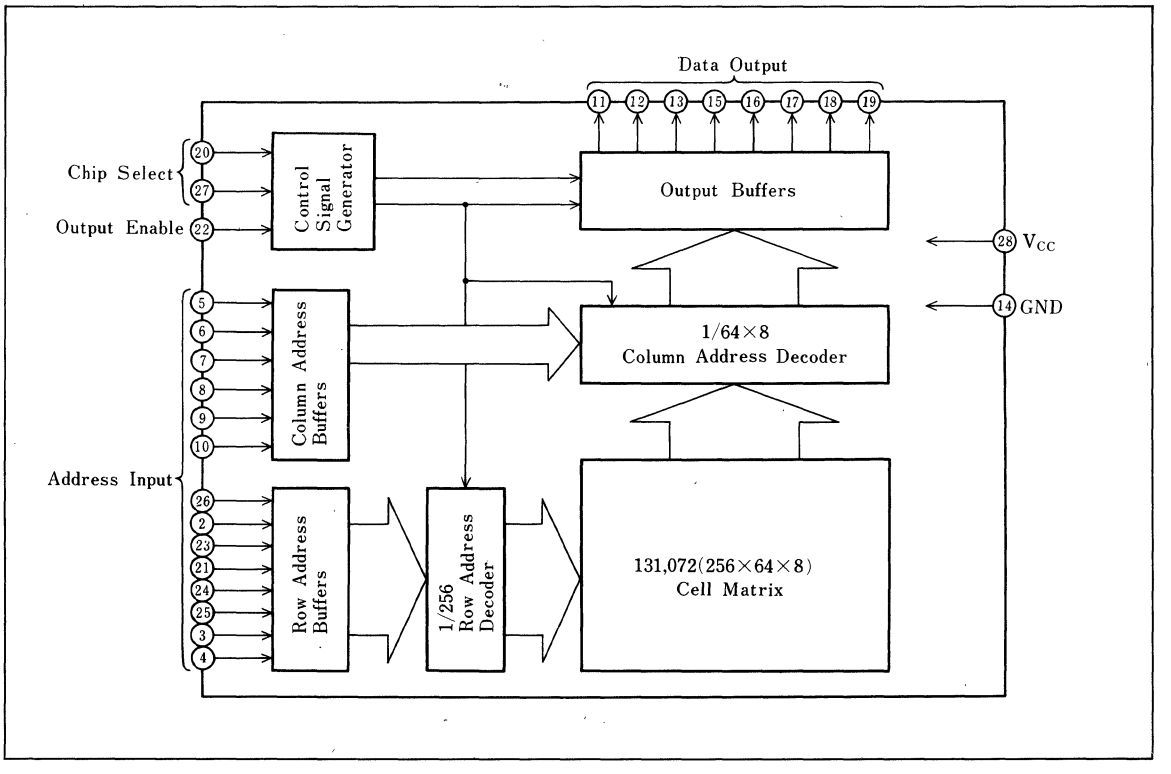
■ Features

1. 16,384-word-by-8-bit organization
2. Single +5V power supply
3. Fully static operation (no clock required)
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.) : 250ns
7. Programmable chip select
8. Programmable output enable
9. 28-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5	5.5	V
Input voltage	V_{IL}			0.8	V
	V_{IH}	2.2			V

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage		V_{IL}		−0.3		0.8	V
Input high voltage		V_{IH}		2.2		V_{CC}	V
Output low voltage		V_{OL}	I_{OL}=3.2mA			0.4	V
Output high voltage		V_{OH}	I_{OH}=−400μA	2.4			V
Input leakage current		$\lvert I_{LI} \rvert$	V_{IN}=0V～V_{CC}			10	μA
Output leakage current		$\lvert I_{LO} \rvert$	V_{OUT}=0～V_{CC} during standby			10	μA
Current consumption	During operation	I_{CC1}				80	mA
	During standby	I_{CC2}	CS≦0.8V, CS≧2.2V			40	mA

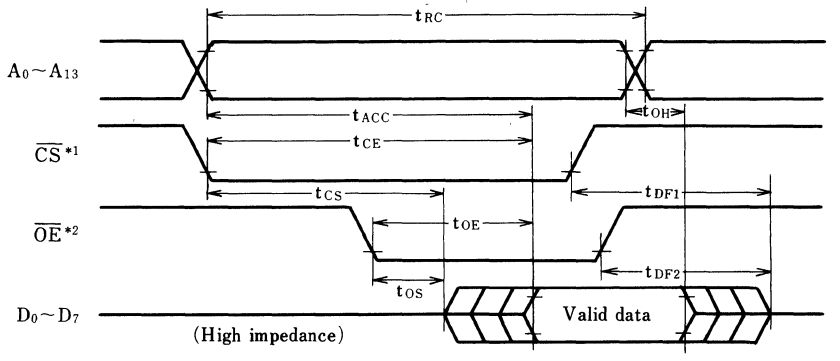
■ AC Characteristics (V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Read cycle time	t_{RC}	250			ns
Access time	t_{ACC}			250	ns
Chip enable time	t_{CE}			250	ns
Output enable time	t_{OE}			100	ns
Chip select time	t_{CS}	10			ns
Output select time	t_{OS}	10			ns
Output turn-off time (from $\overline{CS}$)	t_{DF1}			70	ns
Output turn-off time (from $\overline{OE}$)	t_{DF2}			70	ns
Output hold time	t_{OH}	10			ns

Conditions for measurement of AC characteristics

- Input voltage amplitude ····· +0.4～+2.4V
- Input rising/falling time ····· 20ns
- Input decision level ····· 1.5V
- Output dicision level ····· 0.8V and 2.0V
- Output load condition ····· 1TTL+100pF

Timing Diagram



*1 CS is the reverse polarity of $\overline{CS}$
CS/$\overline{CS}$ is the logical product of $CS_0/\overline{CS_0}$ and $CS_1/\overline{CS_1}$/NC
*2 OE is the reverse polarity of $\overline{OE}$

Chip Select

CS/$\overline{CS}$	OE/$\overline{OE}$	D_0~D_7	Mode
H/L	H/L	D_{OUT}	Operating
	L/H	High impedance	Operating
L/H			Standby

LH53127 CMOS 131072-Bit Mask Programmable Read Only Memory

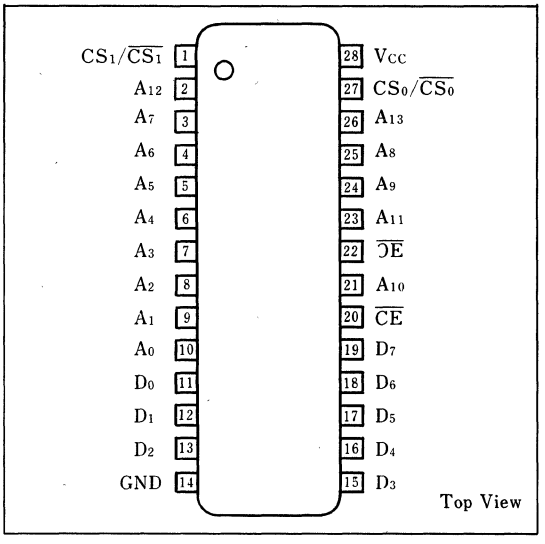
Description

The LH53127 is a mask programmable ROM organized as 16,384-word-by-8-bit by using poly-crystal silicon-gate CMOS process technology.

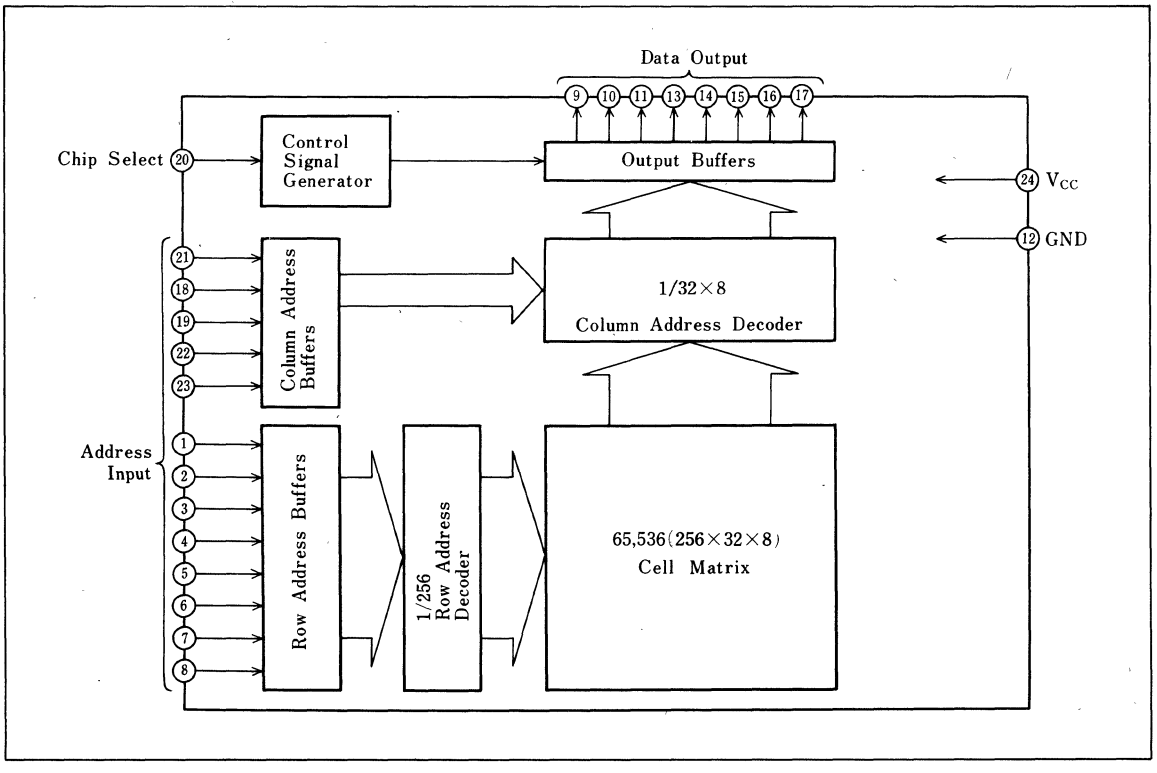
Features

1. 16,384-word-by-8-bit organization
2. Single +5V power supply
3. Low power consumption
4. Edge enabled operation
5. All inputs and outputs TTL compatible
6. Three-state outputs
7. Access time (MAX.) : 250ns
8. Programmable chip select
9. 28-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage*	V_{OUT}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5	5.5	V
Input voltage	V_{IL}			0.8	V
	V_{IH}	2.2			

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{IL}		−0.3		0.8	V	
Input high voltage	V_{IH}		2.2		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=2.0mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V～V_{CC}			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$				1.0	μA	1
Current consumption	I_{CC1}				8	mA	2
	I_{CC2}				1	mA	3
Current consumption during standby	I_{SB}	$\overline{CE}$=V_{CC}, V_{IN}=0V or V_{CC}			30	μA	

Note 1 : During high impedance output, $\overline{CE}$=2.2V or $\overline{OE}$=2.2V, V_{OUT}=0V～V_{CC}
Note 2 : During operation, input amplitude is 0V or V_{CC}, t_{CYC}=350 ns and output pin is open.
Note 3 : During chip non-select, input amplitude is 0V or V_{CC}, t_{CYC}=350 ns, and output pin is open.

■ AC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{CYC}	350			ns
Access time from $\overline{CE}$	t_{CE}			250	ns
Access time from CS/$\overline{CS}$	t_{CS}			250	ns
Access time from $\overline{OE}$	t_{OE}			100	ns
Address setup time (from $\overline{CE}$)	t_{ASE}	0			ns
Address setup time (from CS)	t_{ASS}	0			ns
$\overline{CE}$ precharge time	t_{PE}	100			ns
CS/$\overline{CS}$ precharge time	t_{PS}	100			ns
Data off delay time from $\overline{CE}$	t_{OF1}	0		100	ns
Data off delay time from CS/$\overline{CS}$	t_{OF2}	0		100	ns
Data off delay time from $\overline{OE}$	t_{OF3}	0		100	ns

Conditions for measurement of AC characteristics

- Input voltage frequency ..... 0.4V~2.4V
- Input rise/fall time 10ns
- Input decision level 1.5V
- Output decision level ..... 0.8V and 2.0V
- Output load condition ..... 1TTL+100pF

Address input requires that it should be defined during an active period.

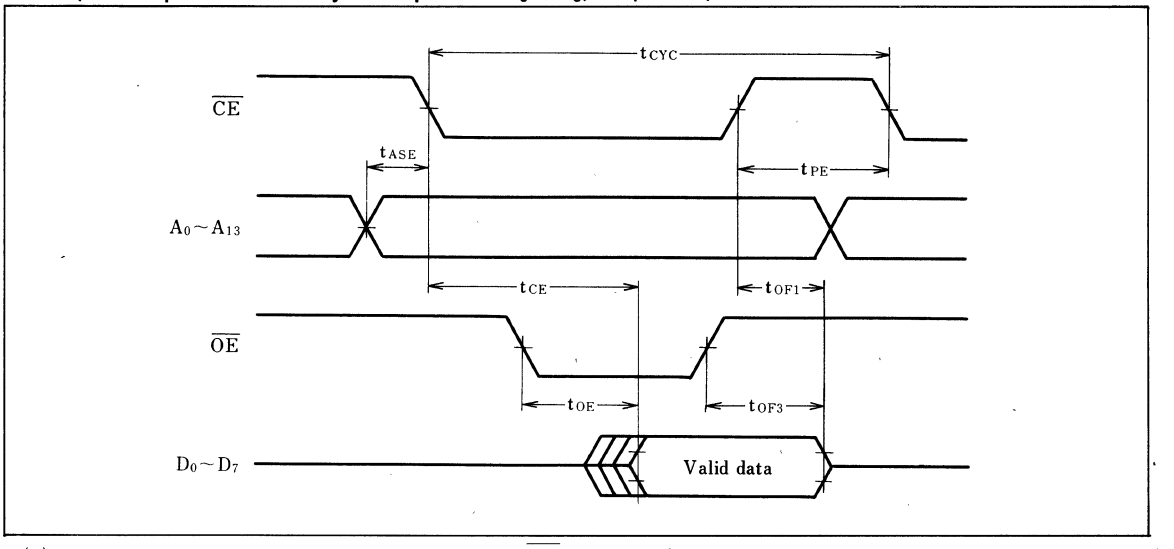
■ Capacitance

Parameter	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
Input capacitance	C_{IN}	V_{IN}=0V			10	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			10	pF

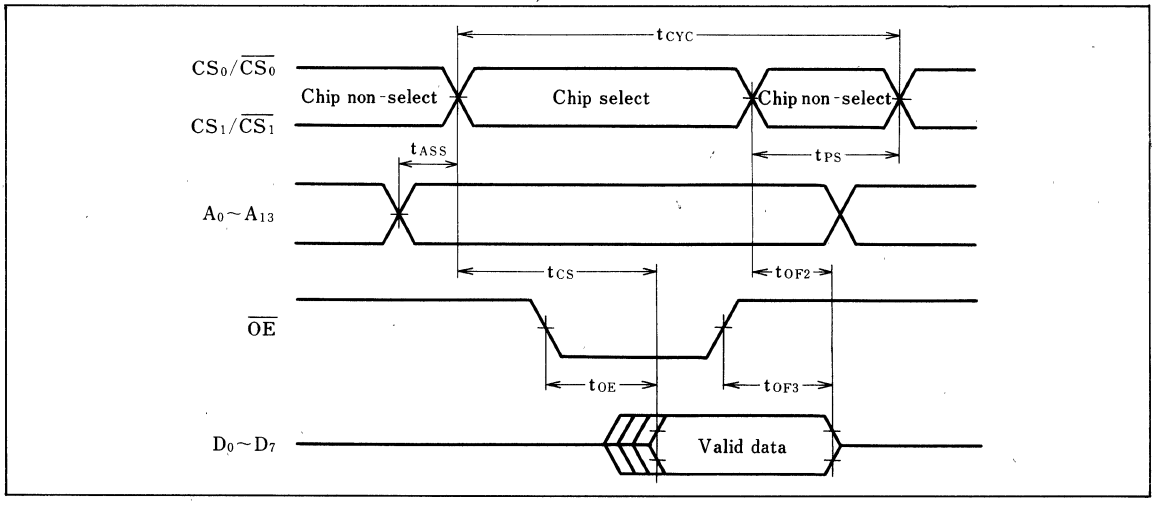
■ Timing Diagram

(1) When the $\overline{CE}$ input is used as the clock

(The chip is selected by the input of $CS_0/\overline{CS_0}$, CS_1 /$\overline{CS_1}$.)



(2) When the CS input is used as the clock ($\overline{CE} \leqq V_{IL(MAX.)}$)



■ Chip Select

$\overline{CE}$	$CS_0/\overline{CS_0}$, $CS_1/\overline{CS_1}$	$\overline{OE}$	$D_0 \sim D_7$	Mode
L	Select	L	Valid data output	Read
		H	High impedance	Output non-select
	Non-select	X		Non-select
H		X		Standby

LH53129 CMOS 131072-Bit Mask Programmable Read Only Memory

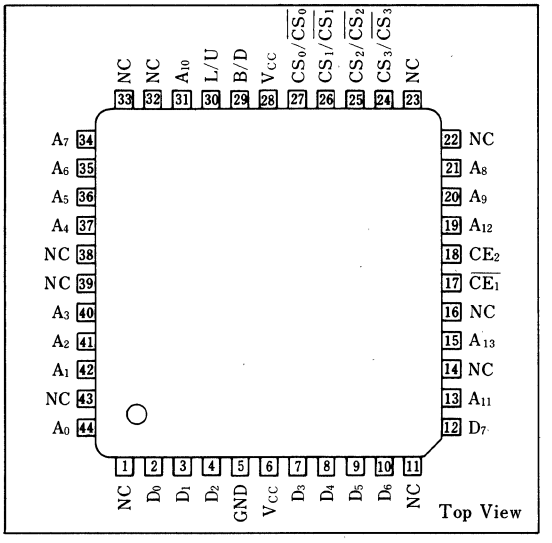
Description

The LH53129 is a mask programmable ROM organized as 16,384-word-by-8-bit by using silicon-gate CMOS process technology.

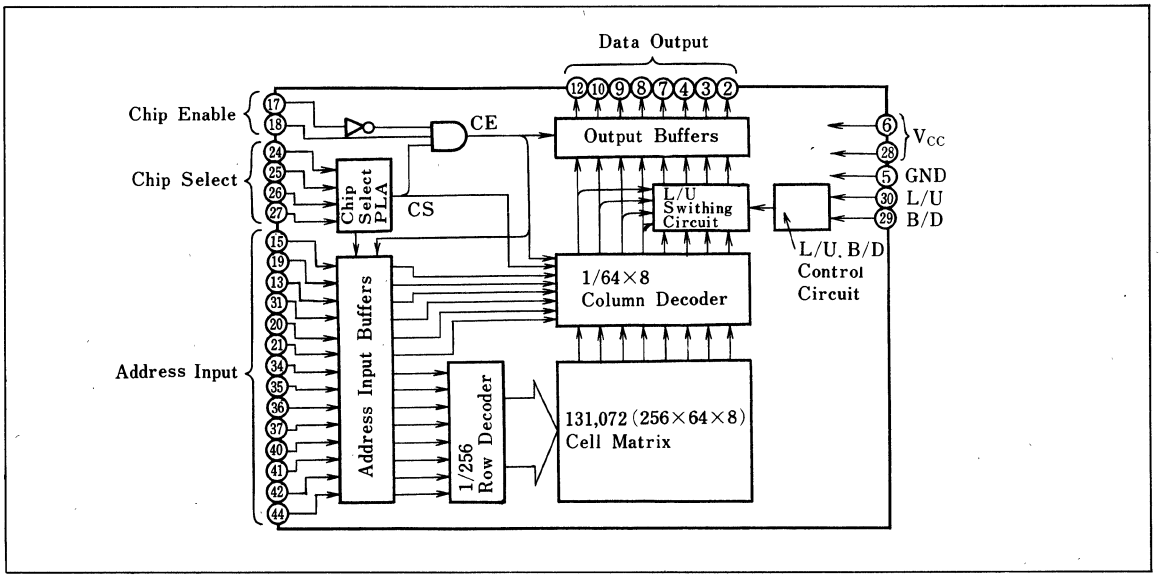
Features

1. 16,384-word-by-8-bit organization
2. Single +4.5V power supply
3. Low power consumption
4. Edge enabled operation ($\overline{CE}_1$, CE_2)
5. Three-state outputs
6. Access time (MAX.) : 6 μs
7. Programmable chip select
8. Byte/digit output select
9. 44-pin quad-flat package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.0	4.5	5.0	V
Input voltage	V_{IL}	−0.3		0.8	V
	V_{IH}	V_{CC}−1.0		V_{CC}	
Operating temperature	T_{opr}	0		60	℃

■ DC Characteristics

(V_{CC}=4.5V±10%, Ta=0～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{IL}		−0.3		0.8	V	
Input high voltage	V_{IH}		V_{CC}−1.0		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=1.6mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=100 μA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V～V_{CC}			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$	In non-selection, V_{OUT}=0V～V_{CC}			1.0	μA	
Chip enabled power supply current	I_{CC1}			3	7	mA	1
Chip disabled power supply current	I_{CC2}	CS, V_{IN}=0.2V or V_{CC}−0.2V			5.0	μA	

Note 1: Average current at cycle time of 7.5 μs with output open and input set to 0V or Vcc.

■ AC Characteristics

(V_{CC}=4.5V±10%, Ta=0～+60℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}	1			μs
Chip enable setup time	t_{CE}			6	μs
Chip enable precharge time	t_p	1.5			μs
Chip turn-off time (CE)	t_{DF1}			1.5	μs
Chip turn-off time (CS)	t_{DF2}			1.5	μs
Cycle time	t_{CYC}	7.5		10,000	μs

Test conditions of AC characteristics

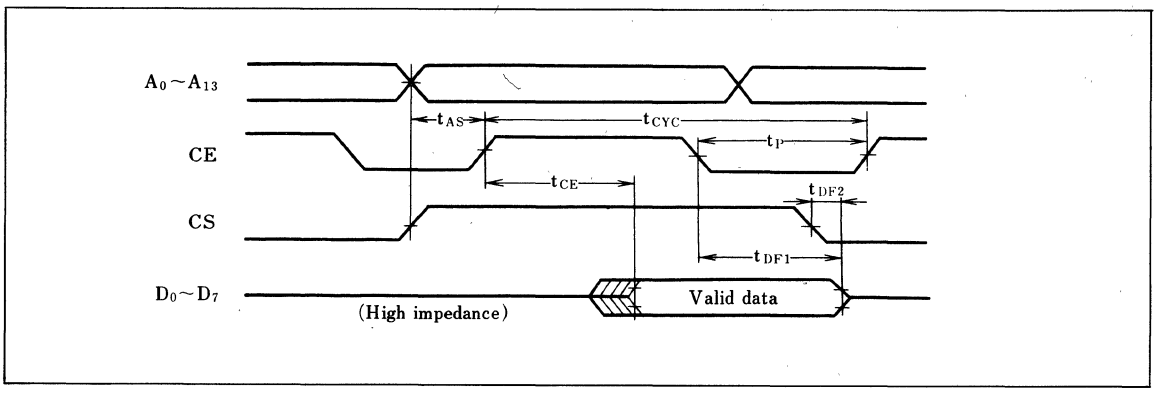
- Input voltage amplitude ····· +0.8V～V_{CC}−1.0V
- Input rising/falling time ····· 20ns
- Input threshold level ····· 1.5V
- Output threshold level ····· 0.4V and 2.4V
- Output load condition ····· 10pF

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			15	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			15	pF

■ Timing Diagram



■ Chip Select

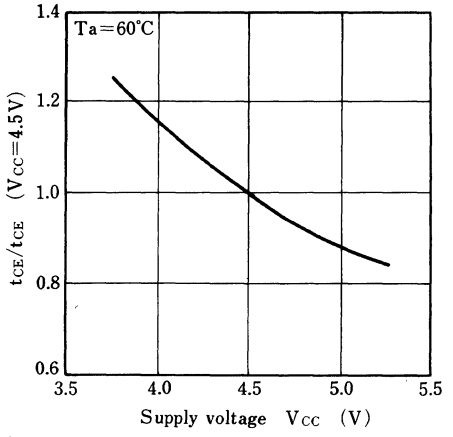
$CS_0/\overline{CS_0}$~$CS_3/\overline{CS_3}$	$\overline{CE_1}$	CE_2	D_0~D_7	Mode
In selection mode	L	H	D_{OUT}	Read
	L	L	High impedance	Non-selection
	H	L		
	H	H		
In non-selection mode	X	X		

■ Byte/Digit Output Select

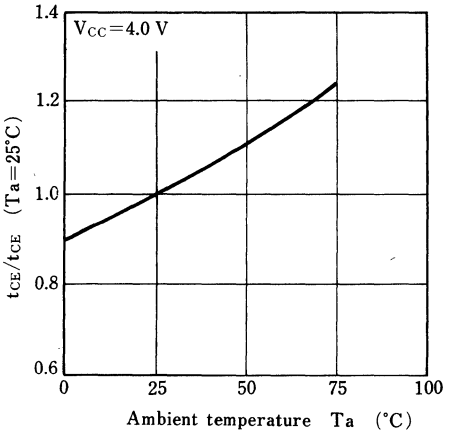
L/U	B/D	Data output pins							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
H	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
H	H	D_7	D_6	D_5	D_4	D_7	D_6	D_5	D_4

■ Electrical Characteristics Curves (Ta=25℃ unless otherwise specified)

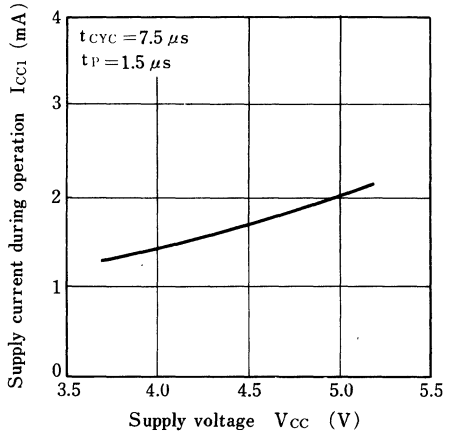
Normalized chip-enable delay time vs. supply voltage



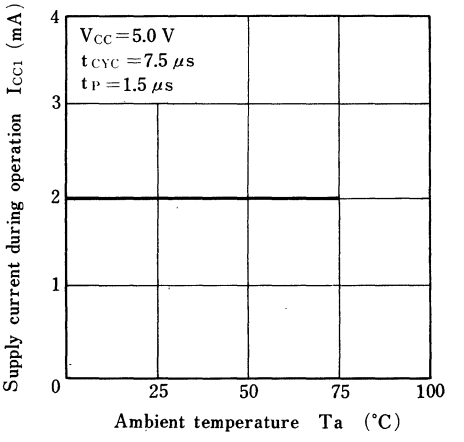
Normalized chip-enable delay time vs. ambient temperature



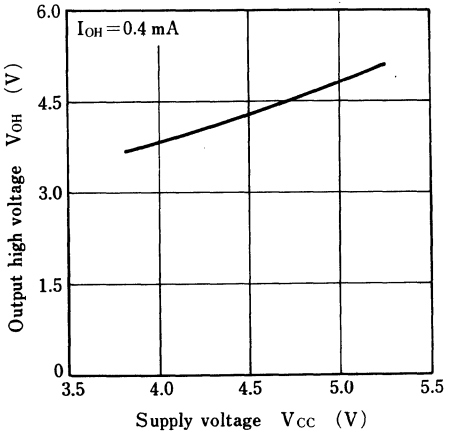
Supply current during operation vs. supply voltage



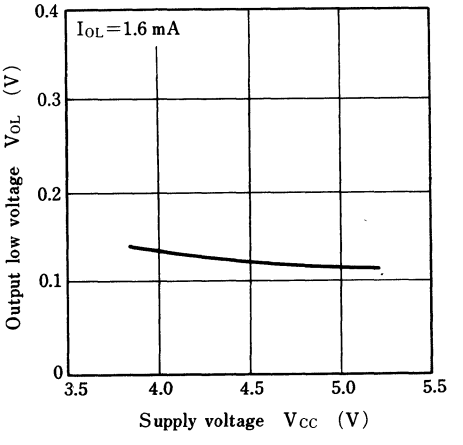
Supply current during operation vs. ambient temperature



Output high voltage vs. supply voltage



Output low voltage vs. supply voltage



8

LH53129A CMOS 131072-Bit Mask Programmable Read Only Memory

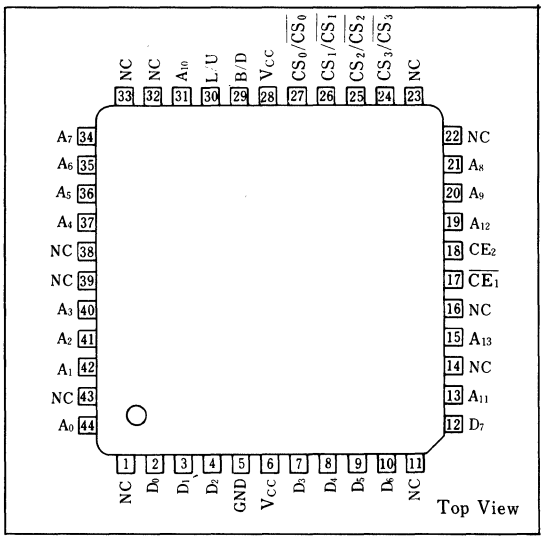
■ Description

The LH53129A is a mask programmable ROM organized as 16,384-word-by-8-bit by using silicon-gate CMOS process technology.

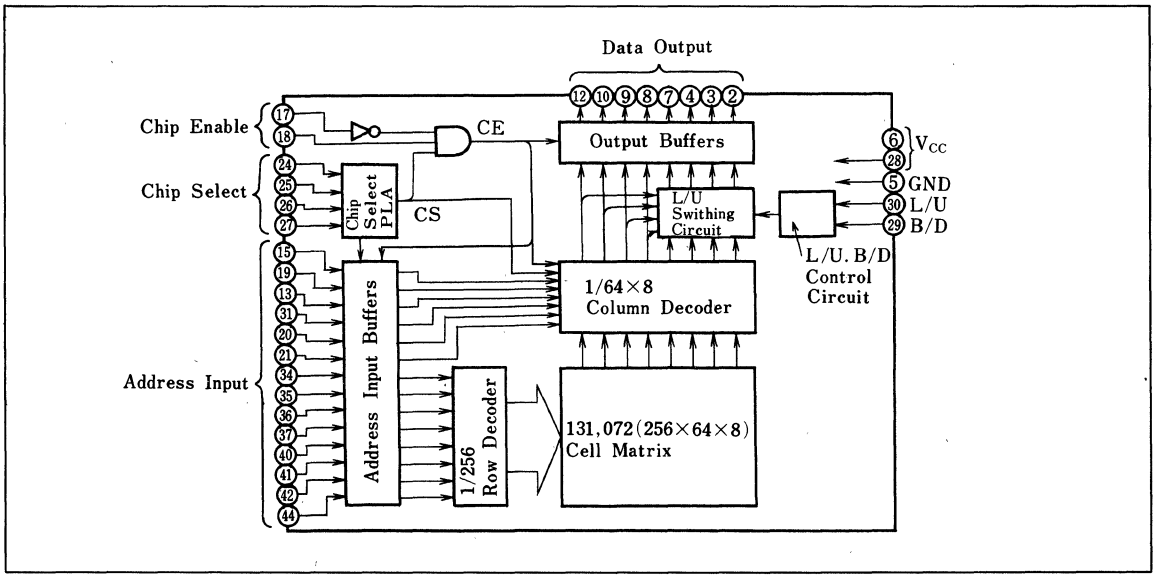
■ Features

1. 16,384-word-by-8-bit organization
2. Single +5V power supply
3. Low power consumption
4. Edge enabled operation ($\overline{CE}_1$, CE_2)
5. Three-state outputs
6. Access time (MAX.) : 2.5 μs
7. Programmable chip select
8. Byte/digit output select
9. 44-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	−5～+55	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5	5.5	V
Input voltage	V_{IL}	−0.3		0.8	V
	V_{IH}	V_{CC}−1.0		V_{CC}	
Operating temperature	T_{opr}	−5		55	℃

■ DC Characteristics

(V_{CC}=4.5V+5V±10%, Ta=−5～+55℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{IL}		−0.3		0.8	V	
Input high voltage	V_{IH}		V_{CC}−1.0		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=1.6mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=100 μA	2.4			V	
Input leakage current	$\|I_{LI}\|$	V_{IN}=0V～V_{CC}			1.0	μA	
Output leakage current	$\|I_{LO}\|$	In non-selection mode, V_{OUT}=0V～V_{CC}			1.0	μA	
Chip enabled power supply current	I_{CC1}			7	14	mA	1
Chip disabled power supply current	I_{CC2}	CS, V_{IN}=0.2V or V_{CC}−0.2V			5.0	μA	

Note 1: Average current at cycle time of 4.0 μs with output open and input set to 0V or Vcc.

■ AC Characteristics (V_{CC}=5V±10%, Ta=−5～+55℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}	1			μs
Chip enable setup time	t_{CE}			2.5	μs
Chip enable precharge time	t_p	1.5			μs
Chip turn-off time (CE)	t_{DF1}			1.5	μs
Chip turn-off time (CS)	t_{DF2}			1.5	μs
Cycle time	t_{CYC}			10,000	μs

Test conditions of AC characteristics

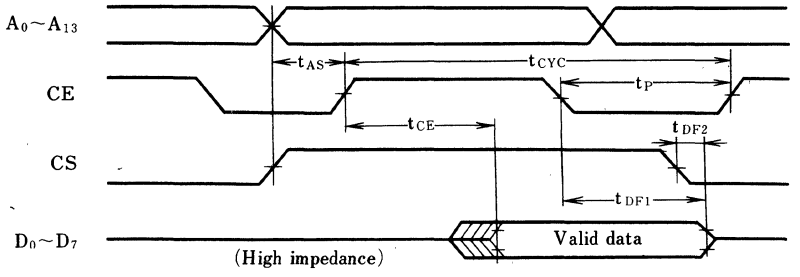
- Input voltage amplitude ····· +0.8V～V_{CC}−1.0V
- Input rising/falling time ····· 20ns
- Input threshold level ····· 1.5V
- Output threshold level ····· 0.4V and 2.4V
- Output load condition ····· 10pF

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			15	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			15	pF

■ Timing Diagram



■ Chip Select

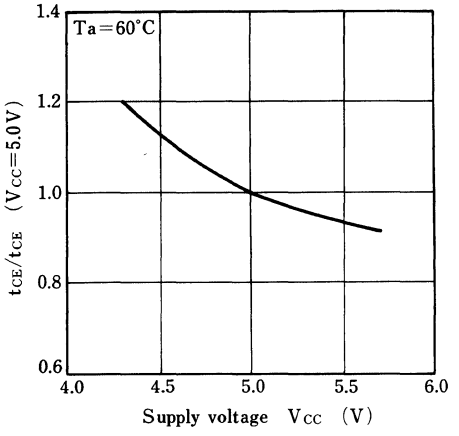
$CS_0/\overline{CS_0}$~$CS_3/\overline{CS_3}$	$\overline{CE_1}$	CE_2	D_0~D_7	Mode
In selection mode	L	H	D_{OUT}	Read
	L	L	High impedance	Non-selection
	H	L		
	H	H		
In non-selection mode	X	X		

■ Byte/Digit Output Select

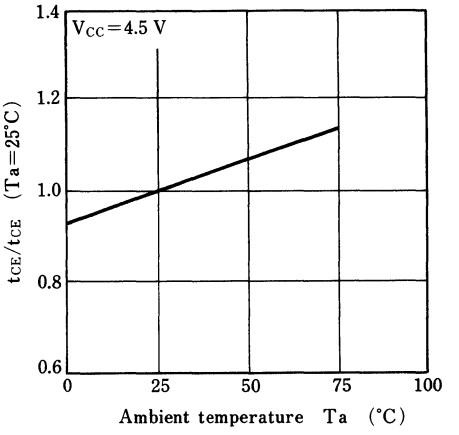
L/U	B/D	Data output pins							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
H	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
H	H	D_7	D_6	D_5	D_4	D_7	D_6	D_5	D_4

■ Electrical Characteristics Curves (Ta=25℃ unless otherwise specified)

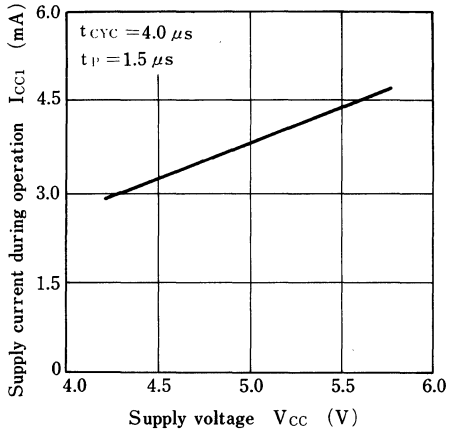
Normalized chip-enable delay time vs. supply voltage



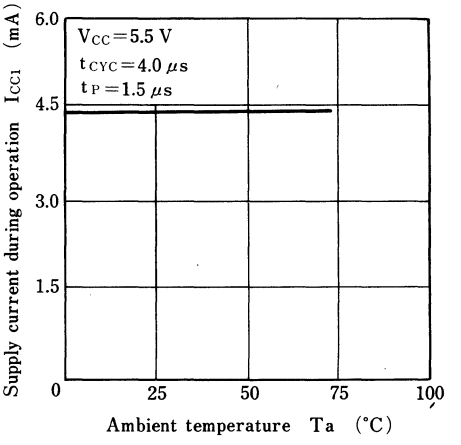
Normalized chip-enable delay time vs. ambient temperature



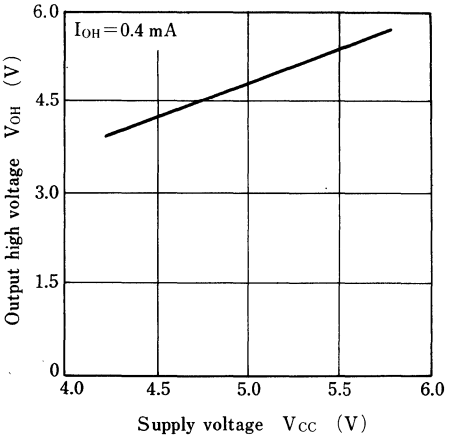
Supply current during operation vs. supply voltage



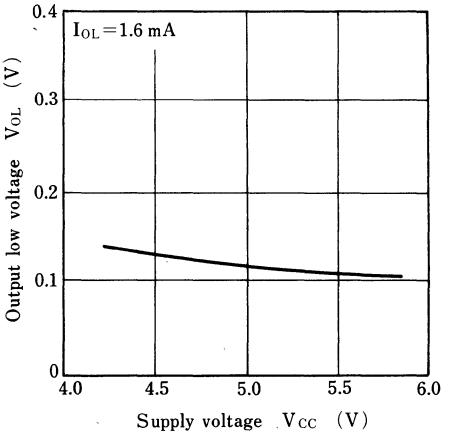
Supply current during operation vs. ambient temperature



Output high voltage vs. supply voltage



Output low voltage vs. supply voltage



LH23257 NMOS 262144-Bit Mask Programmable Read Only Memory

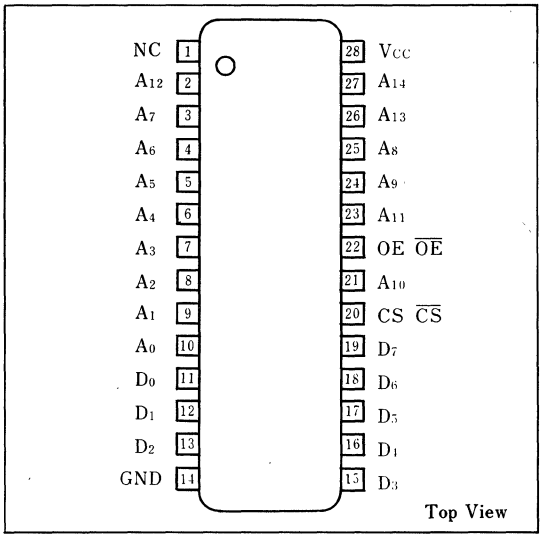
Description

The LH23257 is a fully static mask programmable ROM organized as 32,768-word-by-8-bit by using silicon-gate CMOS process technology.

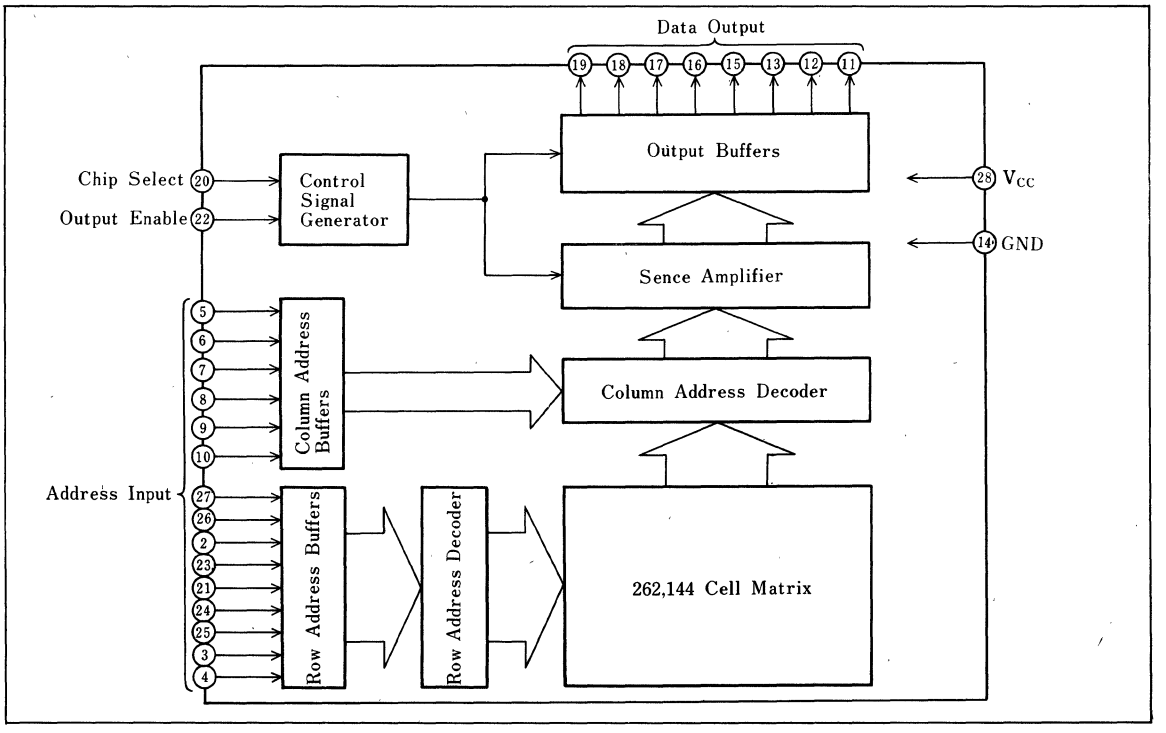
Features

1. 32,768-word-by-8-bit organization
2. Single +5V power supply
3. Fully static operation (No clock required)
4. All input and output TTL compatible
5. Three-state outputs
6. Access time (MAX.) : 250ns
7. Programmable chip select
8. Programmable output enable
9. 28-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5	5.5	V
Input voltage	V_{IL}	−0.3		0.8	V
	V_{IH}	2.2		V_{CC}	V

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage		V_{IL}		−0.3		0.8	V
Input high voltage		V_{IH}		2.2		V_{CC}	V
Output low voltage		V_{OL}	I_{OL}=3.2mA			0.4	V
Output high voltage		V_{OH}	I_{OH}=−400 μA	2.4			V
Input leakage current		$\|I_{LI}\|$	V_{IN}=0～5.5V			10	μA
Output leakage current		$\|I_{LO}\|$	V_{OUT}=0～5.5V during standby			10	μA
Current consumption	during operation	I_{CC1}	I_{OUT}=0mA			80	mA
	during standby	I_{CC2}	$\overline{CS}$≦0.8V, $\overline{CS}$≧2.2V			45	mA

■ AC Characteristics (V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Read cycle time	t_{RC}	250			ns
Access time	t_{ACC}			250	ns
Chip enable time	t_{CE}			250	ns
Output enable time	t_{OE}			100	ns
Chip select time	t_{CS}	10			ns
Output select time	t_{OS}	10			ns
Output turn-off time (from $\overline{CS}$)	t_{DF1}			70	ns
Output turn-off time (from $\overline{OE}$)	t_{DF2}			70	ns
Output hold time	t_{OH}	10			ns

Conditions for measurement of AC characteristics

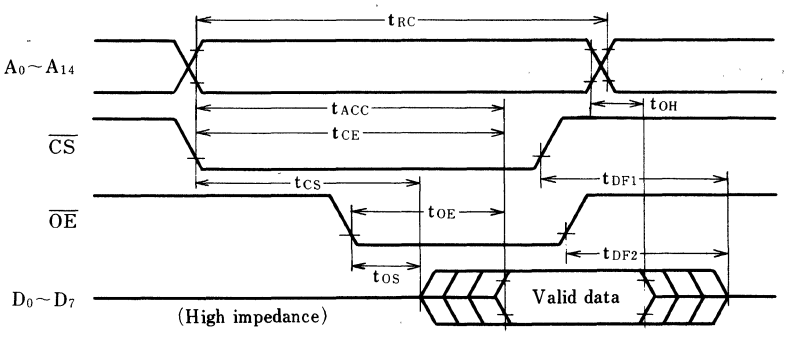
- Input voltage frequency ····· +0.4～+2.4V
- Input rise/fall time ····· 20ns
- Input decision level ····· 1.5V
- Output decision level ····· 0.8V, 2.0V
- Output load ····· 1TTL+100pF

■ Pin Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			8	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			12	pF

■ Timing Diagram

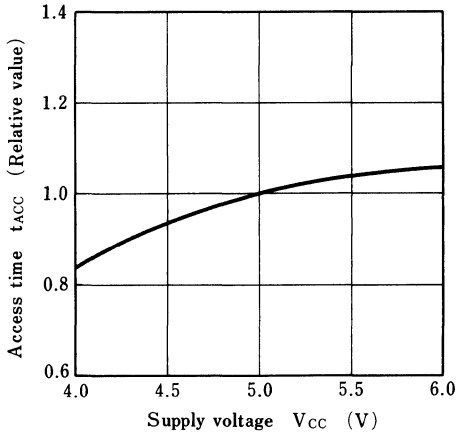


■ Chip Select

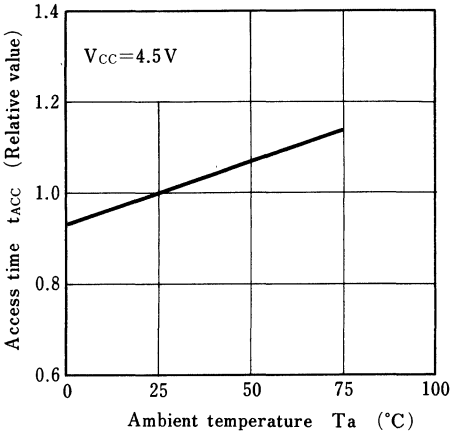
CS/$\overline{CS}$	OE/$\overline{OE}$	Output	Current consumption
L/H		High impedance	Standby
H/L	L/H		Operating
	H/L	D_{OUT}	

■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

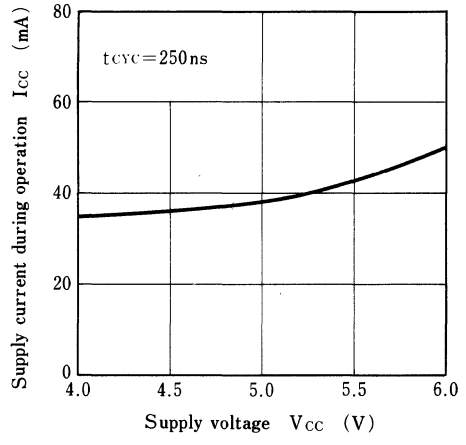
Access time vs. supply voltage



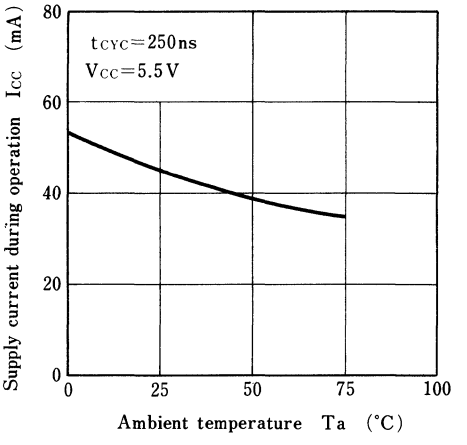
Access time vs. ambient temperature



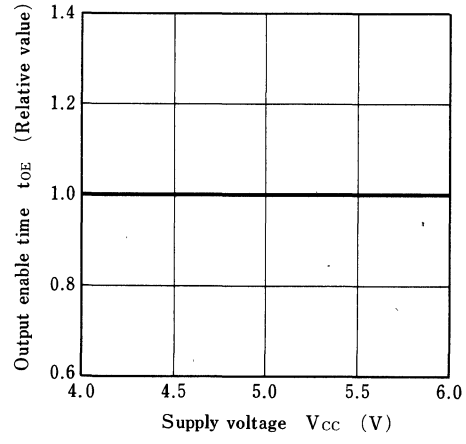
Supply current during operation vs. supply voltage



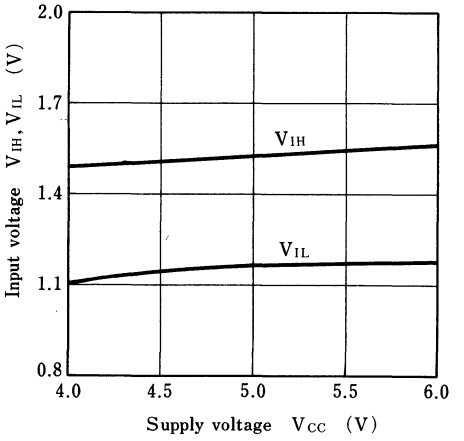
Supply current during operation vs. ambient temperature



Output enable time vs. supply voltage



Input voltage vs. supply voltage



LH53256 CMOS 262144-Bit Mask Programmable Read Only Memory

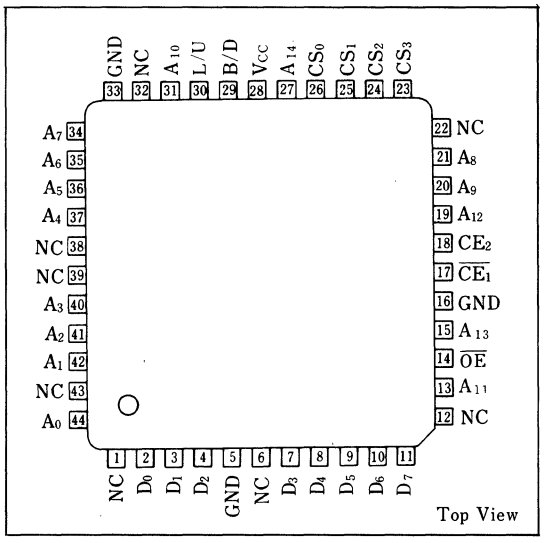
Description

The LH53256 is a mask programmable ROM organized as 32,768-word-by-8-bit by using silicon-gate CMOS process technology.

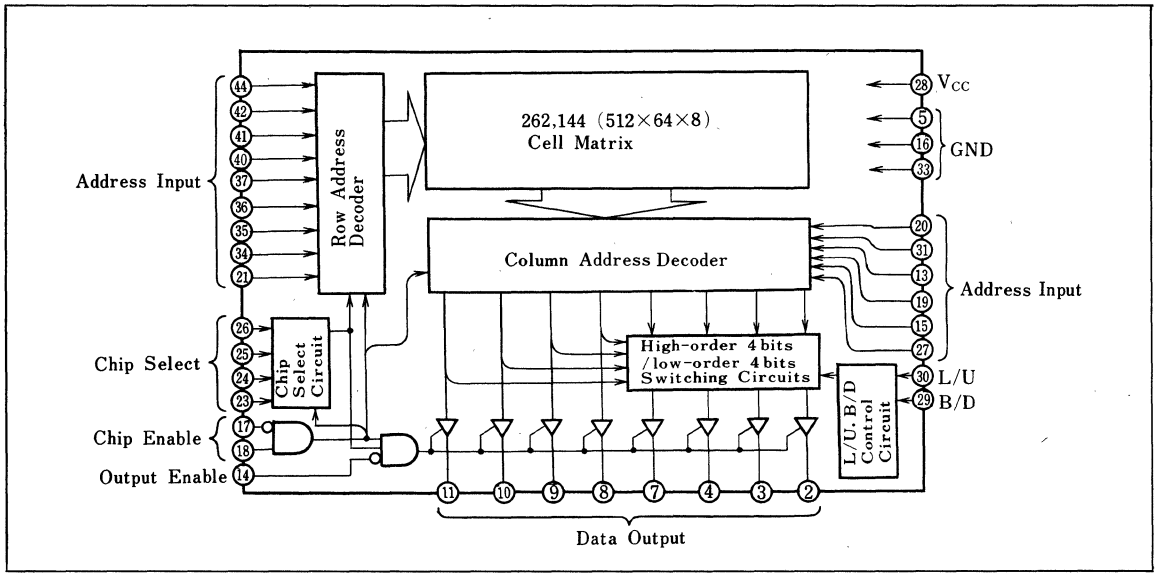
Features

1. 32,768-word-by-8-bit organization
2. Single +5V power supply
3. Low power consumption
4. Edge enable operation ($\overline{CE}_1$, CE_2)
5. Three-state outputs
6. Access time (MAX.) : 800ns
7. Programmable chip sclect
8. Byte/digit output select
9. 44-pin quad-flat package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*	V_{IN}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum application voltage on any pin with respect to GND.

■ DC Characteristics

(V_{CC}=5.0V±10%, Ta=0～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{IL}		−0.3		0.6	V	
Input high voltage	V_{IH}		V_{CC}−0.4		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=2.0mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V～V_{CC}			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$				1.0	μA	1
Chip enabled power supply current	I_{CC1}				10	mA	2
Chip disabled power supply current	I_{CC2}				50	μA	3
Input capacitance	C_{IN}				5	pF	4
Output capacitance	C_{OUT}				10	pF	4

Note 1: $\overline{CE_1}$=Vcc−0.2V or CE2=0.2V or $\overline{OE}$=Vcc−0.2V, VOUT=0V～Vcc
Note 2: Input amplitude : 0.4V～Vcc−0.4V, tcyc=900ns, output open
Note 3: $\overline{CE_1}$=Vcc−0.2V, CE2=0.2V
Note 4: Ta=25℃, f=1MHz

■ AC Characteristics (V_{CC}=5.0V±10%, Ta=0～+60℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Chip enable setup time	t_{CE}			800	ns
Output enable time	t_{OE}			100	ns
Address setup time	t_{AS}	30			ns
Address hold time	t_{AH}	100			ns
Chip turn-off time ($\overline{CE}$)	t_{DF1}			100	ns
Chip turn-off time ($\overline{OE}$)	t_{DF2}			100	ns
Chip enable precharge time	t_p	100			ns
Cycle time	t_{CYC}	900			ns

Test conditions of AC characteristics

- Input voltage amplitude ····· +0.4V～V_{CC}−0.4V
- Input rising/falling time ····· 20ns
- Input threshold level ····· 1.5V
- Output threshold level ····· 0.4V and 2.4V
- Output load condition ····· 10pF

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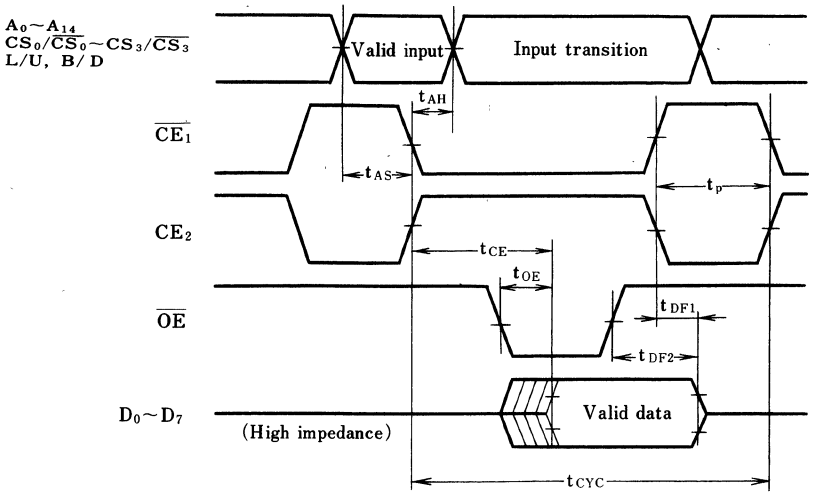
■ Timing Diagram



■ Chip Select

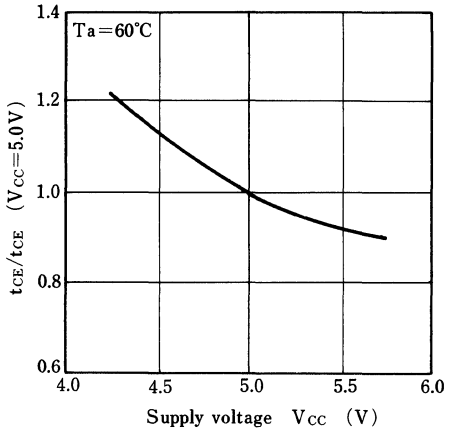
$\overline{CE_1}$	CE_2	$\overline{OE}$	$CS_2/\overline{CS_0}\sim CS_3/\overline{CS_3}$	Mode	$D_0\sim D_7$
L	H	0	In selection mode	Read	D_{OUT}
		1			High impedance
		×	In non-selection mode	Non-selection	
L	L	×		Standby	
H	L	×			
H	H	×			

■ Byte/Digit Output Select

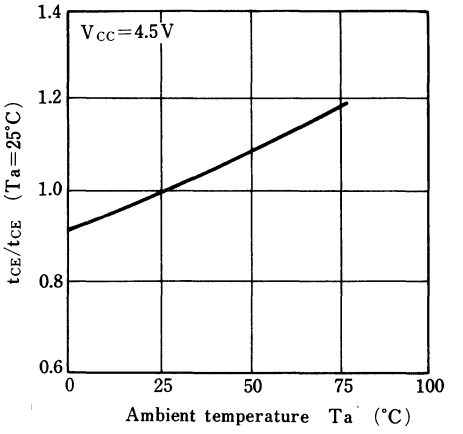
L/U	B/D	Data output pins							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
H	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
H	H	D_7	D_6	D_5	D_4	D_7	D_6	D_5	D_4

■ Electrical Characteristics Curves (Ta=25℃ unless otherwise specified)

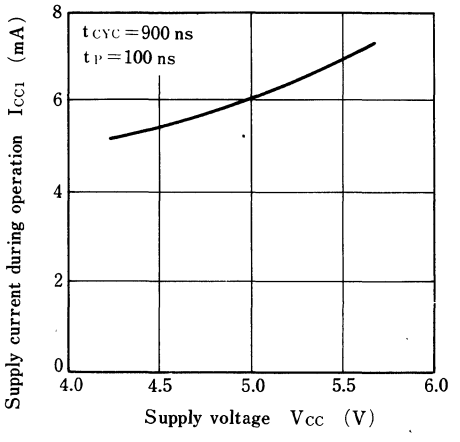
Normalized chip-enable delay time vs. supply voltage



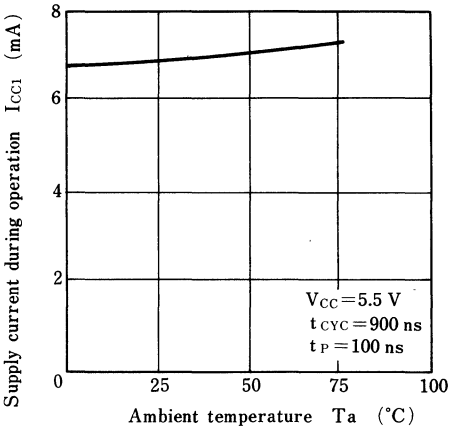
Normalized chip-enable delay time vs. ambient temperature



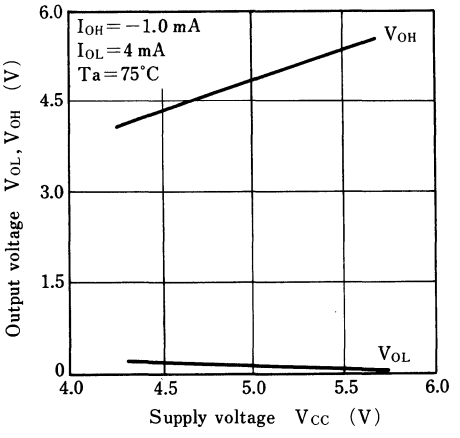
Supply current during operation vs. supply voltage



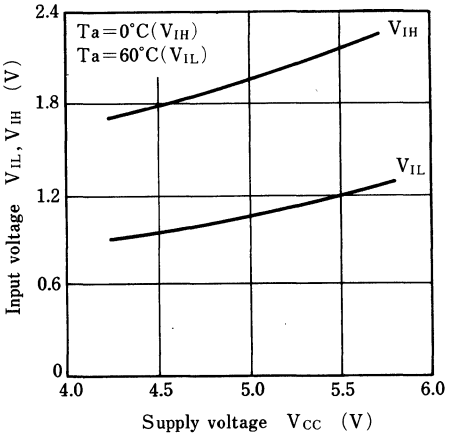
Supply current during operation vs. ambient temperature



Output voltage vs. supply voltage



Input voltage vs. supply voltage

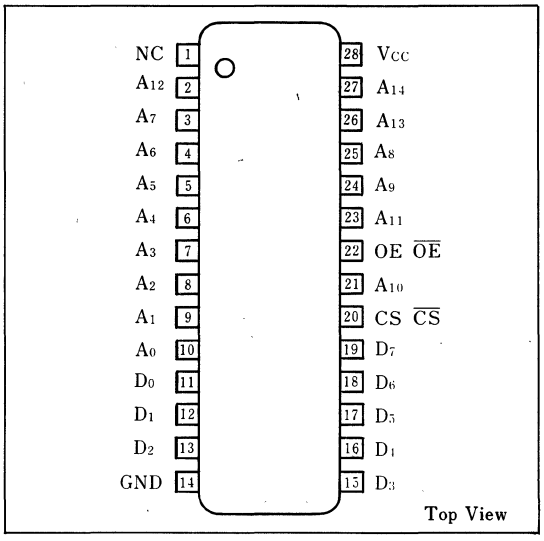


LH53257 CMOS 262144-Bit Mask Programmable Read Only Memory

Description

The LH53257 is a fully static mask programmable ROM organized as 32,768-word-by-8-bit by using polycrystal silicon-gate CMOS process technology.

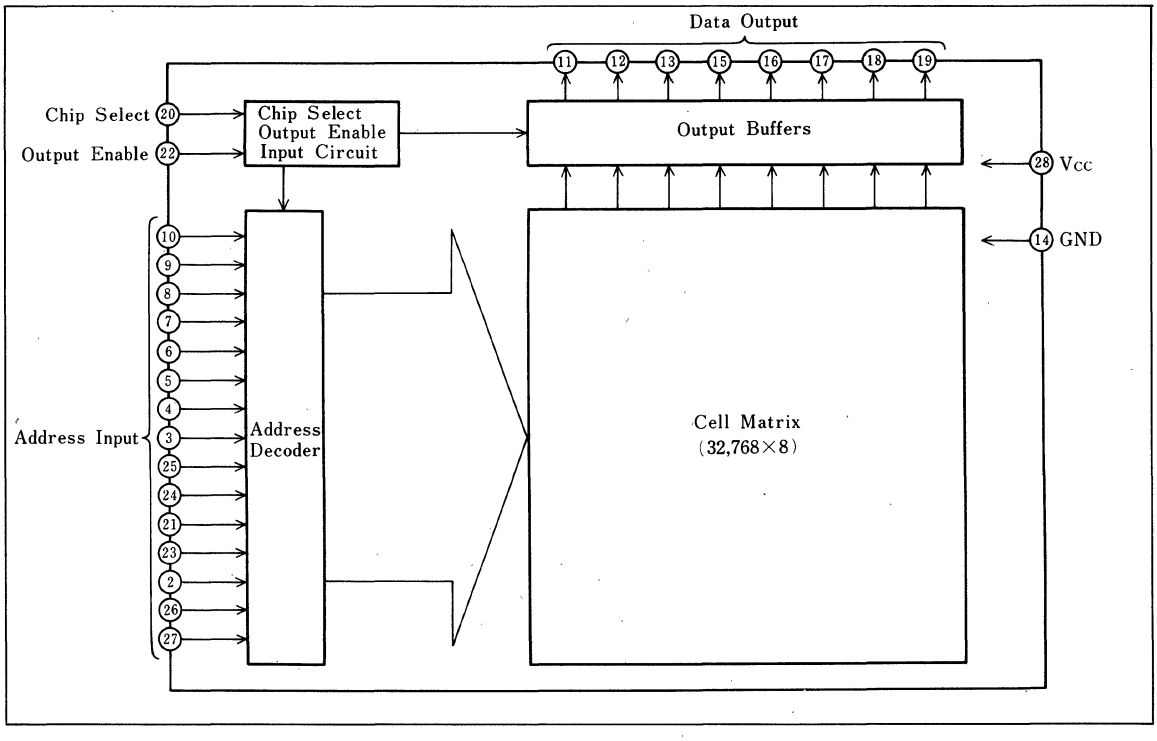
Pin Connections



Features

1. 32,768-word-by-8-bit organization
2. Single +5V power supply
3. Low power consumption
4. Fully static operation (No clock required)
5. All input and output TTL compatible
6. Three-state outputs
7. Access time (MAX.) : 250ns
8. Programmable chip select
9. Programmable output enable
10. 28-pin dual-in-line package

Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

*The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5	5.5	V
Input voltage	V_{IL}	−0.3		0.8	V
	V_{IH}	2.2		V_{CC}	V

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage		V_{IL}		−0.3		0.8	V
Input high voltage		V_{IH}		2.2		V_{CC}	V
Output low voltage		V_{OL}	I_{OL}=1.6mA			0.4	V
Output high voltage		V_{OH}	I_{OH}=−200 μA	2.4			V
Input leakage current		$\|I_{LI}\|$	V_{IN}=0～5.5V			10	μA
Output leakage current		$\|I_{LO}\|$	$\overline{CS}$=0.8V, $\overline{CS}$=2.2V, V_{OUT}=0～5.5V			10	μA
Current consumption	During operation	I_{CC}	I_{OUT}=0mA			30	mA
	During standby	I_{SB}	$\overline{CS}$≦0.2V, $\overline{CS}$≧V_{CC}−0.2V			30	μA

■ AC Characteristics (V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Read cycle time	t_{RC}	250			ns
Access time	t_{ACC}			250	ns
Chip enable time	t_{CE}			250	ns
Output enable time	t_{OE}			100	ns
Chip select time	t_{CS}	10			ns
Output select time	t_{OS}	10			ns
Output turn-off time (from $\overline{CS}$)	t_{DF1}			100	ns
Output turn-off time (from $\overline{OE}$)	t_{DF2}			100	ns
Output hold time	t_{OH}	10			ns

Conditions for measurement of AC characteristics

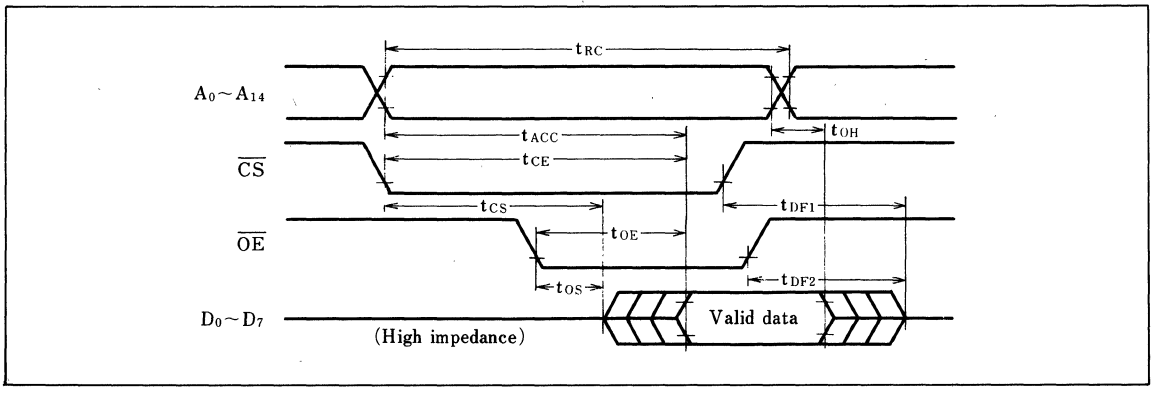
- Input voltage frequency width ····· 0.8～2.2V
- Input rise/fall time ····· 20ms
- Input decision level ····· 1.5V
- Output decision level ····· 0.8V and 2.2V
- Output load ····· 1TTL+100pF

■ Pin Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			10	pF
Output capacitance	C_{IN}	V_{OUT}=0V			10	pF

■ Timing Diagram

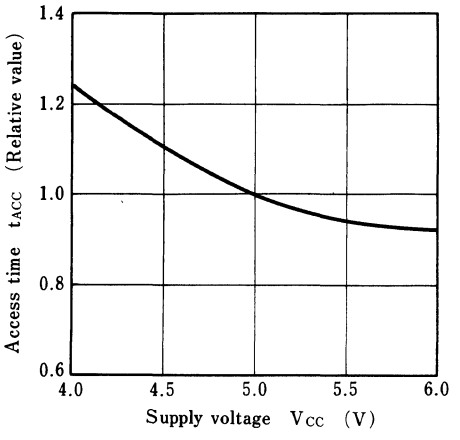


■ Chip Select

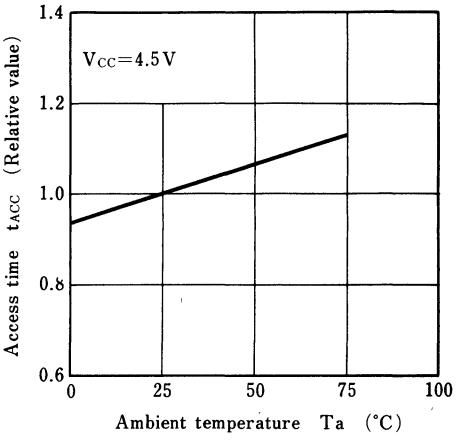
CS/$\overline{CS}$	OE/$\overline{OE}$	Output	Power consumption
L/H	X	High impedance	During standby
H/L	L/H		During operation
	H/L	Output	

■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

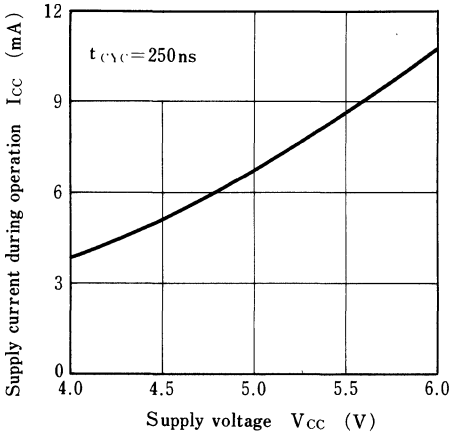
Access time vs. supply voltage



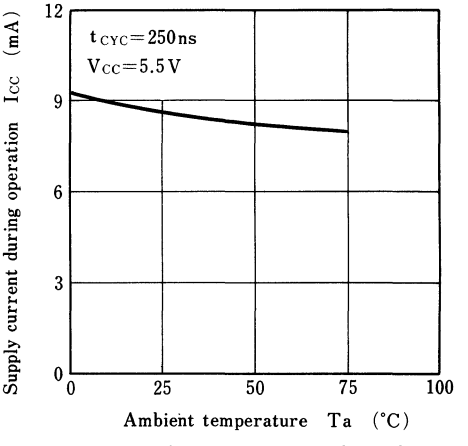
Access time vs. ambient temperature



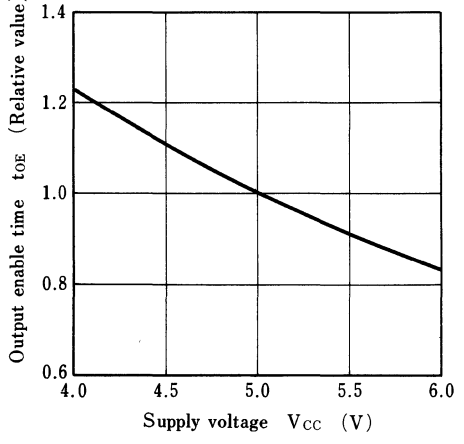
Supply current during operation vs. supply voltage



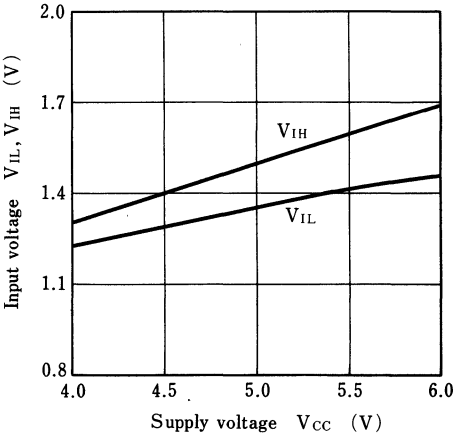
Supply current during operation vs. ambient temperature



Output enable time vs. supply voltage



Input voltage vs. supply voltage



LH53512 CMOS 524288-Bit Mask Programmable Read Only Memory

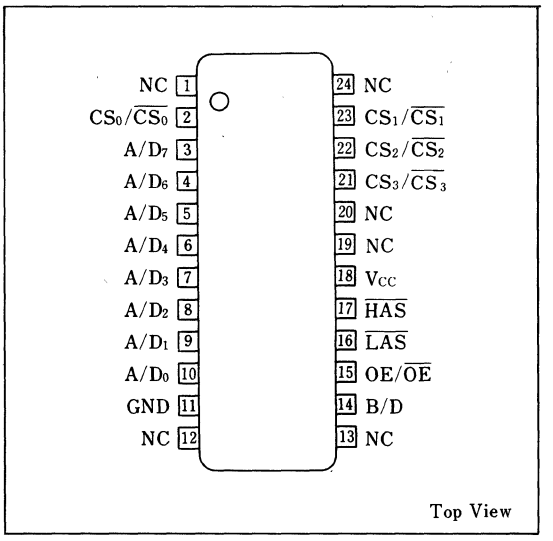
Description

The LH53512 is a mask programmable ROM organized as 65,536-word-by-8-bit by using silicon-gate CMOS process technology.

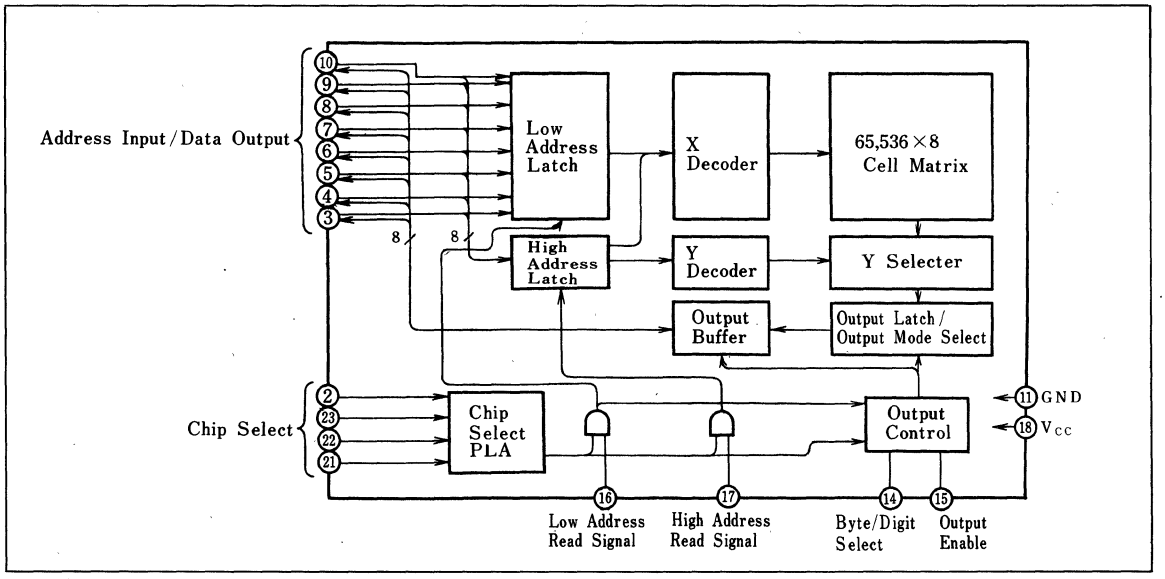
Features

1. 65,536-word-by-8-bit organization
2. Single +5V power supply
3. Low power consumption
4. Edge enabled operation
5. Three-state outputs
6. Access time (MAX.) : 3.0 μs
7. Programmable chip select
8. 24-pin small-outline package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～+7.0	V
Output voltage*	V_{OUT}	−0.3～+7.0	V
Operating temperature	T_{opr}	−5～+55	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

(Ta=25℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.0	5.0	6.0	V
Input voltage	V_{IL}	−0.3		0.8	V
	V_{IH}	V_{CC}−1.0		V_{CC}	V

■ DC Characteristics

(V_{CC}=5.0V±20%, Ta=−5～+55℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{IL}		−0.3		0.8	V	
Input high voltage	V_{IH}		V_{CC}−1.0		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=0.5mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=−0.5mA	V_{CC}−0.8			V	
Input leakage current	$\lvert I_{LI} \rvert$				1.0	μA	1
Output leakage current	$\lvert I_{LO} \rvert$				1.0	μA	1
Chip enable power supply current	I_{CC1}				1,500	μA	2
	I_{CC2}				500	μA	3
Chip disabled power supply current	I_{CC3}				3.0	μA	4

Note 1: Input leakage current (except $A/D_{0\sim7}$) : V_{IN}=0V～V_{CC}
I/O leakage current ($A/D_{0\sim7}$) : $V_{IN/OUT}$=0V～V_{CC}
$\overline{CS_1}$=0.2V, CS_1=V_{CC}−0.2V or $\overline{OE}$=0.2V, $\overline{OE}$=V_{CC}−0.2V
Note 2: t_{CYC}=4.4 μs, V_{CC}=5.5V, output open, V_{IN}=+0.4～+5.1V
Note 3: t_{CYC}=15 μs, V_{CC}=5.5V, output open, V_{IN}=+0.4～+5.1V
Note 4: $\overline{CS_1}$=0.2V, CS_1=V_{CC}−0.2V

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■ AC Characteristics (V_{CC}=5.0V±20%, Ta=−5~+55℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Lower address setup time	t_{SLA}	0			ns
Lower address hold time	t_{HLA}	200			ns
Higher address setup time	t_{SHA}	0			ns
Higher address hold time	t_{HHA}	200			ns
CS hold time (non-selection)	t_{HC}	0			ns
CS setup time	t_{SC}	200			ns
B/D setup time	t_{SB}	0			ns
B/D hold time	t_{HB}	200			ns
$\overline{LAS}$ pulse width	t_{WL}	500			ns
$\overline{HAS}$ pulse width	t_{WH}	500			ns
$\overline{HAS}$ access time	t_{HAS}			3,000	ns
OE access time	t_{OE}			1,000	ns
A/D open setup time	t_{FO}	0			ns
OE to data out delay	t_{OD}	0			ns
OE to pulse width	t_{WO}	0			ns
CS/data off delay	t_{CF}	0		200	ns
OE to data off delay	t_{OF}	0		200	ns
OE $\overline{LAS}$ delay	t_{OL}	200			ns
B/D OE setup time	t_{SBO}	200			ns
B/D OE hold time	t_{HBO}	200			ns
Cycle time (8-bit output mode)	t_{CYC1}	4,400			ns
Cycle time (4-bit output mode)	t_{CYC2}	580			ns

Test conditions of AC characteristics

- Input voltage amplitude ····· +0.4V~V_{CC}−0.4V
- Input rising/falling time ····· 20ns
- Input threshold level ····· 1.5V
- Output threshold level ····· 0.4V and V_{CC}−0.8V
- Output load condition ····· 100pF

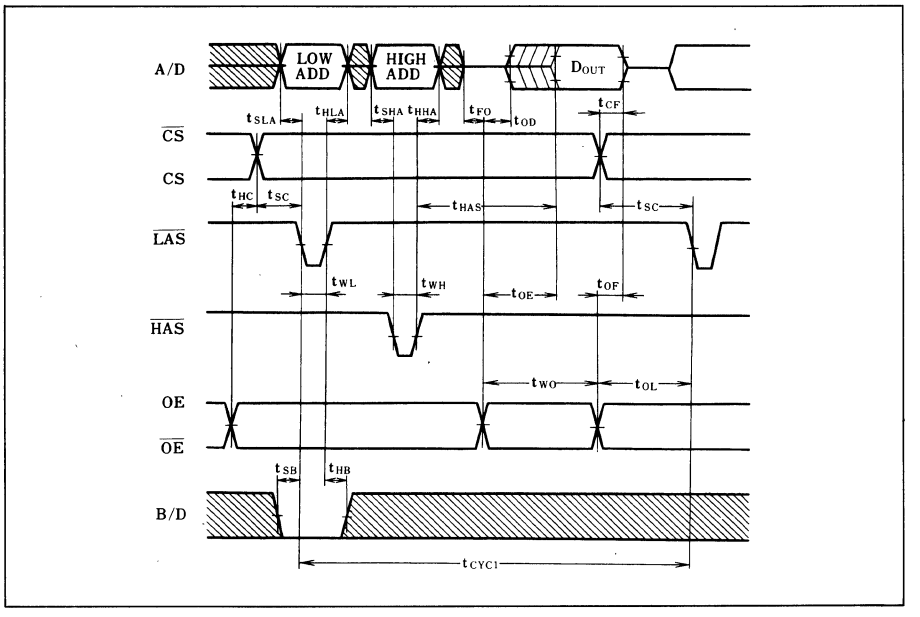
■ Capacitance

(f=1MHz, Ta=25℃)

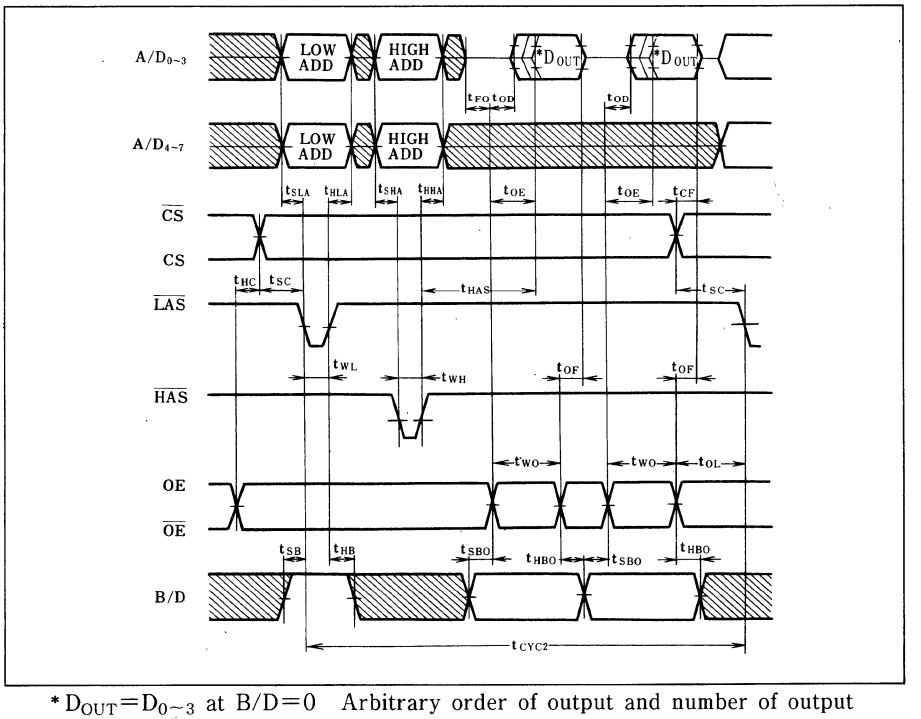
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			10	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			10	pF

■ Timing Diagram

8-bit output mode



4-bit output mode



*$D_{OUT}=D_{0\sim3}$ at B/D=0 Arbitrary order of output and number of output repetition.
$D_{4\sim7}$ at B/D=1

LH531000 CMOS 1048576-Bit Mask Programmable Read Only Memory

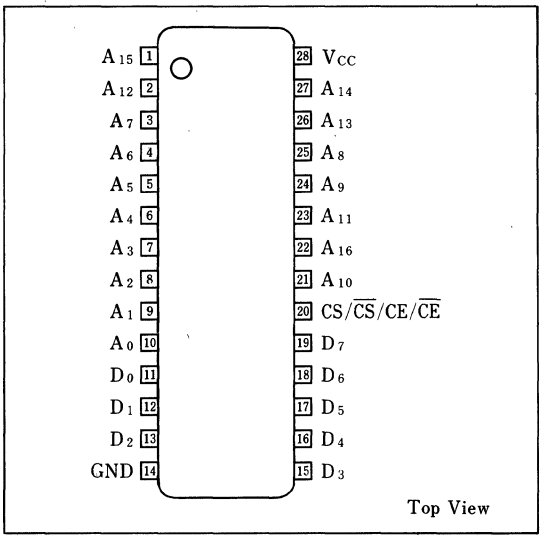
Description

The LH531000 is a mask programmable ROM organized as 131,072-word-by-8-bit by using silicon-gate CMOS process technology.

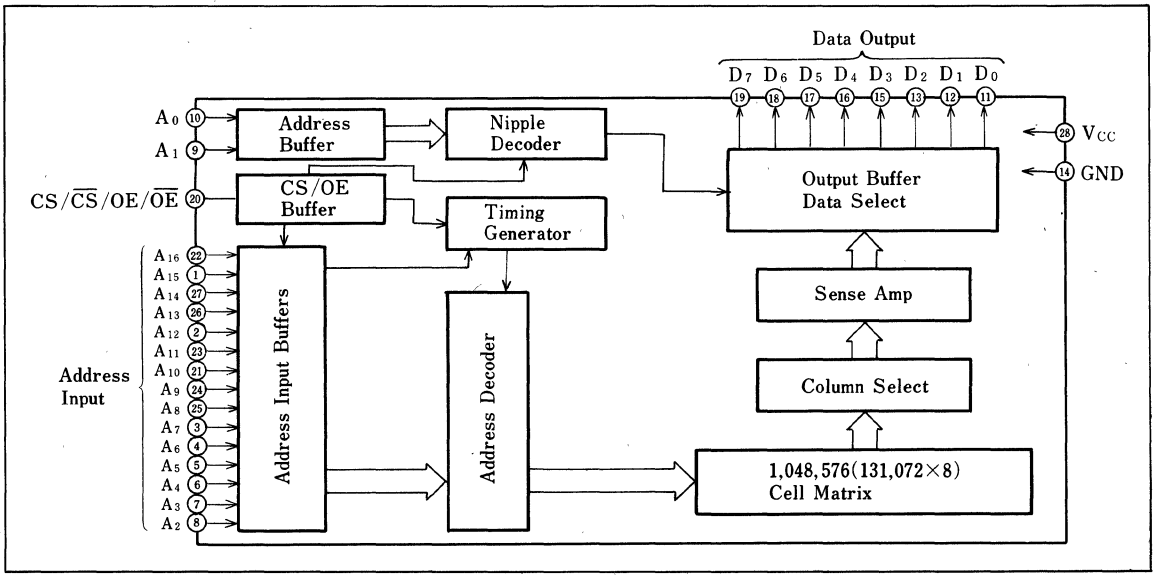
Features

1. 131,072-word-by-8-bit organization
2. Single+5V power supply
3. Low power consumption
4. Fully static operation
5. Automatic power down mode
6. All input and output TTL compatible
7. Three-state outputs
8. Access time (MAX.) : 250ns (normal mode)
   80ns (nibble mode)
9. Programmable chip select
   CS type 20pin = CS/$\overline{CS}$
   OE type 20pin = OE/$\overline{OE}$
10. 28-pin dual-in-line package

Pin Connections



Block Diagram



NEW

LH53012 Series

CMOS 1244160-Bit Mask Programmable Read Only Memory for "kanji" Characters Generation

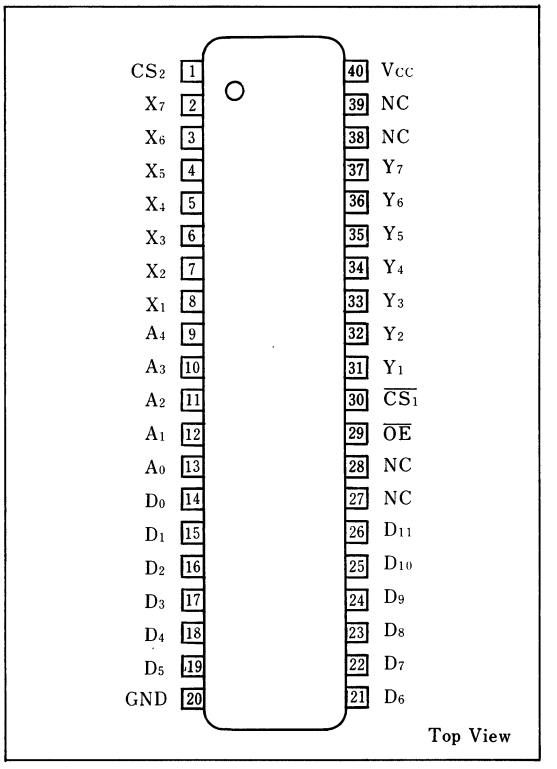
■ Description

LH530101 ~ 4 are mask ROMs for "kanji" characters generation which memorize a total of 6834 characters of non-"kanji" and "kanji". It is able to input the first and second bytes of JIS "kanji" code and a character is composed of 24 × 24 dots prescribed in JIS C 6226-1983

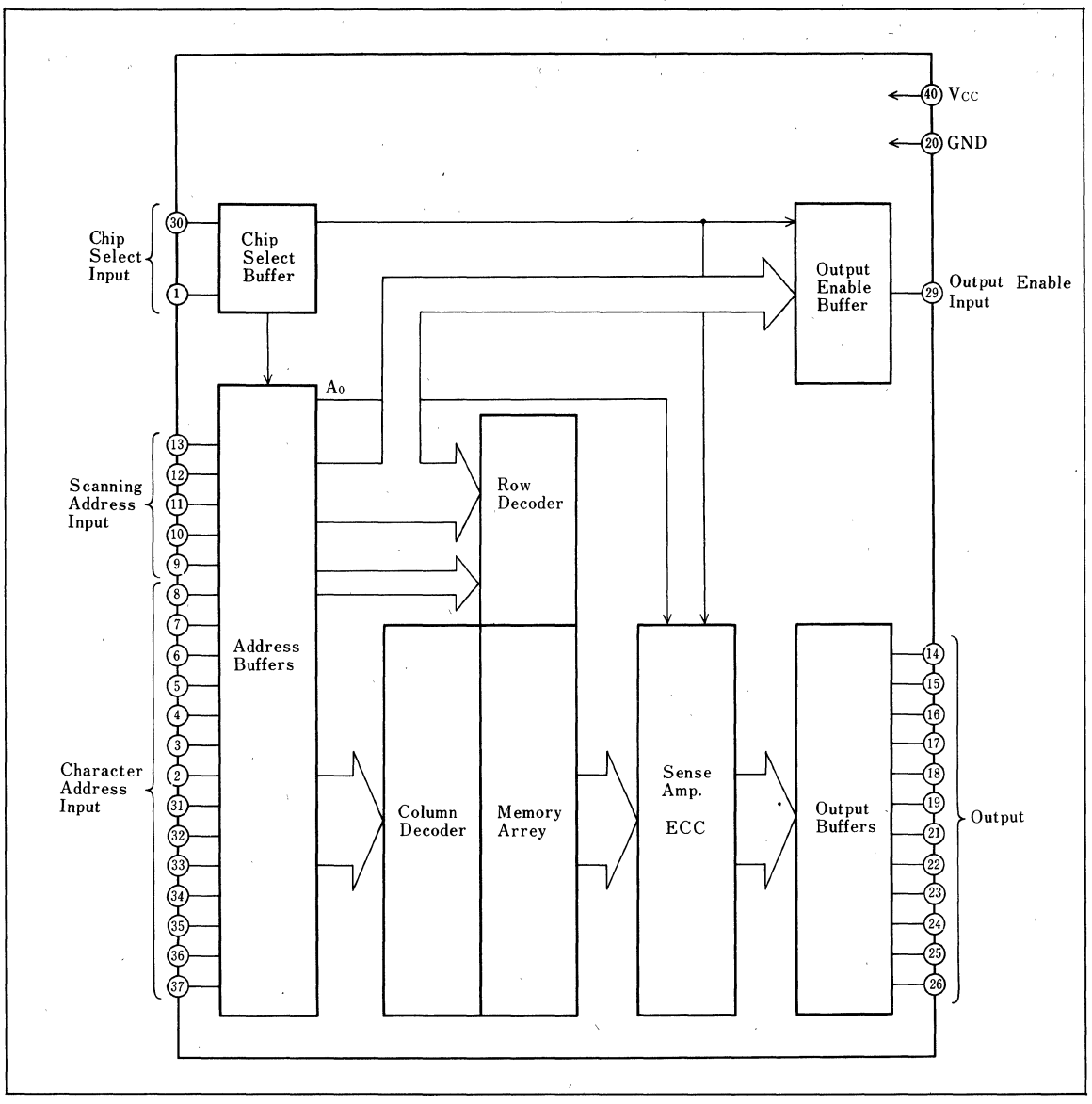
■ Features

1. 4 chips in a set
   Non-"kanji"(524 characters) + First standard "kanji"(2965 characters) : LH530101 + LH530102 Second standard "kanji"(3388 characters) : LH530103 + LH530104
2. Row scanning method
3. 103,680-word-by-12-bit organization
4. Single + 5V power supply
5. Low power consumption
6. Fully static operation (no clock required)
7. Three-state outputs
8. Access time (MAX.) : 250ns
9. Involved the error correcting circuit
10. 40-pin dual-in-line packge

■ Pin Connections



■ Block Diagram



Mask ROM Ordering Procedure

The ordering procedure for mask ROMs is described below along the mask ROM development flow chart.

ROM data from the user should be submitted in the form of an EPROM or on paper tape. At the same time, the following information should be provided.

(1) Type of media on which ROM data is provided
(2) Specified items (chip select, markings)
(3) Corporate name, person in charge, signature
(4) Date of order

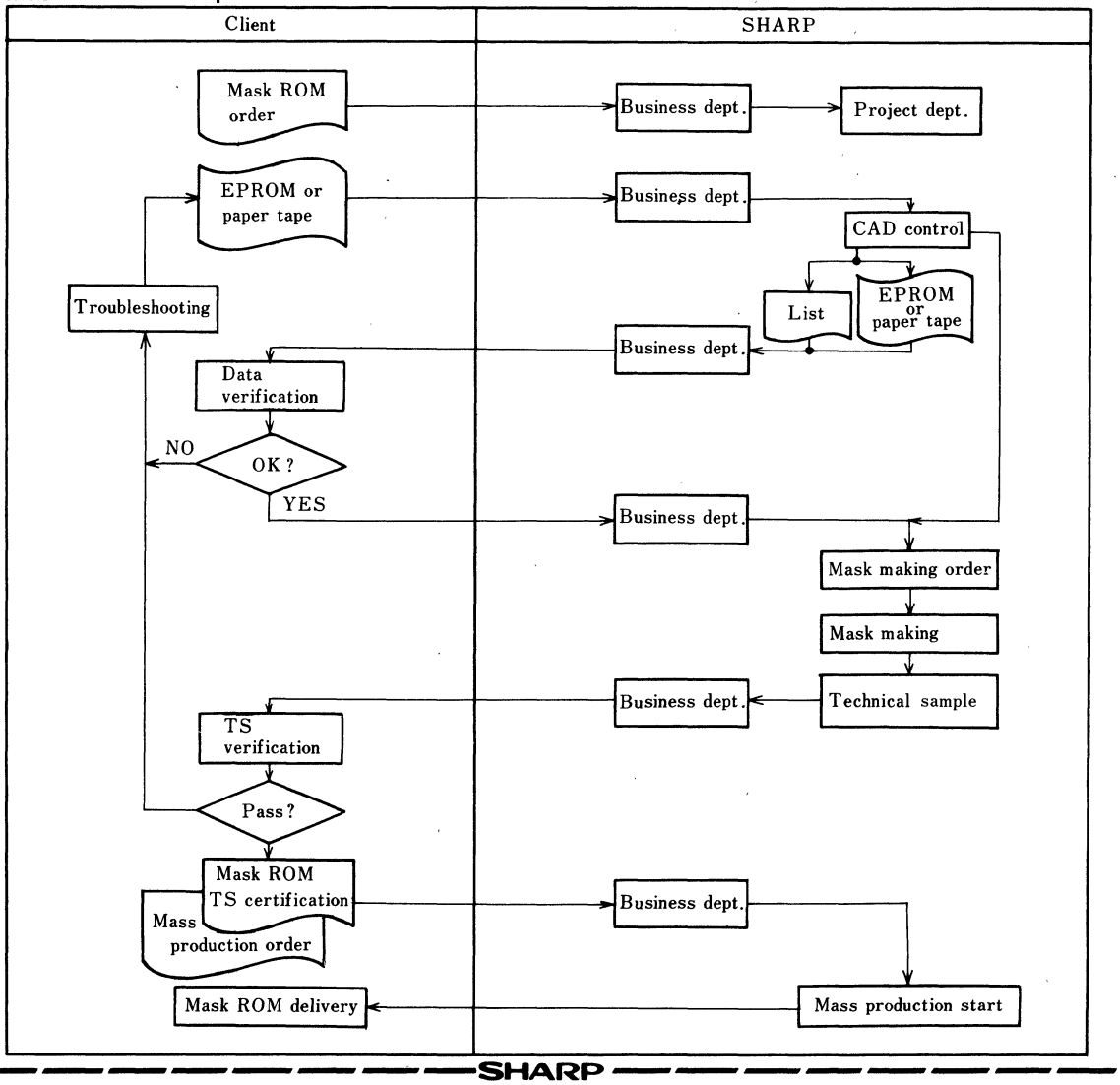
When submitting the ROM, two sets of ROM data media and ROM print-outs must be submitted to make sure that correct data can be read from the ROM.

After the ROM data is received, we use a CAD system to create a magnetic tape to prepare the ROM mask, and create a new EPROM or paper tape and their print-outs for comparison to make sure that the CAD-processed ROM data is correct.

After the user verifies that there are no problems with the results, we start preparing the mask and the TS (technical sample) and submit these to the user for evaluation.

If there are no problems with the TS, the user submits the "Mask ROM TS Certification" to us. We can begin mass production immediately or shortly thereafter according to instructions given by the user.

Mask ROM Development Flow Chart

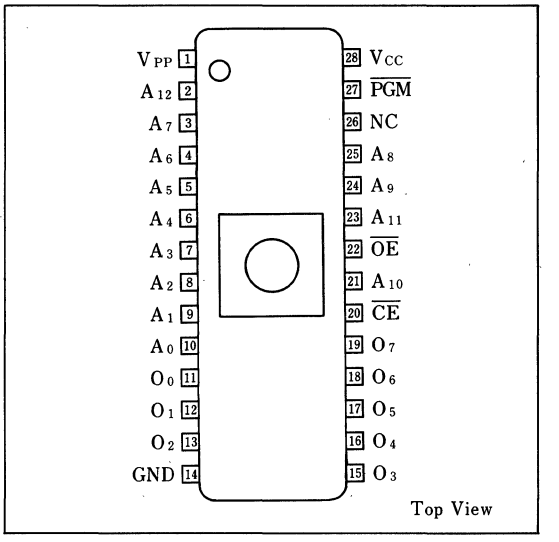


LH5764J CMOS 65536-Bit Electrically Programmable ROM

Description

The LH5764J is a CMOS UV ERASABLE and electrically programmable read only memory organized as 8,192-word-by-8-bit. It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption and fast access time are important.

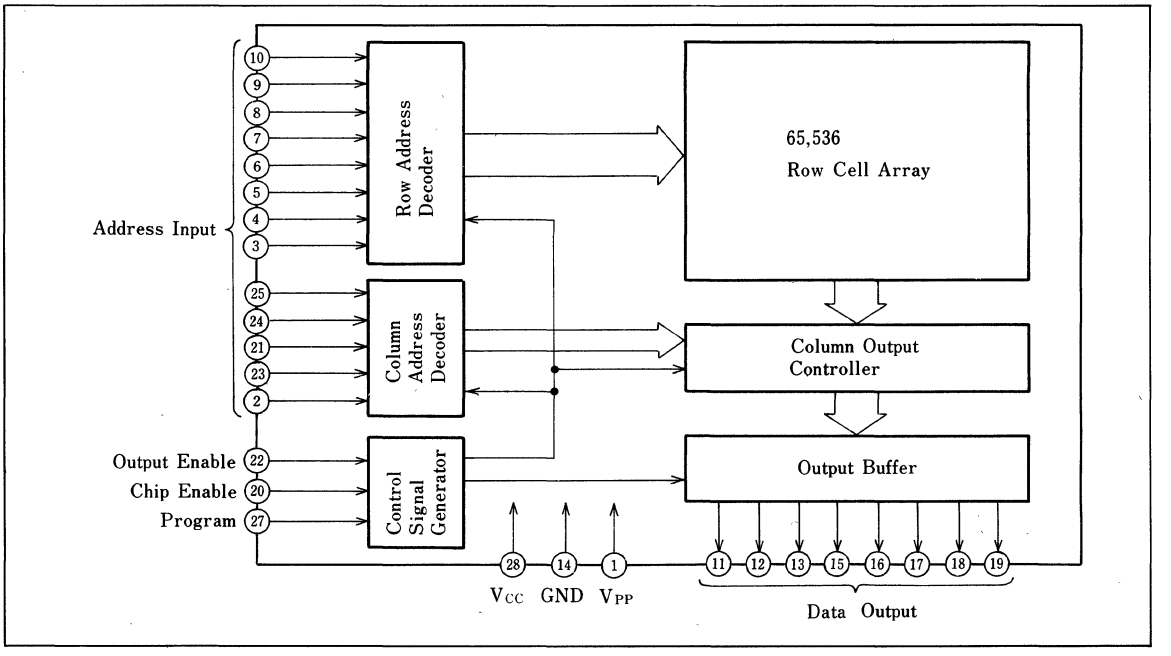
Pin Connections



Features

1. 8,192-word-by-8-bit organization
2. Access Time (MAX.)
   LH5764J-20 : 200ns
   LH5764J-25 : 250ns
   LH5764J-30 : 300ns
   LH5764J-45 : 450ns
3. Single +5V power supply
4. Programming power supply : +12.5V ± 40%
   Programming pulse width : 1ms/byte
5. Power consumption (MAX.) : 150mW (operation)
   0.55mW (standby)
6. Fully static operation
7. Input and output TTL compatible
8. Pin compatible with i2764
9. 28-pin dual-in-line package (Ceramic)

Block Diagram

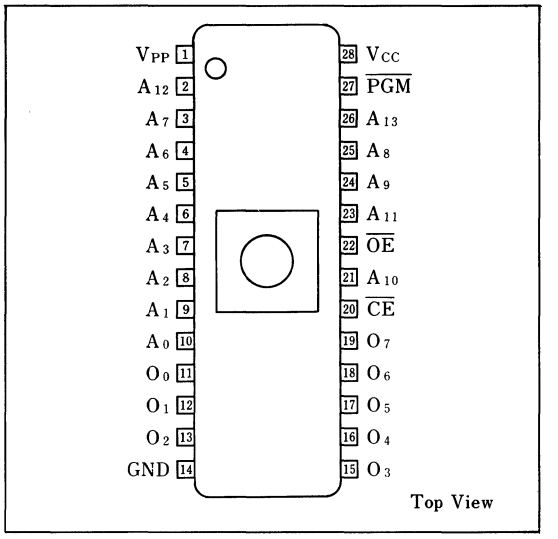


LH57128J CMOS 131072-Bit Electrically Programmable ROM

Description

The LH57128J is a CMOS UV ERASABLE and electrically programmable read only memory organized as 16,384-word-by-8-bit. It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption and fast access time are important.

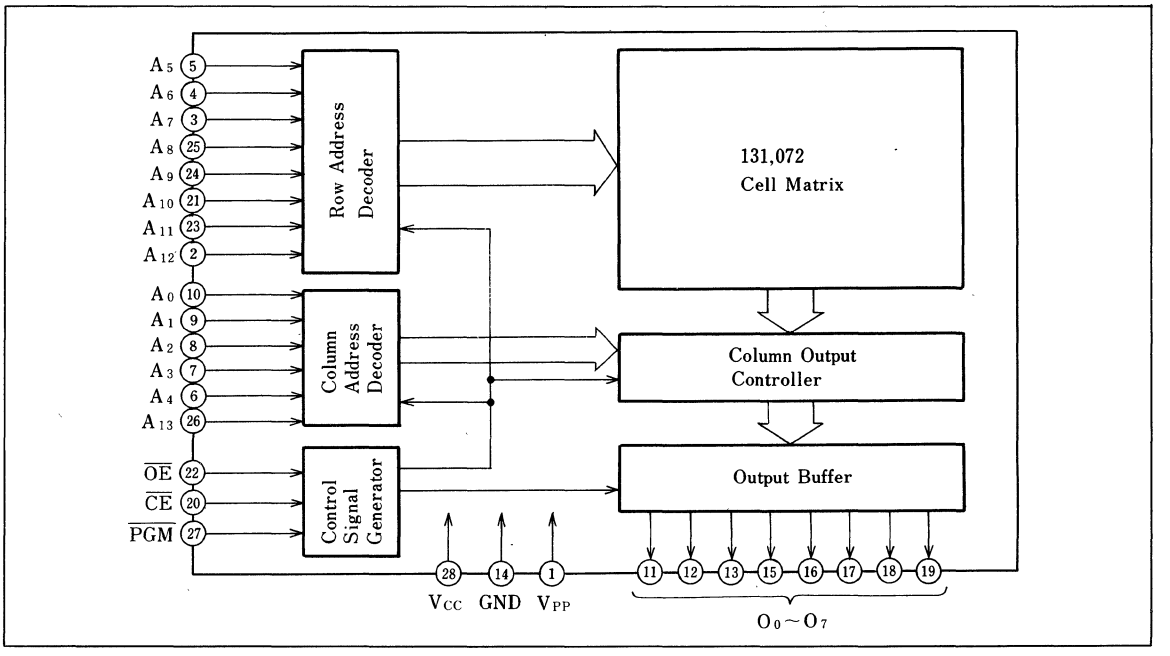
Pin Connections



Features

1. 16,384-word-by-8-bit organization
2. Access Time (MAX.)
   LH57128J-20 : 200ns
   LH57128J-25 : 250ns
   LH57128J-30 : 300ns
   LH57128J-45 : 450ns
3. Single +5V power supply
4. Programming power supply : +12.5V ± 40%
   Programming pulse width : 1ms/byte
5. Power consumption (MAX.) : 150mW (operation)
   0.55mW (standby)
6. Fully static operation
7. Input and output TTL compatible
8. Pin compatible with i27128
9. 28-pin dual-in-line package (Ceramic)

Block Diagram



LH57256J CMOS 262144-Bit Electrically Programmable ROM

NEW

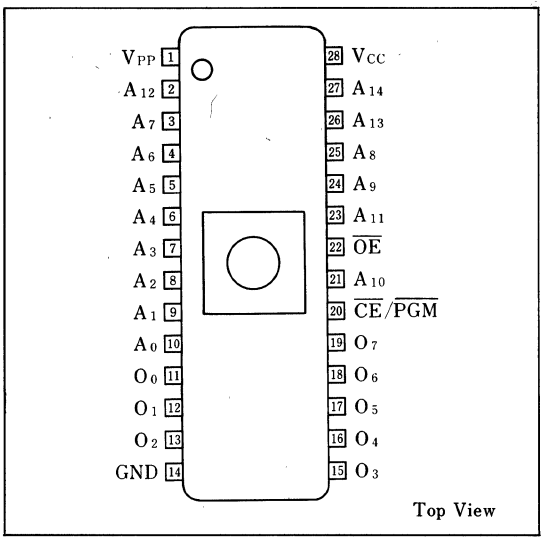
Description

The LH57256J is a CMOS UV ERASABLE and electrically programmable read only memory organized as 32,768-word-by-8-bit. It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption and fast access time are important.

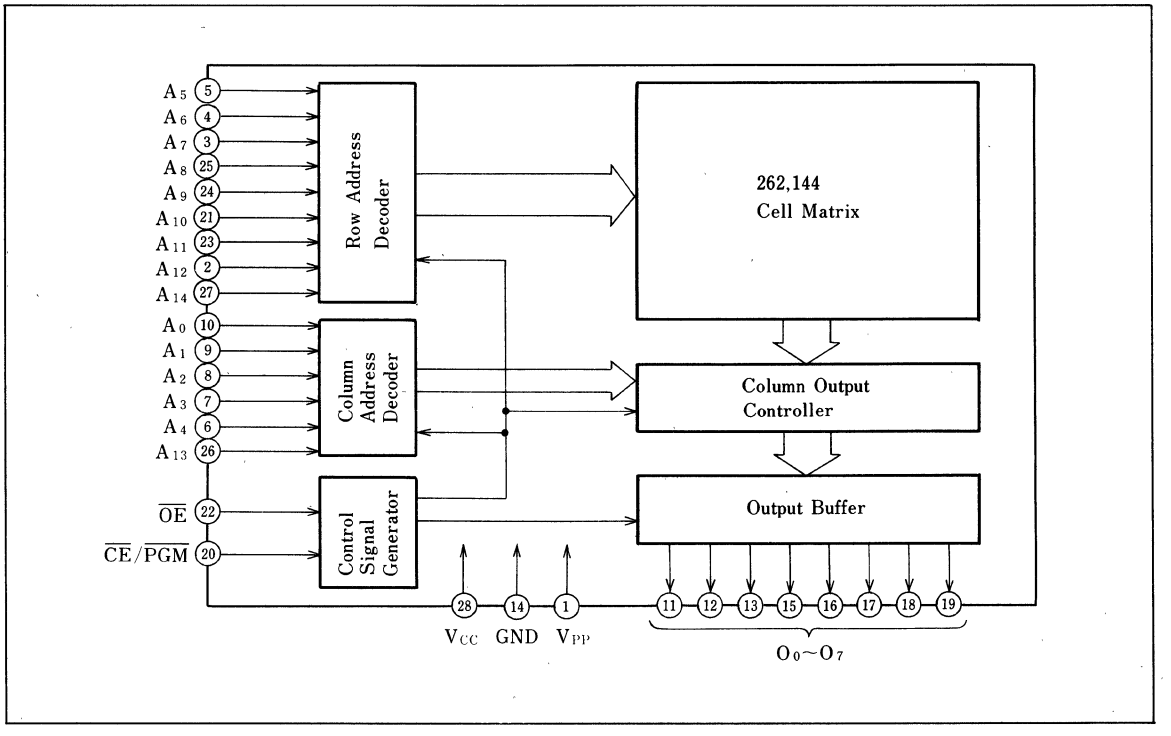
Features

1. 32,768-word-by-8-bit organization
2. Access Time (MAX.)
   - LH57256J-20 : 200ns
   - LH57256J-25 : 250ns
   - LH57256J-30 : 300ns
   - LH57256J-45 : 450ns
3. Single +5V power supply
4. Programming power supply : +12.5V ± 40%
   Programming pulse width : 1ms/byte
5. Power consumption (MAX.) : 150mW (operation)
   0.55mW (standby)
6. Fully static operation
7. Inputs and Outputs TTL compatible
8. Pin compatible with i27256
9. 28-pin dual-in-line package (Ceramic)

Pin Connections



Block Diagram



LH5101-30/LH5101-45

CMOS 1024-Bit Static Random Access Memory

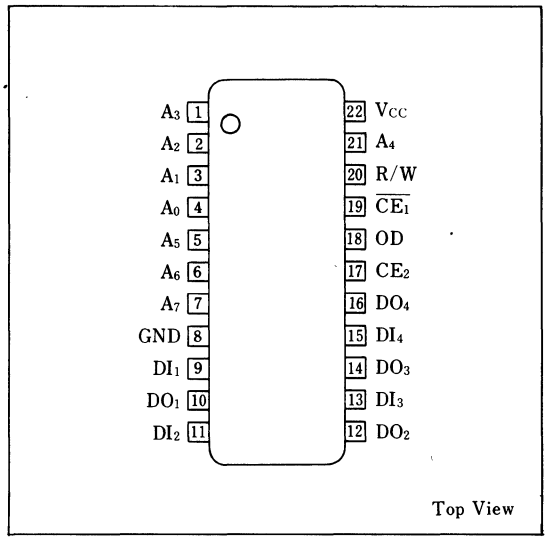
■ Description

The LH5101-30/LH5101-45 are fully static RAMs organized as 256-word-by-4-bit by using silicon-gate CMOS process technology.

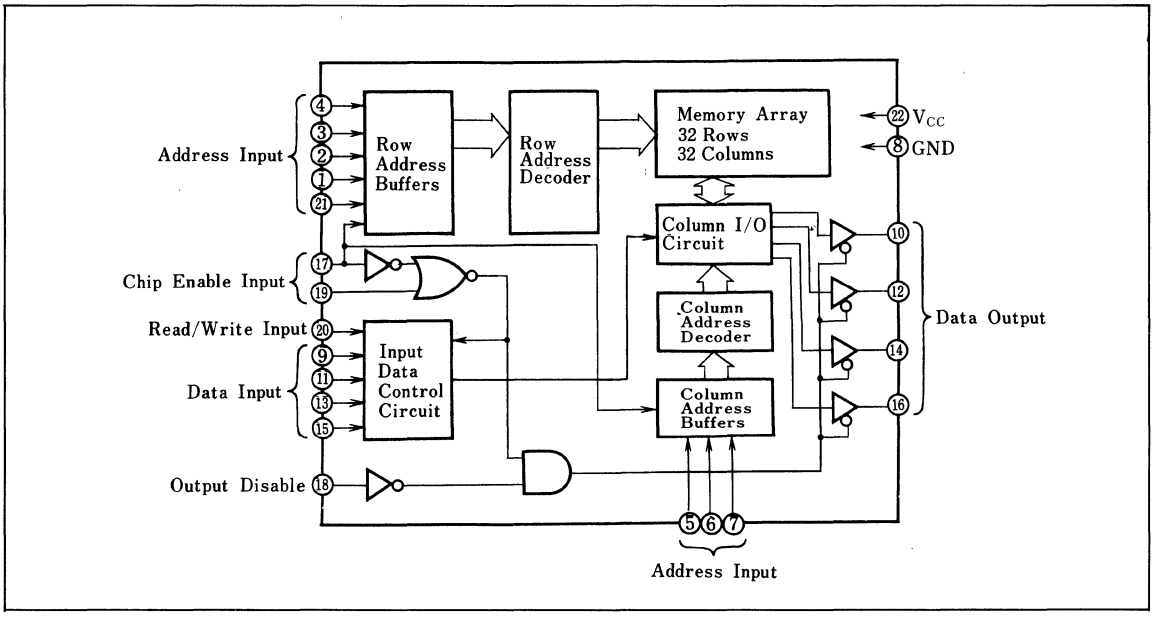
■ Features

1. 256-word-by-4-bit organization
2. Single +5V power supply
3. Fully static operation
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.)
   LH5101-30 : 300ns, LH5101-45 : 450ns
7. Data can be held on +2V supply voltage
8. Low power current consumption at standby mode 10 μA (MAX.)
9. 22-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage*	V_{OUT}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}				0.65	V
Input high voltage	V_{IH}		2.2			V
Output low voltage	V_{OL}	I_{OL}=2.0mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V
Input current	$\|I_{LI}\|$	$0 \leqq V_{IN} \leqq V_{CC}$			1.0	μA
Output leakage current	$\|I_{LO}\|$	$0 \leqq V_{IN} \leqq V_{CC}$, $\overline{CE_1}$=2.2V			1.0	μA
Current consumption 1	I_{CC1}	Output open $V_{IN}=V_{CC}$, $\overline{CE_1} \leqq 0.65V$			20	mA
Current consumption 2	I_{CC2}	Output open V_{IN}=2.2V, $\overline{CE_1} \leqq 0.65V$			25	mA
Chip disabled current consumption	I_{CCL}	$0 \leqq V_{IN} \leqq V_{CC}$, $\overline{CE_2} \leqq 0.2V$			10	μA

■ AC Characteristics

(1) Read cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	LH5101-30			LH5101-45			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{RC}	300			450			ns
Access time	t_{ACC}			300			450	ns
Chip enable time 1	t_{CO1}			250			400	ns
Chip enable time 2	t_{CO2}			350			500	ns
Output enable time	t_{OD}			180			250	ns
Chip turn-off time	t_{DF}	0		100	0		130	ns
Data hold time from address	t_{OH1}	0			0			ns
Data hold time from $\overline{CE_1}$	t_{OH2}	0			0			ns

(2) Write cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	LH5101-30			LH5101-45			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{WC}	300			450			ns
Access time	t_{AW}	60			130			ns
Chip enable time 1	t_{CW1}	250			350			ns
Chip enable time 2	t_{CW2}	250			350			ns
Data setup time	t_{DW}	150			250			ns
Data hold time	t_{DH}	40			50			ns
Pulse width	t_{WP}	180			250			ns
Recovery time	t_{WR}	40			50			ns
Input enable time	t_{DS}	100			130			ns

Test conditions of AC characteristics

- Input voltage amplitude ····· +0.65～+2.2V
- Input rising/falling time ····· 10ns
- Timing reference level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		3.5	6	pF
Output capacitance	C_{OUT}	V_{OUT}=0V		9	12	pF

■ Low-Voltage Data Hold Characteristics

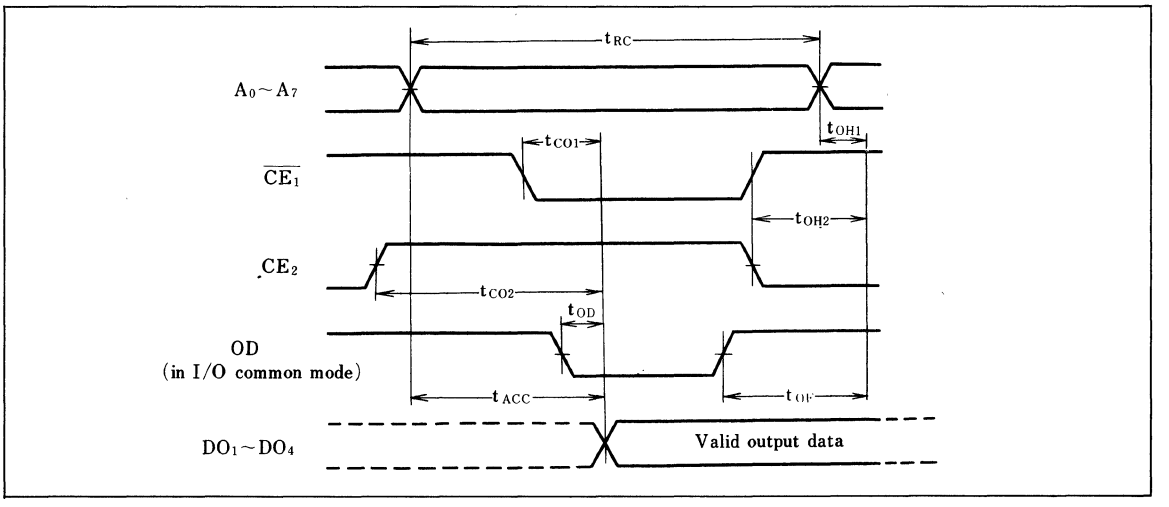
(Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage for data hold	V_{DR}	V_{CE2}≦0.2V	2.0			V	
Supply current for data hold	I_{CCDR}	V_{CE2}≦0.2V, V_{DR}=2.0V			5	μA	
Chip turn-off time	t_{CDR}		0			ns	
Operation recovery time	t_R		t_{RC}			ns	1

Note 1: In data hold mode, all input/output pins are put below V_{DR}. t_{RC} : Read cycle time

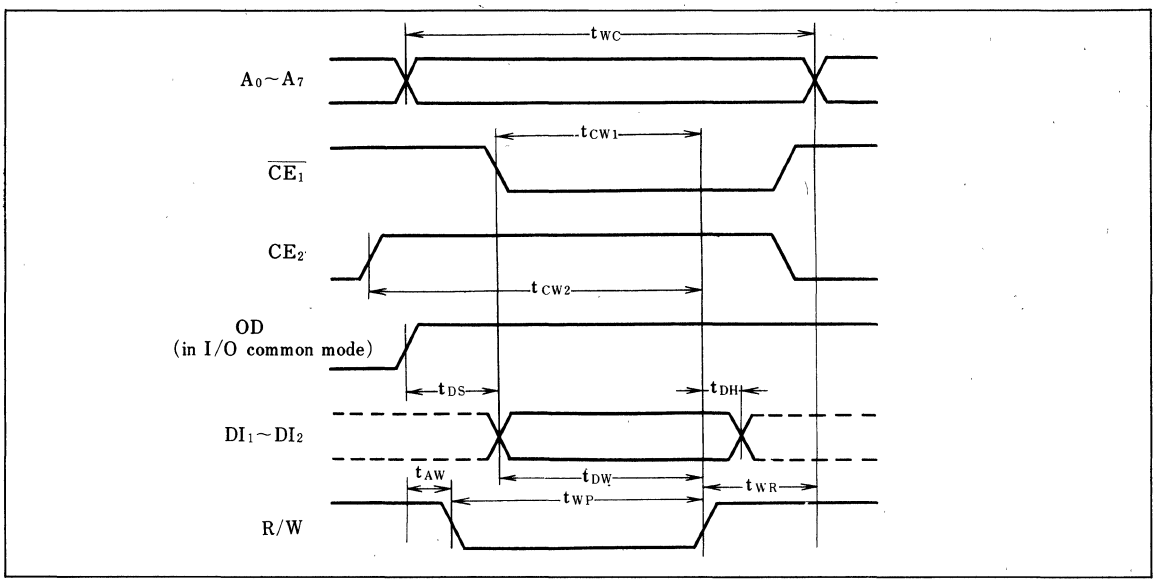
■ Timing Diagram

(1) Read cycle



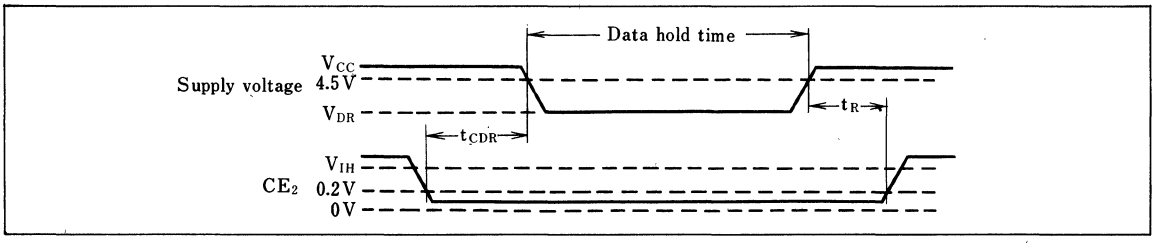
For data input/output separation, OD is made low. In read cycle, R/W is made high.

(2) Write cycle



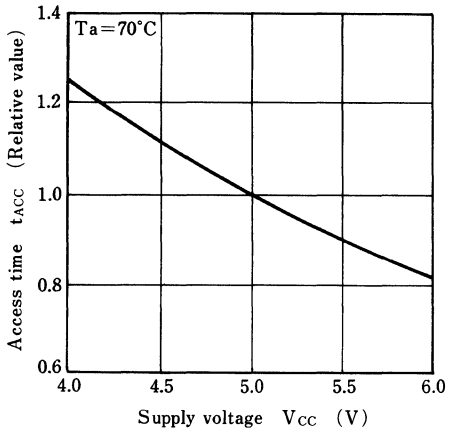
In I/O common mode, OD is made high during the write period. For data input/output separation, OD may be either high or low.

(3) Low-voltage data hold

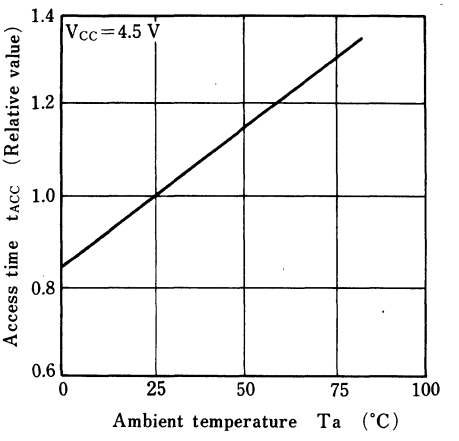


■ Electrical Characteristics Curves (V_{CC}=5V, TA=25℃ unless otherwise specified)

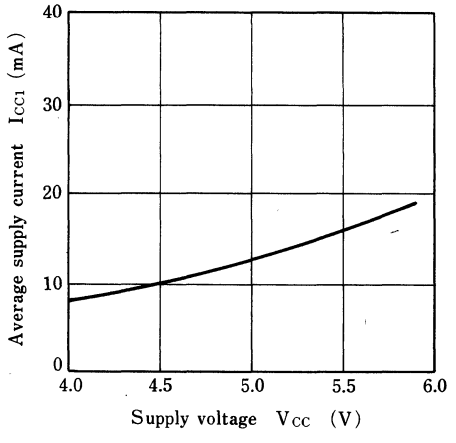
Access time vs. supply voltage



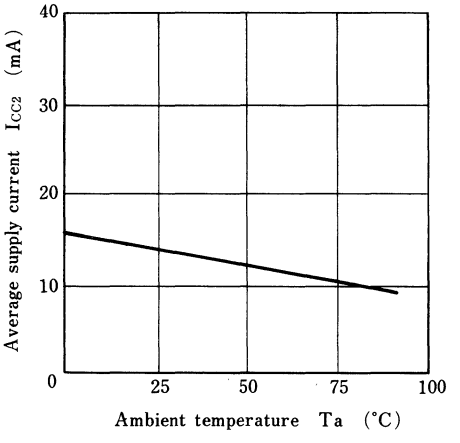
Access time vs. ambient temperature



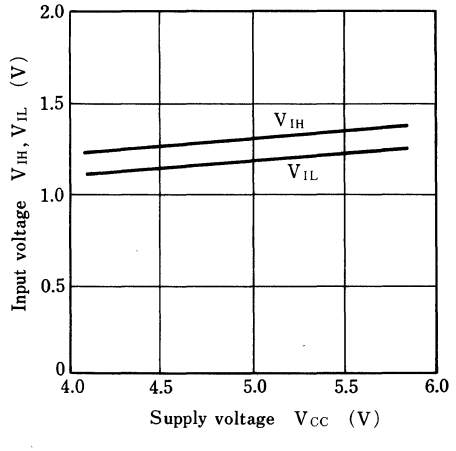
Average supply current vs. supply voltage



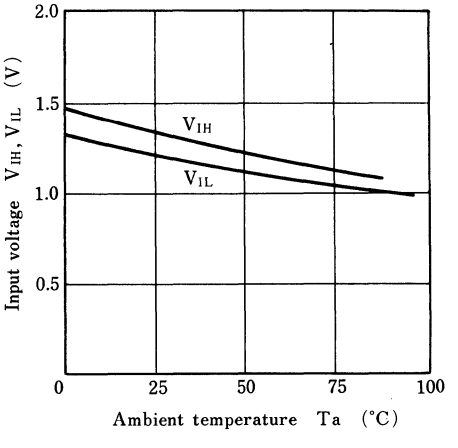
Average supply current vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



8

LH5101/LH5101L3

CMOS 1024-Bit Static Random Access Memory

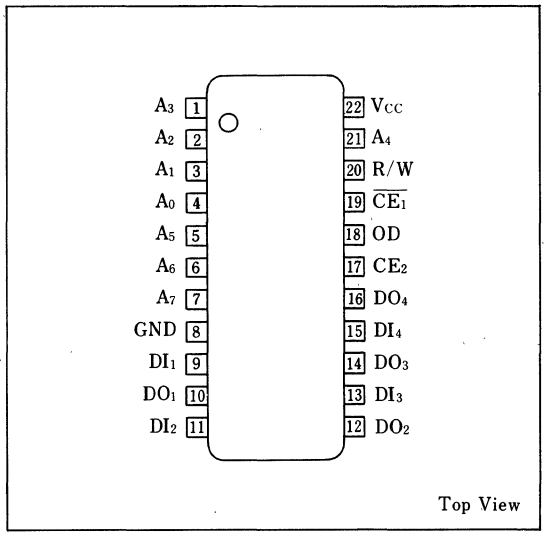
■ Description

The LH5101/LH5101L3 are fully static RAMs organized as 256-word-by-4-bit by using silicon-gate CMOS process technology.

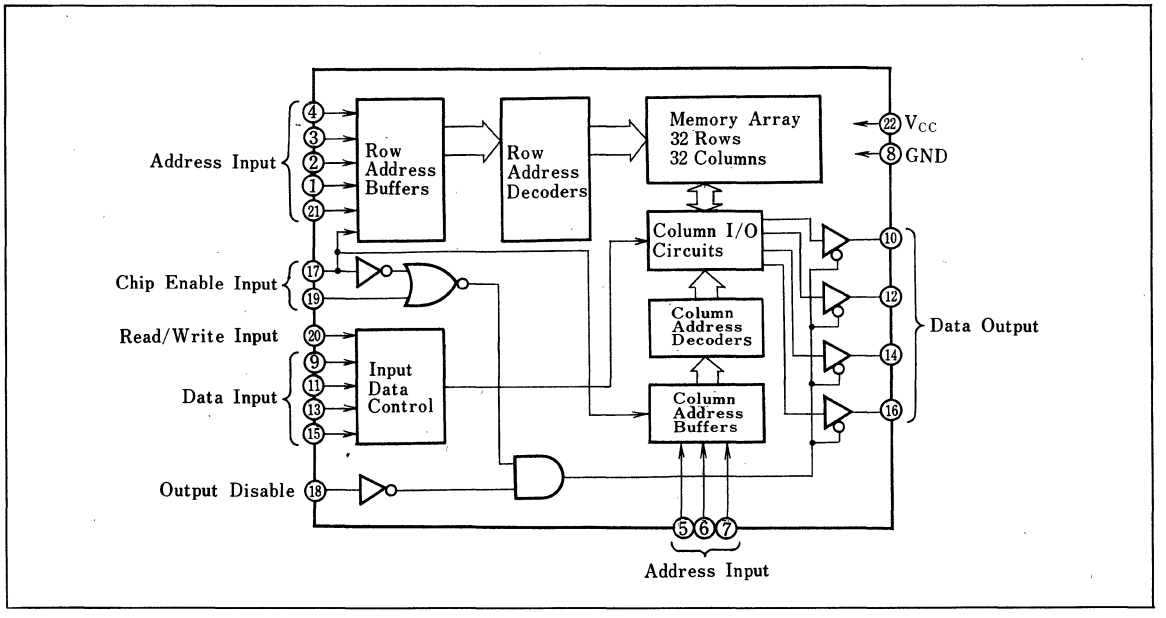
■ Features

1. 256-word-by-4-bit organization
2. Single +5V power supply
3. Fully static operation
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.)
   LH5101 : 800ns, LH5101L3 : 650ns
7. Data can be held on +2V supply voltage
8. Low power supply current at standby mode
9. 22-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage*	V_{OUT}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

*The maximum applicable voltage on any pin with respect to GND.

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}			0.3		0.65	V
Input high voltage	V_{IH}			2.2		V_{CC}	V
Output low voltage	V_{OL}	I_{OL}=2.0mA				0.4	V
Output high voltage	V_{OH}	I_{OH}=−1.0mA		2.4			V
Input current	$\lvert I_{LI} \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$				1.0	μA
Output leakage current	$\lvert I_{LO} \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$, $\overline{CE_1}$=2.2V				1.0	μA
Current consumption 1	I_{CC1}	Output open, $V_{IN}=V_{CC}$ $\overline{CE_1} \leqq 0.65V$			9	22	mA
Current consumption 2	I_{CC2}	Output open, V_{IN}=2.2V $\overline{CE_1} \leqq 0.65V$			13	27	mA
Chip disabled current consumption	I_{CCL}	$CE_2 \leqq 0.2V$	LH5101			100	μA
			LH5101L3			200	

■ AC Characteristics

(1) Read cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	LH5101			LH5101L3			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{RC}	800			650			ns
Access time	t_{ACC}			800			650	ns
Chip enable time 1	t_{CO1}			800			600	ns
Chip enable time 2	t_{CO2}			850			700	ns
Output enable time	t_{OD}			350			350	ns
Chip turn-off time	t_{DF}	0		200	0		150	ns
Data hold time from address	t_{OH1}	0			0			ns
Data hold time from $\overline{CE_1}$	t_{OH2}	0			0			ns

(2) Write cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	LH5101			LH5101L3			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{WC}	800			650			ns
Access time	t_{AW}	200			150			ns
Chip enable time 1	t_{CW1}	600			550			ns
Chip enable time 2	t_{CW2}	600			550			ns
Data setup time	t_{DW}	400			400			ns
Data hold time	t_{DH}	100			100			ns
Pulse width	t_{WP}	400			400			ns
Recovery time	t_{WR}	50			50			ns
Input enable time	t_{DS}	200			150			ns

Test conditions of AC characteristics

- Input voltage amplitude ····· +0.65～+2.2V
- Input rising/falling time ····· 20ns
- Timing reference level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		6	10	pF
Output capacitance	C_{OUT}	V_{OUT}=0V		15	20	pF

■ Low-Voltage Data Hold Characteristics

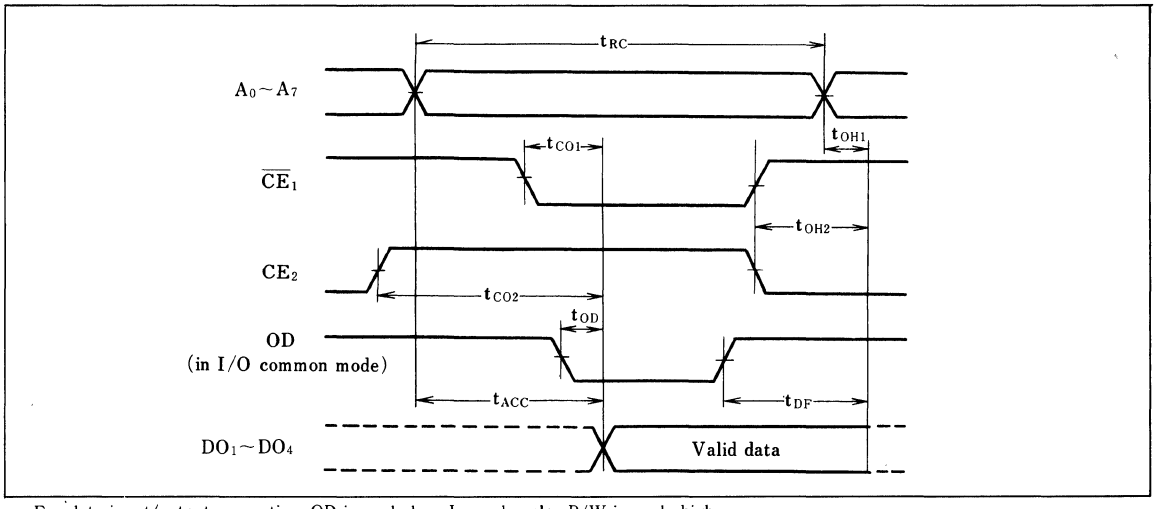
(Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage for data hold	V_{DR}	$V_{CE2} \leqq 0.2V$	2.0			V
Supply current for data hold	I_{CCDR}	$V_{CE2} \leqq 0.2V$, V_{DR}=2.0V			20	μA
Chip turn-off time	t_{CDR}		0			ns
Operation recovery time**	t_R		t_{RC}			ns

** In data hold mode, all input/output pins are put below V_{DR}.
t_{RC} : Read cycle time

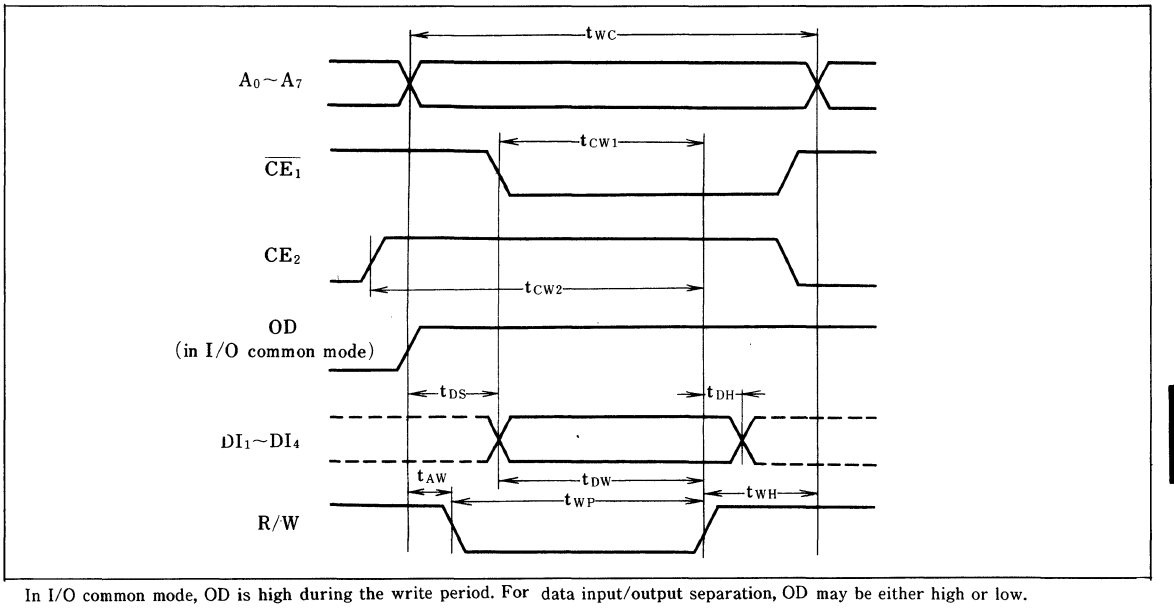
■ Timing Diagram

(1) Read cycle



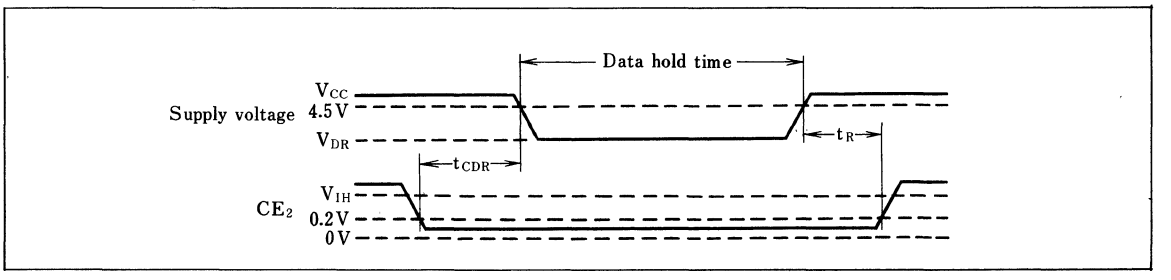
For data input/output separation, OD is made low. In read cycle, R/W is made high.

(2) Write cycle



In I/O common mode, OD is high during the write period. For data input/output separation, OD may be either high or low.

(3) Low-voltage data hold



LH5101S CMOS 1024-Bit Static Random Access Memory

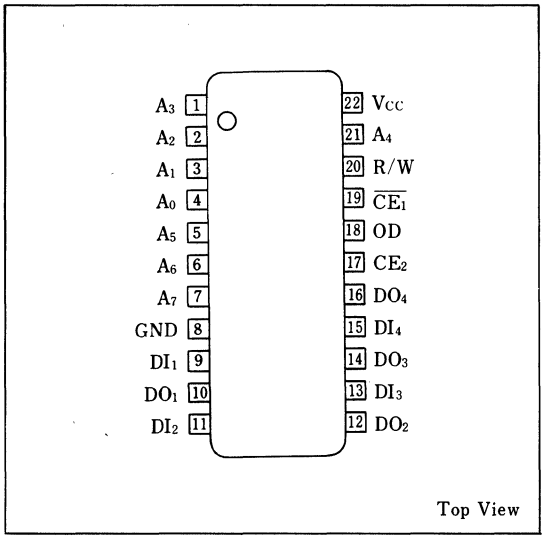
Description

The LH5101S is a fully static RAM organized as 256-word-by-4-bit by using silicon-gate CMOS process technology.

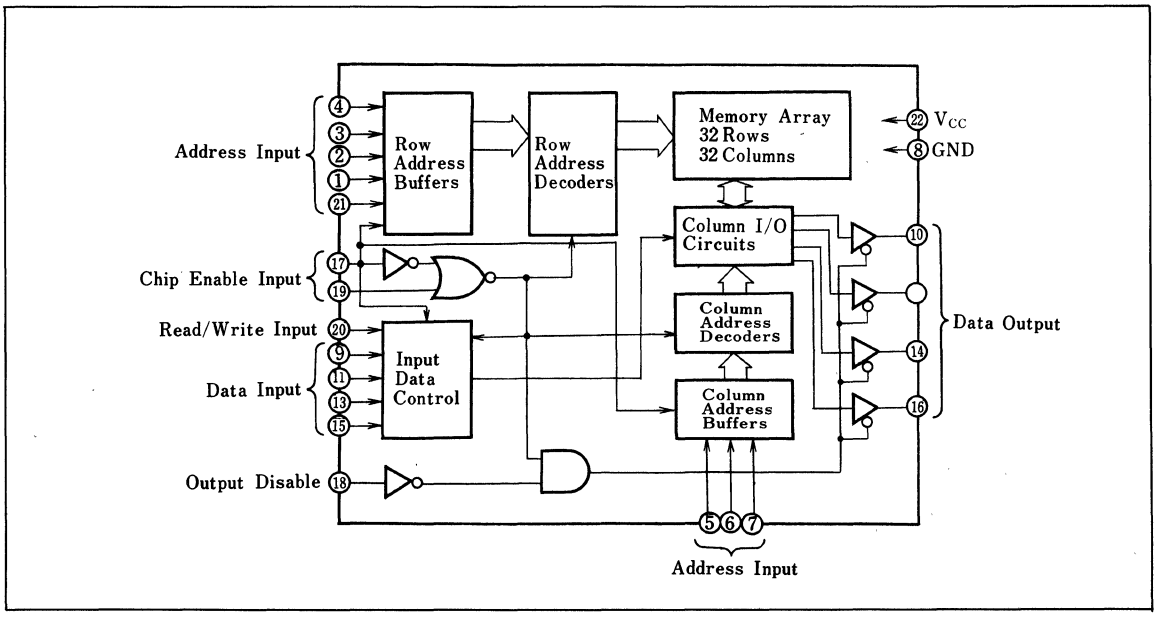
Features

1. 256-word-by-4-bit organization
2. Single +3V power supply
3. Fully static operation
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.) : 3.0 μs
7. Data can be held on +2V supply voltage
8. Low power supply current at standby mode 10 μA (MAX.)
9. 22-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage*	V_{OUT}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	−10～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

*The maximum applicable voltage on any pin with respect to GND.

■ DC Characteristics

(V_{CC}=2.6～3.4V, Ta=−10～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}		−0.3		0.6	V
Input high voltage	V_{IH}		V_{CC}−0.6		V_{CC}	V
Output low voltage	V_{OL}	I_{OL}=500 μA			0.3	V
Output high voltage	V_{OH}	I_{OH}=−30 μA	V_{CC}−0.6			V
Input current	$\lvert I_{LI} \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$			1.0	μA
Output leakage current	$\lvert I_{LO} \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$, $\overline{CE_1}=V_{CC}-0.6$			1.0	μA
Current consumption 1	I_{CC1}	Output open, $V_{IH}=V_{CC}$, $\overline{CE_1} \leqq 0.6V$		5	11	mA
Current consumption 2	I_{CC2}	Output open, $V_{IN}=2.2V$ $\overline{CE_1} \leqq 0.6V$		8	13	mA
Chip disabled current consumption	I_{CCL}	$0 \leqq V_{IN} \leqq V_{CC}$, $CE_2 \leqq 0.2V$			10	μA

■ AC Characteristics

(1) Read cycle

(V_{CC}=2.6～3.4V, Ta=−10～+60℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	3.5			μs
Access time	t_{ACC}			3.0	μs
Chip enable time	t_{CO}			3.0	μs
Address enable time	t_{AEO}			2.9	μs
Output enable time	t_{OD}			1.3	μs
Chip turn-off time	t_{DF}	0		750	ns
Data hold time from address	t_{OH1}	0			ns
Data hold time from CE_1	t_{OH2} t_{OH3}	0			ns
Adress enable delay time	t_{AE1}	0.1			μs
	t_{AE2}	0.5			μs

(2) Write cycle

(V_{CC}=2.6～3.4V, Ta=−10～+60℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{WC}	3.5			μs
Access time	t_{AW}	750			ns
Chip enable time 1	t_{CW1}	2.2			μs
Chip enable time 2	t_{AEW}	2.1			μs
Data setup time	t_{DW}	1.5			μs
Data hold time	t_{DH}	370			ns
Pulse width	t_{WP}	1.5			μs
Recovery time	t_{WR}	180			ns
Input enable time	t_{DS}	750			ns
Address enable delay time	t_{AE3}	0.1			μs
	t_{AE4}	0.5			

Test conditions of AC characteristics

- Input voltage amplitude ····· +0.65～+2.2V
- Input rising/falling time ····· 10ns
- Timing reference level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		6	10	pF
Output capacitance	C_{OUT}	V_{OUT}=0V		15	20	pF

■ Low-Voltage Data Hold Characteristics

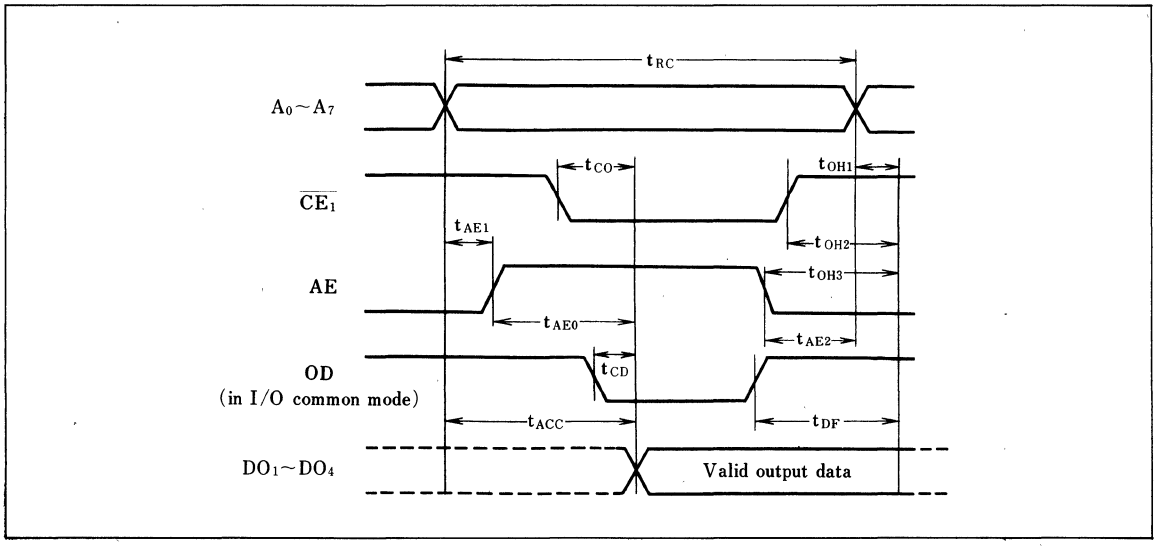
(Ta=−10～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage for data hold	V_{DR}	V_{CE2}≦0.2V	2.0			V
Supply current for data hold	I_{CCDR}	V_{CE2}≦0.2V, V_{DR}=2.0V			5	μA
Chip turn-off time	t_{CDR}		0			ns
Operation recovery time**	t_R		t_{RC}			ns

**In data hold mode, all input/output pins are put below V_{DR}. t_{RC} : Read cycle time

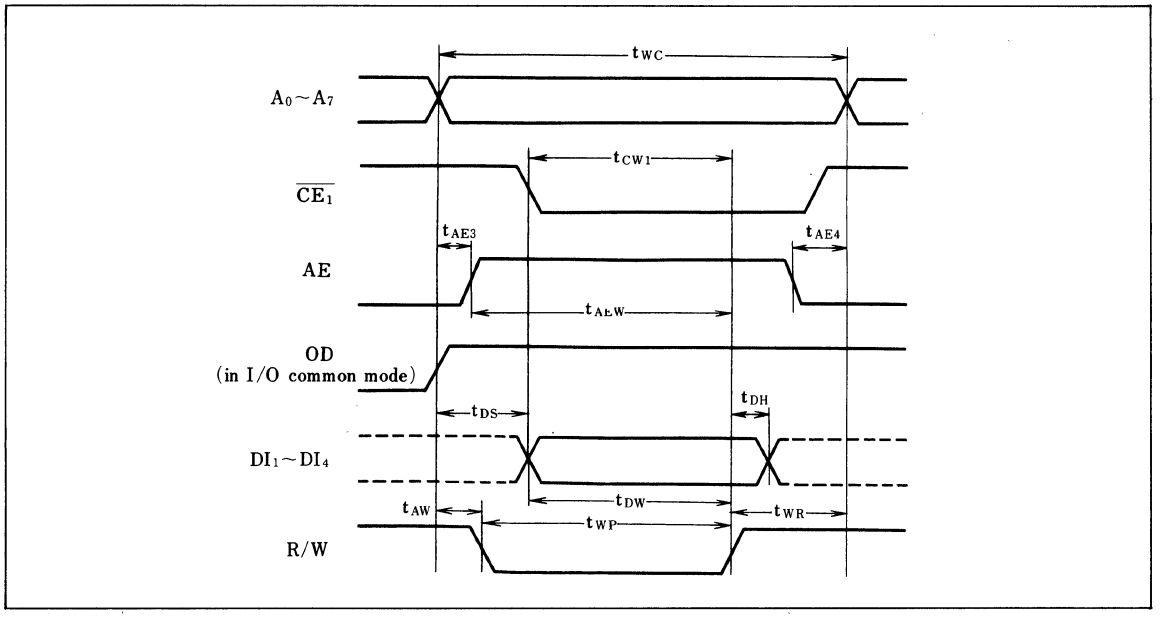
■ Timing Diagram

(1) Read cycle



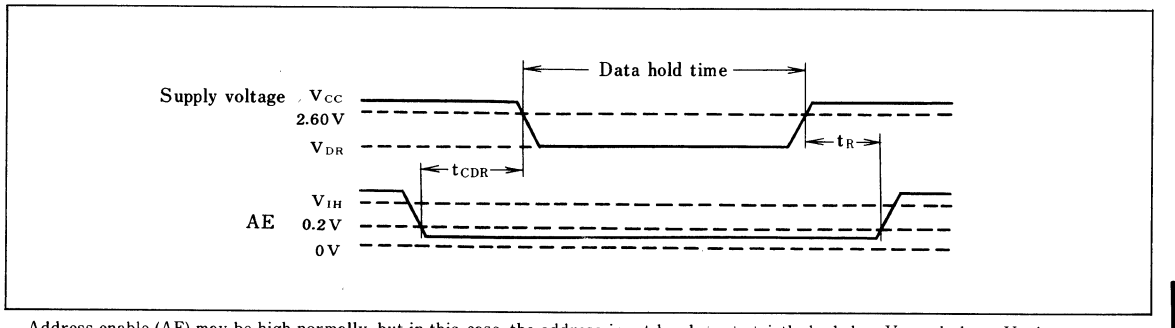
For data input/output separation, OD is made low.

(2) Write cycle



In I/O common mode, OD is made high during the write period. For data input/output separation, OD may be either high or low.

(3) Low-voltage data hold



Address enable (AE) may be high normally, but in this case, the address input level must strictly be below V_{IL} and above V_{IH} inclusive of noise spikes. Use of AE in such a timing relationship that the AE input is included inside the address input as shown in the timing chart is fairly recommended.

LH5101W CMOS 1024-Bit Static Random Access Memory

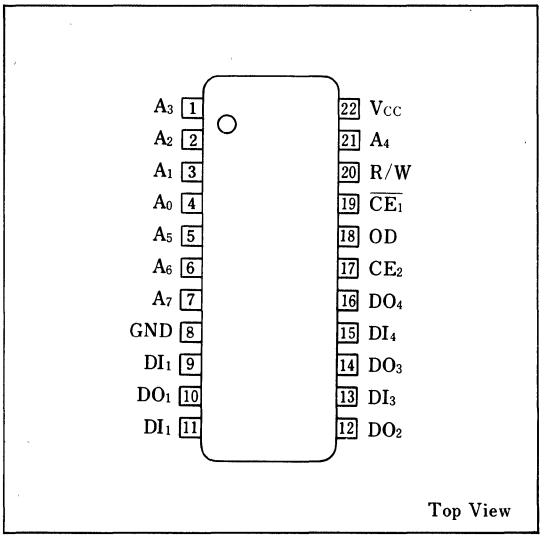
Description

The LH5101W is a fully static RAM organized as 256-word-by-4-bit by using silicon-gate CMOS process technology.

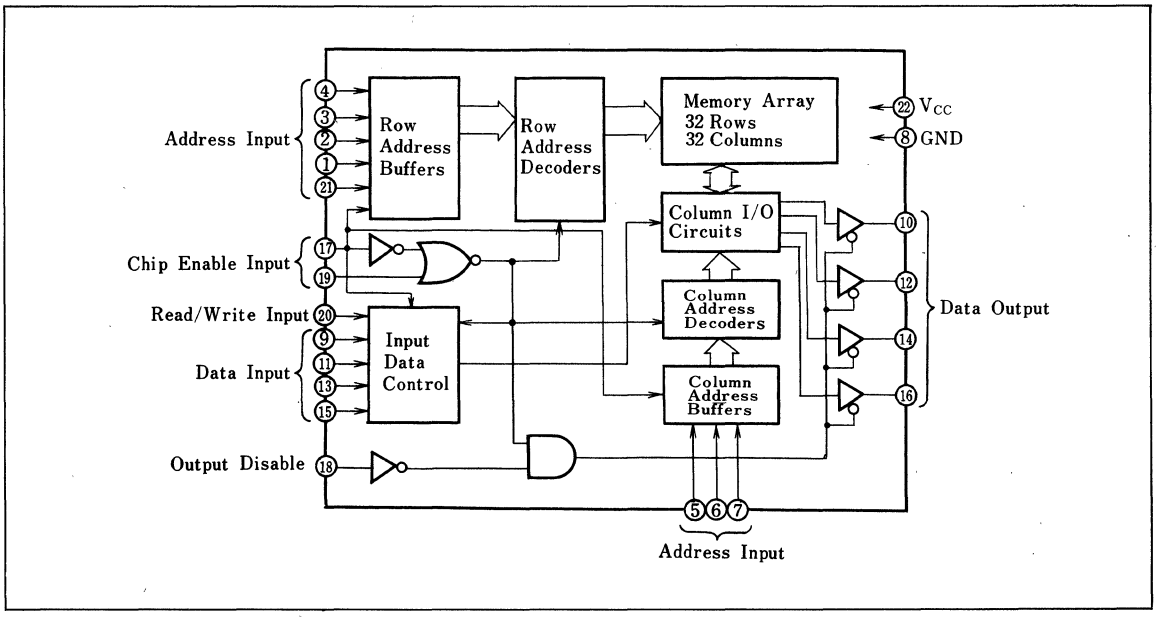
Features

1. 256-word-by-4-bit organization
2. Single +5V power supply
3. Fully static operation
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.) : 800ns
7. Data can be held on +2V supply voltage
8. Low power supply current at standby mode 100 μA (MAX.)
9. 22-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage*	V_{OUT}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

*The maximum applicable voltage on any pin with respect to GND.

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}		0.3		0.65	V
Input high voltage	V_{IH}		2.2		V_{CC}	V
Output low voltage	V_{OL}	I_{OL}=0.2mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V
Input current	$\lvert I_{LI} \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$			1.0	μA
Output leakage current	$\lvert I_{LO} \rvert$	$0 \leqq V_{IN} \leqq V_{CC}$, $\overline{CE_1}$=2.2V			1.0	μA
Current consumption 1	I_{CC1}	Output open, $V_{IN}=V_{CC}$, $\overline{CE_1} \leqq 0.65V$		9	22	mA
Current consumption 2	I_{CC2}	Output open, V_{IN}=2.2V, $\overline{CE_1} \leqq 0.65V$		13	27	mA
Chip disabled current consumption	I_{CCL}	$0 \leqq V_{IN} \leqq V_{CC}$, $\overline{CE_2} \leqq 0.2V$			100	μA

■ AC Characteristics

(1) Read cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	800			ns
Access time	t_{ACC}			800	ns
Chip enable time 1	t_{CO1}			800	ns
Chip enable time 2	t_{CO2}			850	ns
Output enable time	t_{OD}			350	ns
Chip turn-off time	t_{DF}			200	ns
Data hold time from address	t_{OH1}	0			ns
Data hold time from $\overline{CE_1}$	t_{OH2}	0			ns

(2) Write cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{WC}	800			ns
Access time	t_{AW}	200			ns
Chip enable time 1	t_{CW1}	600			ns
Chip enable time 2	t_{CW2}	600			ns
Data setup time	t_{DW}	400			ns
Data hold time	t_{DH}	100			ns
Pulse width	t_{WP}	400			ns
Recovery time	t_{WR}	50			ns
Input enable time	t_{DS}	200			ns

Test conditions of AC characteristics

- Input voltage amplitude ····· +0.65～+2.2V
- Input rising/falling time ····· 10ns
- Timing reference level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		3.5	6	pF
Output capacitance	C_{OUT}	V_{OUT}=0V		9	12	pF

■ Low-Voltage Data Hold Characteristics

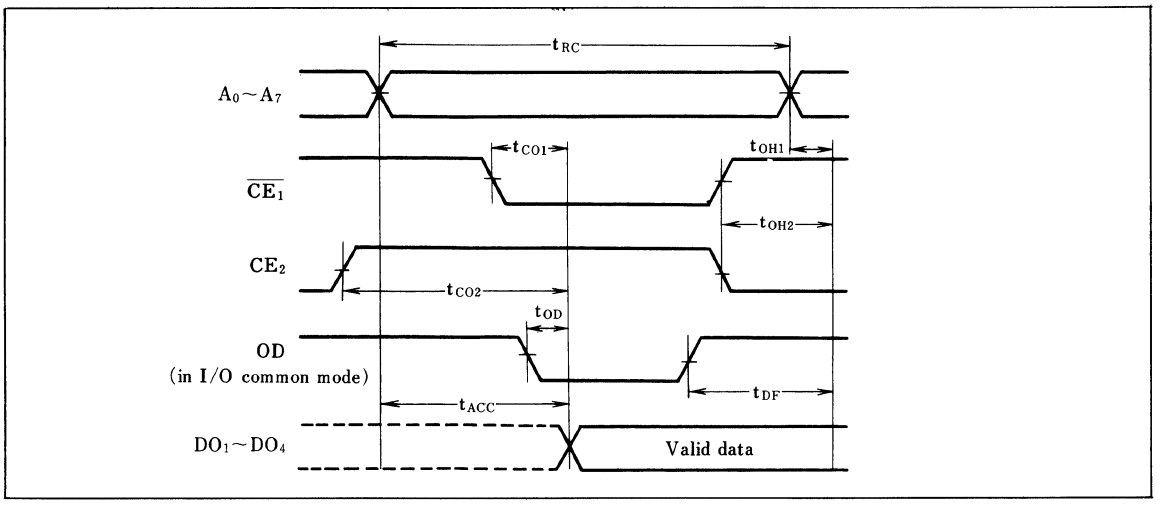
(Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage for data hold	V_{DR}	V_{CE2}≦0.2V	2.0			V
Supply current for data hold	I_{CCDR}	V_{CE2}≦0.2V, V_{DR}=2.0V			5	μA
Chip turn-off time	t_{CDR}		0			ns
Operation recovery time**	t_R		t_{RC}			ns

** In data hold mode, all input/output pins are put below V_{DR}.
t_{RC} : Read cycle time

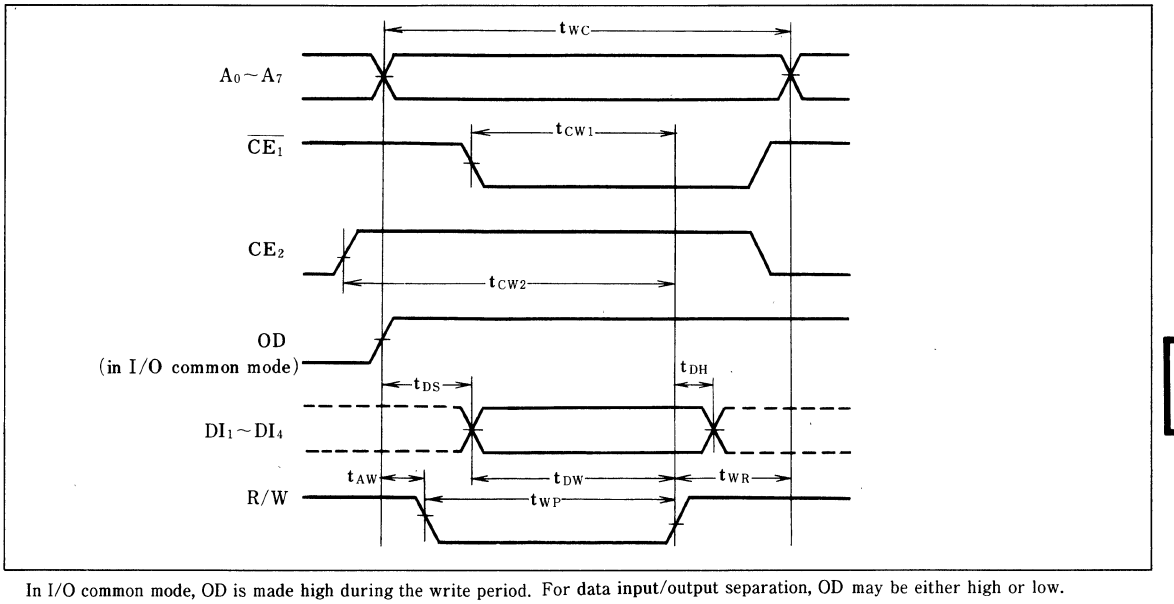
■ Timing Diagram

(1) Read cycle



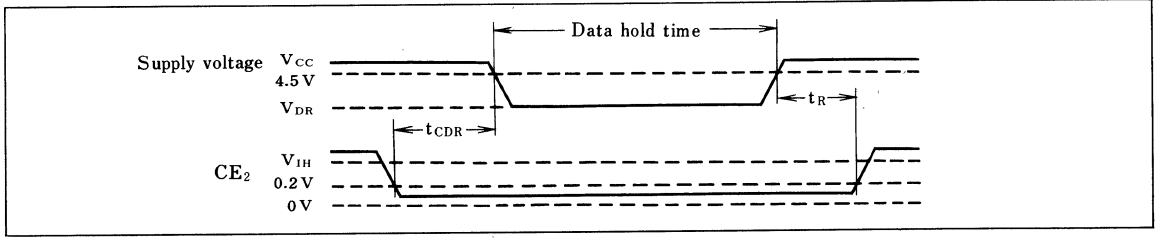
For data input/output separation, OD is mode low, In read cycle, R/W is mode high.

(2) Write cycle



In I/O common mode, OD is made high during the write period. For data input/output separation, OD may be either high or low.

(3) Low-voltage data hold



LH5102/LH5102-8
CMOS 2048-Bit Static Random Access Memory

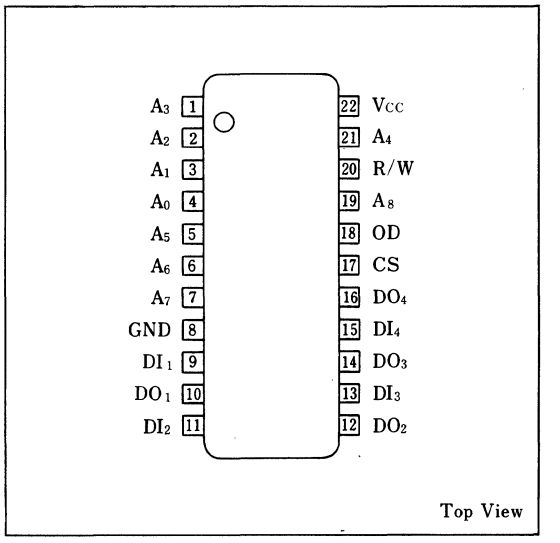
■ Description

The LH5102/LH5102-8 are fully static RAMs organized as 512-word-by-4-bit by using metal-gate CMOS process technology.

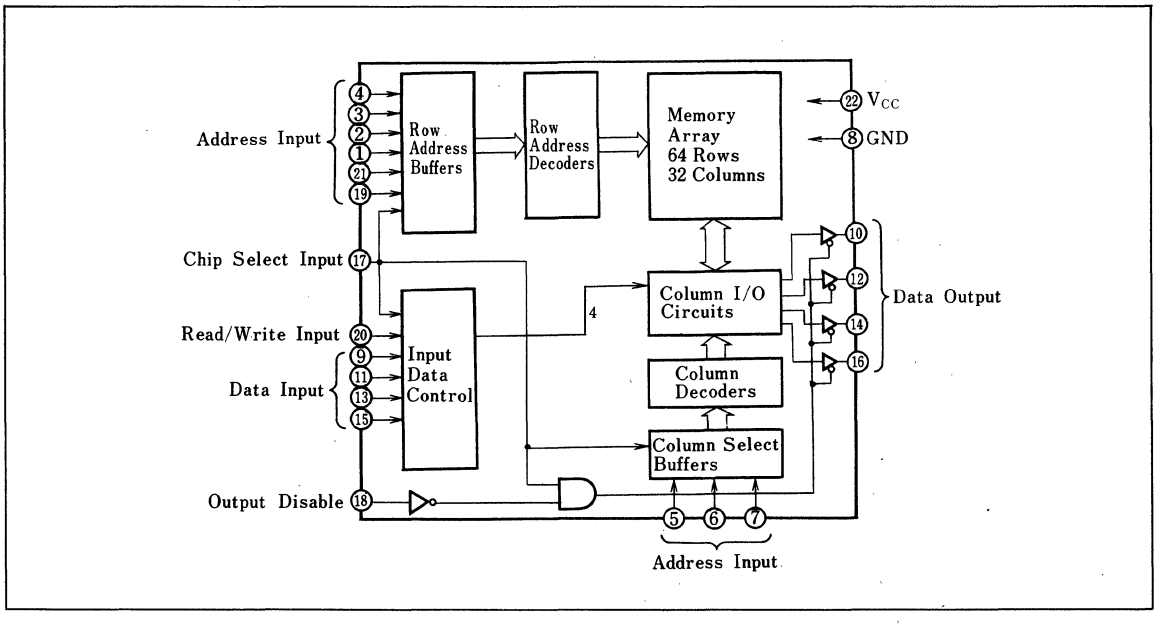
■ Features

1. 512-word-by-4-bit organization
2. Single +5V power supply
3. Low power consumption
4. Data can be held on +2V supply voltage
5. All inputs and outputs TTL compatible
6. Three-state outputs
7. Fully static operation
8. Pin compatible with SHARP LH5101 or Intel 5101 (except Pin 19)
9. Access time (MAX.)
   LH5102-8 : 800ns, LH5102 : 1,200ns
10. 22-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage*	V_{OUT}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

*The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions (Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Input voltage	V_{IL}	−0.3		0.65	V
	V_{IH}	2.2		V_{CC}	V

■ DC Characteristics (V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}		−0.3		0.65	V
Input high voltage	V_{IH}		2.2		V_{CC}	V
Output low voltage	V_{OL}	I_{OL}=2.0mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V
Input current	$\|I_{LI}\|$	V_{IN}=0 or V_{CC}			7.0	μA
Output leakage current	$\|I_{LO}\|$	CS≦0.2V, V_{OUT}=0V or V_{CC}			1.0	μA
Current consumption	I_{CC1}	Output open, V_{IN}=V_{CC}		3	22	mA
	I_{CC2}	Output open, V_{IN}=2.2V		13	27	mA
Chip disable current consumption	I_{CCL}	CS≦0.2V			200	μA

■ AC Characteristics (V_{CC}=5V±5%, Ta=0～+70℃)

Parameter	Symbol	LH5102-8			LH5102			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Read cycle								
Cycle time	t_{RC}	900			1,200			ns
Access time	t_{ACC}			800			1,200	ns
Chip enable time	t_{CO}			800			1,200	ns
Output enable time	t_{OD}			400			500	ns
Chip turn-off time	t_{DF}	0		200	0		250	ns
Data hold time	t_{OH}	0			0			ns
Write cycle								
Cycle time	t_{WC}	900			1,200			ns
Access time	t_{AW}	150			300			ns
Data setup time	t_{DW}	−200			0			ns
Data hold time	t_{DH}	70			100			ns
Pulse width	t_{WP}	650			400			ns
Recovery time	t_{WR}	100			200			ns
Input enable time	t_{DS}	150			250			ns

Test conditions of AC characteristics

- Input voltage amplitude ····· +0.65～+2.2V
- Input rising/falling time ····· 20ns
- Timing reference level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Low-Voltage Data Hold Characteristics

(Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage for data hold	V_{DR}	$V_{CS} \leqq 0.2V$	2.0			V
Supply current for data hold	I_{CCDR}	$V_{CS} \leqq 0.2V$, $V_{DR}=2.0V$			40	μA
Chip turn-off time	t_{CDR}		0			ns
Operation recovery time**	t_R		t_{RC}			ns

**In data hold mode, all input/output pins are put below V_{DR}. t_{RC}: Read cycle time.

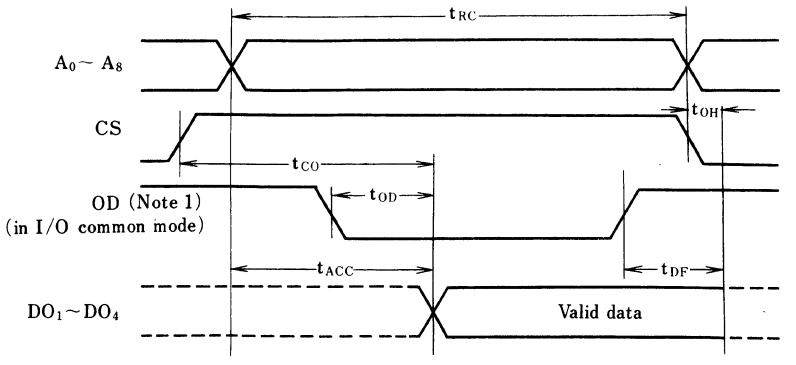
■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN}=0V$		6	10	pF
Output capacitance	C_{OUT}	$V_{OUT}=0V$		15	20	pF

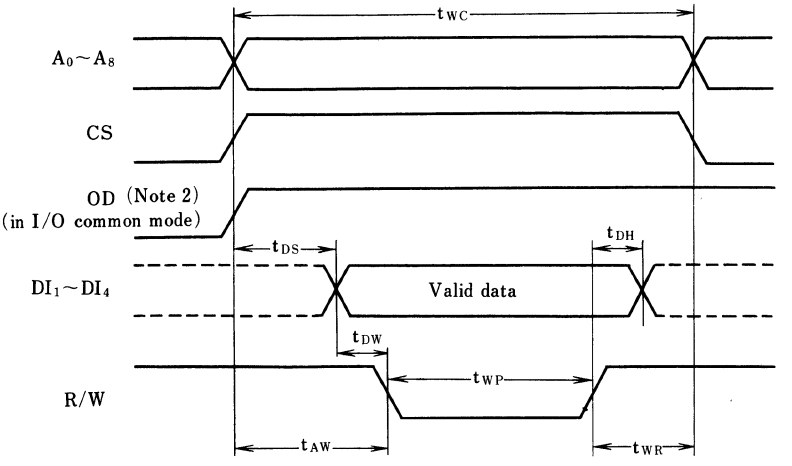
■ Timing Diagram

(1) Read cycle



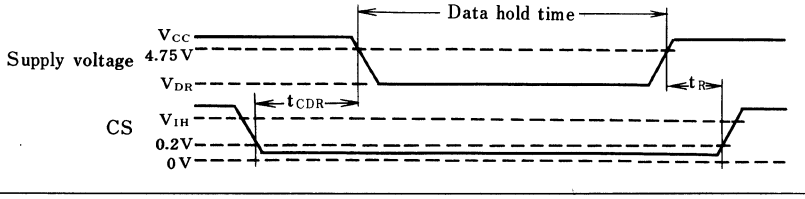
Note 1 : For data input/output separation, OD is made low.

(2) Write cycle



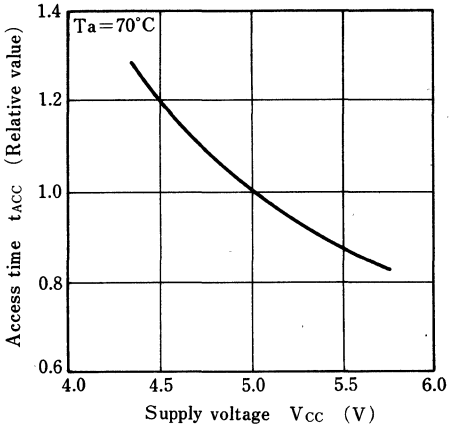
Note 2 : In I/O common mode, OD is made high during the write period. For data input/output separation, OD may be either high or low.

(3) Low-voltage data hold

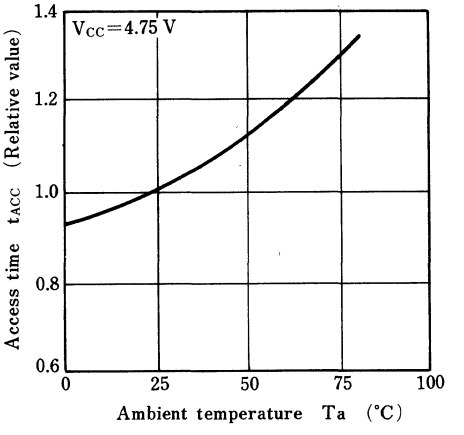


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

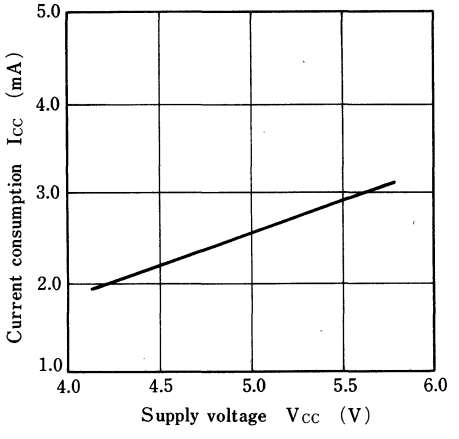
Access time vs. supply voltage



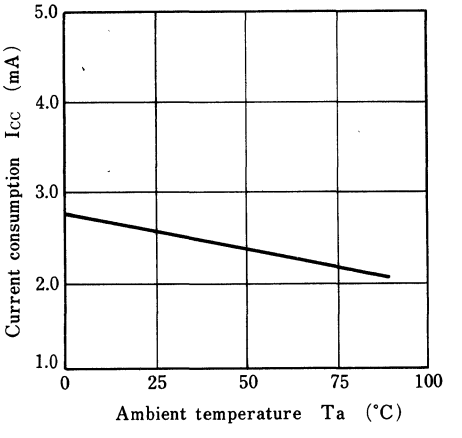
Access time vs. ambient temperature



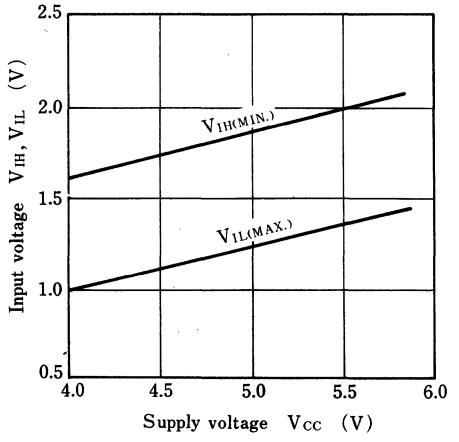
Current consumption vs. supply voltage



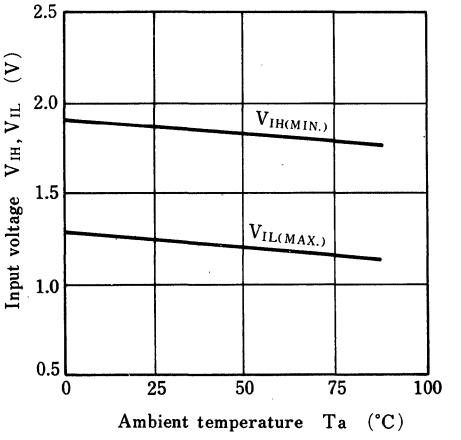
Current consumption vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



LH5102W CMOS 2048-Bit Static Random Access Memory

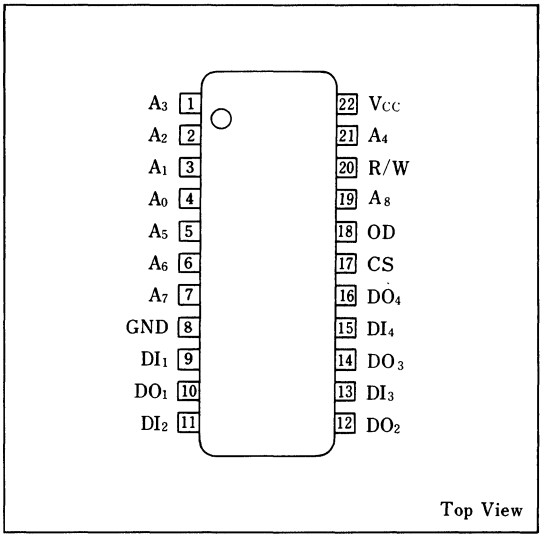
Description

The LH5102W is a fully static RAM organized as 512-word-by-4-bit by using metal-gate CMOS process technology.

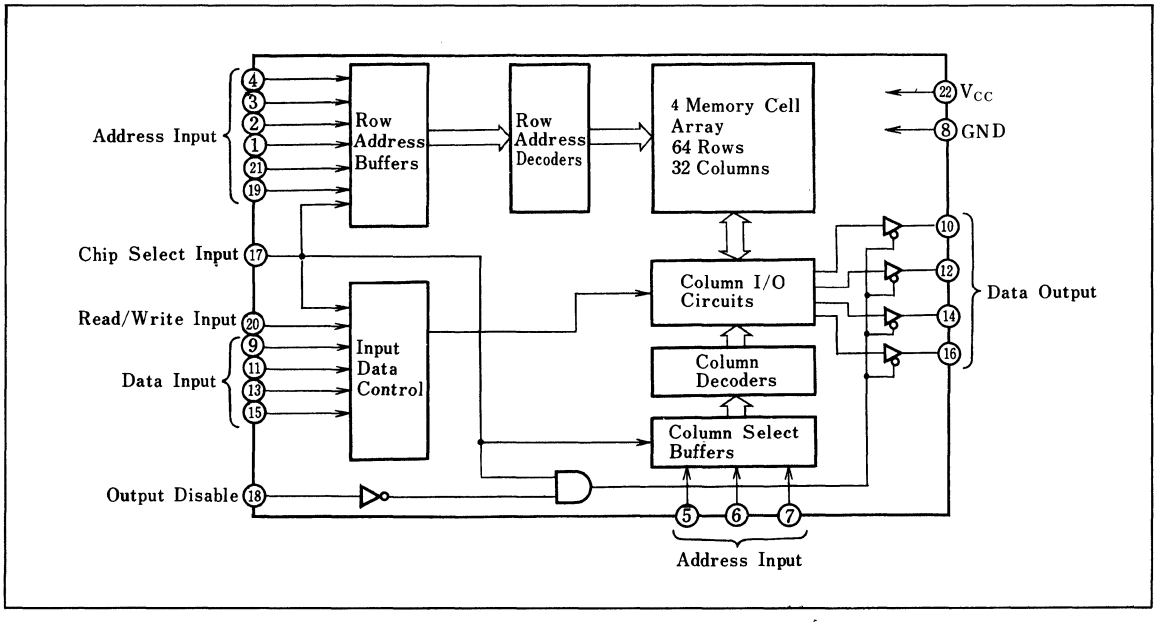
Features

1. 512-word-by-4-bit organization
2. Single +5V power supply
3. Low power consumption
4. Data can be held on +2V supply voltage
5. All inputs and outputs TTL compatible
6. Three-state outputs
7. Fully static operation
8. Pin compatible with SHARP LH5101 or Intel 5101 (except Pin-19)
9. Access time (MAX.) : 1,200ns
10. 22-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage*	V_{OUT}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	−20～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

*The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.0	5	5.5	V
Input voltage	V_{IL}	−0.3		0.65	V
	V_{IH}	2.2		V_{CC}	V

■ DC Characteristics

(V_{CC}=5V±10%, Ta=−20～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}		−0.3		0.65	V
Input high voltage	V_{IH}		2.2		V_{CC}	V
Output low voltage	V_{OL}	I_{OL}=2.0mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V
Input current	$\|I_{LI}\|$	V_{IN}=0V or V_{CC}			7.0	μA
Output leakage current	$\|I_{LO}\|$	CS≦0.2V, V_{OUT}=0V or V_{CC}			1.0	μA
Current consumption	I_{CC1}	Output open, V_{IN}=V_{CC}		3	22	mA
	I_{CC2}	Output open, V_{IN}=2.2V		13	27	mA
Chip disabled current consumption	I_{CCL}	CS≦0.2V			200	μA

■ AC Characteristics

(V_{CC}=5V±10%, Ta=−20～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Read cycle					
Cycle time	t_{RC}	1.2			μs
Access time	t_{ACC}			1.2	μs
Chip enable time	t_{CO}			1.2	μs
Output enable time	t_{OD}			500	ns
Chip turn-off time	t_{DF}	0		250	ns
Data hold time	t_{OH}	0			ns
Write cycle					
Cycle time	t_{WC}	1.2			μs
Access time	t_{AW}	300			ns
Data setup time	t_{DW}	0			ns
Data hold time	t_{DH}	100			ns
Pulse width	t_{WP}	400			ns
Recovery time	t_{WR}	200			ns
Input enable time	t_{DS}	250			ns

Test conditions of AC characteristics

- Input voltage amplitude ····· +0.65～+2.2V
- Input rising/falling time ····· 20ns
- Timing reference level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Low-Voltage Data Hold Characteristics

(Ta=−20～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage for data hold	V_{DR}	$V_{CS} \leqq 0.2V$	2.0			V
Supply current for data hold	I_{CCDR}	$V_{CS} \leqq 0.2V$, $V_{DR}=2.0V$			40	μA
Chip turn-off time	t_{CDR}		0			ns
Operation recovery time**	t_R		t_{RC}			ns

**In data hold mode, all input/output pins are put below V_{DR}. t_{RC} : Read cycle time

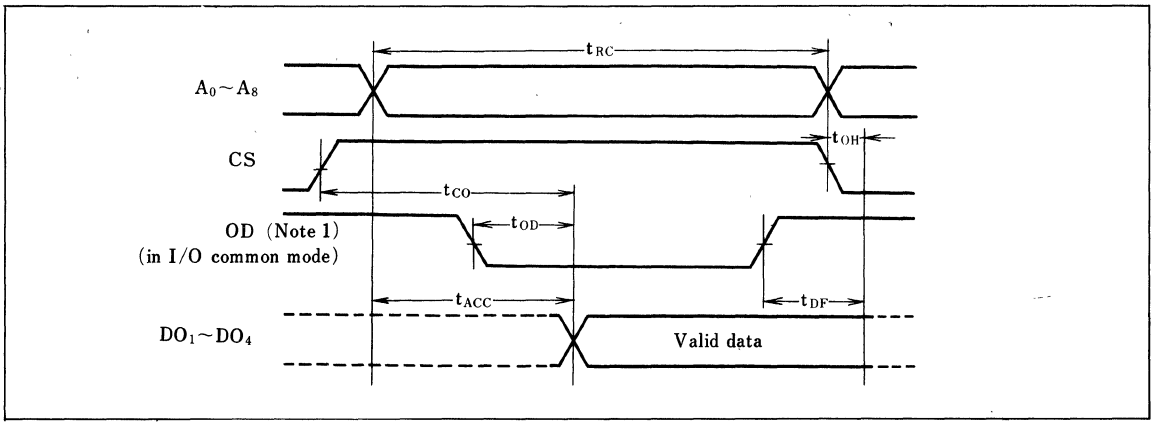
■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN}=0V$		6	10	pF
Output capacitance	C_{OUT}	$V_{OUT}=0V$		15	20	pF

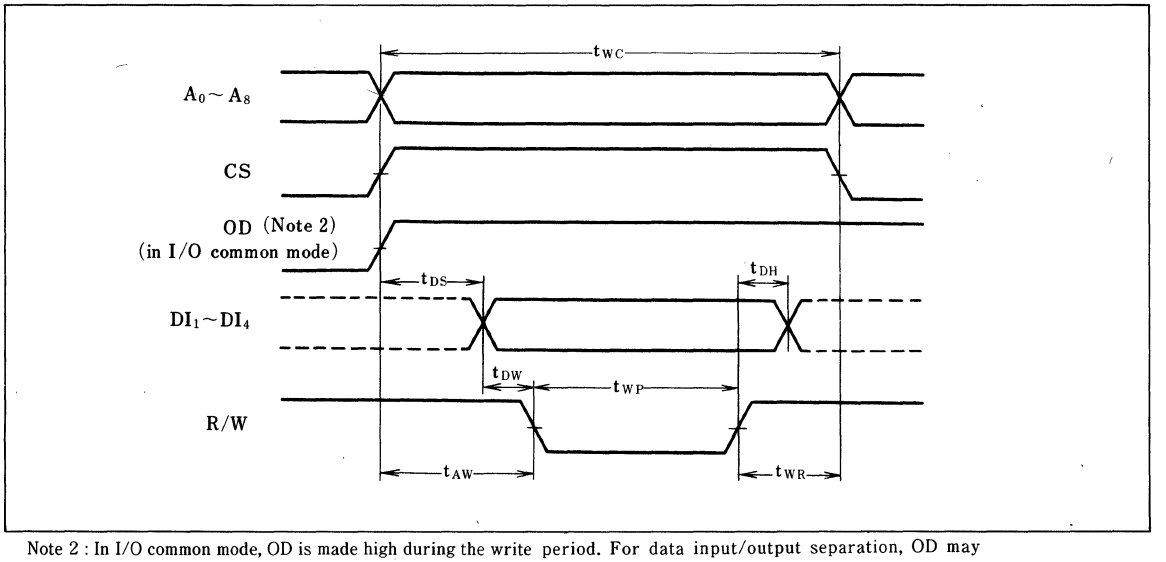
■ Timing Diagram

(1) Read cycle



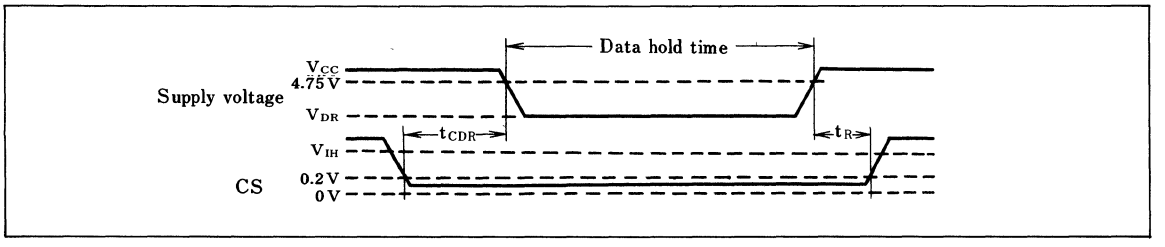
Note 1 : For data input/output separation, OD is made low.

(2) Write cycle



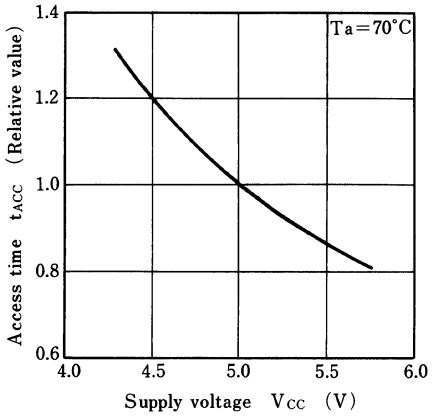
Note 2 : In I/O common mode, OD is made high during the write period. For data input/output separation, OD may be either high or low.

(3) Low-voltage data hold

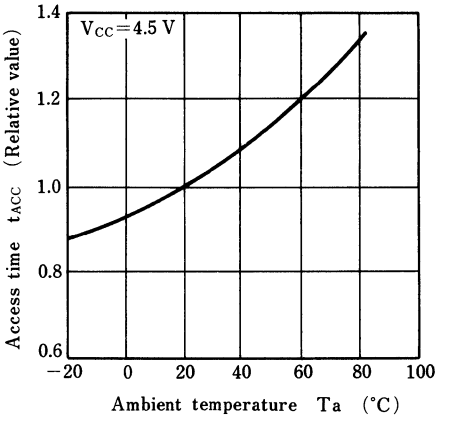


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

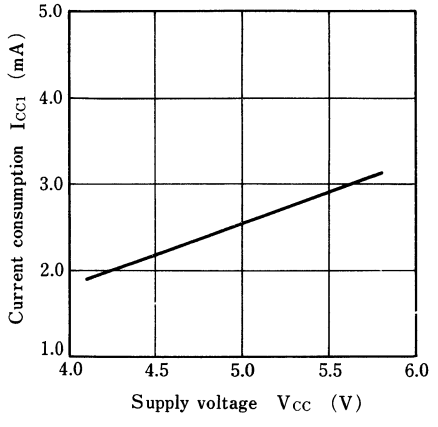
Access time vs. supply voltage



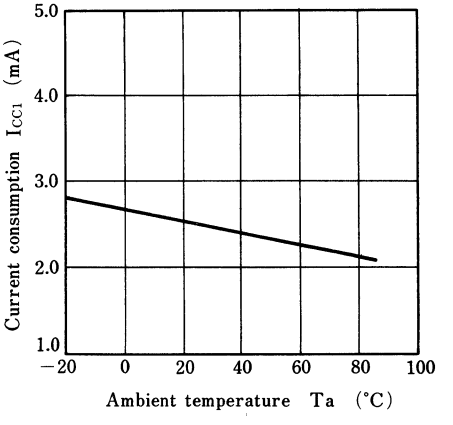
Access time vs. ambient temperature



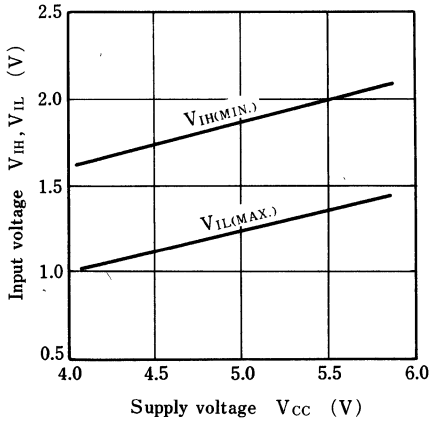
Current consumption vs. supply voltage



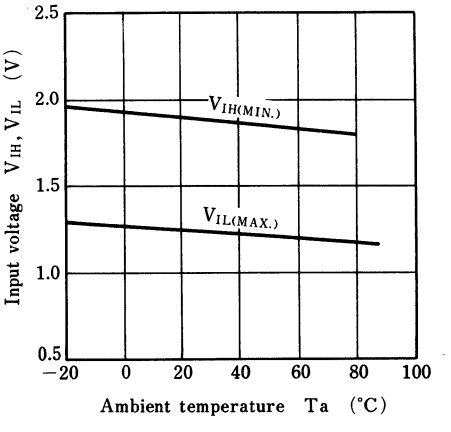
Current consumption vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



8

LH2114L-20

NMOS 4096-Bit Static Random Access Memory

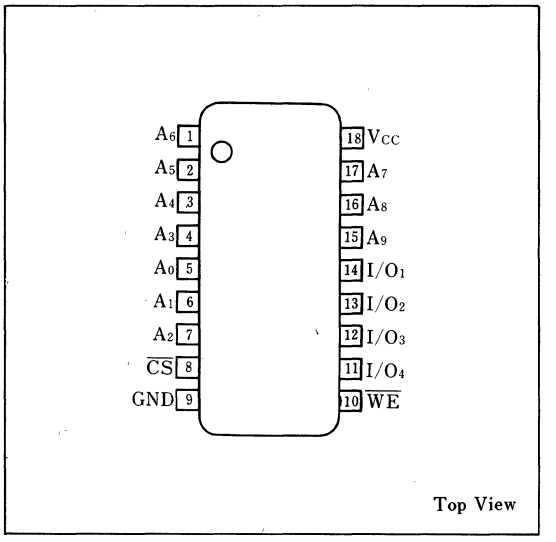
■ Description

The LH2114L-20 is a fully static RAM organized as 1024-word-by-4-bit by using silicon-gate NMOS process technology.

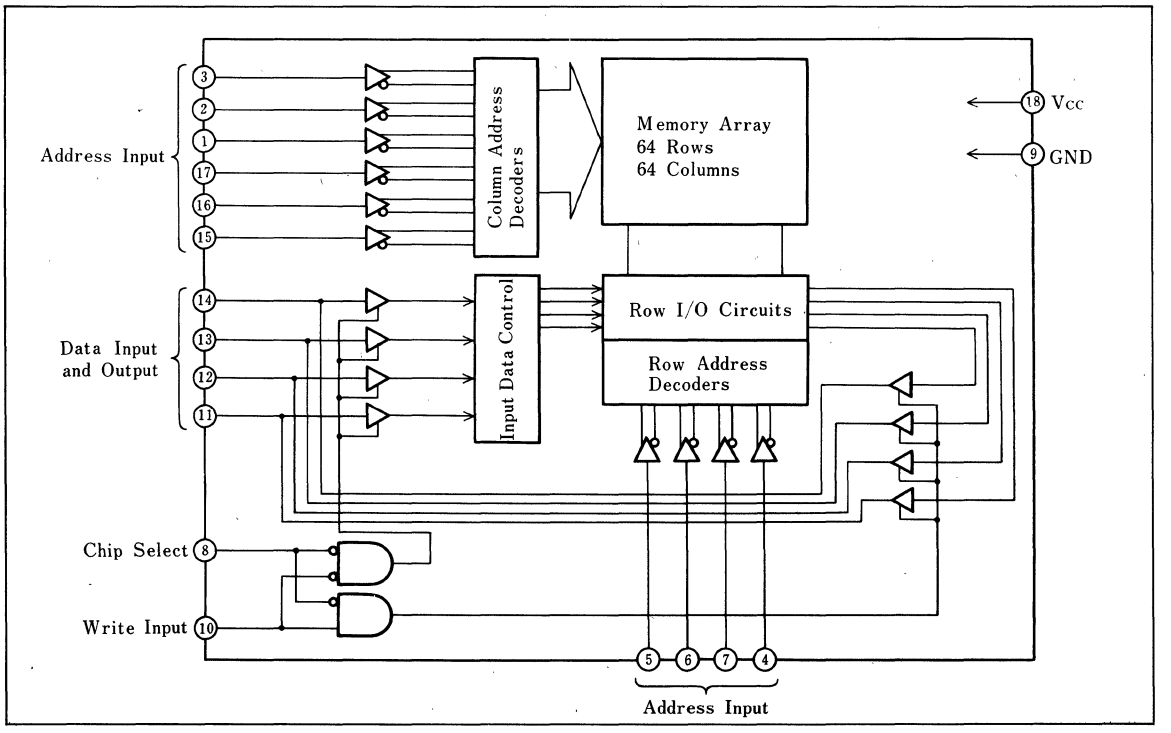
■ Features

1. 1,024-word-by-4-bit organization
2. Single +5V power supply
3. Fully static operation (no refresh or clock required)
4. All inputs and outputs TTL compatible
5. Three-state outputs.
6. Access time (MAX.) : 200ns
7. 18-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.5～+7.0	V
Input voltage*	V_{IN}	−0.5～+7.0	V
Output voltage*	V_{OUT}	−0.5～+7.0	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}				0.8	V
Input high voltage	V_{IH}		2.0			V
Output low voltage	V_{OL}	I_{OL}=2mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−1mA	2.4			V
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V or V_{CC}			10	μA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$=0.4V or V_{CC}			10	μA
Current consumption	I_{CC}	V_{IN}=5.5V, $I_{I/O}$=0mA			70	mA

■ AC Characteristics

(1) Read cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	200			ns
Access time	t_{ACC}			200	ns
Chip enable time	t_{CE}			80	ns
Chip select time	t_{CS}	10			ns
Output turn-off time	t_{DF}			70	ns
Output hold time	t_{OH}	20			ns

(2) Write cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{WC}	200			ns
Access time	t_{AW}	15			ns
Pulse width	t_{WP}	170			ns
Recovery time	t_{WR}	15			ns
Data setup time	t_{DW}	100			ns
Output turn-off time	t_{DF}			70	ns
Data hold time	t_{DH}	0			ns

Conditions for measurment of AC characteristics

- Input signal level ····· +0.4～+2.4V
- Input signal rise/fall time ····· 10ns
- Time measurement level ····· 1.5V
- Output load condition ····· 1TTL+100pF

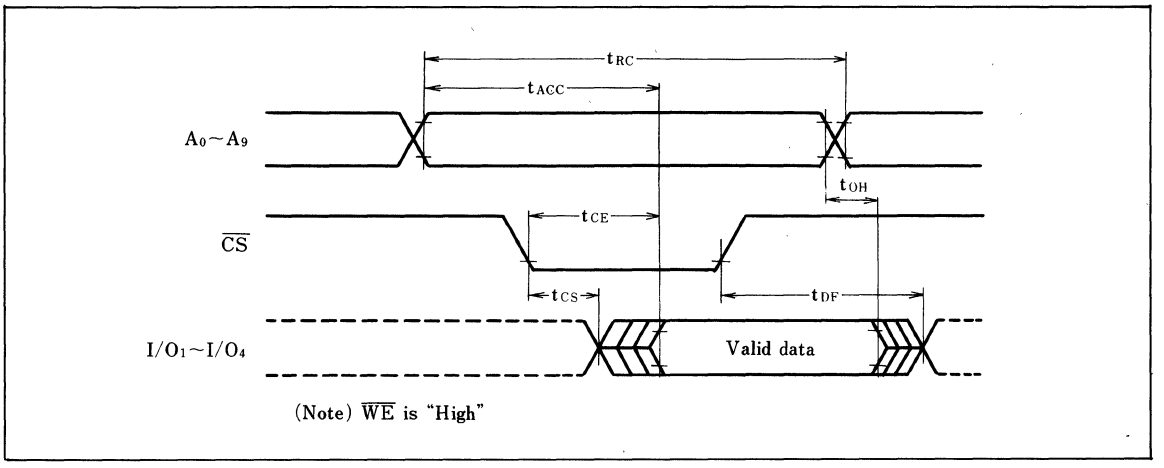
■ Pin Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		2	5	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0V		4.5	10	pF

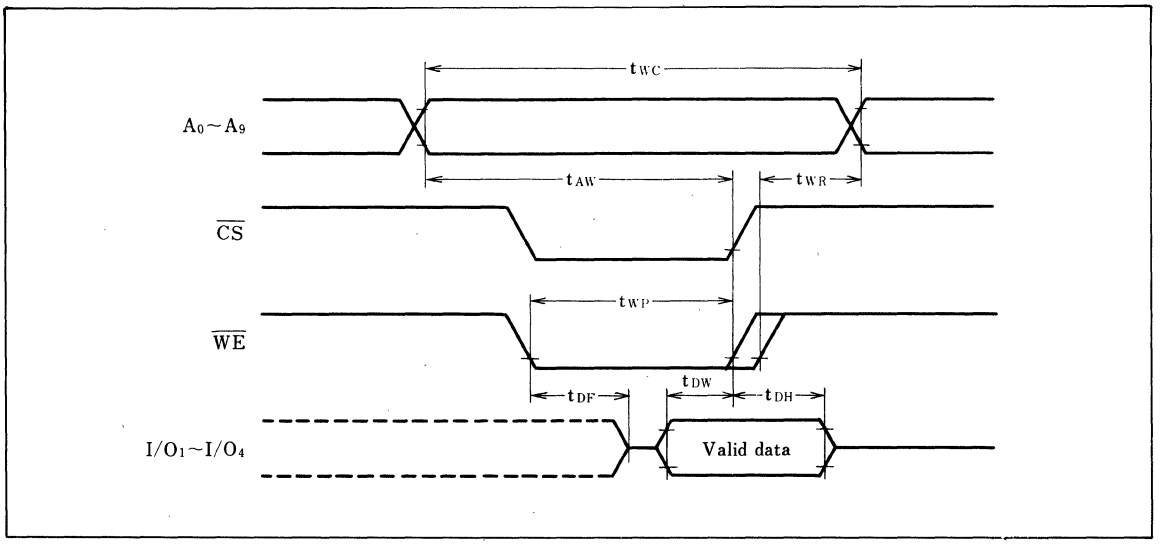
■ Timing Diagram

(1) Read cycle



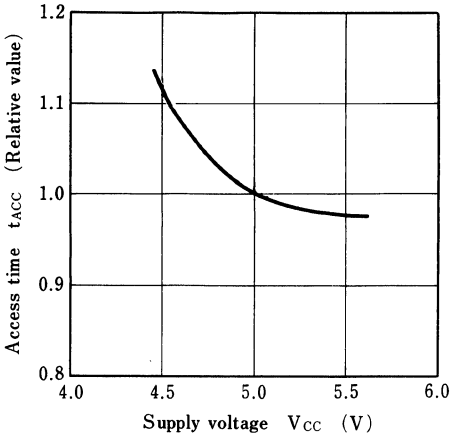
(Note) $\overline{WE}$ is "High"

(2) Write cycle

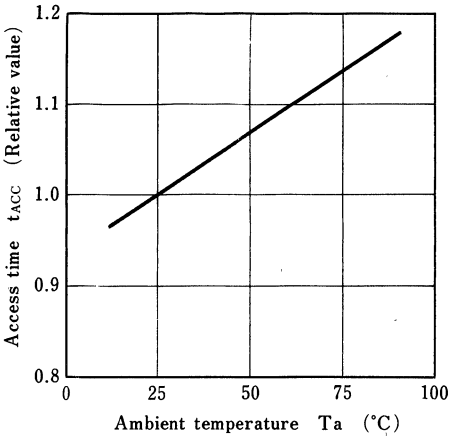


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

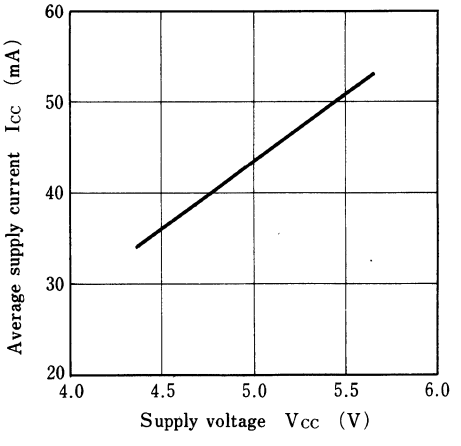
Access time vs. supply voltage



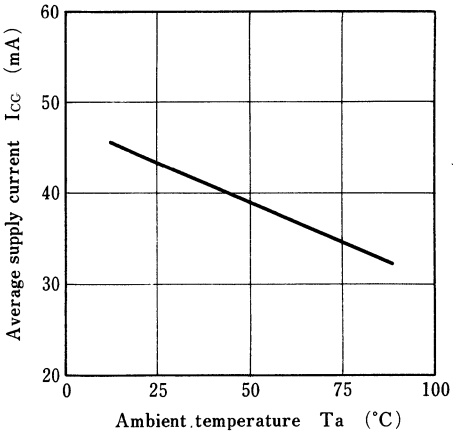
Access time vs. ambient temperature



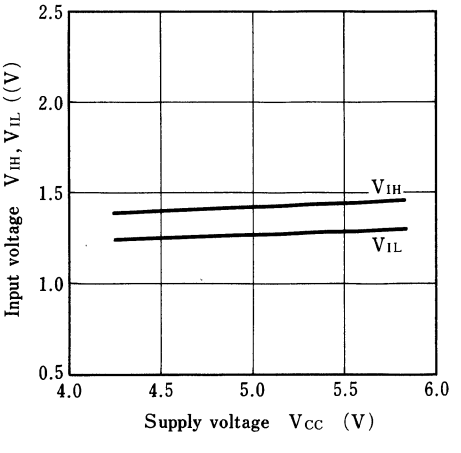
Average supply current vs. supply voltage



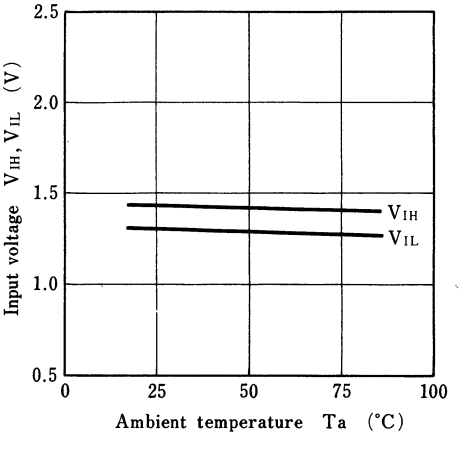
Average supply current vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



8

LH5114-4 CMOS 4096-Bit Static Random Access Memory

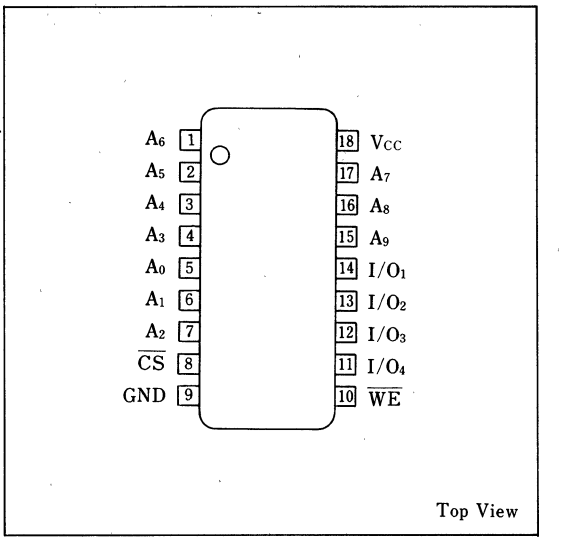
Description

The LH5114-4 is a fully static RAM organized as 1024-word-by-4-bit by using silicon-gate CMOS process technology.

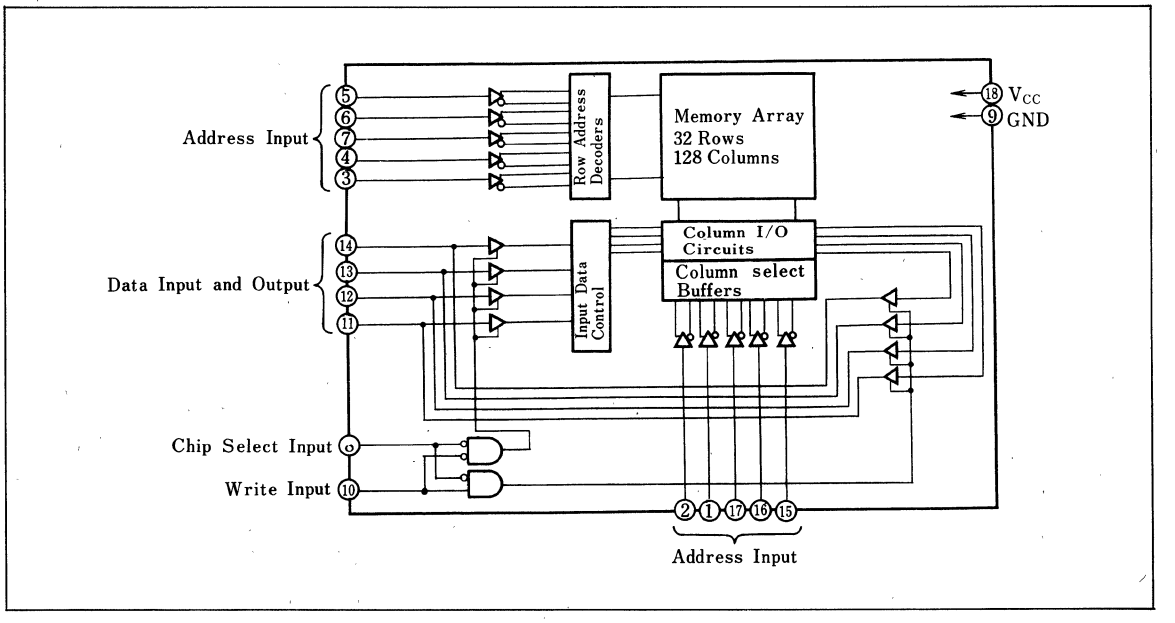
Features

1. 1,024-word-by-4-bit organization
2. Single +5V power supply
3. Fully static operation
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.) : 450ns
7. Data can be held on +2V supply voltage
8. Supply current at standby mode 10 μA (MAX.) on +2V supply voltage
9. 18-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage*	V_{OUT}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

*The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5	5.5	V
Input voltage	V_{IL}	−0.3		0.65	V
	V_{IH}	2.2		V_{CC}	V
Operating temperature	T_{opr}	0		70	℃

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}		−0.3		0.65	V
Input high voltage	V_{IH}		2.2		V_{CC}	V
Output low voltage	V_{OL}	I_{OL}=2mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−1mA	2.4			V
Input leakage current	$\|I_{LI}\|$	V_{IN}=0V or V_{CC}			1.0	μA
Output leakage current	$\|I_{LO}\|$	$\overline{CS}$≦V_{IH}, $V_{I/O}$=0.4V or V_{CC}			1.0	μA
Current consumption	I_{CC}	$\overline{CS}$≦0.65V, V_{IN}=V_{CC}=5.5V		6	15	mA
Chip disabled current consumption	I_{CCL}	$\overline{CS}$≦V_{CC}, 0≦V_{IN}≦V_{CC}			100	μA

■ AC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Read cycle					
Cycle time	t_{RC}	450			ns
Access time	t_{ACC}			450	ns
Chip enable time	t_{CO}			500	ns
Data hold time	t_{OH}	0			ns
Chip turn-off time	t_{DF}			150	ns
Write cycle					
Cycle time	t_{WC}	450			ns
Chip select time	t_{CW}	400			ns
Chip select hold time	t_{CH}	20			ns
Access time	t_{AW}	350			ns
Address setup time	t_{AS}	100			ns
Pulse width	t_{WP}	250			ns
Recovery time	t_{WR}	70			ns
Data setup time	t_{DW}	250			ns
Data hold time	t_{DH}	50			ns

Test conditions of AC characteristics

- Input voltage amplitude ····· +0.65～+2.2V
- Input rising/falling time ····· 10ns
- Timing reference level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Low-Voltage Data Hold Characteristics

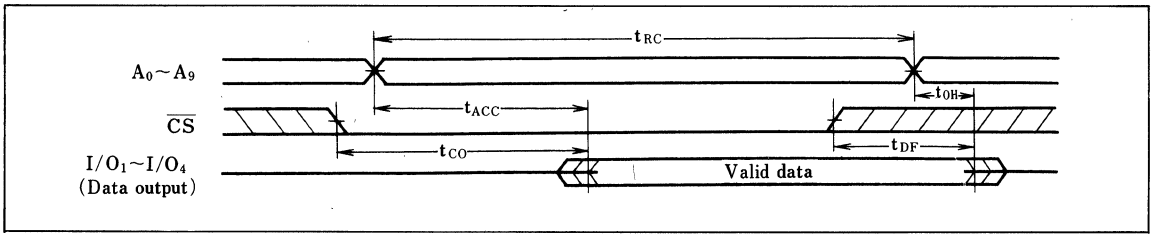
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage for data hold	$V_{CC(PD)}$		2.0			V
$\overline{CS}$ voltage for data hold	$V_{CC(\overline{CS})}$	$2.2V \leqq V_{CC(PD)} \leqq V_{CC}$	2.2			V
		$2.0V \leqq V_{CC(PD)} \leqq 2.2V$	$V_{CC(PD)}$			V
Supply current for data hold	$I_{CC(PD)}$	$V_{IN}=V_{CC}=2.0V$		0.5	10	μA
Chip turn-off time	$t_{S(PD)}$		t_{RC}			ns
Operation recovery time	$t_{R(PD)}$		t_{RC}			ns

■ Capacitance

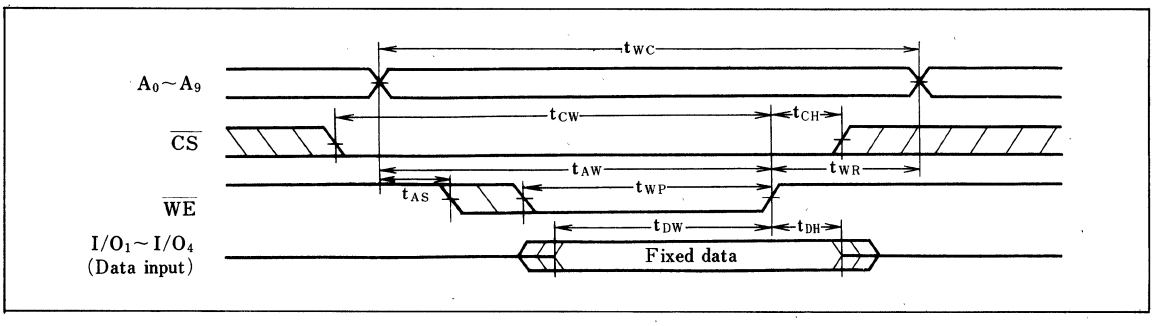
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN}=0V$			15	pF
Output capacitance	$C_{I/O}$	$V_{I/O}=0V$			35	pF

■ Timing Diagram

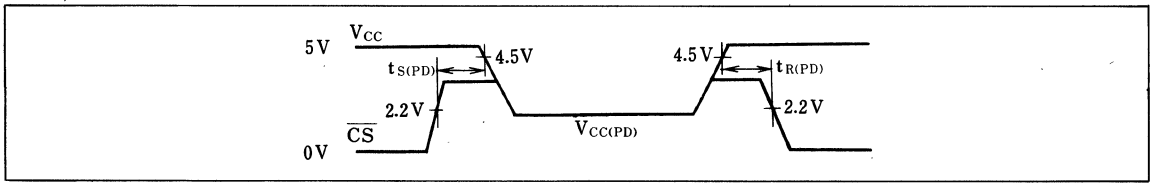
(1) Read cycle



(2) Write cycle

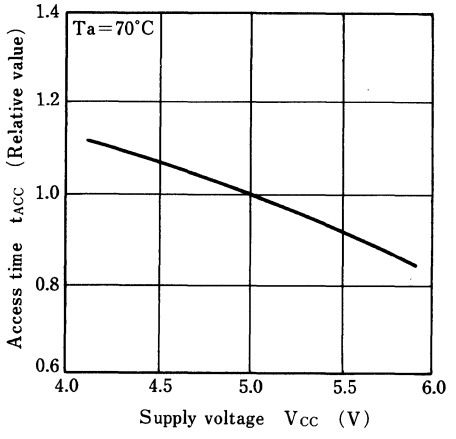


(3) Low-voltage data hold

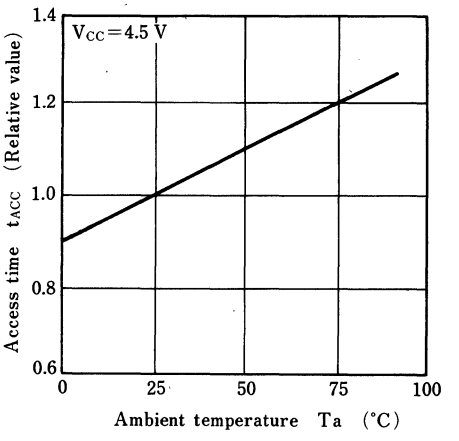


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

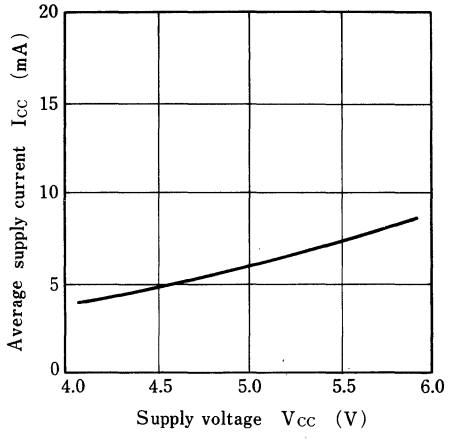
Access time vs. supply voltage



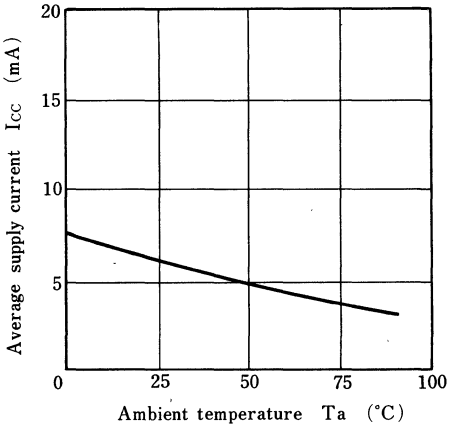
Access time vs. ambient temperature



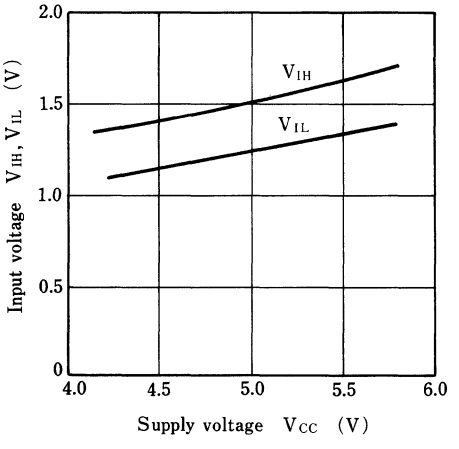
Average supply current vs. supply voltage



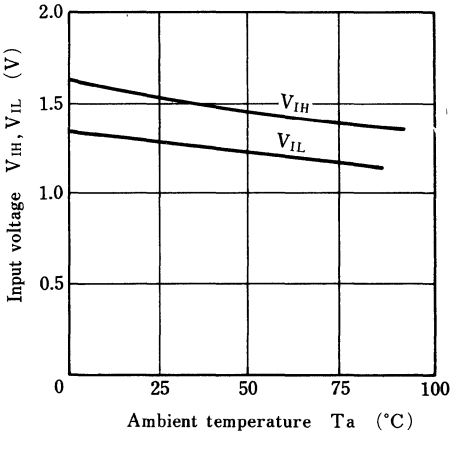
Average supply current vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



LH5104-4 CMOS 4096-Bit Static Random Access Memory

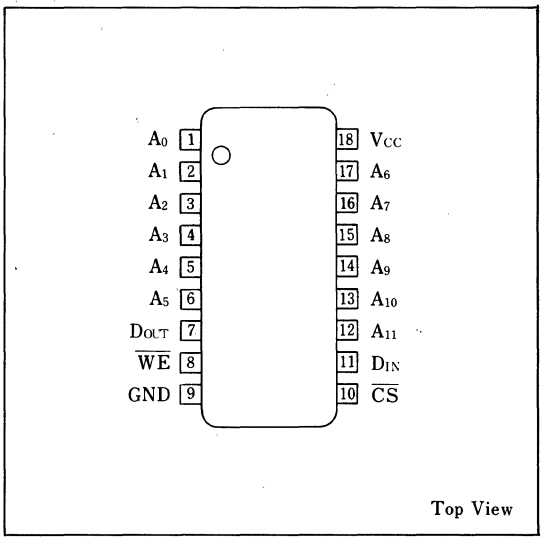
Description

The LH5104-4 is a fully static RAM organized as 4,096-word-by-1-bit by using silicon-gate CMOS process technology.

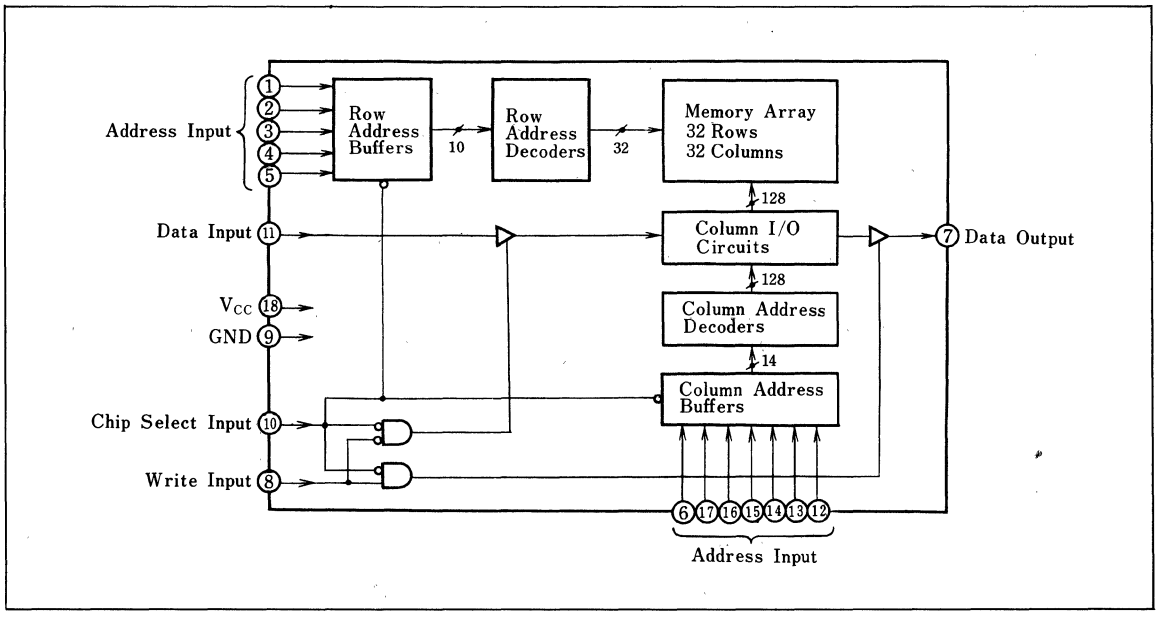
Features

1. 4,096-word-by-1-bit organization
2. Single +5V power supply
3. Fully static operation (no refresh or clock required)
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.) : 450ns
7. Data can be held on +2V supply voltage
8. Supply current at standby mode 10 μA on +2V supply voltage (MAX.)
9. 18-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～V_{CC}+0.3	V
Output voltage*	V_{OUT}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

* The maximum applicable voltage on any pin with respect to GND.

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}				0.65	V
Input high voltage	V_{IH}		2.2			V
Output low voltage	V_{OL}	I_{OL}=3.2mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−1mA	2.4			V
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V or V_{CC} open			1.0	μA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, V_{OUT}=0.4V or V_{CC} open			1.0	μA
Current consumption	I_{CC}	$\overline{CS}$=V_{IN}, Output open V_{IN}=V_{CC}=5.5V		7	15	mA
Chip disabled current consumption	I_{CCL}	$\overline{CS}$≧V_{CC}, V_{IN}=0V or V_{CC}			50	μA

■ AC Characteristics

(1) Read cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	450			ns
Access time	t_{ACC}			450	ns
Chip enable time 1	t_{CO}			450	ns
Data hold time from address	t_{OH}	30			ns
Chip turn-off time	t_{DF}			120	ns
Output enable time	t_{OD}	20			ns

(2) Write cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{WC}	450			ns
Chip select time	t_{CW}	320			ns
Access time	t_{AW}	340			ns
Address setup time	t_{AS}	120			ns
Pulse width	t_{WP}	200			ns
Recovery time	t_{WR}	90			ns
Data setup time	t_{DW}	200			ns
Data hold time	t_{DH}	300			ns
Output disable setup time	t_{WZ}			110	ns
Output enable setup time	t_{OW}	0			ns

Test conditions of AC characteristics

- Input voltage amplitude ····· +0.65～+2.2V
- Input rising/falling time ····· 10ns
- Timing reference level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V			6	pF
Output capacitance	C_{OUT}	V_{OUT}=0V			15	pF

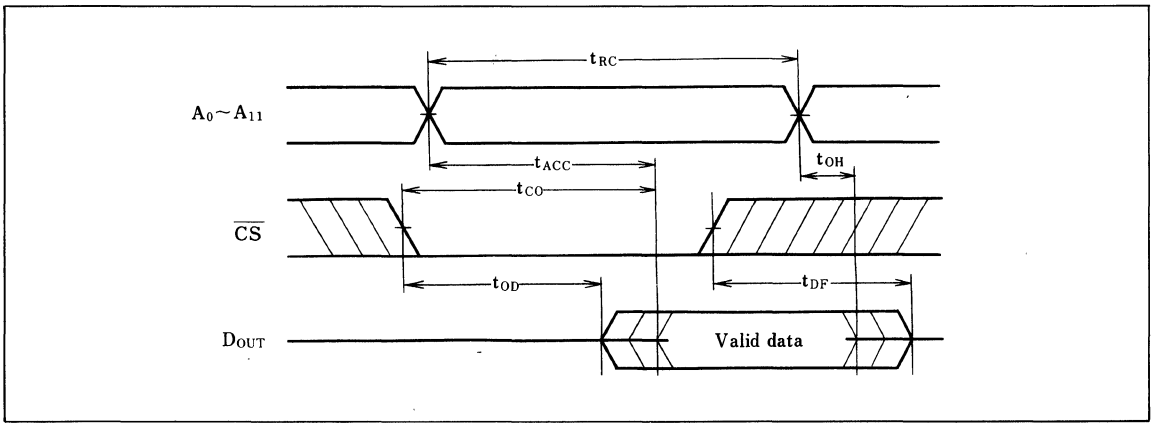
■ Low-Voltage Data Hold Characteristics

(Ta=0～+70℃)

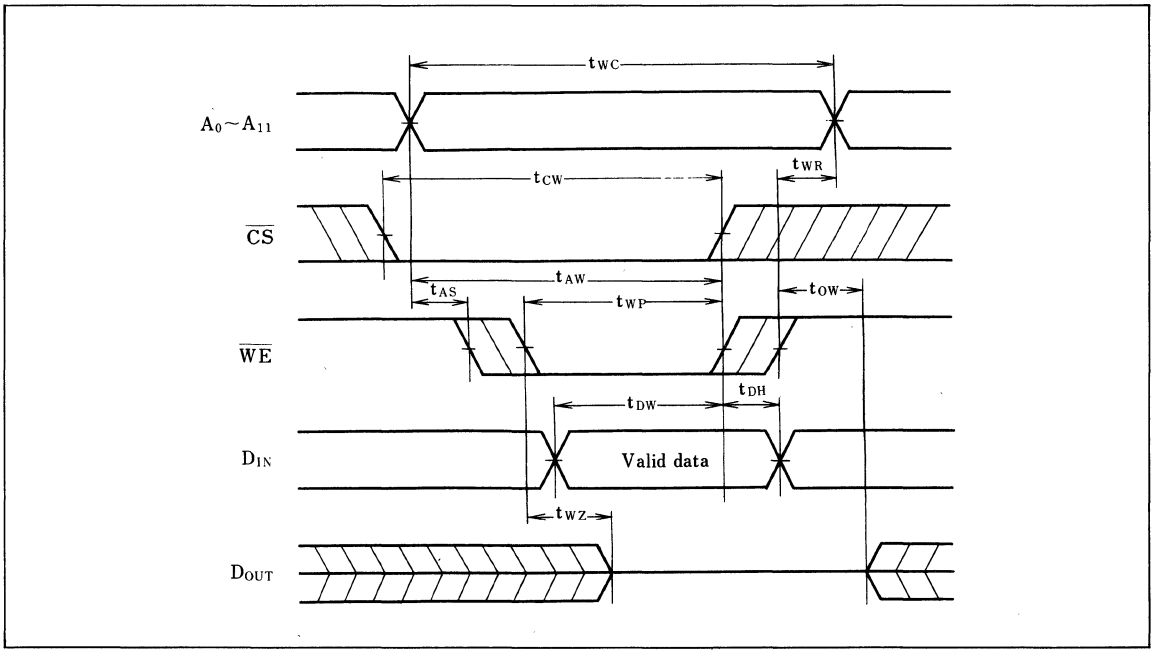
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage for data holding	$V_{CC(PD)}$		2.0			V
$\overline{CS}$ voltage for data hold	V_I	$2.2V \leqq V_{CC(PD)} \leqq V_{CC}$	2.2			V
		$2.0V \leqq V_{CC(PD)} \leqq 2.2V$	$V_{CC(PD)}$			
Supply current for data hold	$I_{CC(PD)}$	$V_{IN}=V_{CC}=2.0V$		0.2	10	μA
Chip turn-off time	$t_{S(PD)}$		t_{RC}			ns
Operation recovery time	$t_{R(PD)}$		t_{RC}			ns

■ Timing Diagram

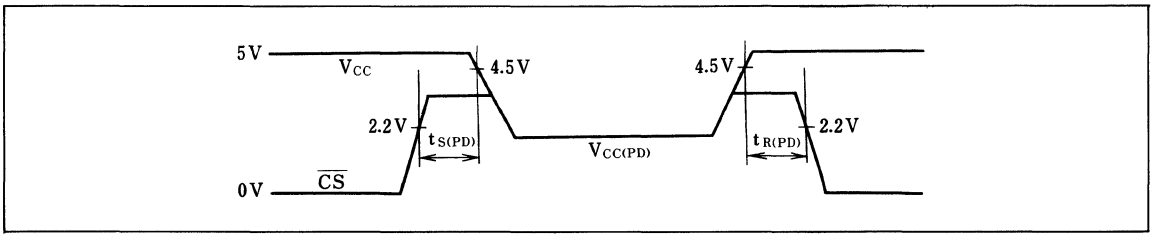
(1) Read cycle



(2) Write cycle

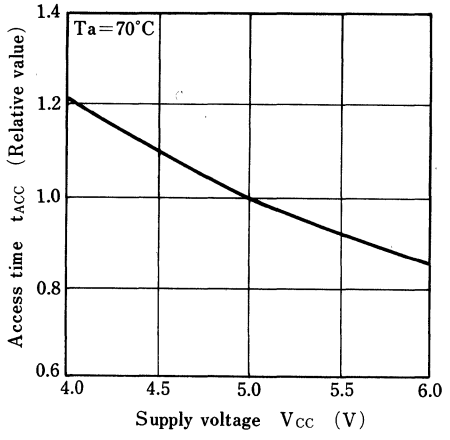


(3) Low-voltage data hold

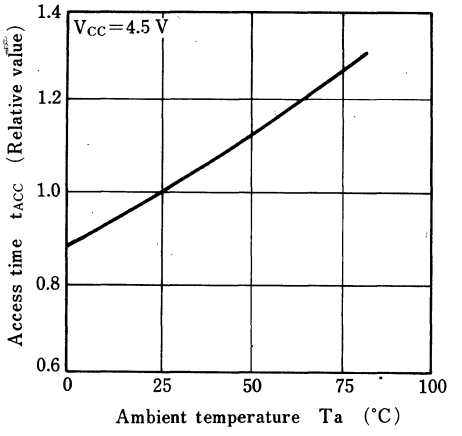


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

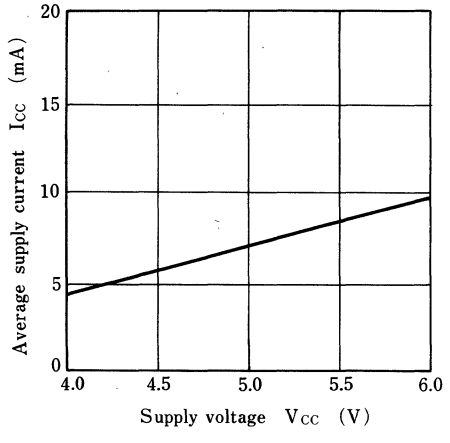
Access time vs. supply voltage



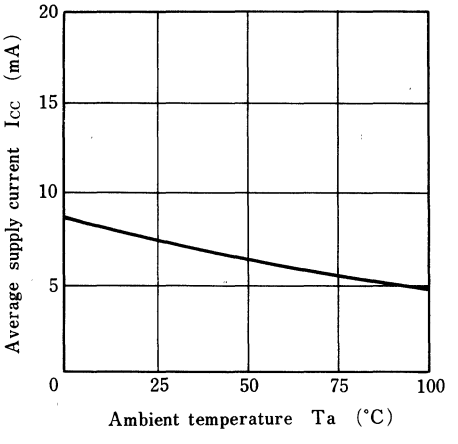
Access time vs. ambient temperature



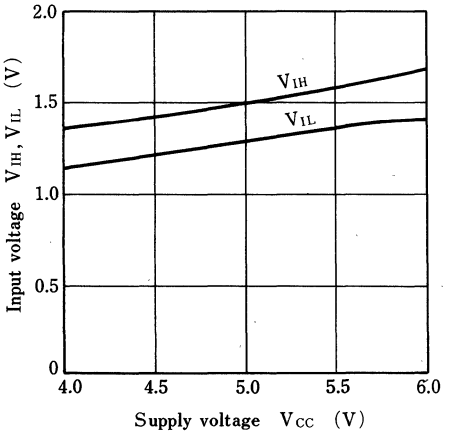
Average supply current vs. supply voltage



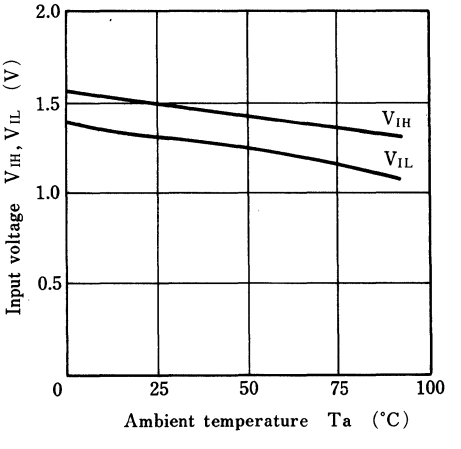
Average supply current vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



LH5116-15/LH5116-20

CMOS 16384-Bit Static Random Access Memory

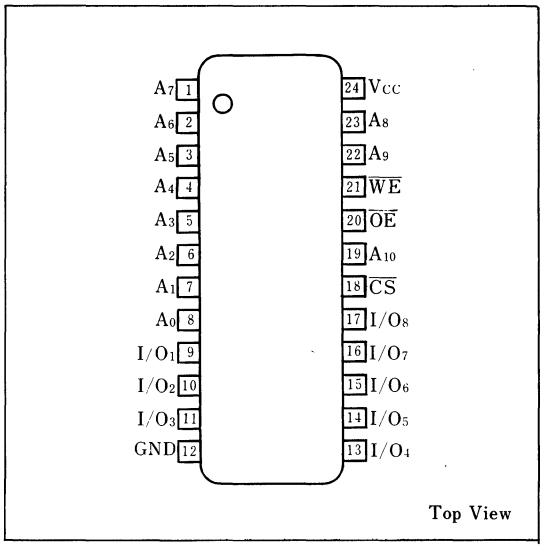
■ Description

The LH5116-15/LH5116-20 are fully static RAMs organized as 2,048-word-by-8-bit by using silicon-gate CMOS process technology.

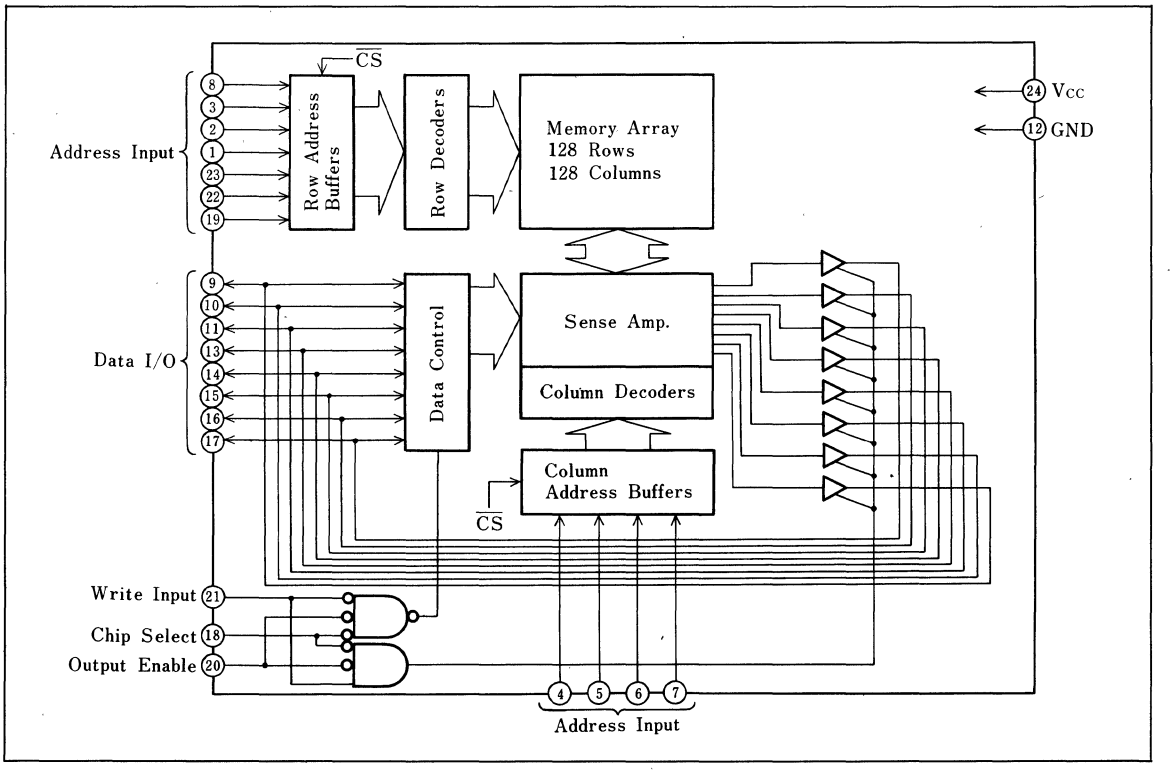
■ Features

1. 2,048-word-by-8-bit organization
2. Single +5V power supply
3. Fully static operation
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.)
   LH5116-15 : 150ns, LH5116-20 : 200ns
7. Supply current at standby mode 10 μA (MAX.) on +2V supply voltage
8. 24-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{CC}	−0.3～+7.0	V
Input voltage*	V_{IN}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

*The maximum applicable voltage on any pin with respect to GND.

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{IL}		−0.3		0.8	V	
Input high voltage	V_{IH}		2.2		V_{CC}+0.3	V	
Output low voltage	V_{OL}	I_{OL}=2.1mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V, V_{CC}			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V～V_{CC}			1.0	μA	
Current consumption	I_{CC1}	$I_{I/O}$=0mA ($\overline{OE}$=V_{CC})		15	30	mA	1
	I_{CC2}	$I_{I/O}$=0mA ($\overline{OE}$=V_{IH})		25	40	mA	2
Current consumption during standby	I_{CCL}	$\overline{CS}$=V_{CC}, all other input pins=0V−V_{CC}			10	μA	

Note 1 : $\overline{CS}$=0V ; all other input pins=V_{CC}
Note 2 : $\overline{CS}$=V_{IL} ; all other input pins=V_{IH}

■ AC Characteristics

(1) Read cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	LH5116-15			LH5116-20			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{RC}	150			200			ns
Access time	t_{ACC}			150			200	ns
Chip enable time	t_{CE}			150			200	ns
Chip select time	t_{CS}	15			20			ns
Output enable time	t_{OE}			75			100	ns
Output select time	t_{OS}	15			20			ns
Output turn-off time (from $\overline{CE_2}$)	t_{DF1}	0		40	0		60	ns
Output turn-off time (from $\overline{CE_1}$)	t_{DF2}	0		40	0		60	ns
Data hold time	t_{OH}	15			20			ns

(2) Write cycle

(V_{CC}=5V±10%, Ta=0～70℃)

Parameter	Symbol	LH5117-15			LH5117-20			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{WC}	150			200			ns
Chip select time	t_{CW}	110			135			ns
Access time	t_{AW}	110			135			ns
Address setup time	t_{AS}	0			5			ns
Pulse width	t_{WP}	110			140			ns
Recovery time	t_{WR}	20			35			ns
Output turn-off time (from $\overline{OE}$)	t_{DF1}			40			60	ns
Data setup time	t_{DW}	70			80			ns
Data hold time	t_{DH}	10			10			ns
Output turn-off hold time (from $\overline{WE}$)	t_{OW}	15			20			ns
Output turn-off time (from $\overline{OE}$)	t_{DF2}			40			60	ns

Conditions for measurement of AC characteristics

- Input voltage amplitude ····· +0.8~+2.2V
- Input signal rise/fall time ····· 10ns
- Time measurement level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Low Supply Voltage Data Hold Characteristics (V_{CC}=5V±10%, Ta=0~70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data hold supply voltage	V_{CCDR}	$V_{\overline{CS}}=V_{CC}$, $V_{IN}=0V$ or V_{CC}	2.0			V
Data hold supply current	I_{CCDR}	$V_{CC}=V_{\overline{CS}}=2.0V$, $V_{IN}=0V$ or V_{CC}			10	μA
$\overline{CS}$ setup time	t_{SDR}		t_{RC}			ns
$\overline{CS}$ hold time	t_{RDR}		t_{RC}			ns

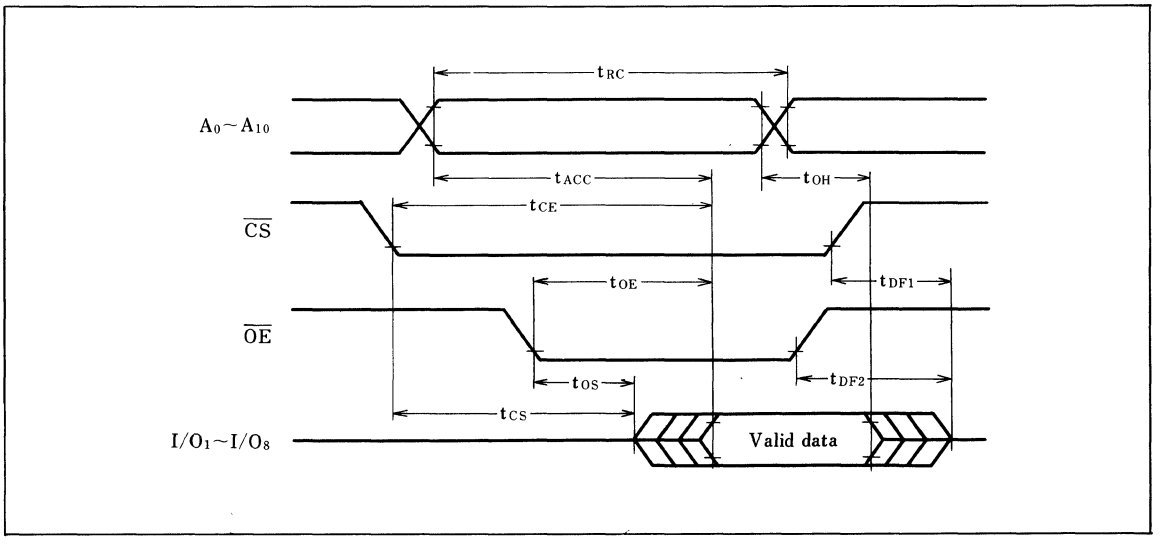
■ Capacitance

(f=1MHz, Ta=25℃)

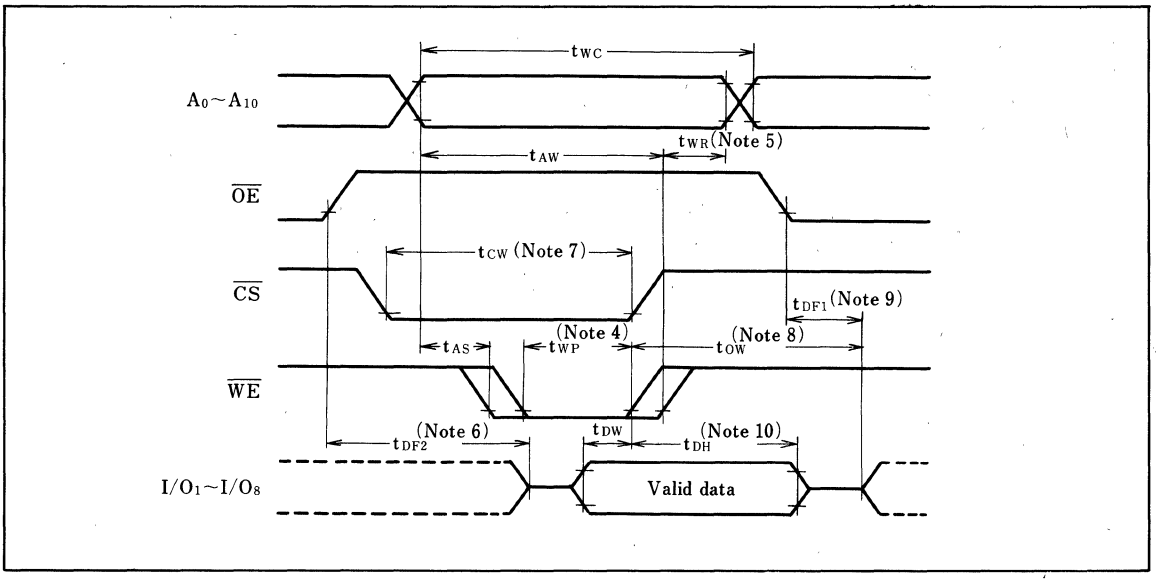
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN}=0V$			5	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}=0V$			8	pF

■ Timing Diagram

(1) Read cycle



(2) Write cycle (Note 3)



Note 3 : $\overline{WE}$ must be high when there is a change in A_0–A_{10}.

Note 4 : When $\overline{CS}$ and $\overline{WE}$ are all low at the same time, write occurs during the period t_{WP}.

Note 5 : t_{WR} is the time from the rise of $\overline{CS}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.

Note 6 : During this period the input/output pin is in an output condition, so input with a phase reversed from that of the output is not permitted.

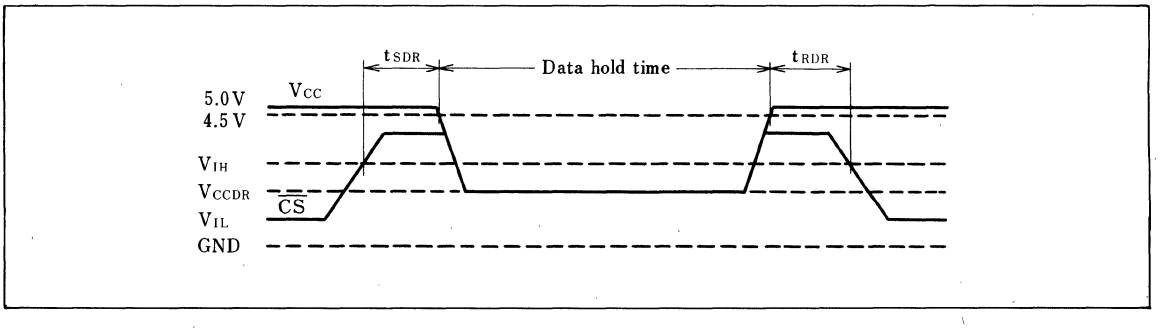
Note 7 : If $\overline{CS}$ should drop at the same time as $\overline{WE}$ or later, the output buffer is maintained at high impedance.

Note 8 : $\overline{OE}$ is maintained at "L" level.

Note 9 : D_{OUT} outputs data with the same phase as the input data of this write cycle.

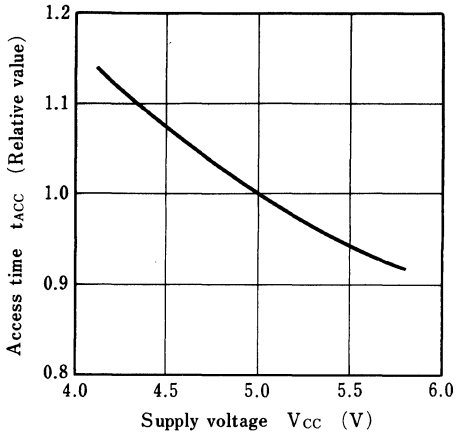
Note 10 : If $\overline{CS}$ is low during this period, the input/output pin is in the output condition. During this condition, a data input signal with a phase opposite that of the output is not permitted.

(3) Low supply voltage data hold

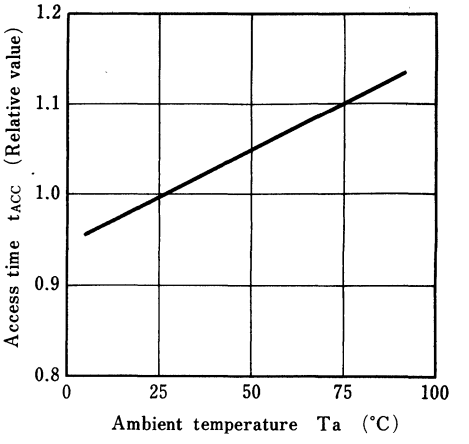


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

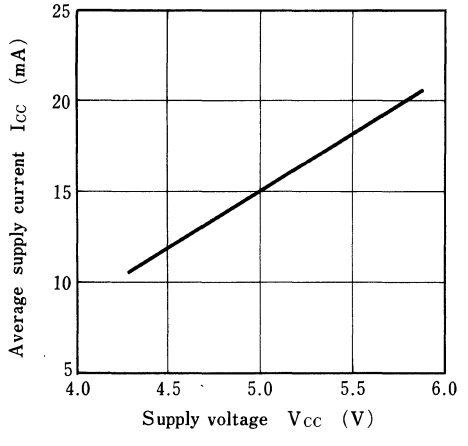
Access time vs. supply voltage



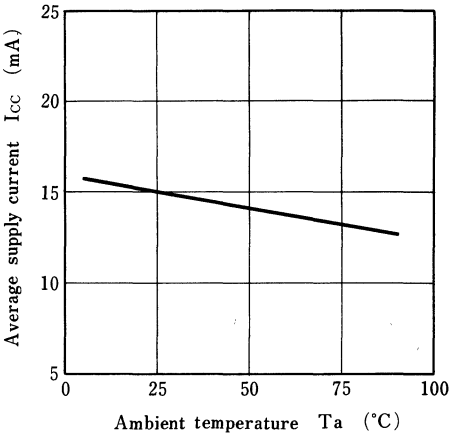
Access time vs. ambient temperature



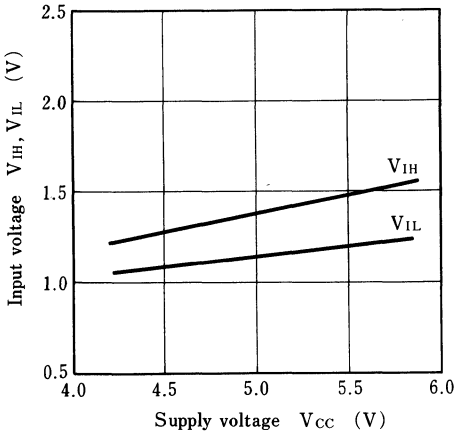
Average supply current 1 vs. supply voltage



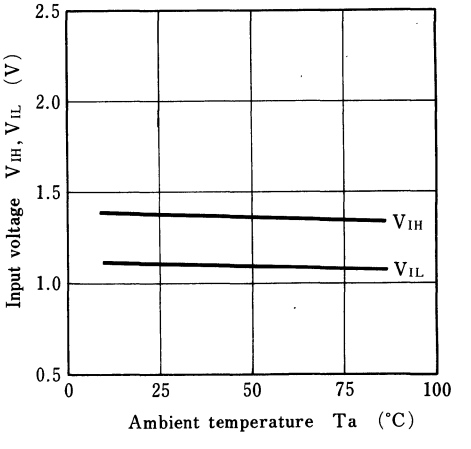
Average supply current 1 vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



LH5117-15/LH5117-20

CMOS 16384-Bit Static Random Access Memory

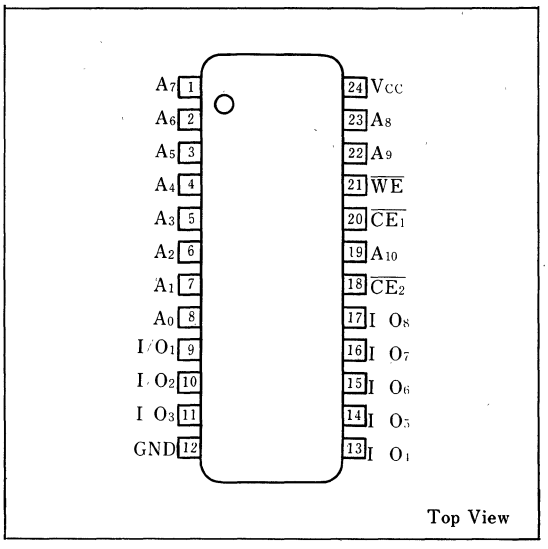
■ Description

The LH5117-15/LH5117-20 are fully static RAMs organized as 2,048-word-by-8-bit by using silicon-gate CMOS process technology.

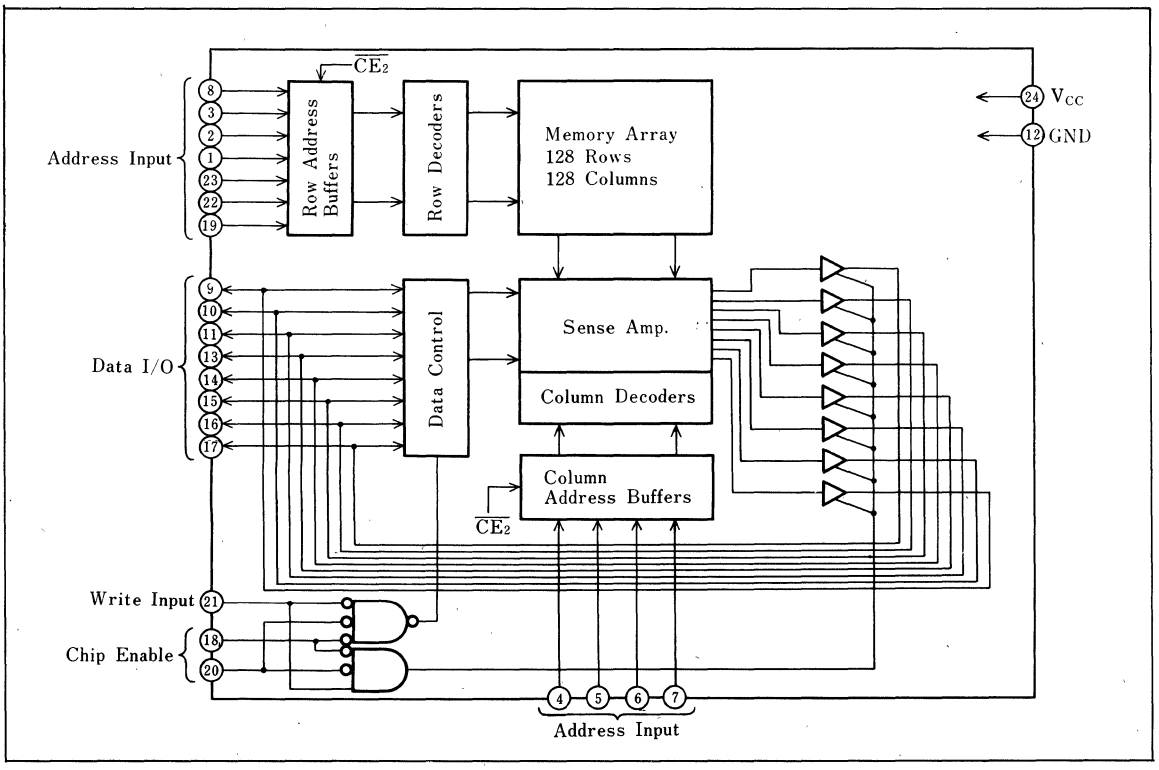
■ Features

1. 2,048-word-by-8-bit organization
2. Single +5V power supply
3. Fully static operation
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.)
   LH5117-15 : 150ns, LH5117-20 : 200ns
7. Supply current at standby mode 10 μA (MAX.)
   on +2V supply voltage
8. 24-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	−0.3～+7.0	V
Input voltage	V_{IN}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{IL}		−0.3		0.8	V	
Input high voltage	V_{IH}		2.2		V_{CC}+0.3	V	
Output low voltage	V_{OL}	I_{CL}=2.1mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V～V_{CC}			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CS_2}$=V_{IH}, $V_{I/O}$=0V～V_{CC}			1.0	μA	
Current consumption	I_{CC1}	$I_{I/O}$=0mA ($\overline{CE_1}$=V_{CC})		15	30	mA	1
	I_{CC2}	$I_{I/O}$=0mA ($\overline{CE_1}$=V_{IH})		25	40	mA	2
Current consumption during standby	I_{CCL}	$\overline{CE_2}$=V_{CC}, all other input pins=0V−V_{CC}			10	μA	

Note 1 : $\overline{CE_2}$=0V ; all other input pins=V_{CC}
Note 2 : $\overline{CE_2}$=V_{IL} ; all other input pins=V_{IH}

■ AC Characteristics

(1) Read cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	LH5117-15			LH5117-20			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{RC}	150			200			ns
Access time	t_{ACC}			150			200	ns
Chip enable time	t_{CE}			150			200	ns
Chip select time	t_{CS}	15			20			ns
Output enable time	t_{OE}			75			100	ns
Output select time	t_{OS}	15			20			ns
Output turn-off time (from $\overline{CE_2}$)	t_{DF1}	0		40	0		60	ns
Output turn-off time (from $\overline{CE_1}$)	t_{DF2}	0		40	0		60	ns
Data hold time	t_{OH}	15			20			ns

(2) Write cycle

(V_{CC}=5V±10%, Ta=0～70℃)

Parameter	Symbol	LH5117-15			LH5117-20			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{WC}	150			200			ns
Chip select time	t_{CW}	110			135			ns
Access time	t_{AW}	110			135			ns
Address setup time	t_{AS}	0			5			ns
Pulse width	t_{WP}	110			140			ns
Recovery time	t_{WR}	20			35			ns
Output turn-off time (from $\overline{WE}$)	t_{DF}			40			60	ns
Data setup time	t_{DW}	70			80			ns
Data hold time	t_{DH}	10			10			ns
Output turn-off hold time (from $\overline{WE}$)	t_{OW}	15			20			ns

Conditions for measurement of AC characteristics

- Input voltage frequency width ..... +0.8～+2.2V
- Input signal rise/fall time 10ns
- Time measurement level 1.5V
- Output load conditions ..... 1TTL+100pF

■ Low Supply Voltage Data Hold Characteristics

(V_{CC}=5V±10%, Ta=0～70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data hold supply voltage	V_{CCDR}	$V_{\overline{CE2}}=V_{CC}$, $V_{IN}=0V$ or V_{CC}	2.0			V
Data hold supply voltage	I_{CCDR}	$V_{CC}=V_{\overline{CE2}}=2.0V$, $V_{IN}=0V$ or V_{CC}			10	μA
$\overline{CS}$ setup time	t_{SDR}		t_{RC}			ns
$\overline{CS}$ hold time	t_{RDR}		t_{RC}			ns

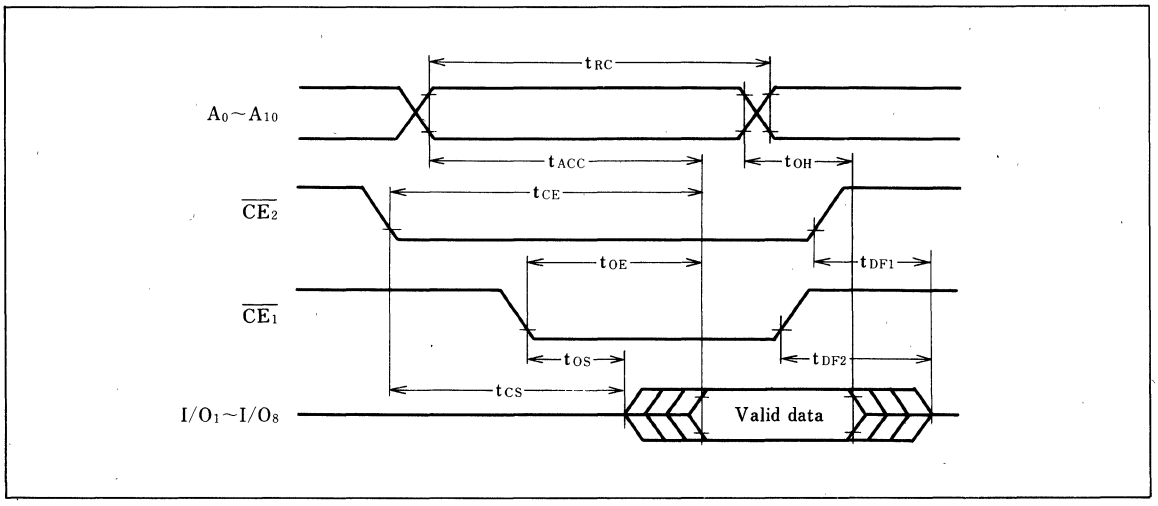
■ Capacitance

(f=1MHz, Ta=25℃)

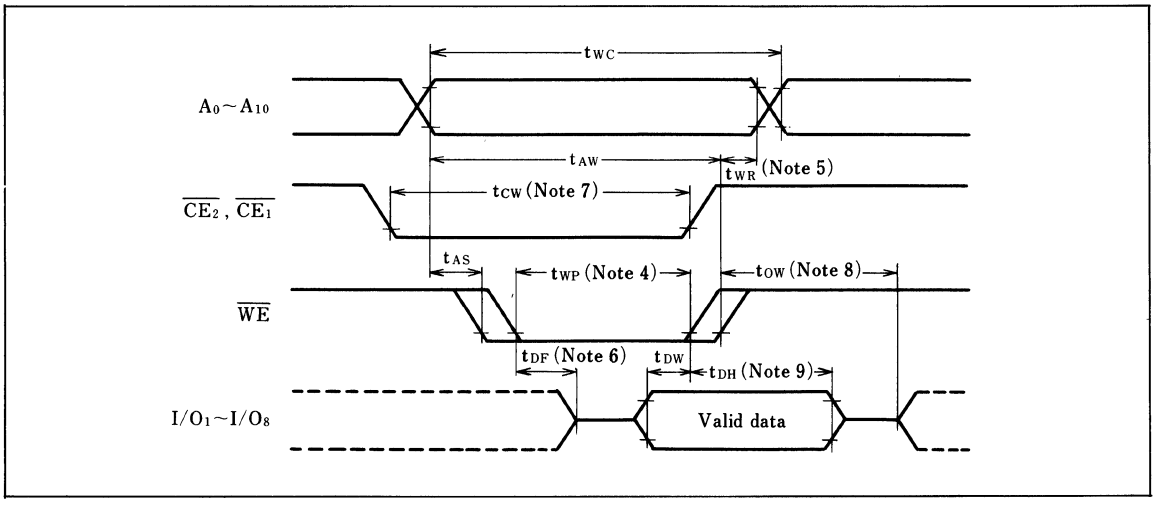
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN}=0V$			5	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}=0V$			8	pF

■ Timing Diagram

(1) Read cycle



(2) Write cycle (Note 3)



Note 3 : $\overline{WE}$ must be high when there is a change in A_0–A_{10}.

Note 4 : When $\overline{CE_2}$, $\overline{CE_1}$, and $\overline{WE}$ are all low at the same time, write occurs during the period t_{WP}.

Note 5 : t_{WR} is the time from the rise of $\overline{CE_2}$ and $\overline{CE_1}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.

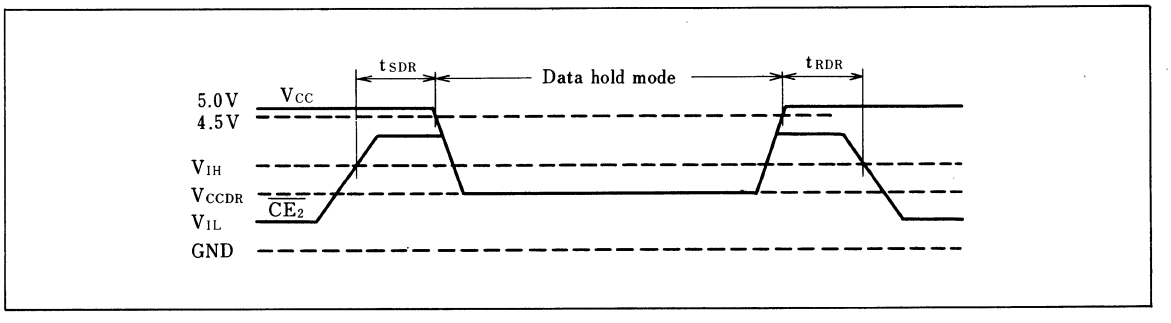
Note 6 : During this period the input/output pin is in an output condition, so input with a phase reversed from that of the output is not permitted.

Note 7 : If $\overline{CE_2}$ or $\overline{CE_1}$ should drop at the same time as $\overline{WE}$ or later, the output buffer is maintained at high impedance.

Note 8 : D_{OUT} outputs data with the same phase as the input data of this write cycle.

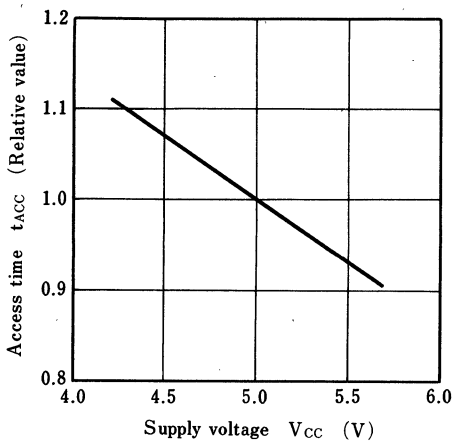
Note 9 : If both $\overline{CE_1}$ and $\overline{CE_2}$ are low during this period, the input/output pin is in the output condition.

(3) Low supply voltage data hold

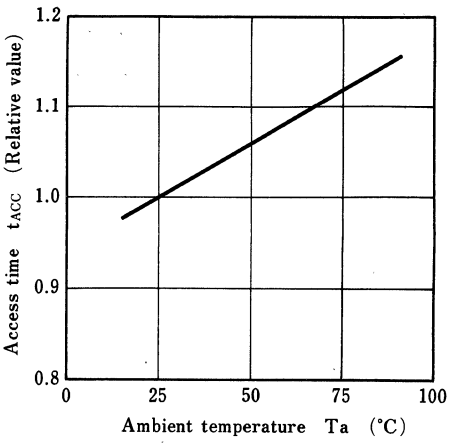


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

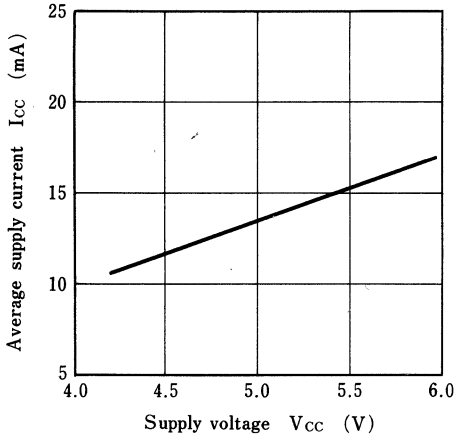
Access time vs. supply voltage



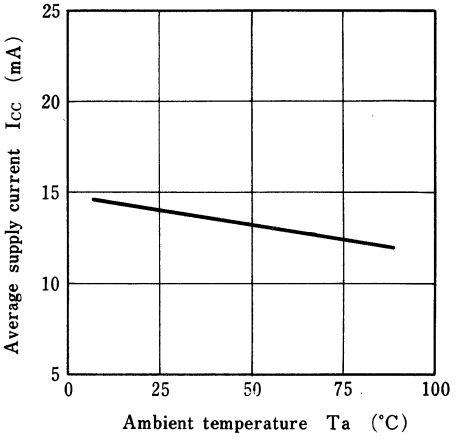
Access time vs. ambient temperature



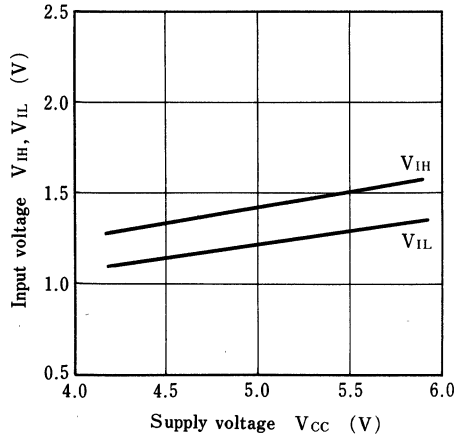
Average supply current 1 vs. supply voltage



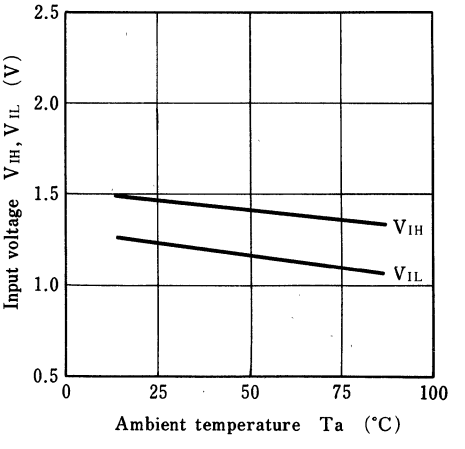
Average supply current 1 vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



LH5118-15/LH5118-20

CMOS 16384-Bit Static Random Access Memory

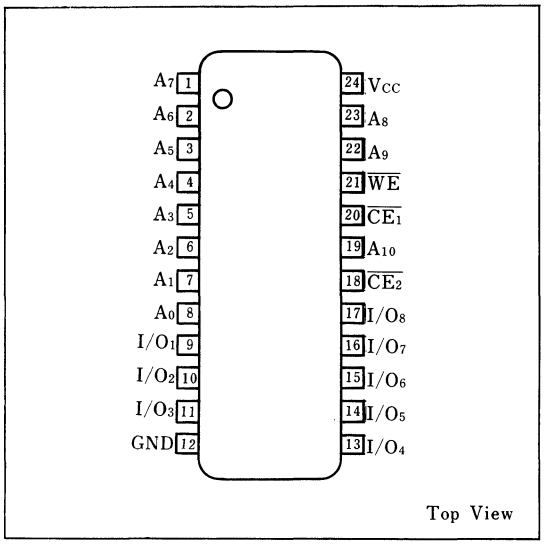
■ Description

The LH5118-15/LH5118-20 are fully static RAMs organized as 2,048-word-by-8-bit by using silicon-gate CMOS process technology.

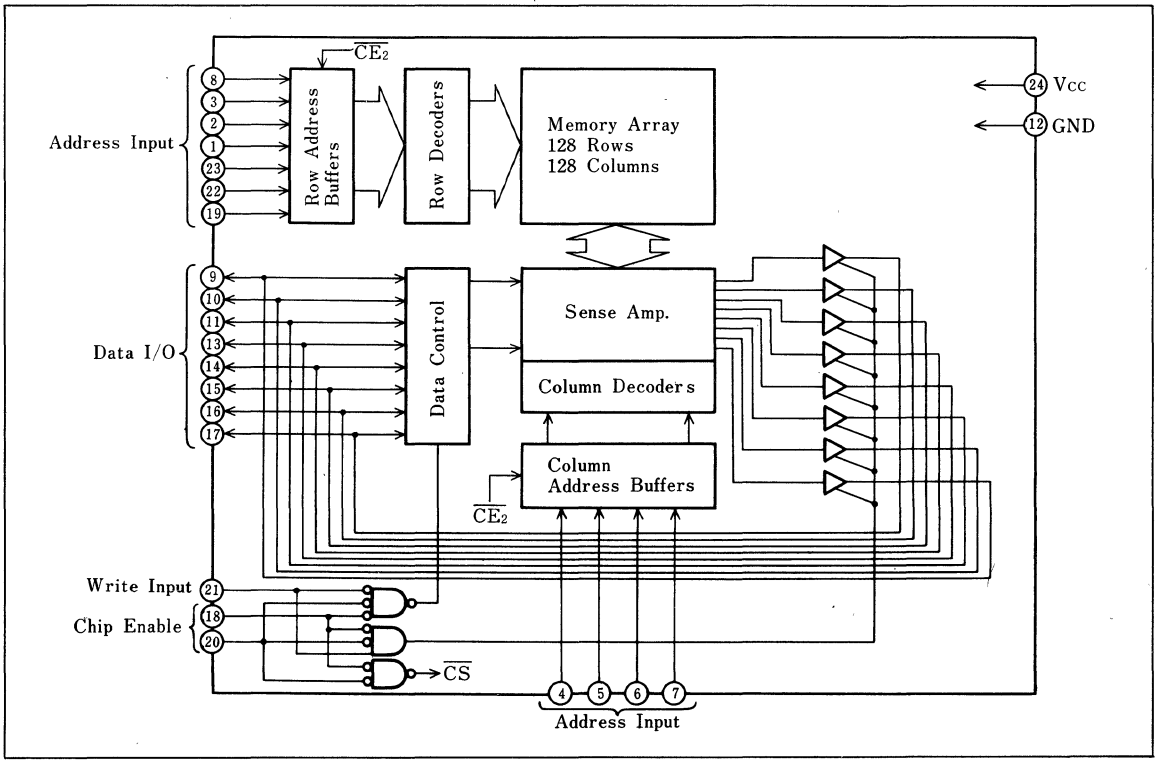
■ Features

1. 2,048-word-by-8-bit organization
2. Single +5V power supply
3. Fully static operation
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.)
   LH5118-15 : 150ns, LH5118-20 : 200ns
7. Supply current at standby mode 10 μA (MAX.) on +2V supply voltage
8. 24-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	−0.3～+7.0	V
Input voltage	V_{IN}	−0.3～V_{CC}+0.3	V
Operating temperature	T_{opr}	0～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{IL}		−0.3		0.8	V	
Input high voltage	V_{IH}		2.2		V_{CC}+0.3	V	
Output low voltage	V_{OL}	I_{CL}=2.1mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V～V_{CC}			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_2}$=V_{IH} or $\overline{CE_1}$=V_{IH}, $V_{I/O}$=0V～V_{CC}			1.0	μA	
Current consumption	I_{CC1}	$I_{I/O}$=0mA ($\overline{WE}$=V_{CC})		15	30	mA	1
	I_{CC2}	$I_{I/O}$=0mA ($\overline{WE}$=V_{IL})		25	40	mA	2
Current consumption during standby	I_{CCL}	$\overline{CE_2}$ and $\overline{CE_1}$=V_{CC}, all other input pins=0V−V_{CC}			10	μA	

Note 1: $\overline{CE_2}$=$\overline{CE_1}$=0V ; all other pins=V_{CC}
Note 2: $\overline{CE_2}$=$\overline{CE_1}$=V_{IL} ; all other pins=V_{IH}

■ AC Characteristics

(1) Read cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	LH5118-15			LH5118-20			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{RC}	150			200			ns
Access time	t_{ACC}			150			200	ns
Chip enable time	t_{CE}			150			200	ns
Chip select time	t_{CS}	15			20			ns
Output enable time	t_{OE}			150			200	ns
Output select time	t_{OS}	15			20			ns
Output turn-off time (from $\overline{CE_2}$)	t_{DF1}	0		40	0		60	ns
Output turn-off time (from $\overline{CE_1}$)	t_{DF2}	0		40	0		60	ns
Data hold time(from address)	t_{OH}	15			20			ns

(2) Write cycle

(V_{CC}=5V±10%, Ta=0～70℃)

Parameter	Symbol	LH5118-15			LH5118-20			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{WC}	150			200			ns
Chip select time	t_{CW}	110			135			ns
Access time	t_{AW}	110			135			ns
Address setup time	t_{AS}	0			5			ns
Pulse width	t_{WP}	110			140			ns
Recovery time	t_{WR}	20			35			ns
Output turn-off time (from $\overline{WE}$)	t			40			60	ns
Data setup time	t_{DW}	70			80			ns
Data hold time	t_{DH}	10			10			ns
Output turn-off hold time (from $\overline{WE}$)	t_{OW}	15			20			ns

Conditions for measurement of AC characteristics

- Input voltage amplitude ····· +0.8～+2.2V
- Input signal rise/fall time ····· 10ns
- Time measurement level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Low Supply Voltage Data Hold Characteristics

(V_{CC}=5V±10%, Ta=0～70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data hold supply voltage	V_{CCDR}	$V_{\overline{CE2}}=V_{CC}$, $V_{IN}=0V$ or V_{CC}	2.0			V
Data hold supply current	I_{CCDR}	$V_{CC}=V_{\overline{CE2}}=2.0V$, $V_{IN}=0V$ or V_{CC}			10	μA
$\overline{CS}$ setup time	t_{SDR}		t_{RC}			ns
$\overline{CS}$ hold time	t_{RDR}		t_{RC}			ns

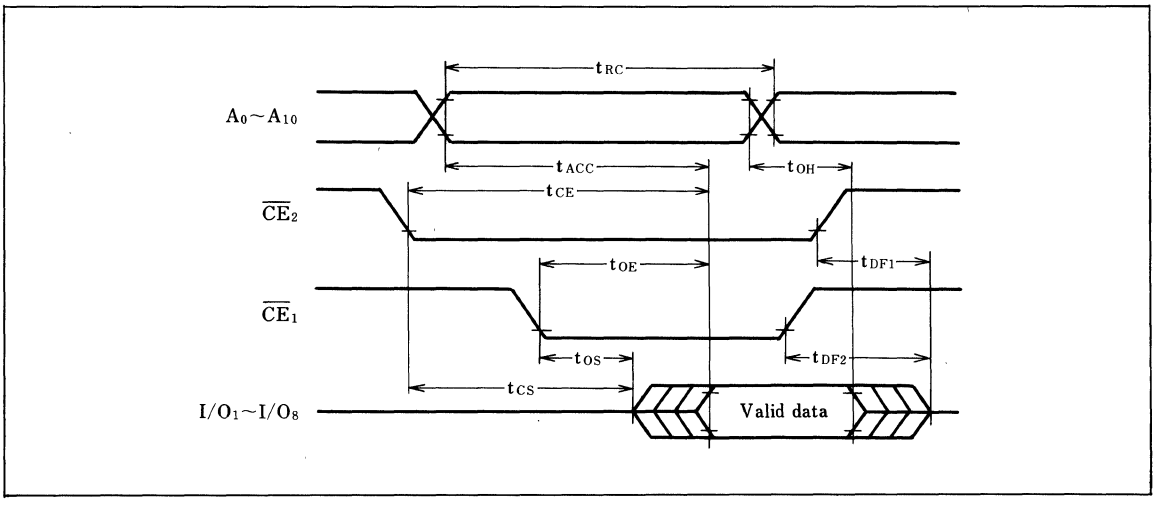
■ Capacitance

(f=1MHz, Ta=25℃)

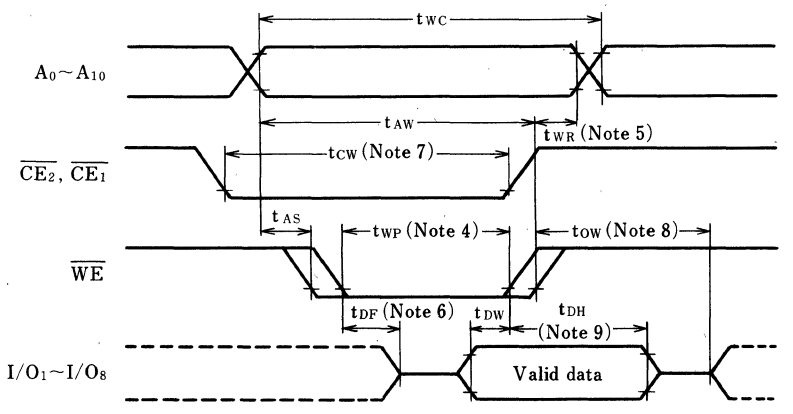
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN}=0V$			5	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}=0V$			8	pF

■ Timing Diagram

(1) Read cycle



(2) Write cycle (Note 3)



Note 3 : $\overline{WE}$ must be high when there is a change in A_0–A_{10}.

Note 4 : When $\overline{CE_2}$, $\overline{CE_1}$, and $\overline{WE}$ are all low at the same time, write occurs during the period t_{WP}.

Note 5 : t_{WR} is the time from the rise of $\overline{CE_2}$ and $\overline{CE_1}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.

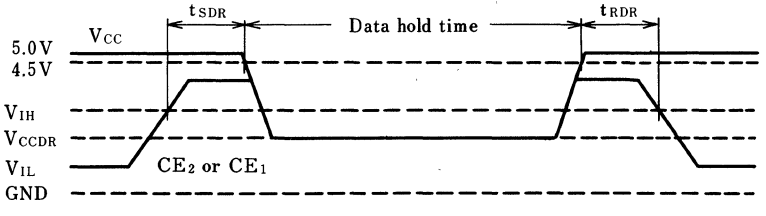
Note 6 : During this period, the input/output pin is in an output condition, so input with a phase reversed from that of the output is not permitted.

Note 7 : If $\overline{CE_2}$ or $\overline{CE_1}$ should drop at the same time as $\overline{WE}$ or later, the output buffer is maintained at high impedance.

Note 8 : D_{OUT} outputs data with the same phase as the input data of this write cycle.

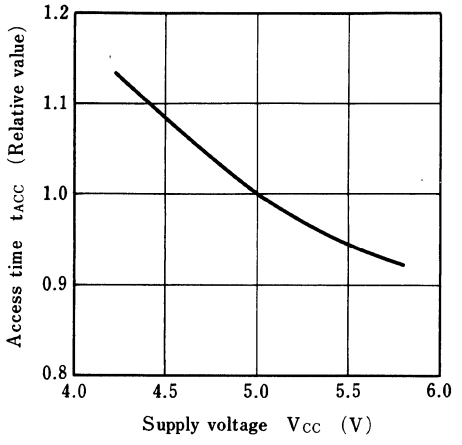
Note 9 : If both $\overline{CE_1}$ and $\overline{CE_2}$ are low during this period, the input/output pin is in the output condition. During this condition, a data input signal with a phase opposite that of the output is not permitted.

(3) Low supply voltage data hold

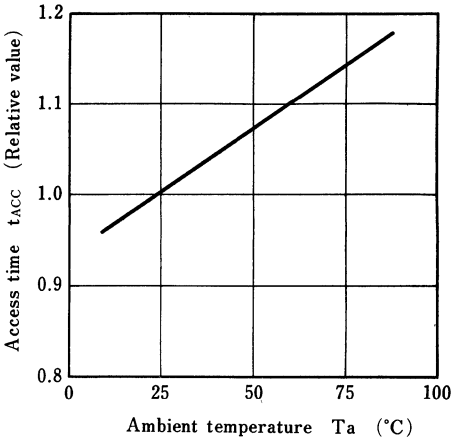


Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

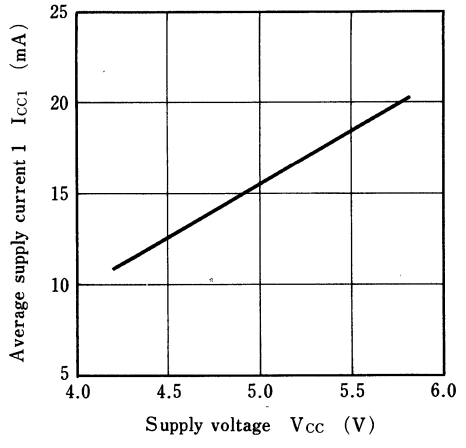
Access time vs. supply voltage



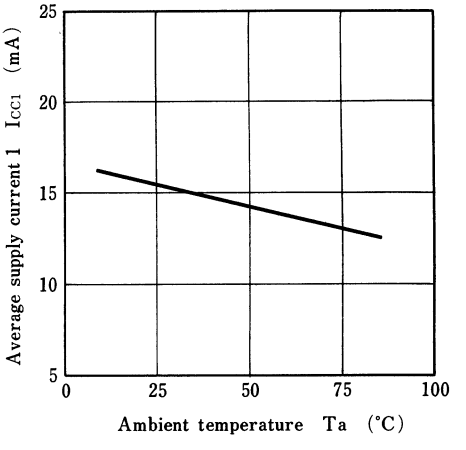
Access time vs. ambient temperature



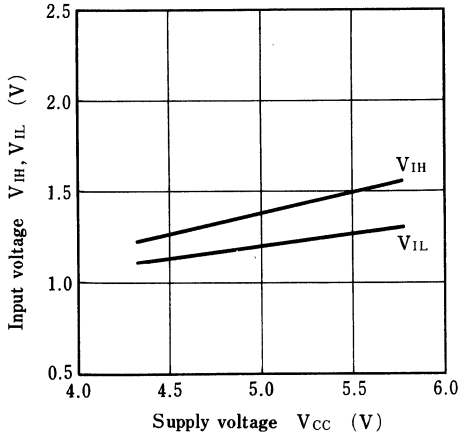
Average supply current 1 vs. supply voltage



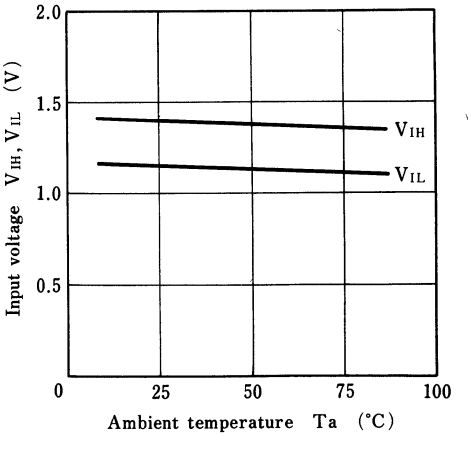
Average supply current 1 vs. ambient temperature



Input voltage vs. supply voltage



Input voltage vs. ambient temperature



8

LH2164-15/LH2164-20

NMOS 65536-Bit Dynamic Random Access Memory

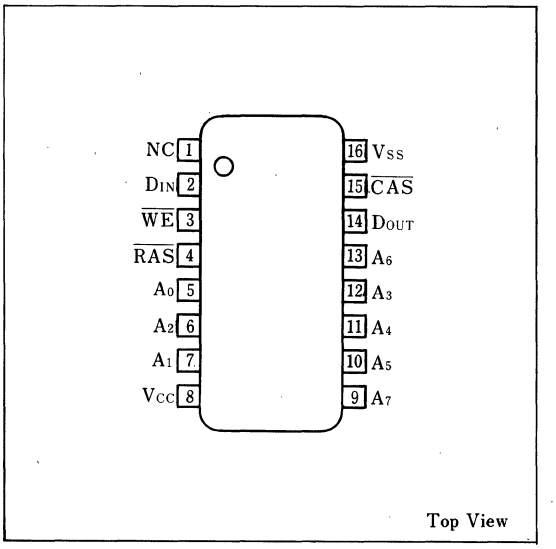
■ Description

The LH2164 is a dynamic RAM organized as 65,536-word-by-1-bit by using high-performance depletion load, n-channel double-poly silicon-gate MOS technology.

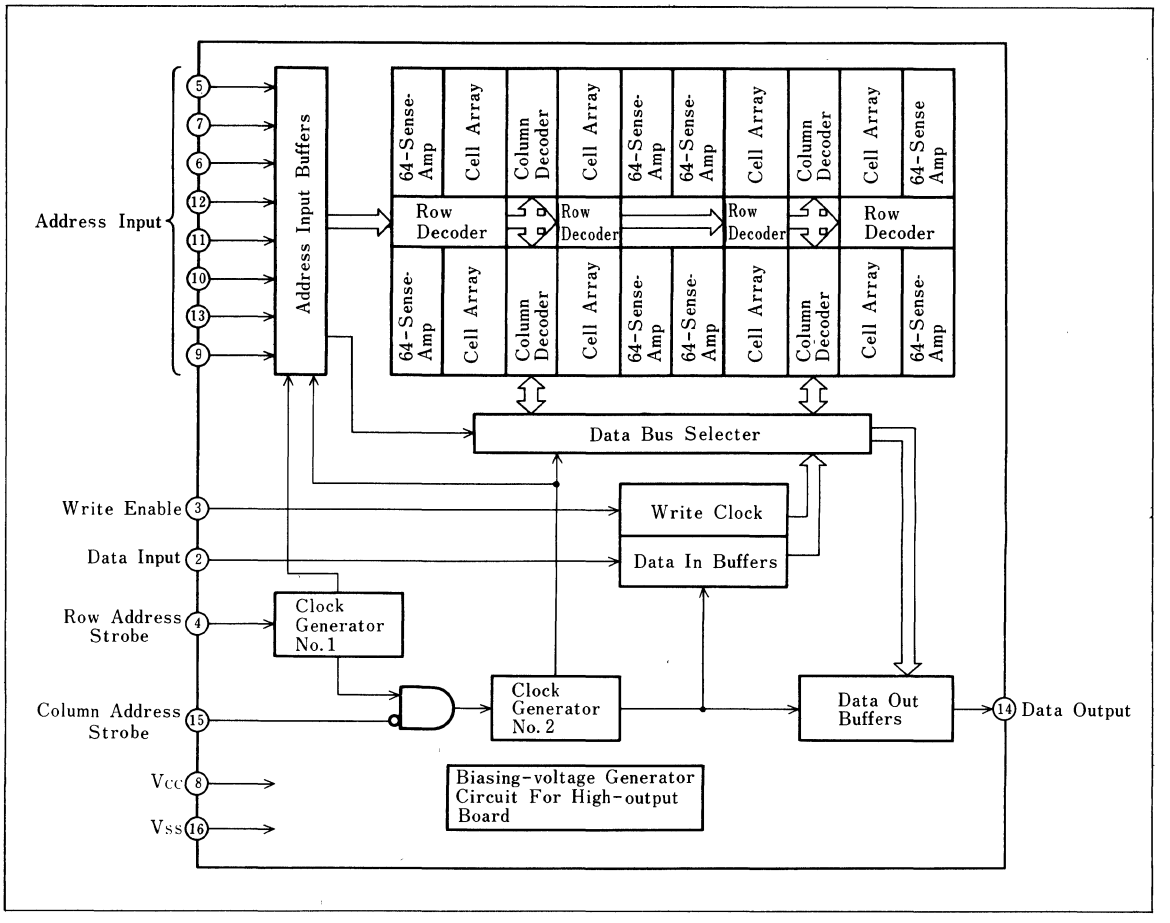
■ Features

1. 65,536-word-by-1-bit organization
2. Access time (MAX.)
   LH2164-15 : 150ns, LH2164-20 : 200ns
3. Cycle time (MIN.)
   LH2164-15 : 270ns, LH2164-20 : 330ns
4. Power supply : +5V±10%
5. Power dissipation (MAX.) : 248mW(operation)
   : 28mW(standby)
6. All inputs and outputs TTL compatible
7. Address and input date latch capability.
8. Three-state outputs date controlled by $\overline{CAS}$ and not latched at the end of cycle
9. Common I/O capability using the early-write mode
10. Read/modify/write, page-mode, $\overline{RAS}$-only refresh, and hidden refresh capabilities
11. Built-in gated $\overline{CAS}$ function
12. Built-in biasing-voltage generator circuit for high-output board
13. 2 ms refresh period, 128 cycle refresh
14. 16-pin dual-in-line package

■ Pin Connections



Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Input voltage	V_{IN}	−1.0～+7.0	V	1
Output voltage	V_{OUT}	−1.0～+7.0	V	1
Supply voltage	V_{CC}	−1.0～+7.0	V	1
Output short-circuit current	I_{OS}	50	mA	
Current consumption	P_D	1.0	W	
Operating temperature	T_{opr}	0～+70	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note 1 : Referenced to V_{SS}.

Recommended Operating Conditions (Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0		
Input voltage	V_{IH}	2.4		6.5	V	2
	V_{IL}	−2.0		0.8		

Note 2 : Referenced to V_{SS}.

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Average supply current during normal operation	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$=cycling t_{RC}=MIN.			45	mA	3,4
Average supply current in standby mode	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$=V_{IH}			5	mA	3
Average supply current during $\overline{RAS}$ only refresh	I_{CC3}	$\overline{RAS}$=cycling, $\overline{CAS}$=V_{IH} t_{RC}=MIN.			35	mA	3,4
Average supply current in page mode	I_{CC4}	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=cycling t_{PC}=MIN.			35	mA	3,4
Input leakage current	$\lvert I_{IL} \rvert$	0V≦V_{IN}≦6.5V Pins other than that being measured are 0V			10	μA	3,4
Output leakage current	$\lvert I_{OL} \rvert$	0V≦V_{OUT}≦6.5V			10	μA	3
Output high voltage	V_{OH}	I_{OUT}=−5mA	2.4			V	
Output low voltage	V_{OL}	I_{OUT}=4.2mA			0.4	V	

Note 3 : Output pin in high impedance state
Note 4 : I_{CC1}, I_{CC3}, and I_{CC4} depend on cycle time.

■ AC Characteristics (Note 5, 6, 7)

(V_{CC}=5.0V±10%, Ta=0～+70℃)

Parameter	Symbol	LH2164-15		LH2164-20		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{RAS}$ cycle time	t_{RC}	270		330		ns	
Read/write cycle time	t_{RWC}	300		375		ns	
Page mode cycle time	t_{PC}	170		225		ns	
Access time from $\overline{RAS}$	t_{RAC}		150		200	ns	8,10
Access time from $\overline{CAS}$	t_{CAC}		100		135	ns	9,10
Output turn off delay	t_{OFF}	0	40	0	50	ns	
Rise/fall time	t_T	3	35	3	50	ns	7
$\overline{RAS}$ precharge time	t_{RP}	100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	100		135		ns	
$\overline{CAS}$ precharge time	t_{CP}	60		80		ns	
$\overline{CAS}$ pulse width (page mode)	t_{CAS}	100	10,000	135	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	150		200		ns	
$\overline{RAS}$/$\overline{CAS}$ delay	t_{RCD}	25	50	30	65	ns	11,12
$\overline{CAS}$/$\overline{RAS}$ precharge time	t_{CRP}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	20		25		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	45		55		ns	
Column address hold time from $\overline{RAS}$	t_{AR}	95		120		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time	t_{RCH}	0		0		ns	15
Write command setup time	t_{WCS}	−10		−10		ns	14
Write command hold time	t_{WCH}	45		55		ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	95		120		ns	
Write command pulse width	t_{WP}	45		55		ns	
Write command/$\overline{RAS}$ read time	t_{RWL}	60		80		ns	
Write command/$\overline{CAS}$ read time	t_{CWL}	60		80		ns	
Data input setup time	t_{DS}	0		0		ns	13
Data input hold time	t_{DH}	45		55		ns	13

Parameter	Symbol	LH2164-15		LH2164-20		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Data input hold time from $\overline{RAS}$	t_{DHR}	95		120		ns	
$\overline{CAS}$/write command delay	t_{CWD}	70		95		ns	14
$\overline{RAS}$/write command delay	t_{RWD}	120		160		ns	14
Read command hold time from $\overline{RAS}$	t_{RRH}	20		25		ns	15
$\overline{CAS}$ precharge time	t_{CPN}	25		30		ns	
Refresh time	t_{REF}		2		2	ms	

Note 5: For the memory to operate normally, a minimum pause of 500 μs after the power is turned on and then several dummy cycles are necessary. Generally, eight normal refresh cycles should be performed.
Note 6: Measure AC characteristics when t_T=5 ns.
Note 7: The prescribed input reference levels for timing are $V_{IH(min)}$ and $V_{IL(max)}$. Transition time (t_T) is the time between V_{IH} and V_{IL}.
Note 8: When $t_{RCD} \leqq t_{RCD(max)}$. When $t_{RCD} < t_{RCD(max)}$, t_{RAC} becomes large by ($t_{RCD} - t_{RCD(max)}$).
Note 9: When $t_{RCD} = t_{RCD(max)}$.
Note 10: Load condition for 2TTL+100pF.
Note 11: $t_{RCD(max)}$ is the largest value of t_{RCD} that protects $t_{RAC(max)}$ and is not an operation limit. If $t_{RCD(max)} \leqq t_{RCD}$, the access time is controlled by t_{CAC}.
Note 12: $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$
Note 13: The fall of $\overline{CAS}$ becomes the reference of t_{DS} and t_{DH} in the early write cycle and $\overline{WE}$ becomes the reference in the read/write cycle and in the read/modify/write cycle.
Note 14: t_{WCS}, t_{CWD}, and t_{RWD} are not operation limits at the point the operation mode is prescribed. When $t_{WCS} \geqq t_{WCS(min)}$, the early write cycle begins and the D_{OUT} pin becomes high impedance.
If $t_{RWD} \geqq t_{RWD(min)}$ when $t_{CWD} \geqq t_{CWD(min)}$, the read/write cycle begins and the output data becomes information of the selector cell.
In the case of timing other than that above, output becomes indeterminate.
Note 15: Operation is guaranteed when either t_{RCH} or t_{RRH} is satisfied.

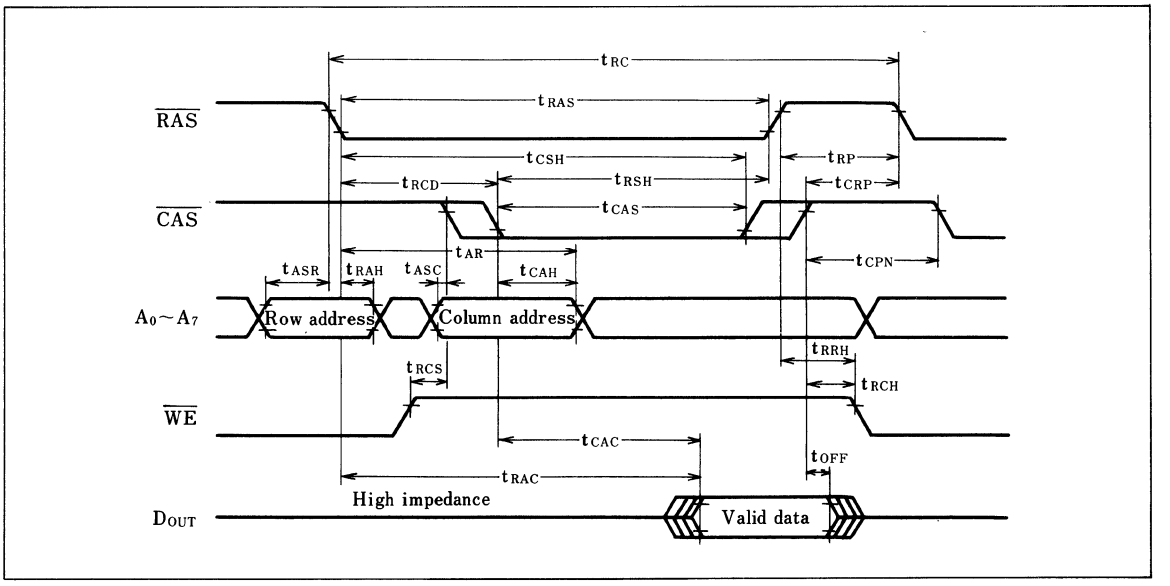
■ Capacitance

(V_{CC}=5V±10%, f=1MHz, Ta=0~70℃)

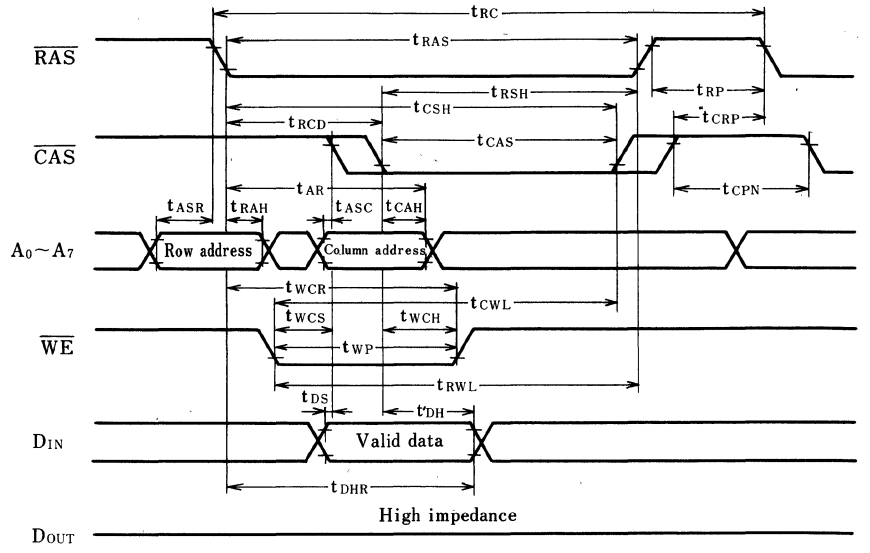
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN1}	A_0~A_7, D_{IN}, $\overline{WE}$			5	pF
Input capacitance	C_{IN2}	$\overline{RAS}$, $\overline{CAS}$			6	pF
Output capacitance	C_{OUT}	D_{OUT}			8	pF

■ Timing Diagram

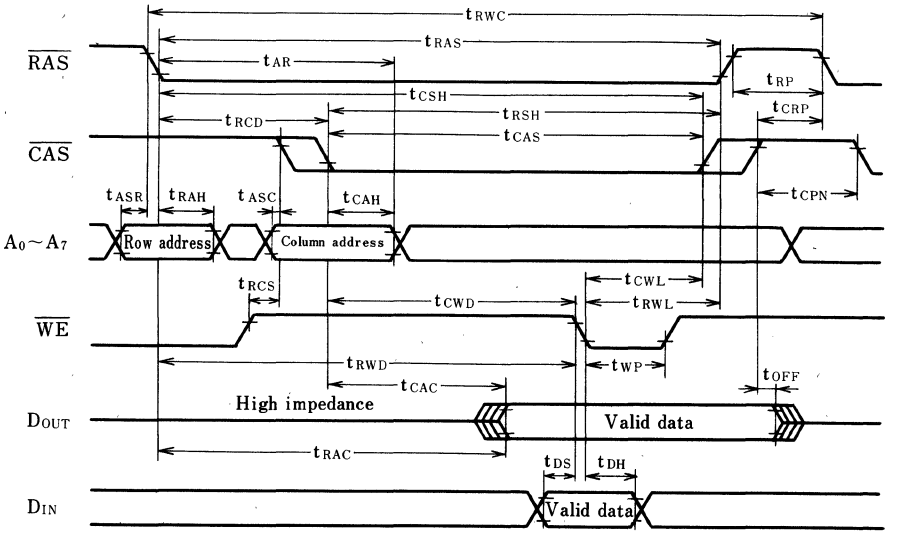
(1) Read cycle



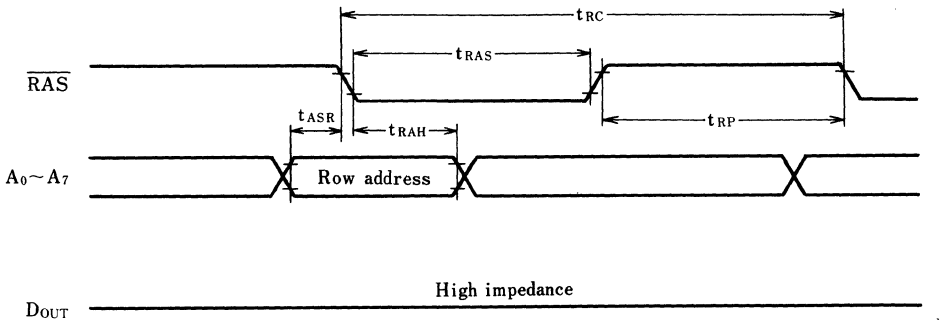
(2) Write cycle (Early write)



(3) Read write and read modify write cycles

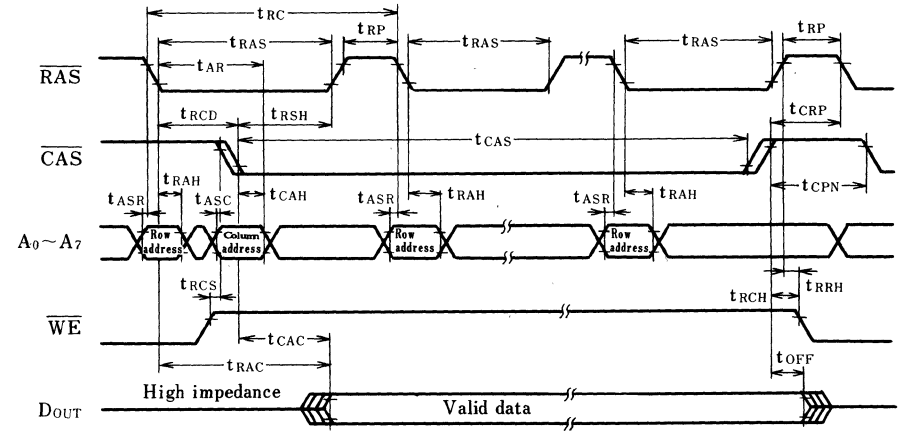


(4) $\overline{RAS}$ only refresh cycle

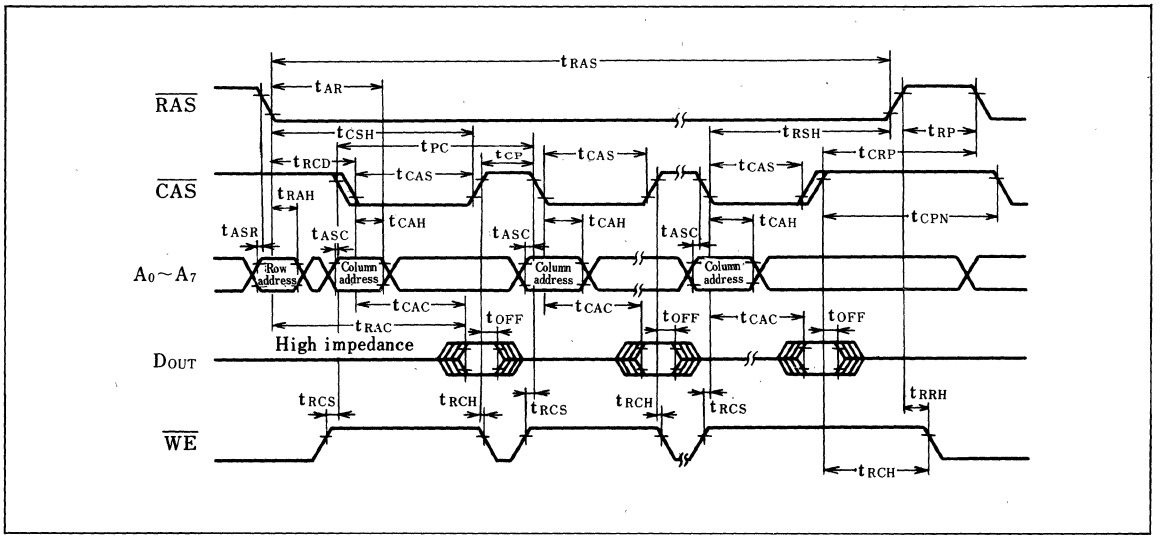


Note : $\overline{CAS}$=VIH

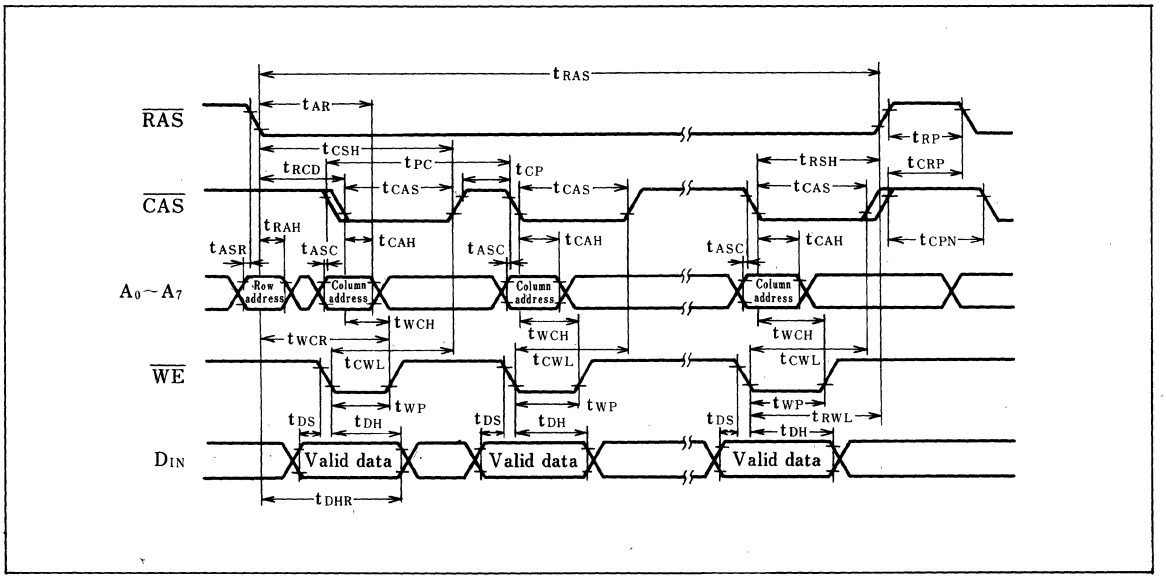
(5) Hidden refresh cycle



(6) Page mode read cycle

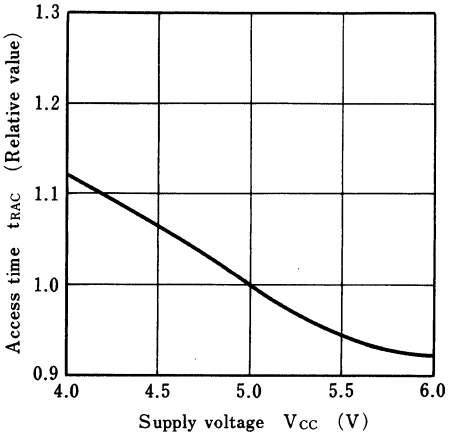


(7) Page mode write cycle

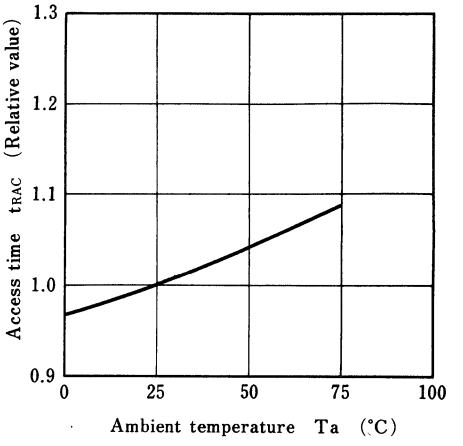


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

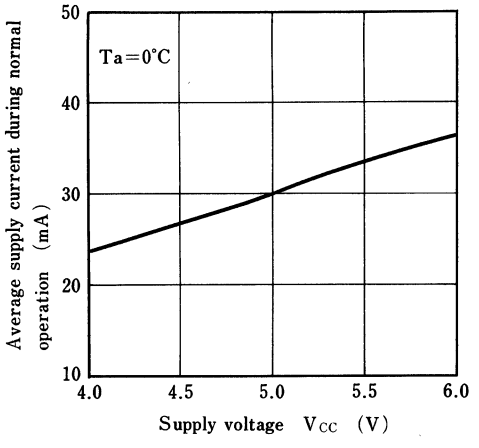
Access time vs. supply voltage



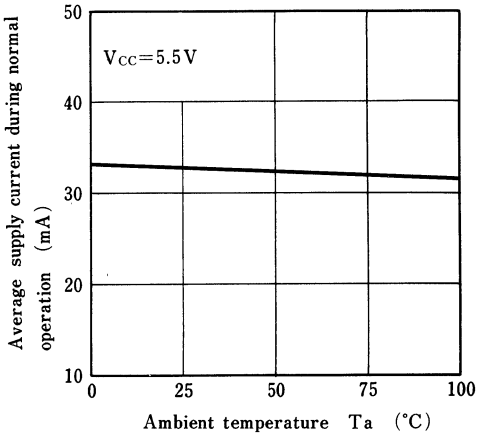
Access time vs. ambient temperature



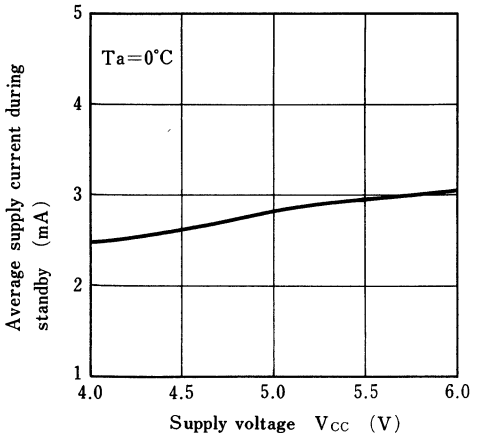
Average supply current during page mode vs. supply voltage



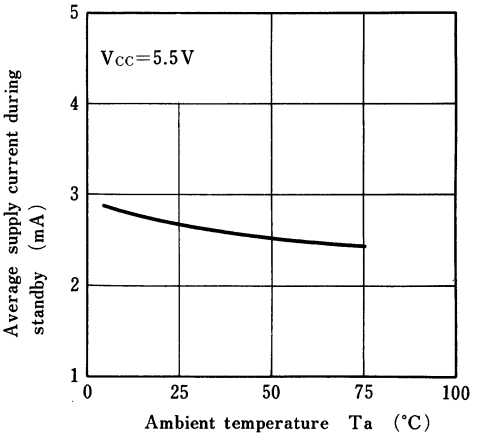
Average supply current during page mode vs. ambient temperature



Average supply current during standby vs. supply voltage



Average supply current during standby vs. ambient temperature



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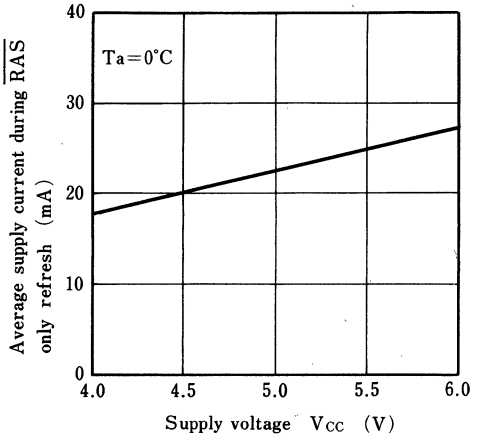
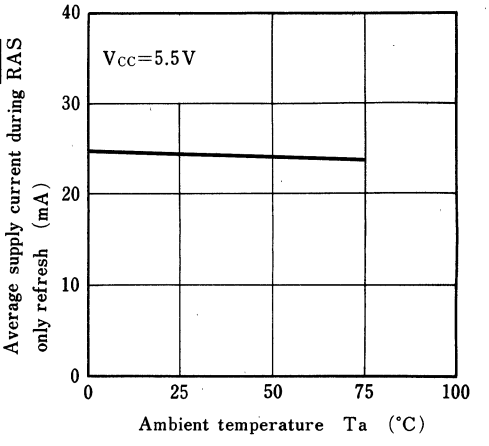
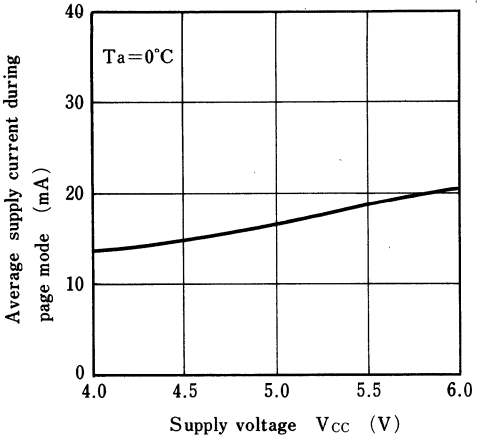
Average supply current during $\overline{RAS}$ only refresh vs. supply voltage



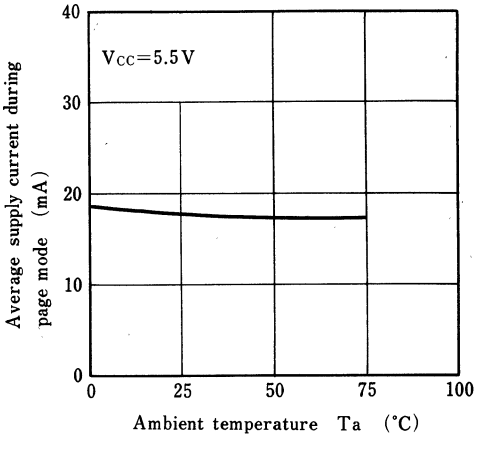
Average supply current during $\overline{RAS}$ only refresh vs. ambient temperature



Average supply current during page mode vs. supply voltage



Average supply current during page mode vs. ambient temperature



LH2164A-15/LH2164A-20

NMOS 65536-Bit Dynamic Random Access Memory

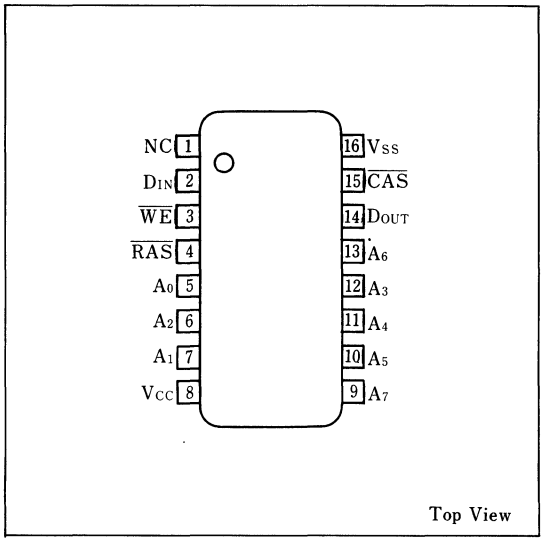
■ Description

The LH2164A is a dynamic RAM organized as 65,536-word-by-1-bit by using high-performance depletion load, n-channel double-poly silicon-gate MOS technology.

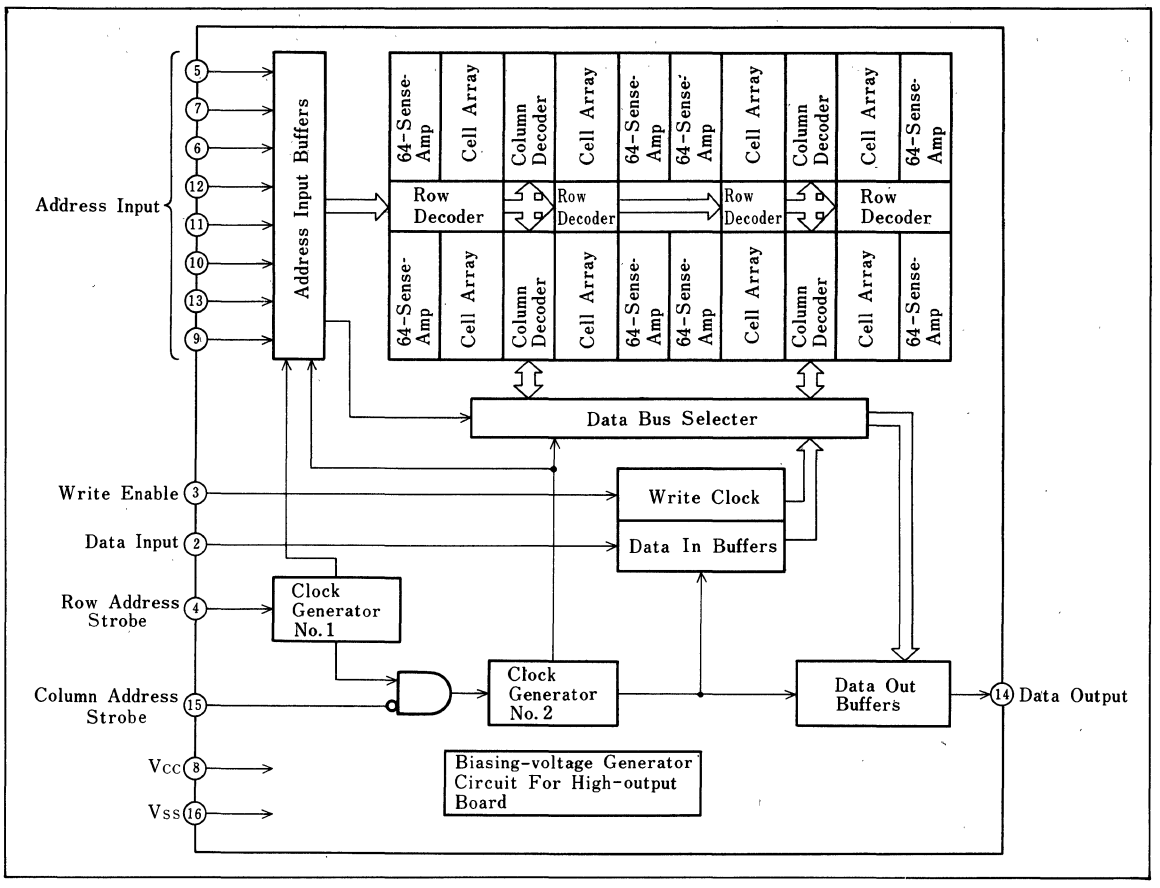
■ Features

1. 65,536-word-by-1-bit organization
2. Access time (MAX.)
   LH2164A-15 : 150ns, LH2164A-20 : 200ns
3. Cycle time (MIN.)
   LH2164A-15 : 260ns, LH2164A-20 : 330ns
4. Power supply : +5V±10%
5. Power consumption (MAX.) : 248mW(operation)
   : 28mW(standby)
6. All inputs and outputs TTL compatible
7. Address and input data latch capability.
8. Three-state output data controlled by $\overline{CAS}$ and not latched at the end of cycle
9. Common I/O capability using the early-write mode
10. Read/modify/write, page-mode, $\overline{RAS}$-only refresh, and hidden refresh capabilities
11. Built-in gated $\overline{CAS}$ function
12. Built-in biasing-voltage generator circuit for high-output board
13. 2 ms refresh period, 128 cycle refresh .
14. 16-pin dual-in-line package

■ Pin Connections



Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Input voltage	V_{IN}	−1.0～+7.0	V	1
Output voltage	V_{OUT}	−1.0～+7.0	V	1
Supply voltage	V_{CC}	−1.0～+7.0	V	1
Output short-circuit current	I_{OS}	50	mA	
Current consumption	P_D	1.0	W	
Operating temperature	T_{opr}	0～+70	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note 1 : Referenced to V_{SS}.

Recommended Operating Conditions (Ta=0～+70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0		
Input voltage	V_{IH}	2.4		6.5	V	2
	V_{IL}	−2.0		0.8		

Note 2 : Referenced to V_{SS}.

DC Characteristics

(V_{CC}=5.0V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Average supply current during normal operation	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$=cycling t_{RC}=MIN.			45	mA	3,4
Average supply current in standby mode	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$=V_{IH}			5	mA	3
Average supply current during $\overline{RAS}$ only refresh	I_{CC3}	$\overline{RAS}$=cycling, $\overline{CAS}$=V_{IH} t_{RC}=MIN.			35	mA	3,4
Average supply current in page mode	I_{CC4}	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=cycling t_{PC}=MIN.			35	mA	3,4
Input leakage current	$\lvert I_{IL} \rvert$	0V≦V_{IN}≦6.5V Pins other than that being measured are 0V			10	μA	3,4
Output leakage current	$\lvert I_{OL} \rvert$	0V≦V_{OUT}≦6.5V			10	μA	3
Output high voltage	V_{OH}	I_{OUT}=−5mA	2.4			V	
Output low voltage	V_{OL}	I_{OUT}=4.2mA			0.4	V	

Note 3 : Output pin in high impedance state
Note 4 : I_{CC1}, I_{CC3}, and I_{CC4} depend on cycle time.

AC Characteristics (Note 5, 6, 7)

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	LH2164A-15		LH2164A-20		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{RAM}$ cycle time	t_{RC}	260		330		ns	
Read/write cycle time	t_{RWC}	285		350		ns	
Page mode cycle time	t_{PC}	145		190		ns	
Access time from $\overline{RAS}$	t_{RAC}		150		200	ns	8,10
Access time from $\overline{CAS}$	t_{CAC}		75		100	ns	9,10
Output turn off delay	t_{OFF}	0	40	0	50	ns	
Rise/fall time	t_T	3	35	3	50	ns	5
$\overline{RAS}$ precharge time	t_{RP}	100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	75		100		ns	
$\overline{CAS}$ precharge time	t_{CP}	60		80		ns	
$\overline{CAS}$ pulse width (page mode)	t_{CAS}	75	10,000	100	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	150		200		ns	
$\overline{RAS}$/$\overline{CAS}$ delay time	t_{RCD}	25	75	30	100	ns	11,12
$\overline{CAS}$/$\overline{RAS}$ precharge time	t_{CRP}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	20		25		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	45		55		ns	
Column address hold time from $\overline{RAS}$	t_{AR}	120		155		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time	t_{RCH}	0		0		ns	15
Write command setup time	t_{WCS}	−5		−5		ns	14
Write command hold time	t_{WCH}	45		55		ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	120		155		ns	
Write command pulse width	t_{WP}	45		55		ns	
Write command/$\overline{RAS}$ read time	t_{RWL}	45		55		ns	

Parameter	Symbol	LH2164A-15		LH2164A-20		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Write command/$\overline{CAS}$ read time	t_{CWL}	45		55		ns	
Data input setup time	t_{DS}	0		0		ns	13
Data input hold time	t_{DH}	45		55		ns	13
Data input hold time from $\overline{RAS}$	t_{DHR}	120		155		ns	
Write command delay time from $\overline{CAS}$	t_{CWD}	50		60		ns	14
Write command delay time from $\overline{RAS}$	t_{RWD}	125		160		ns	14
Read command hold time from $\overline{RAS}$	t_{RRH}	20		25		ns	15
$\overline{CAS}$ precharge time	t_{CPN}	25		30		ns	
Refresh time	t_{REF}		2		2	ms	

Note 5: For the memory to operate normally, a minimum pause of 500 μs after the power is turned on and then several dummy cycles are necessary. Generally, eight normal refresh cycles should be performed.
Note 6: Measure AC characteristics when $t_T=5$ ns.
Note 7: The prescribed input reference levels for timing are $V_{IH(min)}$ and $V_{IL(max)}$. Transition time (t_T) is the time between V_{IH} and V_{IL}.
Note 8: When $t_{RCD} \leqq t_{RCD(max)}$. When $t_{RCD} < t_{RCD(max)}$, t_{RAC} becomes large by ($t_{RCD} - t_{RCD(max)}$).
Note 9: When $t_{RCD}=t_{RCD(max)}$.
Note 10: Load condition for 2TTL+100pF.
Note 11: $t_{RCD(max)}$ is the largest value of t_{RCD} that protects $t_{RAC(max)}$ and is not an operation limit. If $t_{RCD(max)} \leqq t_{RCD}$, the access time is controlled by t_{CAC}.
Note 12: $t_{RCD(min)}=t_{RAH(min)}+2t_T+t_{ASC(min)}$.
Note 13: The fall of $\overline{CAS}$ becomes the reference of t_{DS} and t_{DH} in the early write cycle and $\overline{WE}$ becomes the reference in the read/write cycle and in the read/modify/write cycle.
Note 14: t_{WCS}, t_{CWD}, and t_{RWD} are not operation limits at the point the operation mode is prescribed. When $t_{WCS} \geqq t_{WCS(min)}$, the early write cycle begins and the D_{OUT} pin becomes high impedance.
If $t_{RWD} \geqq t_{RWD(min)}$ when $t_{CWD} \geqq t_{CWD(min)}$, the read/write cycle begins and the output data becomes information of the selector cell.
In the case of timing other than that above, output becomes indeterminate.
Note 15: Operation is guaranteed when either t_{RCH} or t_{RRH} is satisfied.

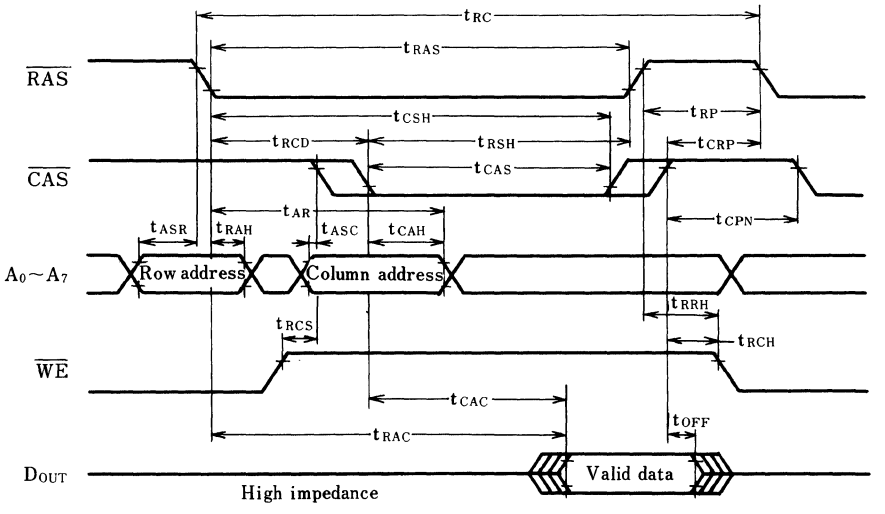
■ Capacitance

($V_{CC}=5V\pm10\%$, f=1MHz, Ta=0~+70℃)

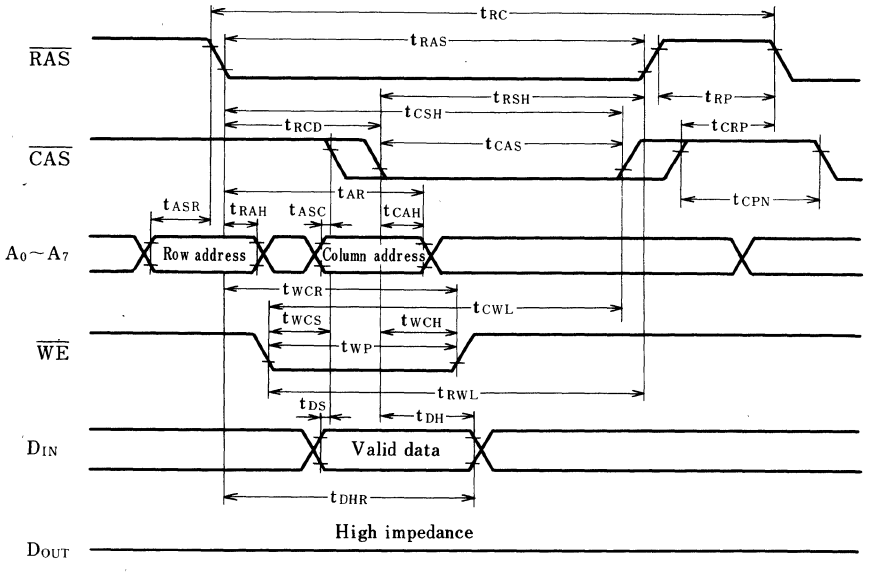
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN1}	$A_0 \sim A_7$, D_{IN}, $\overline{WE}$			5	pF
Input capacitance	C_{IN2}	$\overline{RAS}$, $\overline{CAS}$			6	pF
Output capacitance	C_{OUT}	D_{OUT}			8	pF

■ Timing Diagram

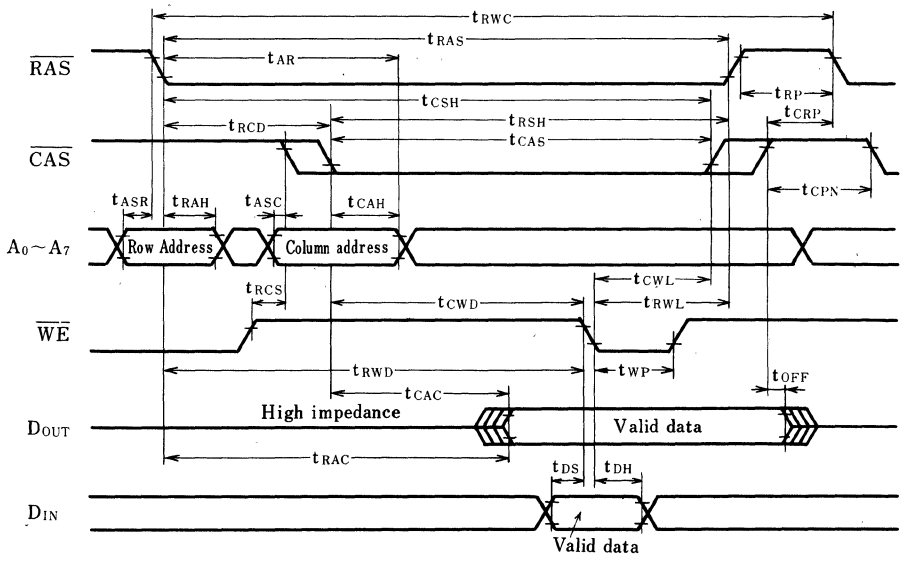
(1) Read cycle



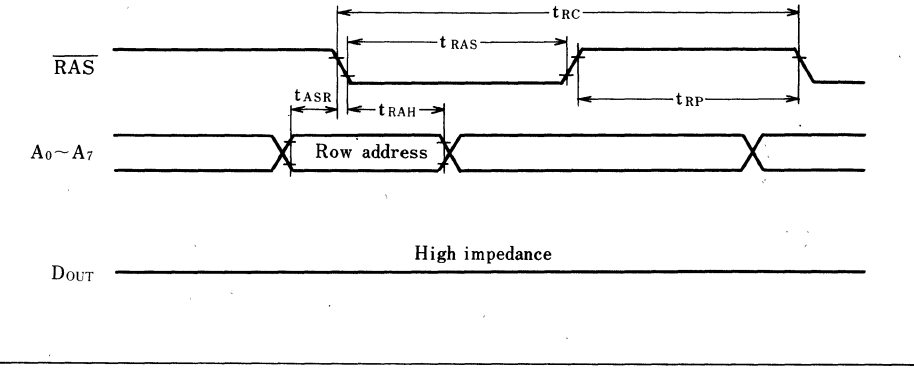
(2) Write cycle (Early write)



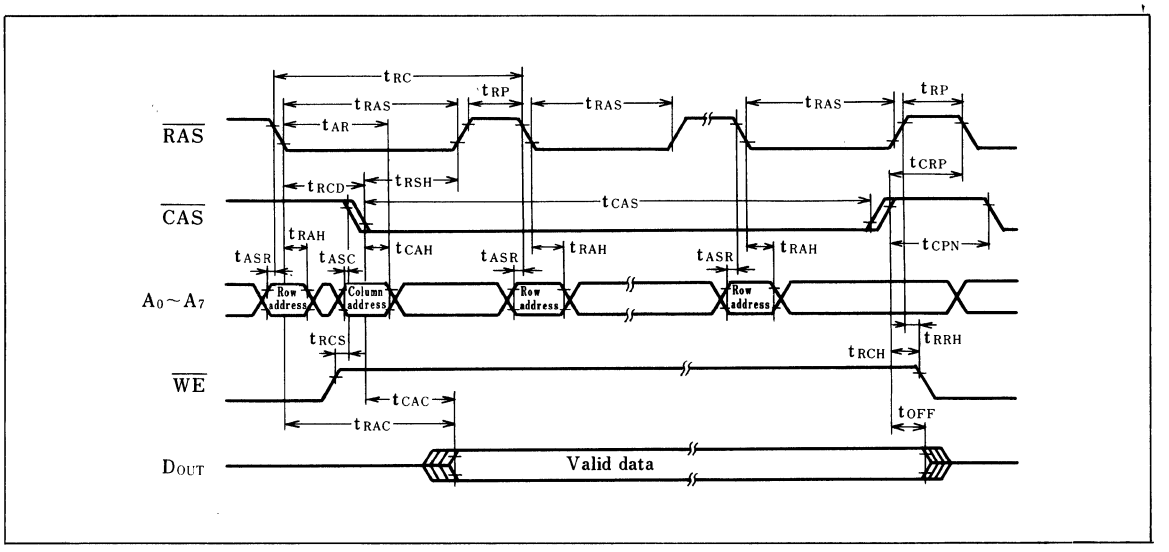
(3) Read/write and read/modify/write cycles



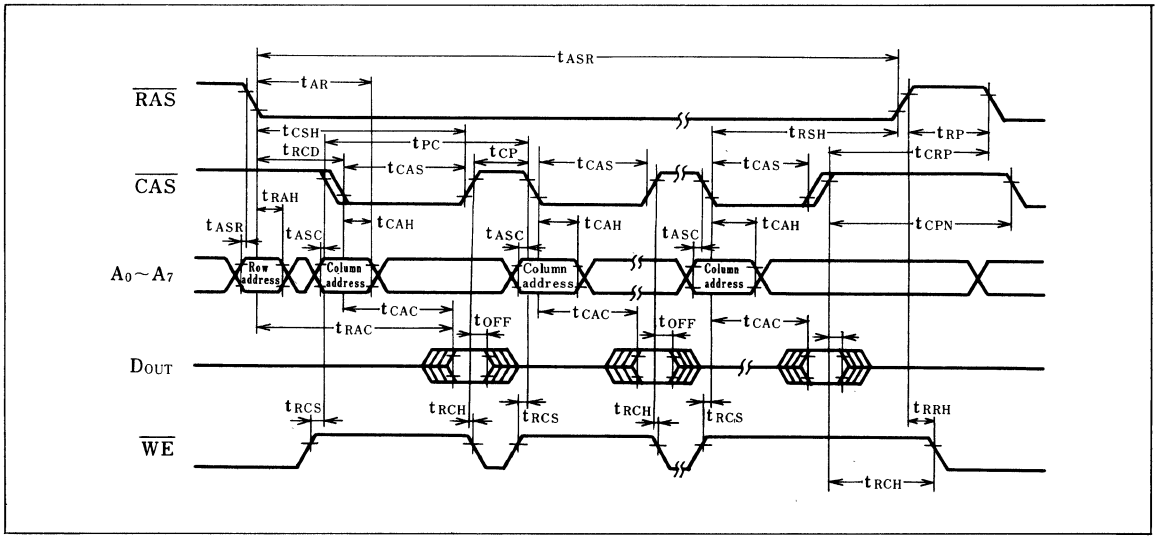
(4) RAS only refresh cycle



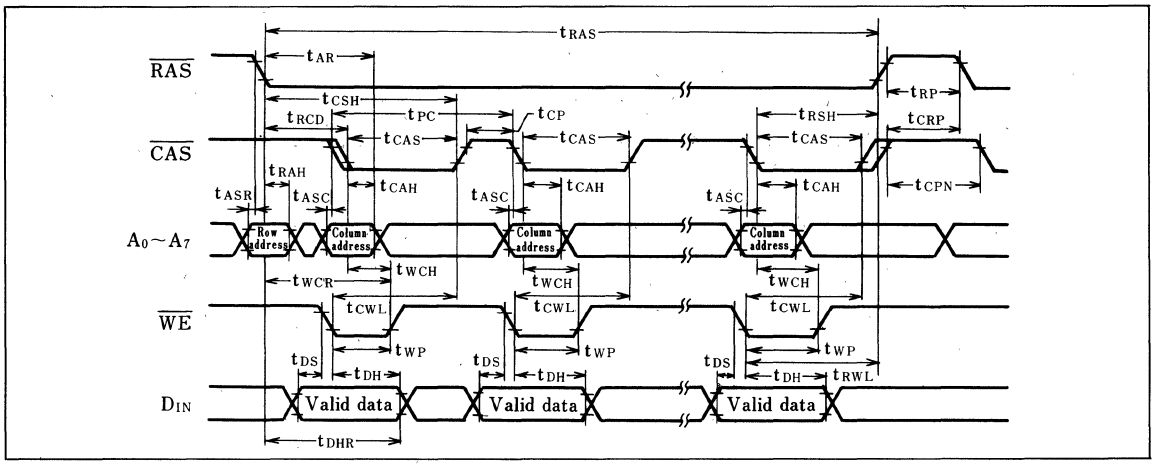
(5) Hidden refresh cycle



(6) Page mode read cycle

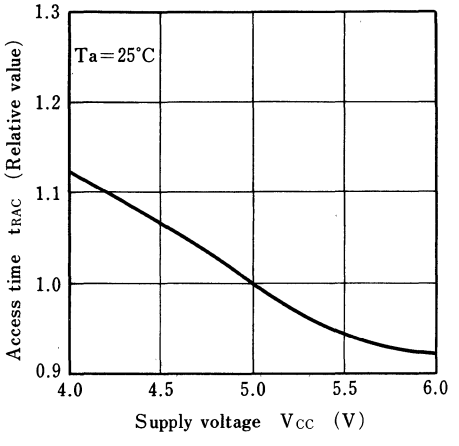


(7) Page mode write cycle

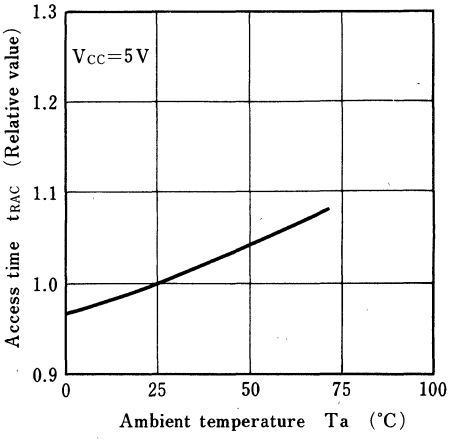


■ Electrical Characteristics Curves

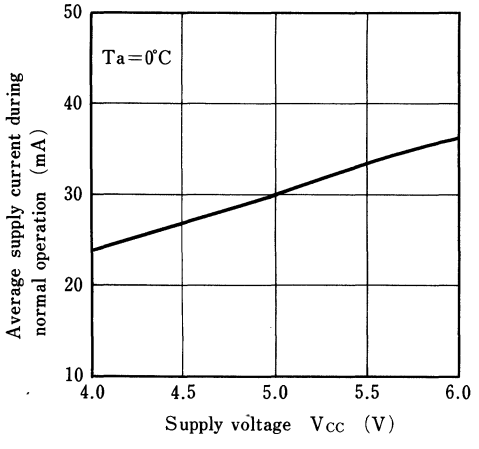
Access time vs. supply voltage



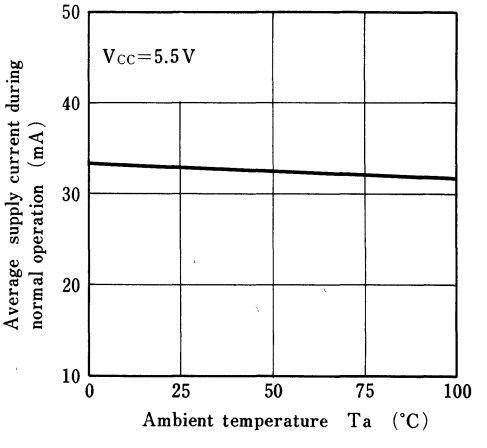
Access time vs. ambient temperature



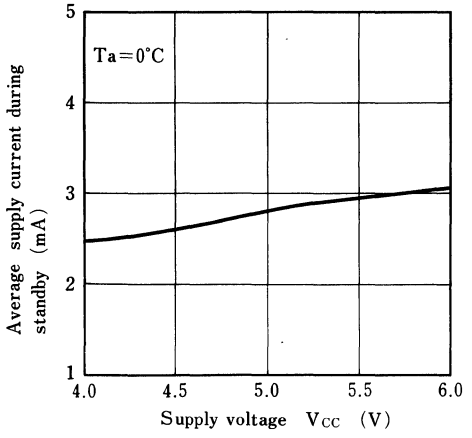
Average supply current during normal operation vs. supply voltage



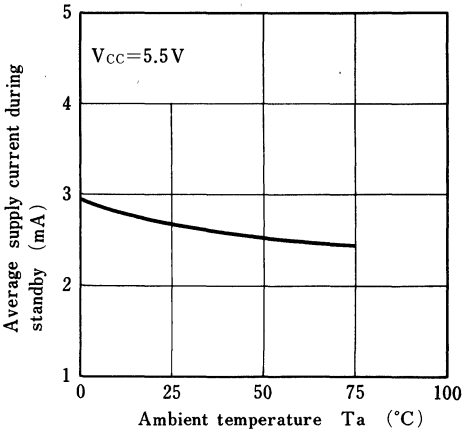
Average supply current during normal operation vs. ambient temperature



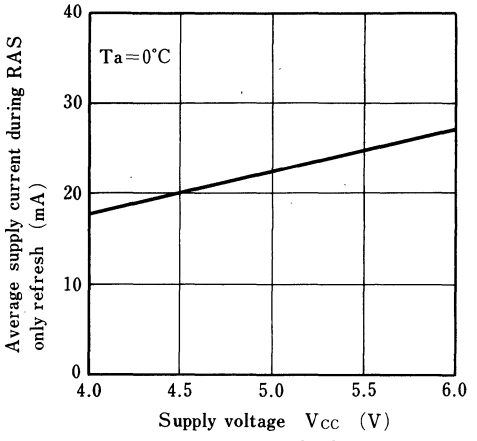
Average supply current during standby vs. supply voltage



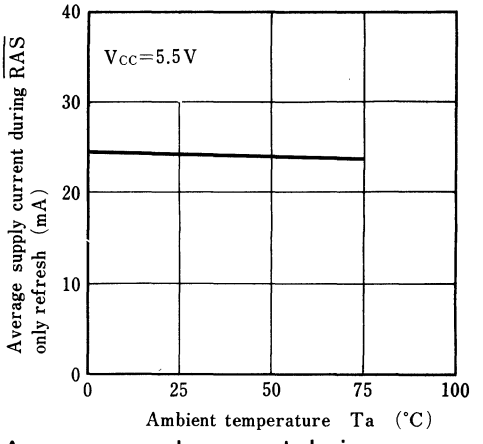
Average supply current during standby vs. ambient temperature



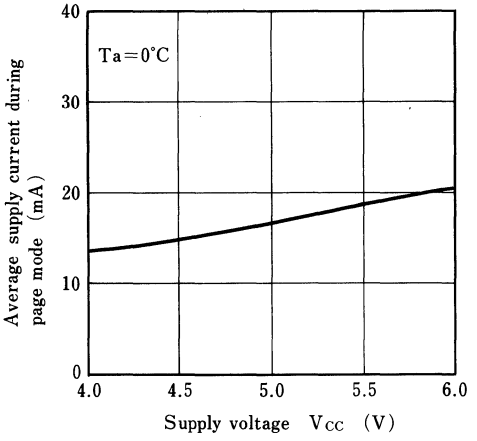
Average supply current during $\overline{RAS}$ only refresh vs. supply voltage



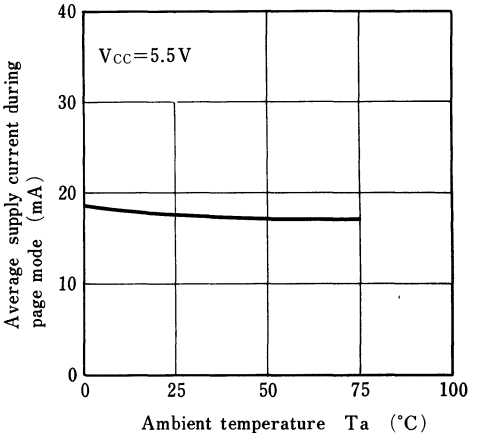
Average supply current during $\overline{RAS}$ only refresh vs. ambient temperature



Average supply current during page mode vs. supply voltage



Average supply current during page mode vs. ambient temperature



8

NEW

LH2464/LH2465 NMOS 262144-Bit Dynamic Random Access Memory

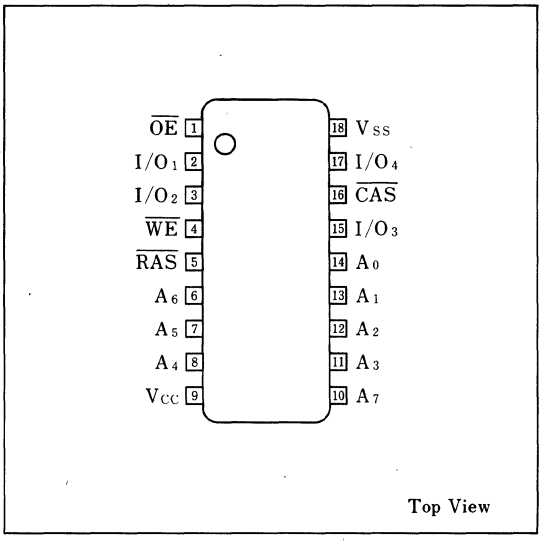
Description

The LH2464/LH2465 are dynamic RAMs organized as 65,536-word-by-4-bit by using high-performance depletion load n-channel double-poly-cide silicon-gate MOS technology.

Features

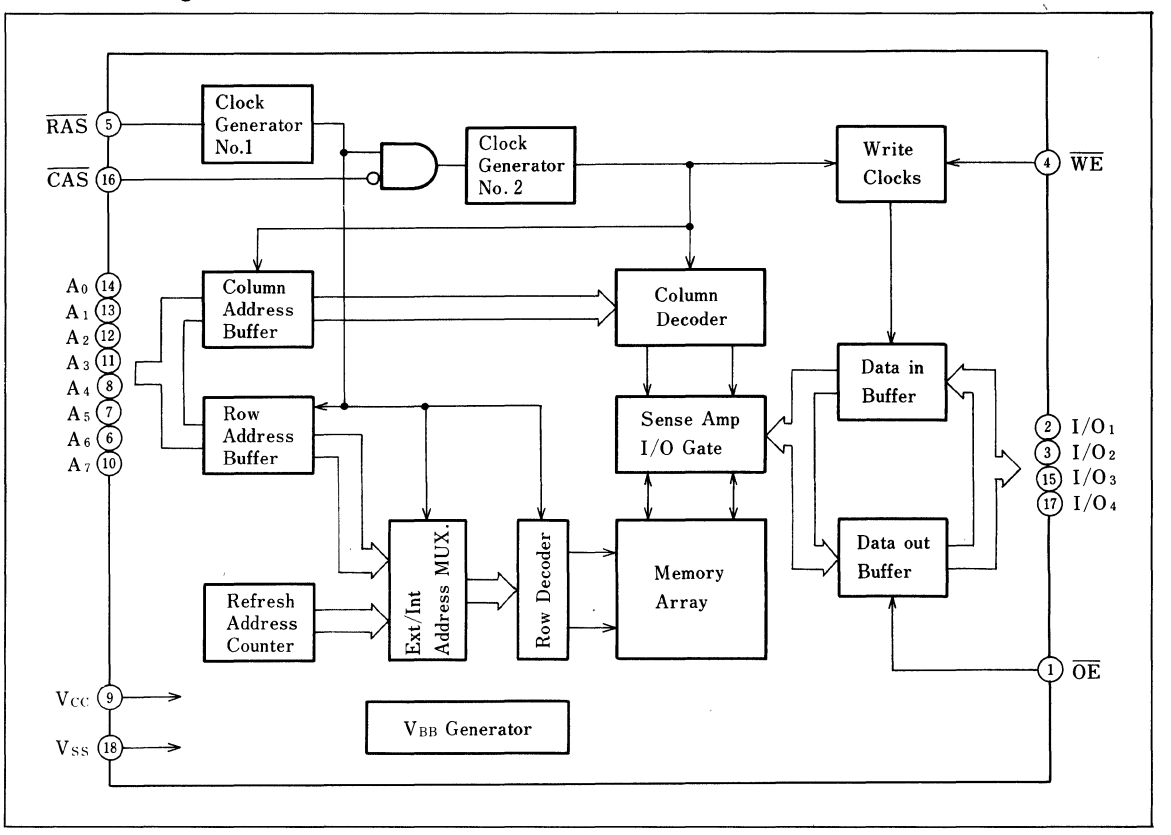
1. 65,536-word by-4-bit organization
2. LH2464 : page-mode
   LH2465 : nibble-mode
3. Access time (MAX.)
   LH2464/5-10 : 100ns
   LH2464/5-12 : 120ns
   LH2464/5-15 : 150ns
4. Single +5V power supply
5. Power consumption (MAX.) :
   467.5mW (operation)
   27.5mW (stand-by)
6. $\overline{CAS}$-before-$\overline{RAS}$ refresh capabilities
7. Built-in refresh counter
8. 4ms refresh period, 256 cycle refresh
9. 18-pin dual-in-line package

Pin Connections



Top View

■ Block Diagram



LH21256/LH21257/LH21258

NMOS 262144-Bit Dynamic Random Access Memory

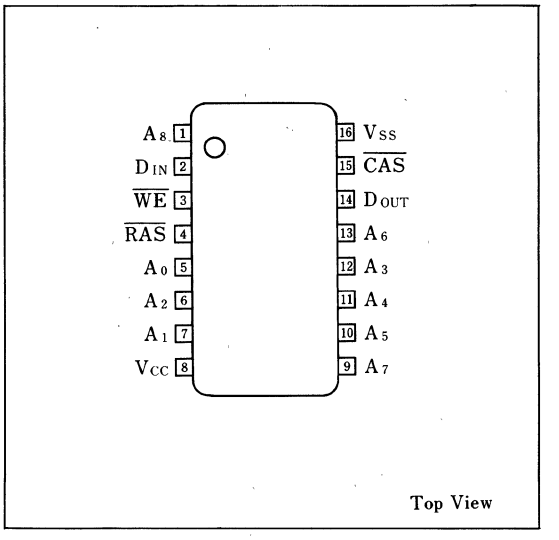
■ Description

The LH21256/LH21257/LH21258 are dynamic RAMs organized as 262,144-word-by-1-bit using high-performance depletion load n-channel double-polycide silicon-gate MOS technology.

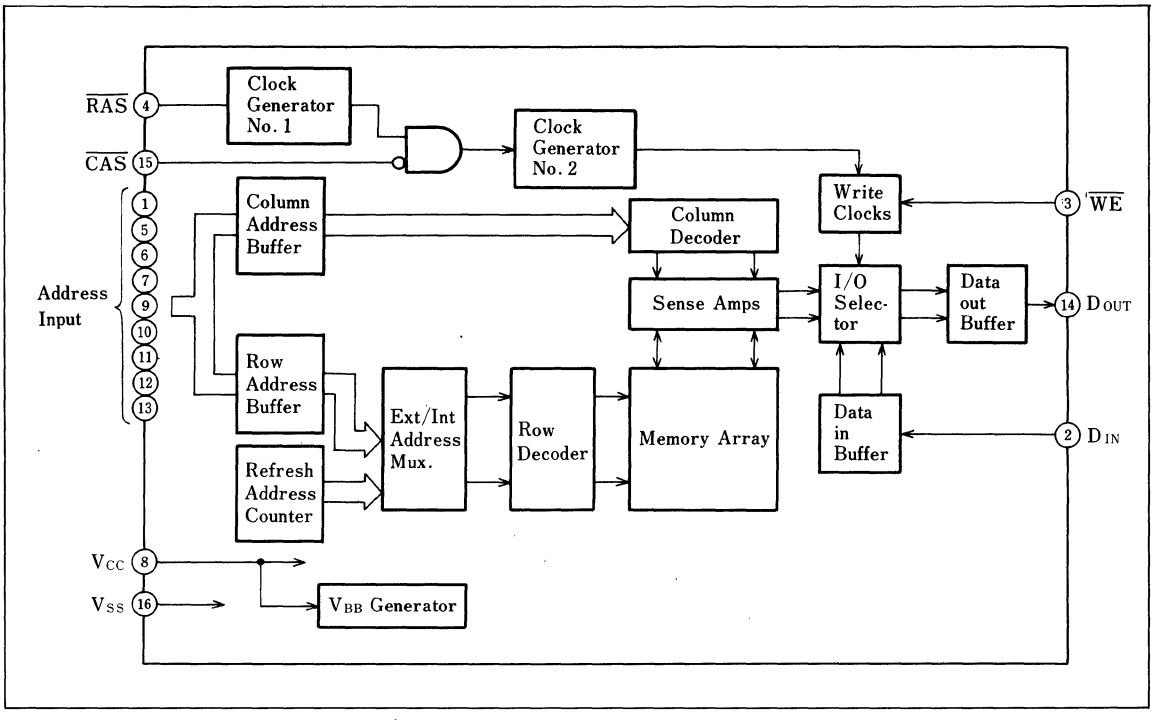
■ Features

1. 262,144-word-by-1-bit organization
2. LH21256 : page-mode
   LH21257 : nibble-mode
   LH21258 : byte-mode
3. Access time (MAX.)
   LH21256/7/8-10 : 100ns
   LH21256/7/8-12 : 120ns
   LH21256/7/8-15 : 150ns
4. Cycle time (MIN.)
   LH21256/7/8-10 : 200ns
   LH21256/7/8-12 : 230ns
   LH21256/7/8-15 : 260ns
5. Single +5V power supply
6. All inputs and outputs TTL compatible
7. Address and input data latch capability
8. Three-state output data controlled by $\overline{CAS}$ and not latched at the end of cycle
9. Common I/O capability using the early-write mode
10. Read/modify/write, $\overline{RAS}$-only refresh hidden refresh capabilites and $\overline{CAS}$ before $\overline{RAS}$ refresh
11. Built-in refresh counter
12. 4ms refresh period, 256 cycle refresh
13. 16-pin dual-in-line package

■ Pin Connections



■ Block Diagram



LSIs for Telephone

9

LR4087 Tone Dialer CMOS LSI

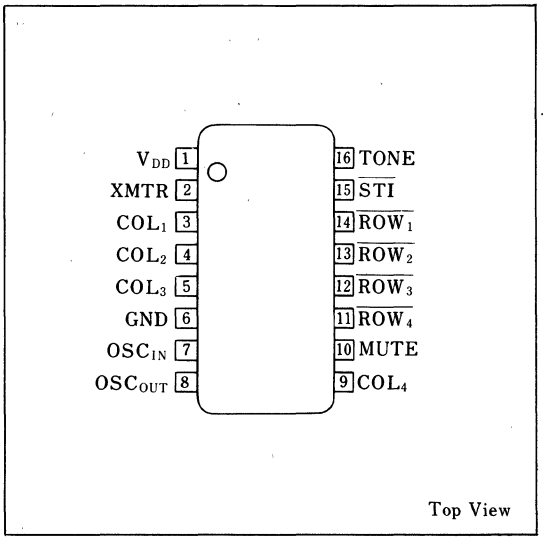
Description

The LR4087 is a monolithic LSI and uses an inexpensive crystal reference to provide eight audio sinusoidal frequencies Dual-Tone Multi-Frequency is obtained by mixing these frequencies.

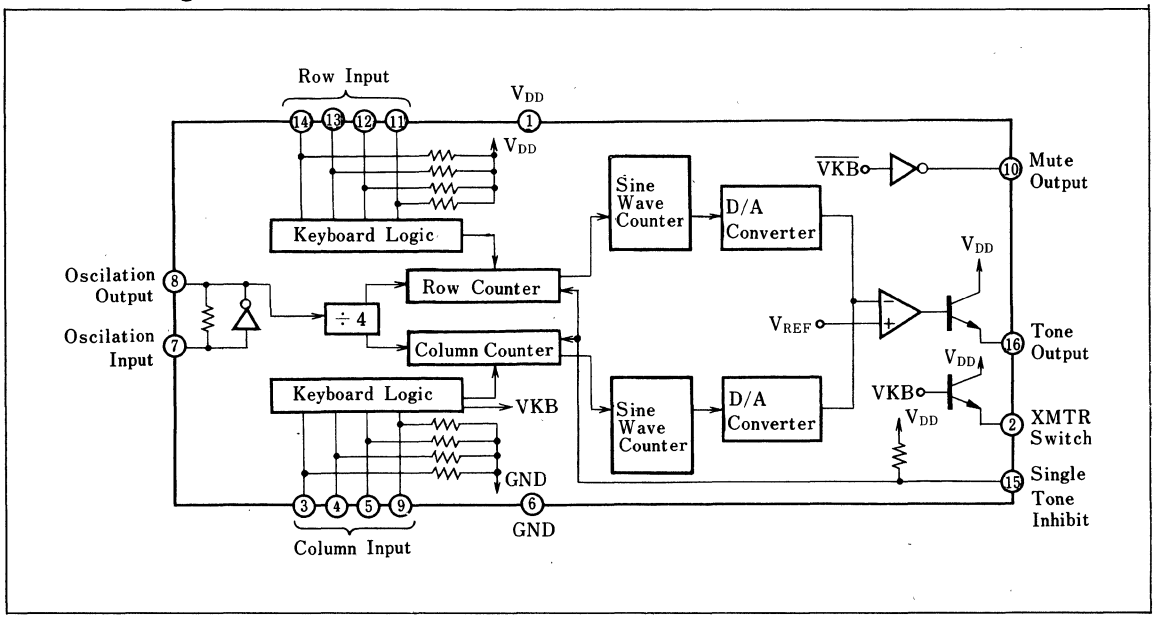
Features

1. Low standby current
2. Auxiliary switching functions on chip
3. Minimum external parts count
4. Uses inexpensive 3.579545MHz television color-burst crystal
5. Built-in regulator of dual or single tone amplitudes
6. 16-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	10.5	V	1
Operating temperature	T_{opr}	−30～+60	℃	
Storage temperature	T_{stg}	−55～+150	℃	
Maximum power consumption	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=25℃
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Recommended Operating Conditions

Parameter	Symbol	Raiting	Unit
Supply voltage	V_{DD}	3.5～10.0	V

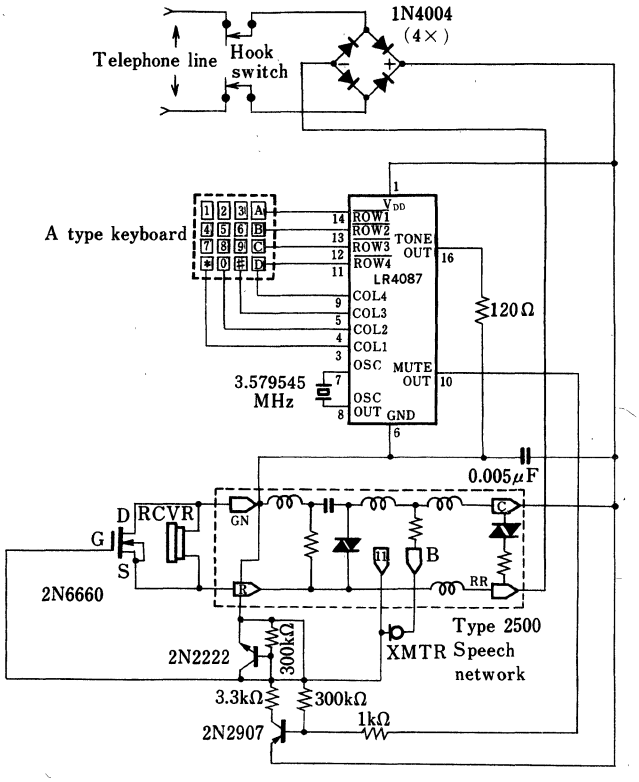
■ Electrical Characteristics

(Ta=−30～+60℃)

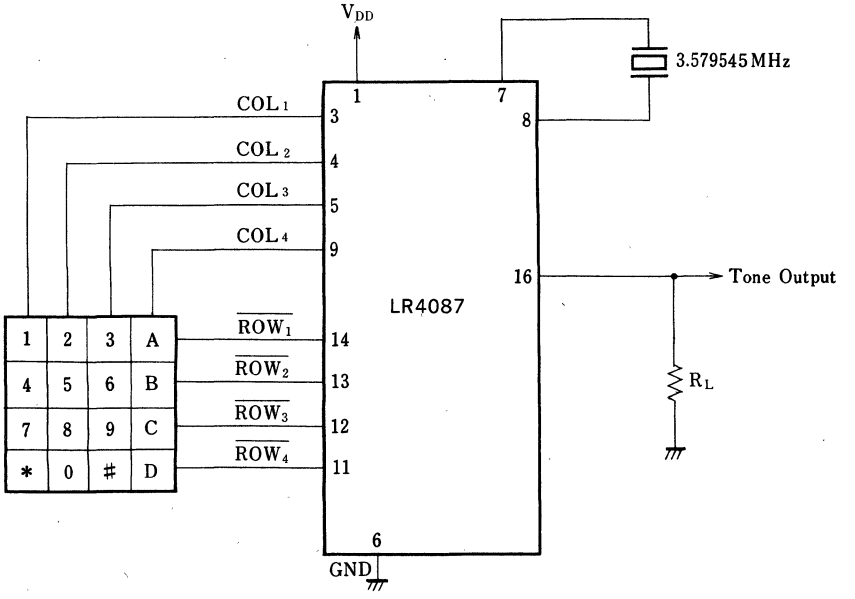
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
$\overline{STI}$ input voltage		V_{IH1}		$0.7V_{DD}$		V_{DD}	V	5
		V_{IL1}		0.0		$0.3V_{DD}$	V	
COL input voltage		V_{IH2}		$0.7V_{DD}$		V_{DD}	V	6
		V_{IL2}		0.0		$0.1V_{DD}$	V	
$\overline{ROW}$ input voltage		V_{IH3}		$0.9V_{DD}$		V_{DD}	V	7
		V_{IL3}		0.0		$0.3V_{DD}$	V	
Output voltage	ROW TONE	V_{OR}	R_L=1kΩ	317	400	504	mV_{rms}	8
	COL TONE	V_{OC}		396	500	630	mV_{rms}	
TONE output resistance		R_{L1}	V_{DD}=3.5V		620		Ω	
		R_{L2}	V_{DD}=10.0V		330		Ω	
XMTR output current, no key input		I_{OHX1}	V_{DD}=3.5V, V_{OHX}=2.5V	−15	−25		mA	10
		I_{OHX2}	V_{DD}=10.0V, V_{OHX}=8.0V	−50	−100		mA	
XMTR output current, in key input		I_{XLEAK}	V_{DD}=10.0V, V_{OUT}=0V		0.1	10.0	μA	10
MUTE output current, no key input		I_{OL1}	V_{DD}=3.5V, V_{OL}=0.5V	0.5	2.0		mA	11
		I_{OL2}	V_{DD}=10.0V, V_{OL}=0.5V	1.0	4.0		mA	
MUTE output current, in key input		I_{OH1}	V_{DD}=3.5V, V_{OH}=3.0V	0.5	2.0		mA	11
		I_{OH2}	V_{DD}=10.0V, V_{OH}=9.5V	1.0	4.0		mA	
Standby current		I_{SB1}	V_{DD}=3.5V		0.25	100	μA	9
		I_{SB2}	V_{DD}=10.0V		0.5	200	μA	
Operating current		I_{OP1}	V_{DD}=3.5V		1.0	2.0	mA	9,13
		I_{OP2}	V_{DD}=10.0V		5.0	10.0	mA	
Input resistance		R_{IN}		20		100	kΩ	5,8
Tone output (no key input)						−80	dBm	
Output rise time		t_r			3.0	5.0	ms	12,13
Pre-emphasis				1.0	2.0	3.0	dB	14
Tone output distortion			V_{DD}≧4.0V			−20	dB	15

Note 5 : Applies to $\overline{STI}$ pin.
Note 6 : Applies COL input pin
Note 7 : Applies $\overline{ROW}$ input pin
Note 8 : Ta=25℃
Note 9 : All output pins open
Note 10 : Applies to XMTR output pins
Note 11 : Applies to MUTE output pin.
Note 12 : Rise time for tone output to reach 90% of maximum amplitude after key input.
Note 13 : Characteristics of crystal resonator used. Rs=100Ω, L_m=96mH, C_M=0.02pF, C_h=5pF, F=3.579545MHz
Note 14 : Level ratio of high group tone to low group tone.
Note 15 : Unnecessary frequency components against total power of basic tone signal of $\overline{ROW}$ and COL.

System Configuration



Test Circuit



LR4089 Tone Dialer CMOS LSI

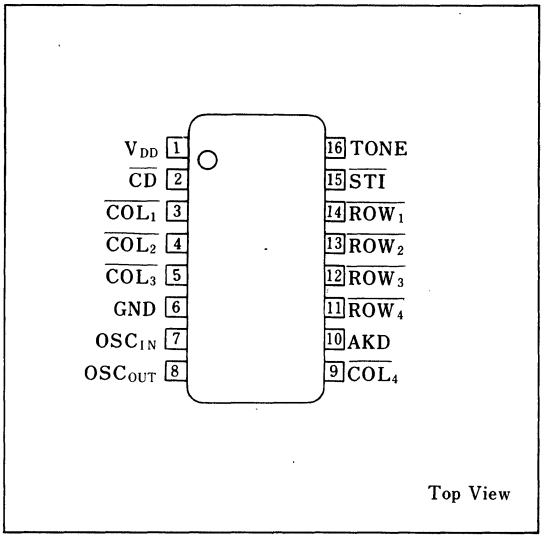
Description

The LR4089 is a monolithic LSI and uses an inexpensive crystal reference to provide eight audio sinusoidal frequencies. Dual-Tone Multi-Frequency is obtained by mixing these frequencies.

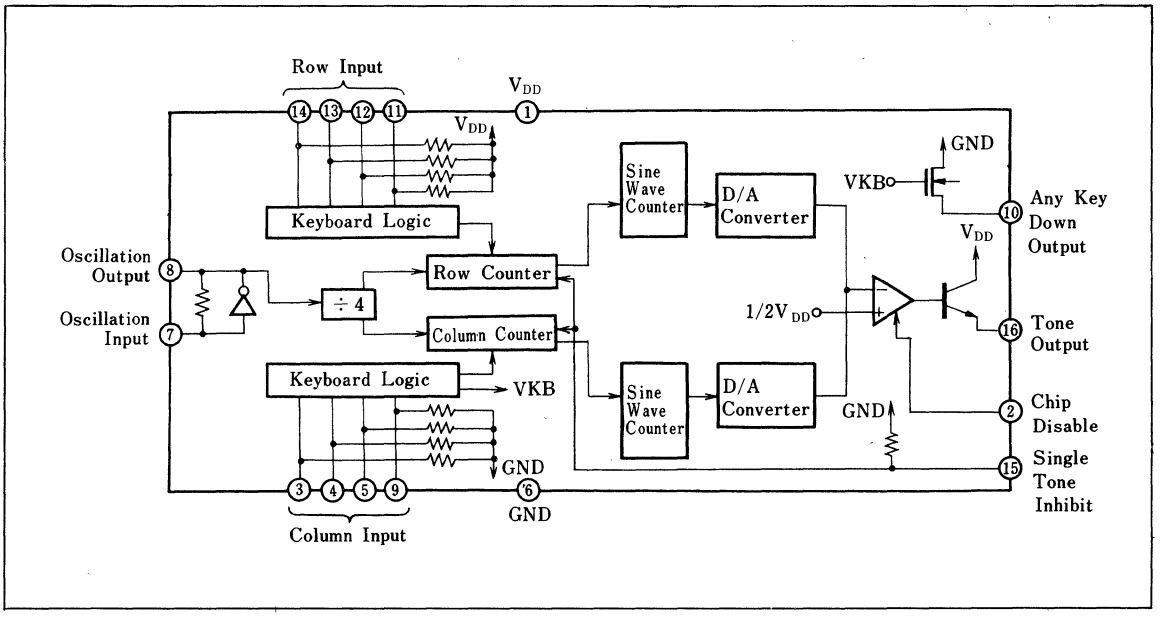
Features

1. Minimum external parts count
2. Divider, R-2R resistive ladder, CMOS operational amplifier on chip
3. High-accuracy tone out
4. Uses inexpensive 3.579545MHz television color-burst crystal
5. Single tone output
6. $\overline{CD}$ inhibits tone generation
7. 16-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	10.5	V	1
Operating temperature	T_{opr}	−30～+60	℃	
Storage temperature	T_{stg}	−55～+150	℃	
Maximum power consumption	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=25℃
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	3.0～10.0	V

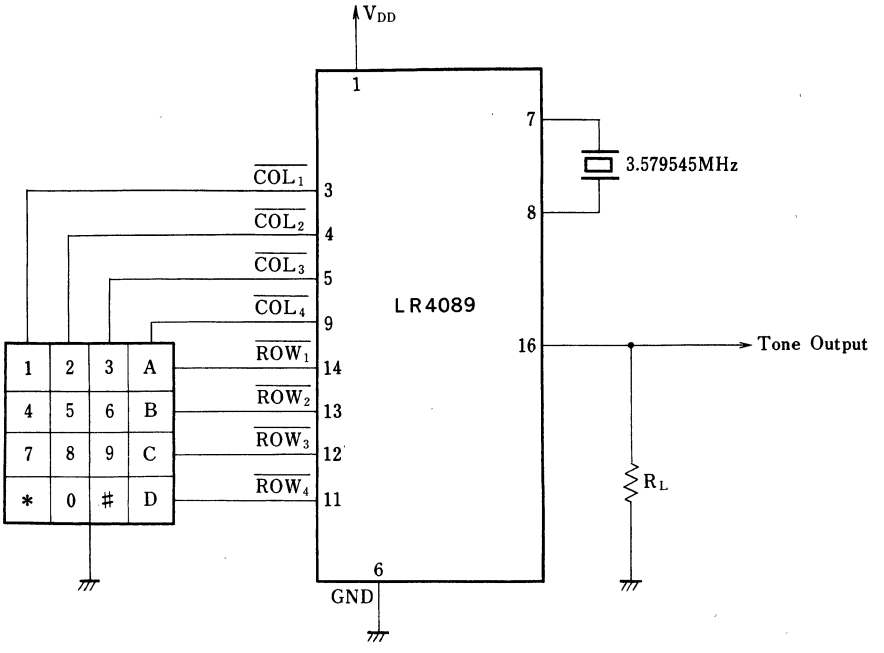
■ Electrical Characteristics

(Ta=−30～+60℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage		V_{INL}		GND		$0.3V_{DD}$	V	5
Input high voltage		V_{INH}		$0.7V_{DD}$		V_{DD}	V	5
Input resistance		R_I	Ta=25℃	20		100	kΩ	6
TONE DISABLE input voltage		V_{INTD}		GND		$0.3V_{DD}$	V	
TONE output level		V_{OUT}	V_{DD}=3.4～3.6V, R_L=100kΩ	−10		−7.0	dBm	7,15
Pre-emphasis				2.4	2.7	3.0	dB	8
TONE output distortion			V_{DD}=3.4～10.0V			−20	dB	9
Output rise time		t_r			2.8	5.0	ms	10,11
AKD output sink current		$I_{AKD\ ON}$	V_{OUT}=0.5V	500			μA	12
AKD output off current		$I_{AKD\ OFF}$	V_{OUT}=5.0V			2	μA	12
Supply current	In operation	I_{OP}	V_{DD}=3.5V			2.0	mA	13
	In standby	I_{SB}	V_{DD}=10.0V			200	μA	14
Tone input level (no key input)						−80	dBm	

Note 5 : Applies to $\overline{ROW}$ and $\overline{COL}$ input pins.
Note 6 : Applies to $\overline{STI}$ and $\overline{CD}$ input pins.
Note 7 : Applies to low group single tone signal.
Note 8 : Level radio of high group tone signal to low group tone signal.
Note 9 : Unnecessary frequency component against basic tone signal total power (RMS) of $\overline{ROW}$ and $\overline{COL}$.
Note 10 : Rise time for tone output to reach 90% of maximum amplitude after key input.
Note 11 : Characteristics of crystal resonator used. R_S=100Ω, L_m=96mH, C_M=0.02pF, C_h=5pF, F=3.579545MHz.
Note 12 : AKD output means N-channel open drain output.
Note 13 : In single key input, $\overline{CD}$="1", $\overline{STI}$="0"
Note 14 : In stand-by, $\overline{CO}$="1", $\overline{STI}$="0"
Note 15 : OdBm=0.775V

Test Circuit



LR4091 Tone Dialer CMOS LSI

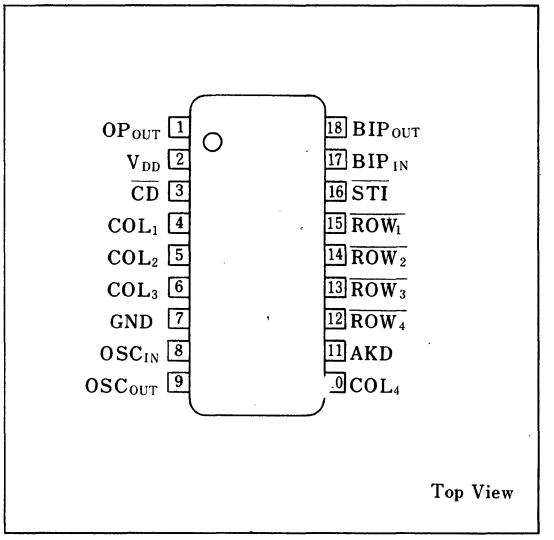
Description

The LR4091 is a monolithic LSI and uses an inexpensive crystal reference to provide eight audio sinusoidal frequencies. Dual-Tone Multi-Frequency is obtained by mixing these frequencies.

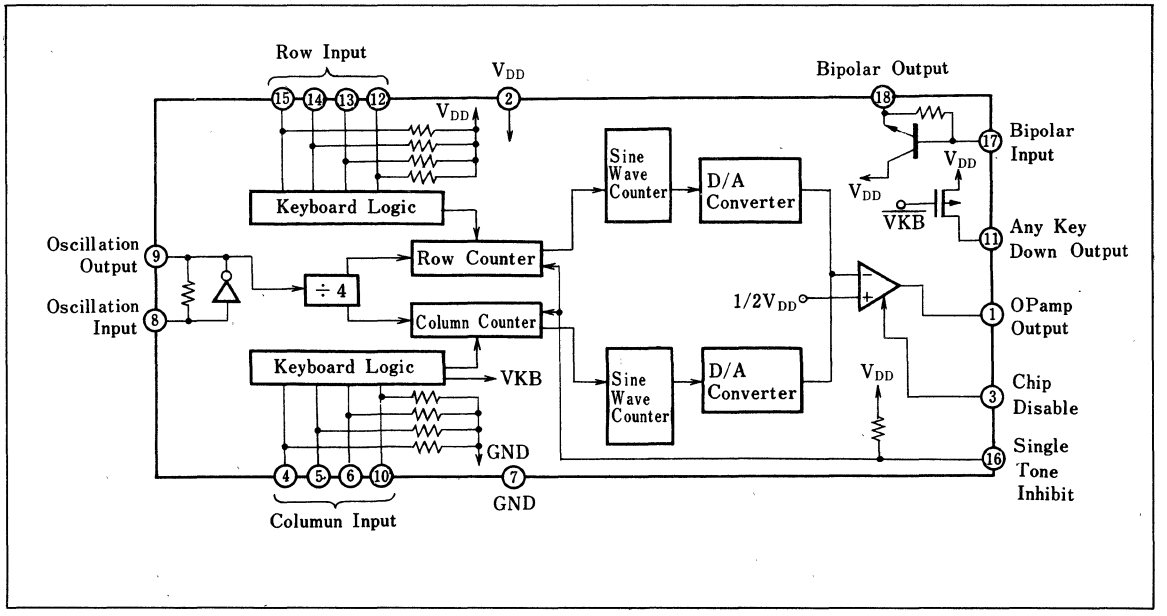
Features

1. CEPT Compatible
2. High accuracy tone output
3. Divider, resistive ladder network, CMOS operational amplifier, and bipolar transistor on chip
4. Uses 3.579545MHz crystal
5. Single tone output
6. Uses either 2-of-8 keyboard or single contact keyboard
7. Low standby current
8. 18-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	10.2	V	1
Operating temperature	T_{opr}	−30～+60	℃	
Storage temperature	T_{stg}	−55～+150	℃	
Maximum power consumption	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=20℃
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	3.0～10.0	V

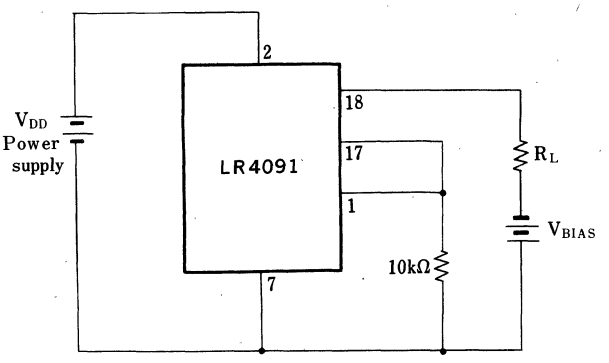
■ Electrical Characteristics

(Ta=−30～+60℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	In operating	V_{DD}	When tone signal is output	3.0		10.0	V	
	In stand-by	V_{DD}	$\overline{CD}$=0	2.0		10.0	V	5
COL input voltage		V_{IH1}		0.7V_{DD}		V_{DD}	V	6
		V_{IL1}		0.0		0.3	V	
$\overline{ROW}$ input voltage		V_{IH2}		V_{DD}−0.3		V_{DD}	V	7
		V_{IL2}		0.0		0.3V_{DD}	V	
Input voltage		V_{IH3}		0.7V_{DD}		V_{DD}	V	8
		V_{IL3}		0.0		0.3V_{DD}	V	
Input resistance		R_I	Ta=25℃	20		100	kΩ	8
Tone output level		V_{OUT}	V_{DD}=3.4～3.6V	−10.0	−8.5	−7.0	dBm	9,17
Pre-emphasis (high-group tone signal)			No filter	1.0	2.0	3.0	dB	10,17
Tone output distortion			V_{DD}=3.4～10.0V			−20	dB	11,17
Output rise time		t_r				5	ms	12
AKD output source current		$I_{AKD\ ON}$	V_{DD}=3.5V, V_{AKD}=3.0V	500			μA	13
AKD output off current		$I_{AKD\ OFF}$	V_{DD}=10.0V, V_{AKD}=0V			10	μA	
Supply current	In operation	I_{OP}	V_{DD}=3.5V		1.0	2.0	mA	14
	In operation	I_{OP}	V_{DD}=10.0V		5.0		mA	
	In stand-by	I_{SB}	V_{DD}=10.0V		1.0	200	μA	15
Tone output (no key input)						−80	dBm	
OP amplifier output resistance					10		kΩ	16
OP amplifier output current			V_{DD}=3.0V	250			μA	16

Note 5 : Voltage to which AKD output responds by key input.
Note 6 : Applies to COL input pins (COL_{1-4}).
Note 7 : Applies to $\overline{ROW}$ input pins ($\overline{ROW}_{1-4}$).
Note 8 : Applies to $\overline{CD}$ and STI input pins.
Note 9 : Applies to low-group single tone signal.
Note 10 : Level ratio of high-group tone signal to low-group tone signal.
Note 11 : Unnecessary frequency component against basic tone signal total power (RMS) of $\overline{ROW}$ and COL.
Note 12 : Rise time for tone output reach 90% of maximum amplitude after key input.
Crystal reasonators used are as follows :
R_S=100Ω, L_M=96mH, C_M=0.02pF, C_h=5pF, F=3.579545MHz
Note 13 : AKD output is P-channel open drain output.
Note 14 : Crystal resonator is used as indicated in Note 12 when single key is pressed (pin 6).
Note 15 : In stand-by, $\overline{CD}$="0", STI="1"
Note 16 : OP amplifier output resistance is determined by capacity of pin 1. The 10 kΩ shown in the test circuit is used in a standard filter circuit. When the capacity of pin 1 is too large, it is necessary to reduce the resistance.
Note 17 : R_L (Pin 18)=620Ω : V_{DD}=3.4−5V
300Ω : V_{DD}=7.5V or more

Test Circuit



$V_{BIAS}=0.5V : V_{DD} \leqq 4.0V$
$V_{BIAS}=0V : V_{DD} > 4.0V$

LR4092 Tone Dialer CMOS LSI

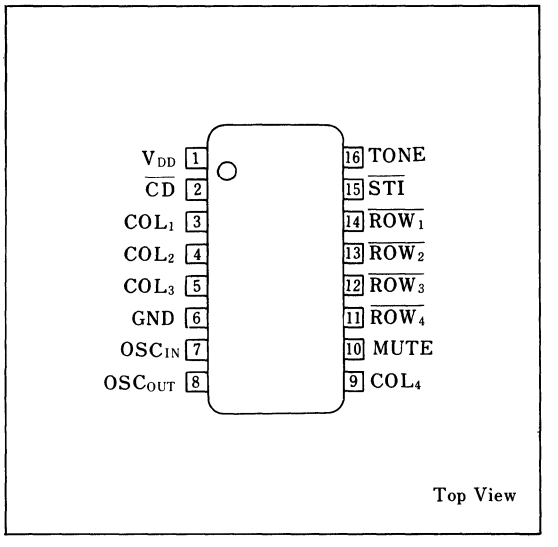
Description

The LR4092 is a monolithic LSI and uses an inexpensive crystal reference to provide eight audio sinusoidal frequencies. Dual-Tone Multi-Frequency is obtained by mixing these frequencies.

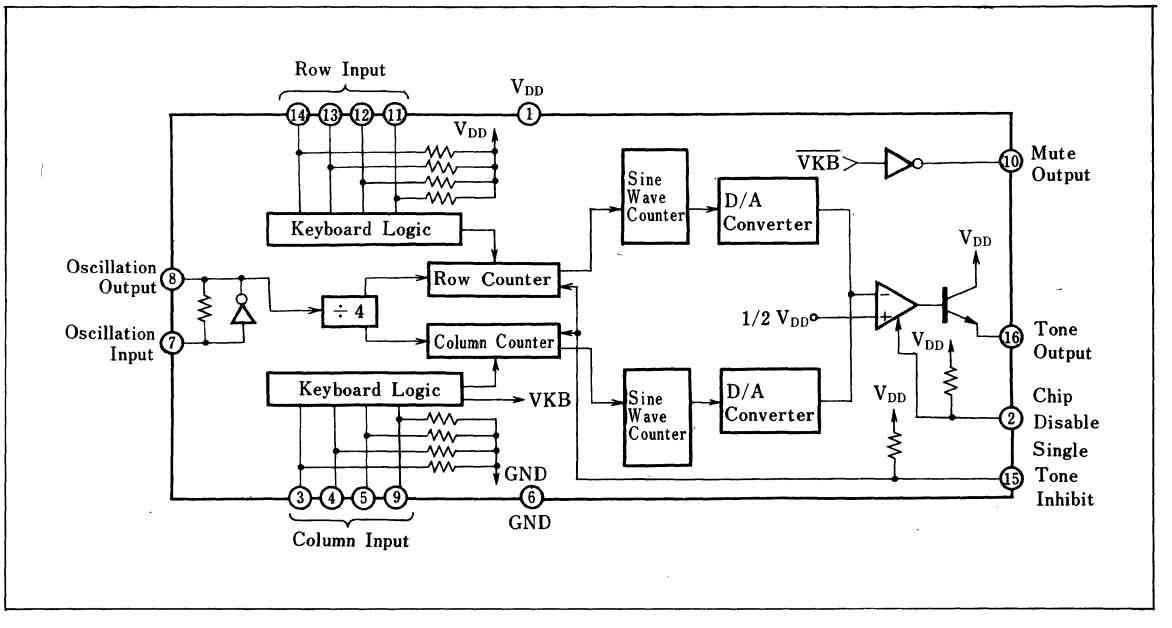
Features

1. Internal regulation of tone amplitudes
2. Internal loop compensation and pre-emphasis
3. Tone frequencies within 0.65% for 12 standard frequencies
4. Uses inexpensive 3.579545MHz television color-burst crystal
5. Tone-disable capability
6. Mute output for electronic switching
7. Uses either 2-of-8 keyboard or single contact keyboard
8. Single-tone capability
9. 16-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	+10.5	V	1
Operating temperature	T_{opr}	0～+60	℃	
Storage temperature	T_{stg}	−35～+85	℃	
Maximum power consumption	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

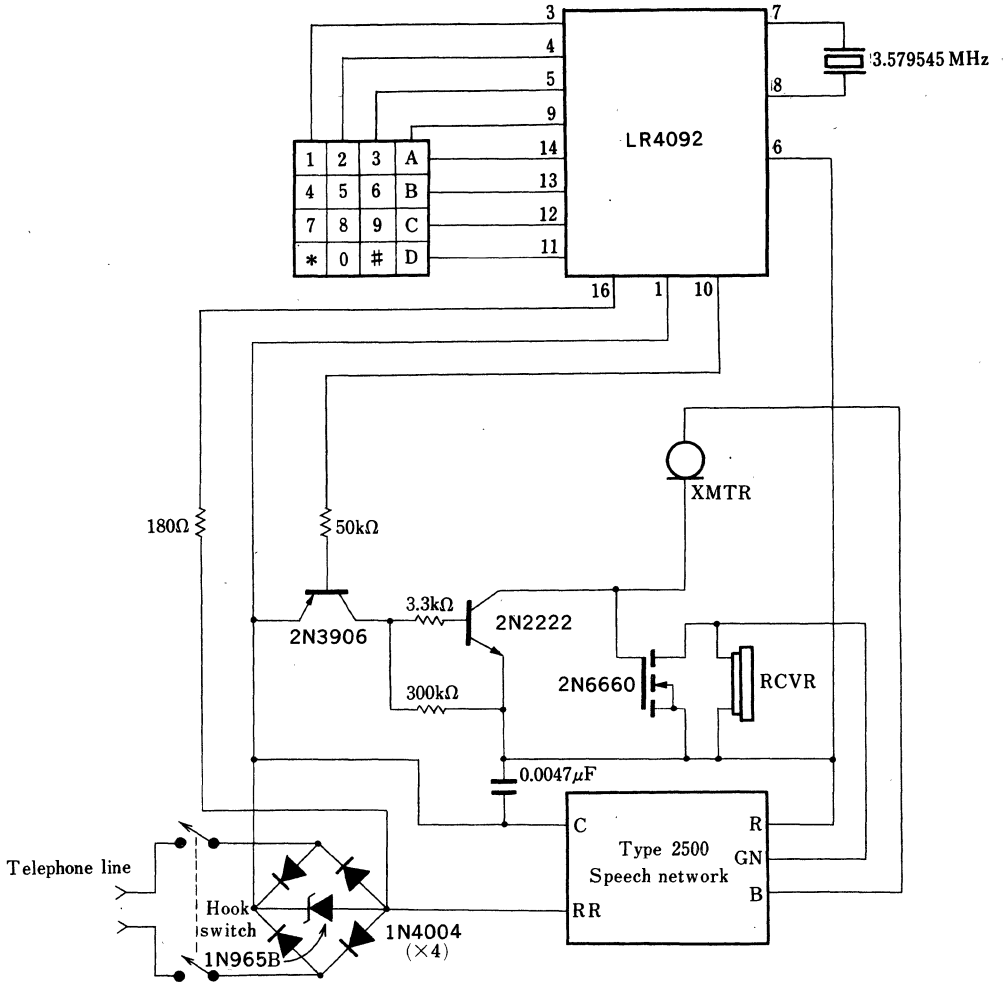
Note 1 : Referenced to GND.
Note 2 : Ta=25℃
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Electrical Characteristics

(Ta=0～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage						
Tel Loop in Operation	V_{DDa}		3.5		10.0	V
Power Supply in Operation	V_{DDb}		3.8		10.0	V
Stand-by	V_S	$\overline{CD}$=GND	3.0		10.0	V
$\overline{CD}$, $\overline{STI}$ input voltage						
logic "1"	V_{IH}		$0.7V_{DD}$		V_{DD}	V
logic "0"	V_{IL}		0.0		$0.3V_{DD}$	V
COL input voltage						
logic "1"	V_{IHC}		$0.7V_{DD}$		V_{DD}	V
logic "0"	V_{ILC}		0.0		$0.1V_{DD}$	V
$\overline{ROW}$ input voltage						
logic "1"	V_{IHR}		$0.9V_{DD}$		V_{DD}	V
logic "0"	V_{ILR}		0.0		$0.3V_{DD}$	V
Input resistance						
$\overline{ROW}$	R_{RI}	Ta=25℃		15		kΩ
COL	R_{CI}	Ta=25℃		15		kΩ
$\overline{CD}$, $\overline{STI}$		Ta=25℃	20	60	125	kΩ

System Configuration



LR40981A Pulse Dialer CMOS LSI

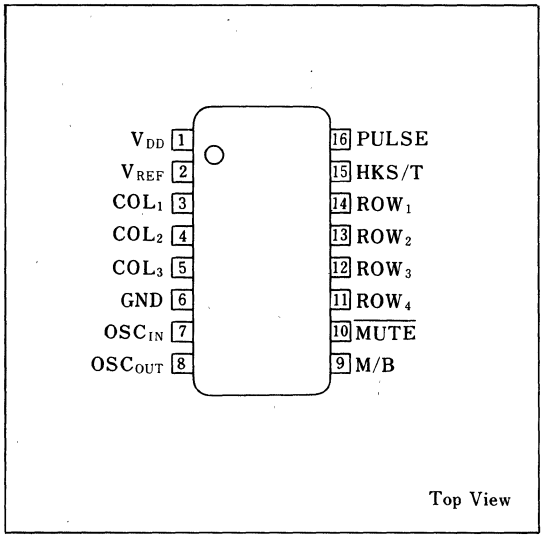
Description

The LR40981A is a monolithic CMOS LSI which uses a ceramic resonator and provides the features required for a pulse dialer with redial.

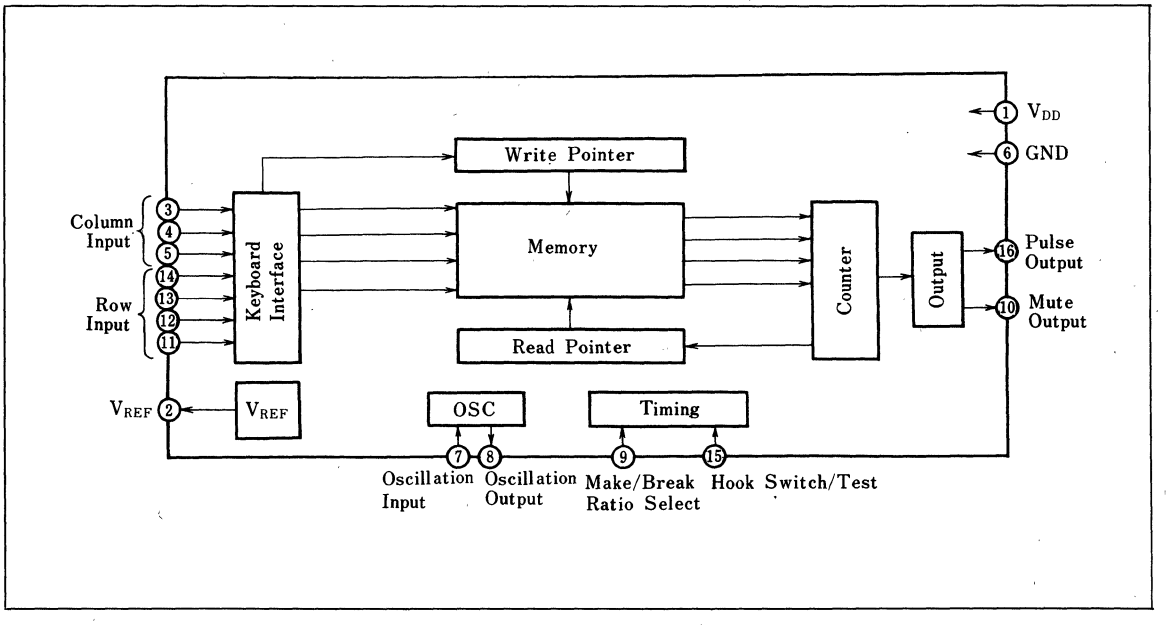
Features

1. Direct telephone-line operation
2. Uses 2-of-7 matrix keyboard
3. CMOS process for low-power operation
4. 2.5~6.0V power supply
5. Make/Break ratio pin-selectable
6. Ceramic resonator used as frequency reference
7. Redial with # or *
8. $\overline{\text{MUTE}}$ output for electronic switching
9. 16-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3～+6.2	V	1
Operating temperature	T_{opr}	−30～+60	℃	
Storage temperature	T_{stg}	−55～+150	℃	
Maximum power consumption	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=25℃
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Recommended Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	2.5～6.0	V

■ Electrical Characteristics

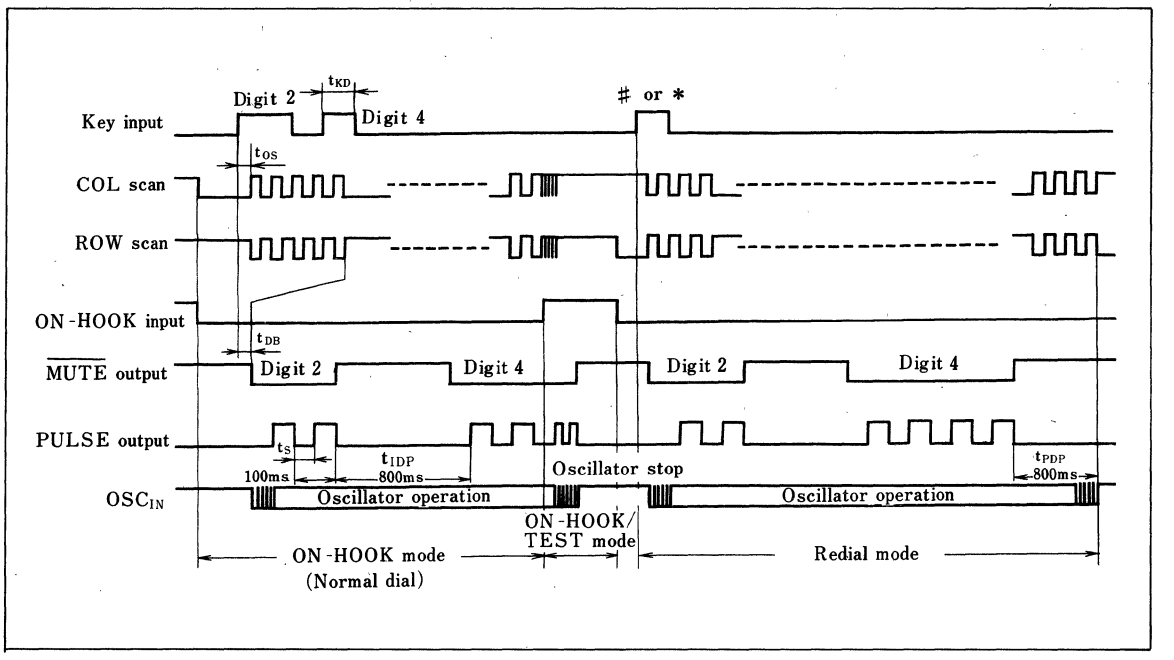
(Ta=−30～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Key contact resistance	R_{KI}				1	kΩ	
Key board capacity	C_{KI}				30	pF	
Input voltage	K_{IH}	2-of-7 input mode	$0.8V_{DD}$		V_{DD}	V	5
	K_{IL}		GND		$0.2V_{DD}$	V	5
Key pull-up resistance	K_{IRU}	V_{DD}=6.0V, V_{IN}=4.8V		100		kΩ	
Key pull-down resistance	K_{IRD}			4		kΩ	
$\overline{\text{MUTE}}$ sink current	I_M	V_{DD}=2.5V, V_{OUT}=0.5V	500			μA	6
Pulse output sink current	I_P	V_{DD}=2.5V, V_{OUT}=0.5V	1.0			mA	7
(V_{DD}-V_{RFF}) value	V_{REF}	I_{SUPPLY}=150 μA	1.5	2.5	3.5	V	8
Memory hold current	I_{MR}	All outputs in no-load state		0.7		μA	
Operating current	I_{OP}	All outputs in no-load state		100	150	μA	
$\overline{\text{MUTE}}$, PULSE Output off current	I_{LKG}	V_{DD}=6.0V, V_{OUT}=6.0V		0.001	1	μA	6,7

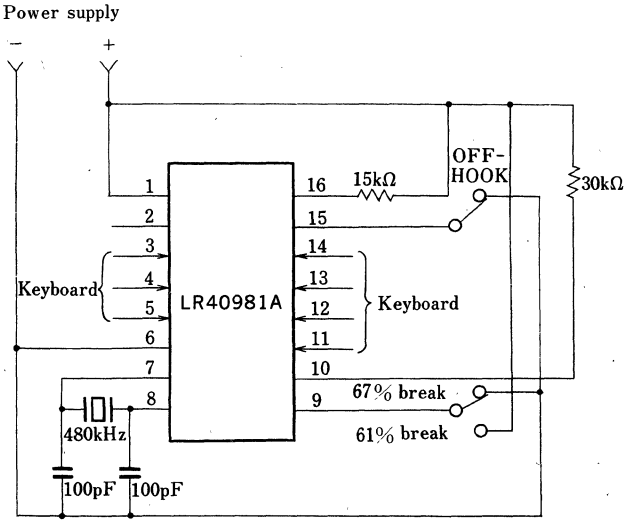
Note 5 : Applies to key input pins ($RDW_{1\sim4}$, $COL_{1\sim3}$)
Note 6 : Applies to $\overline{\text{MUTE}}$ output pin.
Note 7 : Applies to PULSE output pin.
Note 8 : Applies to V_{REF} pin.

9

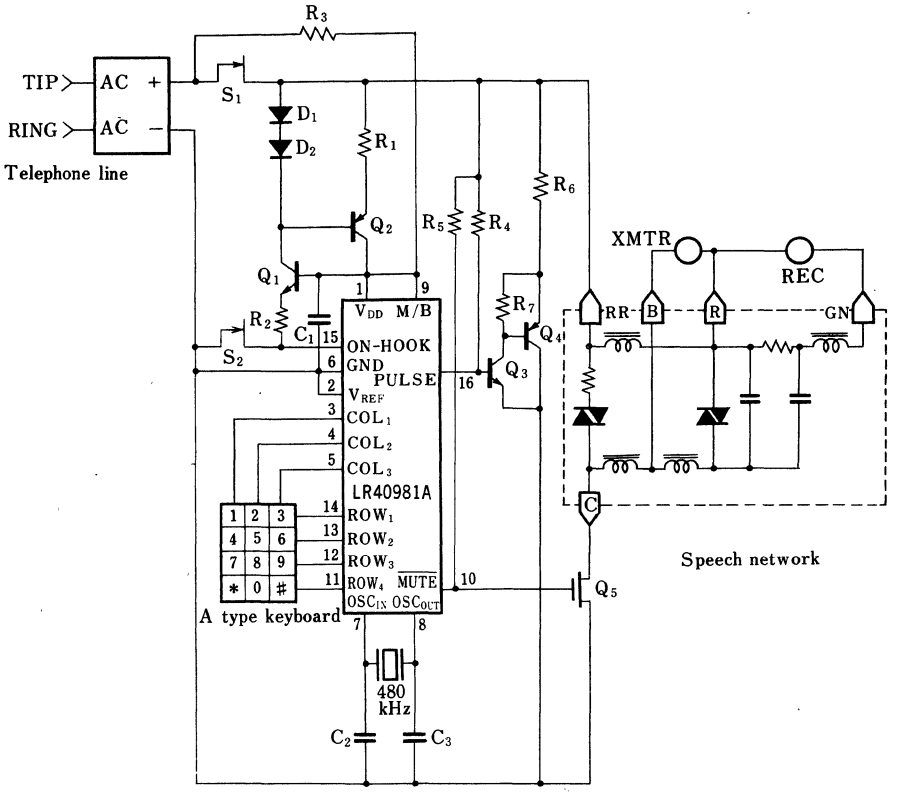
■ Timing Diagram



■ Test Circuit



System Configuration



Q_1, Q_3 : 2N5550
Q_2, Q_4 : 2N5401
Q_5 : 2N6661
D_1, D_2 : 1N914
C_1 : 20μF (low leakage product)
C_2, C_3 : 100pF±20%

R_1 : 2.7kΩ
R_2 : 75kΩ
R_3 : 22MΩ
R_4 : 390kΩ
R_5 : 1MΩ
R_6 : 150Ω
R_7 : 100kΩ

LR40982 Pulse Dialer CMOS LSI

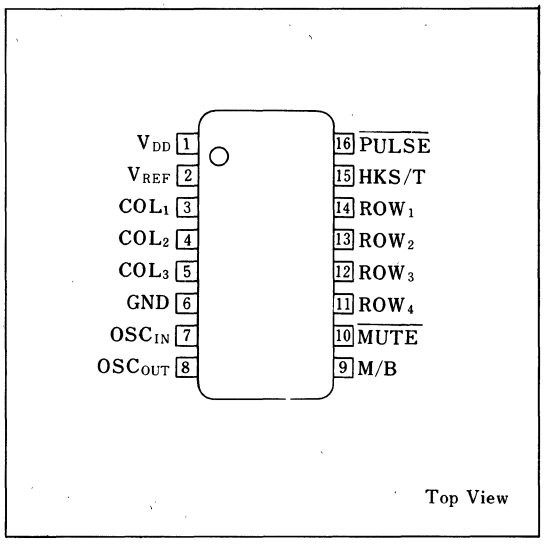
■ Description

The LR40982 is a monolithic CMOS LSI which uses a ceramic resonator and provides the features required for a pulse dialer with redial.

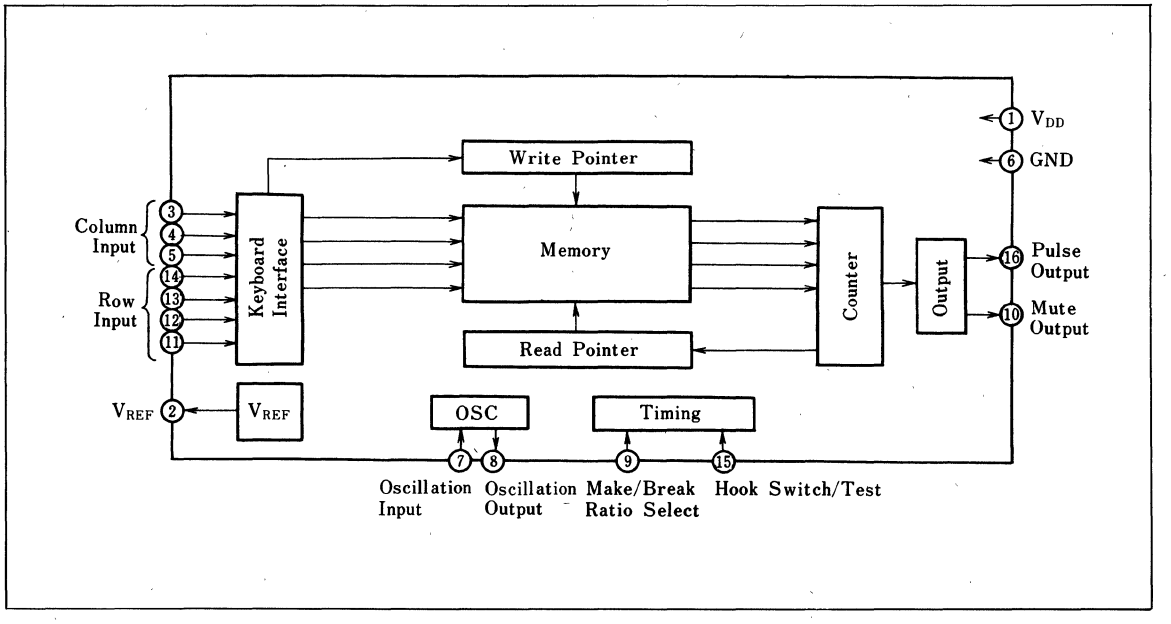
■ Features

1. Direct telephone-line operation
2. Uses 2-of-7 matrix keyboard
3. CMOS process for low-power operation
4. 2.5~6.0V power supply
5. Make/Break ratio pin-selectable
6. Ceramic resonator used as frequency reference
7. Redial with # or *
8. MUTE output for electronic switching
9. 16-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3～+6.2	V	1
Operating temperature	T_{opr}	−30～+60	℃	
Storage temperature	T_{stg}	−55～+150	℃	
Maximum power consumption	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=25℃.
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Recommended Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	2.5～6.0	V

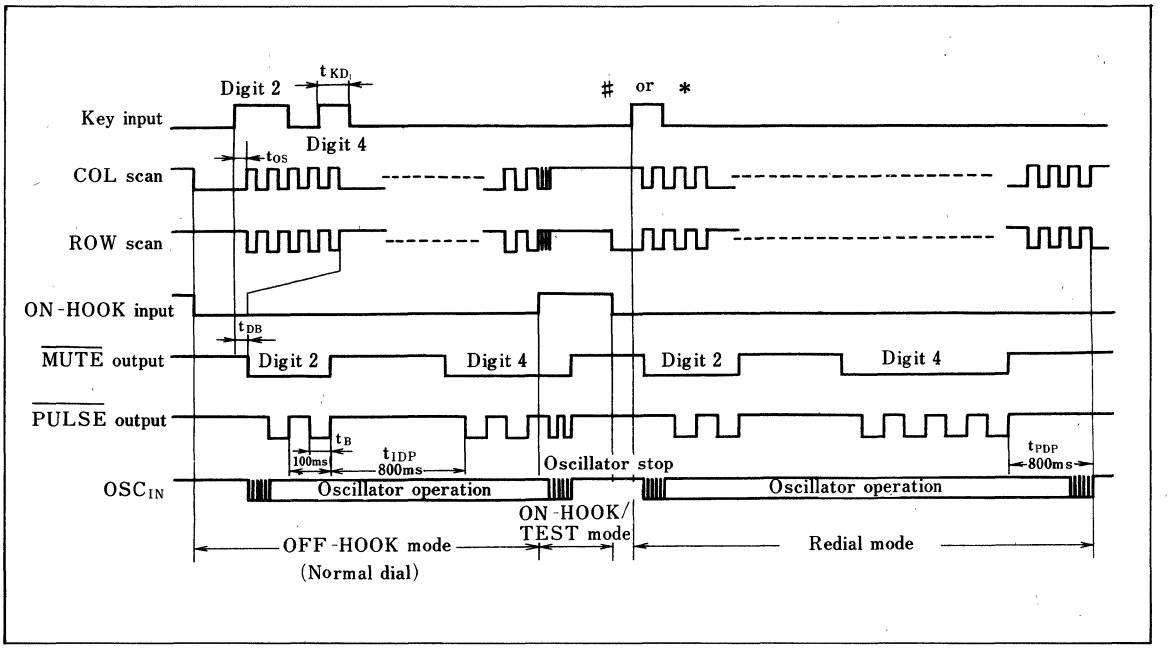
■ Electrical Characteristics

(Ta=−30～+60℃)

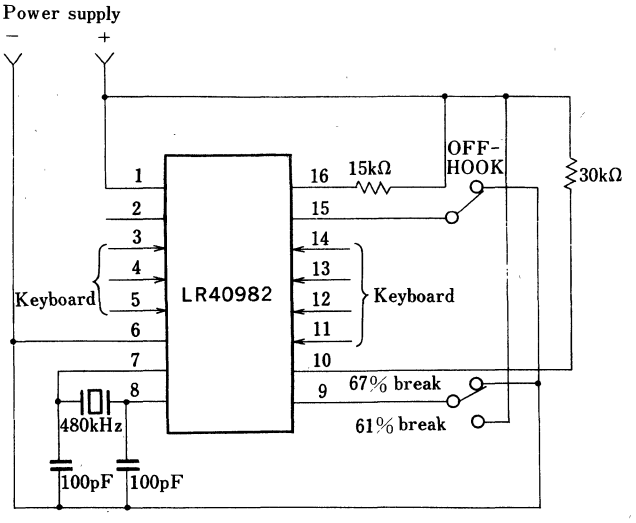
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Key contact resistance	R_{KI}				1	kΩ	
Key board capacity	C_{KI}				30	pF	
Input voltage	K_{IH}	2-of-7 input mode	$0.8V_{DD}$		V_{DD}	V	5
	K_{IL}		GND		$0.2V_{DD}$	V	5
Key pull-up registance	K_{IRU}	V_{DD}=6.0V, V_{IN}=4.8V		100		kΩ	
Key pull-down resistance	K_{IRD}			4		kΩ	
$\overline{\text{MUTE}}$ sink current	I_M	V_{DD}=2.5V, V_{OUT}=0.5V	500			μA	6
Pulse output sink current	I_P	V_{DD}=2.5V, V_{OUT}=0.5V	1.0			mA	7
(V_{DD}-V_{REF}) value	V_{REF}	I_{SUPPLY}=150 μA	1.5	2.5	3.5	V	8
Memory hold current	I_{MR}	All outputs in no-load state		0.7		μA	
Operating current	I_{OP}			100	150	μA	
$\overline{\text{MUTE}}$, $\overline{\text{PULSE}}$ Output off current	I_{LKG}	V_{DD}=6.0V, V_{OUT}=6.0V		0.001	1	μA	6,7

Note 5 : Applies to key input pins (RDW_{1-4}, COL_{1-3}).
Note 6 : Applies to $\overline{\text{MUTE}}$ output pin.
Note 7 : Applies to $\overline{\text{PULSE}}$ output pin.
Note 8 : Applies to V_{REF} pin.

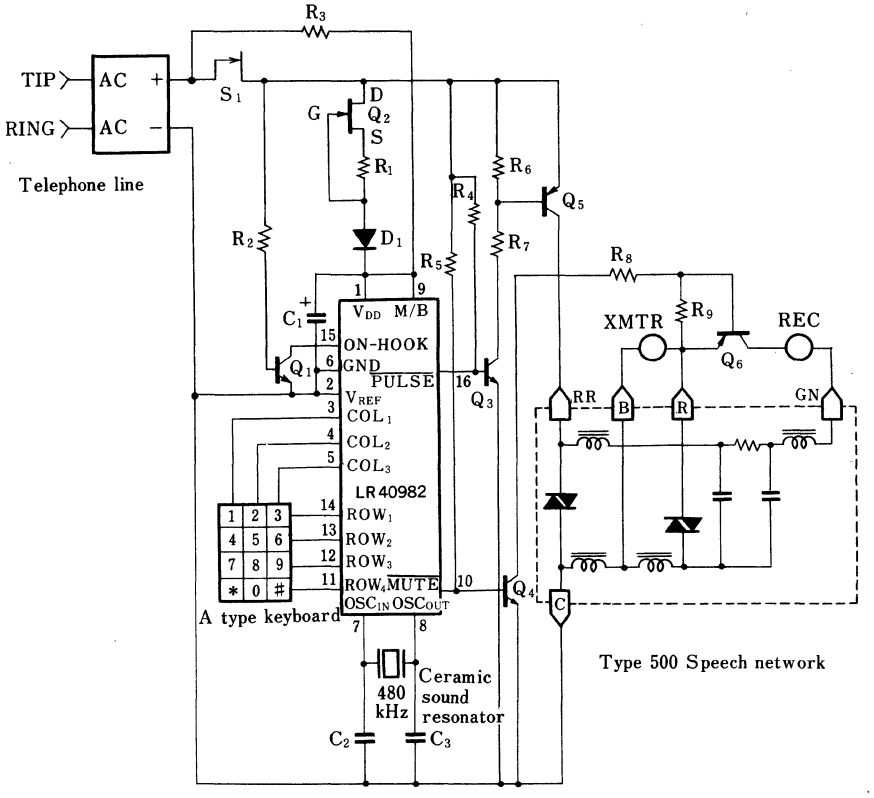
■ Timing Diagram



■ Test Circuit



System Configuration



Q_1, Q_3, Q_4 = 2N5550
Q_5, Q_6 = 2N5401
Q_2 = 2N3822
D_1 = 1N914
C_1 = 20μF (low leakage product)
C_2, C_3 = 100pF ± 20%

R_1 = 8kΩ
R_2 = 500kΩ
R_3 = 22MΩ
R_4, R_5 = 390kΩ
R_6, R_9 = 100kΩ
R_7, R_8 = 3kΩ

LR40991 Pulse Dialer CMOS LSI

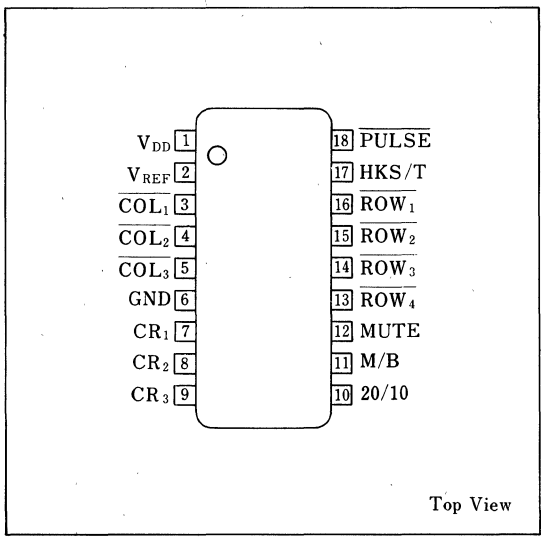
■ Description

The LR40991 is a monolithic CMOS LSI which uses a CR oscillator and provides the features required for a pulse dialer with redial.

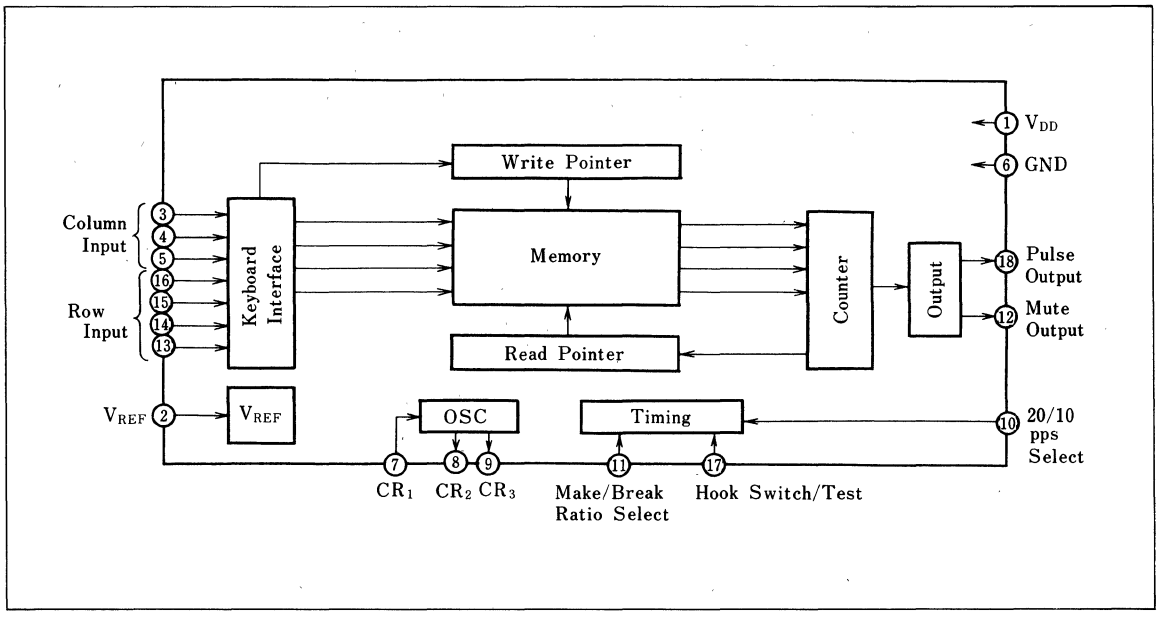
■ Features

1. Direct telephone-line operation
2. Uses 2-of-7 matrix keyboard
3. CMOS process for low-power operation
4. 2.5～6.0V power supply
5. Make/Break ratio pin-selectable
6. 20/10 pps pin-selectable
7. Redial with # or *
8. MUTE output for electronic switching
9. CR oscillator
10. 18-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3～+6.2	V	1
Operating temperature	T_{opr}	−30～+60	℃	
Storage temperature	T_{stg}	−55～+150	℃	
Maximum power consumption	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=25℃.
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	2.5～6.0	V

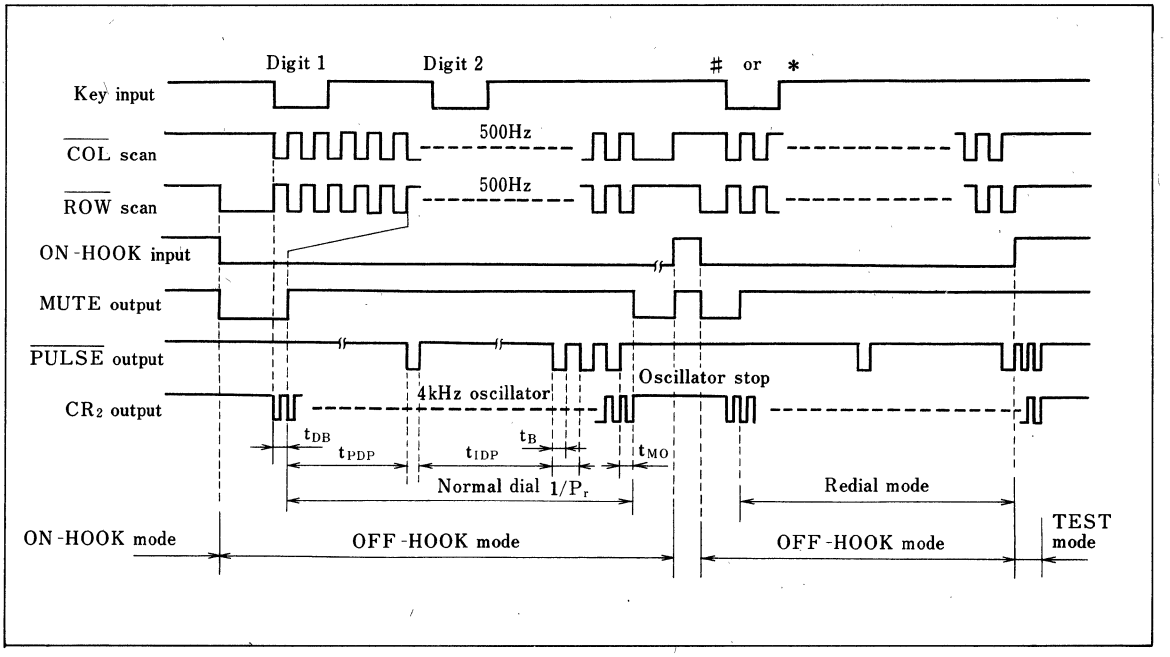
■ Electrical Characteristics

(Ta=−30～+60℃)

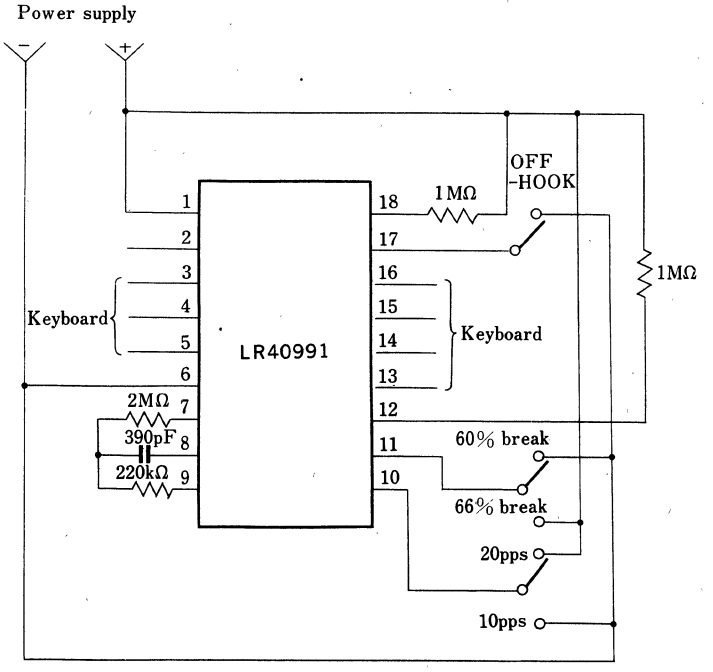
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Key contact resistance	R_{KI}				1	kΩ	
Key board capacity	C_{KI}				30	pF	
Input voltage	K_{IH}	2-of-7 input mode	$0.8V_{DD}$		V_{DD}	V	5
	K_{IL}		GND		$0.2V_{DD}$	V	
MUTE sink current	I_{ML}	V_{DD}=2.5V, V_{OUT}=0.5V	0.5	2.0		mA	6
MUTE source current	I_{MH}	V_{DD}=2.5V, V_{OUT}=2.0V	0.5	2.0		mA	
$\overline{\text{PULSE}}$ sink current	I_P	V_{DD}=2.5V, V_{OUT}=0.5V	1.0			mA	7
V_{REF} output value	V_{REF}	I_{SUPPLY}=150 μA	1.5	2.5	3.5	V	8
Memory hold current	I_{MR}	All outputs in no-load state		0.7		μA	
Operating current	I_{OP}	All outputs in no-load state		100	150	μA	
Key pull-up resistance	K_{IRU}	V_{DD}=6.0V		100		kΩ	
Key pull-down resistance	K_{IRD}	V_{IN}=4.8V		4		kΩ	
ON-HOOK pull-up resistance	R_{OH}			100		kΩ	
MUTE, $\overline{\text{PULSE}}$ output off current	I_{LKG}	V_{DD}=6.0V, V_{OUT}=6.0V		0.001	1	μA	

Note 5 : Applies to key input pins ($\overline{\text{ROW}}_{1\sim4}$, $\overline{\text{COL}}_{1\sim3}$).
Note 6 : Applies to MUTE output pin.
Note 7 : Applies to $\overline{\text{PULSE}}$ output pin.
Note 8 : Applies to V_{REF} pin.

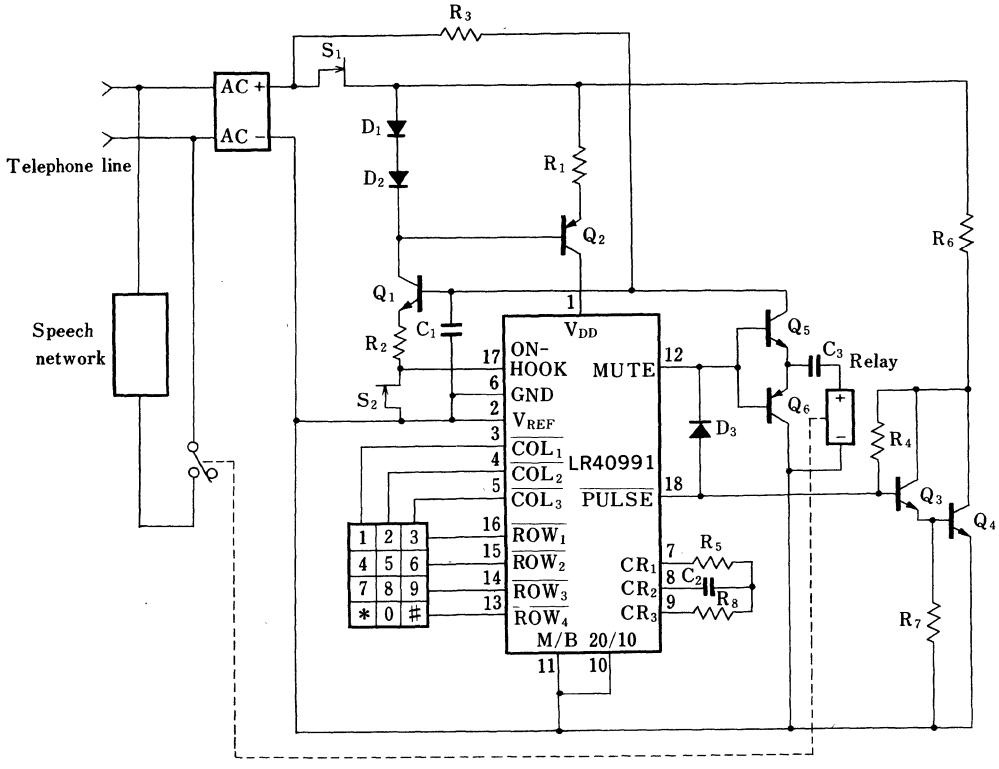
■ Timing Diagram



■ Test Circuit



System Configuration



R_1=2.7kΩ	Q_1=2N5550	C_1=22μF
R_2=75kΩ	Q_2=2N5401	C_2=390pF
R_3=22MΩ	Q_3=2N5550	C_3=10μF
R_4=390kΩ	Q_4=2N5550	D_1=1N914
R_5=2MΩ	Q_5=2N2222	D_2=1N914
R_6=150Ω	Q_6=2N2303	D_3=1N4004
R_7=100kΩ		
R_8=220kΩ	Relay : 1.5V bistable latching	

LR40992 Pulse Dialer CMOS LSI

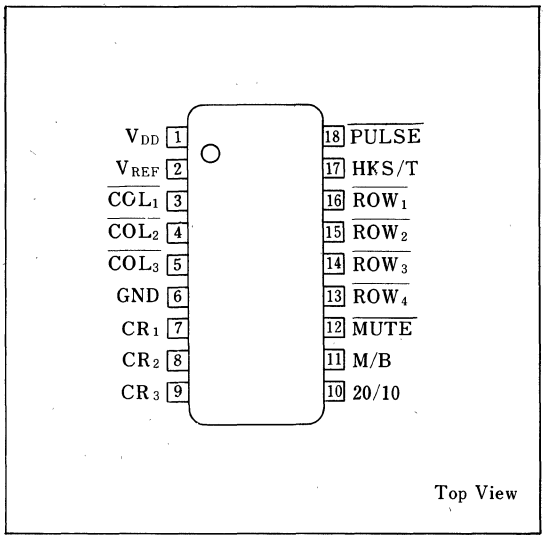
■ Description

The LR40992 is a monolithic CMOS LSI which uses a CR oscillator and provides the features required for a pulse dialer with redial.

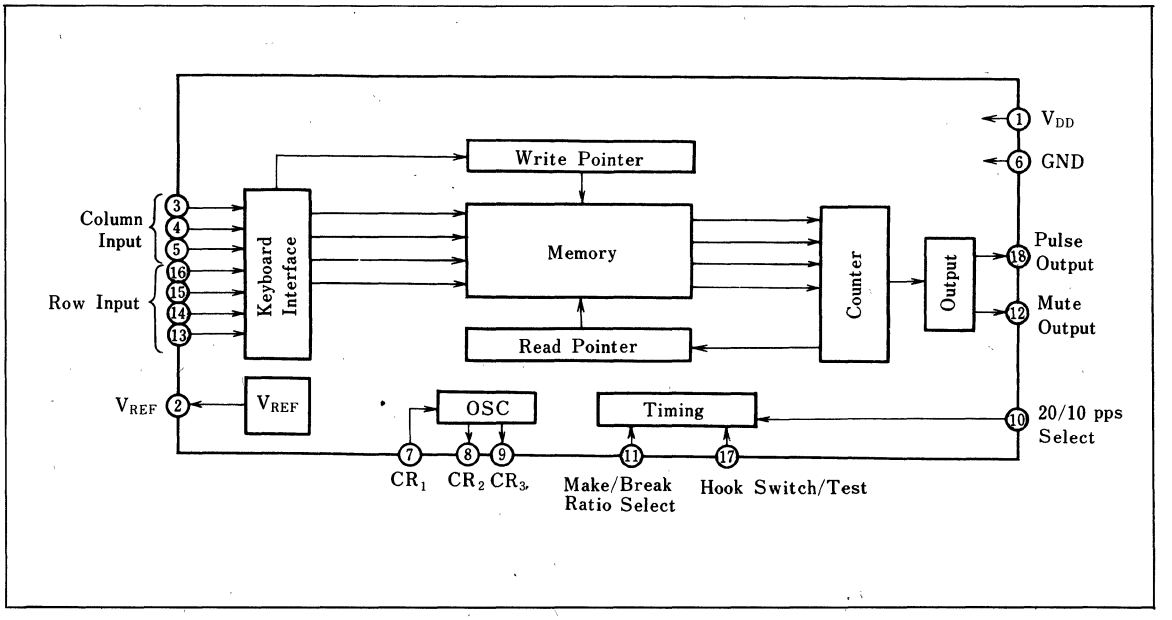
■ Features

1. Direct telephone-line operation
2. Uses 2-of-7 matrix keyboard
3. CMOS process for low-power operation
4. 2.5～6.0V power supply
5. Make/Break ratio pin-selectable
6. 20/10 pps pin-selectable
7. Redial with # or *
8. MUTE output for electronic switching
9. CR oscillator
10. 18-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3～+6.2	V	1
Operating temperature	T_{opr}	−30～+60	℃	
Storage temperature	T_{stg}	−55～+150	℃	
Maximum power consumption	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=25℃.
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Recommended Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	2.5～6.0	V

■ Electrical Characteristics

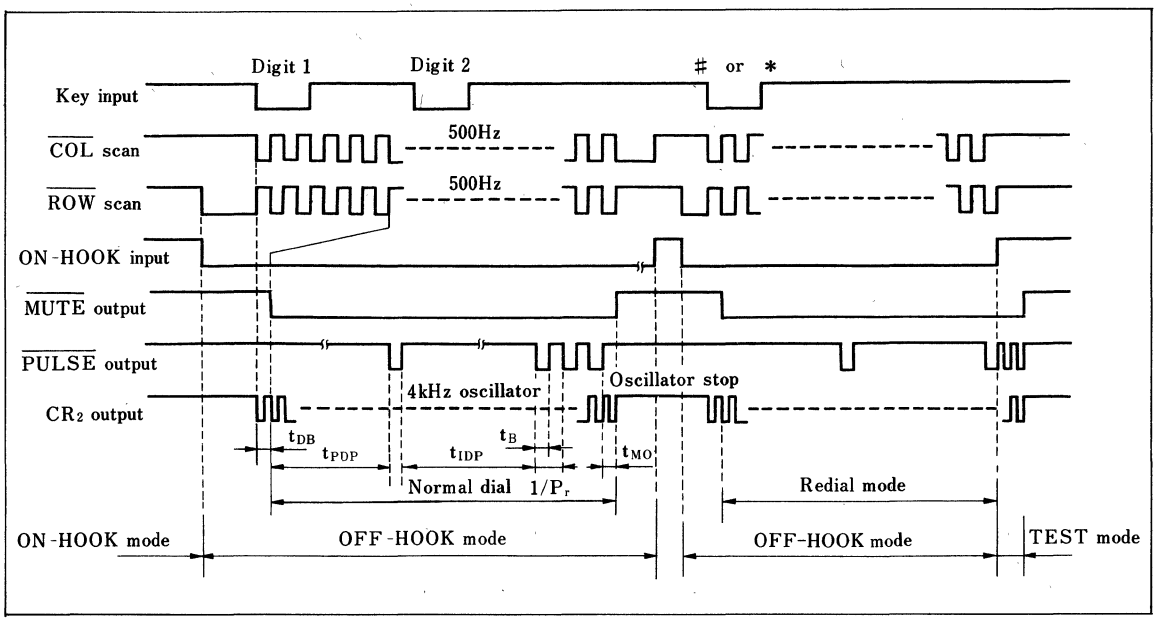
(Ta=−30～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Key contact resistance	R_{KI}				1	kΩ	
Key board capacity	C_{KI}				30	pF	
Input voltage	K_{IH}	2-of-7 input mode	$0.8V_{DD}$		V_{DD}	V	5
	K_{IL}		GND		$0.2V_{DD}$	V	5
Key pull-up resistance	K_{IRU}	V_{DD}=6.0V, V_{IN}=4.8V		100		kΩ	
Key pull-down resistance	K_{IRD}			4		kΩ	
$\overline{\text{MUTE}}$ sink current	I_M	V_{DD}=2.5V, V_{OUT}=0.5V	500			μA	6
Pulse output sink current	I_P		1.0			mA	7
V_{REF} output current	I_{REF}	V_{DD},V_{REF}=6.0V	1.0	7.0		mA	8
Memory hold current	I_{MR}	All outputs in no-load state		0.7		μA	
Operating current	I_{OP}	All outputs in no-load state		100	150	μA	
$\overline{\text{MUTE}}$, $\overline{\text{PULSE}}$ Output off current	I_{LKG}	V_{DD}=6.0V, V_{OUT}=6.0V		0.001	1	μA	6,7

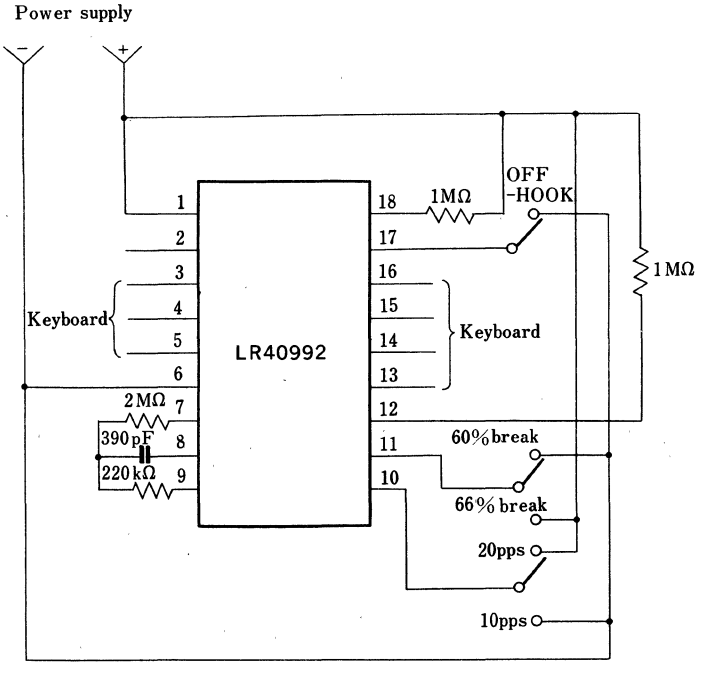
Note 5 : Applies to key input pins ($\overline{RDW_{1-4}}$, $\overline{COL_{1-3}}$)
Note 6 : Applies to $\overline{\text{MUTE}}$ output pin.
Note 7 : Applies to $\overline{\text{PULSE}}$ output pin.
Note 8 : Applies to V_{REF} pin.

9

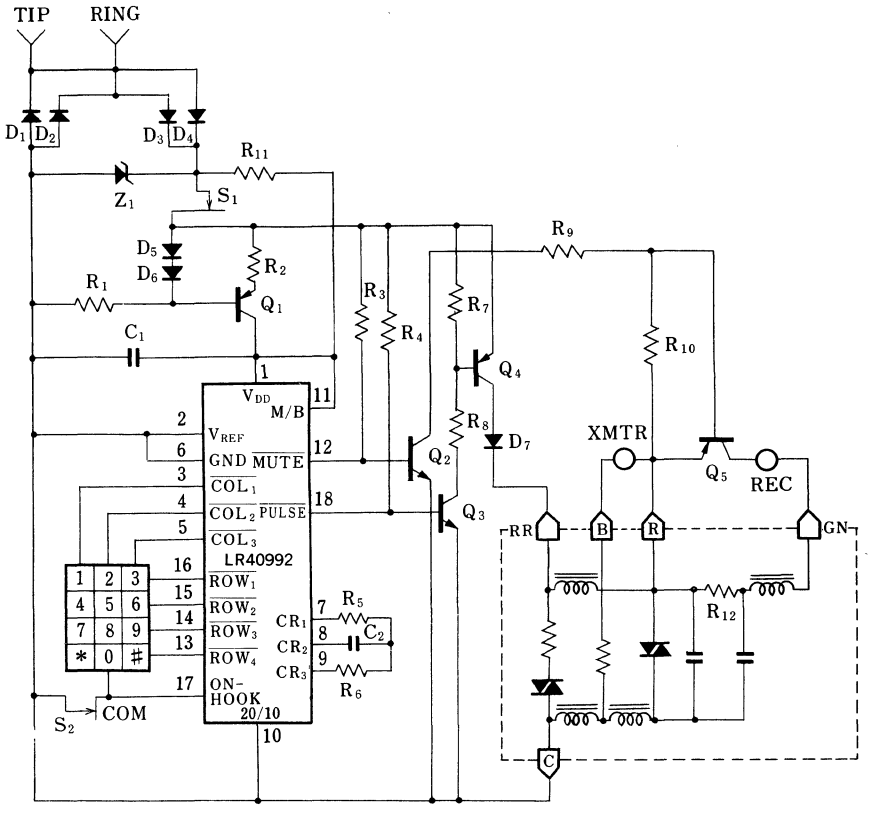
Timing Diagram



Test Circuit



System Configuration



R_1 = 560kΩ
R_2 = 1.4kΩ
R_3 = 470kΩ
R_4 = 330kΩ
R_5 = 2MΩ
R_6 = 220kΩ
R_7 = 100kΩ
R_8 = 3kΩ
R_9 = 3kΩ
R_{10} = 100kΩ
R_{11} = 10MΩ

Q_1 = 2N5401
Q_2 = 2N5550
Q_3 = 2N5550
Q_4 = 2N5401
Q_5 = 2N5401

C_1 = 68 μF
C_2 = 390 pF
Z_1 = 120 volt, 1watt Zener

D_1 = 1N4004
D_2 = 1N4004
D_3 = 1N4004
D_4 = 1N4004
D_5 = 1N914
D_6 = 1N914
D_7 = 1N4004

LR40993 Pulse Dialer CMOS LSI

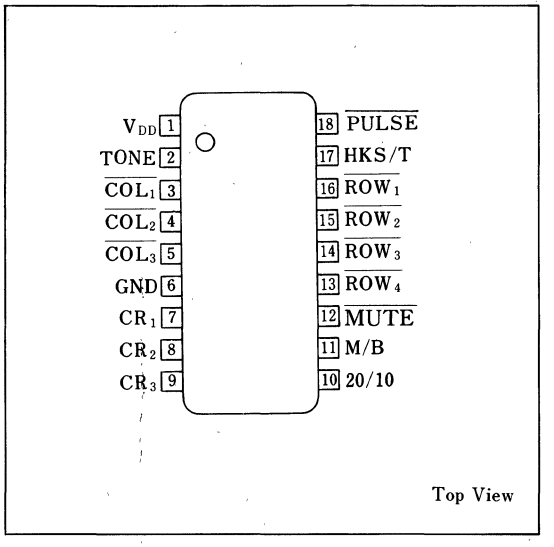
■ Description

The LR40993 is a monolithic CMOS LSI which uses a CR oscillator and provides the features required for a pulse dialer with redial.

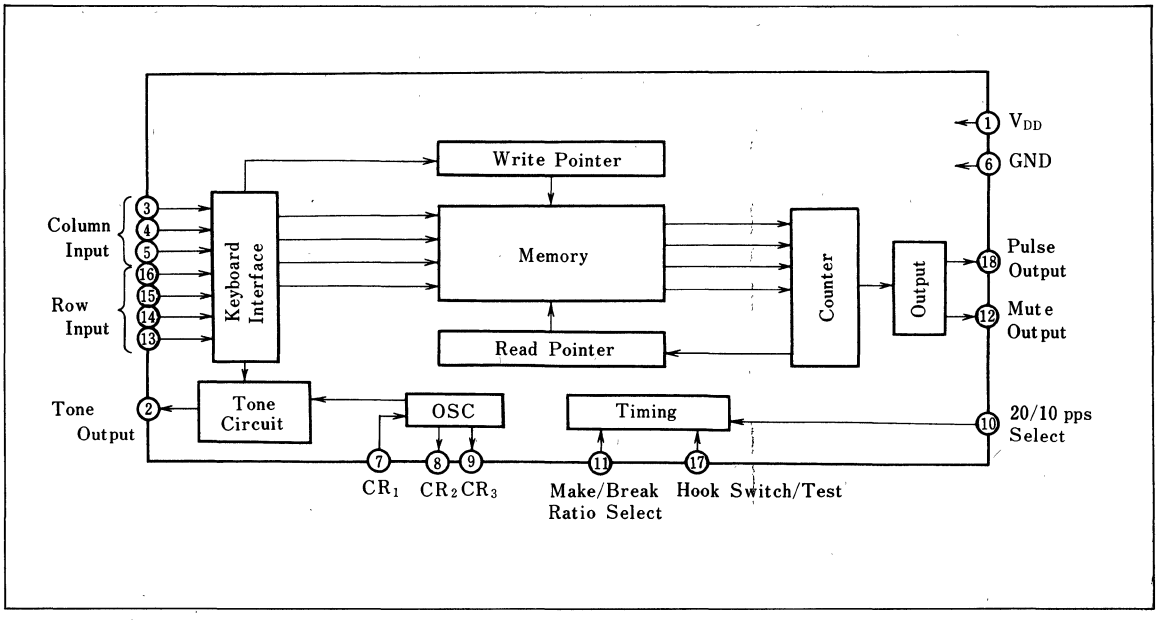
■ Features

1. Direct telephone-line operation
2. Uses 2-of-7 matrix keyboard
3. CMOS process for low-power operation
4. 2.5～6.0V power supply
5. Make/Break ratio pin-selectable
6. 20/10 pps pin-selectable
7. Redial with # or *
8. MUTE output for electronic switching
9. CR oscillator
10. Beep-tone output for key input
11. 18-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3～+6.2	V	1
Operating temperature	T_{opr}	−30～+60	℃	
Storage temperature	T_{stg}	−55～+150	℃	
Maximum power consumption	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=25℃.
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Recommended Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	2.5～6.0	V

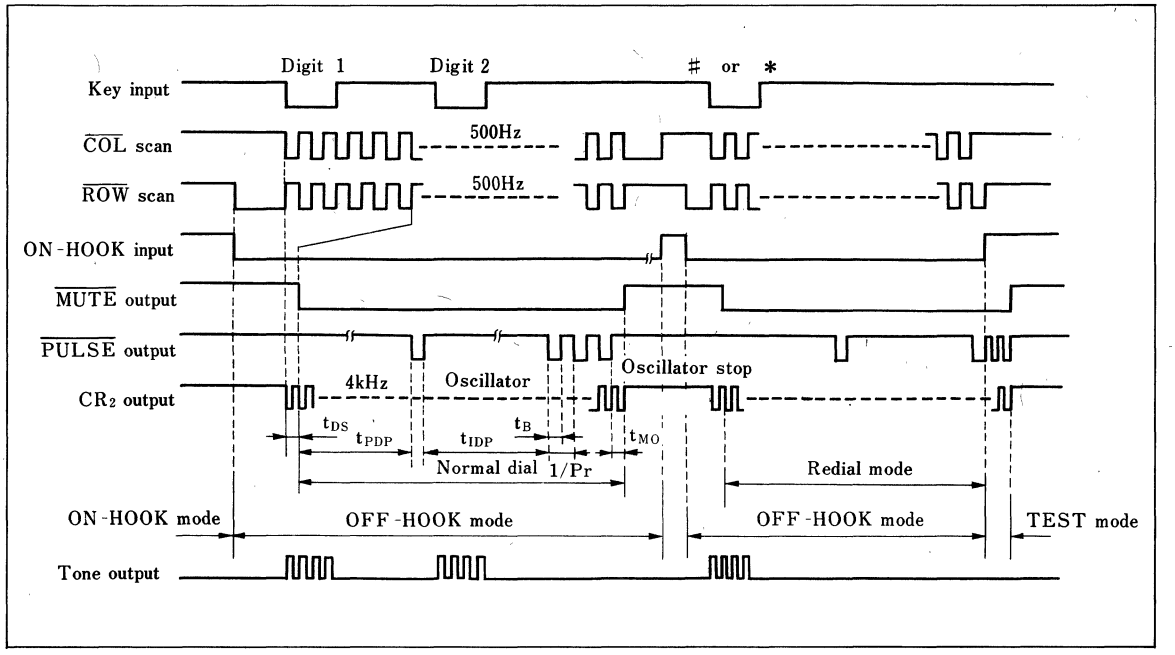
■ Electrical Characteristics

(Ta=−30～+60℃)

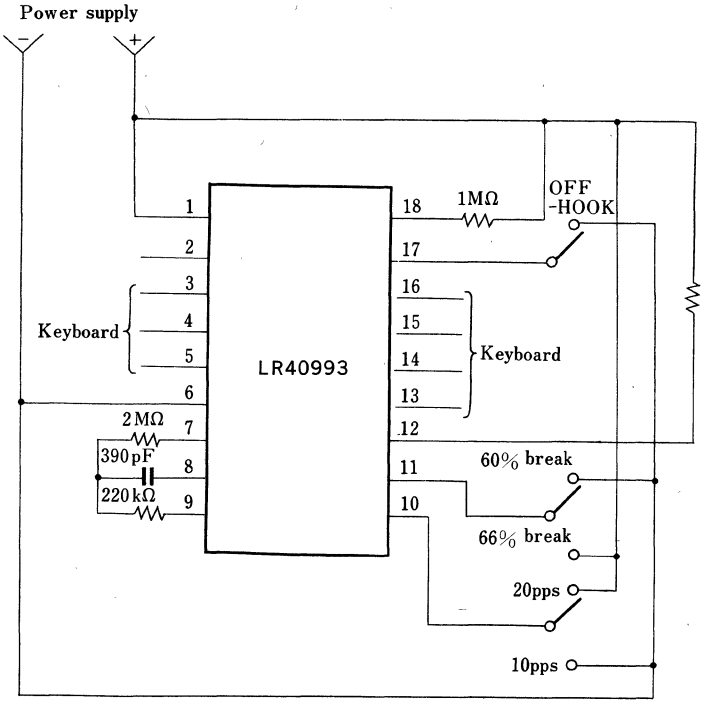
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Key contact resistance	R_{KI}				1	kΩ	
Key board capacity	C_{KI}				30	pF	
Input voltage	K_{IH}	2-of-7 input mode	$0.8V_{DD}$		V_{DD}	V	5
	K_{IL}		GND		$0.2V_{DD}$	V	5
Key pull-up resistance	K_{IRU}	V_{DD}=6.0V, V_{IN}=4.8V		100		kΩ	
Key pull-down resistance	K_{IRD}			4		kΩ	
$\overline{\text{MUTE}}$ sink current	I_M	V_{DD}=2.5V, V_{OUT}=0.5V	500			μA	6
$\overline{\text{Pulse}}$ output sink current	I_P	V_{DD}=2.5V, V_{OUT}=0.5V	1.0			mA	7
TONE output sink current	I_{TL}	V_{DD}=2.5V, V_{OUT}=0.5V	250			μA	8
TONE output source current	I_{TH}	V_{DD}=2.5V, V_{OUT}=V_{DD}−0.5	250			μA	8
Memory hold current	I_{MR}	All outputs in no-load state		0.7		μA	
Operating current	I_{OP}	All outputs in no-load state		100	150	μA	
$\overline{\text{MUTE}}$, $\overline{\text{PULSE}}$ Output off current	I_{LKG}	V_{DD}=6.0V, V_{OUT}=6.0V		0.001	1	μA	6,7

Note 5 : Applies to key input pins ($\overline{ROW}_{1\sim4}$, $\overline{COL}_{1\sim3}$)
Note 6 : Applies to $\overline{\text{MUTE}}$ output pin.
Note 7 : Applies to $\overline{\text{PULSE}}$ output pin.
Note 8 : Applies to TONE pin.

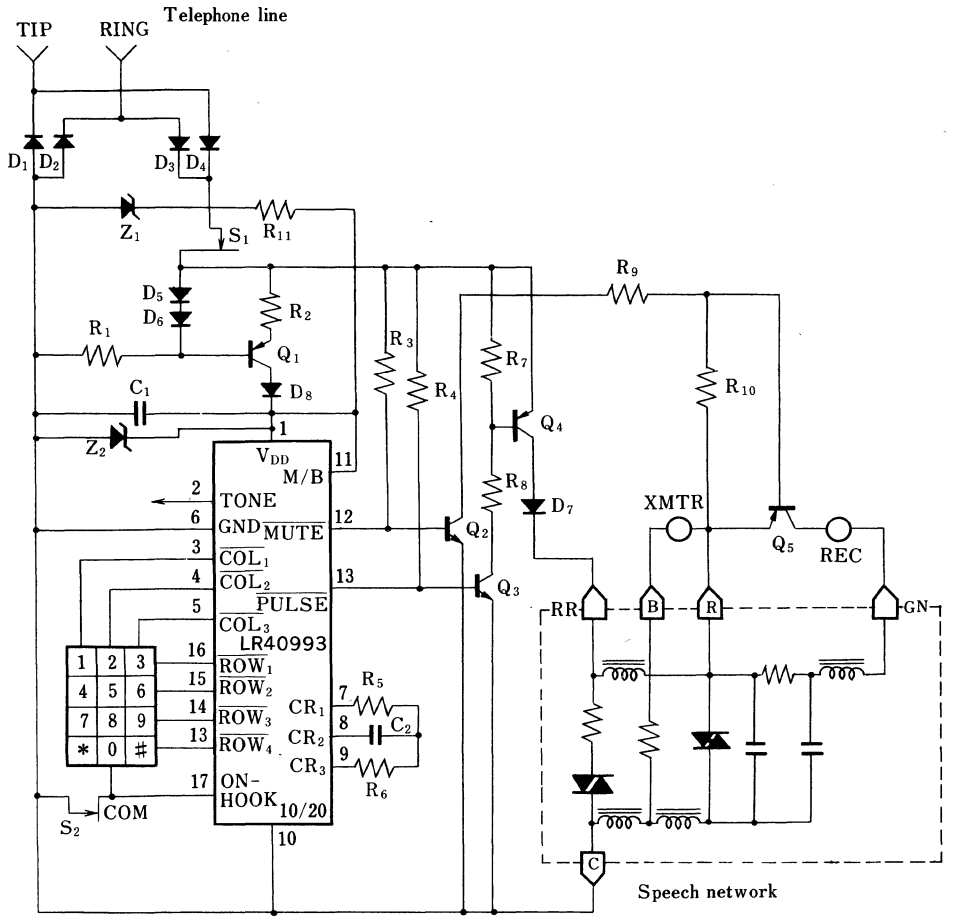
■ Timing Diagram



■ Test Circuit



System Configuration



R_1 = 560kΩ
R_2 = 1.4kΩ
R_3 = 470kΩ
R_4 = 330kΩ
R_5 = 2MΩ
R_6 = 220kΩ
R_7 = 100kΩ
R_8 = 3kΩ
R_9 = 3kΩ
R_{10} = 100kΩ
R_{11} = 10MΩ

Q_1 = 2N5401
Q_2 = 2N5550
Q_3 = 2N5550
Q_4 = 2N5401
Q_5 = 2N5401

D_1 = 1N4004
D_2 = 1N4004
D_3 = 1N4004
D_4 = 1N4004
D_5 = 1N914
D_6 = 1N914
D_7 = 1N4004
D_8 = Zener Diode

C_1 = 68μF
C_2 = 390pF
Z_1, Z_2 = 120V : 1watt Zener Diode

LR40994 Pulse Dialer CMOS LSI

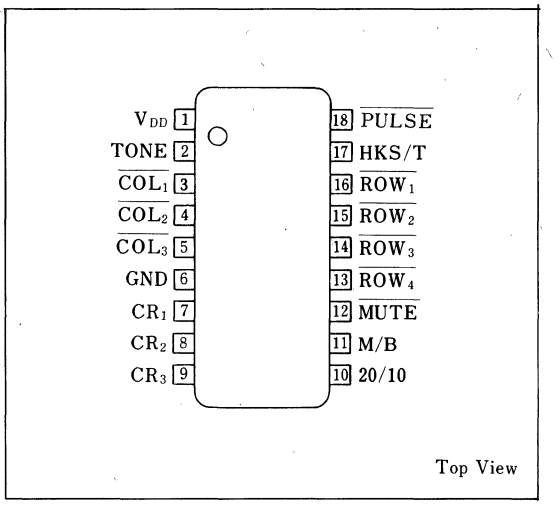
Description

The LR40994 is a monolithic CMOS LSI which uses a CR oscillator and provides the features required for a pulse dialer with redial.

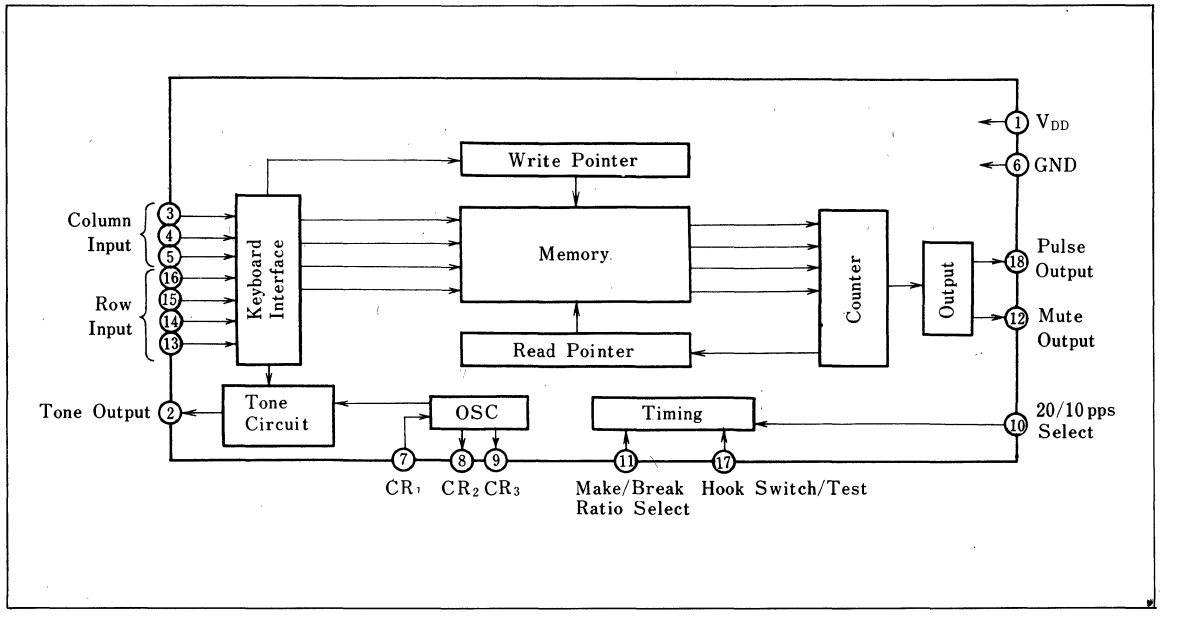
Features

1. Uses 2-of-7 matrix keyboard
2. CMOS process for low-power operation
3. 2.5~6.0V power supply
4. Make/Break ratio pin-selectable
5. 20/10 pps pin-selectable
6. Redial with # or *
7. MUTE output for electronic switching
8. CR oscillator
9. Beep-tone output for key input
10. 18-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3～+6.2	V	1
Operating temperature	T_{opr}	−30～+60	℃	
Storage temperature	T_{stg}	−55～+150	℃	
Maximum power consumption	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=25℃
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

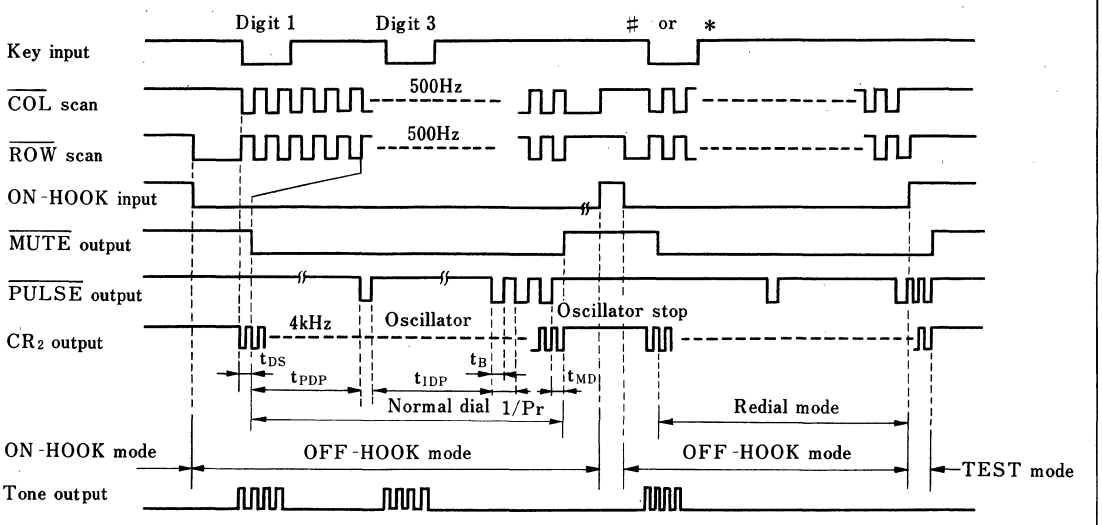
■ Electrical Characteristics

(Ta=−30～+60℃)

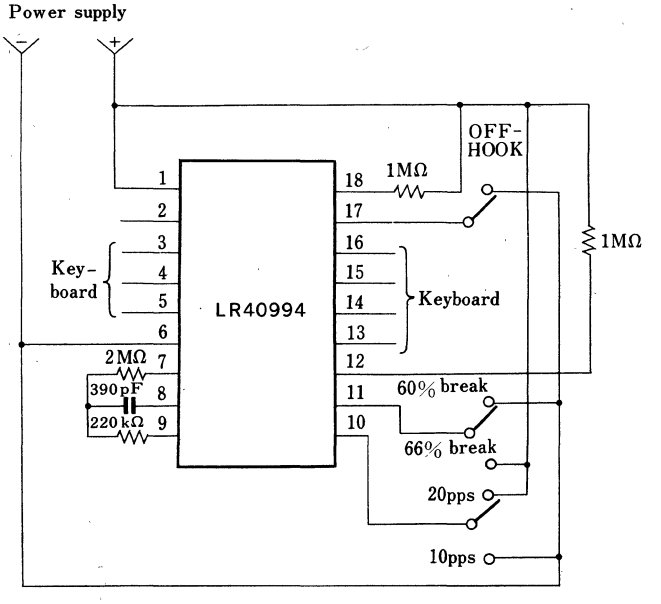
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		2.5		6.0	V	
Key contact resistance	R_{KI}				1	kΩ	
Key board capacity	C_{KI}				30	pF	
Input voltage	K_{IH}	2-of-7 input mode	$0.8V_{DD}$		V_{DD}	V	5
	K_{IL}		GND		$0.2V_{DD}$	V	5
Key pull-up resistance	K_{IRU}	V_{DD}=6.0V, V_{IN}=4.8V		100		kΩ	
Key pull-down resistance	K_{IRD}			4		kΩ	
$\overline{\text{MUTE}}$ sink current	I_M	V_{DD}=2.5V, V_{OUT}=0.5V	500			μA	6
$\overline{\text{PULSE}}$ output sink current	I_P	V_{DD}=2.5V, V_{OUT}=0.5V	1.0			mA	7
TONE output sink current	I_{TL}	V_{DD}=2.5V, V_{OUT}=0.5V	250			μA	8
TONE output source current	I_{TH}	V_{DD}=2.5V, V_{OUT}=V_{DD}−0.5V	250			μA	8
Memory hold current	I_{MR}	All outputs in no-load state		0.7		μA	
Operating current	I_{OP}	All outputs in no-load state		100	150	μA	
$\overline{\text{MUTE}}$, $\overline{\text{PULSE}}$ Output off current	I_{LKG}	V_{DD}=6.0V, V_{OUT}=6.0V		0.001	1	μA	6,7

Note 5 : Applies to key input pins ($\overline{ROW}_{1\sim4}$, $\overline{COL}_{1\sim3}$)
Note 6 : Applies to $\overline{\text{MUTE}}$ output pin.
Note 7 : Applies to $\overline{\text{PULSE}}$ output pin.
Note 8 : Applies to TONE pin.

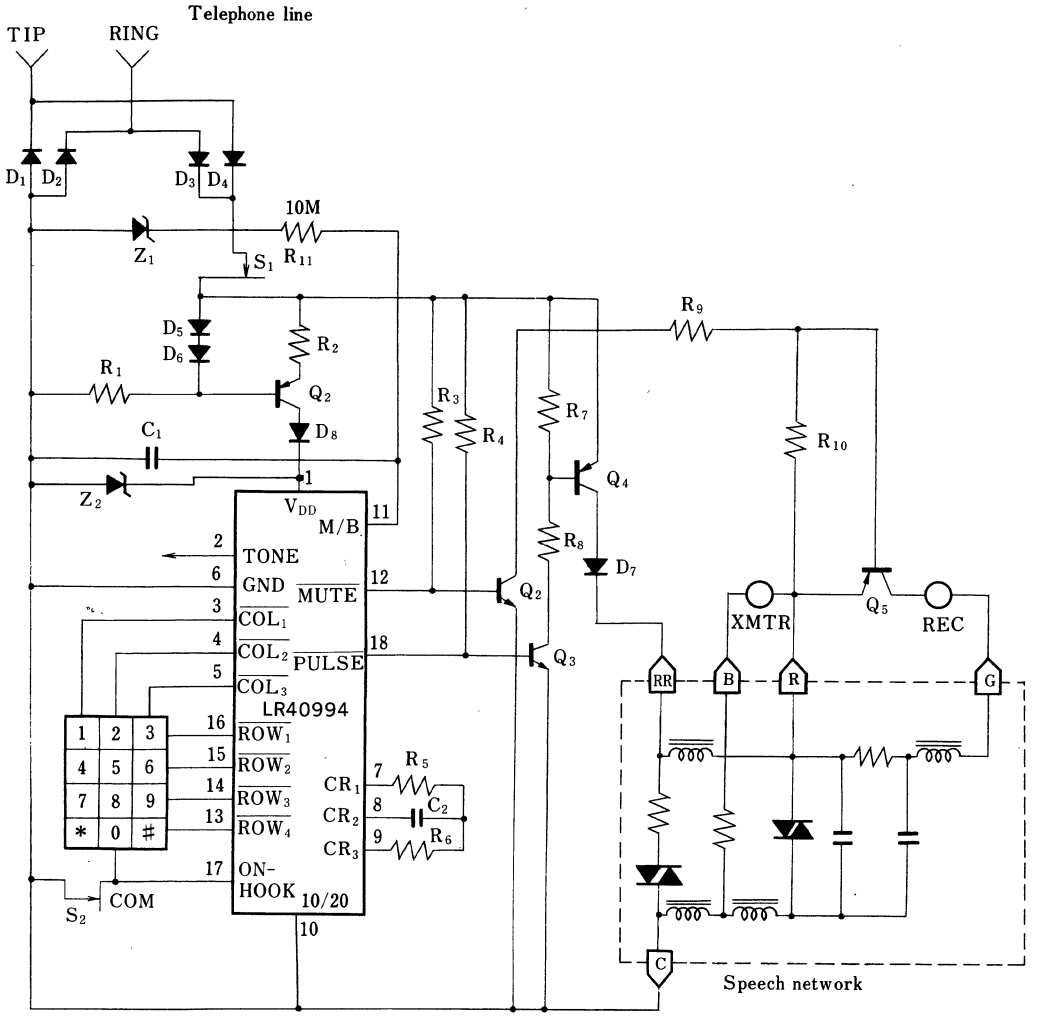
■ Timing Diagram



■ Test Ciruit



■ System Configuration



R_1 = 560kΩ	R_{10} = 100kΩ	D_1 = 1N4004	C_1 = 68μF
R_2 = 1.4kΩ	R_{11} = 10MΩ	D_2 = 1N4004	C_2 = 390 pF
R_3 = 470kΩ		D_3 = 1N4004	Z_1 = 120V, 1-watt Zener Diode
R_4 = 330kΩ	Q_1 = 2N5401	D_4 = 1N4004	Z_2 = 120V, 1-watt Zener Diode
R_5 = 2MΩ	Q_2 = 2N5550	D_5 = 1N914	
R_6 = 220kΩ	Q_3 = 2N5550	D_6 = 1N914	
R_7 = 100kΩ	Q_4 = 2N5401	D_7 = 1N4004	
R_8 = 3kΩ	Q_5 = 2N5401	D_8 = Zener Diode	
R_9 = 3kΩ			

LR4801D Pulse/Tone Dialer CMOS LSI

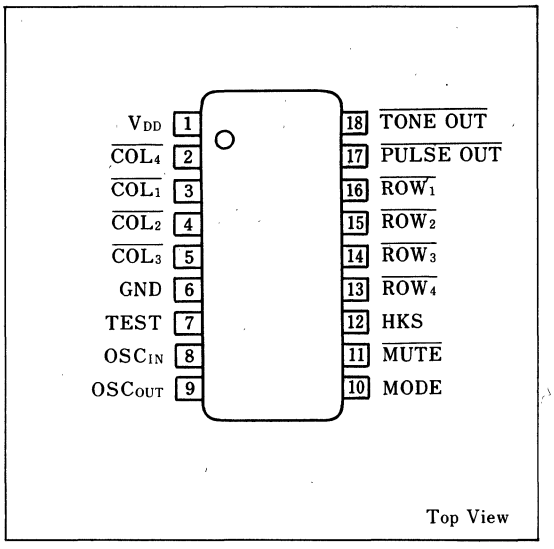
■ Description

The LR4801D is a CMOS LSI for the repertory dialer switchable between tone and pulse dialing with the beep-tone function and ten 18-digit number memory storage.

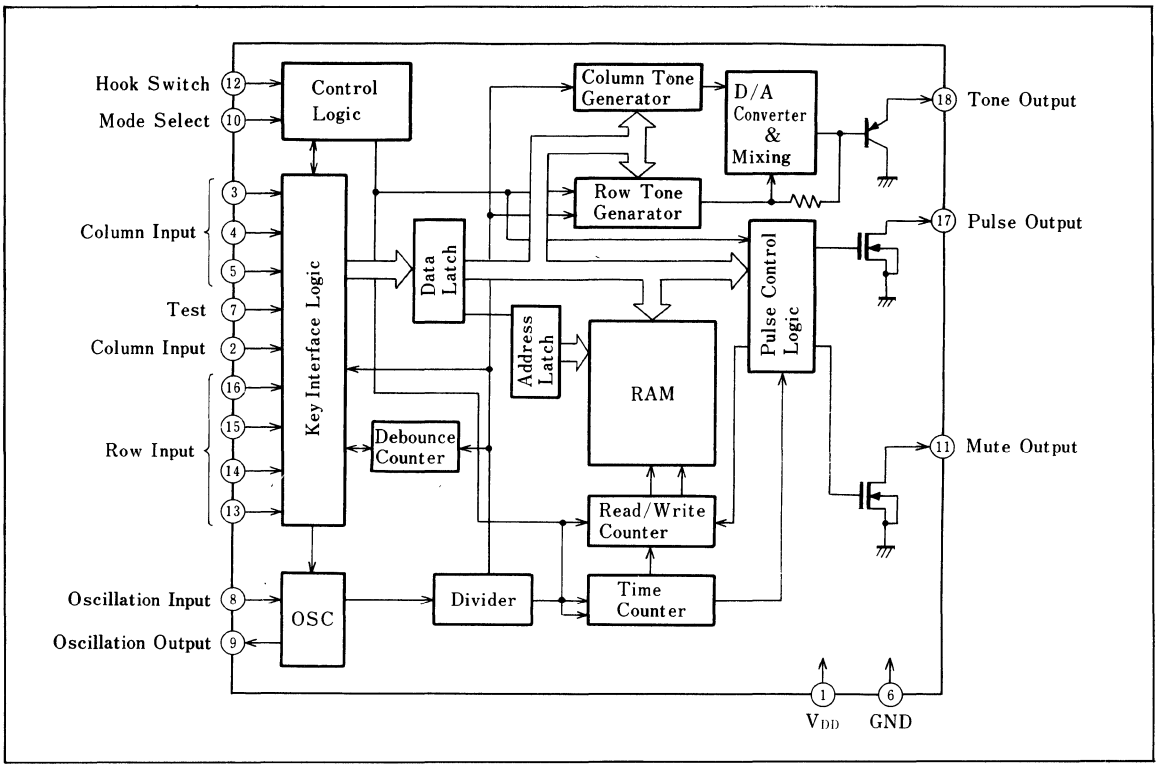
■ Features

1. Switchable between DTMF tone dialing and pulse dialing modes
2. Stores ten 18-digit telephone number memory including a redial memory
3. Beep-tone output for key input
4. PABX pause storage
5. Uses the single contact, the standard 2 of 7 or 2 of 8 matrix keyboard
6. Switchable between 10 pps and 20 pps in pulse dialing mode
7. A 3.579545 MHz color burst crystal can be used for the clock oscillator
8. 18-pin dual-in-line package

■ Pin Connections



Block Diagram



Pin Description

Signal Name	Symbol	I/O	Function
V_{DD}	Power supply		
$\overline{COL_1}$~$\overline{COL_4}$	Key input	I	COL 4-string Key input
$\overline{ROW_1}$~$\overline{ROW_4}$			ROW 4-string key input
GND	Ground		Negative power supply pin
TEST	Test input	I	Pin used for LSI testing
OSC_{IN}	Oscillator connection	I	Connect crystal for color burst
OSC_{OUT}		O	
MODE	Mode select	I	Pin connection / Operating mode: V_{DD} — 20-pps pulse dialer; Open — 10-pps pluse dialer; GND — DTMF tone dialer
$\overline{MUTE}$	Mute output	O	Sending of MUTE signal
HKS	Hook switch input	I	Pin connection / Operating mode: V_{DD} — on-hook mode; Open — off-hook mode; GND — off-hook mode
$\overline{PULSE\ OUT}$	Pulse output	O	Sending of 100pps or 20pps pulse signal
$\overline{TONE\ OUT}$	Tone output	O	Sending of DTMF tone signal or output of beep tone signal: Tone mode — On hook: Beep tone, Off hook: DTMF signal; Pulse mode — On hook: Beep tone, Off hook: Beep tone

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{DD}	10.5	V	1
Input voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V	2
Power consumption	P_D	500	mW	3
Operating temperature	T_{opr}	$-30 \sim +60$	℃	
Storage temperature	T_{opr}	$-55 \sim +150$	℃	

Note 1 : Referenced to GND.
Note 2 : The maximum applicable voltage on any pin with respect to GND.
Note 3 : Ta=25℃

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	2		6	V

■ DC Characteristics

(Ta=25℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage		V_{IL}		GND		$0.2V_{DD}$	V	
		V_{IH}		$0.8V_{DD}$		V_{DD}	V	
Tone output voltage	ROW	V_{OR}	$R_L=1k\Omega$	290	350	450	mV_{Rms}	
	COLUMN	V_{OC}	$R_L=1k\Omega$	380	450	550	mV_{Rms}	
Standby current		I_{SB}	$V_{DD}=3.5V$		3	6	μA	4
Operating current		I_{OP}	$V_{DD}=3.5V$		2	3	mA	5
Mute output current		I_{OL}	$V_{DD}=2V$, $V_{OL}=0.5V$	1	2		mA	6
Pulse sync output current		I_{PL}	$V_{DD}=2V$, $V_O=0.5V$	1			mA	
Pulse leakage output current		$\lvert I_{LKG} \rvert$	$V_{DD}=6V$, $V_O=6V$			1	μA	
Key pull-up input resistance		R_{KP}	$V_{DD}=3.5V$		100		$k\Omega$	7
Key pull-down input resistance		R_{KD}	$V_{DD}=3.5V$		5		$k\Omega$	7
Mode pull-up input resistance		R_{MP}	$V_{DD}=3.5V$		100		$k\Omega$	
Mode pull-down input resistance		R_{MD}	$V_{DD}=3.5V$		100		$k\Omega$	
HKS pull-up input resistance		R_{HK}	$V_{DD}=3.5V$		60		$k\Omega$	
Tone output distortion			$V_{DD} \geqq 4V$, $R_L=1k\Omega$			−20	dB	8
Pre-emphasis		PE_{HB}	$V_{DD} \geqq 4V$, $R_L=1k\Omega$	1	2	3	dB	

Note 4 : All output pins in no-load condition when clock is stopped and when on hook.
Note 5 : All output pins in no-load condition during key input and when on hook/off hook.
Note 6 : Applied to the $\overline{\text{MUTE}}$ pin.
Note 7 : Resistance when $\overline{\text{ROW}}$ pin or $\overline{\text{COL}}$ pin is 125 Hz and is scanned at high or low level.
Note 8 : Unwanted frequency component corresponding to the total power of the fundamental tone signal of the $\overline{\text{ROW}}$ pin and $\overline{\text{COL}}$ pin.

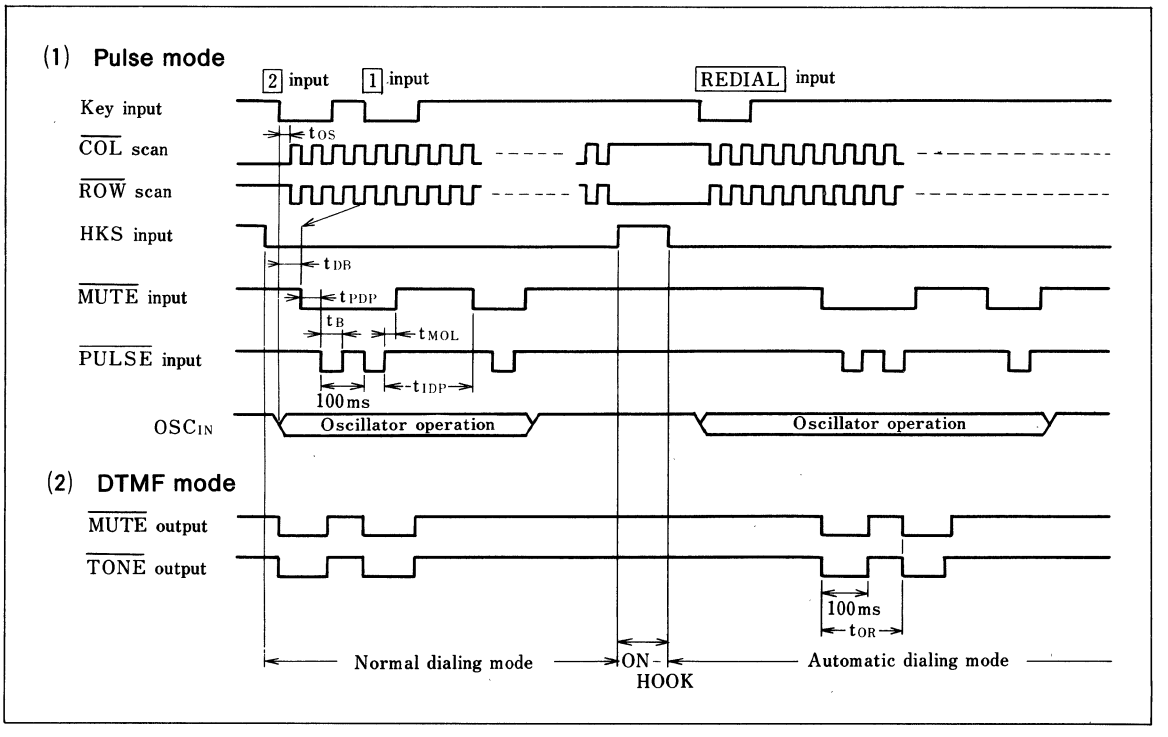
■ AC Characteristics

(Ta=25℃)

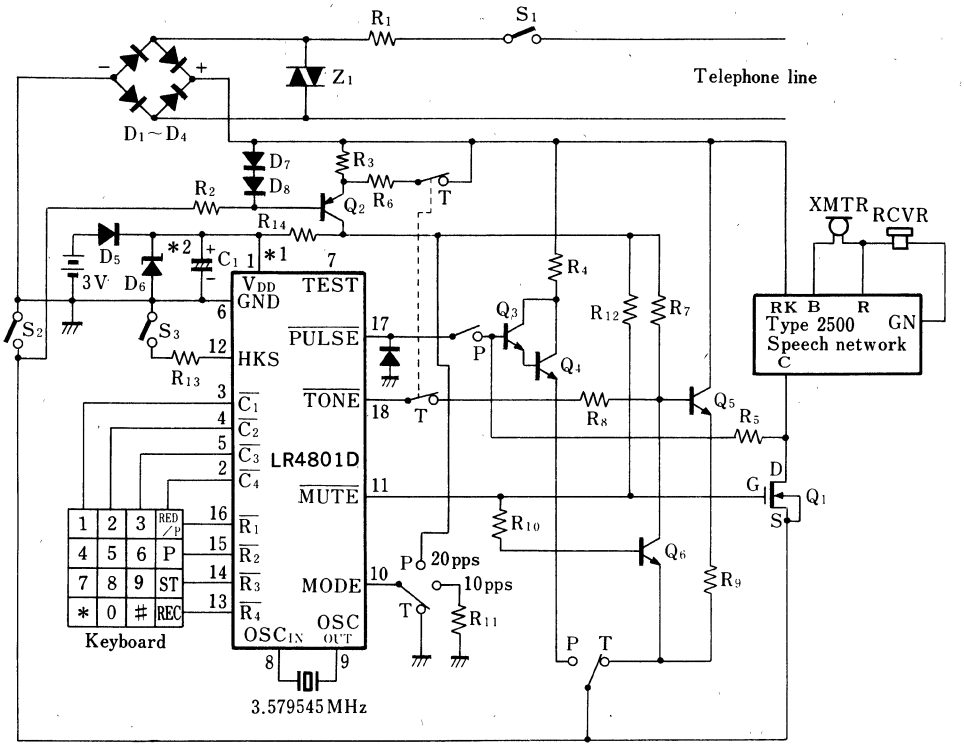
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Oscillation start time	t_{OS}			8	ms	9
Key debounce time	t_{DB}	4		32	ms	10
Pulse rate	P_R		10		pps	11
			20		pps	12
Break time	t_B		60		ms	13
Interdigital pause time	t_{IDP}		1000		ms	13 14
Mute overlap time	t_{MOL}		2	4	ms	
Predigital pause time	t_{PDP}		40		ms	13
Tone output rate	T_{OR}		220		ms	

Note 9 : When crystal oscillation element with characteristics Rs=100Ω, Im=96mH, Cm=0.02pF, Ch=5pF, f=3.579545 MHz is used.
Note 10 : Key input is accepted after oscillation begins if valid after tDB.
Note 11 : Opens the MODE pin.
Note 12 : Connects the MODE pin to VDD.
Note 13 : During 10-pps pulse mode (1/2 during 20-pps mode).
Note 14 : 100 msec during DTMF mode.

■ Timing Diagram



■ System Configuration (tone mode connection example)



Connect to P for pulse mode
Connect to T for tone mode

Z_1 =10DK820
R_1 =22Ω1W
R_2 =560kΩ
R_3 =1.5kΩ
R_4 =150Ω
R_5 =270kΩ
R_6 =51Ω
R_7 =5kΩ
R_8 =100Ω
R_9 =200Ω
R_{10}=100kΩ
R_{11}=1MΩ
R_{12}=10kΩ
R_{13}=470Ω
*1 R_{14}=39Ω
*2 C_1=68μF (Must be input to smooth the power supply and prevent latch up.)

Q_1=2N6660
Q_2=2N5401
Q_3=2N5550
Q_4=2N5550
Q_5=2N5550
Q_6=2N5550
S_1, S_2, S_3=Hook switch
D_1~D_4=1N4004
D_5=1N270
D_6=1N752 (5.6V)
D_7=1N914
D_8=1N914

LR4802 Pulse / Tone Dialer CMOS LSI

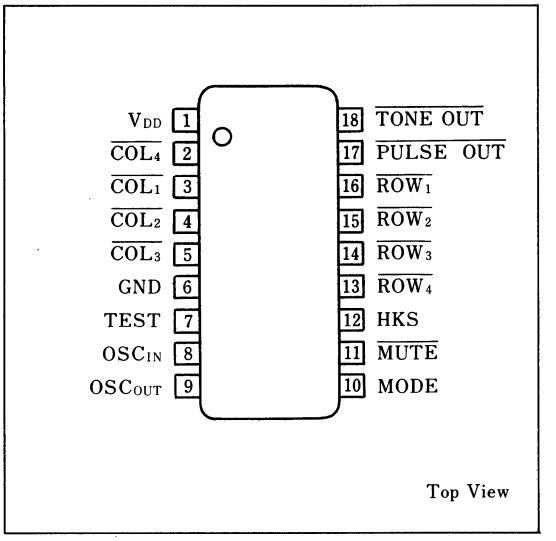
Description

The LR4802 is a CMOS LSI for the repertory dialer switchable between tone and pulse dialing (make/break ratio : 32%/68%) with ten 18-digit number memory storage.

Features

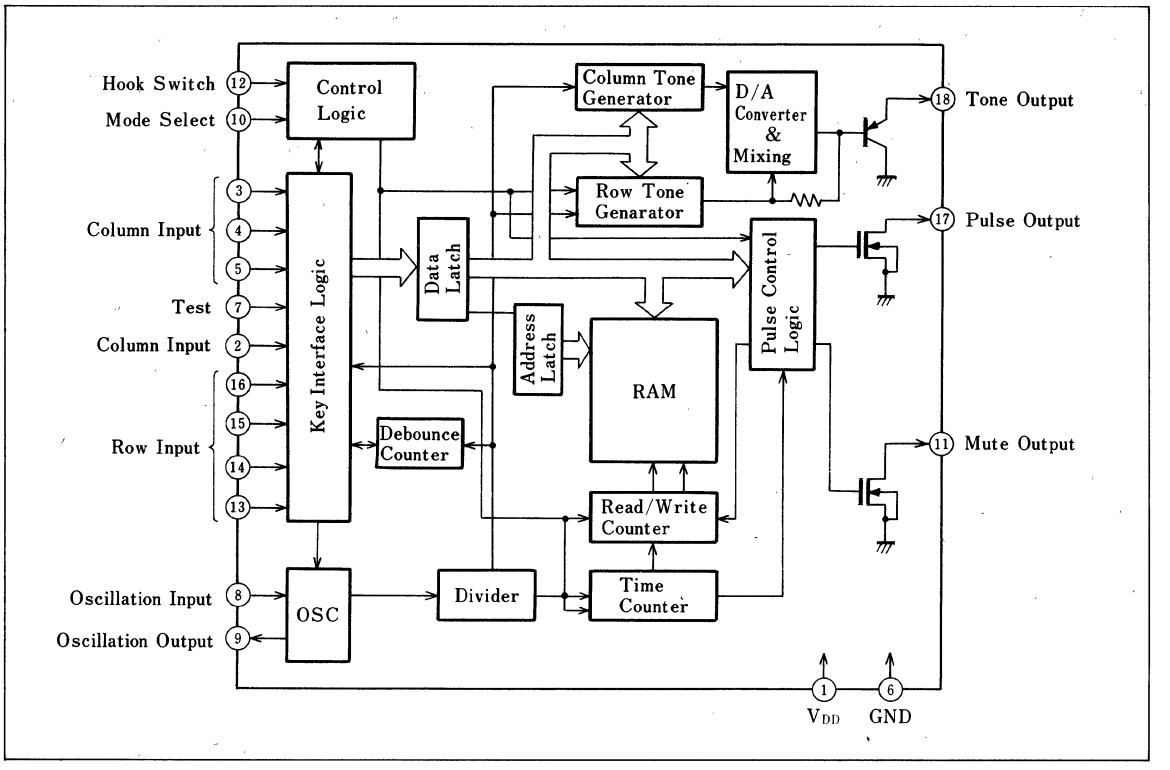
1. Switchable between DTMF tone dialing and pulse dialing modes
2. Stores ten 18-digit telephone number memory including a redial memory
3. PABX pause storage
4. Uses the single contact, the standard 2 of 7 or 2 of 8 matrix keyboard
5. Make/Break ratio : 32%/68%
6. Switchable between 10 pps and 20 pps in pulse dialing mode
7. A 3.579545MHz color burst crystal can be used for the clock oscillator
8. 18-pin dual-in-line package

Pin Connections



Top View

Block Diagram



Pin Description

Signal Name	Symbol	I/O	Function
V_{DD}	Power supply		
$\overline{COL_1}$~$\overline{COL_4}$	Key input	I	COL 4-string key input
$\overline{ROW_1}$~$\overline{ROW_4}$			ROW 4-string key input
GND	Ground		Negative power supply pin.
TEST	Test input	I	Pin used for LSI testing
OSC_{IN}	Oscillator connection	I	Connect crystal for color burst
OSC_{OUT}		O	
MODE	Mode select	I	Pin connection / Operating mode: V_{DD} — 20-pps pulse dialer; Open — 10-pps dialer; GND — DTMF tone dialer
$\overline{MUTE}$	Mute output	O	Sending of MUTE signal
HKS	Hook switch input	I	Pin connection / Operating mode: V_{DD} — On-hook mode; Open — On-hook mode; GND — Off-hook mode
$\overline{PULSE\ OUT}$	Pulse output	O	Sending 100pps or 20pps pulse signal.
$\overline{TONE\ OUT}$	Tone output	O	Sending of DTMF tone signal.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	10.5	V	1
Input voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V	2
Power consumption	P_D	500	mW	3
Operating temperature	T_{opr}	$-30 \sim +60$	℃	
Storage temperature	T_{opr}	$-55 \sim +150$	℃	

Note 1 : Referenced to GND.
Note 2 : The maximum applicable voltage on any pin with respect to GND.
Note 3 : Ta=25℃

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	2		6	V

■ DC Characteristics

(Ta=25℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage		V_{IL}		GND		$0.2V_{DD}$	V	
		V_{IH}		$0.8V_{DD}$		V_{DD}	V	
Tone output voltage	ROW	V_{OR}	$R_L=1k\Omega$	290	350	450	mV_{rms}	
	COLUMN	V_{OC}	$R_L=1k\Omega$	380	450	550	mV_{rms}	
Standby current		I_{SB}	$V_{DD}=3.5V$		3	6	μA	4
Operating current		I_{OP}	$V_{DD}=3.5V$		2	3	mA	5
Mute output current		I_{OL}	$V_{DD}=2V$, $V_{OL}=0.5V$	1.0	2.0		mA	6
Pulse sync output current		I_{PL}	$V_{DD}=2V$, $V_O=0.5V$	1.0			mA	
Pulse leakage output current		$\lvert I_{LKG} \rvert$	$V_{DD}=6V$, $V_O=6V$			1.0	μA	
Key pull-up input resistance		R_{KP}	$V_{DD}=3.5V$		100		$k\Omega$	7
Key pull-down input resistance		R_{KD}	$V_{DD}=3.5V$		5.0		$k\Omega$	7
Mode pull-up input resistance		R_{MP}	$V_{DD}=3.5V$		100		$k\Omega$	
Mode pull-down input resistance		R_{MD}	$V_{DD}=3.5V$		100		$k\Omega$	
HKS pull-up input resistance		R_{HK}	$V_{DD}=3.5V$		60		$k\Omega$	
Tone output distortion			$V_{DD} \geqq 4V$, $R_L=1k\Omega$			-20	dB	8
Pre-emphasis		PE_{HB}	$V_{DD} \geqq 4V$, $R_L=1k\Omega$	1.0	2.0	3.0	dB	

Note 4 : All output pins in no-load condition when clock is stopped and when on hook.
Note 5 : All output pins in no-load condition during key input and when on hook/off hook.
(upper row: during pulse mode, lower row: during tone mode)
Note 6 : Applied to the MUTE pin.
Note 7 : Resistance when ROW pin or COL pin is 125 Hz and is scanned at high or low level.
Note 8 : Unwanted frequency component corresponding to the total power of the fundamental tone signal of the ROW pin and COL pin.

9

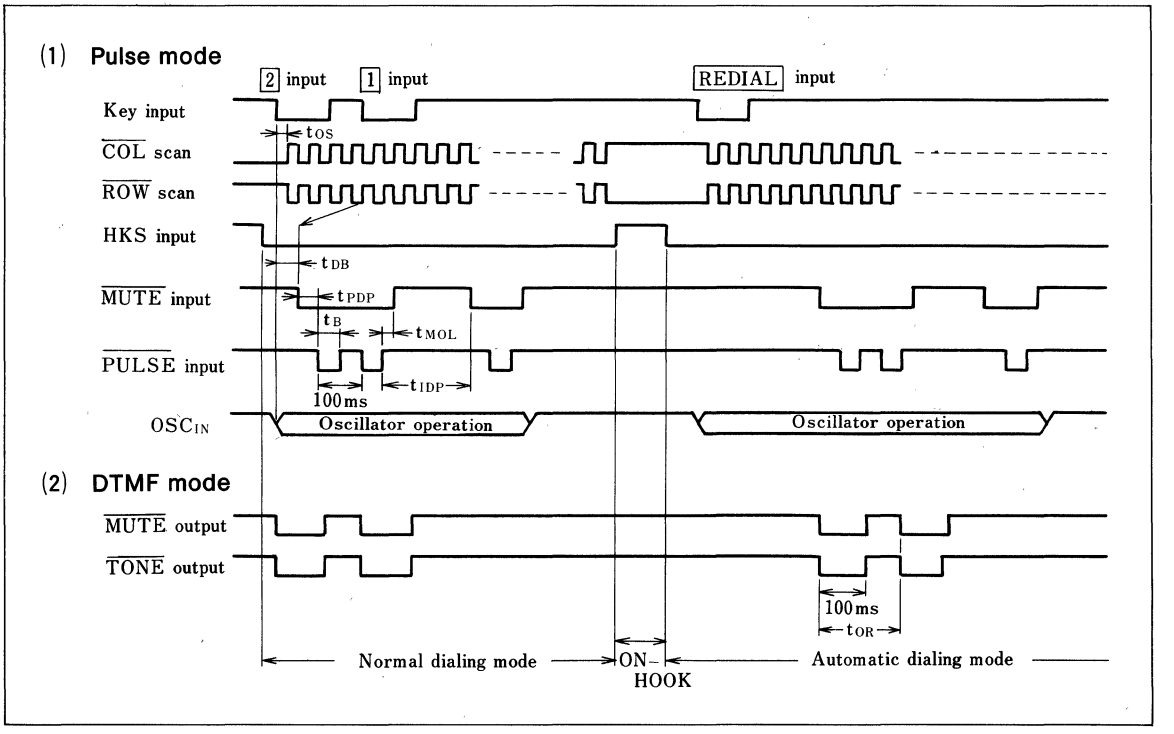
■ AC Characteristics

(Ta=25℃)

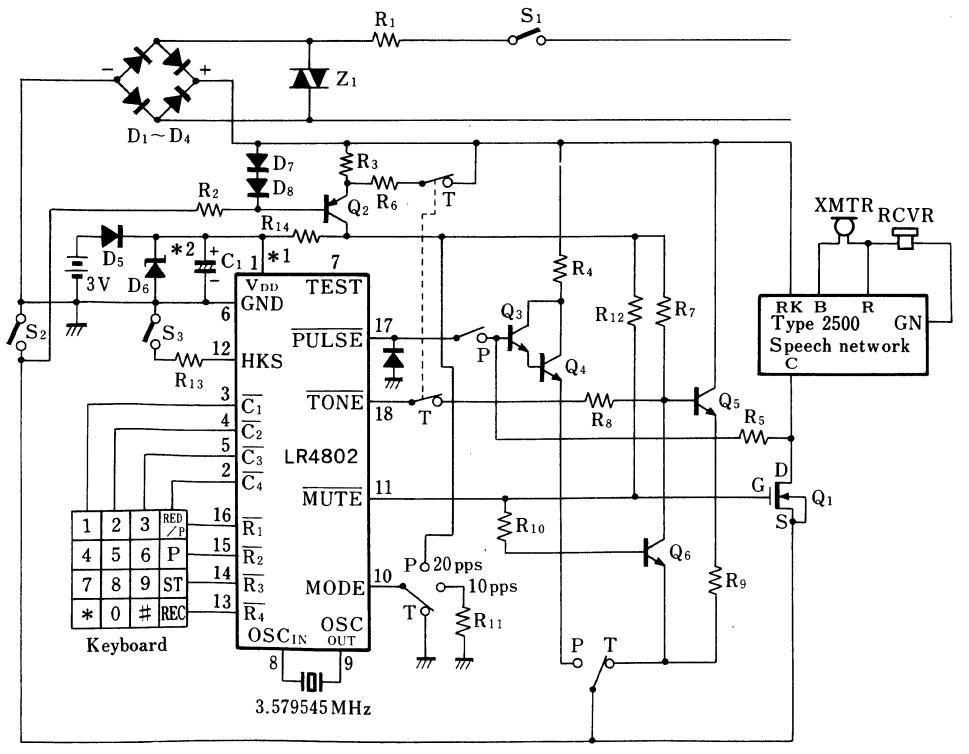
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Oscillation start time	tos			8	ms	9
Key debounce time	t_{DB}	4		32	ms	10
Pulse rate	P_R		10		pps	11
			20			12
Break time	t_B		68		ms	13
Interdigital pause time	t_{IDP}		1000		ms	13 14
Mute overlap time	t_{MOL}		2	4	ms	
Predigital pause time	t_{PDP}		40		ms	13
Tone output rate	t_{OR}		220		ms	

Note 9 : When crystal oscillation element with characteristics Rs=100Ω, Lm=96mH, C_m=0.02pF, C_h=5pF, f=3.579545 MHz is used.
Note 10 : Key input is accepted after oscillation begins if valid after t_{DB}.
Note 11 : Opens the MODE pin.
Note 12 : Connect the MODE pin to V_{DD}.
Note 13 : During 10-pps pulse mode (1/2 during 20-pps mode).
Note 14 : 100 ms during DTMF mode.

■ Timing Diagram



■ System Configuration (tone mode connection example)



Connect to P for pulse mode
Connect to T for tone mode

Z_1 = 10DK820	Q_1 = 2N6660
R_1 = 22Ω 1W	Q_2 = 2N5401
R_2 = 560kΩ	Q_3 = 2N5550
R_3 = 1.5kΩ	Q_4 = 2N5550
R_4 = 150Ω	Q_5 = 2N5550
R_5 = 270kΩ	Q_6 = 2N5550
R_6 = 51Ω	S_1, S_2, S_3 = Hook switch
R_7 = 5kΩ	D_1~D_4 = 1N4004
R_8 = 100Ω	D_5 = 1N270
R_9 = 200Ω	D_6 = 1N752 (5.6V)
R_{10} = 100kΩ	D_7 = 1N914
R_{11} = 1MΩ	D_8 = 1N914
R_{12} = 10kΩ	
R_{13} = 470Ω	

*1 R_{14} = 39Ω

* $2C_1$ = 68μF (Must be input to smooth the power supply and prevent latch up.)

LR4803 Pulse / Tone Dialer CMOS LSI

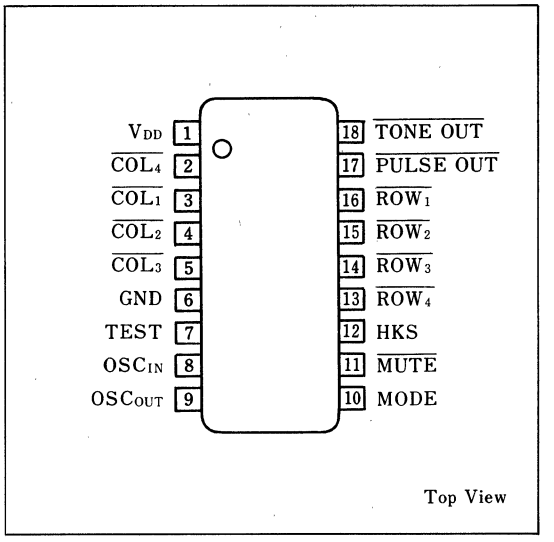
Description

The LR4803 is a CMOS LSI for the repertory dialer switchable between tone and pulse dialing (make/break ratio : 40%/60%) with ten 18-digit number memory storage.

Features

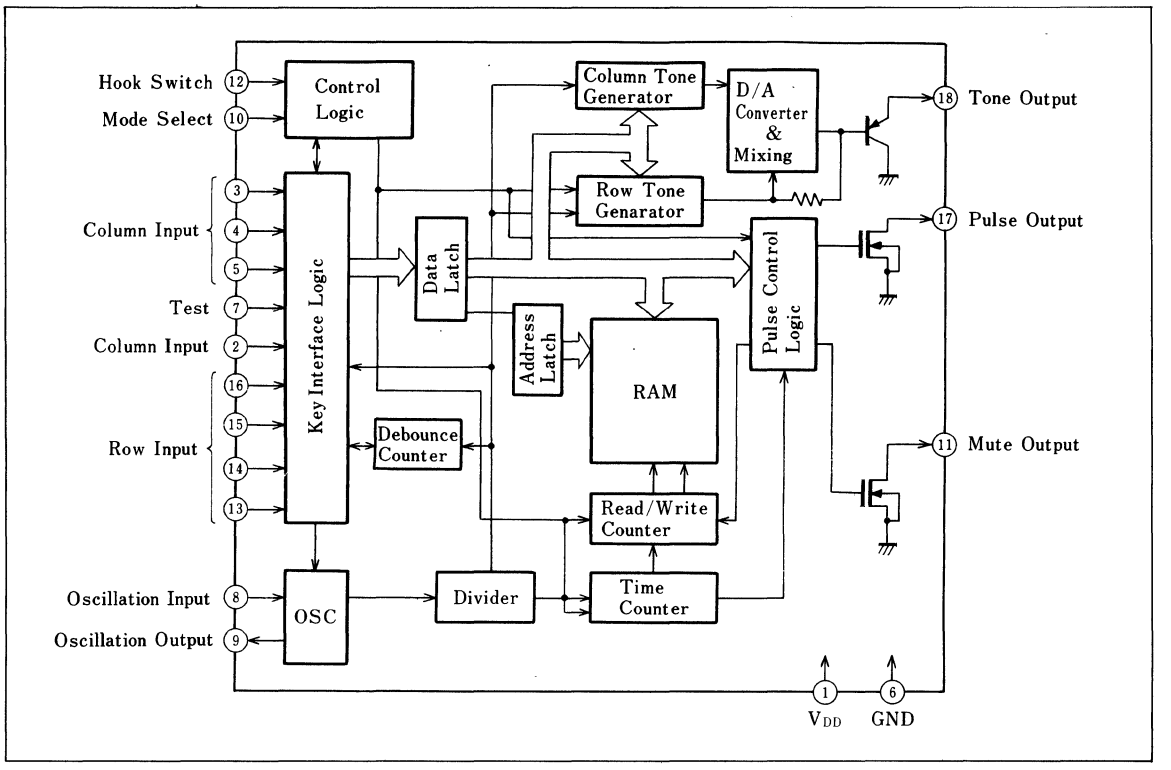
1. Switchable between DTMF tone dialing and pulse dialing modes
2. Stores ten 18-digit telephone number memory including a redial memory
3. PABX pause storage
4. Uses the single contact, the standard 2 of 7 or 2 of 8 matrix keyboard
5. Make/Break ratio : 40%/60%
6. Switchable between 10 pps and 20 pps in pulse dialing mode
7. A 3.579545MHz color burst crystal can be used for the clock oscillator
8. 18-pin dual-in-line package

Pin Connections



Top View

Block Diagram



Pin Description

Signal Name	Symbol	I/O	Function
V_{DD}	Power supply		
$\overline{COL_1}$~$\overline{COL_4}$	Key input	I	COL 4-string key input
$\overline{ROW_1}$~$\overline{ROW_4}$			ROW 4-string key input
GND	Ground		Negative power supply pin.
TEST	Test input	I	Pin used for LSI testing
OSC_{IN}	Oscillator connection	I	Connect crystal for color burst
OSC_{OUT}		O	
MODE	Mode select	I	Pin connection / Operating mode: V_{DD} — 20-pps pulse dialer; Open — 10-pps pulse dialer; GND — DTMF tone dialer
$\overline{MUTE}$	Mute output	O	Sending of MUTE signal
HKS	Hook switch input	I	Pin connection / Operating mode: V_{DD} — On-hook mode; Open — On-hook mode; GND — Off-hook mode
$\overline{PULSE\ OUT}$	Pulse output	O	Sending of 100pps or 20pps pulse signal
TONE OUT	Tone output	O	Sending of DTMF tone signal.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	10.5	V	1
Input voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V	2
Power consumption	P_D	500	mW	3
Operating temperature	T_{opr}	$-30 \sim +60$	℃	
Storage temperature	T_{opr}	$-55 \sim +150$	℃	

Note 1 : Referenced to GND.
Note 2 : The maximum applicable voltage on any pin with respect to GND.
Note 3 : Ta=25℃

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	2		6	V

■ DC Characteristics

(Ta=25℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage		V_{IL}		GND		$0.2V_{DD}$	V	
		V_{IH}		$0.8V_{DD}$		V_{DD}	V	
Tone output voltage	ROW	V_{OR}	$R_L=1k\Omega$	290	350	450	mV_{RMS}	
	COLUMN	V_{OC}	$R_L=1k\Omega$	380	450	550	mV_{RMS}	
Standby current		I_{SB}	$V_{DD}=3.5V$		3	6	μA	4
Operating current		I_{OP}	$V_{DD}=3.5V$		2	3	mA	5
Mute output current		I_{OL}	$V_{DD}=2V$, $V_{OL}=0.5V$	1	2		mA	6
Pulse sync output current		I_{PL}	$V_{DD}=2V$, $V_O=0.5V$	1			mA	
Pulse leakage output current		$\lvert I_{LKG} \rvert$	$V_{DD}=6V$, $V_O=6V$			1	μA	
Key pull-up input resistance		R_{KP}	$V_{DD}=3.5V$		100		kΩ	7
Key pull-down input resistance		R_{KD}	$V_{DD}=3.5V$		5		kΩ	7
Mode pull-up input resistance		R_{MP}	$V_{DD}=3.5V$		100		kΩ	
Mode pull-down input resistance		R_{MD}	$V_{DD}=3.5V$		100		kΩ	
HKS pull-up input resistance		R_{HK}	$V_{DD}=3.5V$		60		kΩ	
Tone output distortion			$V_{DD} \geqq 4V$, $R_L=1k\Omega$			−20	dB	8
Pre-emphasis		PE_{HB}	$V_{DD} \geqq 4V$, $R_L=1k\Omega$	1	2	3	dB	

Note 4 : All output pins in no-load condition when clock is stopped and when on hook.
Note 5 : All output pins in no-load condition during key input and when on hook/off hook.
Note 6 : Applied to the MUTE pin.
Note 7 : Resistance when $\overline{ROW}$ pin or $\overline{COL}$ pin is 125 Hz and is scanned at high or low level.
Note 8 : Unwanted frequency component corresponding to the total power of the fundamental tone signal of the $\overline{ROW}$ pin and $\overline{COL}$ pin.

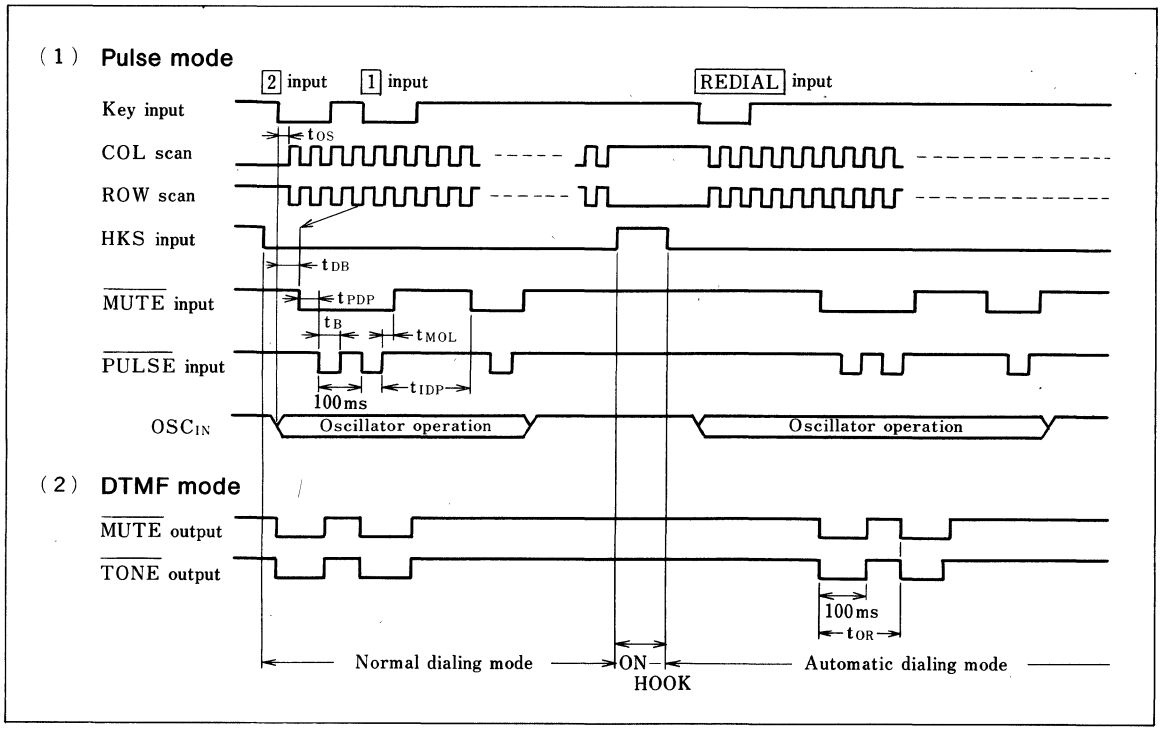
■ AC Characteristics

(Ta=25℃)

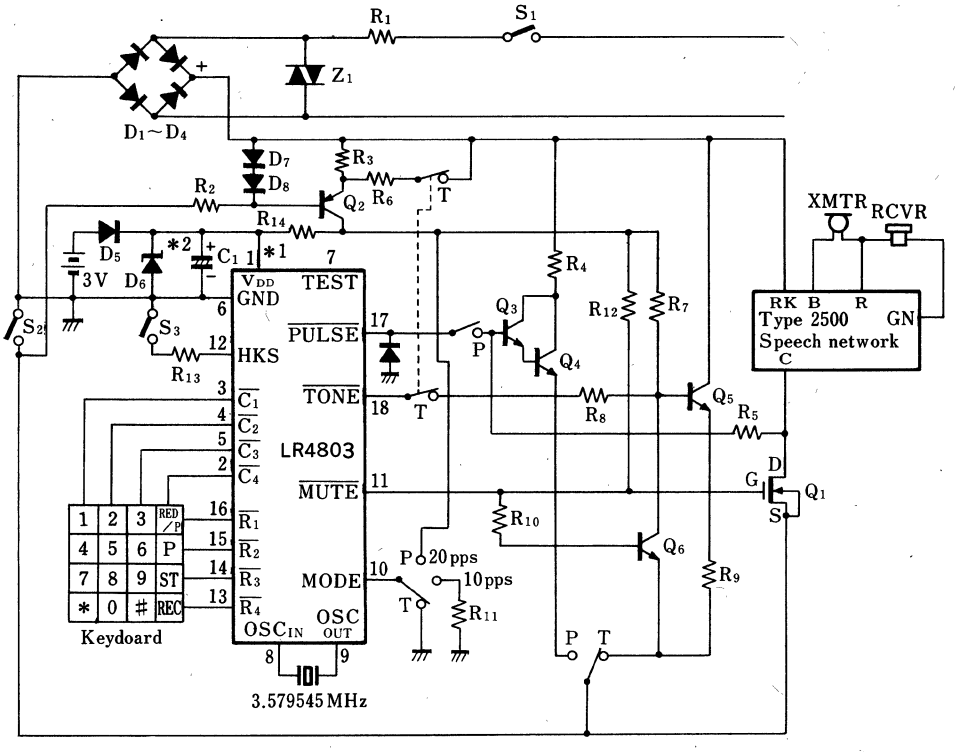
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Oscillation start time	tos			8	ms	9
Key debounce time	t_{DB}	4		32	ms	10
Pulse rate	P_R		10		pps	11
			20			12
Break time	t_B		60		ms	13
Interdigital pause time	t_{IDP}		1000		ms	13 14
Mute overlap time	t_{MOL}		2	4	ms	
Predigital pause time	t_{PDP}		40		ms	13
Tone output rate	T_{OR}		220		ms	

Note 9 : When crystal oscillation element with characteristics Rs=100Ω, Lm=96mH, C_m=0.02pF, C_h=5pF, f=3.579545 MHz is used.
Note 10 : Key input is accepted after oscillation begins if valid after t_{DB}.
Note 11 : Opens the MODE pin.
Note 12 : Connect the MODE pin to V_{DD}.
Note 13 : During 10-pps pulse mode (1/2 during 20-pps mode).
Note 14 : 100 ms during DTMF mode.

■ Timing Diagram



■ System Configuration (tone mode connection example)



Connect to P for pulse mode
Connect to T for tone mode

Z_1 = 10DK820
R_1 = 22Ω, 1W
R_2 = 560kΩ
R_3 = 1.5kΩ
R_4 = 150Ω
R_5 = 270kΩ
R_6 = 51Ω
R_7 = 5kΩ
R_8 = 100Ω
R_9 = 200Ω
R_{10} = 100kΩ
R_{11} = 1MΩ
R_{12} = 10kΩ
R_{13} = 470Ω
*1 R_{14} = 39Ω
*2 C_1 = 68 μF (Must be input to smooth the power supply and prevent latch up.)

Q_1 = 2N6660
Q_2 = 2N5401
Q_3 = 2N5550
Q_4 = 2N5550
Q_5 = 2N5550
Q_6 = 2N5550
S_1, S_2, S_3 = Hook
D_1~D_4 = 1N4004
D_5 = 1N270
D_6 = 1N752 (5.6V)
D_7 = 1N914
D_8 = 1N914

LR4804 Pulse / Tone Dialer CMOS LSI

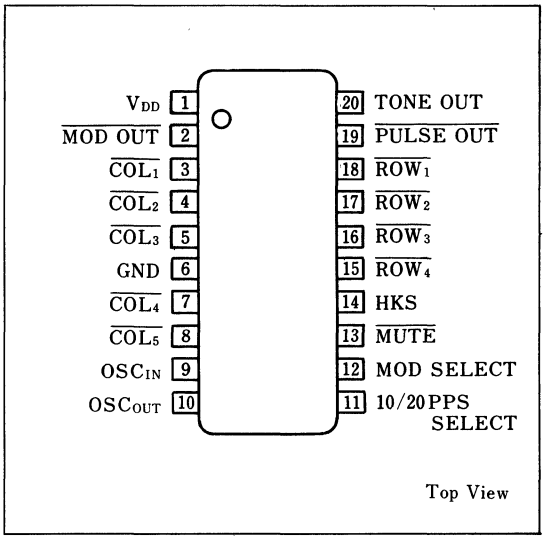
Description

The LR4804 is a CMOS LSI for the repertory dialer switchable between tone and pulse dialing with a 32-digit last number redial and the mode (pulse or tone) memory storages.

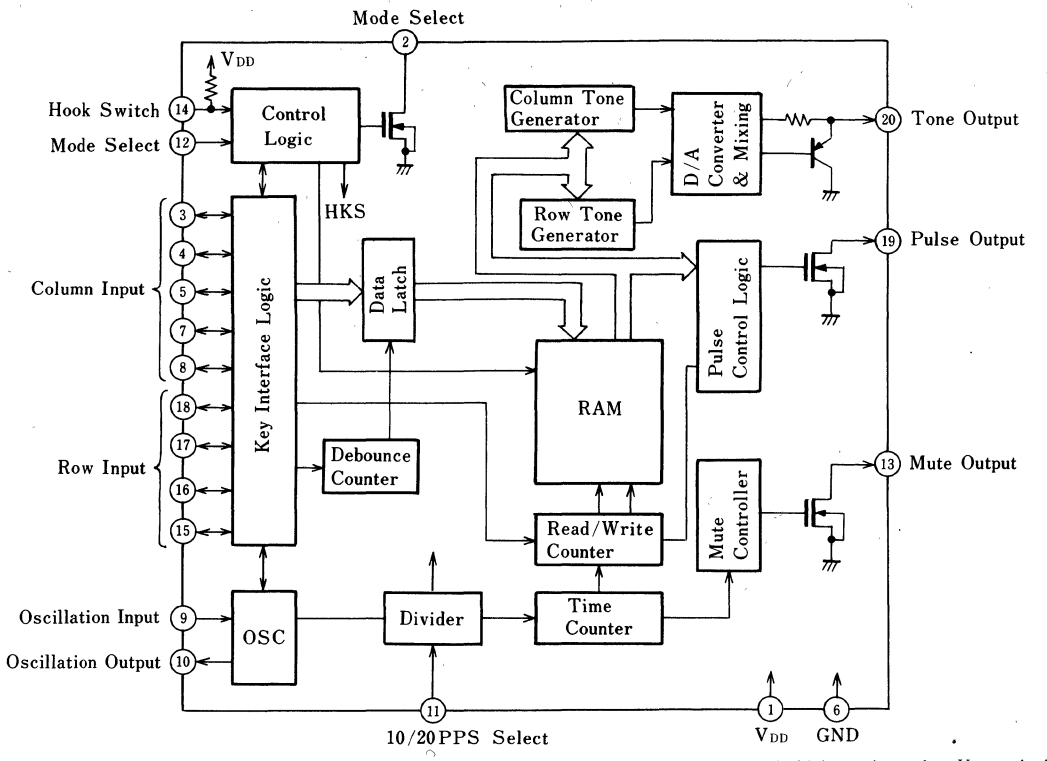
Features

1. Switchable between DTMF tone dialing and pulse dialing modes
2. The original mode in OFF HOOK state switchable by a pin and the mode in dialing by a mode key
3. Stores a 32-digit telephone number redial memory and the mode memory
4. PABX pause Storage
5. Uses the single contact or 15 keys matrix keyboard
6. Make/Break ratio : 40%/60%
7. Switchable between 10 pps and 20 pps in pulse dialing mode
8. A 3.579545MHz color burst crystal can be used for the clock oscillator
9. 20-pin dual-in-line package

Pin Connections



Block Diagram



Note) Be sure not to apply higher voltage than VDD to the TONE OUTPUT pin.

Pin Description

Signal Name	Symbol	I/O	Function
V_{DD}	Power supply		
$\overline{COL_1}$~$\overline{COL_5}$	Key input	I	COL 4-string key input
$\overline{ROW_1}$~$\overline{LOW_4}$			ROW 4-string key input
GND	Ground		Negative power supply pin
OSC_{IN}	Oscillator connection	I	Connect crystal for color burst
OSC_{OUT}		O	
$\overline{MOD\ OUT}$	Mode output	O	Mode: Pulse — High impedance; Tone — Low
10/20PPS SELECT	10/20PPS select input	I	Pin connection: GND — 10-pps pulse dialer; V_{DD} — 20-pps pulse dialer
MOD SELECT	Mode select	I	Pin connection: V_{DD} — Pulse dialer; GND — DTMF tone dialer
$\overline{MUTE}$	Mute output	O	Sending of MUTE signal
HKS	Hook switch input	I	Pin connection: V_{DD} — On-hook mode; Open — On-hook mode; GND — Off-hook mode
$\overline{PULSE\ OUT}$	Pulse output	O	Sending 10-pps or 20-pps pulse signal
TONE OUT	Tone output	O	Sending of DTMF tone signal

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	10.5	V	1
Input voltage	V_{IN1}	−0.3	V	2
	V_{IN2}	0.3	V	3
Power consumption	P_D	500	mW	4
Operating temperature	T_{opr}	−30~+60	℃	
Storage temperature	T_{stg}	−55~+150	℃	

Note 1 : Referenced to GND.
Note 2 : The maximum applicable voltage on any pin with respect to GND.
Note 3 : The maximum applicable voltage on any pin with respect to V_{DD}.
Note 4 : Ta=25℃

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	2		6	V

■ DC Characteristics

(Ta=25℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage		V_{IL}		GND		$0.2V_{DD}$	V	
		V_{IH}		$0.8V_{DD}$		V_{DD}	V	
Tone output voltage	ROW	V_{OR}	R_L=1kΩ, V_{DD}=4V	300	370	500	mV_{RMS}	
	COLUMN	V_{OC}	R_L=1kΩ, V_{DD}=4V	400	480	600	mV_{RMS}	
Standby current		I_{SB}	V_{DD}=3.5V		3	6	μA	5
Operating current		I_{OP}	V_{DD}=3.5V		2	3	mA	6
Mute output current		I_{OL}	V_{DD}=2V, V_{OL}=0.5V		2		mA	7
Pulse sync output current		I_{PL}	V_{DD}=2V, V_O=0.5V	1			mA	
Pulse leakage output current		$\|I_{LKG}\|$	V_{DD}=6V, V_O=6V			1	μA	8
Key pull-up input resistance		R_{KP}	V_{DD}=3.5V		100		kΩ	9
Key pull-down input resistance		R_{KD}	V_{DD}=3.5V		2		kΩ	9
HKS pull-up input resistance		R_{HK}	V_{DD}=3.5V		40		kΩ	
Tone output distortion			V_{DD}≧4V, R_L=1kΩ			−23	dB	10
Pre-emphasis		PE_{HB}	V_{DD}≧4V, R_L=1kΩ	1	2	3	dB	
Memory retention current		I_{MR}			0.7	3	μA	
Key input resistance		R_{KS}				5	KΩ	

Note 5: All output pins in no-load condition when clock is stopped and when on hook.
Note 6: All output pins in no-load condition during key input and when off hook.
Note 7: Applied to the MUTE, MOD pins.
Note 8: Applied to the MUTE, MOD, PULSE pins.
Note 9: Resistance when $\overline{\text{ROW}}$ pin or $\overline{\text{COL}}$ pin is 125 Hz and is scanned at high or low level.
Note 10: Unwanted frequency component corresponding to the total power of the fundamental tone signal of the $\overline{\text{ROW}}$ pin and $\overline{\text{COL}}$ pin.

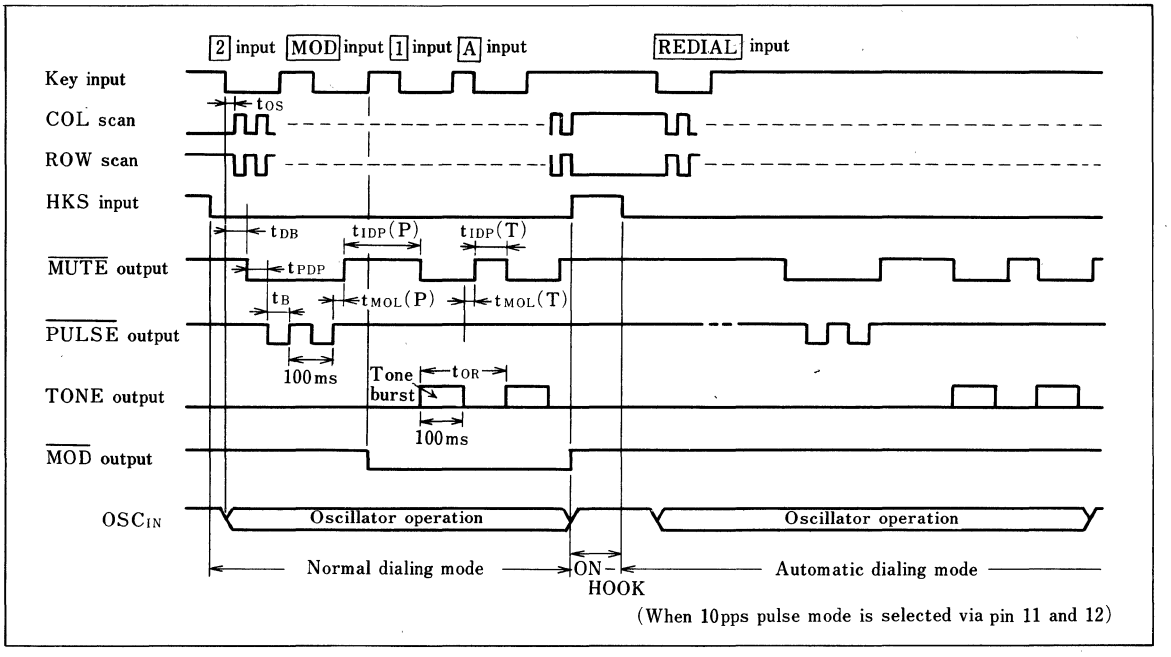
■ AC Characteristics

(Ta=25℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Key debounce time	t_{DB}		54	70	ms	11
Pulse rate	P_R		10		pps	12
			20		pps	13
Break time	t_B		60		ms	14
Interdigital pause time	t_{IDP}		1000		ms	14 15
Mute overlap time	t_{MOL}		6		ms	16
Predigital pause time	t_{PDP}		40		ms	14
Tone output rate	T_{OR}		220		ms	

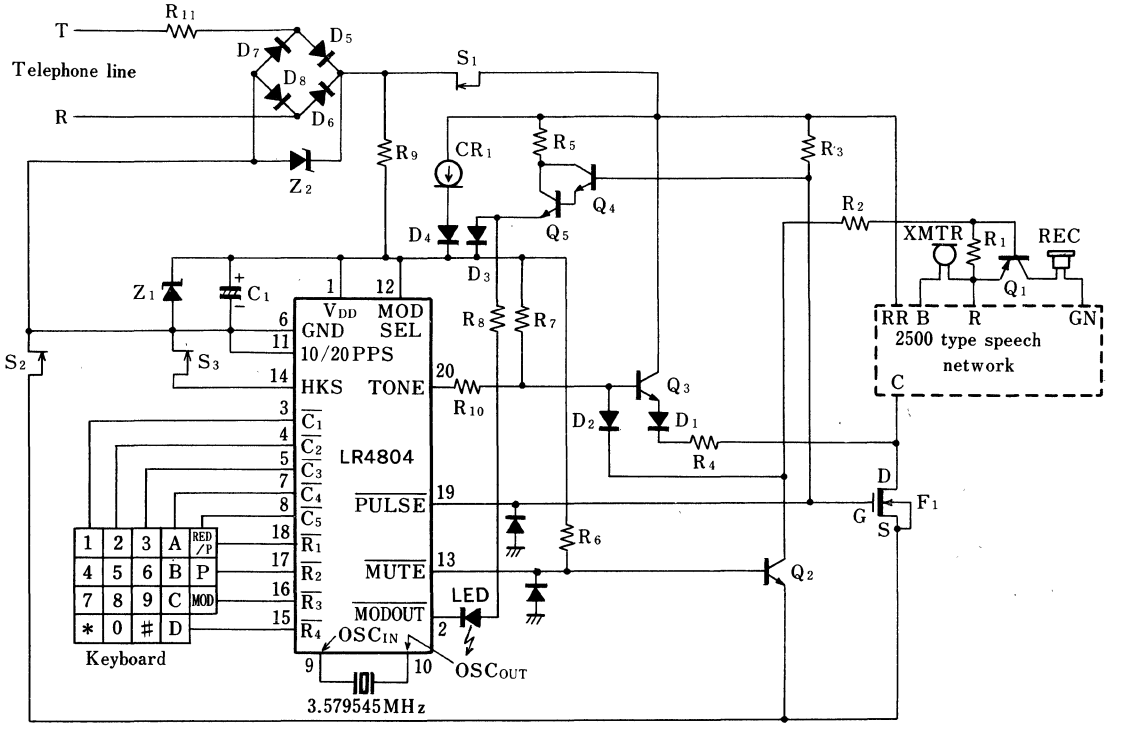
Note 11: Key input is accepted after oscillation begins if valid after t_{DB}.
Note 12: 10/20 pps SELECT pin connect to GND
Note 13: 10/20 pps SELECT pin connect to V_{DD}
Note 14: During 10 pps pulse mode (1/2 during 20 pps mode)
Note 15: 120 ms during DTMF mode
Note 16: 3.5 ms during DTMF mode

■ Timing Diagram



(When 10pps pulse mode is selected via pin 11 and 12)

■ System Configuration



LR4805 Pulse / Tone Dialer CMOS LSI

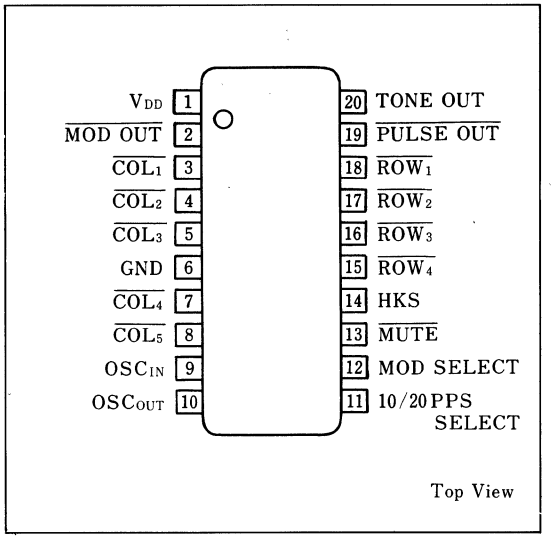
■ Description

The LR4805 is a CMOS LSI for the dialer switchable between tone and pulse dialing (make/break ratio : 32%/68%) with a 32-digit redial number memory and the pulse or tone mode memory storages.

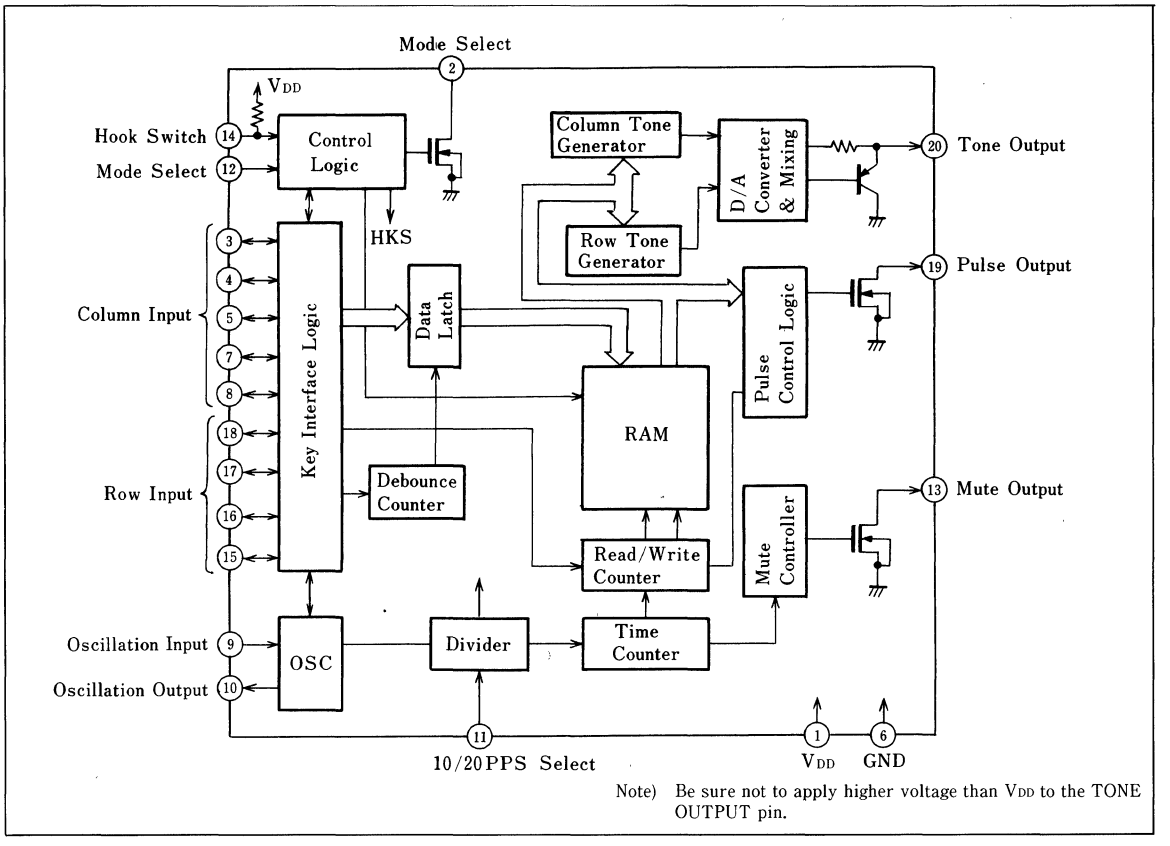
■ Features

1. Switchable between DTMF tone dialing and pulse dialing modes
2. The original mode in OFF HOOK state switchable by a pin and the mode in dialing by a mode key
3. Stores a 32-digit telephone number redial memory and the mode memory
4. PABX pause Storage
5. Uses the single contact or 15 keys matrix keyboard
6. Make/Break ratio : 32%/68%
7. Switchable between 10 pps and 20 pps in pulse dialing mode
8. A 3.579545MHz color burst crystal can be used for the clock oscillator
9. 20-pin dual-in-line package

■ Pin Connections



■ Block Diagram



Note) Be sure not to apply higher voltage than V_{DD} to the TONE OUTPUT pin.

■ Pin Description

Pin	Name	I/O	Function
V_{DD}	Power supply		
$\overline{COL_1}$~$\overline{COL_5}$	Key input	I	Key input of COL 5th row
$\overline{ROW_1}$~$\overline{ROW_4}$			Key input of ROW 4th row
GND	Ground		Negative power supply terminal
OSC_{IN}	Oscillator connection	I	Collar burst crystal connected
OSC_{OUT}		O	
$\overline{MOD\ OUT}$	Mode output	O	Mode: Pulse — High impedance; Tone — LOW
10/20PPS SELECT	10/20PPS select input	I	Pin connection: GND — 10pps pulse dialer; V_{DD} — 20pps pulse dialer
MOD SELECT	Mode select input	I	Pin connection: V_{DD} — Pulse dialer; GND — DTMF tone dialer
$\overline{MUTE}$	Mute output	O	Transmission of Mute signal
HKS	Hook switch input	I	Pin connection: V_{DD} — ON-Hook mode; Open — ON-Hook mode; GND — OFF-Hook mode
$\overline{PULSE\ OUT}$	Pulse output	O	Transmission of 10pps or 20pps pulse signal
TONE OUT	Tone output	O	Transmission DTMF tone signal

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	10.5	V	1
Maximum pin voltage	V_{IN1}	−0.3	V	2
	V_{IN2}	0.3	V	3
Power dissipation	P_D	500	mW	4
Operating temperature	T_{opr}	−30~+60	℃	
Storage temperature	T_{stg}	−55~+150	℃	

Note 1: Referenced to GND
Note 2: The Maximum applicable voltage on any pin with respect to GND
Note 3: The Maximum applicable voltage on any pin with respect to GND
Note 4: Ta = 25℃

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	2		6	V

■ DC Characteristics

Paramater		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage		V_{IL}		GND		$0.2V_{DD}$	V	
		V_{IH}		$0.8V_{DD}$		V_{DD}	V	
Tone output voltage	ROW	V_{OR}	$R_L=1k\Omega$, $V_{DD}=4V$	300	400	500	mV_{RMS}	
	COLUMN	V_{OC}	$R_L=1k\Omega$, $V_{DD}=4V$	400	500	600	mV_{RMS}	
Stand-by current		I_{SB}	$V_{DD}=3.5V$		1	2	μA	5
Operating current		Iop	$V_{DD}=3.5V$		1	2	mA	6
Mute output current		I_{OL}	$V_{DD}=2V$, $V_{OL}=0.5V$	2			mA	7
Pulse sink output current		I_{PL}	$V_{DD}=2V$, $V_O=0.5V$	1			mA	
Pulse leak output current		I_{LKG}	$V_{DD}=6V$, $V_O=6V$			1	μA	8
Key pullup input resistance		R_{KP}	$V_{DD}=3.5V$		60		KΩ	9
Key pulldown input resistance		R_{KD}	$V_{DD}=3.5V$		2		KΩ	9
HKS pullup input resistance		R_{HK}	$V_{DD}=3.5V$		30		KΩ	
Tone output distortion			$V_{DD} \geqq 4V$			−23	dB	10
Pre-emphasis		PE_{HB}	$V_{DD} \geqq 4V$, $R_L=1k\Omega$	1	2	3	dB	
Memory retention current		I_{MR}			0.5	1	μA	

Note 5: All output pins in no-load state, clock stationary, on-hook.
Note 6: All output pins in no-load state, key input, off-hook.
Note 7: Applies to $\overline{\text{MUTE}}$ and MOD pins.
Note 8: Applies to $\overline{\text{MUTE}}$, MOD, and PULSE pins.
Note 9: Resistance at which $\overline{\text{ROW}}$ pin or $\overline{\text{COL}}$ pin is scanned to High/Low level by 125Hz.
Note 10: Unnecessary components against basic tone signal total power of $\overline{\text{ROW}}$ and $\overline{\text{COL}}$ pins.

■ AC Characteristics

Paramater	Symbol	MIN.	TYP.	MAX.	Unit	Note
Key bounce time	t_{DB}		54	70	ms	11
Pulse rate	P_R		10		pps	12
			20			13
Break time	t_B		68		ms	14
Interdigital pause time	t_{IDP}		1,000		ms	14 15
Mute overlap time	t_{MOL}		6		ms	16
Pre-digital pause time	t_{PDP}		40		ms	14
Tone output rate	t_{OR}		220		ms	

Note 11: Key input is acccpted t_{DB} after oscillation starts, if effective.
Note 12: 10/20PPS SELECT pin connected to GND.
Note 13: 10/20PPS SELECT pin connected to V_{DD}.
Note 14: 10PPS pulse mode (1/2 in 20PPS pulse mode).
Note 15: 120 ms in DTMF mode.
Note 16: 3.5 ms in DTMF mode.

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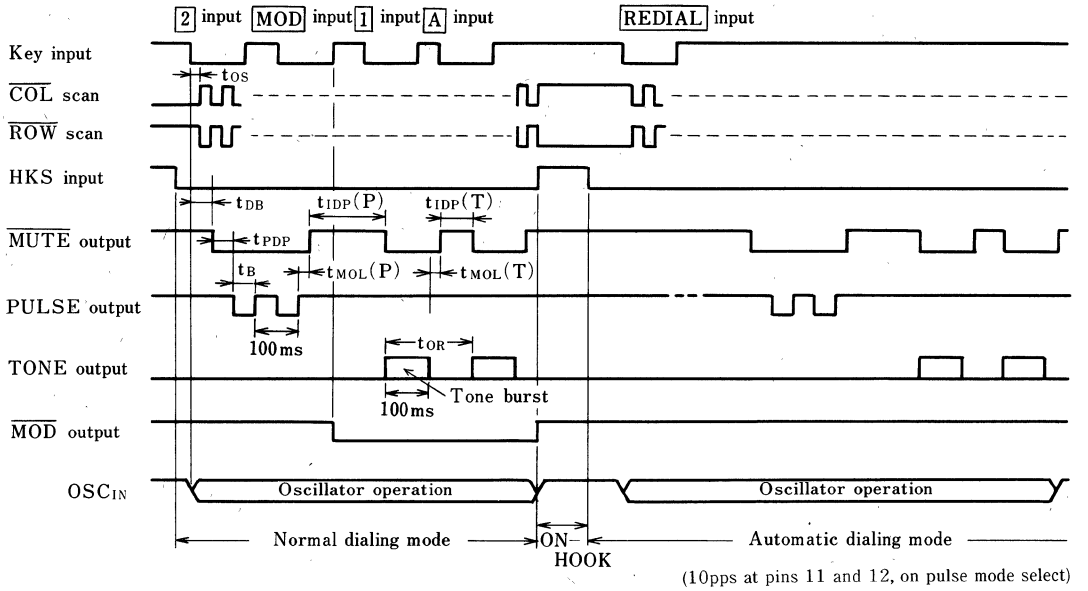
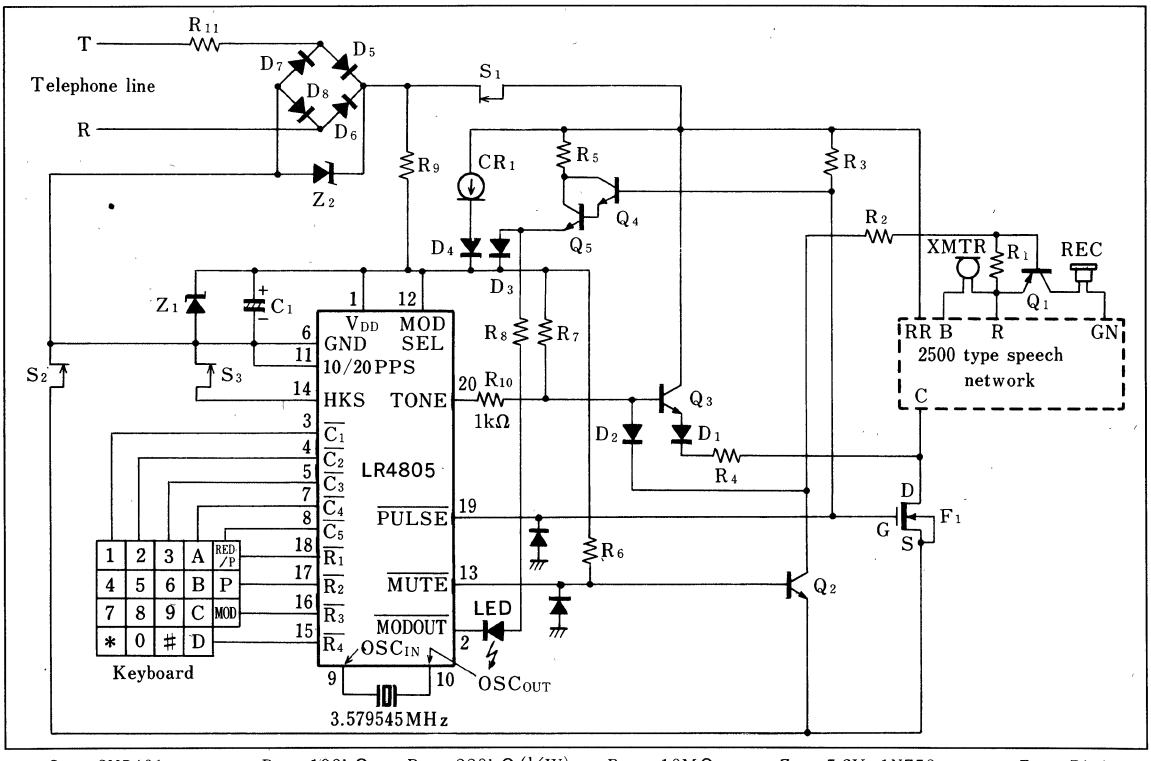
■ Timing Diagram



■ System Configuration



Q_1 = 2N5401
$Q_2 \sim Q_5$ = 1N5550
CR_1 = CR033
$D_1 \sim D_8$ = 1N4004

R_1 = 100kΩ
R_2 = 3kΩ
R_3 = 470kΩ
R_4 = 100Ω

R_5 = 220kΩ (½W)
R_6 = 120kΩ
R_7 = 2.5kΩ
R_8 = 3.3Ω

R_9 = 10MΩ
R_{10} = 1kΩ
R_{11} = 22Ω (W)

Z_1 = 5.6V : 1N752
Z_2 = 110V : 1N5379
$S_1 \sim S_3$ = Hook Switch
C_1 = 68μF
F_1 = 2N6660

Zener Diode

LR4806B Pulse / Tone Dialer CMOS LSI

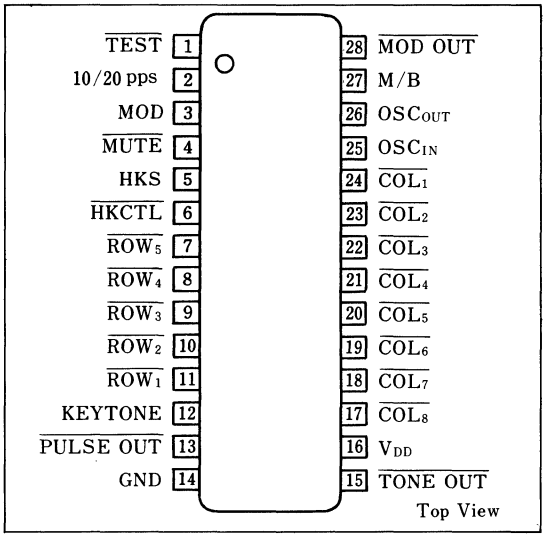
■ Description

The LR4806B is a CMOS LSI for the repertory dialer switchable between tone and pulse dialing. It offers one-touch dialing of up to 21 numbers, last number redial and other features.

■ Features

1. Switchable between DTMF tone dialing and pulse dialing modes
2. The original mode in OFF HOOK state switchable by a pin and the mode in dialing by a mode key
3. Stores twenty 16-digit telephone number memory and recalls by one-touch in the same mode as the storing mode
4. Stores a 32-digit telephone number redial memory and the mode memory and can clear it arbitrarily
5. Switchable for pulse ratio (10pps/20pps) and for make ratio (33%/37%) in pulse dialing mode
6. Hooking control input applied to on-hook dialing and speakerphone
7. Beep-tone output for key input
8. Auto-repeat dialing function (In other party's absence, repeats recalls automatically at constant intervals)
9. Flash signal output
10. PABX pause storage
11. A 3.579545MHz color burst crystal can be used for the clock oscillator
12. 28-pin dual-in-line package

■ Pin Connections



MOS ICs/LSIs

LZ92 Series CMOS Gate Array

■ Description

The LZ92 series employs the lastest silicon-gate CMOS technology, and features high speed and low power consumption.

The LZ92 series uses a single +5V power source, allowing a wide operating voltage range, and having a TTL-level I/O interface.

The basic internal gate operates in a time delay of 2.8ns. Ten series are available depending on the number of gates : LZ92300, LZ92450, LZ92600, LZ92800, LZ921000, LZ921500, LZ922200, LZ923000,LZ924000 and LZ925000.

As development is supported by CAD system, reliable development of special purpose LSI is possible in a short time. In choosing a series, considers that 90% of the internal gate can be used.

■ Feature

1. Short developing time
2. Low development cost
3. Suitable for ralatively small volume production but large variety of special-purpose LSIs
4. Abundant series (for 300, 450, 600, 800, 1000, 1500,2200, 3000,4000, and 5000 gates)

■ LZ92 Series Device List

Parameter \ Model		LZ92300	LZ92450	LZ92600	LZ92800	LZ921000	LZ921500	LZ922200	LZ923000	LZ924000	LZ925000
No. of gates (as counted in terms of dual-input NAND gates)		300	450	600	816	1010	1500	2240	3145	4009	5000
No. of I/O buffers		37	45	51	61	67	83	97	112	128	140
Total No. of pins		40	48	54	64	70	86	100	120	136	150
I/O level		TTL/CMOS level									
Delay time	Internal gate	2.8 ns per gate (F.O.=3, wire length 2mm)									
	Input buffer	TTL input 4.5ns/CMOS input 4.0ns (F.O.=3, wire length 2mm)									
	Output buffer	4.5ns (C_L=20pF)									
Supply voltage		5V±5% (TTL interface)/5V±10% (CMOS interface)									
Power consumption	Internal gate	25 μW/gate (F.O.=3, wire length 2mm, f=1MHz)									
	Input buffer	32 μW/gate (F.O.=3, wire length 2mm, f=1MHz)									
	Output buffer	600 μW/gate (f=1MHz, C_L=20pF)									
Package	DIP	16,18,20 22,24,28 30,40	16,18,20 22,24,28 30,40,42 48	18,20,22 24,28,30 40,42,48 64	18,20,22 24,28,30 40,42,48 64	22,24,28 30,40,42 48,64	24,28,30 40,42,48 64	24,28,40 64	40,64	64	64
	QFP	36,44,48	36,44,48	36,44,48 60	36,44,48 60,64	44,48,60 64,76	44,48,60 64,76,80 96	60,64,76 80,96 100	64,76,80 96,100	76,80,*96 100	76,80,*96 100
	SOP	24	24	24	24	24					
	PGA								120	120,144	120,144,180

DIP : dual-in-line package SOP : small-out-line package

QFP : quad-flat package PGA : pin-grid array

* Limited to 18 × 18 mm square type.

■ Absolute Maximum Ratings

Paramater	Symbol	Ratings	Unit
Supply voltage	V_{CC}	−0.3~7	V
Input voltage	V_I	−0.3~V_{CC}+0.3	V
Output voltage	V_O	−0.3~V_{CC}+0.3	V
Operating temperature	T_{opr}	−10~+70	℃
Storage temperature	T_{stg}	−55~+150	℃

■ Recommended Operating Conditions

Parameter	Symbol	TTL level			CMOS level			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V_{CC}	4.75	5	5.25	4.5	5	5.5	V
Operating temperature	T_{opr}	−10		+70	−10		+70	℃

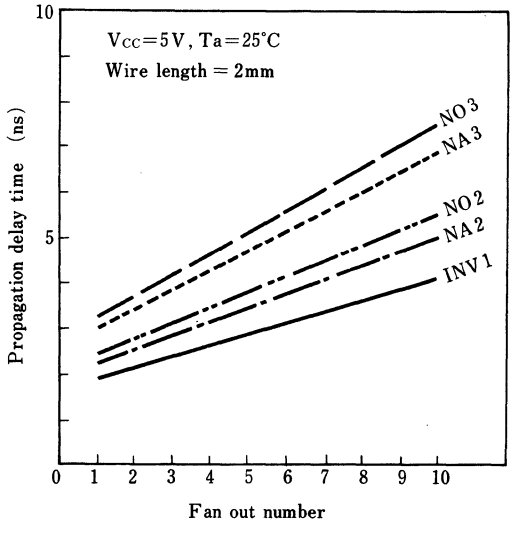
■ Electrical Characteristics

(V_{CC}=5V±5%, Ta=−10~+70℃)

Paramater	Symbol	Test conditions	TTL level			CMOS level			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input low voltage	V_{IL}				0.8			1.5	V
Input high voltage	V_{IH}		2.0			3.5			V
Output low voltage	V_{OL}	I_{OL}=4mA			0.4			0.4	V
Output high voltage	V_{OH}	I_{OH}=−2mA	2.4			4.0			V
Input leakage current	I_{IL}	V_I=0V~V_{CC}	−10		10	−10		10	μA
Output leakage current	I_{OZ}	High impedance status	−10		10	−10		10	μA

■ Basic Cell Delay Time

The following figure shows typical propagation delay times of a three-input NAND gate, two-input NAND gate, and inverter each configured with basic cells.



(1) Logic cells

Logic cells such as inverters, NAND gates, and NOR gates, and composite gates such as latches and flip-flops are available in 81 cell types.

(2) Input/output buffer cells

Buffer cells used in the periphery of a chip are available in 6 types of write-only buffers, 4 types of read-only buffers, and 4 types of read/write buffers: 14 types in all.

■ Development of LSI Devices Using Gate Arrays

For gate array development we provide the following:

① Design manual
② Cell library
③ Design form (2mm graph paper in A2 size)
④ Test pattern coding sheet
⑤ Logic template

After completing logic design in accordance with the design manual, please submit the following to us:

① Logic diagram
② Input/output timing diagrams (test data)
③ Package specifications
④ Pin configuration

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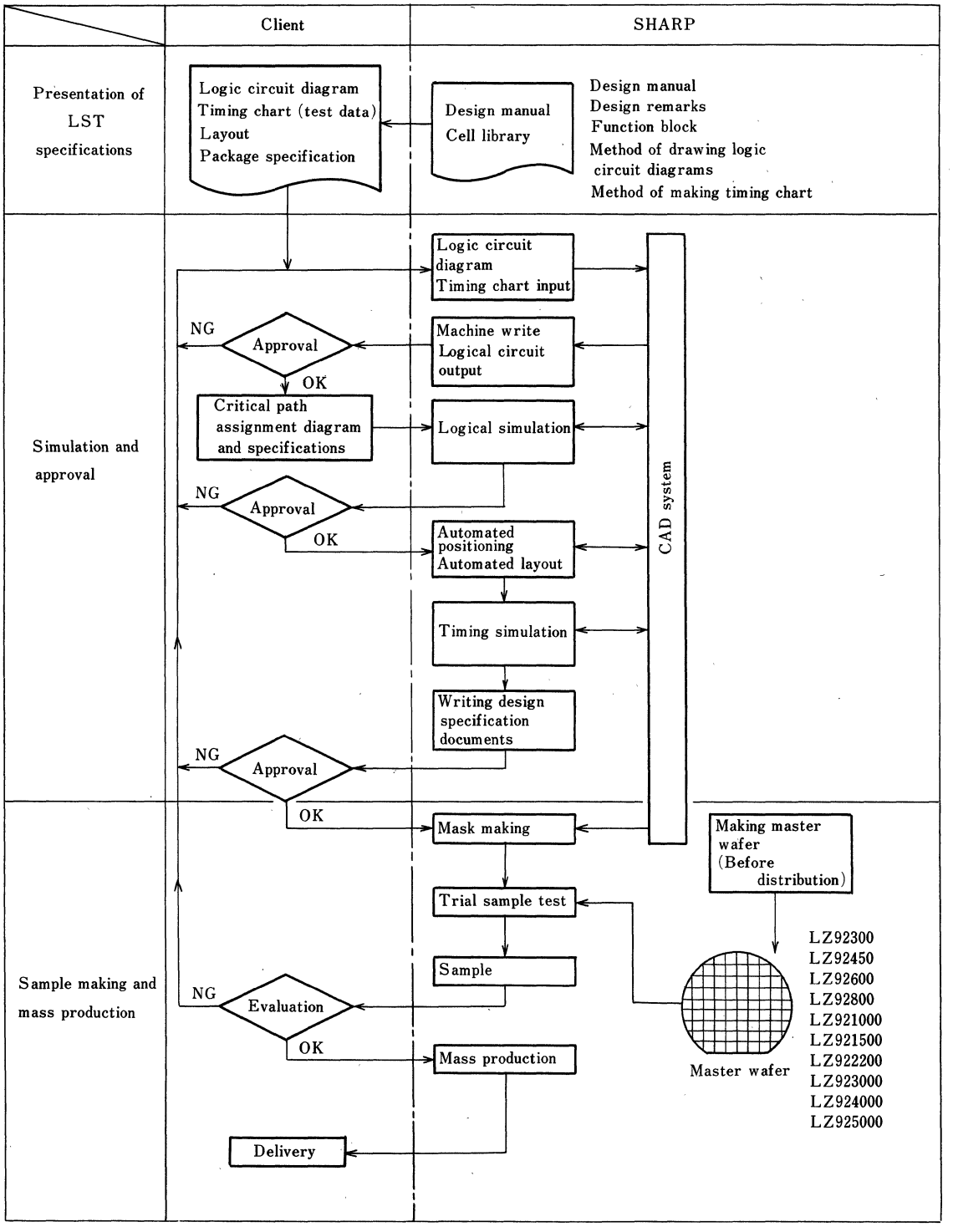
■ Development Sequence Flowchart for Gate Array LSI



LZ2020 CCD Image Sensor

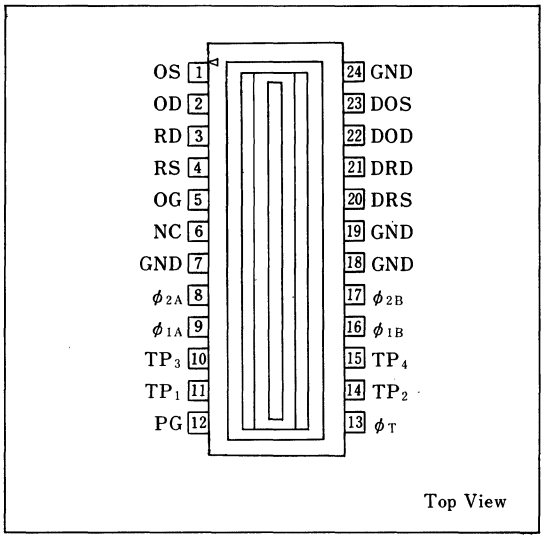
■ Description

The LZ2020 is a CCD linear image sensor with 2,048 PN photodiode elements, two 1,024-bit analog shift registers, an output amplifier and compensation output amplifier on a single chip.

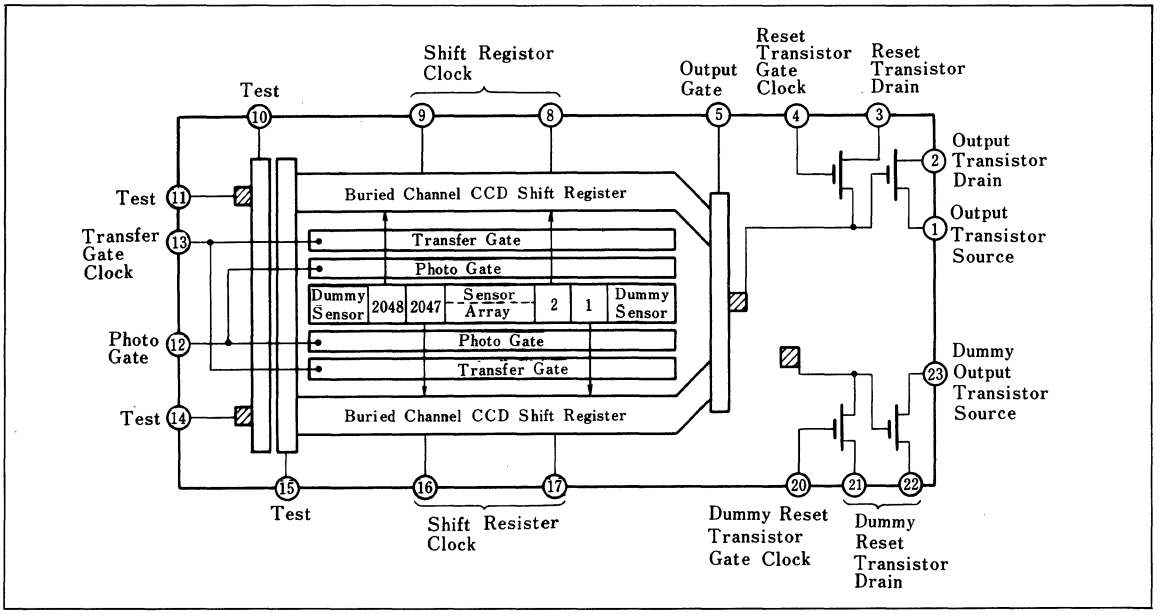
■ Features

1. Dynamic range 54dB (TYP.)
2. Enhanced spectral response (particularly in the blue range) and excellent output uniformity
3. Transfer efficiency 99.996%
4. 2,048 elements on a single chip ; picture element size : 14 μm×14 μm
5. On chip output amplifier and compensation amplifier
6. All operating voltages under 15V
7. 8 lines/mm resolution across a 256 mm page
8. 24-pin dual-in-line package (Ceramic)

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*	V_T	−0.3～+18	V
Operating temperature	V_{opr}	−25～+55	℃
Operating temperature	T_{stg}	−40～+100	℃

* Voltage applied to any pin with respect to V_{SS}.

■ Electrical Characteristics

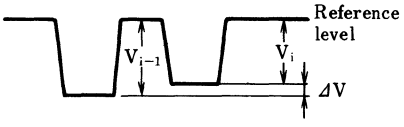
($f_{\phi 1}=f_{\phi 2}=0.2$MHz, $f_{RS}=0.4$MHz, $T_{Int}=10$ms, $V_{OD}=15$V, $V_{RD}=14$V, $V_{OG}=9$V, $V_{PG}=11$V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Dynamic range	DR	(1)(2)		54		dB
Saturation exposure	SE	(1)	0.4	0.7	1.3	lx·s
Saturation output voltage	V_{sat}	(1)(2)	400	550	650	mV
Sensitivity	R	(1)(2)	0.5	0.8	1.2	V/lx·s
Photo response non-uniformity	PRNU	(2)(3)		±7.5	±10	%
Average dark signal	ADS	(2)	0	0.8	5.0	mV
Dark signal non-uniformity	DSNU	(2)	0		5.0	mV
Spectrum range	SR		0.35		1.1	μm
Power consumption	P	(2)		150		mW
Output impedance	Z	(2)		1.0		kΩ

Condition (1) : Standard tungsten lamp, 2854°K
Condition (2) : Load resistance, 1k
Condition (3) : Standard tungsten lamp, 2854°K, with I-75 filter

(1) Photo Response Non-Uniformity (PRNU)

Bit voltage non-uniformity
Within ±3.0% relative to the previous bit



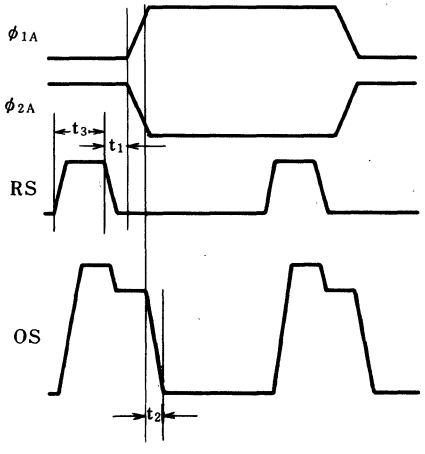
$$\Delta V = |V_{i-1} - V_i|$$

$$\frac{\Delta V}{V_{i-1}} \times 100 \leqq 3.0\,\%$$

where, i=1～2,048

Effective bits : 0～2,047, Reference level is a voltage at reset.

(2) Signal Rise Time



$t_1=120$ns
$t_2=100$ns
$t_3=160$ns
The output voltage shall settle within 100ns after ϕ_{1A} has risen above 8 volts.
(Waveform is observed with an oscilloscope.)

(3) Output during halt period

$f_{\phi 1}=f_{\phi 2}=0.5MHz$, $f_{RS}=1MHz$
$T_{Int}=2.2ms$, $V_{OD}=12V$, $V_{RD}=14V$, $V_{OG}=9V$
$V_{PG}=11V$, Ta=25℃
The output during the halt period shall be 7mV or lower, while the output level is kept at 125mV.

Note : The test conditions (1), (2) and (3) are applicable to items (1), (2), and (3).

■ Pin Capacitance

(Ta=25℃)

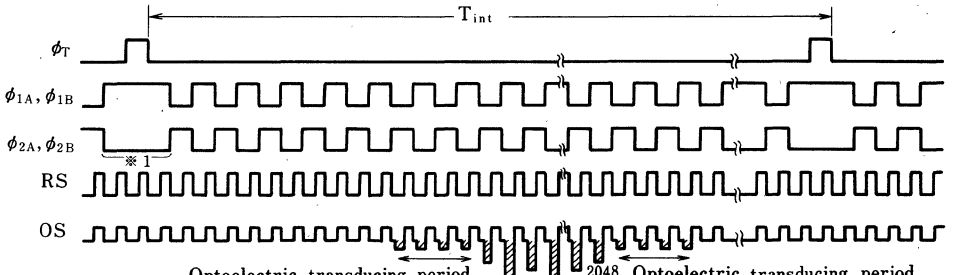
Parameter	Pin number	TYP.	Unit
Shift register clock	8, 9, 16, 17	550	pF
Transfer gate clock	13	230	pF
Reset transistor gate clock	4, 20	10	pF
Output transistor source	1, 23	10	pF

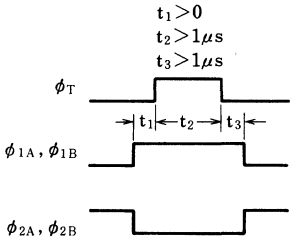
■ Recommended Operating Conditions

(Ta=25℃)

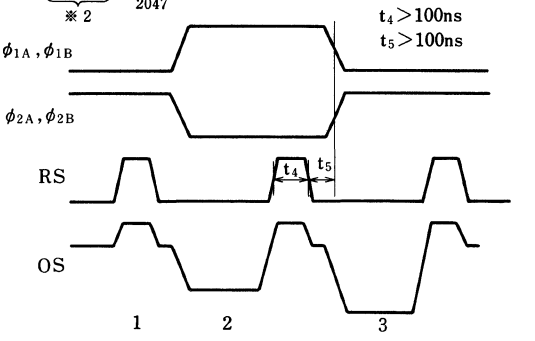
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output transistor drain voltage	V_{OD}		14.5	15.0	15.5	V
Reset transistor drain voltage	V_{RD}		13.5	14.0	14.5	V
Output gate voltage	V_{OG}		8.0	9.0	10.0	V
Photo gate voltage	V_{PG}	$V_{PG}=V_{\phi TH}+1(V)$	10.0	11.0	12.0	V
Test pins 1 and 2	TP_1, TP_2		14.5	15.0	15.5	V
Test pins 3 and 4	TP_3, TP_4			0		V
Shift register clock, low level	ϕ_{1AL}, ϕ_{2AL} ϕ_{1BL}, ϕ_{2BL}		0	0.5	0.8	V
Shift register clock, high level	ϕ_{1AH}, ϕ_{2AH} ϕ_{1BH}, ϕ_{2BH}		11.0	12.0	13.0	V
Transfer gate clock, low level	$V_{\phi TL}$		0	0.5	0.8	V
Transfer gate clock, high level	$V_{\phi TH}$		9.0	10.0	11.0	V
Reset gate clock, low level	V_{RSL}		0	0.5	0.8	V
Reset gate clock, high level	V_{RSH}		9.0	10.0	11.0	V
Shift register clock frequency	$f_{\phi 1A}$, $f_{\phi 2A}$ $f_{\phi 1B}$, $f_{\phi 2B}$			0.5		MHz
Reset gate clock frequency	f_{RS}			1.0		MHz

■ Drive Signal Timing Chart



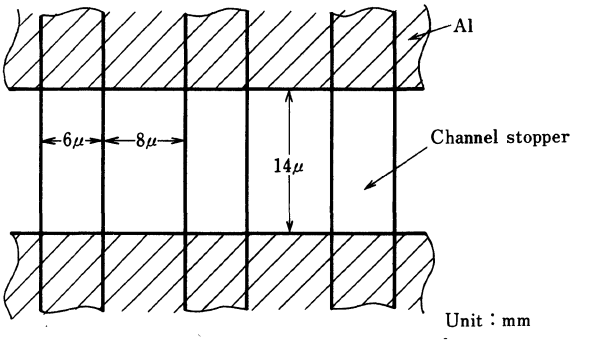


※1 ϕ_1, ϕ_2 vs. ϕ_T relationships



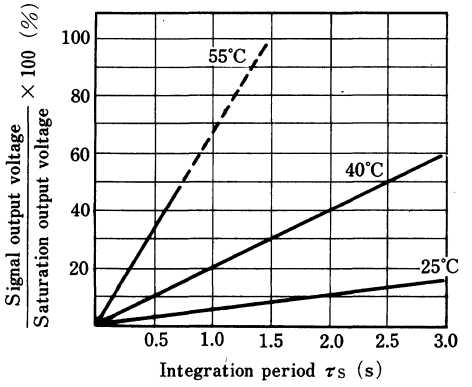
*2 ϕ_1, ϕ_2 vs. RS relationships

■ Photo-element Structure

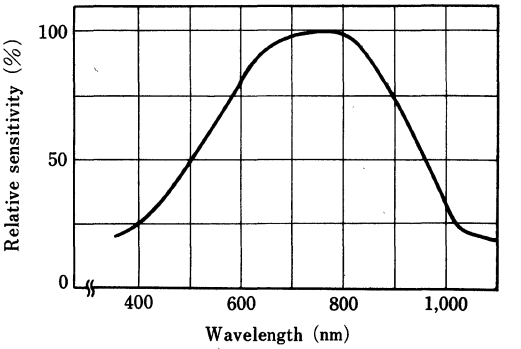


■ Standard Characteristics

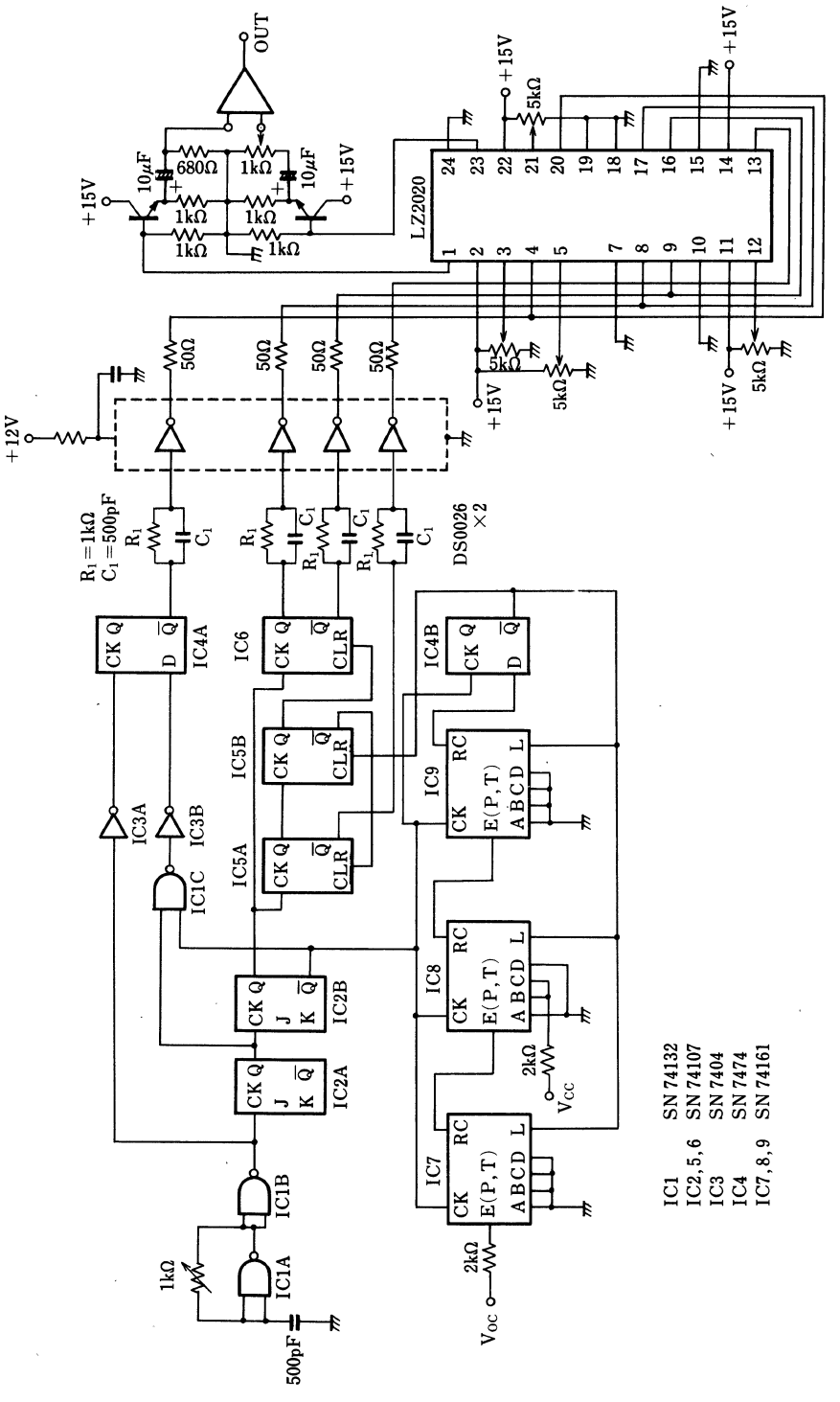
Dark current characteristics



Spectral sensitivity characteristics



■ Sample Drive Circuit



LZ1008AD High Voltage MOS IC

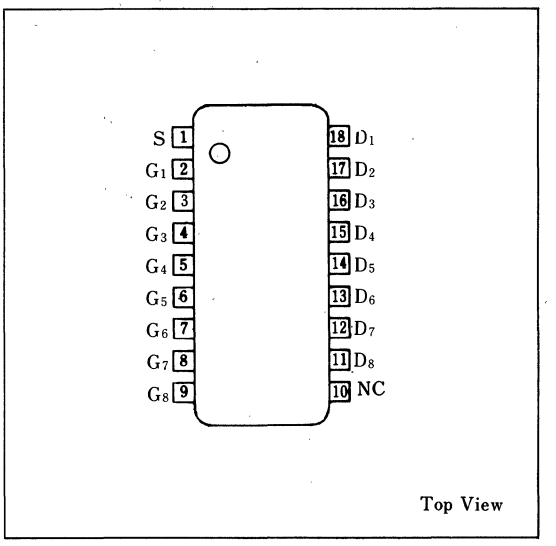
Description

The LZ1008AD is a high voltage (300V) 8-output-port monolithic IC fabricated using Sharp's advanced N-channel DMOS process. It can be used as a matrix driver for electroluminescent panels, plasma display panels, electrostatic printers and TTL-high voltage circuit interfaces.

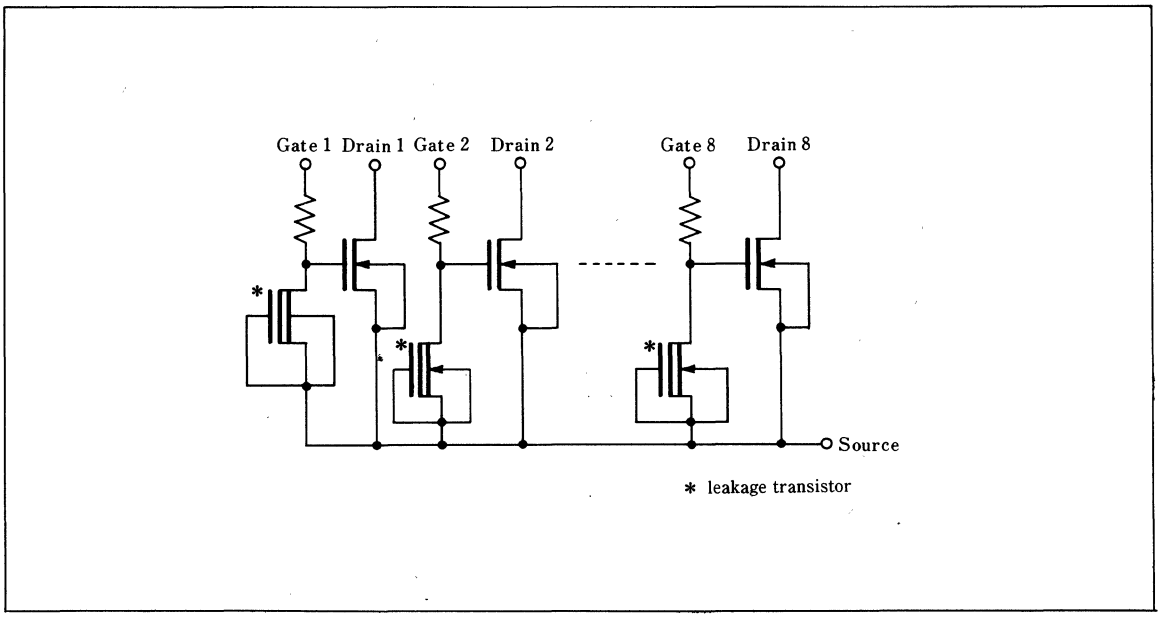
Features

1. High voltage 300V (MIN.)
2. Output current 35mA (TYP.)
3. Mutual conductance 10m℧ (TYP.)
4. TTL compatible
5. DMOS process
6. 18-pin dual-in-line package

Pin Connections



Equivalent Circuit



■ Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit	Note
Input high voltage	BV_{IN}	Applied to input pins.	−0.4～+15	V	1,2
On-output high voltage	$V_{O\ IN}$	Applied to output pins at V_{IN}=5.5V.	−0.4～+300	V	1,2
Off-output high voltage	$V_{O\ OFF}$	Applied to output pins at V_{IN}=0V.	−0.4～+600	V	1,2
Power consumption	P_D	Ta≦25℃	0.91	W	
Derating ratio		Ta＞+25℃	9.5	mW/℃	
Operating temperature	T_{opr}		−20～+70	℃	
Storage temperature	T_{stg}		−55～+155	℃	

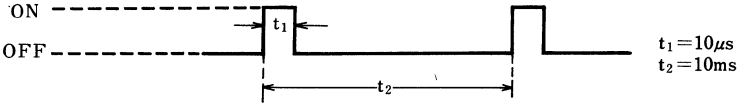
Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Permanent damage will result if a voltage above the rated value is applied.

■ Electrical Characteristics

(Ta=−20～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Output high voltage	BV_{OUT}	V_{IN}=0V, I_{OUT}=20 μA	600			V	
Output voltage	V_{OUT}	V_{IN}=5.5V, D=0.1%			300	V	3
Input high voltage	BV_{IN}	I_{IN}=20 μA	15			V	
Threshold voltage	V_P	V_{OUT}=10V, I_{OUT}=1 μA	0.8		1.4	V	4
Output current	I_{OUT}	V_{IN}=4.5V, V_{OUT}=300V, D=0.1%	30	35		mA	3,4
		V_{IN}=2.5V, V_{OUT}=300V, D=0.1%	1.5				
Output leakage current	I_{LO}	V_{IN}=0.4V, V_{OUT}=300V			10	μA	5
		V_{IN}=0.8V, V_{OUT}=300V			10	μA	4,5
Input leakage current	I_{LIN}	V_{IN}=10V	1.0		5.0	μA	4
On-state resistance	R_{ON}	V_{IN}=4.5V, I_{OUT}=5mA			1.0	kΩ	4
Mutual conductance	G_m	V_{IN}=2.55V, V_{OUT}=100V	3	10		m℧	4
Input capacitance	C_{IN}	V_{IN}=0V, f=1MHz			10	pF	

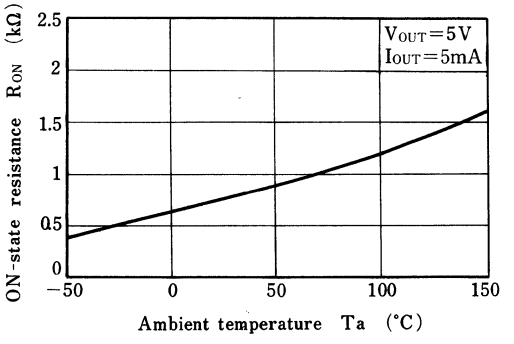
Note 3: D(duty cycle)=0.1%, see following waveform.



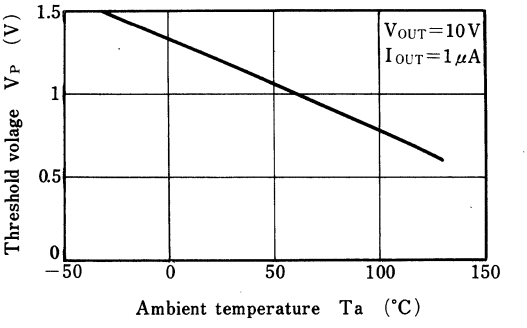
Note 4: At Ta=25℃
Note 5: The value for one HVMOST output pin.

■ Electrical Characteristics Curves (Ta=25℃ unless otherwise specified)

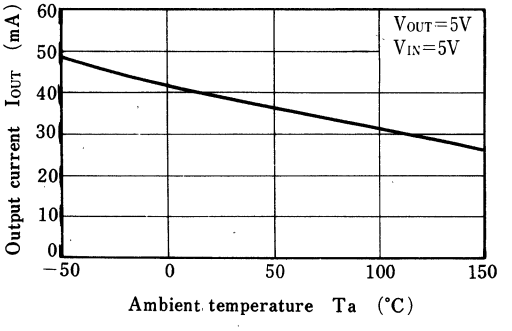
On-state resistance vs. Ambient temperature



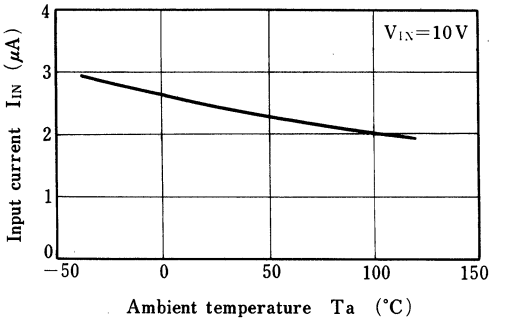
Threshold voltage vs. Ambient temperature



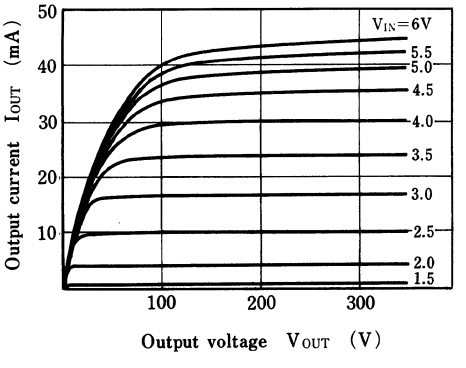
Output current vs. Ambient temperature



Input current vs. Ambient temperature



Output current vs. Output voltage

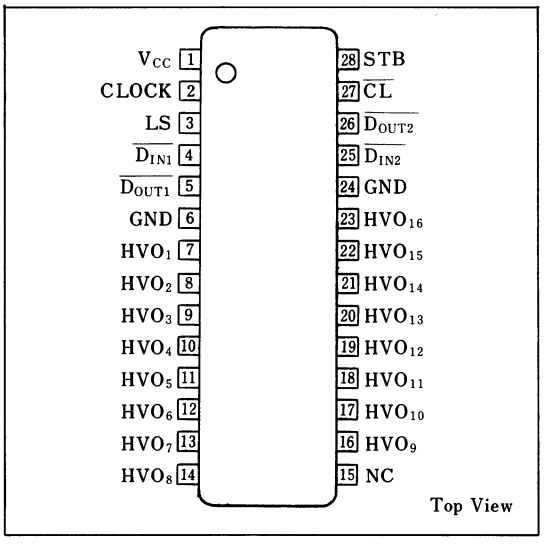


LZ1016AD High Voltage MOS IC

Description

The LZ1016AD is a high voltage (250V) 16-output-port monolithic IC fabricated using Sharp's advanced N-channel DMOS process. It can be used as a matrix driver for electroluminescent panels, plasma display panels, electrostatic printers and TTL-high voltage circuit interfaces.

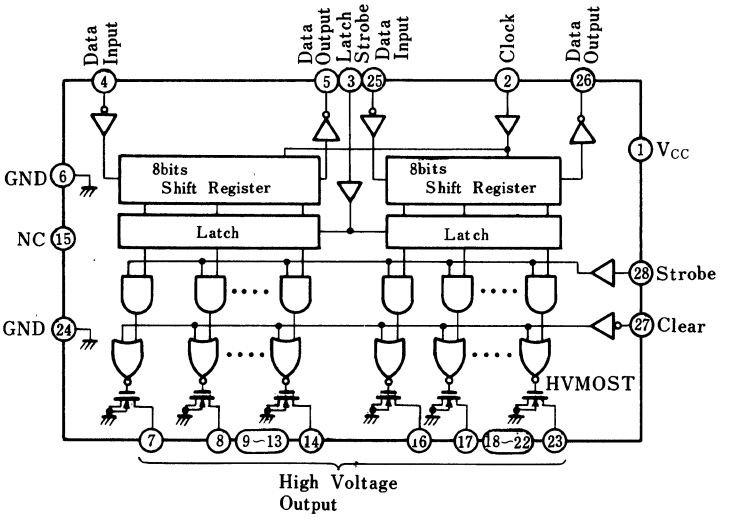
Pin Connections



Features

1. High voltage output 250V (MIN.)
2. Output current 45mA (TYP.)
3. Internal 8-bit × 2-shift-register circuit
4. Circuit expansion capability
5. TTL compatible
6. High speed data transfer (clock frequency 4MHz)
7. Single power supply : + 5V
8. DMOS process
9. 28-pin dual-in-line package

Block Diagram



Truth Table

D_{IN}	CL	STB	HVMOST
X	L	X	OFF
X	H	L	ON
L	H	H	ON
H	H	H	OFF

■ Absolute Maximum Ratings

(Ta=25℃)

Parameter	Symbol	Conditions	Ratings	Unit	Note
Supply voltage	V_{CC}	Applied to the logic supply pin.	−0.3～+7	V	1
Input voltage	V_{IN}	Applied to all input pin.	−0.3～+7	V	1
Output voltage	V_{OUT}	Applied to the data output pin.	−0.3～+7	V	1
ON-output high voltage	$V_{HVO(ON)}$	Applied to the high voltage output pin.	−0.3～+250	V	1,2,4
OFF-output high voltage	$V_{HVO(OFF)}$	Applied to the high voltage output pin.	−0.3～+350	V	1,3,4
Power consumption	P_D	Ta≦25℃	600	mW	
Derating ratio		Ta＞+25℃	5	mW/℃	
Operating temperature	T_{opr}		−20～+70	℃	
Storage temperature	T_{stg}		−55～+155	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Applied when HVMOST is on.
Note 3: Applied when HVMOST is off.
Note 4: Permanent damage will result if a voltage above the started value is applied.

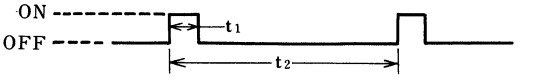
■ DC Characteristics

(1) HVMOST Characteristics

(V_{CC}=+5V±10%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
ON-state resistance	R_{ON}	HVMOST "ON" I_{HVO}=5mA, Ta=25℃			650	Ω	
Output current	I_{HVO}	HVMOST "ON" V_{HVO}=250V, Ta=25℃	40			mA	5
Output leakage current	$\|I_L\|$	HVMOST "OFF" V_{HVO}=300V, Ta=−20～70℃			10	μA	6
Total output leakage current	$\|I_{TL}\|$	HVMOST "OFF" V_{HVO}=300V, Ta=−20～70℃			30	μA	7

Note 5: D(duty circle)=0.1%, see following waveform.



t_1=10μs, t_2=10ms

Note 6: Value for each HVMOST output pin.
Note 7: Sum of total output leakage current.

(2) Logic Section Characteristics

(V_{CC}=+5V±10%, Ta=−20～+70℃)

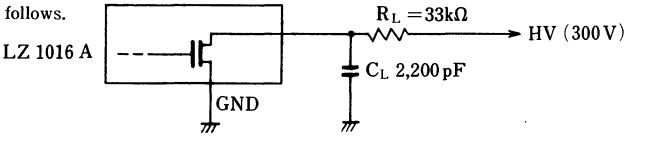
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	I_{CC}	V_{IN}=0V			18	mA
Input high voltage	V_{IH}		2.0		V_{CC}	V
Input low voltage	V_{IL}		−0.3		0.8	V
Output high voltage	V_{OH}	I_{OH}=−0.5mA; applied to $\overline{D_{OUT1}}$, $\overline{D_{OUT2}}$.	2.4			V
Output low voltage	V_{OL}	I_{OL}=1.6mA; applied to $\overline{D_{OUT1}}$, $\overline{D_{OUT2}}$.			0.4	V
Input leakage current	$\|I_{IL}\|$	V_{IN}=0V～V_{CC}			10	μA

AC Characteristics

(V_{CC}=+5V±10%, Ta=−20~+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock frequency	f_ϕ				4	MHz	
Clock pulse width	t_ϕ, $t_{\overline{\phi}}$		100			ns	
$\overline{D_{IN}}$ setup time	t_{DS}		60			ns	
$\overline{D_{IN}}$ hold time	t_{DH}		60			ns	
LS pulse width	t_{LP}		150			ns	
Clock to LS delay	t_{CL}		0			ns	
LS to clock delay	t_{LC}		0			ns	
$\overline{D_{OUT}}$ delay	t_{PD}	C_L=30pF+1TTL			190	ns	7
LS to STB delay	t_{LSB}		0			μs	
LS to $\overline{CL}$ delay	t_{LCL}		0			μs	
STB pulse width	t_{SP}		1			μs	
$\overline{CL}$ pulse width	t_{CLP}		1			μs	
HVO fall time	t_{PL}	C_L=2,200pF			50	μs	8
HVO rise time	t_{PH}	R_L=33kΩ			340	μs	8

Note 7: Applied to data output pins.
Note 8: Applied to high voltage output pins; test circuit is as follows.



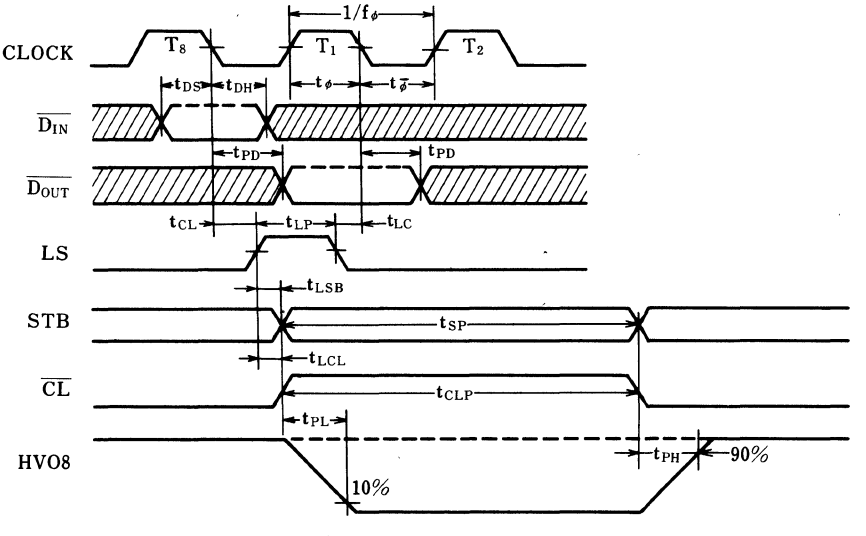
Input signal conditions:
Input pulse level: +0.8 to +2.0V
Input rise/fall time: 20 ns
Time measurement level: 50%

Pin Capacitance

(V_{CC}=0V, f=1MHz, Ta=25℃)

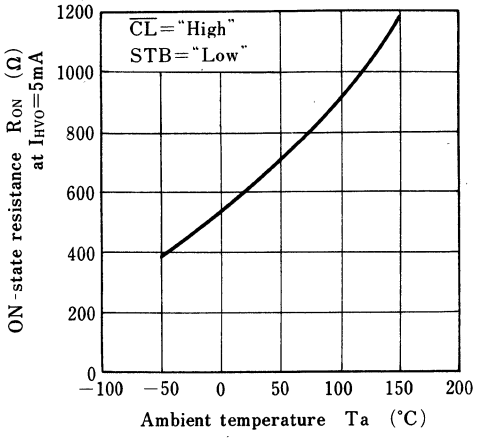
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		6	10	pF
High voltage output pin capacitance	C_{HVO}	V_{HVO}=0V		17	30	pF

AC Timing Chart

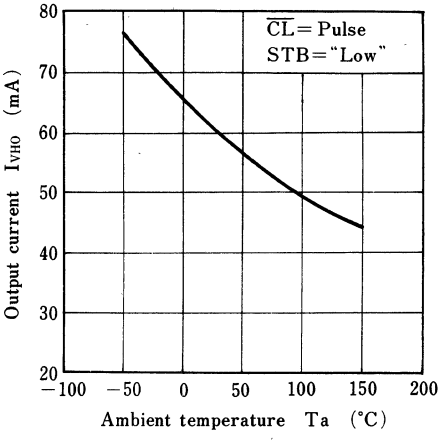


■ Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

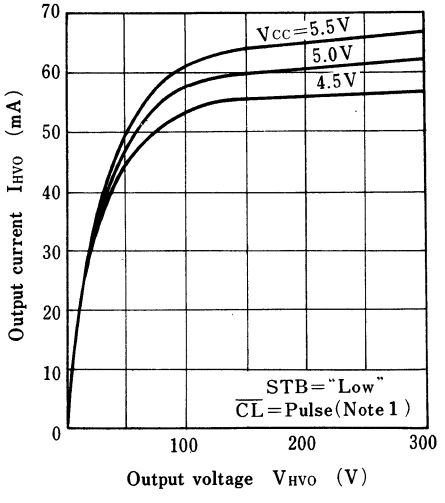
ON-state resistance vs. ambient temperature



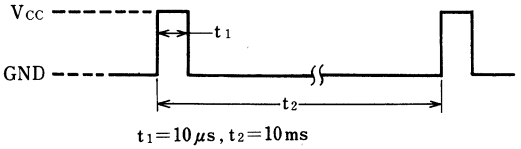
Output current vs. ambient temperature



Output current vs. output voltage



Note 1 : The pulse described below is applied to $\overline{CL}$.



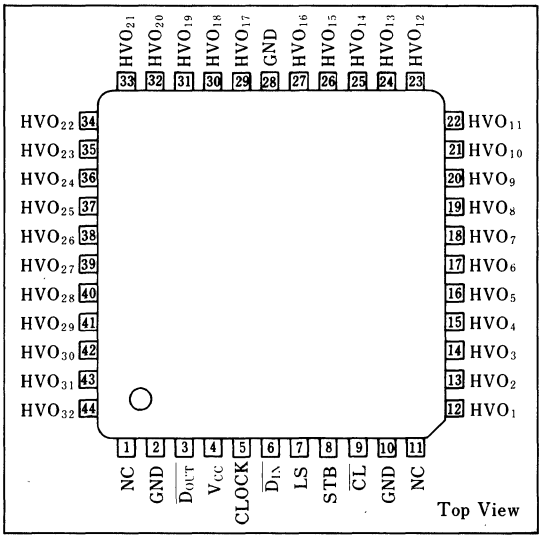
t_1=10μs, t_2=10ms
(D=0.1%)

LZ1032AM High Voltage MOS IC

■ Description

The LZ1032AM is a high voltage (250V) 32-output-port monolithic IC fabricated using Sharp's advanced N-channel DMOS process. It can be used as a matrix driver for electroluminescent panels, plasma display panels, electrostatic printers and TTL-high voltage circuit interfaces.

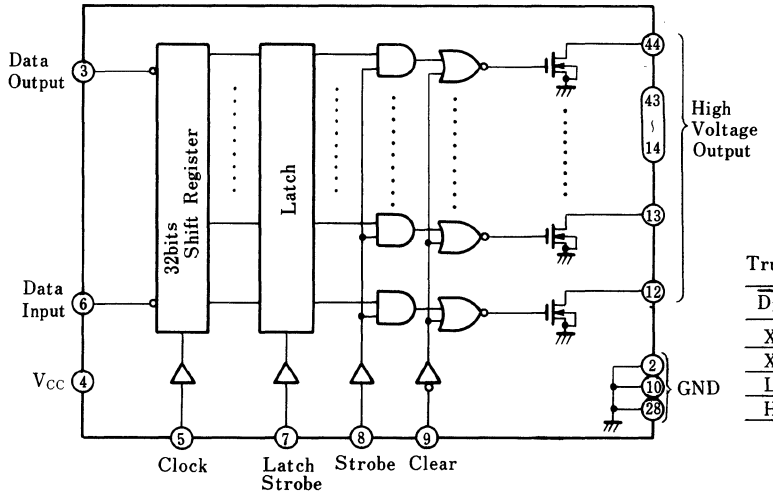
■ Pin Connections



■ Features

1. High voltage output 250V (MIN.)
2. Output current 45mA (TYP.)
3. Internal 32-bit shift register circuit
4. Expandable circuit structure
5. TTL compatible
6. High speed data transfer (clock frequency 4MHz)
7. Single power supply : + 5V
8. DMOS process
9. 44-pin quad-flat package

■ Block Diagram



Truth Table

$\overline{D_{IN}}$	$\overline{CL}$	STB	HVMOST
X	L	X	OFF
X	H	L	ON
L	H	H	ON
H	H	H	OFF

10

■ Absolute Maximum Ratings

(Ta=25℃)

Parameter	Symbol	Conditions	Ratings	Unit	Note
Supply voltage	V_{CC}		−0.3～+7	V	1
Input voltage	V_{IN}	Applied to input pins.	−0.3～+7	V	1
Output voltage	V_{OUT}	Applied to data output pins.	−0.3～+7	V	1
	$V_{HVO(ON)}$		−0.3～+250	V	1,2
	$V_{HVO(OFF)}$		−0.3～+350	V	1,3
Power consumption	P_D	Ta≦25℃	600	mW	
Derating ratio		Ta＞+25℃	5	mW/℃	
Operating temperature	T_{opr}		−20～+70	℃	
Storage temperature	T_{stg}		−55～+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: The maximum applicable voltage when HVMOST is ON.
Note 3: The maximum applicable voltage when HVMOST is OFF.

■ DC Characteristics

(1) HVMOST Characteristics

(V_{CC}=+5V±10%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
ON-state resistance	R_{ON}	HVMOST "ON" I_{HVO}=5mA, Ta=25℃			650	Ω	
Drain current	I_{HVO}	HVMOST "ON" V_{HVO}=250V, Ta=25℃	40			mA	4
Output leakage current	I_L	HVMOST "OFF" V_{HVO}=300V, Ta=−20～+70℃			10	μA	5
Output total leakage current	I_{TL}	HVMOST "OFF" V_{HVO}=300V, Ta=20～70℃			30	μA	6

Note 4: Duty circle=0.1%, with 10 μs ON-period.
Note 5: The value for one HVO output pin.
Note 6: The total leakage current of HVO.

(2) Logic Characteristics

(V_{CC}=+5V±10%, Ta=−20～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	I_{CC}	V_{IN}=0V			18	mA
Input high voltage	V_{IH}		2.0		V_{CC}	V
Input low voltage	V_{IL}		−0.3		0.8	V
Output high voltage	V_{OH}	I_{OH}=−0.5mA, Applied to $\overline{D_{OUT}}$	2.4			V
Output low voltage	V_{OL}	I_{OL}=1.6mA, Applied to $\overline{D_{OUT}}$			0.4	V
Input leakage current	I_{IL}	V_{IN}=0V～V_{CC}			10	μA

■ AC Characteristics

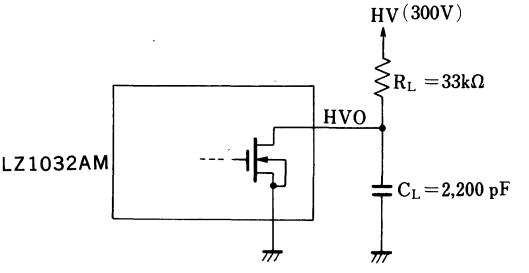
(V_{CC}=+5V±10%, Ta=−20～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock frequency	f_ϕ				4	MHz	
Clock pulse width	t_ϕ, $t_{\overline{\phi}}$		100			ns	
$\overline{D_{IN}}$ setup time	t_{DS}		60			ns	
$\overline{D_{IN}}$ hold time	t_{DH}		60			ns	
LS pulse width	t_{LP}		150			ns	
Clock to LS delay	t_{CL}		0			ns	
LS to clock delay	t_{LC}		0			ns	
$\overline{D_{OUT}}$ delay	t_{PD}	C_L (D_{OUT})=30pF+1TTL			190	ns	
LS to STB delay	t_{LSB}		0			ns	
LS to $\overline{CL}$ delay	t_{LCL}		0			ns	
STB pulse width	t_{SP}		1			μs	
$\overline{CL}$ pulse width	t_{CLP}		1			μs	
HVO fall time	t_{PL}	C_L (HVO)=2,200pF, R_L=33kΩ			50	μs	
HVO rise time	t_{PH}	C_L (HVO)=2,200pF, R_L=33kΩ			340	μs	7

Note 7: The output delay depends on the load condition.

Test conditions:

Input pulse level: + 0.8 to + 2.0V
Input rise/fall time: 20 ns
Time measurement level: 50%
HVO output load condition: See figure.



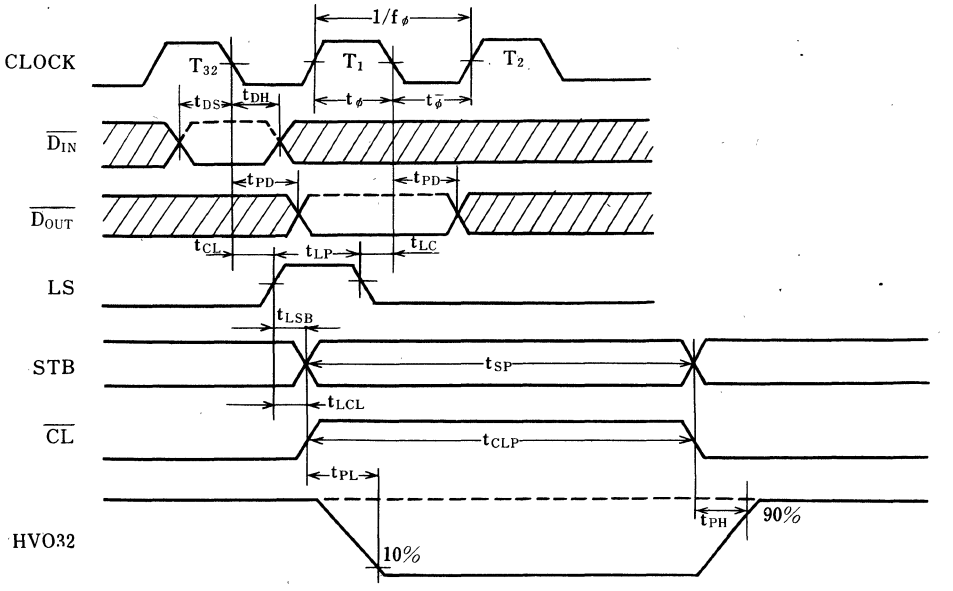
■ Capacitance

(V_{CC}=0V, f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IH}=0V		6	10	pF
Output capacitance	C_{HVO}	V_{HVO}=0V		17	30	pF

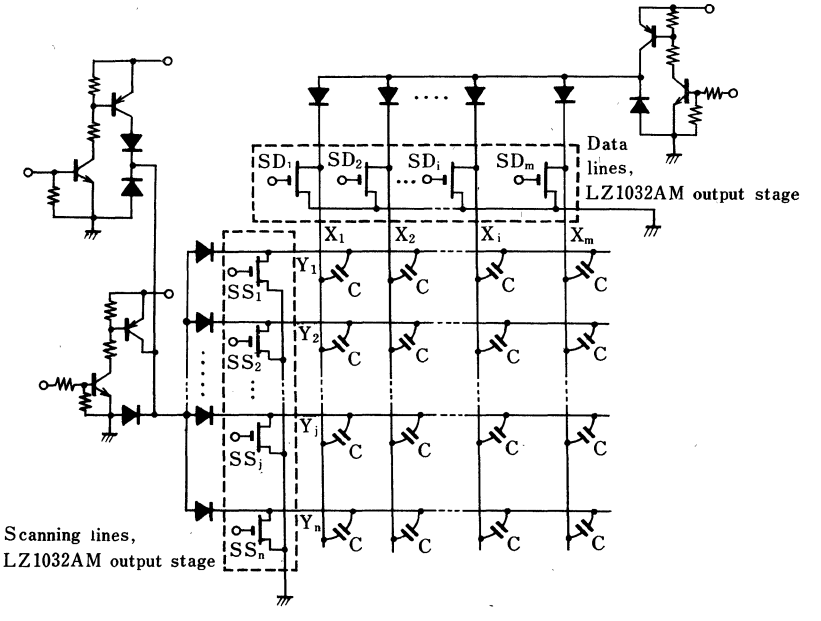
All pins except for the pin under measurement are grounded.

■ AC Timing Diagram



■ Example of Application

The following is a thin film EL matrix panel drive circuit fabricated by application of the high voltage MOS IC.



Note : The thin film EL matrix panel is a capacitive load.

LZ1108AD High Voltage MOS IC

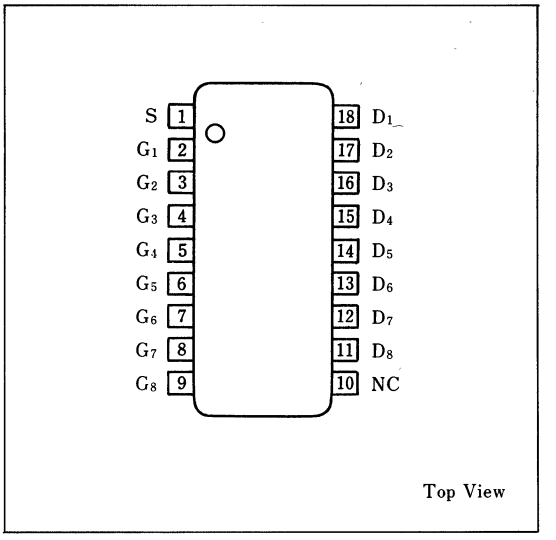
■ Description

The LZ1108AD is a monolithic FET array fabricated using Sharp's abvanced P-channel DMOS process. It provides voltage as high as 600V in input-off state, and permits stable operation at 300V drain voltage in input on state. It can be used as a matrix driver for electroluminescent panels, plasma display panels, and electrostatic printers.

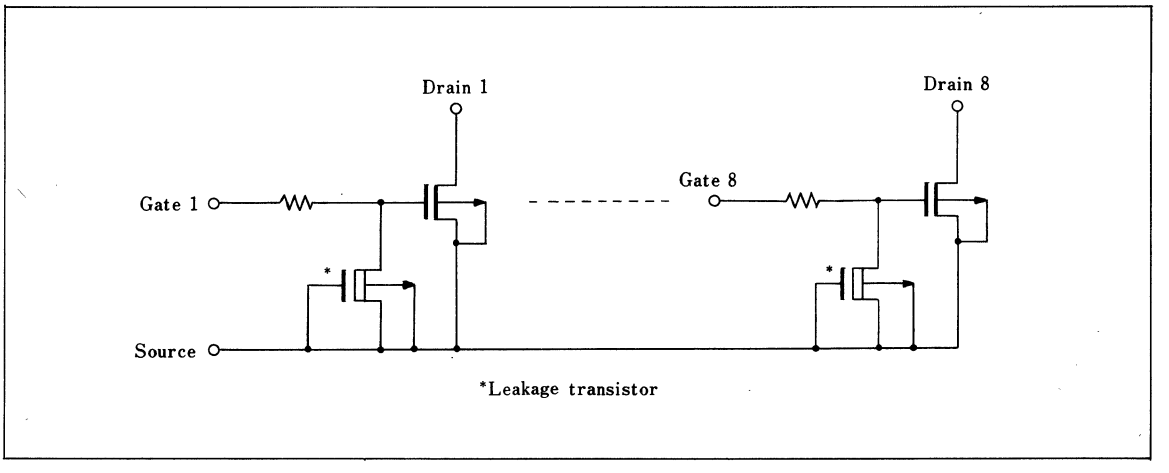
■ Features

1. High voltage 300V (MIN.)
2. High density 8 output/package
3. Output current 20mA (TYP. : V_{HVO} = 300V)
4. High mutual conductance 7.5m℧ (TYP.)
5. DMOS process
6. 18-pin dual-in-line package

■ Pin Connections



■ Equivalent Circuit



■ Absolute Maximum Ratings

(Ta=25℃)

Parameter	Symbol	Conditions	Ratings	Unit	Note
Input high voltage	BV_{IN}	Apply to input pins.	−15～+0.4	V	1,2
ON-output high voltage	$BV_{O\ ON}$	Applied to the output pin, when V_{IN}=5.5V.	−300～+0.4	V	1,2,3
OFF-output high voltage	$BV_{O\ OFF}$	Applied to the output pin, when V_{IN}=0V.	−600～+0.4	V	1,2
Power consumption	P_D	Ta≦25℃	600	mW	
Derating ratio		Ta＞+25℃	5	mW/℃	
Operating temperature	T_{opr}		−20～+70	℃	
Storage temperature	T_{stg}		−55～+150	℃	

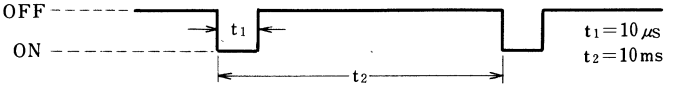
Note 1: The maximum applicable voltage on any pin with respect to S (Source).
Note 2: Permanent damage will result if a voltage above the stated value is applied.
Note 3: D (duty cycle) = 0.1%, ON time = 10 μs.

■ Electrical Characteristics

(Ta=−20～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Output high voltage	BV_{OUT}	V_{IN}=0V, I_{OUT}=−20 μA	−600			V	
Output voltage	V_{OUT}	V_{IN}=−5.5V, D=0.1%			−300	V	4
Input high voltage	BV_{IN}	I_{IN}=−20 μA	−15			V	
Threshold voltage	V_P	V_{OUT}=−10V, I_{OUT}=−1 μA	−1.1		−1.7	V	5
Output current	I_{OUT}	V_{IN}=−4.5V, V_{OUT}=−300V, D=0.1%	−15	−20		mA	4,5
		V_{IN}=−2.5V, V_{OUT}=−300V, D=0.1%	−1				
Output leakage current	$\lvert I_{LO} \rvert$	V_{IN}=−0.4V, V_{OUT}=−600V			10	μA	6
		V_{IN}=−0.8V, V_{OUT}=−600V			10	μA	5,6
Total output leakage current	$\lvert I_{TLO} \rvert$	V_{IN}=−0.4V, V_{OUT}=−600V			30	μA	7
		V_{IN}=−0.8V, V_{OUT}=−600V			30	μA	5,7
Input leakage current	$\lvert I_{LIN} \rvert$	V_{IN}=−10V	1		5	μA	5
ON resistance	R_{ON}	V_{IN}=−4.5V, I_{OUT}=−1mA			2	kΩ	5
Mutual conductance	G_m	V_{IN}=−3.0V, V_{OUT}=−150V	3	7.5		m℧	5
Input capacitance	C_{IN}	V_{IN}=0V, f=1MHz			10	pF	

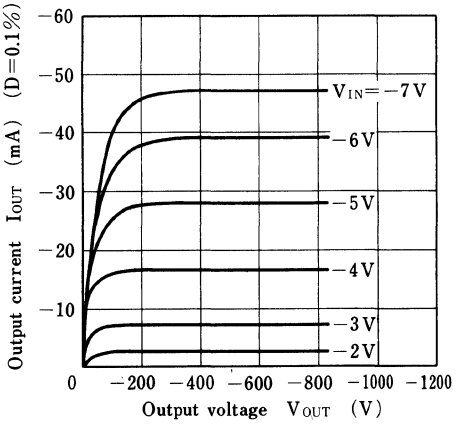
Note 4: D (duty cycle) = 0.1%; see following waveform.



Note 5: Ta=25℃
Note 6: Value for each HVMOST output pin.
Note 7: Sum of total HVMOST output current.

■ Electrical Characteristics Curves

Output current vs. Output voltage

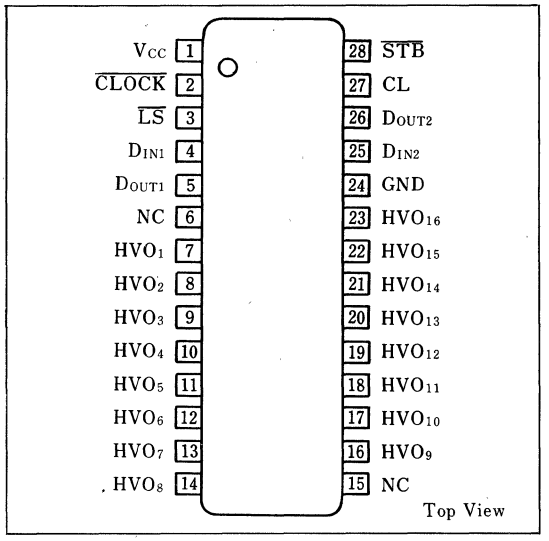


LZ1116AD High Voltage MOS IC

■ Description

The LZ1116AD is a high voltage (− 300V) 16-output-port monolithic IC fabricated using Sharp's advanced P-channel DMOS process. It can be used as a matrix driver for electroluminescent panels, plasma display panels, electrostatic printers.

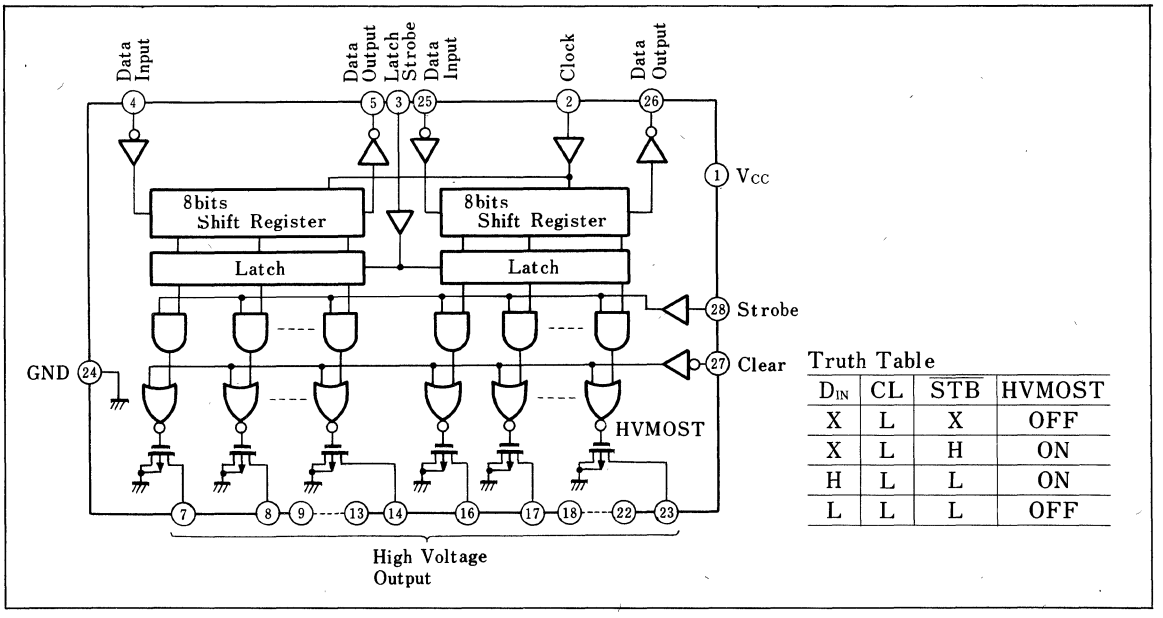
■ Pin Connections



■ Features

1. High voltage output 300V (MIN.)
2. Output current 30mA (TYP. : V_{HVO} = 300V)
3. Internal 8-bit × 2-shift-register circuit
4. Expandable circuit structure
5. High speed data transfer (clock frequency 4MHz)
6. Single power supply : −5V
7. DMOS process
8. 28-pin dual-in-line package

■ Block Diagram



Truth Table

D_{IN}	CL	$\overline{STB}$	HVMOST
X	L	X	OFF
X	L	H	ON
H	L	L	ON
L	L	L	OFF

■ Absolute Maximum Ratings

(Ta=25℃)

Parameter	Symbol	Conditions	Ratings	Unit	Note
Supply voltage	V_{CC}	Applied to the logic supply pin.	−7～+0.3	V	1
Input voltage	V_{IN}	Applied to all input pins.	−7～+0.3	V	1
Output voltage	V_{OUT}	Applied to the data output pin.	−7～+0.3	V	1
ON-output high voltage	$V_{HVO(ON)}$	Applied to the high voltage output pin.	−300～+0.3	V	1,2,4
OFF-output high voltage	$V_{HVO(OFF)}$	Applied to the high voltage output pin.	−300～+0.3	V	1,3,4
Power consumption	P_D	Ta≦25℃	600	mW	
Derating ratio		Ta＞+25℃	5	mW/℃	
Operating temperature	T_{opr}		−20～+70	℃	
Storage temperature	T_{stg}		−55～+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Applied when HVMOST is ON. D (duty cycle) = 0.1%, ON time = 10 μs
Note 3: Applied when HVMOST is OFF.
Note 4: Permanent damage will result if a voltage above the stated value is applied.

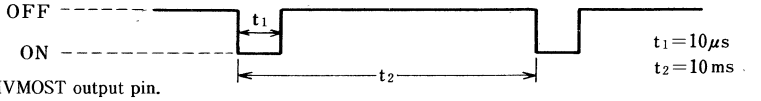
■ DC Characteristics

(1) HVMOST Characteristics

(V_{CC}=+5V±10%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
ON-state resistance	R_{ON}	HVMOST "ON" I_{HVO}=−1mA, Ta=25℃			1.3	kΩ	
Output current	I_{HVO}	HVMOST "ON" V_{HVO}=−300V, Ta=25℃	−20	−30		mA	5
Output leakage current	$\|I_L\|$	HVMOST "OFF" V_{HVO}=−300V, Ta=−20～+70℃			10	μA	6
Total output leakage current	$\|I_{TL}\|$	HVMOST "OFF" V_{HVO}=−300V, Ta=−20～+70℃			10	μA	6

Note 5: D (duty cycle) = 0.1%; see following waveform.



Note 6: Value for each HVMOST output pin.
Note 7: Sum of total output leakage current.

(2) Logic Section Characteristics

(V_{CC}=+5V±10%, Ta=−20～+70℃)

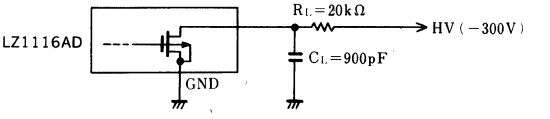
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	I_{CC}	V_{IN}=0V		−6	−12	mA
Input high voltage	V_{IH}		−0.8		0.3	V
Input low voltage	V_{IL}		V_{CC}		−2.4	V
Output high voltage	V_{OH}	I_{OH}=−0.5mA; applied to $\overline{D_{OUT1}}$, $\overline{D_{OUT2}}$	−0.5			V
Output low voltage	V_{OL}	I_{OL}=1.6mA; applied to $\overline{D_{OUT1}}$, $\overline{D_{OUT2}}$			−2.5	V
Input leakage current	I_{IL}	V_{IN}=0V～V_{CC}			10	μA

■ AC Characteristics

(V_{CC}=+5V±10%, Ta=−20~+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock frequency	f_ϕ				4	MHz	
Clock pulse width	t_ϕ, $t_{\overline{\phi}}$		125			ns	
$\overline{D_{IN}}$ setup time	t_{DS}		60			ns	
$\overline{D_{IN}}$ hold time	t_{DH}		60			ns	
LS pulse width	t_{LP}		150			ns	
Clock to LS delay	t_{CL}		0			ns	
LS to clock delay	t_{LC}		0			ns	
$\overline{D_{OUT}}$ delay	t_{PD}	C_L=30pF			250	ns	7
LS to STB delay	t_{LSB}		0			μs	
LS to $\overline{CL}$ delay	t_{LCL}		0			μs	
STB pulse width	t_{SP}		1			μs	
$\overline{CL}$ pulse width	t_{CLP}		1			μs	
HVO fall time	t_{PL}	C_L=900pF,			15	μs	8
HVO rise time	t_{PH}	R_L=20kΩ			60	μs	8

Note 7: Applied to data output pins.
Note 8: Appiled to high voltage output pins; test circuit is as follows.



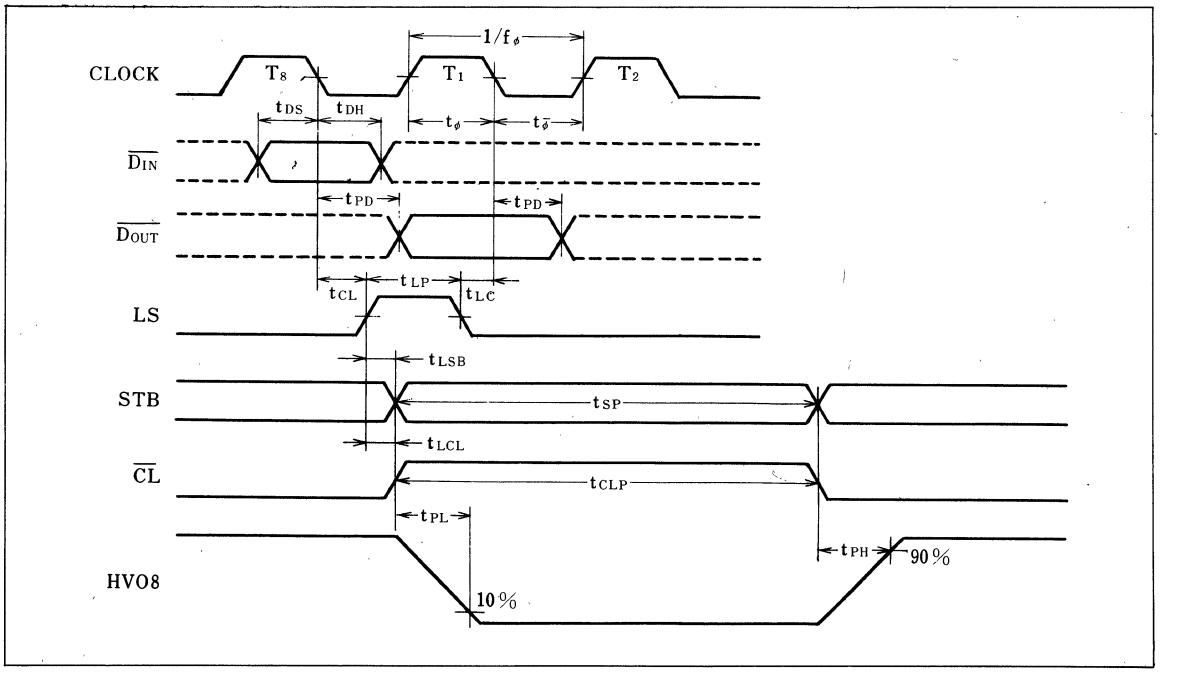
Input signal conditions:
Input pulse level: −2.0 to −0.8V
Input rise/fall time: 20 ns
Time measurement level: 50%

■ Capacitance

(V_{CC}=0V, f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		6	10	pF
Output capacitance	C_{HVO}	V_{HVO}=0V		17	30	pF

■ AC Timing Diagram

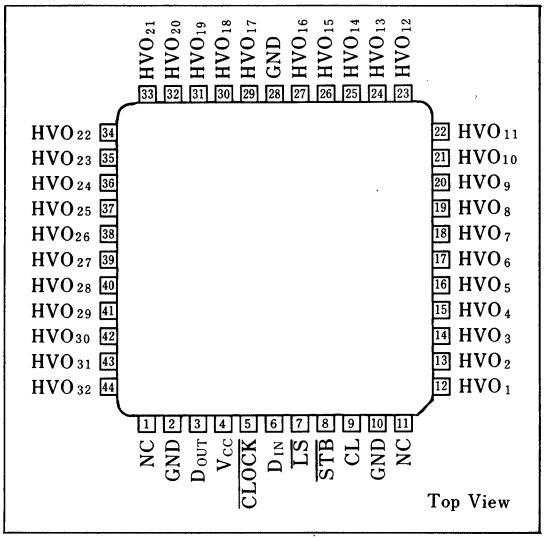


LZ1132AM High Voltage MOS IC

Description

The LZ1132AM is a high voltage (300V) 32-output-port monolithic IC fabricated using Sharp's advanced P-channel DMOS process. It can be used as a matrix driver for electroluminescent panels, plasma display panels, electrostatic printers.

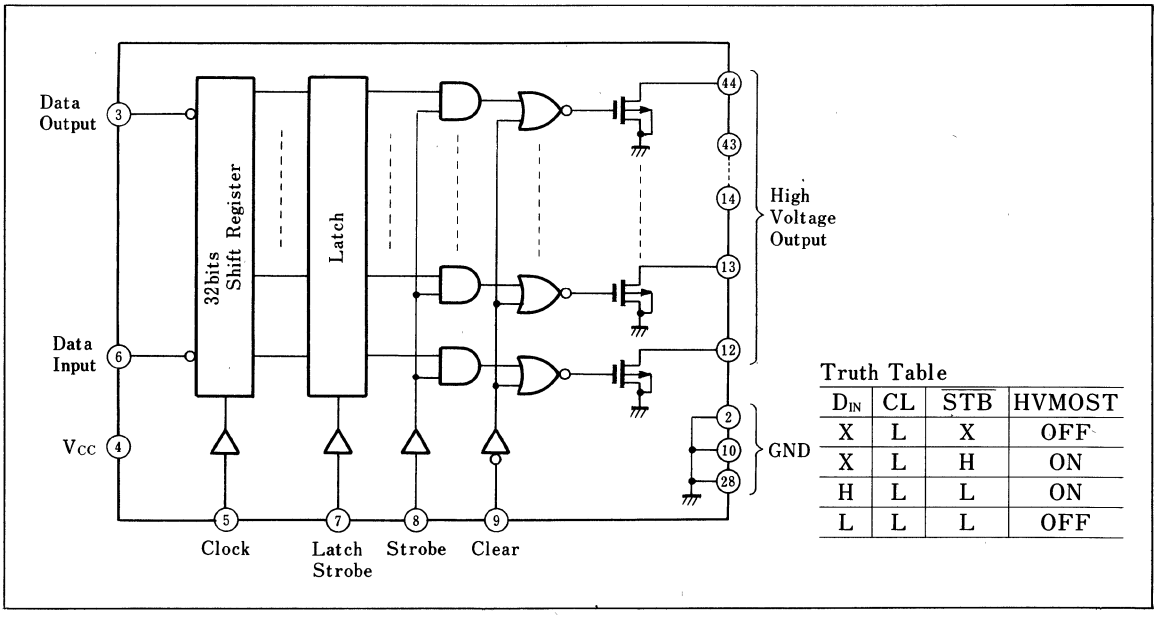
Pin Connections



Features

1. High voltage output 300V (MIN.)
2. Output current 30mA (TYP. : V_{HVO} = 300V)
3. Internal 32-bit shift register circuit
4. Expandable circuit structure
5. High speed data transfer (clock frequency 4MHz)
6. Single power supply : −5V
7. DMOS process
8. 44-pin quad-flat package

Block Diagram



Truth Table

D_{IN}	CL	$\overline{STB}$	HVMOST
X	L	X	OFF
X	L	H	ON
H	L	L	ON
L	L	L	OFF

10

■ Absolute Maximum Ratings

(Ta=25℃)

Parameter	Symbol	Conditions	Ratings	Unit	Note
Supply voltage	V_{CC}		−7～+0.3	V	1
Input voltage	V_{IN}	Applied to all input pins.	−7～+0.3	V	1
Output voltage	V_{OUT}	Applied to the data output	−7～+0.3	V	1
	$V_{HVO(ON)}$		−300～+0.3	V	1,2
	$V_{HVO(OFF)}$		−350～+0.3	V	1,3
Power consumption	P_D	Ta≦25℃	600	mW	
Derating ratio		Ta＞+25℃	5	mW/℃	
Operating temperature	T_{opr}		−20～+70	℃	
Storage temperature	T_{stg}		−55～+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: The maximum applicable voltage when HVMOST is ON. D (duty cycle) = 0.1%, ON time = 10 μs
Note 3: The maximum applicable voltage when HVMOST is OFF.

■ DC Characteristics

(1) HVMOST Characteristics

(V_{CC}=−5V±10%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
ON-state resistance	R_{ON}	HVMOST "ON" I_{HVO}=−1mA, Ta=25℃			1.3	Ω	
Output current	I_{HVO}	HVMOST "ON" V_{HVO}=−300V, Ta=25℃	−20	−30		mA	4
Output leakage current	$\|I_L\|$	HVMOST "OFF" V_{HVO}=−300V, Ta=−20～+70℃			10	μA	5
Total output leakage current	$\|I_{TL}\|$	HVMOST "OFF" V_{HVO}=−300V, Ta=−20～70℃			30	μA	6

Note 4: Duty cycle = 0.1%, ON time = 10 μs
Note 5: Value for each HVMOST output pin.
Note 6: Sum of total output leakage current.

(2) Logic Section Characteristics

(V_{CC}=+5V±10%, Ta=−20～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	I_{CC}	V_{IN}=0V		−8	−16	mA
Input high voltage	V_{IH}		−0.8		0.3	V
Input low voltage	V_{IL}		V_{CCC}		−2.4	V
Output high voltage	V_{OH}	I_{OH}=−0.2mA; applied to $\overline{D_{OUT}}$	−0.5			V
Output low voltage	V_{OL}	I_{OL}=1.6mA; applied to $\overline{D_{OUT}}$			−2.5	V
Input leakage current	I_{IL}	V_{IN}=0V～V_{CC}			10	μA

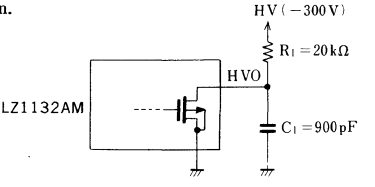
■ AC Characteristics

(V_{CC}=5V±10%, Ta=−20~+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock frequency	f_ϕ				4	MHz	
Clock pulse width	t_ϕ, $t_{\overline{\phi}}$		125			ns	
$\overline{D_{IN}}$ setup time	t_{DS}		60			ns	
$\overline{D_{IN}}$ hold time	t_{DH}		60			ns	
LS pulse width	t_{LP}		150			ns	
Clock to LS delay	t_{CL}		0			ns	
LS to clock delay	t_{LC}		0			ns	
$\overline{D_{OUT}}$ delay	t_{PD}	C_L (D_{OUT})=30pF			250	ns	
LS to STB delay	t_{LSB}		0			ns	
LS to $\overline{CL}$ delay	t_{LCL}		0			ns	
STB pulse width	t_{SP}		1			μs	
$\overline{CL}$ pulse width	t_{CLP}		1			μs	
HVO fall time	t_{PL}	C_L (HVO)=900pF, R_L=20kΩ			15	μs	
HVO rise time	t_{PH}	C_L (HVO)=900pF, R_L=20kΩ			600	μs	7

Note 7: Output delay time varies depending on load condition.

Test conditions:
- Input pulse level: −2.0 to +0.8V
- Input rise/fall time: 20 ns
- Time measurement level: 50%
- HVO output load conditions (figure at right).



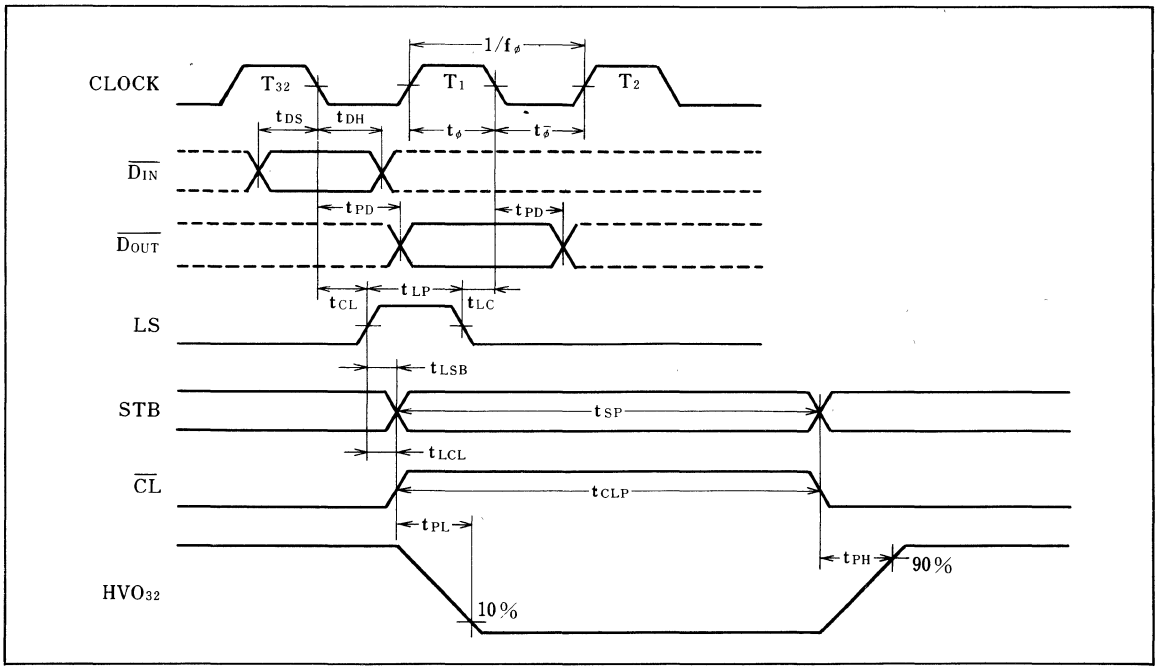
■ Capacitance

(V_{CC}=0V, f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		6	10	pF
Output capacitance	C_{HVO}	V_{HVO}=0V		17	30	pF

All pins except pin being measurement are counnected to GND.

■ AC Timing Diagram



LR3461 Electronic Melody Generator CMOS LSI

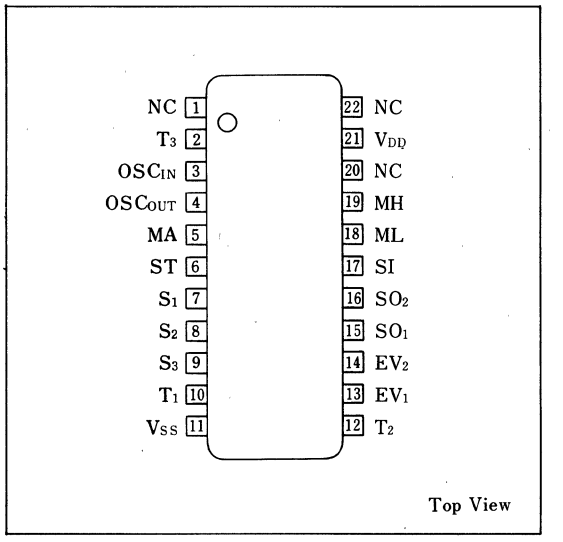
Description

The LR3461 is a CMOS LSI with melodies and alarm functions. It can be used in music boxes and alarm sound generators.

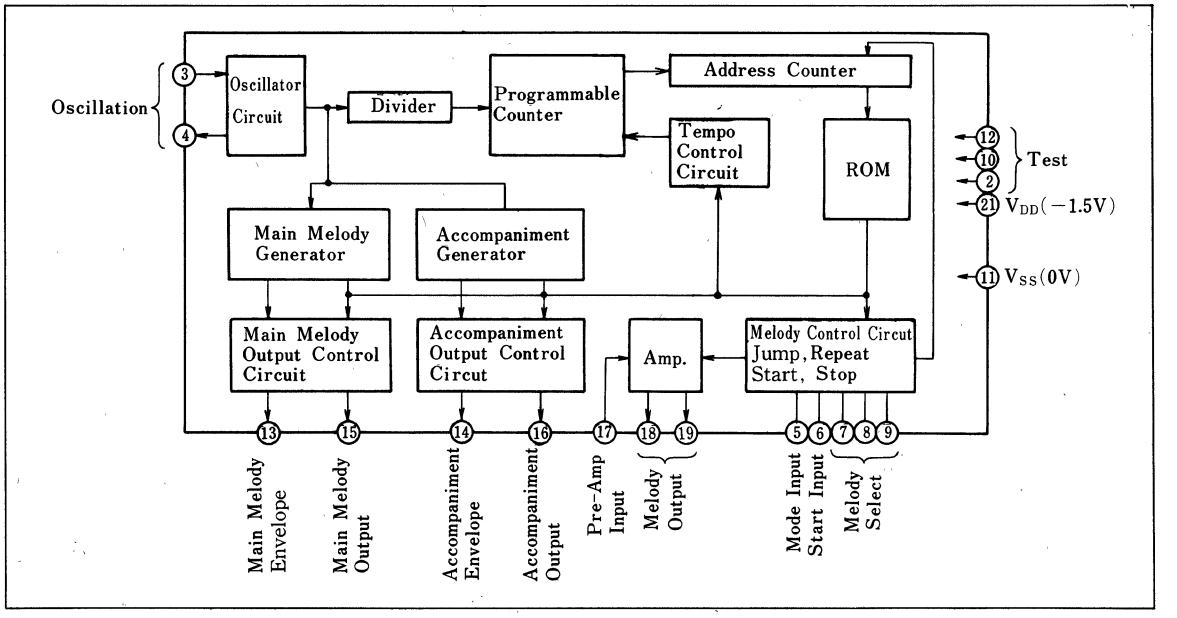
Features

1. Melody with accompaniment
2. Mask ROM programmable
3. 8 melodies (3-melody select inputs)
4. Loudness volume control function
5. Melody envelope controlled by external CR circuit
6. CR controlled oscillation system (with external resistor)
7. Single power supply : −1.5V
8. CMOS process
9. 22-pin dual-in line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*1	V_{T1}	+0.3～−3.0	V
Pin voltage*2	V_{T2}	+0.3～V_{DD}−0.3	V
Operating temperature	T_{opr}	−10～+50	℃
Storage temperature	T_{stg}	−20～+100	℃

* 1 : Applied to V_{DD} pin. Referenced to V_{SS}.
* 2 : Applied to pins other than V_{SS} and V_{DD}. Refers to the V_{SS} pin.

■ Recommended Operating Conditions (Ta=25℃)

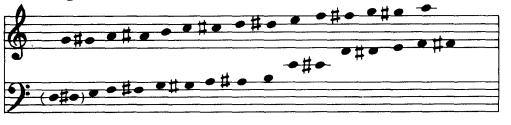
Parameter	Symbol	Specifications	Unit
Supply voltage	V_{DDa}	−2.0～−1.2	V
Ext. resistor for OSC	R_S	390±5%	kΩ

■ Electrical Characteristics (V_{DD}=−1.5V, Ta=25℃)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.3			V	1
	V_{IL}				−1.2		
Input current	I_{IH1}	V_{IH}=0V		2	10	μA	
	I_{IH2}	V_{IH}=0V	10		200	μA	2
Output current	I_{OH1}	V_{OH}=−0.5V	250			μA	3
	I_{OH2}	V_{OH}=−0.5V	3			μA	4
	I_{OL2}	V_{OL}=−1V	3				
	I_{OH3}	V_{OH}=−0.5V	5			μA	5
	I_{OL3}	V_{OL}=−1V	200				
	I_{OH4}	V_{OH}=−0.5V	200			μA	6
	I_{OL4}	V_{OL}=−1V	5				
Supply current	I_{DDS}	Standby state with no load			3	μA	
	I_{DDa}	Melody ON with no load			1	mA	

Note 1: Applied to ST, S_1-S_3, and MA pins.
Note 2: Applied to SI pin when melody is OFF.
Note 3: Applied to EV_1 and EV_2 pins.
Note 4: Applied to SO_1 and SO_2 pins.
Note 5: Applied to ML pin; I_{OH} is for melody OFF.
Note 6: Applied to MH pin; I_{OL} is for melody OFF.

■ Melody Specifications

〈No. of tunes〉 Max. 8
〈R O M〉 600 steps x 13 bits
〈Sound source〉 2 channels
〈Coverage〉 2.5 octaves

Note: given in parentheses are output only for attack sounds.

〈Tempo〉 Variable at 15 steps each (minimum length of note is selectable between 31 and 468 ms.)

〈Length of notes〉 2 types (other types are made available by controlling step count.)

If the shortest note in a tune is ♪, the two types of note, ♪ and ♩, can be specified in a step. The length of notes is controlled with "1" and "0".

♩ = ♪(1)+ ♪(0) ····· 2 steps
♩. = ♪(1)+ ♪(0)+ ♪(0) ····· 3 steps
♪ = ♪(1)+ ♪(0) ····· 2 steps

Numbers given in parenthese provide envelope control.

〈No. of repeated plays〉 1 to 15 endless
(A single play with auto stop can be specified by connecting the T_3 input to V_{DD}, overriding the number of repeated plays specified in ROM.)

〈Command types〉 Melody command
Control commands
- Jump command
- Set Repeat Count command
- End command

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〈Command configuration〉

I_1 ~I_5	Main melody tones
I_6	Main melody envelope control
I_7 ~ I_{11}	Accompaniment tones
I_{12}	Accompaniment envelope control
L_{13}	Length-of-note control

〈Music selection〉

One of eight pieces of music is selected by the status of the music select input S_1 to S_3. Since these inputs are provided with pull-down resistors, they may be connected to Vss or be left open.

If the status of the music select input is changed during play, the newly selected piece of music will be played from the beginning at that point.

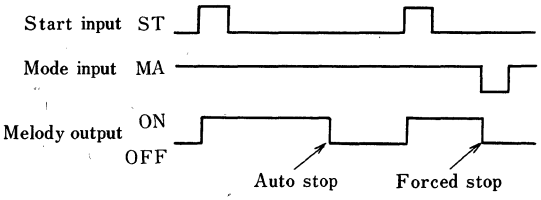
LR3461(A version of the LR3461 into which the following pieces of music have been written in at Sharp:)

S_1	S_2	S_3	Music	Remarks
H	H	H	For Elise	Beethoven
L	H	H	Lorelei	German song
H	L	H	The Smith in the Village	Japanese children's song
L	L	H	Romance of Love	Spanish song
H	H	L	Sakura Sakura	Japanese old folk song
L	H	L	Annie Rolley	Scottish song
H	L	L	Green Sleeves	English fork song
L	L	L	Cuckoo	German song

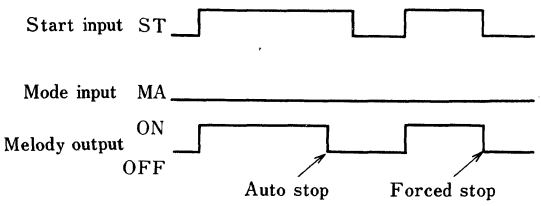
H: Vss, L: VDD or open (specifies endless for all the pieces.)

〈Melody Start / Stop〉

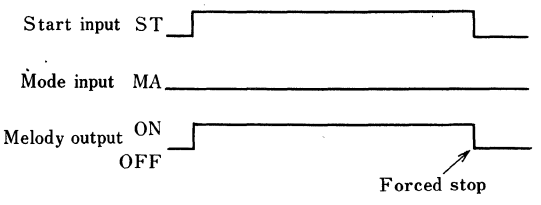
① One shot type (repeat 1~15 times)



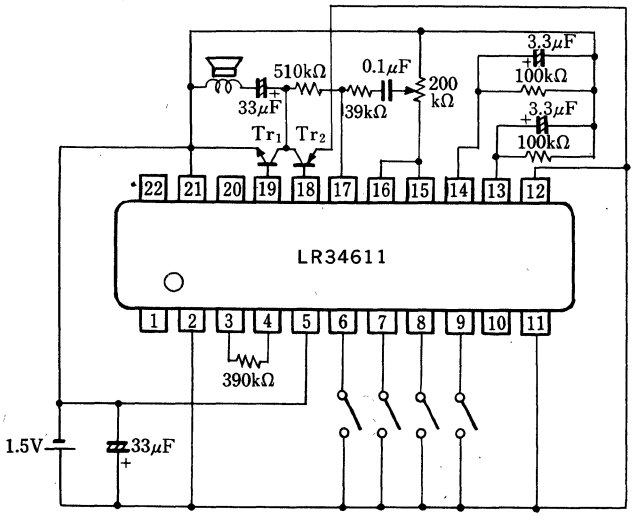
② Hold type (repeat 1~15 times)



③ Hold type (endless)



■ System Configuration



Tr1 : 2SC1383
Tr2 : 2SA683

LR3462 Electronic Melody Generator CMOS LSI

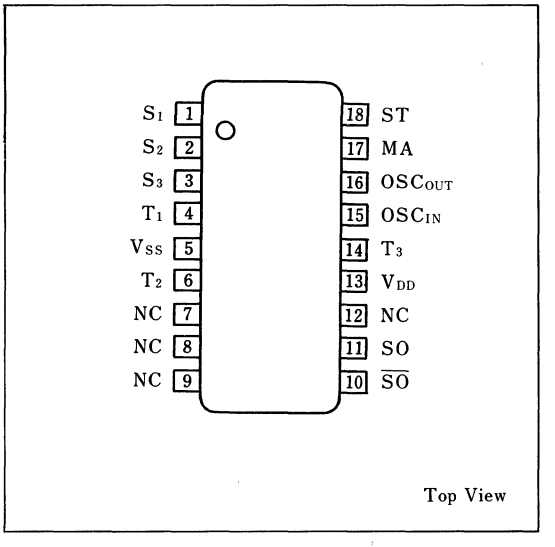
■ Description

The LR3462 is a CMOS LSI with melodies and alarm function.

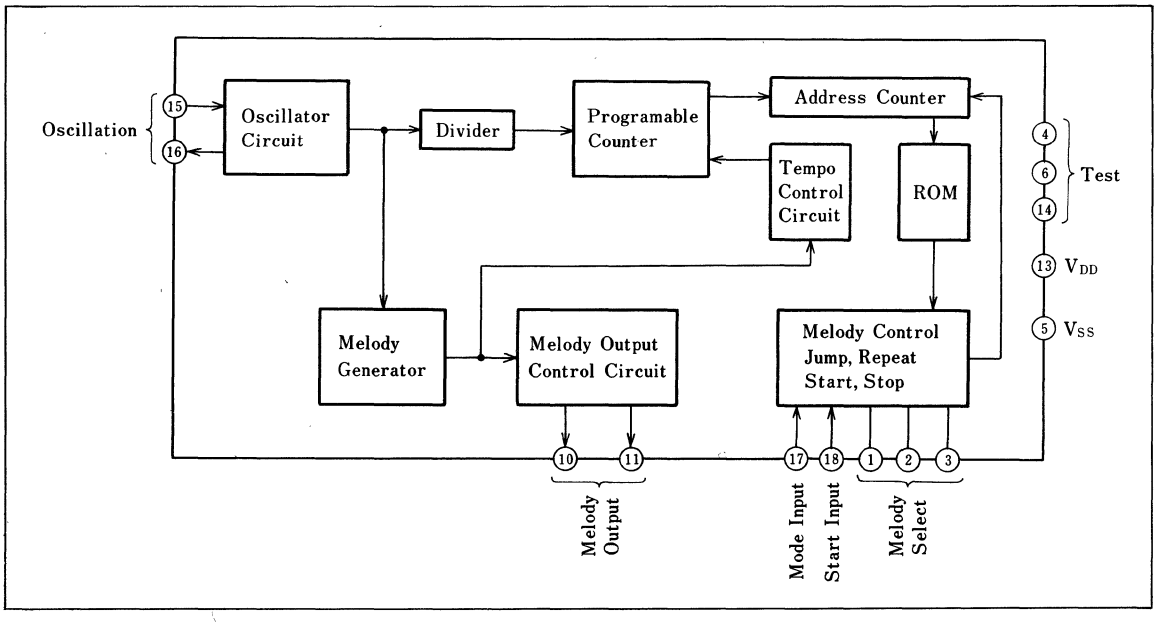
■ Features

1. Mask ROM programmable
2. 8 melodies (3-melody select input)
3. Capable of driving piezo-electric buzzer
4. CR controlled oscillation system (with external resistor)
5. Single power supply : −1.5V
6. 18-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{T1}	−0.3～+0.3	V	1,3
Pin voltage	V_{T2}	V_{TI}−0.3～+0.3	V	2,3
Operating temperature	T_{opr}	−10～+50	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note 1: Applied to V_{DD} pin.
Note 2: Applied to pins except V_{SS}, V_{DD}.
Note 3: Referenced to V_{SS}.

■ Recommended Operating Conditions

(Ta=25℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}	−2		−1.2	V	
Oscillator frequency	f_{OSC}		33		kHz	4

Note 4: The variable resistance R_S externally attached between pins 15 and 16 varies between 0 − 1MΩ. When variance in the oscillation frequency between pins is permitted, use a fixed resistance R_S=680kΩ±5%. (Note that when measuring the OSC_{OUT} signal, variations in the oscillation frequency may be caused by the input impedance of the measuring device.)

■ Electrical Characteristics

(V_{DD}=−1.5V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.3			V	5
	V_{IL}				−1.2		
Input current	I_{TH}	V_{IH}=0V		2	10	μA	
Output current	I_{OH}	V_{OH}=−0.5V	800			μA	6
	I_{OL}	V_{OL}=V_{DD}+0.5V	800				
Current consumption	I_{DDs}	Standby, no-load			3	μA	
	I_{DDa}	Merody ON, no-load			1	mA	

Note 5: Applied to pins ST, $\overline{S1}$, S2, S3, MA
Note 6: Applied to pins SO, $\overline{SO}$

■ Melody Specifications

〈Number of melodies〉 Max. 8
〈ROM〉 600 steps
〈Sound source〉 1 sequence
〈Sound range〉 2.5 octaves
〈Tempo〉 15 steps each (select minimum note length between 31 and 468 ms)
〈Note length〉 2 types (lengths other than these are realized by the number of steps)

Example : When the longest note in the melody is ♪, the two types of notes that can be specified for one step are 𝅘𝅥𝅯 and ♪. The length of notes is controlled using "1" and "0".

♩ = ♪ (1) + ♪ (0) ····· 2 steps
♩. = ♪ (1) + ♪ (0) + ♪ (0) ····· 3 steps
𝅗𝅥. = ♪ (1) + ♪ (0) ····· 7 steps

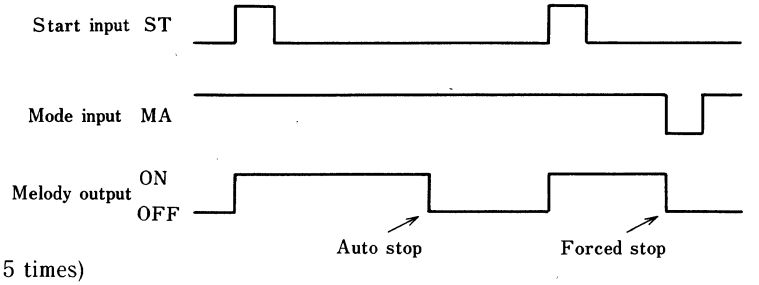
value in parentheses ( ) : envelope control
〈Times played〉 1 to 15 or endless (by connecting the T_3 input to V_{DD}, the melody can be set to play once and then turn off automatically.)
〈Commands〉 Melody commands

Control commands
- Jump command
- Times repeat command
- End command

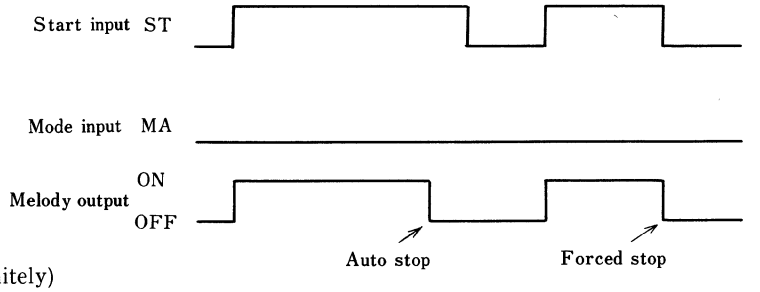
〈Melody selection〉 One of the eight melodies is selected depending on the state of the melody selection inputs S_1~S_3. The melody selection input pins have a built-in pull-down resistance, so they can be connected to V_{SS} or used open. When the state of the melody selection inputs changes during play, the melody specified is played from the first.

〈Melody start and stop〉

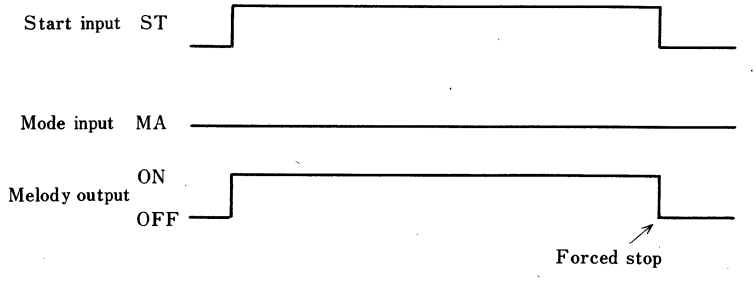
(1) **One shot type** (repeats 1 to 15 times)



(2) **Hold type** (repeats 1 to 15 times)



(3) **Hold type** (repeats indefinitely)



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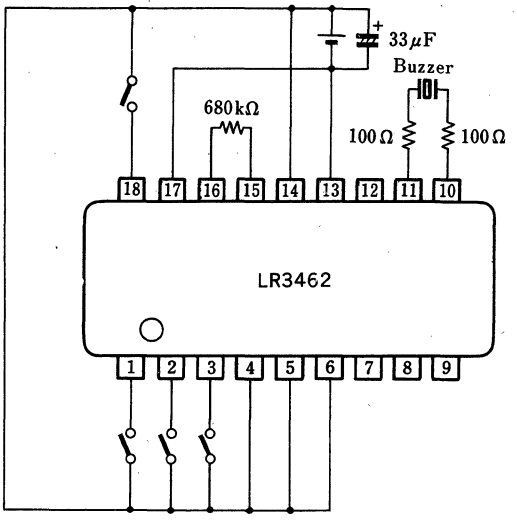
System Configuration



LR3462/ (LSI with melodies written by Sharp)

S_1	S_2	S_3	Melody
H	H	H	When the Saints Go Marching in
L	H	H	Twinkle Twincle Little Star
H	L	H	Bridal March
L	L	H	Silent Night
H	H	L	O Sole Mio
L	H	L	For Elise
H	L	L	Wedding March
L	L	L	Jingle Bells

H: High, L: Low

LR3681 Voice Synthesizer CMOS LSI

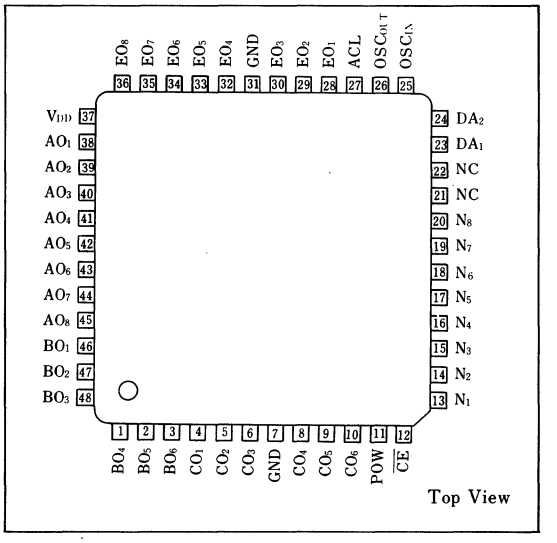
■ Description

The LR3681 is a voice synthesizer CMOS LSI. The integration of all the functions required for generating voice output enables voice synthesizer systems to be easily composed.

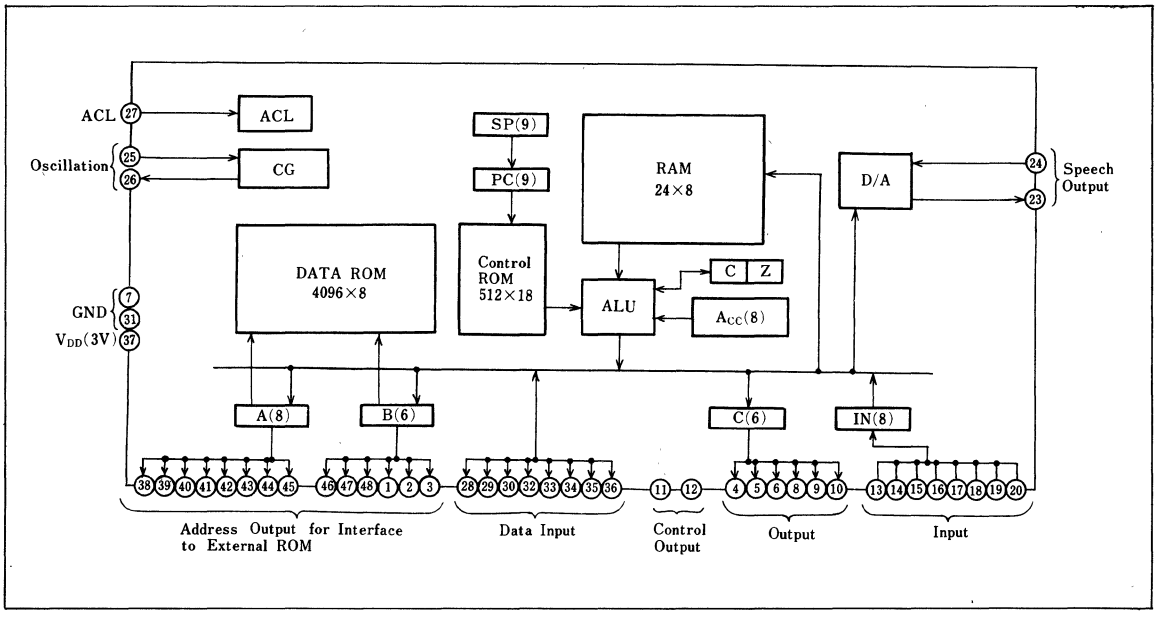
■ Features

1. Voice output period of time : 4 ~ 5sec
   (The voice quality is determined by the length of voice generated)
2. Available sound sources include male, female voices and effect sounds
3. Voice synthesis method is based on a waveform encoding system
4. 32K bits of data ROM on chip
5. Expandable up to 128K bits of external ROM
6. Internal 8-bit of D/A converter
7. Time base : 4.19MHz crystal
8. Single power supply : −3V
9. CMOS process
10. 48-pin quad-flat package

■ Pin Connections



■ Block Diagram



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■ Absolute Maximum Ratings

Perameter	Symbol	Ratings	Unit	Note
Pin voltage 1	V_{DD}	−6.0～+0.3	V	
Pin voltage 2	V_{IN}	V_{DD}−0.3～+0.3	V	1
Operating temperature	T_{opr}	−20～+70	℃	
Storage temperature	T_{stg}	−55～+150	℃	

The maximum applicable voltage on any pin with respect to V_{SS}.

Note 1: Applied to pins N_1-N_8, $\overline{CE}$, $\overline{POW}$, DA_1, DA_2, OSC_{IN}, OSC_{OUT}, EO_1~EO_8. AO_1~AO_8, BO_1~BO_6, and CO_1~CO_6.

■ Recommended Operating Conditions

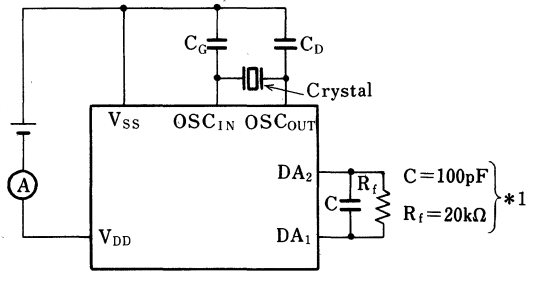
Parameter	Symbol	Specifications	Unit
Supply voltage	V_{DD}	−2,7～−3.3	V
Oscillator frequency	f_{OSC}	4.1943 (TYP.)	MHz

■ Electrical Characteristics

(V_{DD}=−3.0V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.6			V	2
	V_{IL}				V_{DD}+0.6		
Input current	I_{IH1}	V_{IN}=0V	2		30	μA	3
	I_{IH2}	V_{IN}=0V	2		30	μA	4
	I_{IH3}	V_{IN}=0V			3	μA	5
Output current	I_{OH1}	V_{OUT}=−0.5V	100			μA	6
	I_{OL1}	V_{OUT}=V_{DD}+0.5V	100				
	I_{OH2}	V_{OUT}=−0.5V	100			μA	7
	I_{OL2}	V_{OUT}=V_{DD}+0.5V	100				
D/A converter bits				8		bit	8
D/A converter monotonicity		Rf open	6			bit	9
Max. output voltage amplitude	V_{PP}	Rf = 20kΩ, C=100pF, Rf = 20kΩ	1	1.7		V	10
Oscillation start time	T_{OSC}	V_{DD}=−2.7～−3.3V			50	ms	11
Current consumption	I_{total}	During region-wide operation		1.5		mA	12
	I_{CEND}	During standby			1	μA	

Note 2: Applied to pins ACL, N_1 - N_4, and EO_1 - EO_8.
Note 3: Applied to pins N_1 - N_8.
Note 4: Applied to pins EO_1 - EO_8.
Note 5: Applied to the ACL pin.
Note 6: Applied to pins AO_1 - AO_8, BO_1 - BO_6, and CO_1 - CO_6.
Note 7: Applied to pins $\overline{CE}$ and $\overline{ROW}$.
Note 8: Applied to the built-in DA converter.
Note 9: Applied to pin DA_2, with resistor Rf connected to pins DA_1 and DA_2 left open.
Note 10: Applid to pin DA_1. The difference in the output voltages at DA_1,V_{DA1} (00) and V_{DA1} (FF), obtained when the input data to D/A converter is 00 and FF, respectively is: V_{DA1} (00)-V_{DA1} (FF)=Vp-p (where Rf=20 KΩ*1).
Note 11: Applied to pins OSC_{IN} and OSC_{OUT} (C_D=C_G=5 pF). Refers to the time required for the LSI to enter the region-wide operating status ($\overline{POW}$ rises) from the rising edge of the N_2 pin under standby status.
Note 12: Measurement circuit



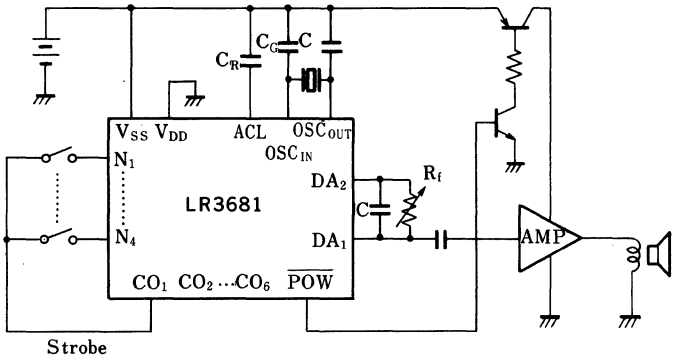
Crystal : 4.1943MHz ceramic oscillator
C_G=C_D=5pF

■ System Configuration

(1) Stand-alone LSI configuration

Pressing one, out of the eight switches (N_1-N_8) connected to the input pins, produces the corresponding speech message. The number of connectable switches can be increased to 32 by building a matrix with the output pins.

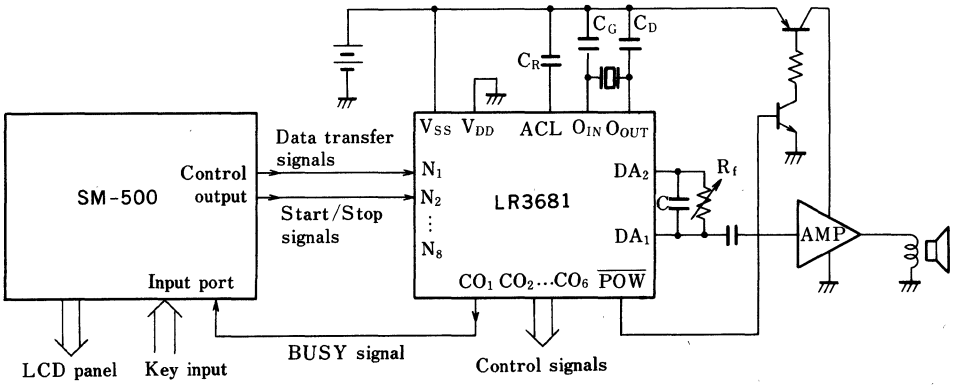
The voice output's maximum amplitude is almost equal to the supply voltage. It is amplified by a power amplifier to drive a speaker. A simple low-pass filter (CR network, etc.) should be used to eliminate RF noise.



(2) System combined with a microcomputer

A microcomputer may be used to command the voice synthesizer LSI to produce a specific speech message. The device can be readily interfaced with the CMOS version of the SM Series.

The following figure shows a sample system configuration in which serial data is transferred from the SM-500 to pin N_1 of the device:



Note N2: Starts in the standby mode.

■ Developing Procedure

The following table shows a typical procedure for developing the LR3681 with customized specifications:

	Parameter	Description	Responsible Party
1	System specs	Determines the I/O formats for the LSI, interface with microcomputer, etc.	Customer
2	Synthesized voice tone	Selects the tone from the samples provided by Sharp.	Customer
3	Determination of speech message	Specifies the words to be written into the device, extracts common words, and creates the recording manuscript.	Customer Sharp
4	Recording	As a rule, a professional announcer records the contents of the recording manuscript onto a tape, in a noise-free environment.	Customer
5	Recorded tape check	Checks the recorded tape for noise and proper recording level. If any problem is found, Sharp requests the customer to record once again.	Sharp
6	Voice analysis	Inputs the recorded message into a computer, where it is subjected to voice analysis and data compression for writing into ROM.	Sharp
7	ROM writing	Writes the resulting voice data into PROM, and programs the control section for I/O and other operations.	Sharp
8	Emulation for voice tone and LSI functions	Emulates the PROM containing data to evaluate the tone of the recorded voice as well as the systems operations.	Customer
9	LSI mask generation	If the result of emulation was positive, Sharp creates the mask for LSI device.	Sharp
10	TS submission	Fabricates test sample devices, tests them, and submits them to the customer.	Sharp
11	TS evaluation	Customer evaluates the sample devices.	Customer
12	ES submission	Sharp submits engineering samples.	Sharp

LI2048 5 × 7 Dot Matrix Decoder PMOS LSI

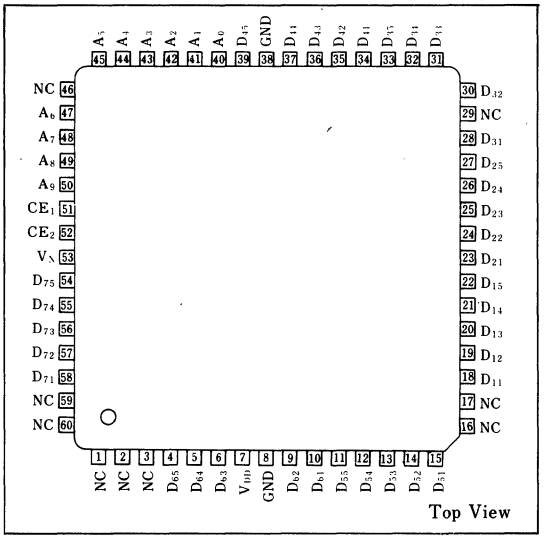
■ Description

The LI2048 is a PMOS LSI capable of driving 5 × 7 dot-matrix vacuum-fluorescent displays, and displaying 128 kinds of pattern.

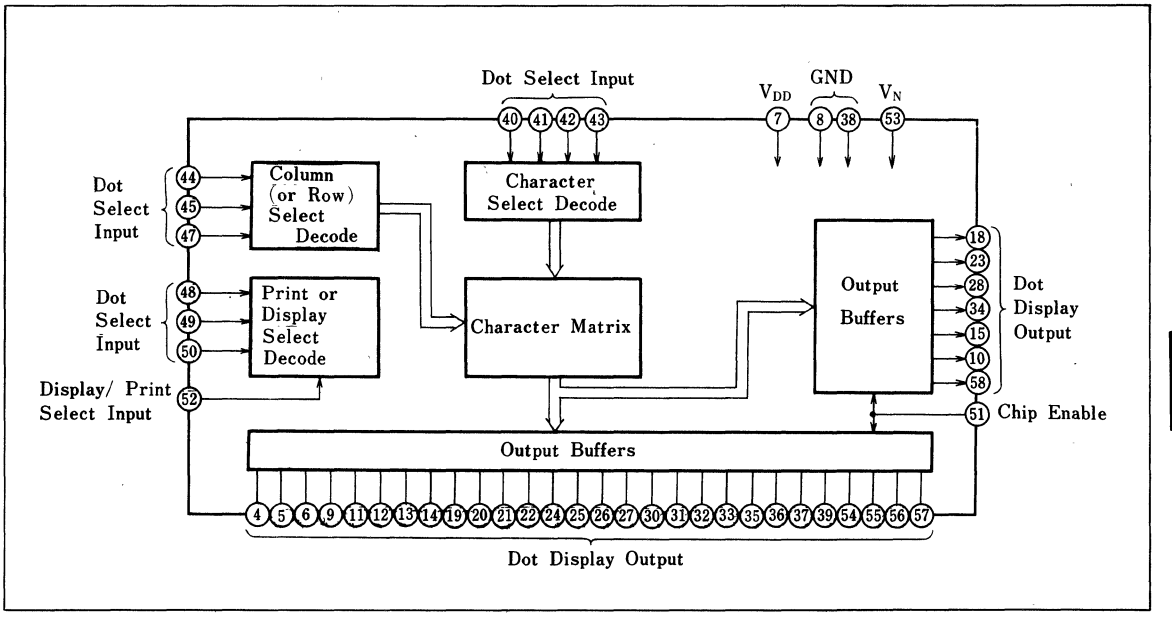
■ Features

1. 128 patterns display
2. Direct drive of vacuum-fluorescent displays
3. Printer drive output
4. TTL level voltage drive
5. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*	V_{DD}	−20～+0.3	V
	V_N	−44～+0.3	V
	V_{IN}	−44～+0.3	V
Operating temperature	T_{opr}	−5～+55	℃
Storage temperature	T_{stg}	−55～+150	℃

*Referenced to GND.

■ Recommeded Operating Conditions

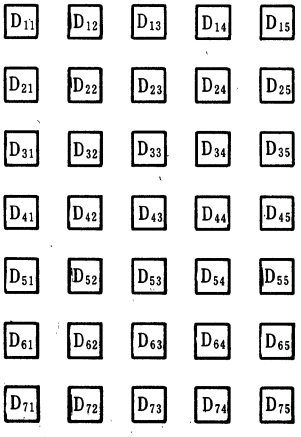
Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−8.1～−9.9	V
Display voltage	V_N	−40	V

■ Electrical Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	V_{IH}		−1.1			V
	V_{IL}				−4.2	
Output voltage	V_{OH1}	I_{OH}=3.0mA	−1.0			V
	V_{OH2}	I_{OH}=1.0mA	−1.0			
	V_{OL}	V_{IN}=−40V			−36.5	
Current consumption	I_{DD}	V_{DD}=−9.0V		8.5		mA
	I_N	V_N=−40V		3.0		
Output delay time	t_{U1}	V_{IN}=−40V		4.0		μs
	t_{d1}	No loading		5.5		
	t_{U2}	V_N=−40V		5.0		
	t_{d2}	Loading capacity; 100pF.		15.0		
Input resistance	R_{IN}	V_{IN}=−40V	1.0			MΩ

■ Function

(1) Dot matrix arrangement



(2) Dot data output

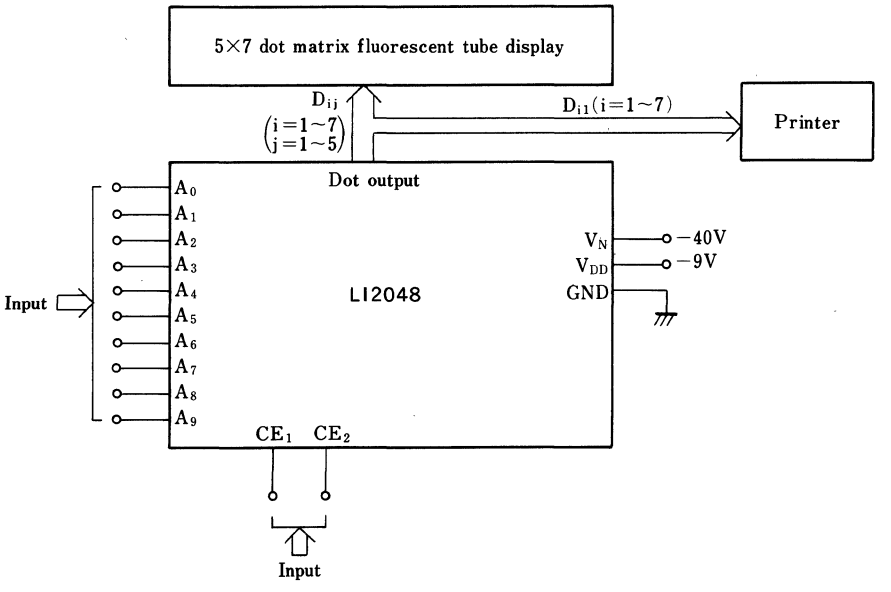
(i) For low CE_1 and CE_2 inputs.
Dot data output is determined by input $A_0 - A_6$.

(ii) For low CE_1 and high CE_2 inputs.
Dot data determined by input $A_0 - A_6$ is stored by input $A_7 - A_9$ and outputted as dot data output D_{i1} (i=1−7) to the printer.

(iii) For high input CE_1.
No dot data output.

Input					D_{ij} output						
CE_1	CE_2	A_7	A_8	A_9	D_{11}	D_{21}	D_{31}	D_{41}	D_{51}	D_{61}	D_{71}
0	1	1	0	0	D_{11}	D_{21}	D_{31}	D_{41}	D_{51}	D_{61}	D_{71}
		0	1	0	D_{12}	D_{22}	D_{32}	D_{42}	D_{52}	D_{62}	D_{72}
		1	1	0	D_{13}	D_{23}	D_{33}	D_{43}	D_{53}	D_{63}	D_{73}
		0	0	1	D_{14}	D_{24}	D_{34}	D_{44}	D_{54}	D_{64}	D_{74}
		1	0	1	D_{15}	D_{25}	D_{35}	D_{45}	D_{55}	D_{65}	D_{75}
		0	1	1	No dot data output						
		1	1	1							
		0	0	0							

■ System Configuration



LH5008 LCD Controller / Driver CMOS LSI

■ Description

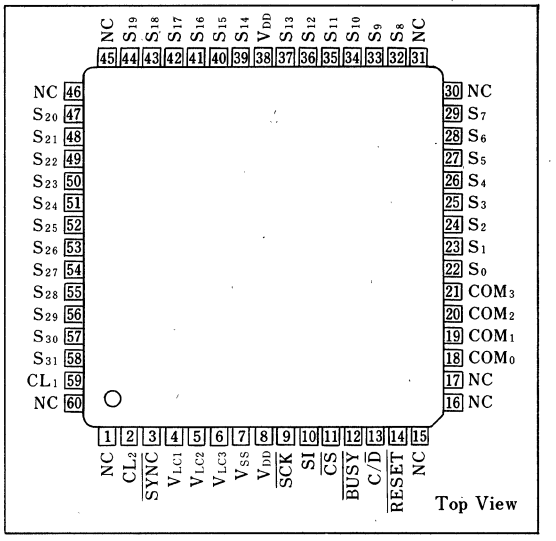
The LH5008 is a programmable LCD controller/driver which interfaces in serial fashion to the CPU of a microcomputer application system to directly control and drive LCDs in static operation or dynamic operation (1/2, 1/3 or 1/4-duty cycle).

The LH5008 incorporates a segment decoder for generating specific segment patterns, and is also capable of controlling the blinking of the display.

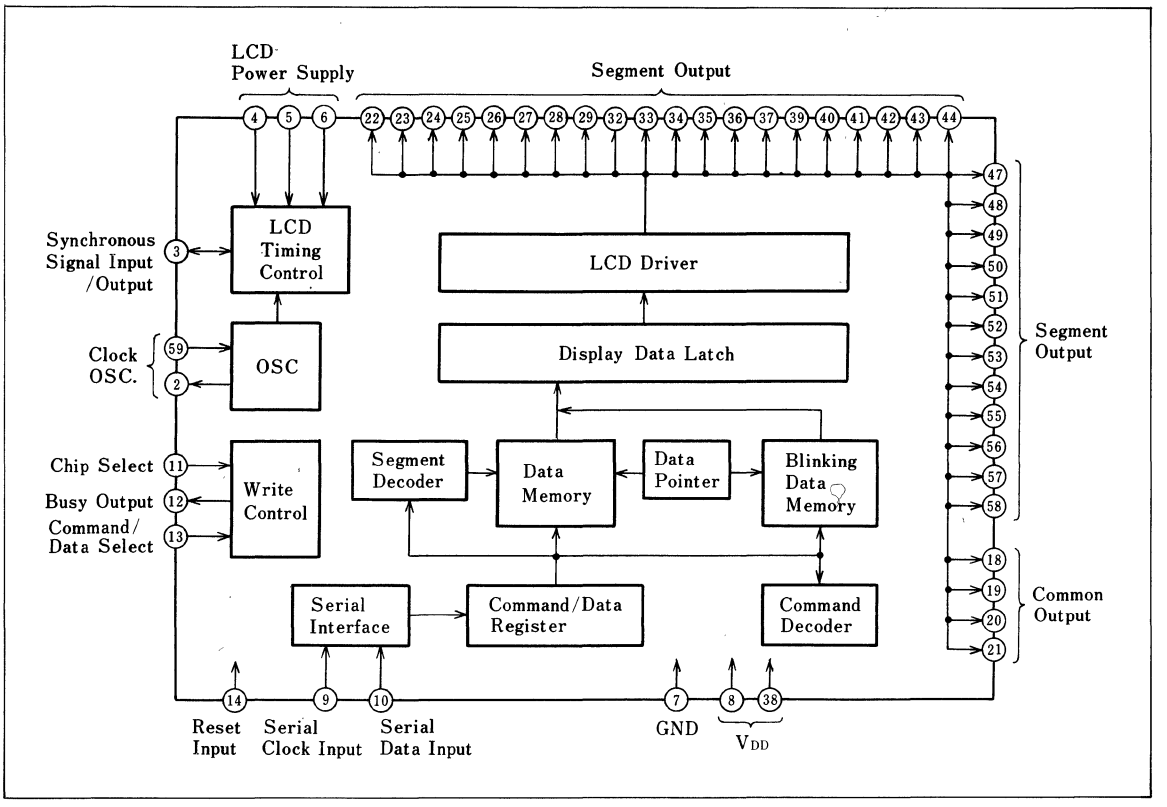
■ Features

1. CMOS process
2. Number of display digits
   - 7-segment device
     - 1/4-duty cycle ····· 16 digits
     - 1/3-duty cycle ····· 10⅔ digits
     - 1/2-duty cycle ····· 8 digits
     - Static operation ·····4 digits
   - 14-segment device
     - 1/4-duty cycle 8 digits
3. Operating mode
   Static, 1/2, 1/3, and 1/4-duty drive
4. Biasing
   Static, 1/2 and 1/3
5. Segment decoder output
   - 7-segment device ; numerics 0 ~ 9 and 5 symbols
   - 14-segment device ; 36 alphanumerics and 12 symbols
6. Blinking function
7. LCD direct drive
8. Serial input (8-bit unit)
9. Capable of multi-chip configuration
10. Single power supply : + 5V
11. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Pin Description

Pin name	No. of pins	I/O	Connect to	Functions
V_{DD}, V_{SS}	3	I	Power supply	Power supply for logic circuit
V_{LC1}, V_{LC2}, V_{LC3}	3			Power supply for liquid crystal drive
SI	1		MPU	Serial data input
$\overline{SCK}$	1			Clock input for data shift
C/$\overline{D}$	1			Data/command select pin
$\overline{CS}$	1			Chip select pin
$\overline{RESET}$	1			Reset input
CL_1	1		Resistance	Internal clock oscillation pin
CL_2	1	O	Resistance	Internal clock oscillation pin
$S_0 \sim S_{31}$	32		Liquid crystal	Liquid crystal segment drive signal
$COM_0 \sim COM_3$	4			Liquid crystal common drive signal
$\overline{BUSY}$	1		MPU	Busy output
$\overline{SYNC}$	1	I/O	LH5008	Sync. signal

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3～+7.0	V	1
Input voltage	V_{IN}	−0.3～V_{DD}+0.3	V	
Output voltage	V_{OUT}	−0.3～V_{DD}+0.3	V	
Operating temperature	T_{opr}	−10～+70	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note 1: Referenced to V_{SS}.

■ Recommend Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.7		5.5	V
Oscillator frequency	f_{OSC}	R=200kΩ, V_{DD}=5V±10%		130		kHz
		R=240kΩ, V_{DD}=3V±10%		100		

■ DC Characteristics

(V_{DD}=5V±10%, Ta=−10～70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		0.7V_{DD}		V_{DD}	V	
	V_{IL}		0		0.3V_{DD}	V	
Input leakage current	$\lvert I_{LIH} \rvert$	$V_{IN}=V_{DD}$			2	μA	
	$\lvert I_{LIL} \rvert$	$V_{IN}=0V$			2	μA	
Output leakage current	$\lvert I_{LOH} \rvert$	$V_{OUT}=V_{DD}$			2	μA	
	$\lvert I_{LOL} \rvert$	$V_{OUT}=0V$			2	μA	
Output current	I_{OH1}	$\overline{SYNC}$, $\overline{BUSY}$ $V_{OUT}=V_{DD}-0.5V$	10			μA	
	I_{OH2}	$\overline{SYNC}$, $V_{OUT}=1V$			300	μA	
	I_{OL1}	$\overline{SYNC}$, $V_{OUT}=1V$	900			μA	
	I_{OL2}	$\overline{BUSY}$, $V_{OUT}=0.5V$	350			μA	
Output resistance	R_{COM}	COM_0～COM_3 $V_{DD}\geqq V_{LCD}\geqq 2.7V$		3	7	kΩ	2
	R_{SEG}	S_0～S_{31} $V_{DD}\geqq V_{LCD}\geqq 2.7V$		7	14	kΩ	
Current consumption	I_{DD}	No-load, external clock f_C=200kHz		100	250	μA	

(V_{DD}=2.7～4.5V, Ta=−10～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}	Except $\overline{SCK}$	0.7V_{DD}		V_{DD}	V	
	V_{IH2}	$\overline{SCK}$	0.8V_{DD}		V_{DD}	V	
	V_{IL1}	Except Except $\overline{SCK}$	0		0.3V_{DD}	V	
	V_{IL2}	$\overline{SCK}$	0		0.2V_{DD}	V	
Input leakage current	$\lvert I_{LTH} \rvert$	$V_{IN}=V_{DD}$			2	μA	
	$\lvert I_{LIL} \rvert$	$V_{IN}=0V$			2	μA	
Output leakage current	$\lvert I_{LOH} \rvert$	$V_{OUT}=V_{DD}$			2	μA	
	$\lvert I_{LOL} \rvert$	$V_{OUT}=0V$			2	μA	
Output current	I_{OH1}	$\overline{SYNC}$, $\overline{BUSY}$ $V_{OUT}=V_{DD}-0.75V$	7			μA	
	I_{OH2}	$\overline{SYNC}$, $V_{OUT}=0.5V$			200	μA	
	I_{OL1}	$\overline{SYNC}$, $V_{OUT}=0.5V$	400			μA	
	I_{OL2}	$\overline{BUSY}$, $V_{OUT}=0.5V$	150			μA	
Output resistance	R_{COM}	COM_0～COM_3 $V_{DD}\geqq V_{LCD}\geqq 2.7V$		6	12	kΩ	2
	R_{SEG}	S_0～S_{31} $V_{DD}\geqq V_{LCD}\geqq 2.7V$		12	24	kΩ	
Current consumption	I_{DD}	No-load, external clock f_C=160kHz V_{DD}=3V±10%		30	100	μA	

Note 2: Applicable to static, 1/2 bias, 1/3 bias; V_{LCD}: LCD drive voltage

■ AC Electric Characteristics

(V_{DD}=5V±10%, Ta=−10~70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_C		50		200	kHz
Oscillator frequency	f_{OSC}	R=200kΩ+5%	85	130	175	kHz
High-level clock pulse width	t_{WHC}	CL_1, external clock	2		16	μs
Low-level clock pulse width	t_{WLC}	CL_1, external clock	2		16	μs
$\overline{SCK}$ frequency	t_{CYK}		900			ns
High-level $\overline{SCK}$ pluse width	t_{WHK}		400			ns
Low-level $\overline{SCK}$ pluse width	t_{WLK}		400			ns
$\overline{BUSY}$ ↑ →$\overline{SCK}$ hold time	t_{HBK}		0			ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SIK}		250			ns
SI hold time (to $\overline{SCK}$ ↑)	t_{HKI}		200			ns
Delay of 8th $\overline{SCK}$ ↑ →$\overline{BUSY}$ ↓	t_{DKB}	Load capacitance = 50 pF			3	μs
$\overline{CS}$ ↓ →$\overline{BUSY}$ ↓ delay	t_{DCSB}	Load capacitance = 50 pF			1.5	μs
C/$\overline{D}$ setup time (to 8th $\overline{SCK}$ ↑)	t_{SDK}		9			μs
C/$\overline{D}$ hold time (to 8th $\overline{SCK}$ ↑)	t_{HKD}		1			μs
$\overline{CS}$ hold time (to 8th $\overline{SCK}$ ↑)	t_{HKCS}		1			μs
High-level/$\overline{CS}$ pluse width	t_{WHCS}		$8t_{CYC}$*			μs
Low-level/$\overline{CS}$ pluse width	t_{WLCS}		$8t_{CYC}$*			μs
$\overline{SYNC}$ load capacitance	C_{LSY}	t_{CYC}*=5 μs			50	pF

* $t_{CYC}=1/f_C$

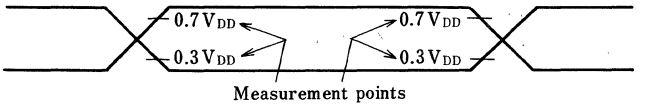
(V_{DD}=2.7V~4.5V, Ta=−10~70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_C		50		140	kHz
Oscillator frequency	f_{OSC}	R=240kΩ±5% V_{DD}=3V±10%	50	100	140	kHz
High-level clock pulse width	t_{WHC}	CL_1, external clock	3		16	μs
Low-level clock pulse width	t_{WLC}	CL_1, external clock	3		16	μs
$\overline{SCK}$ frequency	t_{CYK}		4			μs
High-level $\overline{SCK}$ pluse width	t_{WHK}		1.8			μs
Low-level $\overline{SCK}$ pluse width	t_{WLK}		1.8			μs
$\overline{BUSY}$ ↑ →$\overline{SCK}$ hold time	t_{HBK}		0			ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SIK}		1			μs
SI hold time (to $\overline{SCK}$ ↑)	t_{HKI}		1			μs
Delay of 8th $\overline{SCK}$ ↑ →$\overline{BUSY}$ ↓	t_{DKB}	Load capacitance=50 pF			5	μs
$\overline{CS}$ ↓ →$\overline{BUSY}$ ↓ delay	t_{DCSB}	Load capacitance=50 pF			5	μs
C/$\overline{D}$ setup time (to 8th $\overline{SCK}$ ↑)	t_{SDK}		18			μs
C/$\overline{D}$ hold time (to 8th $\overline{SCK}$ ↑)	t_{HKD}		1			μs
$\overline{CS}$ hold time (to 8th $\overline{SCK}$ ↑)	t_{HKCS}		1			μs
High-level/$\overline{CS}$ pluse width	t_{WHCS}		$8t_{CYC}$*			μs
Low-level/$\overline{CS}$ pluse width	t_{WLCS}		$8t_{CYC}$*			μs
$\overline{SYNC}$ load capacitance	C_{LSY}	t_{CYC}*=6.25 μs			50	pF

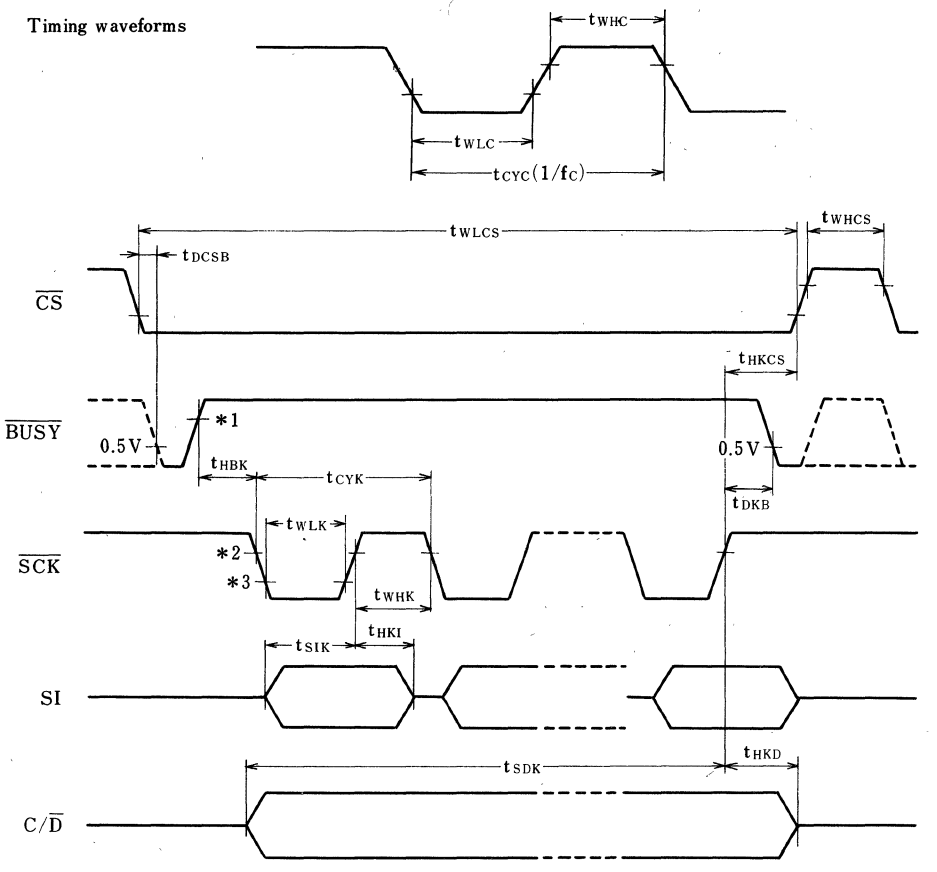
* $t_{CYC}=1/f_C$

■ AC Timing Diagram

Timing measurement voltage level

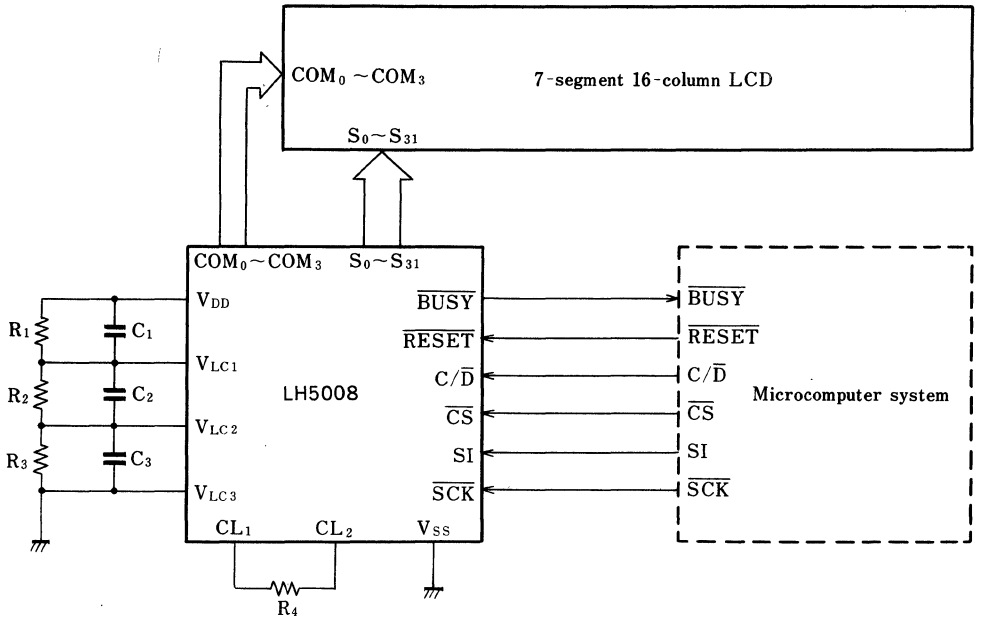


Timing waveforms



*1 : $V_{DD}-0.5V$ at $V_{DD}=5V\pm10\%$, $V_{DD}-0.75V$ at $V_{DD}=2.7\sim4.5V$
*2 : $0.8V_{DD}$ at $V_{DD}=2.7\sim4.5V$
*3 : $0.2V_{DD}$ at $V_{DD}=2.7\sim4.5V$

■ System Configuration



LR3691A LCD Dot Matrix Controller CMOS LSI

■ Description

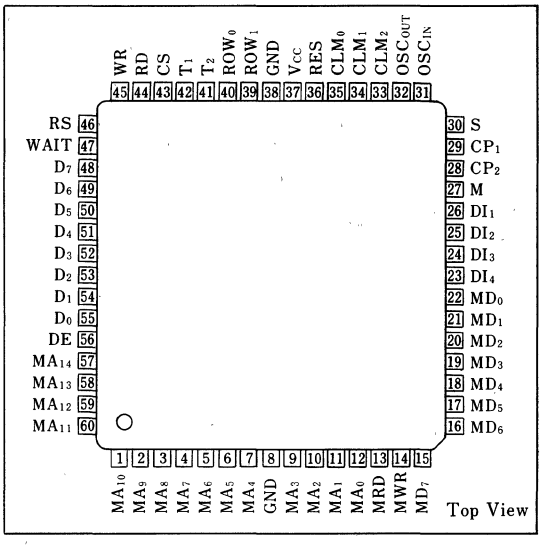
The LR3691A is a controller CMOS LSI for dot matrix graphic LCD units. It stores display data corresponding to dot patterns from the 8-bit CPU in the external RAM. From this RAM, it transfers the display data to the LCD driver and generates clocks necessary to drive the LCD.

■ Features

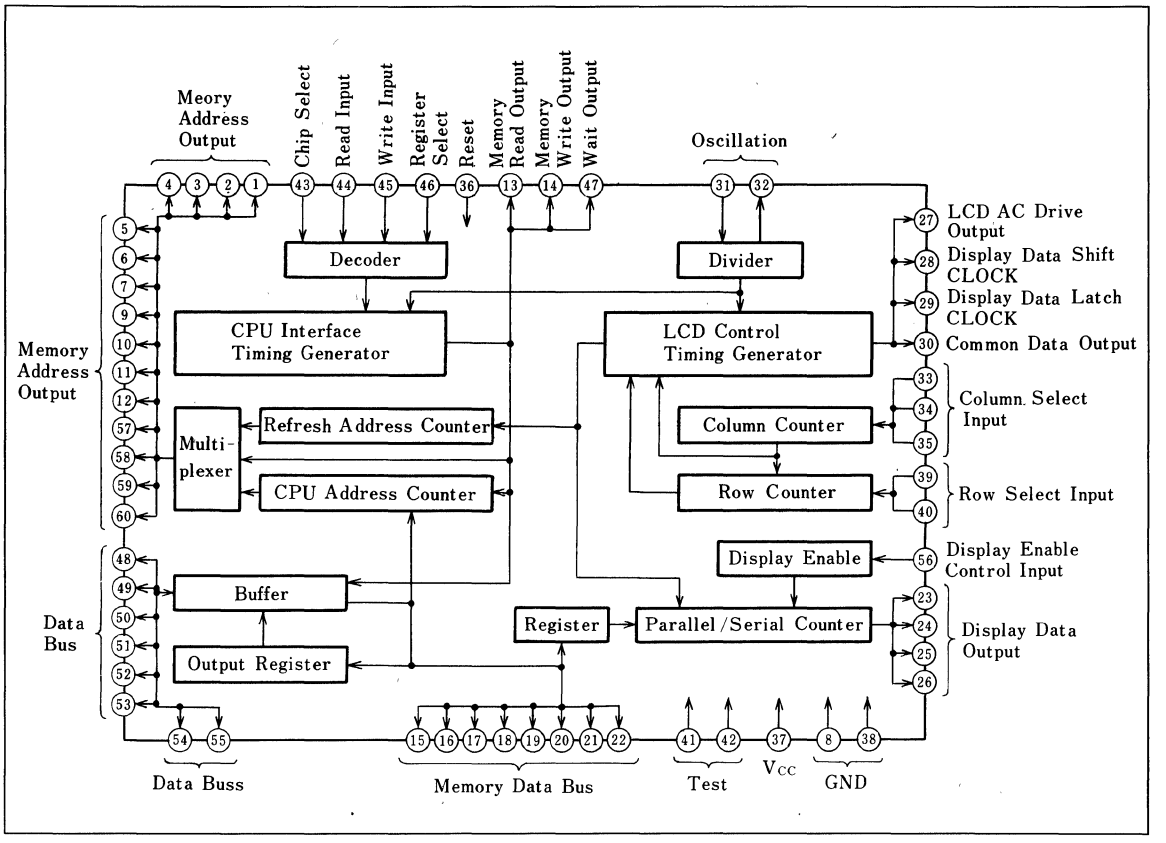
1. Controller for LCD dot matrix graphic display
2. Maximum display data = 163, 840 dots (Horizontal × Vertical)
3. General 8-bit CPU interface
4. High-speed write cycle
5. Low frequency due to parallel output of data to 4 divisions of the LCD
6. Selectable display dots
   a. The number of horizontal dots
   - The LCD without right and left divisions
     120, 160, 240, 320, 480, 640 dots
   - The LCD with right and left divisions
     240, 320, 480, 640, 960, 1280 dots

   b. The number of vertical dots
   - The LCD without upper and lower divisions
     32, 64, 100, 128 dots
   - The LCD with upper and lower divisions
     64, 128, 200, 256, dots
7. Single power supply : 5V (TYP.)
8. CMOS process
9. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{CC}	−0.3~+7	V	1
Input voltage	V_I	−0.3~V_{CC}+0.3	V	1
Output voltage	V_O	−0.3~V_{CC}+0.3	V	1
Operating temperature	T_{opr}	−10~+70	°C	
Storage temperature	T_{stg}	−55~+150	°C	

Note 1: The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_I	0		V_{CC}	V
Output low current	I_{OL}			4	mA
Output high current	I_{OH}			−500	μA
Clock frequency	f_{osc}	0.6		6.6	MHz

Note : Any current sinks into the LSI is regarded posititve.

■ DC Characteristics

(V_{CC}=5V±10%, GND=0V, Ta=−10~+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Output low voltage	V_{OL1}	I_{OL}=4mA			0.4	V	1,2
	V_{OL2}	I_{OL}=400 μA			0.2V_{CC}	V	3
Output high voltage	V_{OH1}	I_{OH}=−0.5mA	2.4			V	1,2
	V_{OH2}	I_{OH}=−400 μA	0.8V_{CC}			V	3
Input low voltage	V_{IL1}				0.4	V	2,4
	V_{IL2}				0.5	V	5
Input high voltage	V_{IH1}		2.4			V	2,4
	V_{IH2}		V_{CC}−0.6			V	5
Input low current	I_{IL1}	V_{IL}=0V			−20	μA	4,5
	I_{IL2}	V_{IL}=0V		−30	−100	μA	2
Input high current	I_{IH}	V_{IH}=V_{CC}			20	μA	2,4,5
Current consumption	I_{CC}	fosc=6.6MHz		12	36	mA	

MD_0~MD_7 and D_0~D_7 are I/O pins which are pulled up by built-in resistors when in input mode.

Note 1: Applied to output pins other than CP_1, CP_2, S, M, DI_1~DI_4, and OSC_{OUT}.

Note 2: Applied to pins MD_0~MD_7 and D_0~D_7.

Note 3: Applied to pins CP_1, CP_2, S, M, DI_1~DI_4, and OSC_{OUT}

Note 4: Applied to input pins other than OSC_{IN}, T_1 and T_2.

Note 5: Applied to pins OSC_{IN}, T_1, and T_2.

■ AC Characteristics

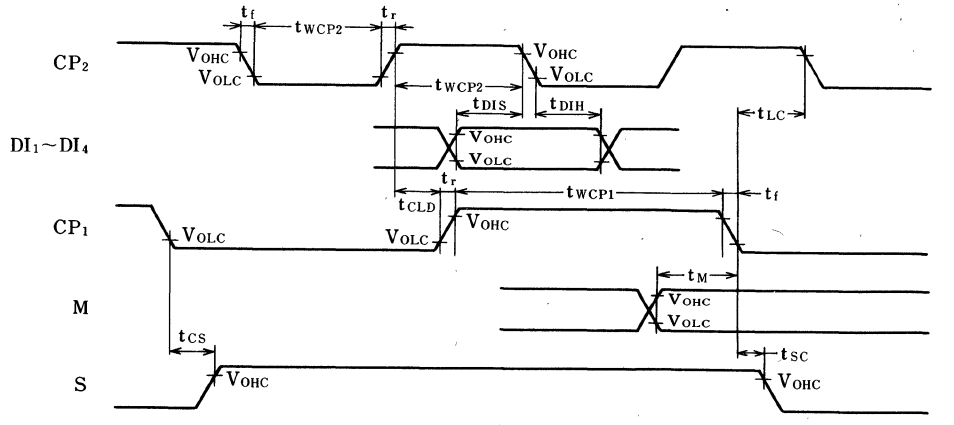
(1) LCD control timing

(V_{CC}=5V±10%, Ta=−10~+70℃)

Parameter	Symbol	MIN.	TYP	MAX.	Unit
CP_2 clock width	t_{WCP2}	ϕ−50	ϕ		ns
Data setup time	t_{DIS}	ϕ−100	ϕ		ns
Data hold time	t_{DIH}	ϕ−100	ϕ		ns
Clock setup time (CP_1 ↓ → CP_2 ↓)	t_{LC}	20	ϕ/2	ϕ/2+25	ns
Clock setup time (CP_2 ↑ → CP_1 ↑)	t_{CLD}	20	ϕ/2		ns
CP_1 clock width	t_{WCP1}	2·ϕ−50	2ϕ		ns
Fall time of CP_1 referring to M signal	t_M	−(ϕ/2+100)	−ϕ/2	ϕ	ns
Clock setup time (CP_1 ↓ → S ↓)	t_{SC}	200			ns
Clock setup time (CP_1 ↓ → S ↑)	t_{CS}	200			ns
Rise time of CP_1 and CP_2	t_r		30	50	ns
Fall time of CP_1 and CP_2	t_f		30	50	ns

Measurement Conditions

ϕ=1/fosc(fosc=0.6~6.6MHz), C_L=50pF, V_{OLC}=0.2V_{CC}, V_{OHC}=0.8V_{CC}

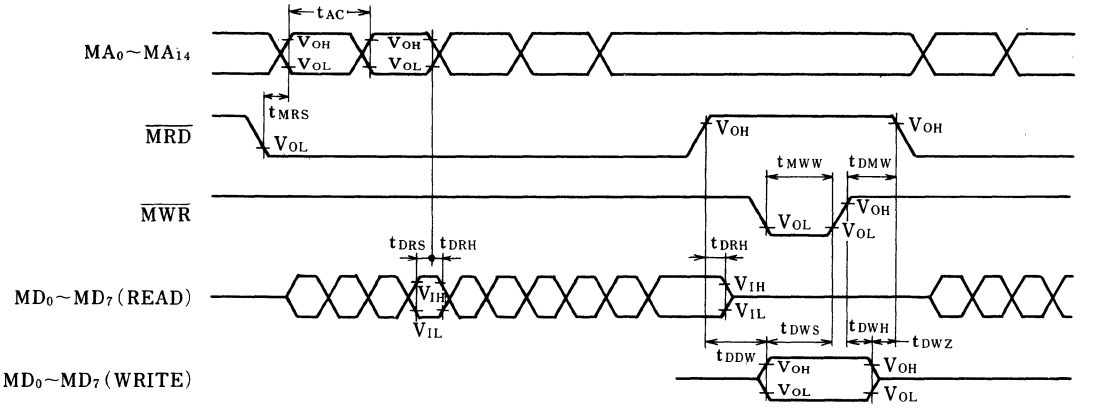


(2) RAM interface timing

(V_{CC} = 5V ± 10%, Ta = −10 ~ +70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address output cycle time	t_{AC}	$2\phi-50$	2ϕ	$2\phi+50$	ns
$\overline{MRD}$ setup time (to address)	t_{MRS}	0	30	100	ns
Read data setup time	t_{DRS}	180			ns
Read data hold time	t_{DRH}			15	ns
Memory write pulse width	t_{MWW}	$\phi-50$	ϕ		ns
Write recovery time	t_{DMW}	$2\phi-150$	2ϕ		ns
Write data output delay time (to $\overline{MRD}$ ↑)	t_{DDW}	$\phi-100$	ϕ		ns
Write data setup time	t_{DWS}	$\phi-100$	ϕ		ns
Write data hold time	t_{DWH}	$\phi-100$	ϕ		ns
$\overline{MRD}$ time from write data (Hz)	t_{DWZ}	$\phi-100$	ϕ		ns

Measurement Conditions
ϕ = 1/fosc(fosc = 0.6 ~ 6.6MHz), C_L = 20pF, V_{OL} = 0.8V, V_{OH} = 2.0V, V_{IL} = 0.8V, V_{IH} = 2.0V, and t_r and t_f of input signal are less than 50 ns.

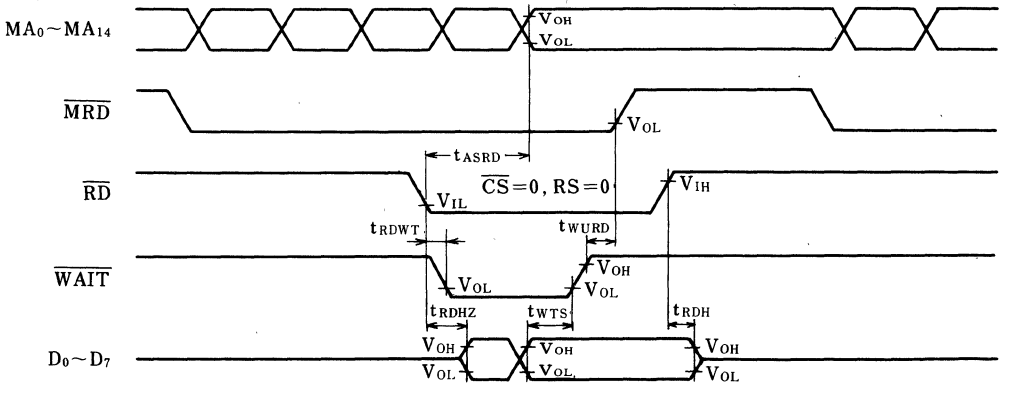


(3) CPU interface (read cycle) timing

(V_{CC} = 5V ± 10%, Ta = −10 ~ +70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
$\overline{WAIT}$ output time referring to $\overline{RD}$	t_{RDWT}		45	150	ns
$\overline{WAIT}$ rise time referring to $\overline{MRD}$	t_{WURD}	$\phi-100$	ϕ		ns
Data output delay time referring to $\overline{RD}$	t_{RDHZ}		25	150	ns
Data output settling time referring to $\overline{WAIT}$ ↑	t_{WTS}	$2\phi-150$	2ϕ		ns
Data output hold time referring to $\overline{RD}$	t_{RDH}	0	20		ns
$\overline{RD}$ setup time referring to MA	t_{ASRD}	200			ns

Measurement Conditions
ϕ = 1/fosc(fosc = 0.6 ~ 6.6MHz), C_L = 20pF, V_{OL} = 0.8V, V_{OH} = 2.0V, V_{IL} = 0.8V, V_{IH} = 2.0V, and t_r and t_f of input signal are less than 50 ns.

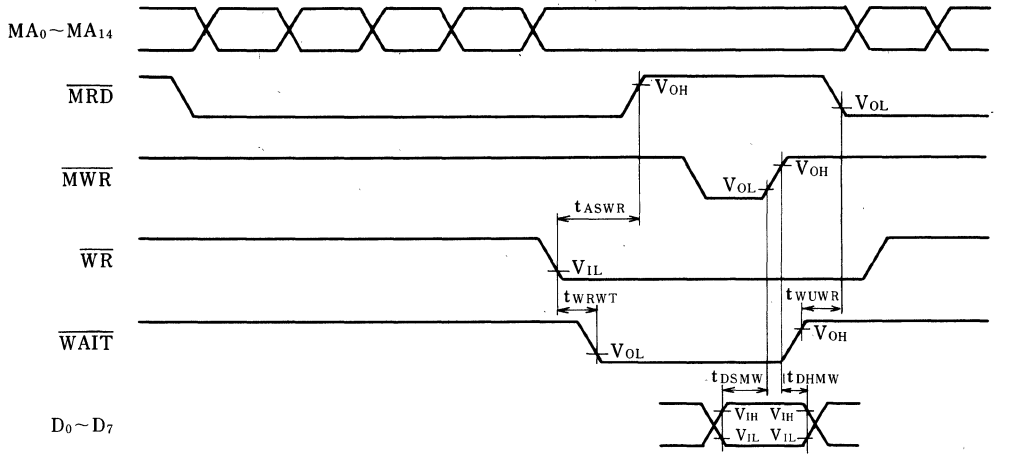


(4) CPU interface (read cycle) timing

(V_{CC} = 5V ± 10%, Ta = −10 ~ +70℃)

Paramerter	Symbol	MIN.	TYP.	MAX.	Unit
$\overline{WAIT}$ rise time referring to $\overline{MRD}$	t_{WUWR}	ϕ −100	ϕ		ns
Data setup time referring to $\overline{MWR}$	t_{DSMW}	ϕ −50	ϕ		ns
Data hold time referring to $\overline{MWR}$	t_{DHMW}	ϕ −50	ϕ		ns
$\overline{WR}$ setup time referring to $\overline{MRD}$	t_{ASWR}	200			ns
$\overline{WAIT}$ output time referring to $\overline{WR}$	t_{WRWT}		45	150	ns

Measurement Conditions
$\phi = 1/fosc(fosc = 0.6 \sim 6.6MHz)$, $C_L = 20pF$, $V_{OL} = 0.8V$, $V_{OH} = 2.0V$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, and t_r and t_f of input signal are less than 50 ns.



■ Functional Descriptions

(1) Power supply

The V_{CC} pin requires +5 VDC to the ground. The GND pin should be externally grounded.

(2) Clock pulse and divider

The OSC_{IN} pin of the device requires constant application of a clock. A clock used for the CPU may be used for this purpose. The OSC_{OUT} pin, which provides an inverse of the clock applied to the OSC_{IN} pin, should be left open.

(3) RES pin and reset pulse

The RES pin requires application of a reset pulse when power is turned ON to initialize the LR3691A's internal registers. The reset pulse should be active high, and should have a pulse width more than 4 time as long as that of the clock pulse.

The input circuit for the RES pin uses a floating gate.

(4) Data control pins

The LR3691A is controlled from the host CPU through pins CS, RD, WR, and RS, The signals applied to pins RD, WR, and RS are made valid if the $\overline{CS}$ pin is set to low.

The RD and WR pins are used to determine the direction of data transfer between the display RAM and CPU.

The RS pin specifies the type of data exchanged with the CPU through pins D_0-D_7, identifying display RAM address specification data and display data.

The data control pin signal timing is shown in the paragraph for Electrical Characteristics.

The input circuit for these control pins have floating gates.

(5) WAIT signal

The display RAM is accessed from both the CPU and the LCD driver. To avoid contention, the LR3691A delivers a WAIT signal to its WAIT pin when the LCD driver is accessing the display RAM, suspending display RAM access from the CPU.

(6) Data input/output

The LR3691A exchanges data with its host CPU through its pins D_0-D_7. The data transferred through these pins are display RAM address data, display RAM read data, and display RAM write data. The data type is specified by controlling a data control pin. The D_0-D_7 pins are normally connected to the host CPU's data bus. When in the input mode, the D_0-D_7 pins are pulled up through pull-up resistors.

(7) Screen division and dot number selection

The LR3691A controls an LCD screen through LCD drivers using serial data transfer scheme with duty cycle of 1/32 to 1/128. The LCD screen is often divided into sections to improve contrast and reduce driving frequency and driving voltage.

The LR3691A permits division of the LCD screen into two sections both in the horizontal and vertical directions. The ROW and CLM pins have floating gate inputs with high impedance.

(8) Connection to display RAM

The LR3691A should be connected to the display RAM as follows: The address data for display RAM is output through pins MA_0-MA_{14}. If the display RAM consists of more than one chip, the address data shoud be decoded through an address decoder before being coupled to the display RAM.

Display data is transferred through pins MD_0-MD_7. The MRD and MWR pins are used to control the display RAM: the MAD pin provides a display RAM read command signal; the MWR pin provides a display RAM write command signal.

(9) Display screen versus display RAM

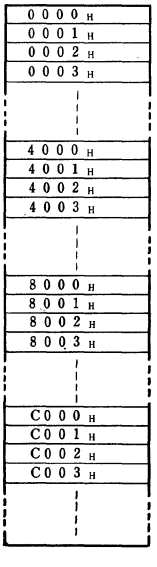
The display RAM is accessed from the CPU or LCD driver via the LR3691A. Access from the LCD driver occurs every 32 cycles of the system clock (applied to the OSC_{IN} pin), of which one 16 cycle period is occupied by the LCD driver, and the remaining 16 cycle period is available to the CPU. Display data is written and read byte-by-byte (8 bits). When viewed from the CPU, display RAM address alllocations to the display screen address are fixed. (To facilitate data read/write access to the display RAM and to impove availability of the RAM area, RAM addresses are actually translated within the LR3691A before read /write access is performed.) The first addresses of the four sections on the screen are fixed to 0000H, 4000H, 8000H, and C000H. An example of the relationship between display RAM addresses and screen addresses as viewed from the CPU is shown in Fig. 1, where the number of pixels per row on the screen is 640 (numbers given in parentheses are that of 240).

(10) LCD driver control

The LR3691A drives an LCD dot matrix display panel via LCD drivers using serial data transfer scheme. It uses its pins S, M, CP_1 CP_2, and DI_1 -DI_4 for controlling the LCD driver.

The S pin provides data signal to the shift register input of the LCD driver which drives the common electrodes. The M pin supplies a signal needed for synchronized AC driving of the LCD driver.

The CP_2 pin drlivers a clock signal used to shift display data. The CP_1 pin provides a display data latch signal. The pins DI_1 -DI_4 otuput display data after converting the 8-bit parallel data from the display RAM into serial data.



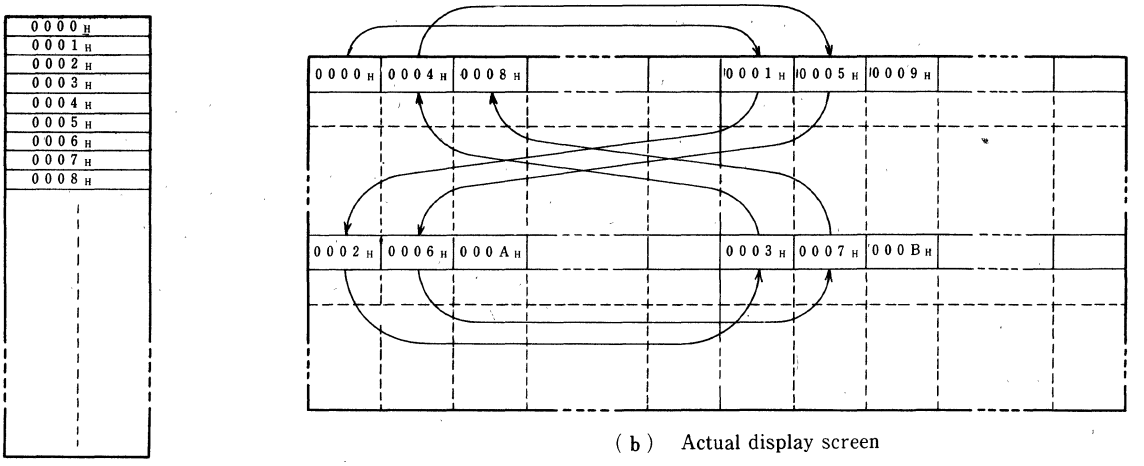
(a) Memory map viewed from CPU

0000H (0000H)	0001H (0001H)	0002H (0002H)	-------	0027H (000EH)	4000H (4000H)	4001H (4001H)	4002H (4002H)	-------	4027H (400EH)
0028H (000FH)	0029H (0010H)	002AH (0011H)			4028H (400FH)	4029H (4010H)	402AH (4011H)		
8000H (8000H)	8001H (8001H)	8002H (8002H)	-------	8027H (800EH)	C000H (C000H)	C001H (C001H)	C002H (C002H)	-------	C027H (C00EH)
8028H (800FH)	8029H (8010H)	802AH (8011H)			C028H (C00FH)	C029H (C010H)	C02AH (C011H)		

(Note) Number of pixels per row is 640. (numbers given in ( ) are that of 240)

(b) Display viewed from CPU

Fig. 1 Relationship between display RAM map and display screen as accessed from the CPU



(a) Actual memory map

(b) Actual display screen

Fig. 2 Actual relationship beween display RAM map and display screen

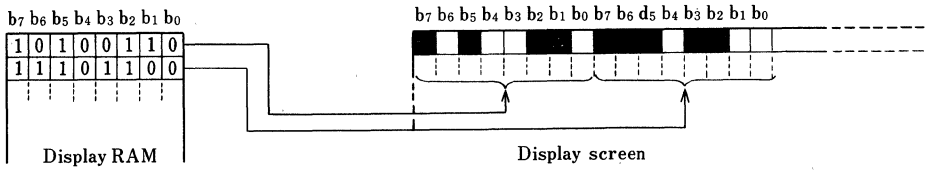


Fig. 3 Bit-by-bit relationship of display screen and display RAM

The DI_1 pin provides display data for the upper left section of the display screen; the DI_2 pin provides that for the upper right section of the screen; the DI_3 pin provides that for the lower left section; and the DI_4 pin provides that for the lower right section.

The LCD driver control singnal timing is shown in the paragraph describing Electrical Characteristics.

(11) Display enable

The DE pin is used to enable or disable display to the screen. If set at low, the entire screen is blanked. Data display is enabled only when the DE pin is set at high. The DE pin is used to suppress meaningless information from the screen power is being turned on. It has a floating gate input.

(12) T_1 and T_2 pins

The T_1 and T_2 pins should be connected to the ground. These pins, having floating gate inputs, are used for device test and are not available to the user.

■ Display Control Method

Display control consists of display data processing, RAM addressing, and display screen selection.

(1) Display screen selection

The LR3961A drives the display screen via shift-register type LCD drivers by, if necessary, dividing the screen into four sections according to the number of pixels (on the row and column) to be displayed. The number of pixels per row is specified with the CLM_0-CLM_2 pins. The number of pixels per column (duty) is specified with the ROW_0 and ROW_1 pins. See the following table.

CLM (2,1,0)	No. of pixels per row
000	120
001	160
010	240
011	320
100	480
101	640
110	unused
111	unused

ROW (1,0)	No. of pixels per column
00	32
01	64
10	100
11	128

If the screen is divided into two half sections (left and right), the displayable number of pixels becomes twice the numbers shown in the above left table. If the screen is divided into upper and lower halves, the displayable number of pixels becomes twice the numbers shown in the below-right table on page 850.

To prevent flicker of the display image, the total number of pixels per section should be limited to 40,960 of total pixels/divided screens.

(2) Display RAM address control

The addresses for the display RAM are apparently specified with 15-bit address data, whose output is implemented through pins MA_0-MA_{14}. Meanwhile, the host CPU uses an 8-bit bus, D_0-D_7, to address the display RAM. To specify a full 15-bit address, the CPU must transfer address data in two consecutive sequences: first the lower byte, and next the upper byte. At this time the RS pin (address specification) should be set to '1'. Once a display RAM address is specified, it is automatically incremented each time the CPU accesses it for read or write operation. So for display RAM addresses which are consecutive can be accessed by setting only the first address.

CS	RD	WR	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	Address data							

Address data is transferred in two consecutive sequences for upper and lower bytes.

(3) Data write into display RAM

Data can be written into the specified display RAM location. Specification is conducted by the RAM address counter through the D_0-D_7 pins when the RS is set at zero.

CS	RD	WR	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	Display data							

Once data is written, the RAM address counter is automatically incremented, so that data may be written consecutively.

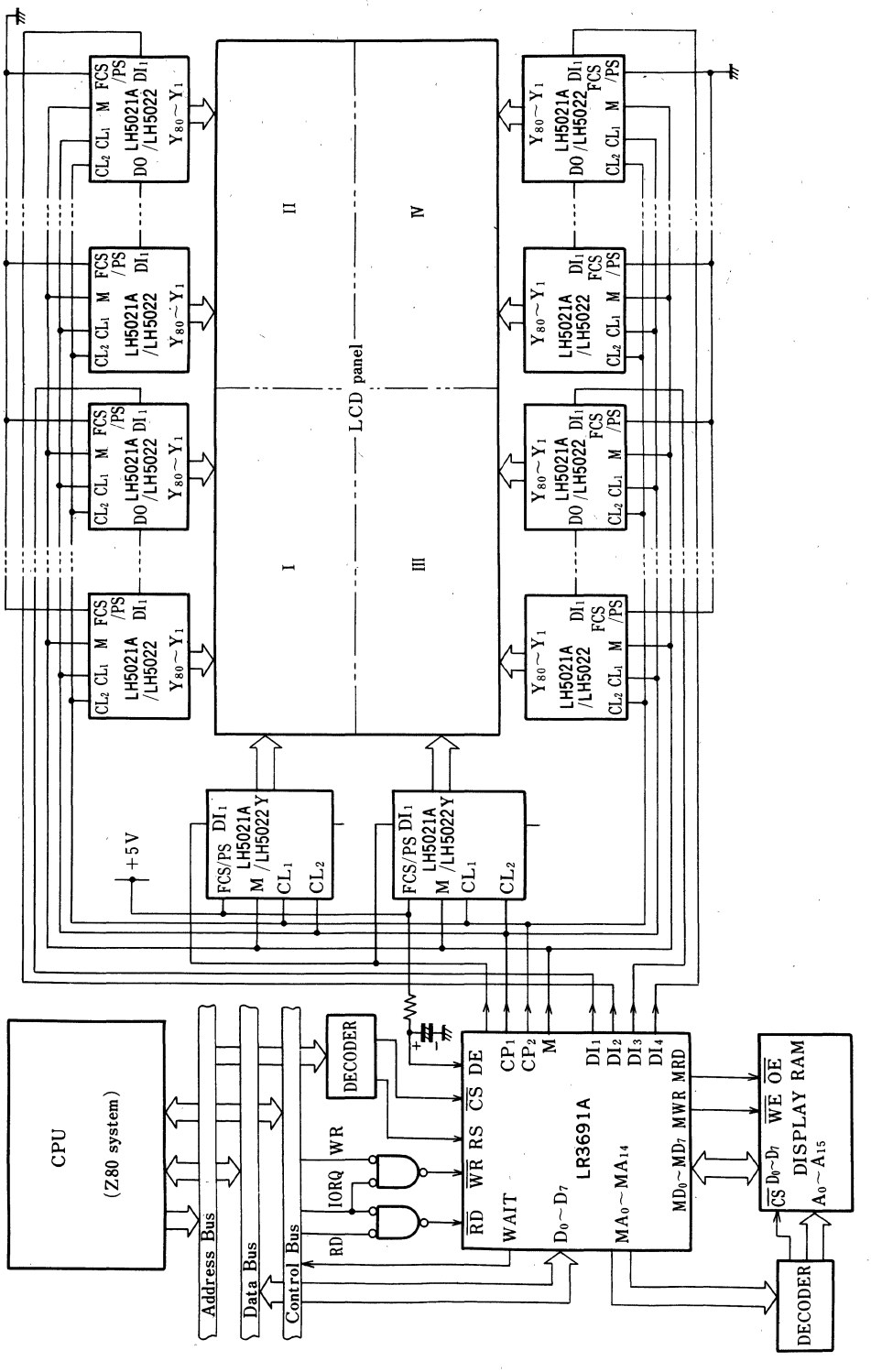
(4) Data read from display RAM

Data can be read out of the display RAM location specified by the RAM address counter. Specification is implemented through the D_0-D_7 pins when the RS is set at zero.

CS	RD	WR	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	Display data							

Once data is read, the RAM address counter is automatically incremented.

■ System Configuration



LR3692 LCD Dot Matrix Controller CMOS LSI

■ Description

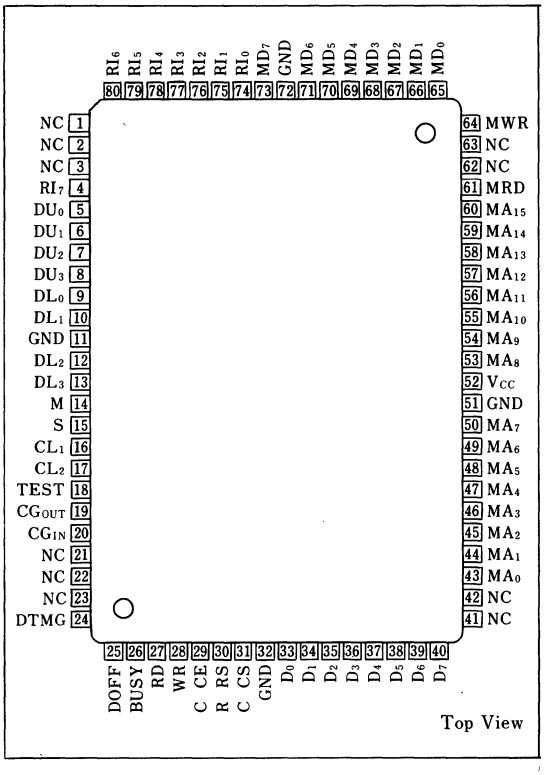
The LR3692 is a controller LSI for dot matrix graphic LCD unit. It stores display data transferred from 8-bit microcomputer in the external RAM and generates LCD drive signal suitable as serial type LCD driver.

Selectable from graphic mode and character mode using character ROM for character display.

■ Features

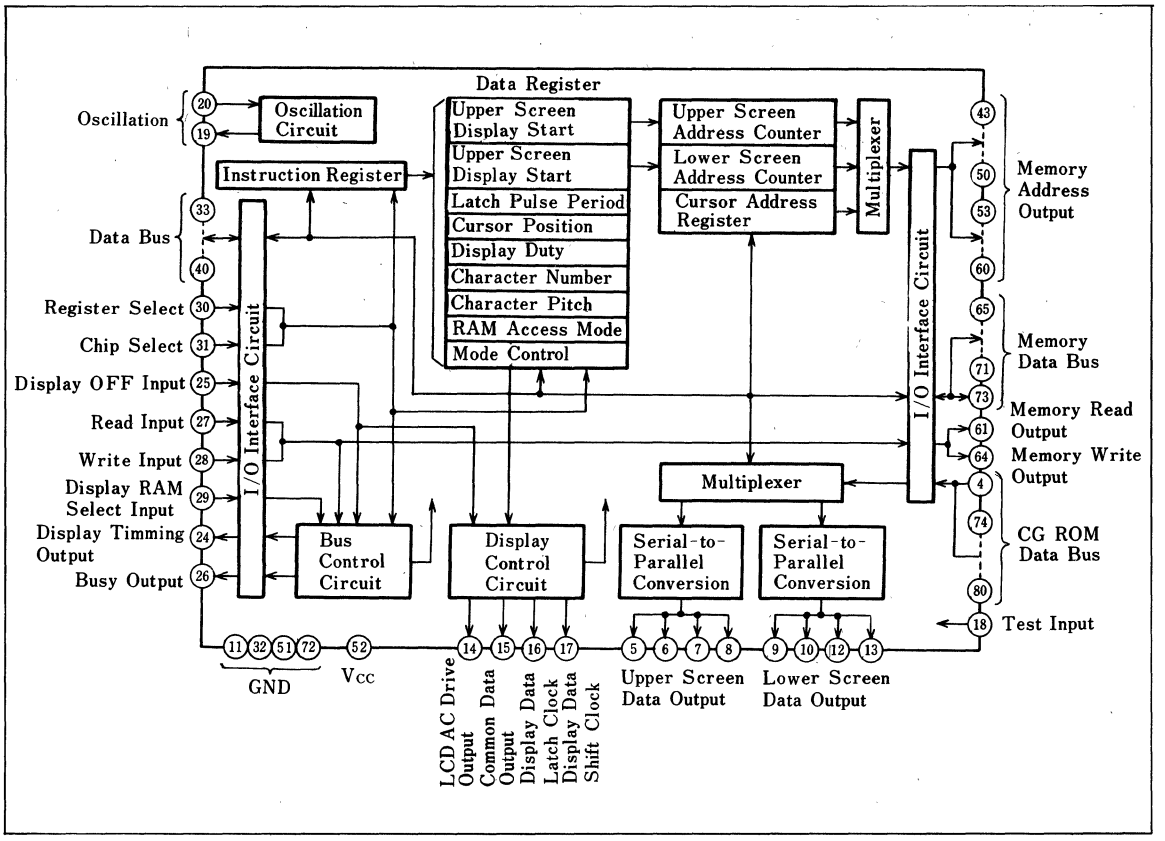
1. Graphic or character mode selectable
2. Display duty : 1/32 ~ 1/256
3. Maximum display capability
   Graphic mode : 640 × 256 dots
   Character mode : 80 × 32 characters
   (if character font is 8 × 8)
4. Capable of interfacing to an 8-bit CPU
5. Serial/ 4-bit parallel output
6. Capable of driving upper and lower divisions LCD
7. Scroll function
8. Cursor display : ON, OFF, and BLINK
9. Character BLINK
10. Display ON, OFF
11. On-chip crystal oscillator
12. Single power supply : 5V (TYP.)
13. CMOS process
14. 80-pin quad-flat package

■ Pin Connections



Top View

■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3～+7	V	1
Input voltage	V_{IN}	−0.3~V_{DD}+0.3	V	1
Operating temperature	T_{opr}	0～+50	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	4.75		5.25	V

■ DC Characteristics

(V_{DD}=5V±5%, Ta=0～+50℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{ILT}		0		0.4	V	1
Input high voltage	V_{IHT}		2.4		V_{DD}	V	1
Input low voltage	V_{ILC}		0		0.2V_{DD}	V	2
Input high voltage	V_{IHC}		0.8V_{DD}		V_{DD}	V	2
Output low voltage	V_{OLT}	I_{OL}=2.0mA			0.4	V	3
Output high voltage	V_{OHT}	I_{OH}=1.0mA	2.4			V	3
Output low voltage	V_{OLC}	I_{OL}=0.6mA			0.4	V	4
Output high voltage	V_{OHC}	I_{OH}=0.6mA	V_{DD}−0.4			V	4
Pull-up current	I_{LI}	V_{IN}=0V		10		μA	5
Supply current	I_{DD}	fosc = 4MHz					
Oscillator frequency	fosc	With crystal oscillator		4		MHz	6
Ext. clock frequency	f_{CL}		0.2		4	MHz	6
Ext. clock duty	Duty		47.5	50	52.5	%	6
Rise time	t_{RCL}				50	ns	6
Fall time	t_{FCL}				50	ns	6

Note 1: Applied to pins $\overline{MD_0}$-MD_7, RI_0-RI_7, D_0-D_7, $\overline{CS}$, RS, $\overline{CE}$, $\overline{WR}$, $\overline{RD}$, and $\overline{DOFF}$.
Note 2: Applied to pins $\overline{TEST}$ and CG_{IN}.
Note 3: Applied to pins MA_0-MA_{15}, MD_0-MD_7, $\overline{MWR}$, $\overline{MRD}$, D_0-D_7, $\overline{BUSY}$, and DTMG.
Note 4: Applied to pins CL_1, CL_2, S, DU_0-OU_3, DL_0-DL_3, and M.
Note 5: Applied to pins TEST, MA_0-MA_{15}, MD_0-MD_7, RI_0-RI_7, D_0-D_7, $\overline{CS}$, RS, $\overline{CE}$, $\overline{WR}$, $\overline{RD}$, and $\overline{DOFF}$.
Note 6: Applied to pins CG_{IN} and CG_{OUT}.

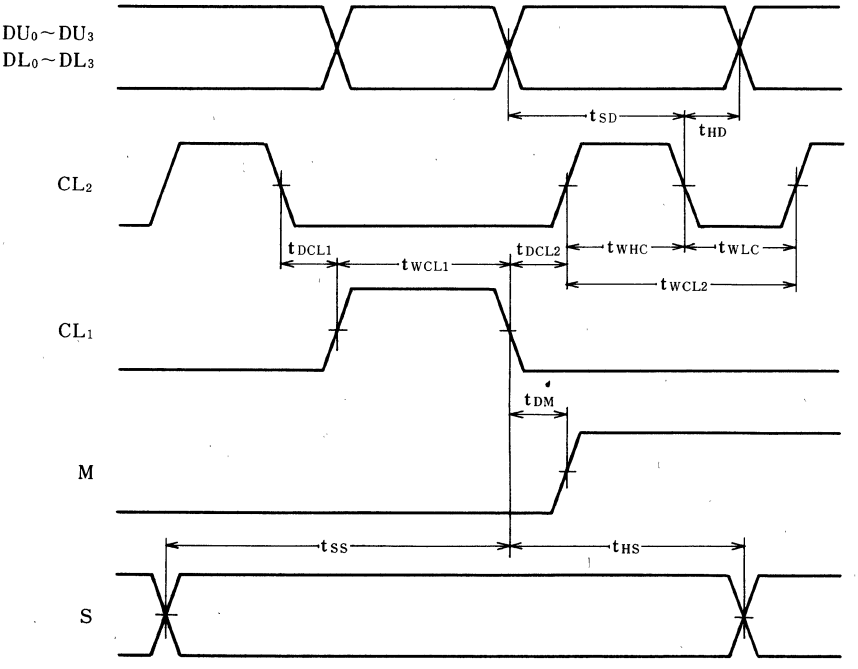
10

■ AC Characteristics

(1) LCD control signal

(V_{CC}=5V±5%, fosc=4MHz, C_L=15pF, Ta=0~+50℃)

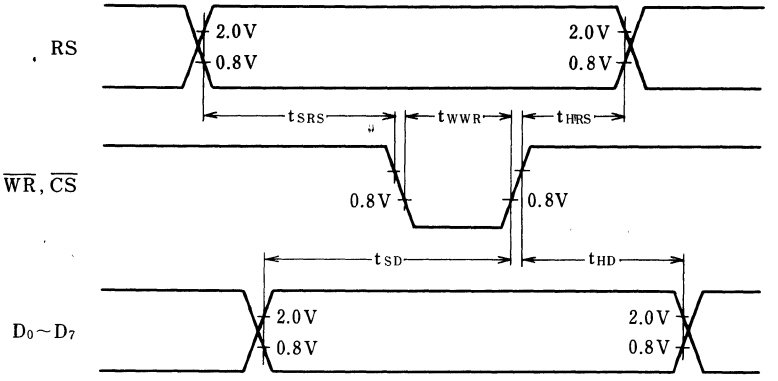
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data setup time	t_{SD}		100	375		ns
Data hold time	t_{HD}		50	125		ns
Clock pulse low width	t_{WLC}		150	250		ns
Clock pulse high width	t_{WHC}		150	250		ns
Clock cycle time	t_{WCL2}			500		ns
Clock delay time	t_{DCL1}		0	125		ns
Clock pulse width	t_{WCL1}		2	4		μs
Clock delay time	t_{DCL2}		0	135		ns
Data delay time	t_{DM}				500	ns
Data hold time	t_{HS}		2			μs
Data setup time	t_{SS}		2			μs
Signal rise time	t_r	$0.1V_{DD}$~$0.9V_{DD}$			50	ns
Signal fall time	t_f	$0.1V_{DD}$~$0.9V_{DD}$			50	ns



(2) Writing display control command

(V_{DD}=5V±5%, Ta=0～+50℃)

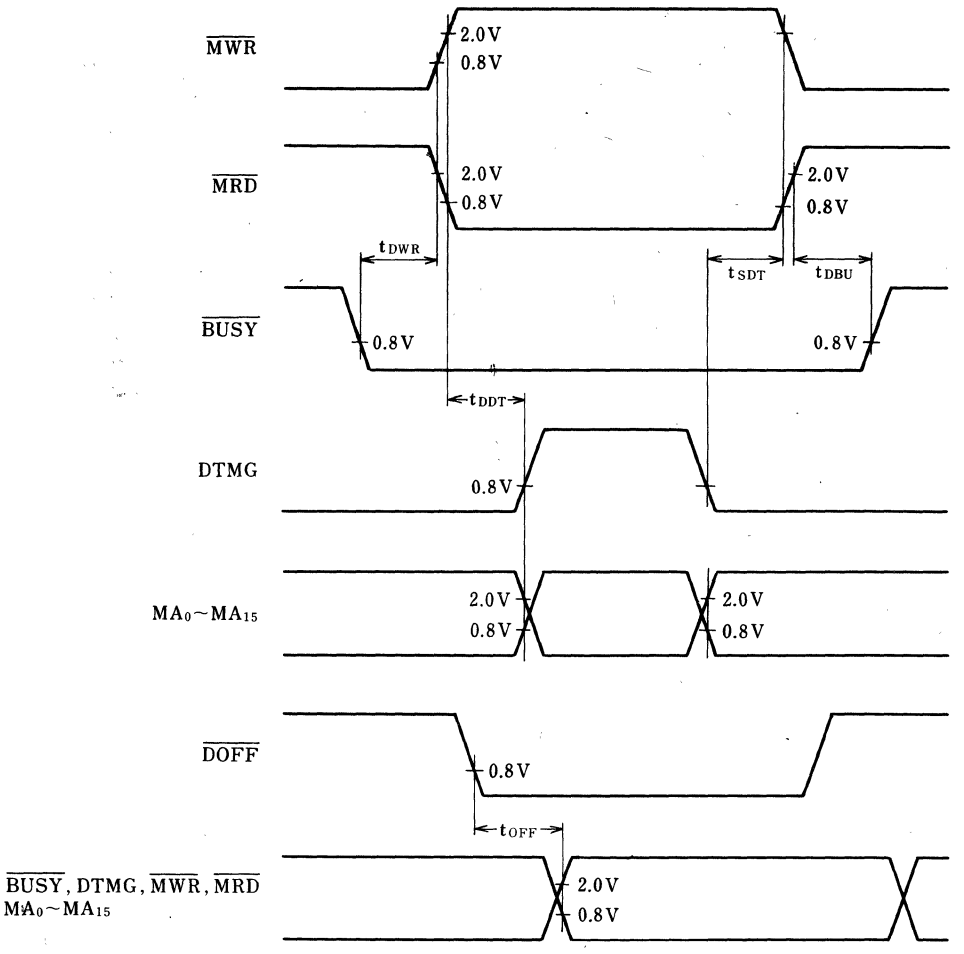
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Signal setup time	t_{SRS}		500			ns
Signal pulse width	t_{WWR}	$\overline{WR}$ and $\overline{CS}$ overlap time	220			ns
Signal hold time	t_{HRS}		30			ns
Data setup time	t_{SD}		250			ns
Data hold time	t_{HD}		30			ns



(3) Control signal timing

(V_{DD}=5V±5%, fosc=4MHz, C_L=15pF Ta=0～+50℃)

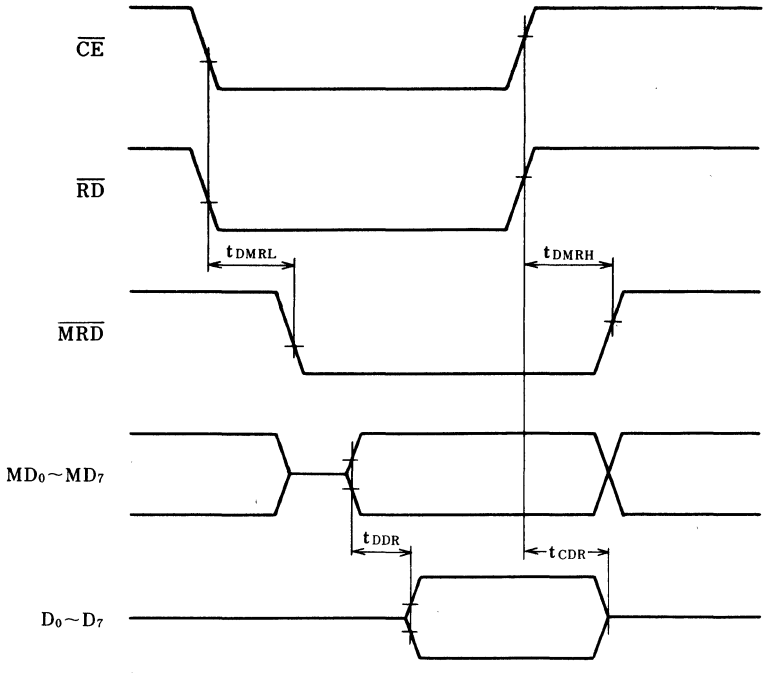
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Signal delay time	t_{DWR}		0.2	1		μs
Signal delay time	t_{DDT}		0.2	1		μs
Signal setup time	t_{SDT}		0.2	1		μs
Signal delay time	t_{DBU}		0.2	1		μs
Signal delay time	t_{OFF}				200	ns

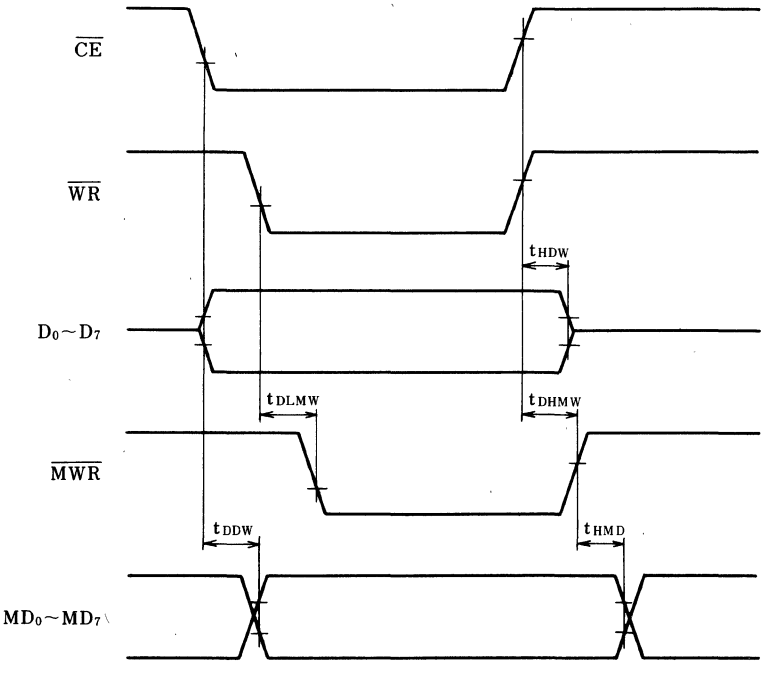


(4) Bus timing (Direct mode)

(V_{DD}=5V±5%, fosc=4MHz, C_L=15pF, Ta=0~+50℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{MOR}$ delay time	t_{DMRL}				150	ns
	t_{DMRH}				150	
Data delay time	t_{DDR}				150	ns
Bus switching time	t_{CDR}		0			ns
$\overline{MWR}$ delay time	t_{DLMW}				150	ns
	t_{DHMW}				150	ns
Data delay time	t_{DDW}				150	ns
Data hold time	t_{HDW}		50			ns
Data hold time	t_{HMD}		0			ns

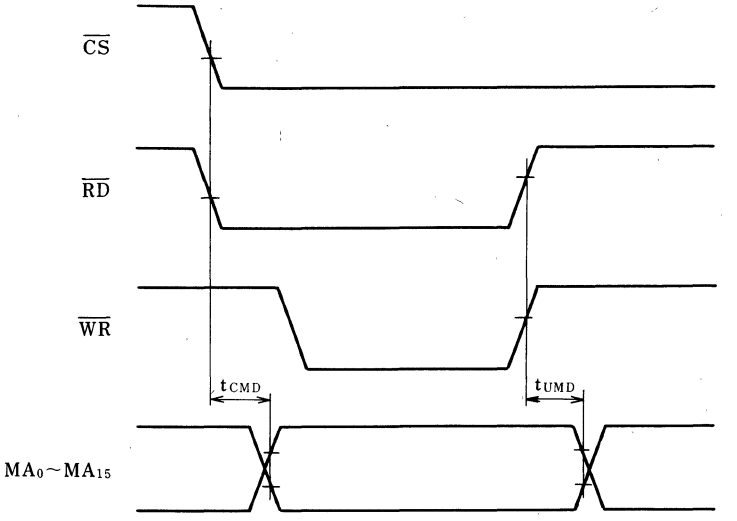

CE
RD
tDMRL
tDMRH
MRD
MD0~MD7
tDDR
tCDR
D0~D7


CE
WR
tHDW
D0~D7
tDLMW
tDHMW
MWR
tDDW
tHMD
MD0~MD7

(5) Bus timing (I/O mode)

(V_{DD}=5V±5%, fosc=4MHz, C_L=15pF, Ta=0~+50℃)

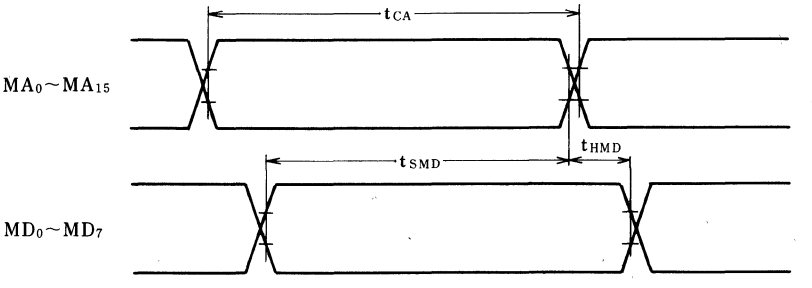
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address delay time	t_{CMD}				150	ns
Address hold time	t_{UMD}				1	μs



(6) Display RAM access (display busy in 4-bit mode)

(V_{DD}=5V±5%, fosc=4MHz, C_L=15pF, Ta=0~+50℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data setup time	t_{SMD}		200			ns
Data hold time	t_{HMD}		0			ns
Access cycle time	t_{CA}			500		ns



■ Display Control Commands

Display control is accomplished by writing commands and data into the command and data registers.

(1) Mode control

When writing data into the data register, write code 00H into the command register to specify the Write Mode Control register.

Register name: Mode Control register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	0
0	0	0	0	MODE DATA				

Data contents

D4	1: 4-bit parallel output 0: 1-bit serial output
D3	1: Character mode 0: Graphic mode
D2	1: Display ON 0: Display OFF
D1	1: Cursor blink (character blink when cursor is off.)
D0	1: Cursor ON 0: Cursor OFF

(2) Setting character pitch

Register name: Character Pitch register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	1
0	(VP-1)				0	0	(HP)	

VP: Vertical pitch in character mode. Invalid for Graphic mode.
HP: Horizontal pitch in character mode. Invalid for Graphic mode.

The HP can take on any of the following three values. However, when in the 4-bit parallel output mode, the horizontal character pitch is fixed at 8.

HP	D1	D0	
5	0	1	Horizontal character pitch 5
6	1	0	Horizontal character pitch 6
8	0	0	Horizontal character pitch 8

(3) Setting the number of characters per row

Register name: Characters Per Row register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1	0
0	0	(HN-1)						

HN: Specifies the number of characters per row when in the character mode, and the number of bytes per row when in the Graphic mode. When in the 4-bit parallel output mode, HN should be set to a multiple of four (4).

Nunmber of pixels per row NX:

NX=HP x HN in Character mode

NX=8 x HN in Graphic mode

(4) Setting display duty

Register name: Display register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1	1
0	(NY-1)							

NY: Display duty —— 1/(32-256)

(5) Setting cursor position

Register name: Cursor Position register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0	0
0	0	0	0	0	(CP-1)			

CP: Specifies the row on which the cursor is located in Character mode. The horizontal length of the cursor is identical to the HP.

(6) Setting lower byte of display start address (upper screen)

Register name: Display Start Address register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	0	0
0	Lower byte of start address							

(7) Setting upper byte of display start address (upper screen)

Register name: Display Start Address register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	0	1
0	Upper byte of start address							

This command sets the display start address for the upper section of the screen. The display start address refers to the RAM location in which the data to be displayed in the upper left corner of the screen is stored.

(8) Setting lower byte of display start address (lower screen)

Register name: Display Start Address register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0	1
0	Lower byte of start address							

(9) Setting upper byte of display start address (lower screen)

Register name: Display Start Address register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1	0
0	Upper byte of start address							

This command sets the display start address for the lower section of the screen. The display start address refers to the RAM location in which the data to be displayed in the upper left corner of the lower section of the screen is stored.

10

(10) Setting lower byte of cursor address

Register name: Cursor Address register

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	1	0	1	0
0	Lower byte of cursor address							

(11) Setting upper byte of cursor address

Register name: Cursor Address register

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	1	0	1	1
0	Upper byte of cursor address							

This command sets cursor address data into the cursor address counter.

(12) Setting latch pulse period

Regipter name: Latch Pulse Period register

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	1	1
0	0	(NLP−1)						

NLP: $HN + 1 \leqq NLP \leqq 128$ when in serial mode.
$HN/4 + 1 \leqq NLP \leqq 128$ when in 4-bit mode.
The display frequency f_d is related with the latch pulse period NLP by the following formula:
$f_d = 1/(8NLP.\ TXS.\ NY)$
TXS: Shift clock period
TXS = 500 ns when OSC frequency is 4 MHz.

(13) Setting display RAM access mode

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	1	1	0	0
0	DATA							

I/O mode is selected by writing OCH into the command register. When BUSY = 1, the display RAM location specified by the Cursor Address register can be accessed through DI_0-DI_7 for read or write operations.

The LR3692 also permits direct display RAM access using the address data furnished from the CPU. In either case the value of the Cursor Address register is incremented each time the display RAM is accessed.

■ System Configuration

(1) Interface with CPU

As shown in Figs. 1 and 2, the LR3692 (LCDC) is connected to the standard bus of the Z80-type CPU, using it as a means of transferring data and commands.

If the $\overline{CS}$ is at low and RS is at high, the command register within the LCDC is specified and the data on the data bus is written in. The write timing is determined by the $\overline{WR}$ signal. If the $\overline{CS}$ is at low and RS is at high, the contents of the LCDC's internal register requested by the command register cannot be read.

The $\overline{CE}$, $\overline{BUSY}$, $\overline{DOFF}$, and DTMG signals are used for CPU access to the display RAM.

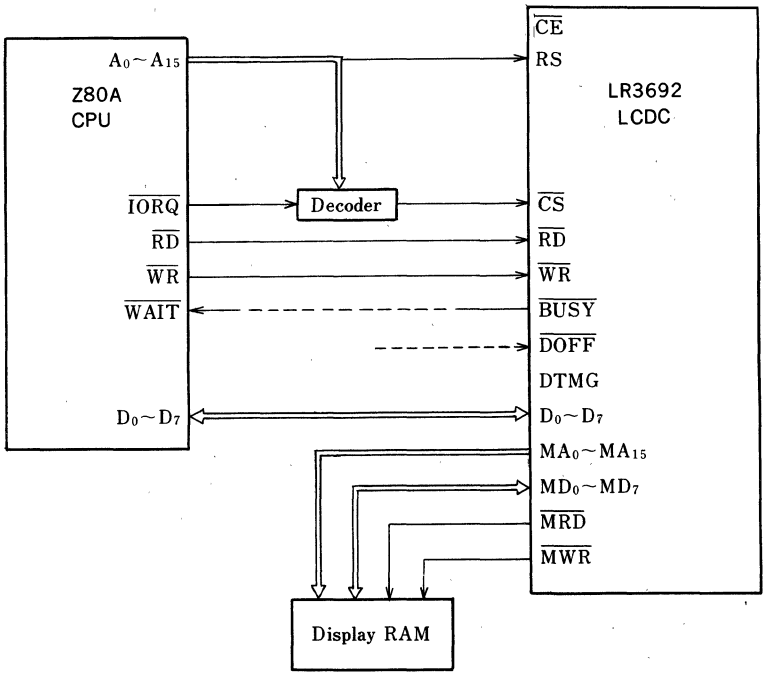


Fig. 1 Interface with CPU(I/O mode)

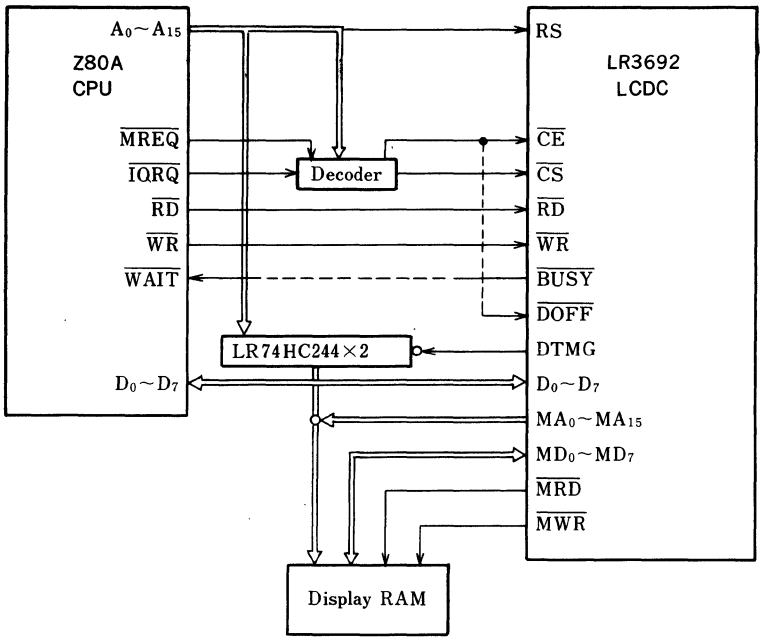


Fig. 2 Interface with CPU (Direct mode)

(2) CPU access to display RAM

CPU access to the display RAM includes the I/O mode which is made through the LCDC, and the Direct mode which is directly performed from the CPU.

① I/O mode A sample system configuration for I/O mode access is shown in Fig. 1. A value for $0C_H$ is first set into the command register. If the $\overline{BUSY}$ is high, $\overline{CS}$ is low, and RS is low, the $\overline{RD}$, $\overline{WR}$, and D_0-D_7 lines are linked to the $\overline{MRD}$, $\overline{MWR}$, and MD_0-MD_7 lines, respectively. At this time the value of the Cursor Address register is output at the MA_0-MA_{15} pins. The Cursor Address register is incremented at the rising edge of the $\overline{RD}$ or $\overline{WR}$ signal. The $\overline{BUSY}$ line is set to high during the fly-back period in which the LCDC does not access the display RAM. Setting the $\overline{DOFF}$ to low causes the $\overline{BUSY}$ to be set to high, making the display RAM accessible at any timing. At this time, the LCD display is turned off.

② Direct mode A sample system configuration for Direct mode access is shown in Fig. 2. The Direct mode is selected if the value of the command register is anything but $0C_H$. If $\overline{BUSY}$ is high and $\overline{CE}$ is low, the $\overline{RD}$, $\overline{WR}$ and D_0-D_7 pins are linked to the $\overline{MRD}$, $\overline{MWR}$, and MD_0-MD_7 lines, respectively. At this time the DTMG is set at low and the MA_0-MA_{15} pins are set to high impedance, to transfer the address specified of the CPU directly to the display RAM. The Cursor Address register is incremented at the rising edge of the $\overline{RD}$ or $\overline{WR}$ signal. The functions of the $\overline{BUSY}$ and $\overline{DOFF}$ signals are identical to those in the I/O mode.

Note: In either mode the $\overline{BUSY}$ signal is output only when the CPU is accessing the display RAM. (When $\overline{CE}$ = 0 in Direct mode; when $\overline{CS}$=0, RS=0 and the command register value is $0C_H$ in I/O mode.) The $\overline{BUSY}$ is set to high in all other cases.

■ LCD Control

(1) Graphic mode

The Graphic mode is selected by the Mode Control register value. In this mode each bit of the display RAM corresponds to each pixel on the LCD screen.

① Screen configuration The numbers of pixels per row and per column are determined by the values of the Character-Per-Row register and Duty register.

No. of pixels per row: HN×8, HN=16 to 128

No. of pixels per column: NY×2, NY=32 to 256

(When both the upper and lower sections of the screen are used.)

② Display start address The display start address refers to the first location of the display RAM area to displayed, specified by 16-bit data. Independent specification for the upper and lower sections of the screen is possible. Further, the utilization of display start address makes page con-

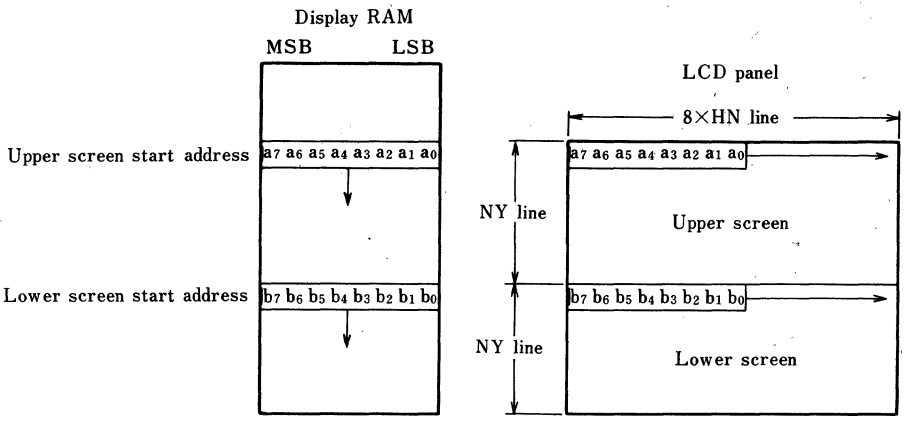


Fig. 3 Screen configuration (Graphic mode)

trol and screen scroll possible.

(2) Character mode

The Character mode is specified by the value of the Mode Control register. In this mode pixel patterns are displayed by combining character codes of the display RAM with the corresponding character patterns of the character generator ROM (CGROM).

① Screen configuration The numbers of characters per row and per column are determined by the content of the Character-Per Row register, Duty register, and Character Pitch register.

No. of characters per row: HN=16 to 128
No. of characters per column: NY×2/VVP, NY=32×256
(When the upper and lower sections of the screen are used.)

The numbers of pixels per row and per column are determined as follows:

No. of pixels per row: HHY×2

② Character font The character font is specified by the value of the Character Pitch register.

Horizontal pitch: HP=5, 6, 8
Vertical pitch: VP=1~16

Fig. 4 shows an example of character font. If HP=5 or 6, the LSB side of the RI_0-RI_7 is invalid.

③ Cursor display The cursor display mode is determined by the value of the Mode Control register. The cursor position is specified by the value of Cursor Address register. Since the character code address on the display RAM is specified for cursor position specification, screen scrolling is accompained by cursor scrolling.,

The cursor position in a character font is specified by the Cursor Position register.

④ Cursor blink Cursor or character blinking is controlled by the Mode Controll register.

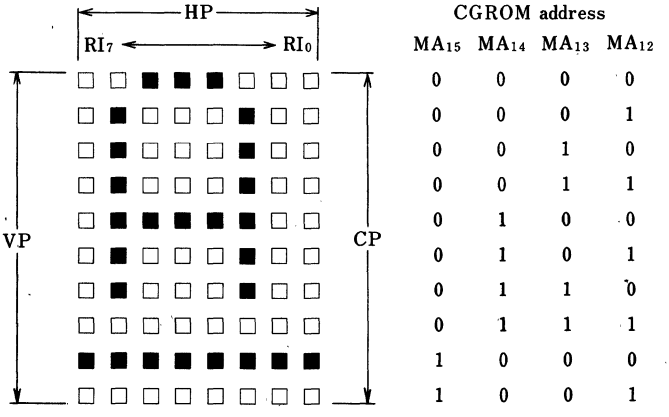


Fig. 4 Example of character font (HP=8, VP=10, CP=9)

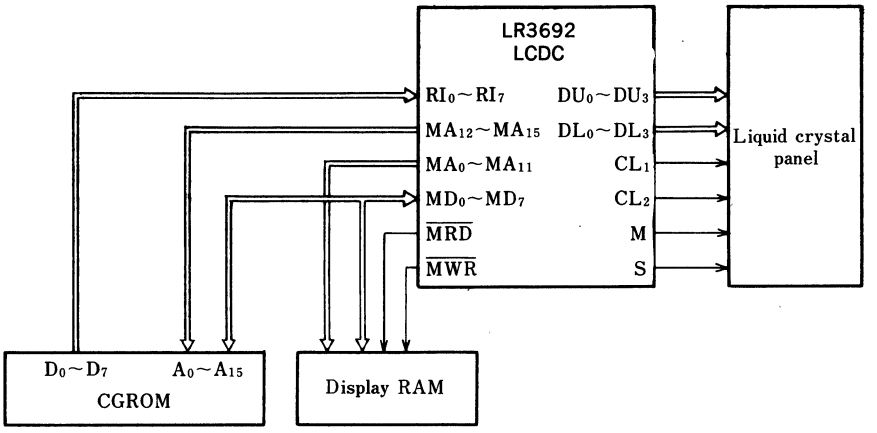


Fig. 5 Connections to CGROM and LCD panel

Blinking is performed for approx. 1H (64 frams) at 1/2 duty.

(3) Parameter setting

① Display frequency The LR3692 uses the two-frame AC display system. The display system. The display frequency is determined by Display Duty and the value of the Latch Pulse Period register.

One frame period: $T_d = 8NLP.TXS.NY$

Display frequency: $f_d = 1/T_d$

(TXS=500 ns when OSC frequency is 4 MHz.)

② Flyback period The LCDC does not access the display RAM during flyback period.

Flyback period TDIS:

When in Serial mode: TDIS= {8 (NLP−1)−8HN} . TXS

When in 4-bit mode: TDIS= {8 (NLP−1)−2HN} .TXS

Fig. 6 Flyback period

LH5006A LCD Dot Matrix Driver CMOS LSI

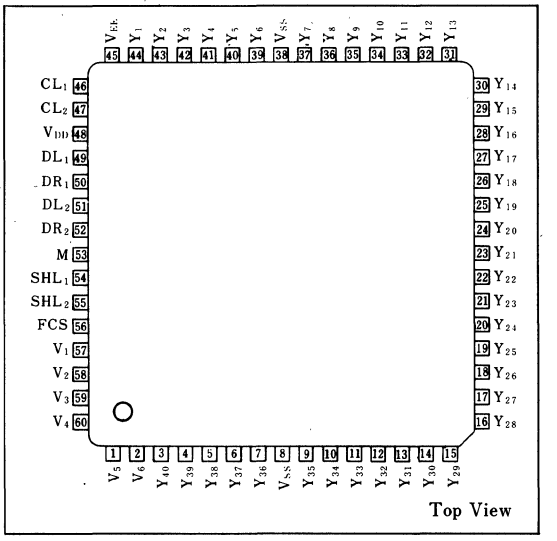
■ Description

The LH5006A has 2 sets of 20-stage bidirectional shift registers, 2 sets of 20-bit latches and 2 sets of 20 LCD drivers, so it converts serial character pattern data to parallel data and provides selected or nonselected waveforms output in accordance with mode select signal.

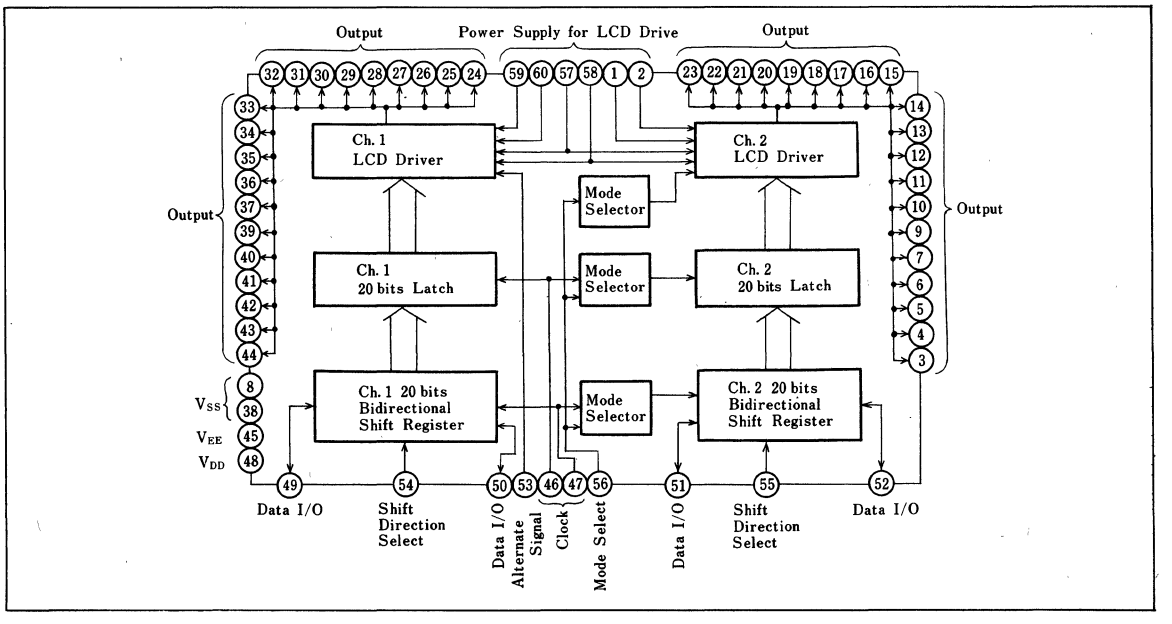
■ Features

1. CMOS process
2. 40-LCD driver circuit
   (a half of 40 drivers can be used either as segment signal drivers or as common signal drivers)
3. Single power supply : −5V (TYP.)
4. 60-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Pin Description

<table>
<tr><th>Pin name</th><th>Name</th><th>I/O</th><th>Functions</th></tr>
<tr><td>$Y_1 \sim Y_{20}$</td><td rowspan="2">Liquid crystal output</td><td rowspan="2">O</td><td>Ch. 1 liquid crystal output</td></tr>
<tr><td>$Y_{21} \sim Y_{40}$</td><td>Ch. 2 liquid crystal output</td></tr>
<tr><td>SHL_1</td><td>Ch. 1 data shift direction selection</td><td>I</td><td>
<table>
<tr><th>SHL_1</th><th>DL_1</th><th>DR_1</th><th>Shift direction</th></tr>
<tr><td>Low</td><td>IN</td><td>OUT</td><td>$SR_1 - SR_{20}$</td></tr>
<tr><td>High</td><td>OUT</td><td>IN</td><td>$SR_{20} - SR_1$</td></tr>
</table>
</td></tr>
<tr><td>SHL_2</td><td>Ch. 2 data shift direction selection</td><td>I</td><td>
<table>
<tr><th>SHL_2</th><th>DL_2</th><th>DR_2</th><th>Shift direction</th></tr>
<tr><td>Low</td><td>IN</td><td>OUT</td><td>$SR_{21} - SR_{40}$</td></tr>
<tr><td>High</td><td>OUT</td><td>IN</td><td>$SR_{40} - SR_{21}$</td></tr>
</table>
</td></tr>
<tr><td>FCS</td><td>Ch. 2 mode selection</td><td>I</td><td>
<table>
<tr><th>FCS</th><th>Mode</th></tr>
<tr><td>High</td><td>Common signal drive mode</td></tr>
<tr><td>Low</td><td>Segment signal drive mode</td></tr>
</table>
</td></tr>
<tr><td>M</td><td>Clock for liquid crystal drive circuit</td><td>I</td><td>
Common signal drive mode
<table>
<tr><th>M</th><th>Display</th><th>Non-display</th></tr>
<tr><td>High</td><td>V_2</td><td>V_6</td></tr>
<tr><td>Low</td><td>V_1</td><td>V_5</td></tr>
</table>
Segment signal drive mode
<table>
<tr><th rowspan="2">M</th><th rowspan="2">Display</th><th colspan="2">Non-display</th></tr>
<tr><th>Ch. 1</th><th>Ch. 1</th></tr>
<tr><td>High</td><td>V_1</td><td>V_5</td><td>V_3</td></tr>
<tr><td>Low</td><td>V_2</td><td>V_6</td><td>V_4</td></tr>
</table>
</td></tr>
<tr><td>DL_1, DR_1</td><td rowspan="2">Data output</td><td rowspan="2">I/O</td><td>Ch. 1 input/output</td></tr>
<tr><td>DL_2, DR_2</td><td>Ch. 2 input/output</td></tr>
<tr><td>CL_1, CL_2</td><td>Clock</td><td>I</td><td>Clock for data latch</td></tr>
<tr><td>V_1, V_2</td><td rowspan="3">Liquid crystal drive circuit output voltage supply</td><td rowspan="3">I</td><td>Durling select</td></tr>
<tr><td>V_3, V_4</td><td>Ch. 1 durling non-select</td></tr>
<tr><td>V_5, V_6</td><td>Ch. 2 durling non-select</td></tr>
<tr><td>V_{DD}</td><td rowspan="3">Power supply</td><td rowspan="3"></td><td>For logic circuit (−5V)</td></tr>
<tr><td>V_{EE}</td><td>For liquid crystal drive circuit (−17V)</td></tr>
<tr><td>V_{SS}</td><td>GND</td></tr>
</table>

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Applied voltage* (logic)	V_{DD}	+0.3～−7.0	V
Applied voltage* (LCD drive circuit)	V_{EE}	+0.3～−13.5	V
Input voltage*	V_{IN}	+0.3～V_{DD}−0.3	V
Operating temperature	T_{opr}	−10～+70	℃
Storage temperature	T_{stg}	−55～+150	℃

*The maximum applicable voltage on any pin with respect to V_{SS}.

■ DC Characteristics

(V_{SS}=GND, V_{DD}=−5±5%, V_{EE}=−10V±10%, Ta=−10～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}				−3.5	V
Input high voltage	V_{IH}		−1.5			V
Output low voltage	V_{OL}	I_{OL}=0.4mA			V_{DD}+0.4	V
Output high voltage	V_{OH}	V_{OH}=0.4mA	−0.4			V
Voltage drop between	V_{D1}	When 1mA current flows into one of the pins Y_1 through S_{40}			1.1	V
Y_1−Y_1	V_{D2}	When 0.2mA current flows into each of pins Y_1 through S_{40}			1.5	V
Input leakage current	$\|I_{LI}\|$				5.0	μA
Output leakage current	$\|I_{LO}\|$				10.0	μA
Logic current consumption	I_{LOG}	Logic clock 1.6MHz			3.0	mA
LCD driver current consumption	I_{DRV}	LCD driver clock 1kHz			10.0	μA

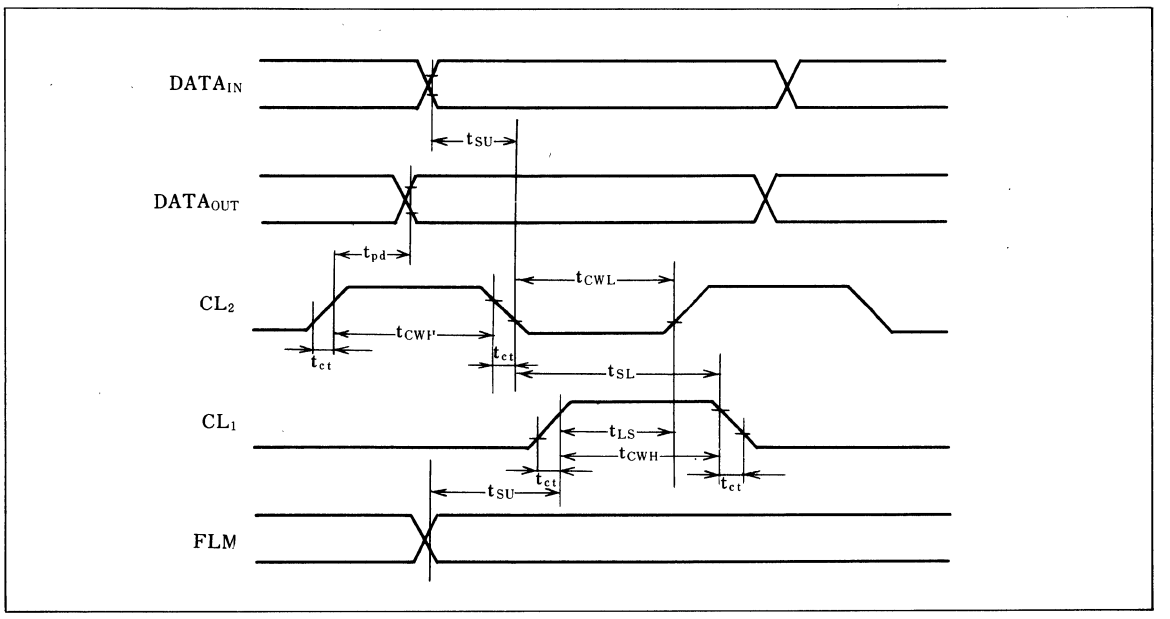
■ AC Characteristics

(V_{SS}=GND, V_{DD}=−5±5%, V_{EE}=−18～−16V, Ta=−10～+70℃)

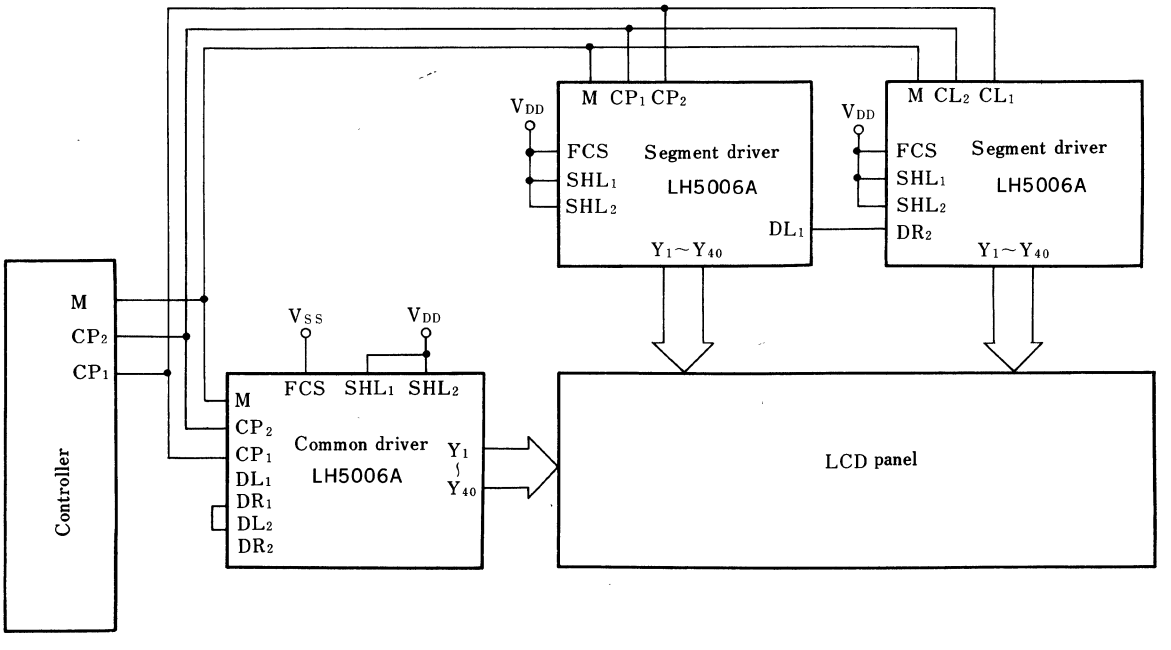
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock high width	t_{CWH}		250		ns	1
Clock low width	t_{CWL}		250		ns	2
Data setup time	t_{SU}		70		ns	3
Clock setup time (CL_2→CL_1)	t_{SL}		200		ns	1
Clock setup time (CL_1→CL_2)	t_{LS}		200		ns	1
Output delay time	t_{pd}	C_L=15pF		180	ns	3
Clock rise/fall time	t_{ct}			50	ns	1

Note 1: Applicable pins CL_1, CL_2
Note 2: Applicable pin CL_2
Note 3: Applicable pins DL_1, DR_1, DL_2, DR_2

■ Timing Diagram



■ System Configuration



10

LH5021A/LH5022 LCD Dot Matrix Driver CMOS LSI

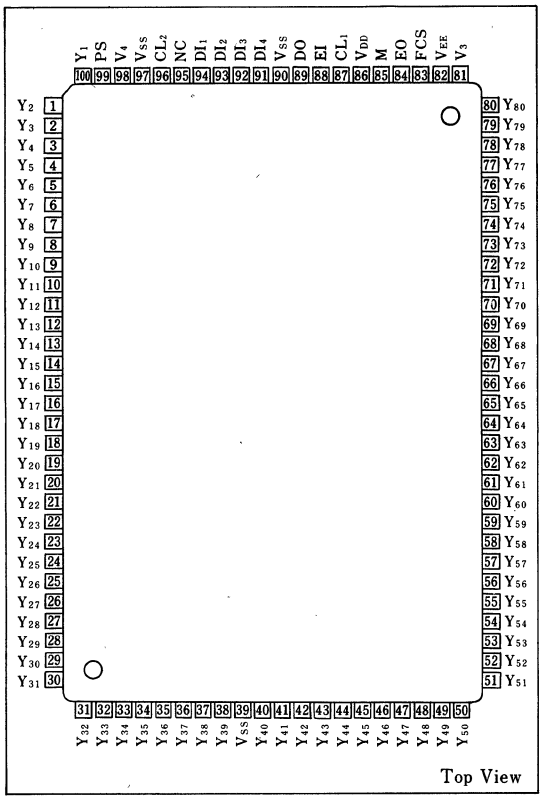
Description

LH5021A/LH5022 is an LCD driver LSI which can receive either serial input data or parallel input data. In case of the serial input mode, it can be connected in series. It converts character pattern data input to parallel data output with 80-bit latch circuit and provides character pattern waveforms output in accordance with mode select signal.

Features

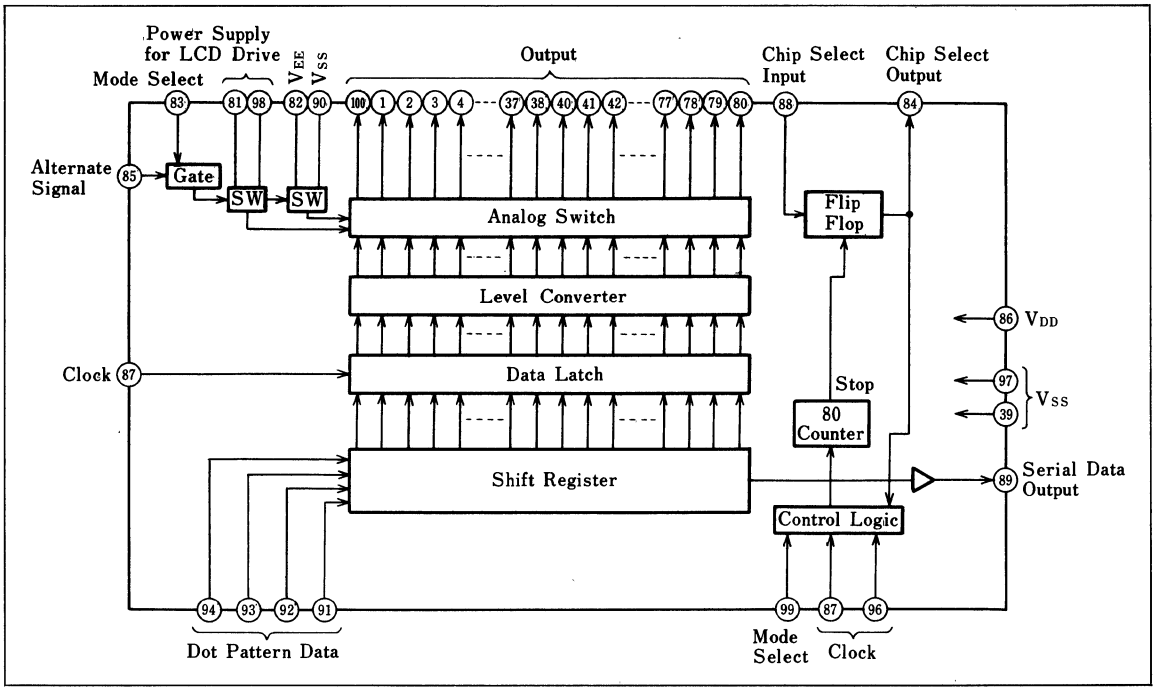
1. CMOS process
2. 80-LCD driver circuit
3. 4 functions selectable as follows
   (a) Segment signal drivers on the serial input mode
   (b) Segment signal drivers with the chip-selectable function on the serial input mode
   (c) Segment signal drivers with the chip-selectable function on the parallel input mode
   (d) Common signal drivers on the serial input mode
4. Auto count function ; in a chip selected state, counts 80 input data automatically and stops the internal clock CL_2
5. Power supply voltage : −5V (TYP.)
6. Display voltage
   LH5021A : −17V (TYP.),
   LH5022 : −24V (TYP.)
7. 100-pin quad-flat package

Pin Connections



Top View

■ Block Diagram



■ Pin Description

<table>
<tr><th>Pin name</th><th>Name</th><th>I/O</th><th>Functions</th></tr>
<tr><td>V_{DD}</td><td rowspan="3">Power supply</td><td rowspan="3"></td><td>For logic circuit (−5V)</td></tr>
<tr><td>V_{EE}</td><td>For liquid crystal drive circuit (LH5021A: −17V, LH5022: −24V)</td></tr>
<tr><td>V_{SS}</td><td>GND</td></tr>
<tr><td>V_3, V_4</td><td rowspan="2">Liquid crystal drive circuit output voltage supply</td><td rowspan="2">O</td><td>Durling non-select, however $V_{SS} > (V_3, V_4) > V_{EE}$</td></tr>
<tr><td>$Y_1 \sim Y_{80}$</td><td></td></tr>
<tr><td>CL_1</td><td rowspan="2">Clock</td><td rowspan="2">I</td><td>For data latch *Must be applied when 4 times the shift clock</td></tr>
<tr><td>CL_2</td><td>For data shift</td></tr>
<tr><td>FCS, PS</td><td>Mode select</td><td>I</td><td>
<table>
<tr><th>FCS</th><th>PS</th><th>Mode</th><th>Chip select</th><th>DO out.</th></tr>
<tr><td>Low</td><td>Low</td><td>1-bit serial input segment driver</td><td>×</td><td>○</td></tr>
<tr><td>Low</td><td>High</td><td>4-bit parallel input segment driver</td><td>○</td><td>High</td></tr>
<tr><td>High</td><td>Low</td><td>1-bit serial input segment driver</td><td>○</td><td>High</td></tr>
<tr><td>High</td><td>High</td><td>Commnn driver (serial input)</td><td>×</td><td>○</td></tr>
</table>
Note 1: In the serial input mode, data is supplied from the DI_1 pin.
Note 2: The relationship between data input during 4-bit parallel input and the Y output is as follows.
・DI_1 : Y_1, Y_5, Y_9, ⋯ Y_{13}, Y_{77}
・DI_2 : Y_2, Y_6, Y_{10}, ⋯ Y_{74}, Y_{78}
・DI_3 : Y_3, Y_7, Y_{11}, ⋯ Y_{75}, Y_{79}
・DI_4 : Y_4, Y_8, Y_{12}, ⋯ Y_{76}, Y_{80}
Note 3: When used as a comon driver, the clock used for transfer is input to the CL_2 pin. CL_1 is internally fixed.
Note 4: To minimize current consumption, it is necessary to fix unused input pins to the same level as the V_{SS} pin or the V_{DD} pin.
</td></tr>
<tr><td>M</td><td>Liquid crystal drive waveform AC conversion signal input</td><td>I</td><td>
Common signal drive mode
<table>
<tr><th>Latch data</th><th>M</th><th>Y out.</th></tr>
<tr><td rowspan="2">Low (non-display)</td><td>Low</td><td>V_3</td></tr>
<tr><td>High</td><td>V_4</td></tr>
<tr><td rowspan="2">High (display)</td><td>Low</td><td>V_{EE}</td></tr>
<tr><td>High</td><td>GND</td></tr>
</table>
Segment signal drive mode
<table>
<tr><th>Latch data</th><th>M</th><th>Y out.</th></tr>
<tr><td rowspan="2">Low (non-display)</td><td>Low</td><td>V_3</td></tr>
<tr><td>High</td><td>V_4</td></tr>
<tr><td rowspan="2">High (display)</td><td>Low</td><td>GND</td></tr>
<tr><td>High</td><td>V_{EE}</td></tr>
</table>
</td></tr>
<tr><td>$DI_1 \sim DI_4$</td><td>Display data input</td><td>I</td><td>When used with a common driver and in the serial input mode, supply the data to the DI_1 pin. In this case, it is necessary to fix $DI_2 - DI_4$ to the V_{SS} level or the V_{DD} level.</td></tr>
<tr><td>DO</td><td>Serial data output</td><td>O</td><td>When used in the chip select mode, it becomes high level.</td></tr>
<tr><td>EI</td><td rowspan="2">For chip select</td><td>I</td><td rowspan="2">Used only in the chip select mode.
(1) The (CL_1 ・ CL_2) timing causes EO to become low level.
(2) After (1), the device is set to the select mode by inputting a high signal to EI, and the input data is read in according to the timing of the fall of CL_2.
(3) When 80 items of input data (equivalent to 80 CL_2 clock cycles in the serial mode or 20 CL_2 clock cycles in the 4-bit parallel mode) have been read in, EO automatically becomes high level and data read in is terminated. EO is reset 1.5 cycles later.</td></tr>
<tr><td>ED</td><td>O</td></tr>
</table>

Pin name	Name	I/O	Functions
			(4) When two or more devices are used in the chip select mode, EO of the first stage and EI of the second stage are connected and used. 1. EO of all devices connected is reset by (1) and goes to the non-select condition and waits for EI input. 2. When a high signal is applied to EI of the initial device in the cascade connection, this device performs the operations in (2) and (3). 3. Connecting EO of the initial devices to EI of the next devices causes the devices perform the operations in (2) and (3) after the initial device. This operation is repeated in the same manner for all subsequent devices. In the non-select condition, the shift clock CL_2 stops internally, so power consumption becomes extremely small.

■ Absolute Maximum Ratings

Parameter	Symbol	LH5021A Ratings	LH5022 Ratings	Unit	Note
Applied voltage (logic)	V_{DD}	−7∼+0.3	−7∼+0.3	V	1
Applied voltage (Liquid crystal drive circuit)	V_{EI}	−20∼+0.3	−30∼+0.3	V	1
Input voltage (logic)	V_{IN}	V_{DD}−0.3∼+0.3	V_{DD}−0.3∼+0.3	V	1
Operating temperature	T_{opr}	−20∼+70	−20∼+70	℃	
Storage temperature	T_{stg}	−55∼+150	−55∼+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to V_{SS}.

■ DC Characteristics

Parameter	Symbol	Conditions	LH5021A*1			LH5022*2			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input low voltage	V_{IL}				$0.8V_{DD}$			$0.8V_{DD}$	V
Input high voltage	V_{IH}		$0.2V_{DD}$			$0.2V_{DD}$			V
Output high voltage	V_{OL}	I_{OL}=0.4mA			V_{DD}+0.4			V_{DD}+0.4	V
Output low voltage	V_{OH}	I_{OH}=0.4mA	−0.4			−0.4			V
Voltage fall between V_i−Y_i	V_{D1}	1 mA to one of Y_1−Y_{80}			1.1			1	V
Voltage fall between V_i−Y_i	V_{D2}	0.2 mA to each of Y_1−Y_{80}			1.5			1.5	V
Input leakage current	$\lvert I_{LX} \rvert$				1			1	μA
Output leakage current	$\lvert I_{LO} \rvert$				10			10	μA
Logic circuit selection current consumption	I_{LOG}	1 bit serial transfer (3.3MHz)		2.2	6.0		2.0	5.0	mA
		4 bit parallel transfer (2.0MHz)		1.0	2.0		1.0	2.0	mA

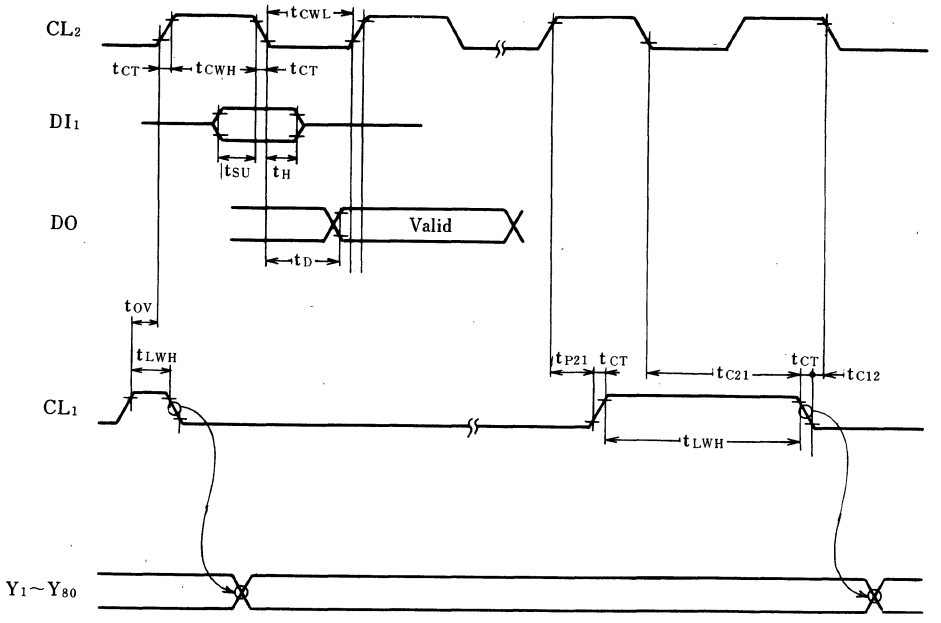
*1 V_{EE}=−17V±1V
*2 V_{EE}=−24V

■ AC Characteristics

(1) 1-bit Serial Input Segment Driver (PS=FCS="Low") (V_{DD}=−5V±10%, V_{SS}=0V, Ta=−20~+70℃)

Parameter	Symbol	Conditions *1	MIN.	MAX.	Unit	Applicable pins
Clook frequency	t_C		300		ns	CL_2
High-level clock width	t_{CWH}		130		ns	CL_2
Low-level clock width	t_{CWL}		130		ns	CL_1, CL_2
Data setup time	t_{SU}		70		ns	DI_1
Data hold time	t_H		50		ns	DI_1
Output delay	t_D	C_L=15pF		230	ns	DO
High-level latch clock width	t_{LWH}		130	*3	ns	CL_1
Clock margin time (from CL_1 ↓ to CL_2 ↓)	t_{C12}		20		ns	CL_1, CL_2
Clock margin time *2 (from CL_2 ↓ to CL_1 ↓)	t_{C21}		200		ns	CL_1, CL_2
Clock margin time (from CL_2 ↑ to CL_1 ↑)	t_{P21}		20		ns	CL_1, CL_2
Clock ↑, ↓ time	t_{CT}			50	ns	CL_1, CL_2
Overlap time of CL_2 "L" and CL_1 "H"	t_{OV}		130		ns	CL_1, CL_2

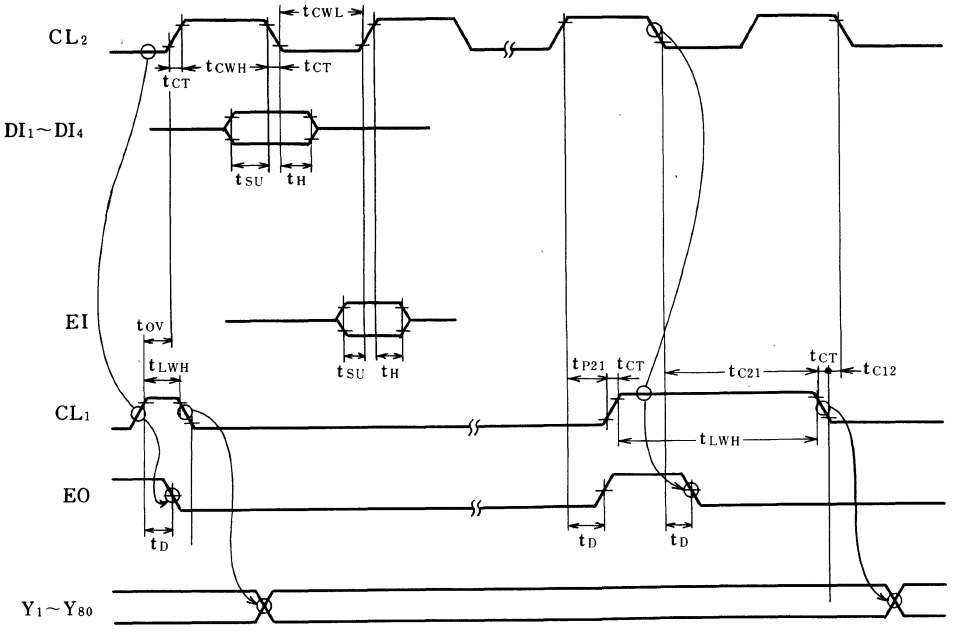
Test conditions
Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.2V_{DD}$, $0.8V_{DD}$
*1 LH5021A V_{EE}=−17V±1V, LH5022 : V_{EE}=−24V
*2 Internal shift register determination time
*3 $1.5t_C-t_{C12}-t_{P21}-3t_{CT}$



(2) **4-bit Input Segment Driver** (PS="High", FCS="Low") ($V_{DD}=-5V\pm10\%$, $V_{SS}=0V$, $Ta=-20\sim+70℃$)

Parameter	Symbol	Conditions*1	MIN.	MAX.	Unit	Applicable pins
Clock frequency	t_C		500		ns	CL_2
High-level clock width	t_{CWH}		230		ns	CL_2
Low-level clock width	t_{CWL}		230		ns	CL_1, CL_2
Data setup time	t_{SU}		70		ns	DI_1, DI_2, DI_3, DI_4, EI
Data hold time	t_H		50		ns	DI_1, DI_2, DI_3, DI_4, EI
Output delay	t_D	$C_L=15pF$		230	ns	EO
High-level latch clock width	t_{LWH}		130	*3	ns	CL_1
Clock margin time (from $CL_1\downarrow$ to $CL_2\downarrow$)	t_{C12}		20		ns	CL_1, CL_2
Clock margin time *2 (from $CL_2\downarrow$ to $CL_1\downarrow$)	t_{C21}		200		ns	CL_1, CL_2
Clock margin time (from $CL_2\uparrow$ to $CL_1\uparrow$)	t_{P21}		20		ns	CL_1, CL_2
Clock $\uparrow$, $\downarrow$ time	t_{CT}			50	ns	CL_1, CL_2
Overlap time of CL_2 "L" and CL_1 "H"	t_{OV}		130		ns	CL_1, CL_2

Test conditions
Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.2V_{DD}$, $0.8V_{DD}$
*1 LH5021A $V_{EE}=-17V\pm1V$, LH5022 : $V_{EE}=-24V$
*2 Internal shift register determination time
*3 $1.5t_C-t_{C12}-t_{P21}-3t_{CT}$

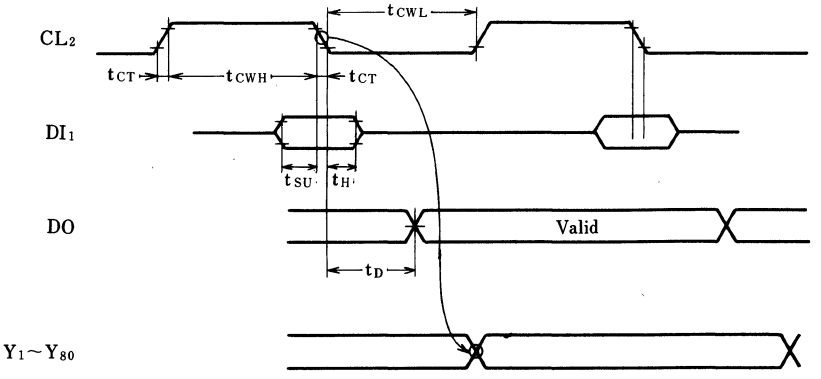


(3) Common Driver (PS="Low", FCS="High")

(V_{DD}=−5V±10%, V_{SS}=0V, Ta=−20~+70℃)

Parameter	Symbol	Conditions*1	MIN.	MAX.	Unit	Applicable pins
Clock frequency	t_C		1000		ns	CL_2
High-level clock width	t_{CWH}		130		ns	CL_2
Low-level clock width	t_{CWL}		830		ns	CL_2
Data setup time	t_{SU}		70		ns	DI_1
Data hold time	t_H		50		ns	DI_1
Output delay	t_D	C_L=15pF		500	ns	DO
Clock ↑, ↓ time	t_{CT}			50	ns	CL_2

Test conditions
Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.8V_{DD}$, $0.2V_{DD}$
*1 LH5021A V_{EE}=−17V±1V, LH5022 : V_{EE}=−24V

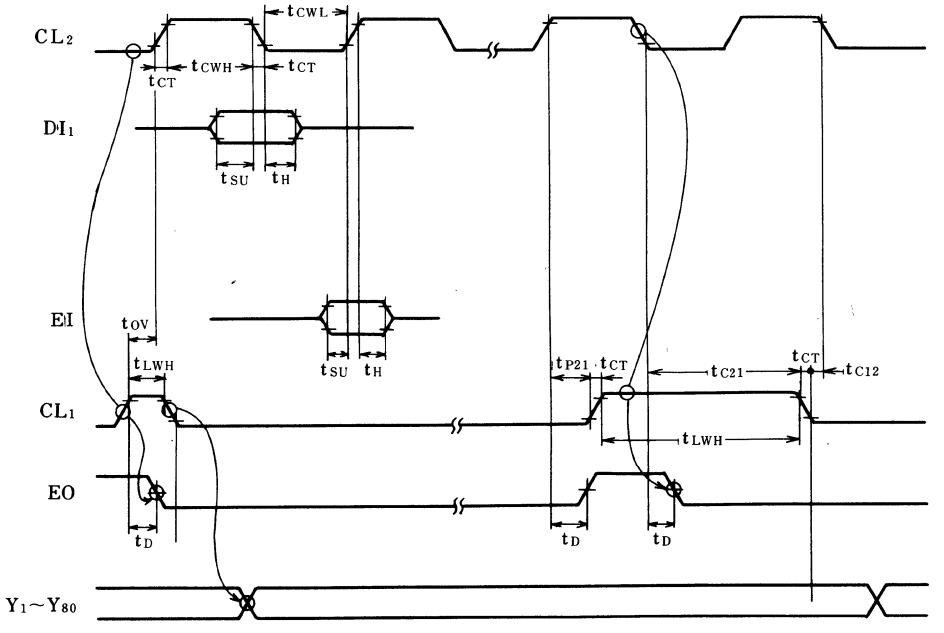


(4) 1-bit Serial Input Segment Driver (PS="Low", FCS="High")

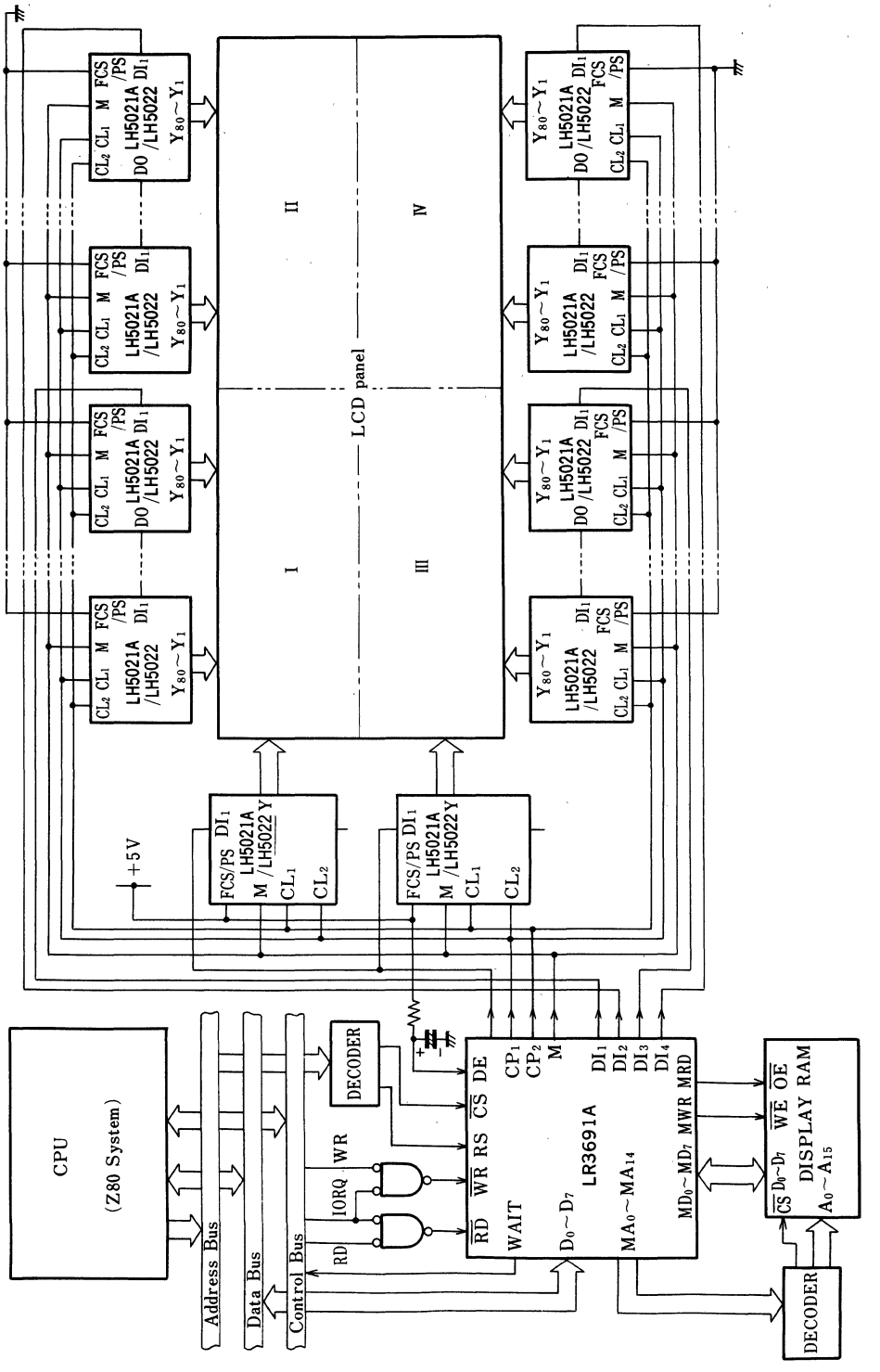
(V_{DD}=−5V±10%, V_{SS}=0V, Ta=−20~+70℃)

Parameter	Symbol	Conditions *1	MIN.	MAX.	Unit	Applicable pins
Clock frequency	t_C		380		ns	CL_2
High-level clock width	t_{CWH}		170		ns	CL_2
Low-level clock width	t_{CWL}		170		ns	CL_1, CL_2
Data setup time	t_{SU}		70		ns	DI_1, EI
Data hold time	t_H		50		ns	DI_1, EI
Output delay	t_D	C_L=15pF		230	ns	EO
High-level latch clock width	t_{LWH}		130	*3	ns	CL_1
Clock margin time (from CL_1 ↓ to CL_2 ↓)	t_{C12}		20		ns	CL_1, CL_2
Clock margin time *2 (from CL_2 ↓ to CL_1 ↓)	t_{C21}		200		ns	CL_1, CL_2
Clock margin time (from CL_2 ↑ to CL_1 ↑)	t_{P21}		20		ns	CL_1, CL_2
Clock ↑, ↓ time	t_{CT}			50	ns	CL_1, CL_2
Overlap time of CL_2 "L" and CL_1 "H"	t_{OV}		130		ns	CL_1, CL_2

Test conditions
Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.2V_{DD}$, $0.8V_{DD}$
*1 LH5021A V_{EE}=−17V±1V, LH5022 : V_{EE}=−24V
*2 Internal shift register determination time
*3 $1.5t_C-t_{C12}-t_{P21}-3t_{CT}$



■ System Configuration Example



LH5821/LH5822/LH5823

LCD Dot Matrix Driver CMOS LSI

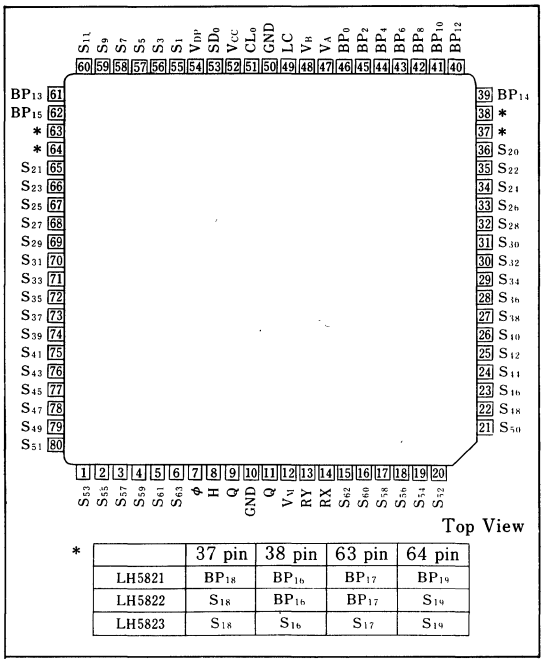
■ Description

The LH5821/LH5822/LH5823 are CMOS driver LSIs for LCD dot matrix display.
Any one of display duty ratio, 1/7 ~ 1/20 can be selected by programming.
Write and read to/from the built-in RAM of display data can be made only by 3 signals, serial data, synchronous signal, and transfer clock.
The LH5826 is available for segment output expansion.

■ Features

1. Display data RAM : 1280bits
2. 10-bit serial data transfer
3. Built-in oscillator for display
4. Duty (Selectable by programming)
   LH5821 : 1/7~1/20
   LH5822 : 1/7~1/18
   LH5823 : 1/7~1/16
5. Segment output
   LH5821 : 44bits
   LH5822 : 46 bits
   LH5823 : 48 bits
6. Common output
   LH5821 : 20 bits
   LH5822 : 18 bits
   LH5823 : 16 bits
7. Clock output for double voltage
8. Power supply voltage : 5V (TYP.)
9. Display voltage
   LH5821, LH5822 : 12V (MAX.)
   LH5823 : 10V (MAX.)
10. 80-pin quad-flat package

■ Pin Connections

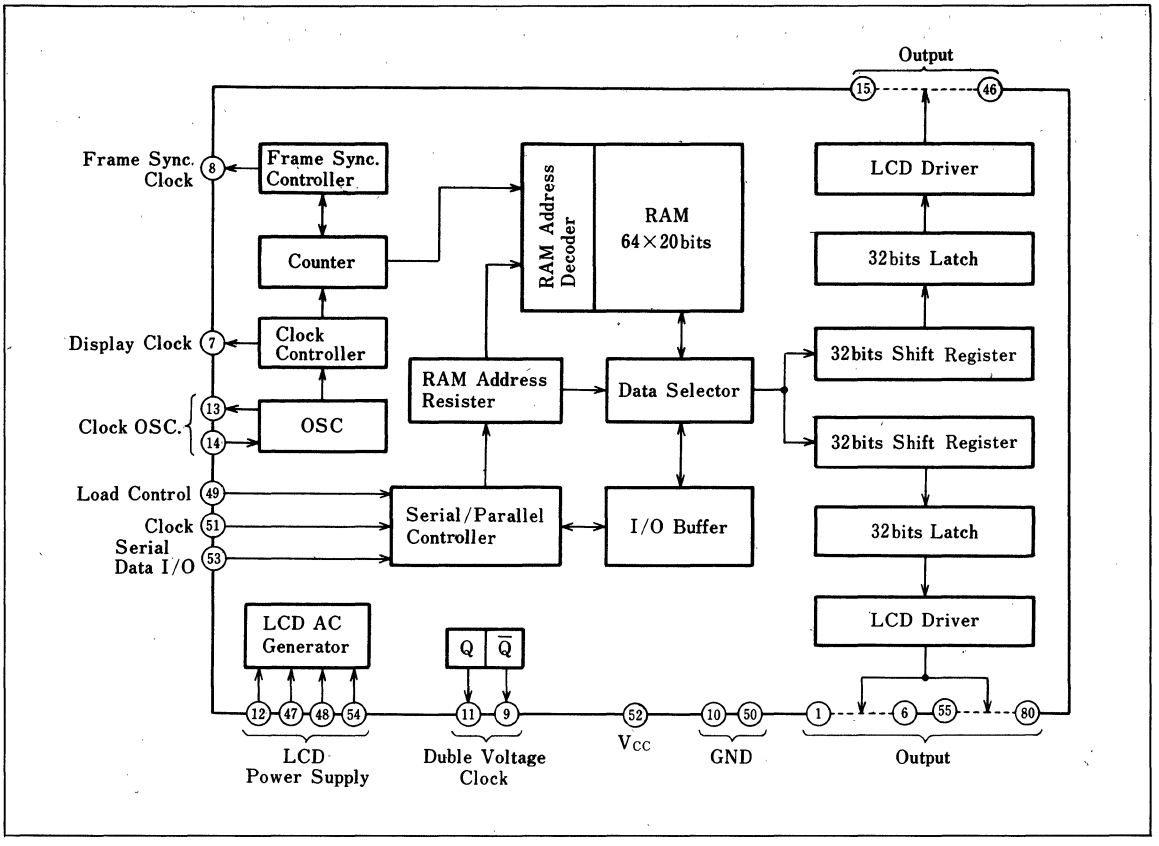


Top View

*

	37 pin	38 pin	63 pin	64 pin
LH5821	BP_{18}	BP_{19}	BP_{17}	BP_{19}
LH5822	S_{18}	BP_{16}	BP_{17}	S_{19}
LH5823	S_{18}	S_{16}	S_{17}	S_{19}

■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage*	V_{CC}	−0.3～+7	V	1
	V_{DP}	−0.3～+13(+11)	V	1
Operating temperature	T_{opr}	−5～+55	℃	
Storage temperature	T_{stg}	−5～+150	℃	

Note 1: Referenced to GND. Value in parentheses ( ) applies to LH5823.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{CC}	4.5		5.5	V	
Display voltage	V_{DP}	6		12(10)	V	2

Note 2: Value in parentheses ( ) applies to LH5823.

■ DC Characteristics

(V_{CC}=4.5～5.5V, Ta=−5～55℃)

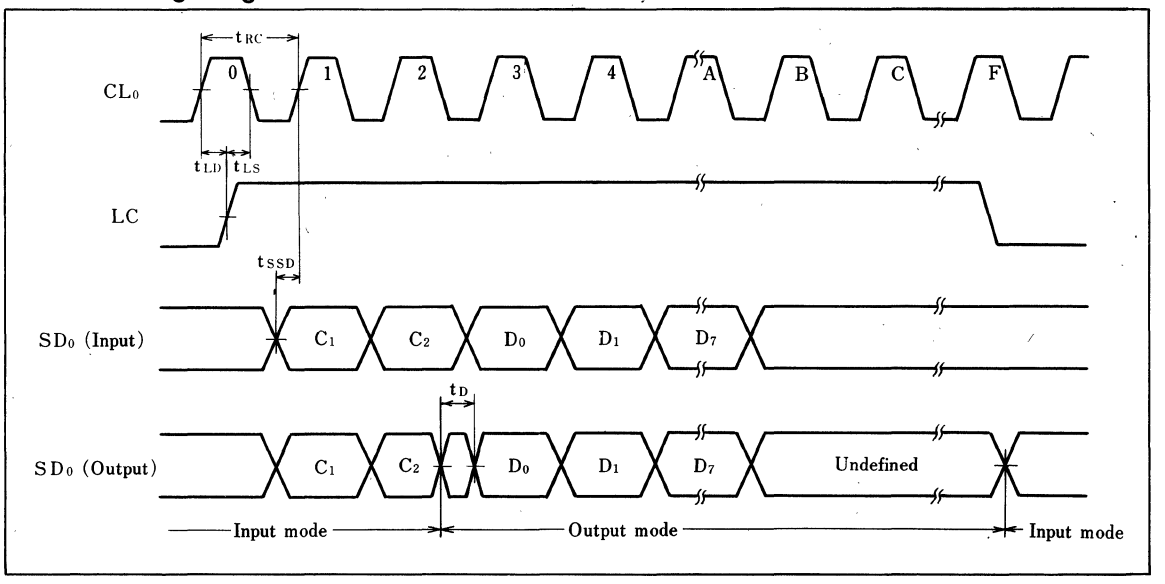
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		V_{CC}−0.8		V_{CC}	V	3
	V_{IL}		0		0.8		
Input current	I_{IH}	$V_{IH}=V_{CC}$		25	50	μA	4
	I_{IL}	V_{IL}=0V			1		
Output voltage	V_{OH}	I_{OH}=410 μA	2.4			V	5
	V_{OL}	I_{OL}=1.6mA			0.8		
Output resistance	R_Q	V_{CC}=5V, V_{DS}=1.0V		80		Ω	7
	R_{SEG}	V_{DP}=6V, Ta=25℃, V_{DS}=1V		1.0	30	kΩ	8
	R_{COM}			1.5	4.5	kΩ	9
	R_V			40	1	Ω	10
Input leakage current	$\|I_L\|$					μA	6
Current consumption	I_{CC1}	Durling no-load blank display f_ϕ=100kHz, f_{CL0}=0Hz, Ta=25℃		200	500	μA	
	I_{CC2}	Durling data write (write cycle 1/45 MHz) f_ϕ=100kHz, f_{CL0}=1MHz, Ta=25℃			2	mA	
	I_{DP}	Durling no-load blank display V_{DP}=12V, f_ϕ=100kHz, 1/16 duty		5	10	μA	

Note 3: Applied to pins CL_0, LC, SD_0
Note 4: Applied to pin LC
Note 5: Applied to pins SD_0, H, ϕ
Note 6: Applied to all pins except LC
Note 7: Applied to pins Q, $\overline{Q}$
Note 8: Applied to segment output pin.
Note 9: Applied to common output pin.
Note10: Applied to pins V_A, V_B

■ AC Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CL_0 cycle time	t_{RC}		1			μs
LC hold time	t_{LD}		0			ns
LC setup time	t_{LS}		100			ns
SD_0 setup time	t_{SSD}		100			ns
SD_0 input/output switching time	t_D	C_L=50pF		80	450	ns

■ AC Timing Diagram



■ Functions

(1) Pin description

Pin name	No. of pins	I/O	Functions
V_{CC}, GND	3	I	Power supply for logic circuit
V_{DP}, V_A, V_M, V_B	4		Power supply for liquid crystal drive
LC	1		Serial data transfer sync. signal
CL_0	1		Serial data transfer clock input
RX	1		Input clock oscillation pin
RY	1	O	Input clock oscillation pin
ϕ	1		Clock output for display
H	1		Liquid crystal frame sync. signal
Q, $\overline{Q}$	2		Clock output for double voltage generation
S_{20}~S_{63} (LH5821)	44		Liquid crystal segment drive signal
S_{18}~S_{63} (LH5822)	46		
S_{16}~S_{63} (LH5823)	48		
BP_0~BP_{19} (LH5821)	20		Liquid crystal common drive signal
BP_0~BP_{17} (LH5822)	18		
BP_0~BP_{15} (LH5823)	16		
SD_0	1	I/O	Serial data input/output

(2) Relationship between 10-bit serial data and modes

10-bit data/mode	C_0	C_1	D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
Chip select/duty setup mode	0	0	Chip select data | Duty data
RAM address setup mode	0	1	A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
8-bit data write mode	1	0	Data
8-bit data read mode	1	1	Data

(C_1, C_2 : Control data, D_0~D_7 : Data)

• LC single

The LC signal is a sync. signal for serial transfer, and when LC is low, LSI remains in the standby condition regardless of the condition of SD_0 and CL_0, When LC becomes high and clock CL_0 is supplied, the LSI is enabled.

• CL signal

The CL signal is the clock signal for serial transfer and is used to write and read serial transfer data SD_0.

• SD_0 signal

The SD_0 signal is 10-bit serial transfer data of which the first 2 bits are control data and the remaining 8 bits are data. In the read mode the SD_0 pin becomes an output pin and outputs the 8-bit RAM data in serial. After the write or read mode has been executed, the lower 6 bits, A_0-A_5, of the RAM address are automatically incremented, but A_6 and A_7 do not change.

• Chip select

In the LSI, the chip select code is set at "0000", so by inputting the chip select code "0000" through the SD_0 pin, this chip is selected.

The RAM address setting and writing and reading of the 8-bit data is executed only for the chip selected, and once a chip is selected, it remains in the selected condition until a select code for the next chip is input.

• ϕ signal

The ϕ signal is the clock output for display and is supplied to LH5826.

• H signal

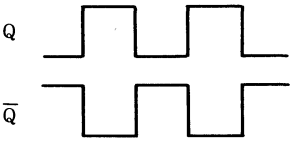
The H signal is the frame period signal for the liquid crystal and is supplied to LH5826. When the power is turned on, the timing signal in each device is in an unsynchronized condition, and after the H signal is generated, they are synchronized.

• Auto clear

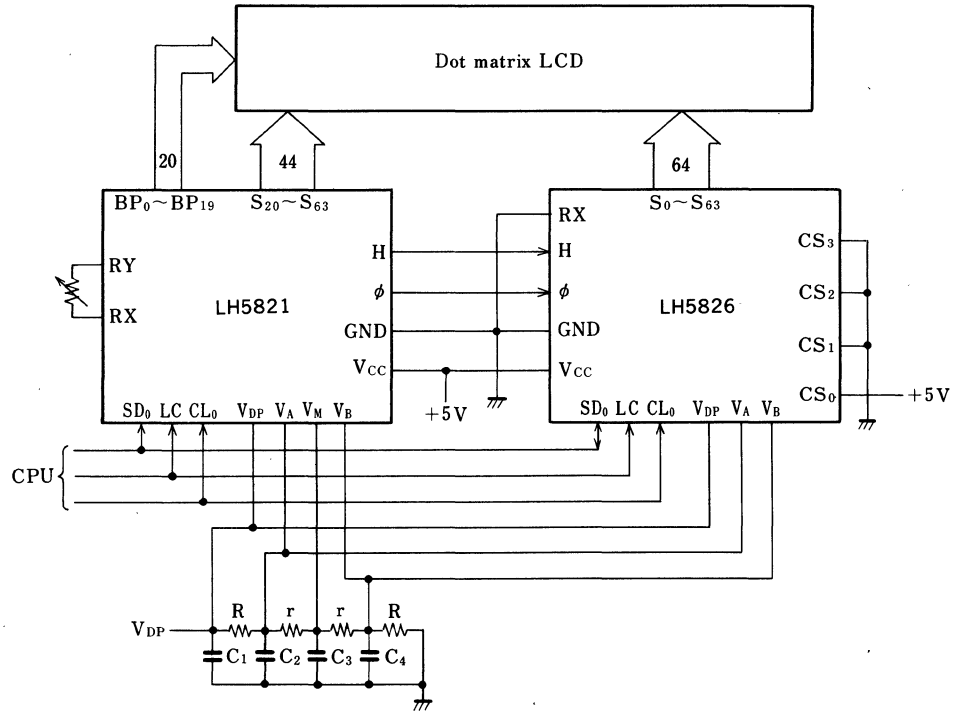
When the power is turned on, the display signal generates an OFF pattern. Auto clear is canceled when all of the duty data of the chip select duty data are made "1" and input, and then the contents of the RAM are displayed. The chip select duty does not change at this time.

• Double voltage clock

A double voltage clock is output from pins Q and $\overline{Q}$. The Q and $\overline{Q}$ signals are clock signals made by dividing the display clock ϕ by 2, and their respective polarities are opposite.



■ System Configuration



LH5826 LCD Dot Matrix Segment Driver CMOS LSI

■ Description

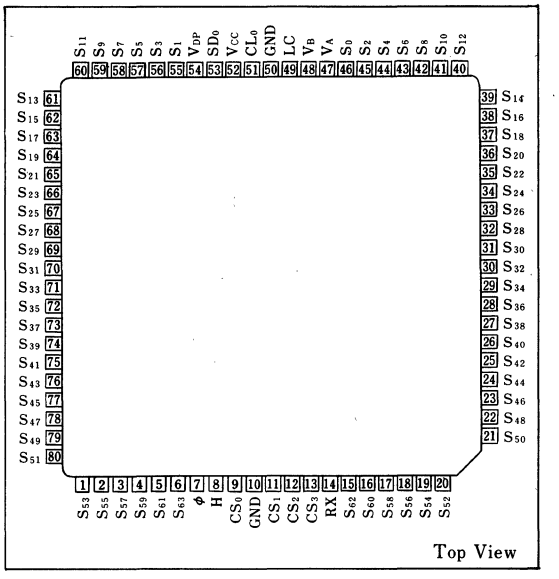
The LH5826 is a segment driver CMOS LSI for LCD dot matrix display. Write and read to/from the built-in RAM of display data can be made only by 3 signals, serial data, synchronous signal, and transfer clock.

The LH5826 is available for segment output expansion of the LH5821, LH5822 and LH5823.

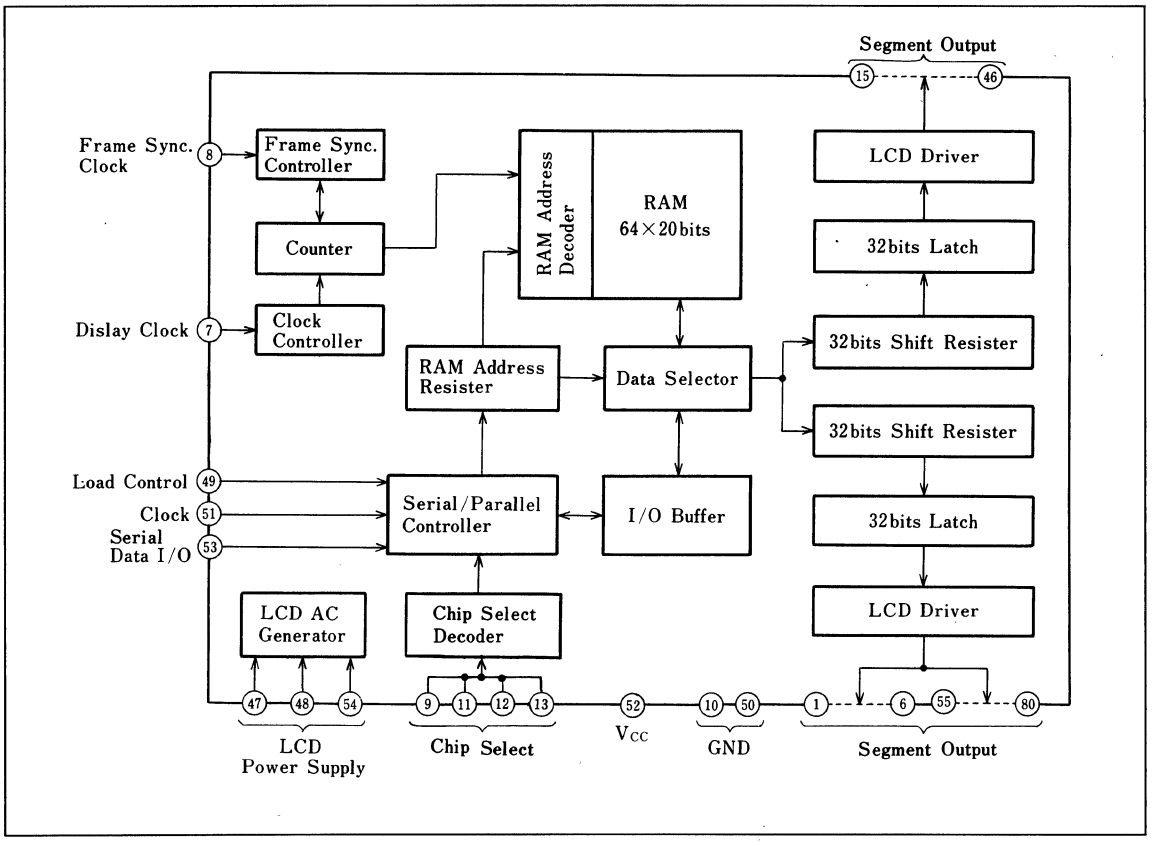
■ Features

1. Display data RAM : 1280 bits
2. 10-bit serial data transfer
3. Segment output : 64 bits
4. Up to 15 drivers expandable
5. Power supply voltage : 5V (TYP.)
6. Display voltage : 12V (MAX.)
7. 80-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{CC}	−0.3～+7	V	1
	V_{DP}	−0.3～+13		
Operating temperature	T_{opr}	−5～+55	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note:1 Referenced to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5		5.5	V
Display voltage	V_{DP}	6		12	V

10

■ DC Characteristics

(V_{CC}=5V±10%, Ta=−5~+55℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		V_{CC}−0.8		V_{CC}	V	2
	V_{IL}		0		0.8		
Input current	I_{IH}	V_{IH}=V_{CC}		25	50	μA	3
	I_{IL}	V_{IL}=0V			1		
Output voltage	V_{OH}	I_{OH}=400μA	2.4			V	4
	V_{OL}	I_{OL}=1.6mA			0.8		
I/O leakage current	$\lvert I_L \rvert$				1	μA	5
Output resistance	R_{SEG}	V_{DP}=6V, V_{DS}=1V, Ta=25℃		10	30	kΩ	6
Current consumption	I_{CC1}	During still image display under no load $f\phi$=100kHz, f_{CLO}=0Hz, Ta=25℃		200	500	μA	
	I_{CC2}	During data write (write cycle 1/45 MHz) $f\phi$=100kHz, f_{CLO}=1MHz, Ta=25℃			2	mA	
	I_{DP}	During still image display under no load V_{DP}=12V, $f\phi$=100kHz, 1/20duty		5	10	μA	

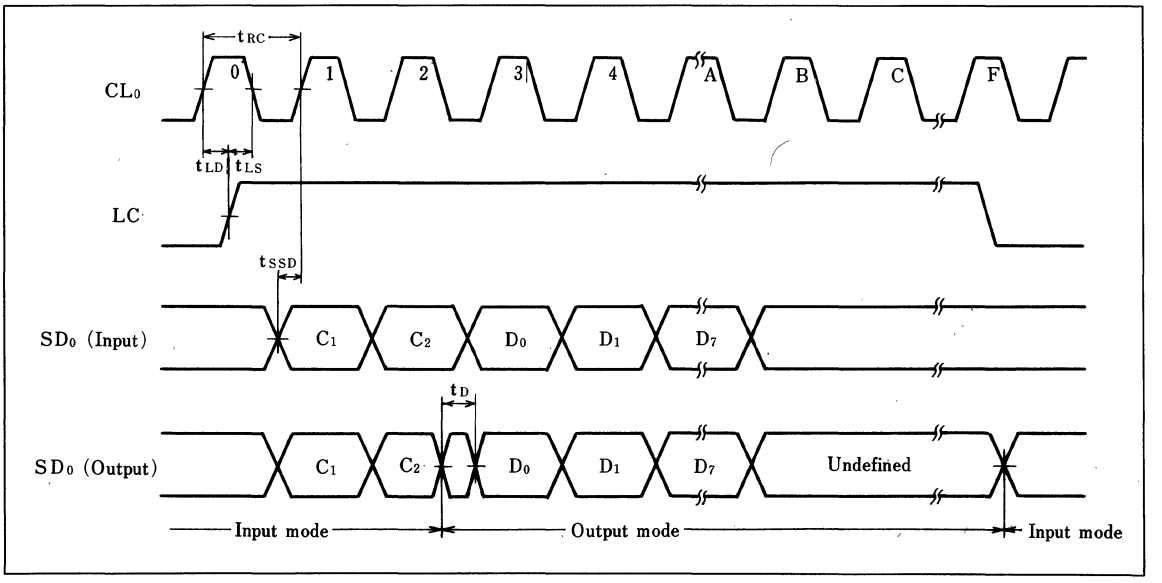
Note 2: Applied to pins CL_O, LC, SD_O, H, and ϕ.
Note 3: Applied to pin LC.
Note 4: Applied to pin SD_O.
Note 5: Applied to all pins other than LC.
Note 6: Applied to pins S_O-S_{63}.

■ AC Characteristics

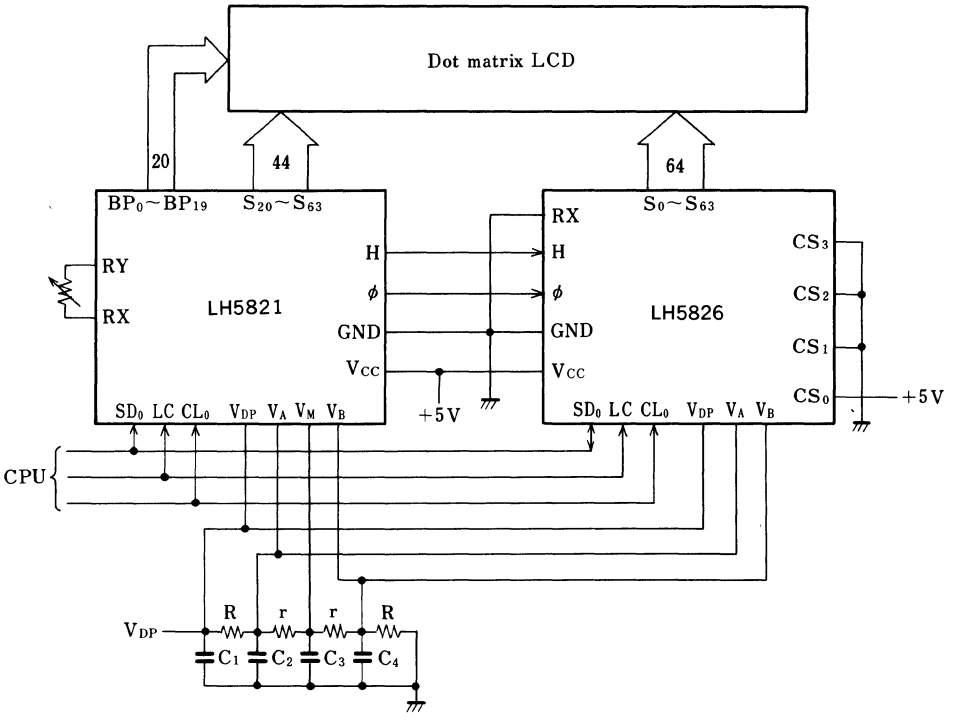
(Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CL_O cycle time	t_{RC}		1			μs
LC hold time	t_{LB}		0			ns
LC setup time	t_{LS}		100			ns
SD_O setup time	t_{SSD}		100			ns
SD_O I/O switching time	t_{LD}	C_L=50pF		80	450	ns

■ AC Timing Diagram



System Configuration



■ Functions

(1) Pin Description

Signal	No. of pins	I/O	Function
V_{CC}, GND	3	I	Power supply for logic circuit
V_{DP}, V_A, V_B	3		LCD driving power
ϕ	1		Display clock input
H	1		LCD frame sync signal
CS_0~CS_3	4		Chip select input
LC	1		Serial data transfer sync signal
CL_0	1		Serial data transfer clock input
RX	1		Connected V_{CC} or GND
S_0~S_{63}	64	O	LCD segment driver signal
SD_0	1	I/O	Serial data I/O

(2) 10-bit serial data versus mode

10-bit data/mode	C_1	C_2	D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
Chip Select Duty Setting Mode	0	0	Chip Select Data ; Duty Data
RAM Address Setting Mode	0	1	A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
8-bit Data Write Mode	1	0	Data
8-bit Data Read Mode	1	1	Data

(C_1, C_2: Control Data, D_0-D_7: Data)

● LC signal

The LC is a serial transfer sync signal input. If the LC is at low, the LH5826 maintains standby status ignoring the statuses of SD_0 and CL_0. The device enters the enable status when the LC is set at high and the clock CL_0 is supplied.

● CL_0 signal

The CL_0 is a serial transfer clock input used for writing or reading serial transfer data SD_0.

● SD_0 signal

The SD_0 is a 10-bit serial transfer data line. Data consists of two control bits and 8 data bits. When in the Read mode, the SD_0 pin functions as an output to deliver 8-bit RAM data in serial form. When read or write operation is completed, the lower 6 bits, A_0-A_5, of the RAM address are incremented. Bits A_6 and A_7 do not change, however.

● CS_0-CS_3 pins

The CS_0-CS_3 are chip select inputs. On the LH5826,
the chip select code can take on a value between 0001 and 1111 for CS_3, CS_2, CS_1, and CS_0, respectively. Chip select code 0000, used to select the LH5821-5823, cannot be used for the LH6826.

● ϕ signal

The ϕ is a display clock input. The clock is supplied from the LH5821-5823.

● H signal

The H pin accepts an LCD frame sync signal from the LH5821-LH5823. When power is turned on, the internal timing signals of each device are asynchronous with each other. They are synchronized when the H signal is activated.

● Auto clear

When power is turned on, the display provides an OFF pattern (screen clear). The Auto Clear feature is deactivated when all the chip select duty data are set at "1" whereupon the contents of RAM are displayed on the screen. At this time the chip select duty does not change.

LH5035A/LH5036A

LCD Dot Matrix Segment Driver CMOS LSI

■ Description

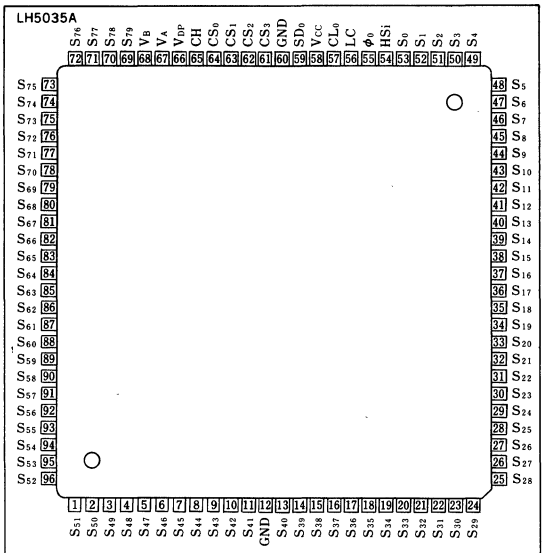
The LH5035A/LH5036A are segment driver CMOS LSIs for LCD dot matrix graphic display. To change the built-in 3.2K bit RAM contents enables the display pattern to be changed.

■ Features

1. Display data RAM : 3200 bits
2. Segment output : 80 bits
3. 1/32 or 1/40 duty
4. Automatic address modify
5. Scroll function
6. Power supply voltage : 5V (TYP.)
7. Display voltage : 15V (MAX.)
8. 96-pin quad-flat package

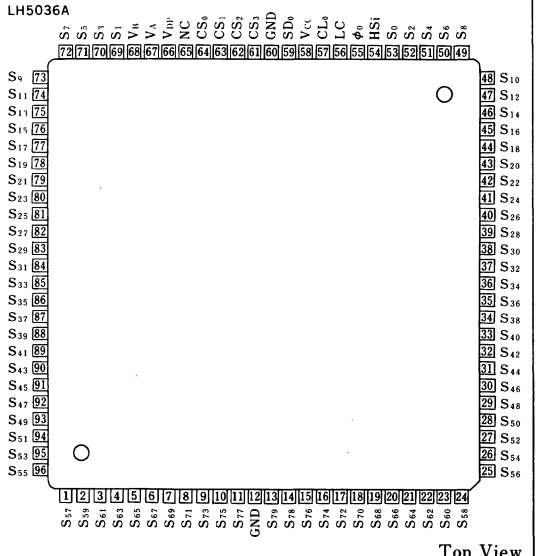
■ Pin Connections

LH5035A



Top View

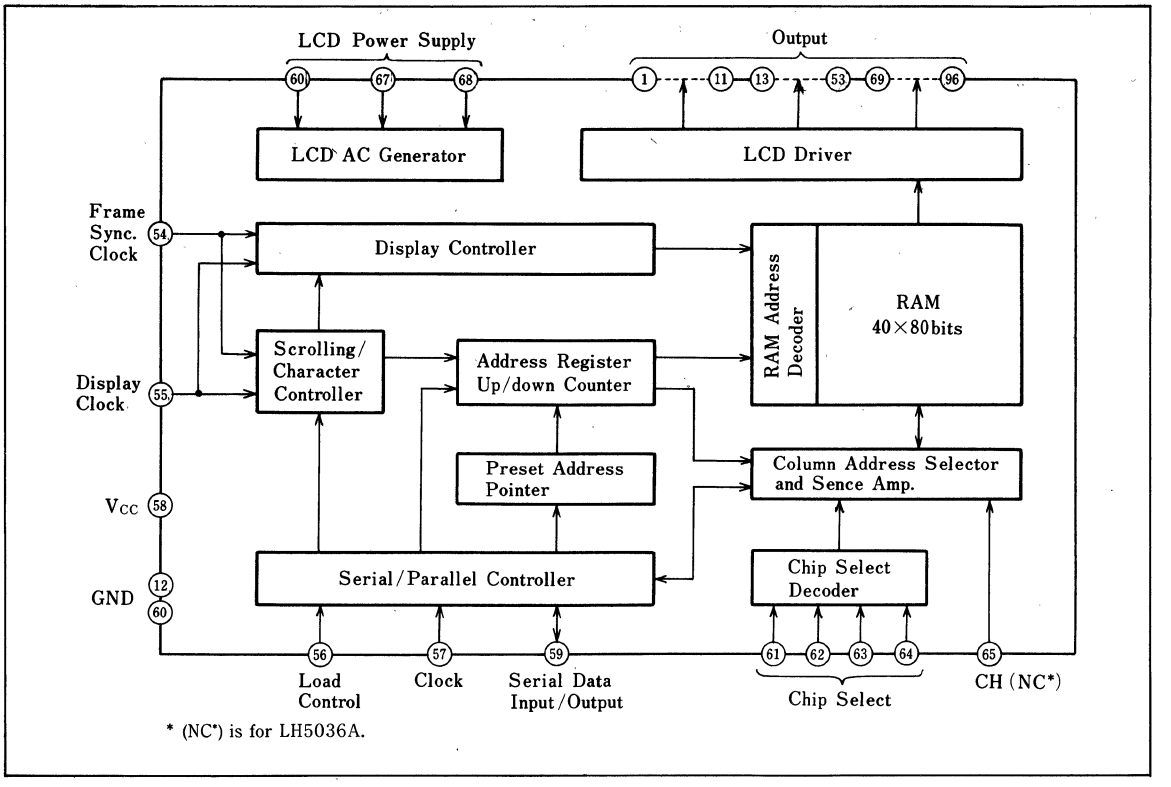
LH5036A



Top View

10

■ Block Diagram



* (NC*) is for LH5036A.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{CC}	−0.3~+0.7	V	1
	V_{DP}	−0.3~+16	V	
	V_{T1}	−0.3~V_{CC}+0.3	V	1,2
	V_{T2}	−0.3~V_{DP}+0.3	V	1,3
Operating temperature	T_{opr}	−5~+55	℃	
Storage temperature	T_{stg}	−55~+150	℃	

Note 1: Referenced to GND.
Note 2: Applied to pins HSi, ϕ_0, LC, CL_0, SD_0, CS_0~CS_3, CH
Note 3: Applied to pins V_A, V_B, S_0~S_{79}

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4		6	V
Display voltage	V_{DP}	9.6		14.4	V

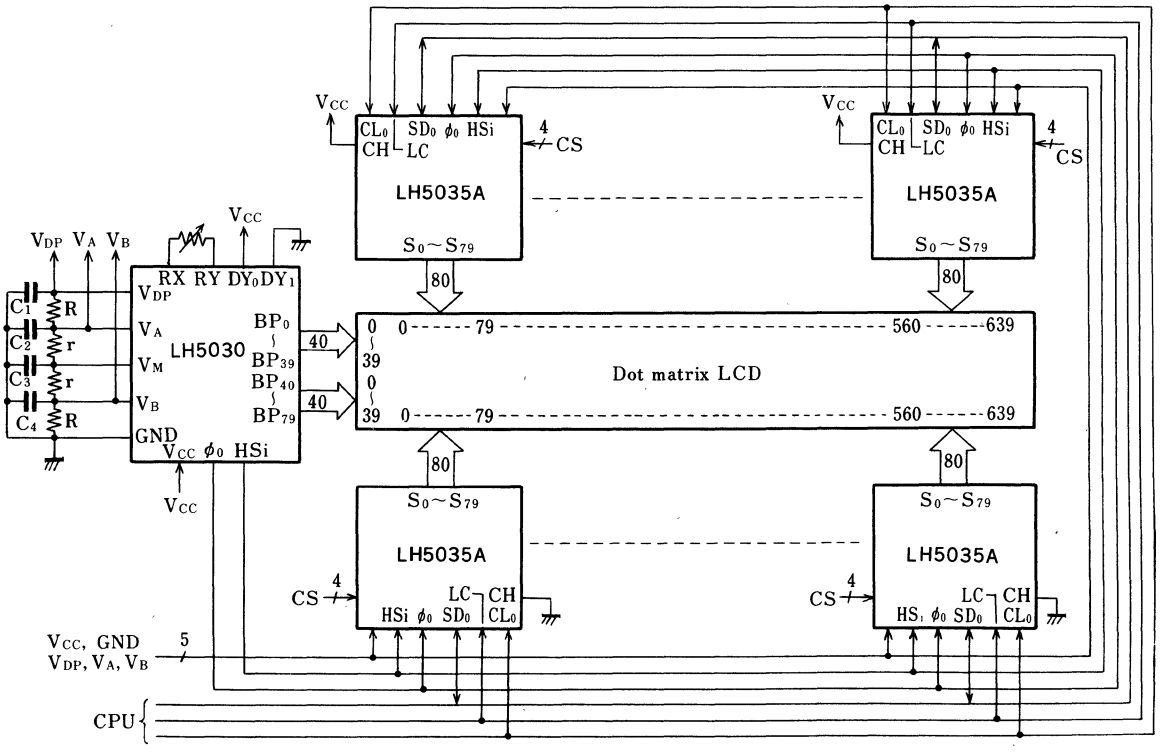
■ DC Characteristics

(V_{CC}=4.0～6.0V, V_{DP}=6.0～15V, Ta=−5～55℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage 1	V_{IH}		2.4		V_{CC}	V	4
	V_{IL}		0		0.8		
Input voltage 2	V_{IH}		3.2		V_{CC}	V	5
	V_{IL}		0		0.8		
Output voltage	V_{OH}	I_{OH}=400 μA	2.4			V	6
	V_{OL}	I_{OL}=1.6mA			0.8		
Output current	I_{OH}	$V_{DP}-V_{OH1}$=1V	100			μA	7
	I_{OL}	V_{OL}=1V	100				
Logic current consumption	I_{CC}	V_{DP}=15V, V_{CC}=6V Durling no-load display f_ϕ=4kHz CL_0=0Hz 1/40 duty		50	300	μA	
Display current consumption	I_{DP}			1	20	μA	
Input current	$\lvert I_{L1} \rvert$	V_{IN}=0V or V_{CC}		0.1	1.0	μA	8
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT}=0V (V_B) or V_{CC} (V_A)		0.1	10	μA	9

Note 4: Applicable to pins LC, CL_0, SD_0, CS_0～CS_3, CH; V_{CC}=4.5～5.5V
Note 5: Applicable to pins ϕ_0, HS_i; V_{CC}=4.5～5.5V
Note 6: Applicable to pins SD_0; V_{CC}=4.5～5.5V
Note 7: Applicable to pins S_0～S_{79}; V_{OH1}, V_{OH1} is light signal output "High", "Low" voltage
Note 8: Applicable to all input pins
Note 9: Applicable to all output pins, ( ) applicable to segment output

■ System Configuration



LH5030 LCD Dot Matrix Common Driver CMOS LSI

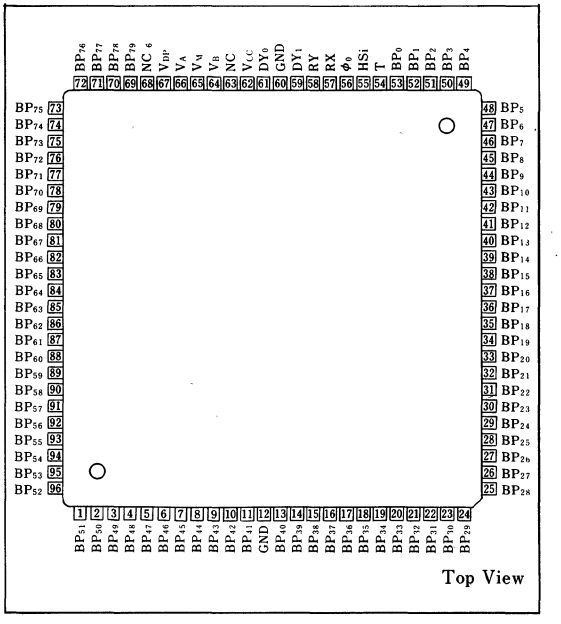
■ Description

The LH5030 is a common driver CMOS LSI for LCD dot matrix graphic display. A built-in CR oscillator generates synchronous signal and clocks necessary for display to send to a segment driver.

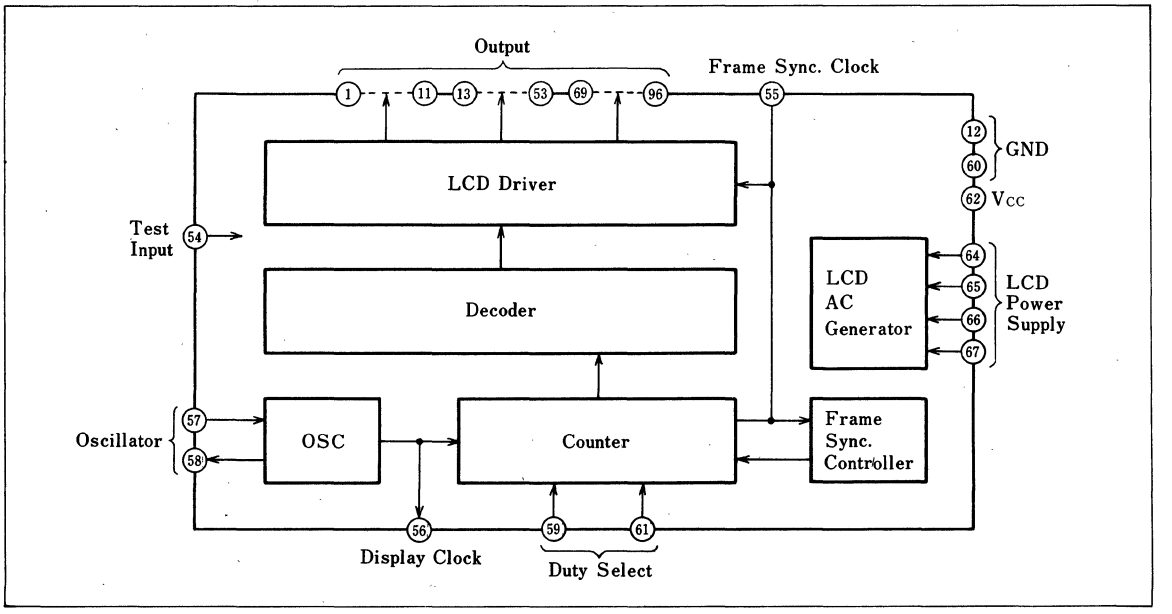
■ Features

1. Common outputs : 80 bits
2. Built-in CR oscillator
3. Selectable duty ratio
   1/32, 1/40, 1/64, 1/80 duty
   (2 pairs of common output, if 1/32, 1/40)
4. Power supply voltage : 5V (TYP.)
5. Display voltage : 15V (MAX.)
6. 96-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{CC}	−0.3～+7.0	V	1
	V_{DP}	−0.3～+16	V	1
	V_{T1}	−0.3～V_{CC}+0.3	V	1,2
	V_{T2}	−0.3～V_{DP}+0.3	V	1,3
Operating temperature	T_{opr}	−5～+55	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note 1: Referenced to GND
Note 2: Applicable to pins HS_i, ϕ_0, RX, RY, DY_0, DY_1
Note 3: Applicable to pins BP_0～BP_{79}, V_A, V_B, V_M

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4		6	V
Display voltage	V_{DP}	6		15	V

■ DC Characteristics

(V_{CC}=5V±1V, V_{DP}=6～15V, Ta=−5～+55℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		2.4		V_{CC}	V	4
	V_{IL}		0		0.8		
Output voltage	V_{OH}	I_{OH}=400 μA	2.4			V	5
	V_{OL}	I_{OL}=1.6mA			0.4		
Output current	I_A	$V_{DP}-V_A$=1V, V_{DP}=6V	10	30		mA	6,8
	I_B	V_B=1V, V_{DP}=6V	10	30			
	I_{OH}	$V_{DP}-V_{OH}$=1V, V_{DP}=6V	1.5	5		mA	7
	I_{OM}	V_M-V_{OM}=1V, V_{DP}=6V	1.5	5			
	I_{OL}	V_{OL}=1V, V_{DP}=6V	1.5	5			
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V or V_{CC}		0.1	1	μA	4
Output leakage current	$\lvert I_{LO} \rvert$	HSi, P_O : V_{OUT}=0V or V_{CC} BP_0～BP_{79} : V_{OUT}=0V or V_{DP}		0.1	1	μA	
Current consumption	I_{CC}	V_{DP}=15V, V_{CC}=6V no load		50	150	μA	
	I_{DP}	Durling no-load display (f_ϕ=8kHz, 1/80 duty)		2	6	μA	9

Note 4: Applicable to pins DY_0, DY_1; V_{CC}=5V±10%
Note 5: Applicable to pins HS_i, ϕ_0; V_{CC}=5V±10%
Note 6: Applicable to pins V_A, V_B
Note 7: Applicable to pins BP_0～BP_{79}
V_{OH} and V_{OL} are the high and low voltage resulting when the scan signal is output to the common pin. When the voltage division resistance R for display equals r. (See System Configuration Example.)
Note 8: This specification prescribes the internal transistor drive force of the LSI. The normal maximum effective current of I_A, I_B is 10 mA.
Note 9: When pins V_A, V_M and V_B are open.

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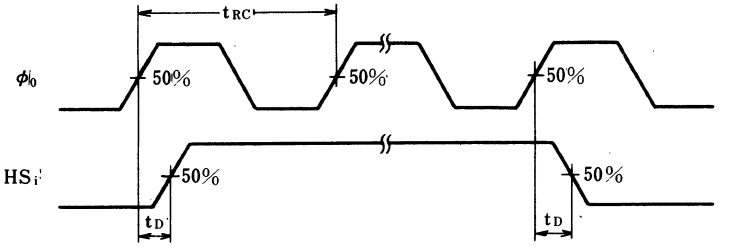
■ AC Characteristics

(V_{CC}=5V±1V, V_{DP}=6~15V, Ta=−5~+55℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Sync. signal delay	t_D	ϕ_0, HSi pin load C_L=15pF	50	100		ns	
Display clock frequency (ϕ_0)	f_ϕ	R_f=R_0±2%, V_{CC}=5V±10%	f_0−30%	f_0	f_0+30%		1,2

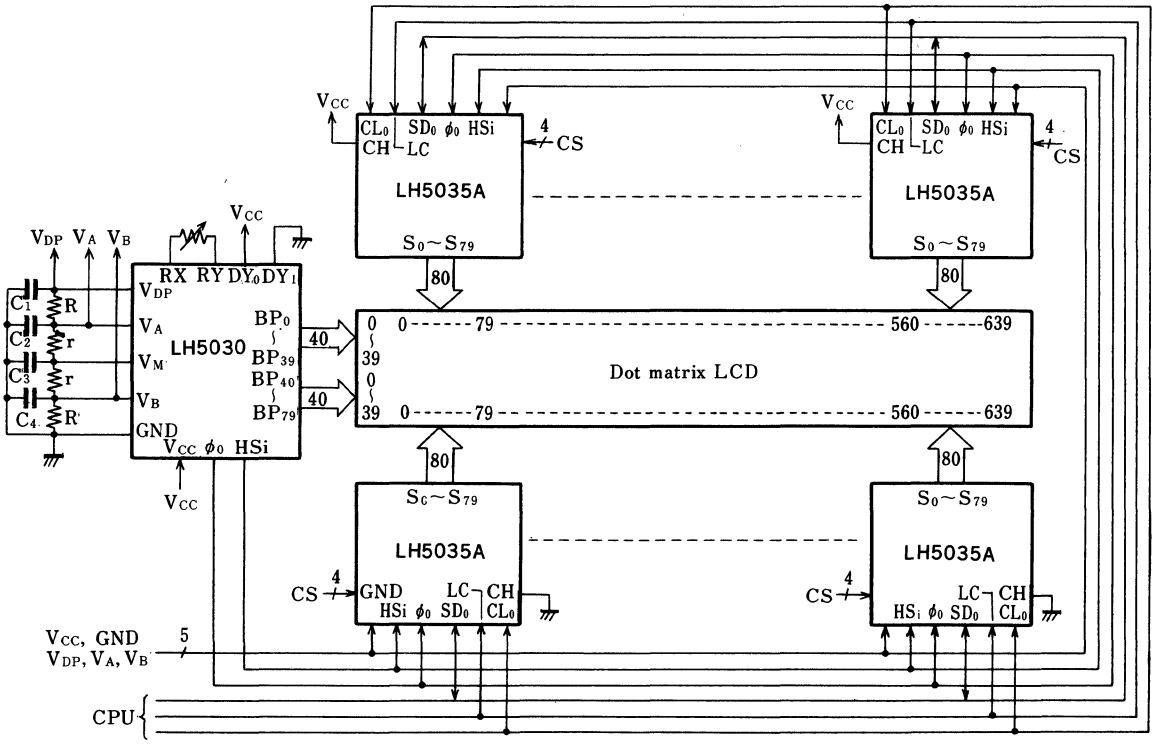
Note 1: When $f_\phi = 1/t_{RC}$, R_0=530kΩ, f_0=3.0kHz
Note 2: When f_0=2.24kHz~8.0kHz (Combination range of R_f resistance)



■ Pin Description

Pin name	No. of pins	I/O	Functions
V_{CC}, GND	3	I	Power supply for logic circuit
V_{DP}, V_A, V_M, V_B	4		Power supply for liquid crystal drive
DY_0, DY_1	2		Duty select input
T	1		Test input
RX	1		Internal clock oscillation pin
RY	1	O	Internal clock oscillation pin
HS_i	1		Frame sync. signal
ϕ_0	1		Display clock
BP_0~BP_{79}	80		Liquid crystal common drive signal

System Configuration



LH5031 LCD Dot Matrix Common Driver CMOS LSI

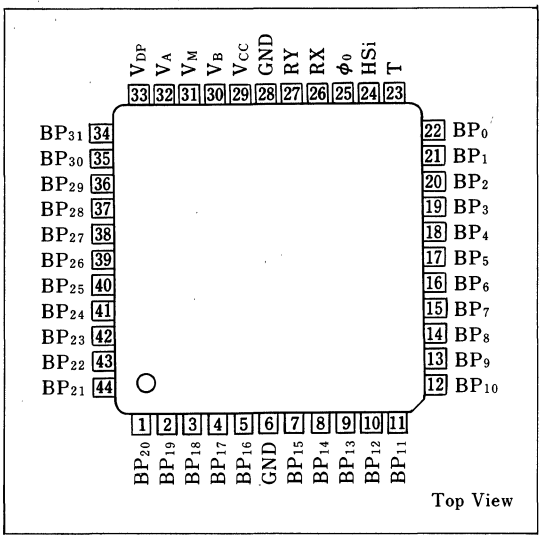
Description

The LH5031 is a common driver CMOS LSI for LCD dot matrix graphic display. A built-in CR oscillator generates synchronous signal and clocks necessary for display to send to a segment driver.

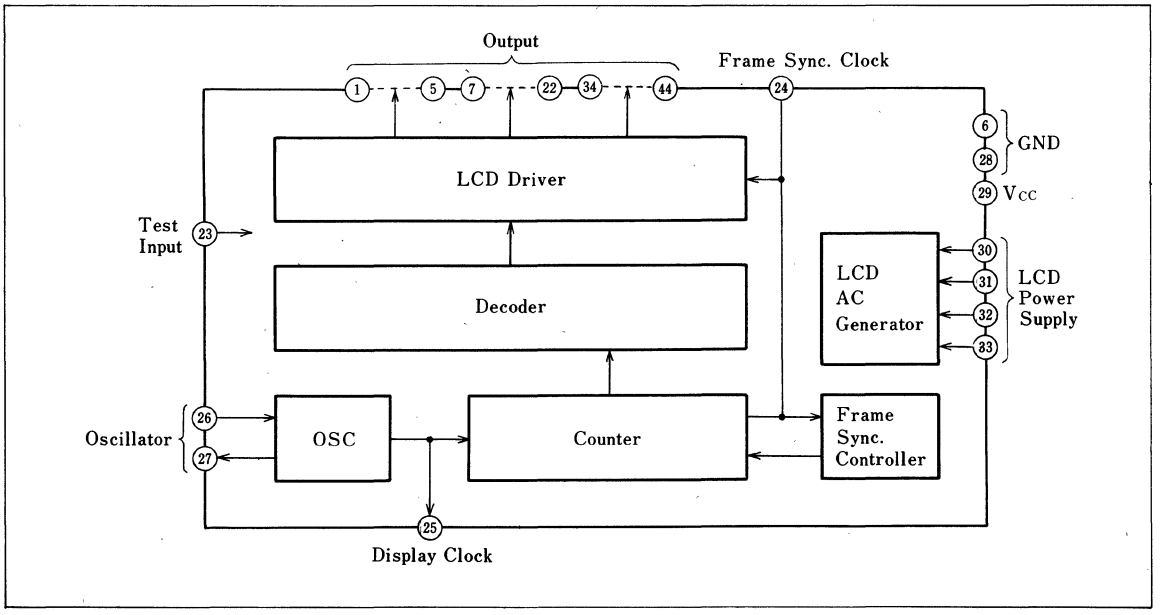
Features

1. Common output : 32 bits
2. Built-in CR oscillator
3. Duty ratio : 1/32 duty
4. Power supply voltage : 5V (TYP.)
5. Display voltage : 15V (MAX.)
6. 44-pin quad-flat package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{CC}	−0.3～+7	V	1
	V_{DP}	−0.3～+16	V	1
	V_{T1}	−0.3～V_{CC}+0.3	V	1,2
	V_{T2}	−0.3～V_{DP}+0.3	V	1,3
Operating temperature	T_{opr}	−5～+55	℃	
Storage temperature	T_{stg}	−55～+150	℃	

Note 1 : Referenced to GND
Note 2 : Applied to pins HS_i, ϕ_0, RX, RY, DY_0, DY_1
Note 3 : Applied to pins BP_0～BP_{79}, V_A, V_B, V_M

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4		6	V
Display voltage	V_{DP}	6		15	V

■ DC Characteristics

(V_{CC}=5V±1V, V_{DP}=6～15V, Ta=−5～+55℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Output voltage	V_{OH}	I_{OH}=400 μA	V_{CC}−0.8			V	4
	V_{OL}	I_{OL}=1.6mA			0.8		
Output current	I_A	$V_{DP}-V_A$=1V	10	30		mA	5
	I_B	V_B=1V	10	30			
	I_{OH}	$V_{DP}-V_{OH}$=1V	1.5	5		mA	6
	I_{OM}	V_M-V_{OM}=1V	1.5	5			
	I_{OL}	V_{OL}=1V	1.5	5			
Output leakage current	I_{LO}	HS_i, ϕ_0 : V_{OUT}=0V or V_{CC} BP_0～BP_{31} : V_{OUT}=0V or V_{DP}		0.1	1	μA	
Current consumption	I_{CC}	V_{DP}=15V, V_{CC}=6V Durling		25	80	μA	
	I_{DP}	no-load display (f_ϕ=3.2kHz)		1	3		

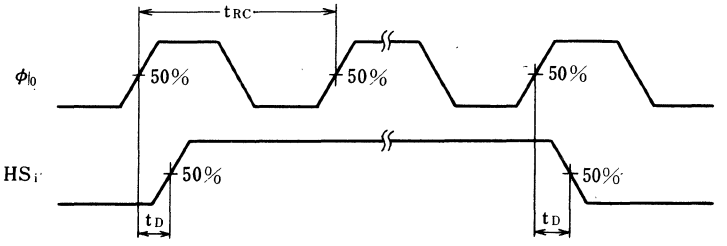
Note 4 : Applicated to pins HSi, ϕ_0; V_{CC}=5V±10%
Note 5 : Applied to pins V_A, V_B
Note 6 : Applied to pins BP_0, BP_{31}
V_{OH} and V_{OL} are the high and low voltages resulting when the scan signal is output to the common pin.

AC Characteristics

(V_{CC}=4~6V, Ta=−5~+55℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Sync. signal delay time	t_D		50			ns	
Display clock frequency (ϕ_0)	f_ϕ	$R_f=R_0\pm5\%$	$f_0-30\%$	f_0	$f_0+30\%$		1,2

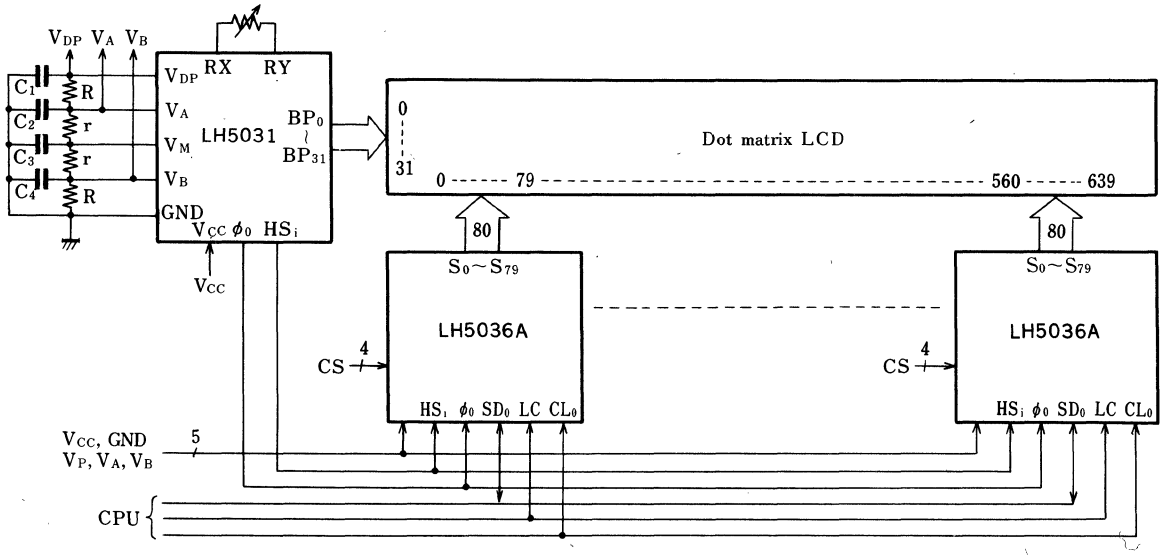
Note 1 : When $f_\phi=1/t_{RC}$, R_0=850kΩ, f_0=2kHz
Note 2 : When f_0=1.12kHz~3.2kHz (Combination range of R_f resistance)



Pin Description

Pin name	No. of pins	I/O	Functions
V_{CC}, GND	3	I	Power supply for logic circuit
V_{DP}, V_A, V_M, V_B	4		Power supply for liquid crystal drive
T	1		Test input
RX	1		Internal clock oscillation pin
RY	1	O	Internal clock oscillation pin
HSi	1		Frame sync. signal
ϕ_0	1		Display clock
BP_0~BP_{31}	32		Liquid crystal common drive signal

System Configuration



LH5003/LH5004 LCD Character Display CMOS LSI

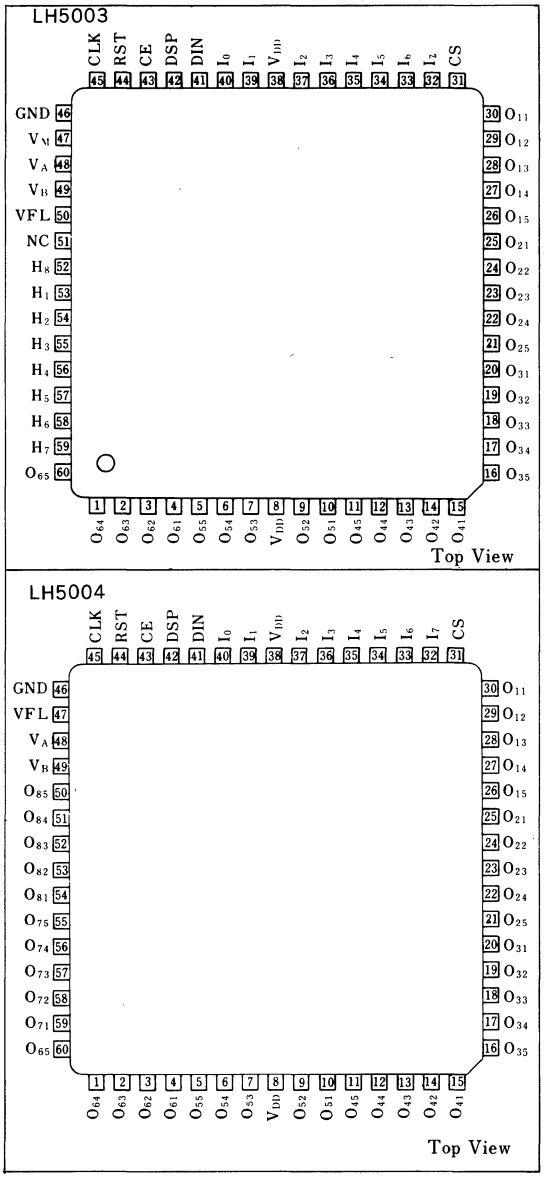
■ Description

The LH5003/LH5004 are dot-matrix LCD controller driver capable of displaying 128 kinds of alphanumeric and symbolic characters. They are the most suitable LSIs for constructing small dot-matrix LCD systems under under the control of 4-bit or 8-bit microcomputer.

■ Features

1. CMOS process
2. 5 × 7 dot-matrix LCD controller/driver
3. Display data RAM
   240 bits (LH5003)
   320 bits (LH5004)
4. Character Generator 128 patterns
5. Driving method duty ··· 1/8 duty
6. Character configuration is 5 × 7 dots plus cursor
   LH5003 (Master) 6 digits
   LH5004 (Slave) 8 digits
7. LCD drive circuit
   LH5003 ; Common signal 8 bits
   Segment signal 40 bits
   LH5004 ; Segment signal 30 bits
8. Single power supply : − 5V (TYP.)
9. 60-pin quad-flat package

■ Pin Connections



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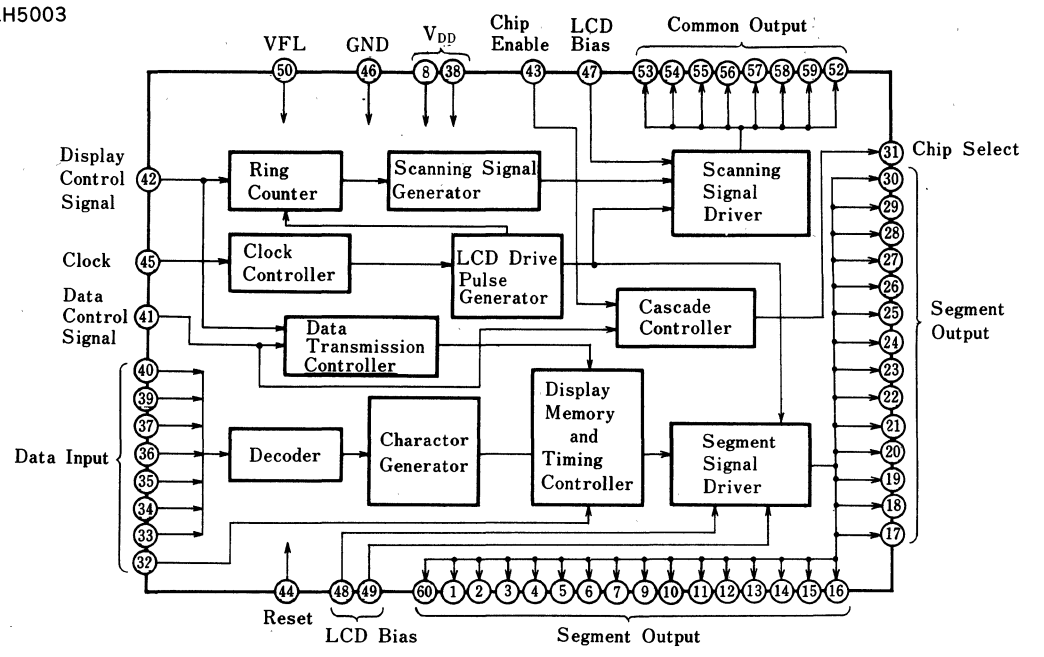
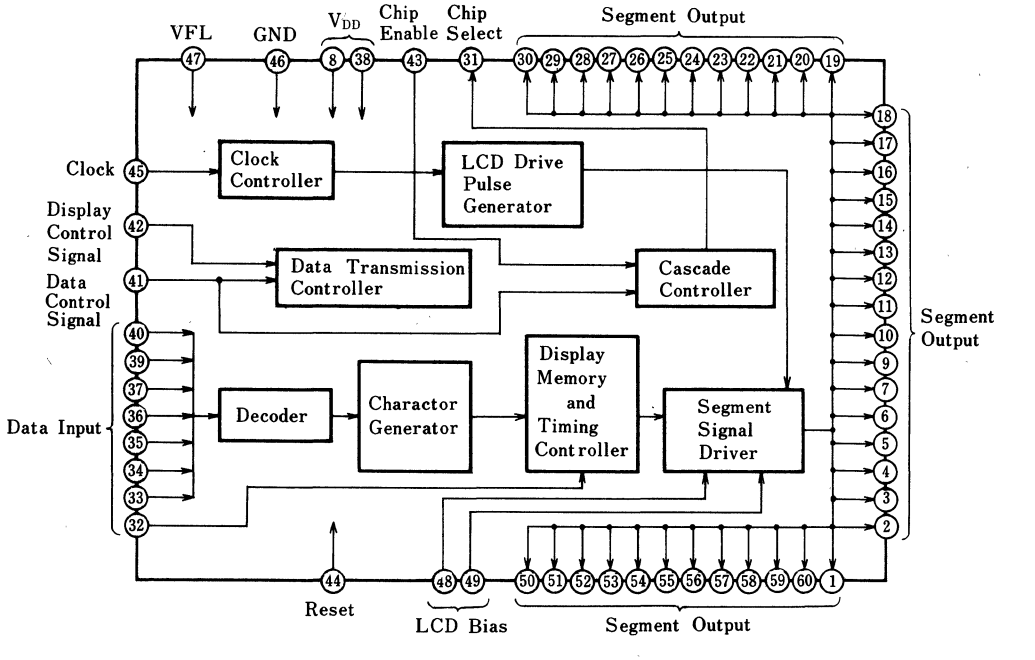
■ Block Diagram

LH5003



LH5004



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage	V_{DD}	−0.3～+8.0	V
	V_{IN}	−0.3～V_{DD}+0.3	V
Operating temperature	T_{opr}	−10～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

■ Recommended Operating Conditions

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	4.2～6.3	V
Oscillator frequency	f_{CLK}	32～320	kHz

■ Electrical Characteristics

(V_{DD}=5V, GND=0V, Ta=−10～+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IL}				1	V	1
	V_{IH}		4				
	V_M			2.5			2
	V_A		3.5	4	5		3
	V_B		0	1	1.5		4
Input current	I_{IL}	V_{IN}=0V			1	μA	1
	I_{IH}	V_{IN}=5V			1		
Output voltage	V_{OL1}	No-load condition		V_B	V_B+0.2	V	5
	V_{OH1}		V_A−0.2	V_A			
	V_{OL1}	$\lvert I_{OL} \rvert$ =50 μA			0.8		6
	V_{OH1}	I_{OH}=50 μA	4.2				
	V_{OL3}	No-load condition		0	0.2		7
	V_{OM}		V_M−0.2	V_M	V_M+0.2		
	V_{OH3}		4.8	5			
Current consumption	I_{D1}	f_{CLK}=32kHz		28	50	μA	8
	I_{D2}	f_{CLK}=64kHz		60	100		
	I_{D3}	f_{CLK}=320kHz		220	400		

Note 1: Applied to pins I_0～I_7, VFL, CLK, RST, CE, DISP, DIN
Note 2: Applied to pin V_M
Note 3: Applied to pin V_A
Note 4: Applied to pin V_B
Note 5: Applied to pins O_{11}～O_{85}
Note 6: Applied to pin CS
Note 7: Applied to pins H_1～H_8
Note 8: Output pin is opened and input pin set to GND level.

■ Functions

Pin description

Pin name	No. of pins	I/O	Connect to	Functions
V_{DD}, GND	3	I	Power supply	Power supply for logic circuit
V_A, V_B, V_M	3			Power supply $V_M=V_{DD}/2$ for liquid $V_A=V_M+\Delta V$ crystal drive $V_B=V_M-\Delta V$ ($\Delta V=1.0\sim V_M$)
$I_0\sim I_7$	8		MPU	Character code input (I_0-I_6) from MPU Cursor display data input (I_7)
DIN	1			High: character data read one character shift in display memory
DSP	1			"High" : Display mode "Low" : Blank mode (reset of cascade control data transfer control circuit)
CLK	1			Clock pulse input
RST	1			"High" : Operation start signal (reset of cascade controller, cascade control data transfer control circuit, ring counter, etc.)
CE	1		Power supply (CS)*	Chip enable pin
CS	1	O	CE	Chip select pin
VFL	1		MPU	LCD frame frequency swithcing signal "High : 1/1024 of clock frequency "Low" : 1/512 of clock frequency
$H_1\sim H_2$	8(0)*		Liquid crystal	LCD common signal drive signal
$O_{11}\sim O_{15}$	30(40)*			LCD segment signal drive signal

*Applied to LH5004

• CLK signal The clock signal is a clock pulse used to operate LH5003 and LH5004 and is continually applied while the power is on. For the CLK signal, apply the clock pulse made in the microcomputer system or a pulse made by dividing this clock pulse and in sync with the microcomputer system.

• DIN signal The DIN signal is used to set the data in the display memories of LH5003 and LH5004. Each time the DIN signal rises, it reads display data corresponding to the character code applied to pins I_0 through I_7 into the display memory and shifts the existing contents of the display memory one character. Set the pulse width of the DIN signal to at least two cycles of the clock pulse (a pulse width of $2T_{CK}$ or greater when the clock pulse period is T_{CK}.)

• DSP signal The DSP signal determines the display condition. When it is high, the display mode is set and when it is low, the blank mode is set and the cascade controller and data transfer control circuit are reset. Normally, the DSP signal is made high after setting the data in the display memories of the LH5003 and LH5004.

• RST signal The RST signal is used to initialize the internal control circuits of the LH5003 and LH5004 by applying the pulse of the RST signal to this pin immediately after the power is turned on. Synchronize the fall of the RST pulse with the rise of the clock pulse, and set the pulse width of the RST pulse to at least four times that of the normal clock pulse width ($4T_{CK}$.)

• I_0-I_7 signal The I_0-I_7 signal is an 8-bit parallel signal that determines the characters and symbols to be displayed. Select the desired characters using the data of pins I_0-I_6 (see the table relating input codes with displayed characters and symbols). When the I_7 signal is high, the cursor is displayed, and when it is low, the cursor is displayed, and when it is low, the cursor is blanked out. LH5003 and LH5004 are controlled from the microcomputer system by the following procedure.

(1) The clock pulse is applied continually to the CLK pin during the period from immediately after the power is turned on until it is turned off.

(2) Immediately after the power is turned on, the RST pulse is applied to the RST pin.

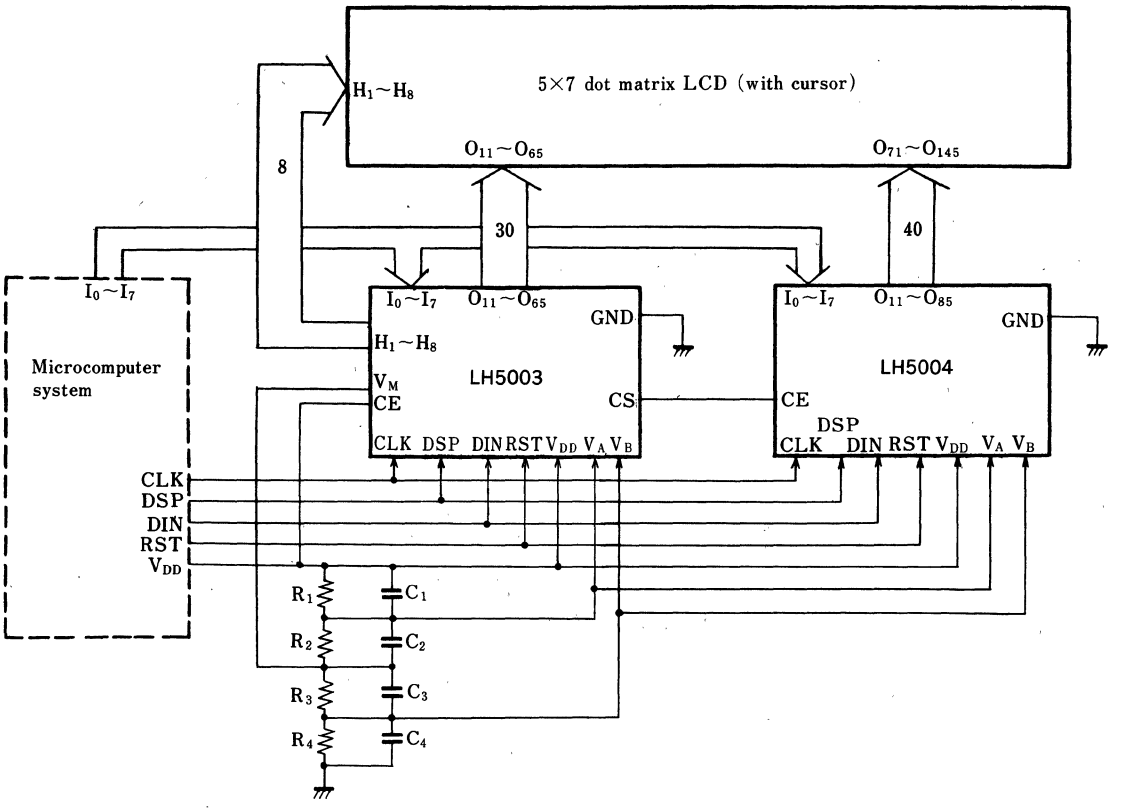
(3) The DSP and DIN pins are made low. (Not necessary if they are already low.)
(4) The character code of the character to be displayed is output to pins I_0-I_7.
(5) The DIN pin becomes high level and then low level again. (Apply one pulse to the DIN pin.)
(6) Steps 4 and 5 are repeated for each display position.
(7) The DSP pin is made high level. (This condition sets the display mode.)
(8) The contents of the display are changed by repeating steps 3 through 7.

■ Input Codes and Displayed Characters and Symbols

(LH5003/LH5004)

Data I_3~I_0 \ Data I_6~I_4	0	1	2	3	4	5	6	7
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								
A								
B								
C								
D								
E								
F								

System Configuration



LH1001 VFD Grid Driver PMOS LSI

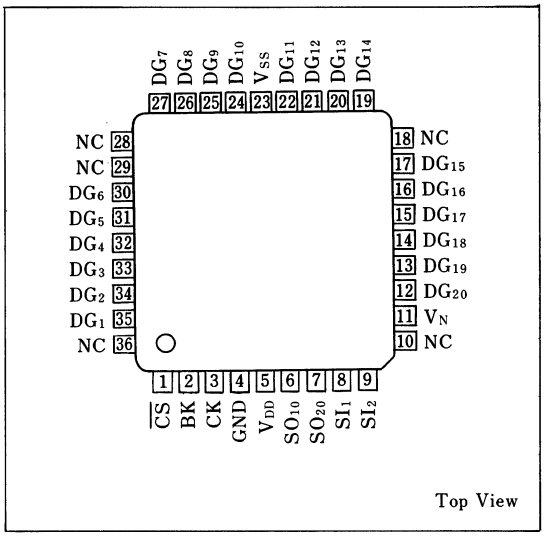
■ Description

The LH1001 is a VFD (Vacuum Fluorescent Display) grid driver with an internal 20-bit serial shift register. Can be easily cascaded to extend the display.

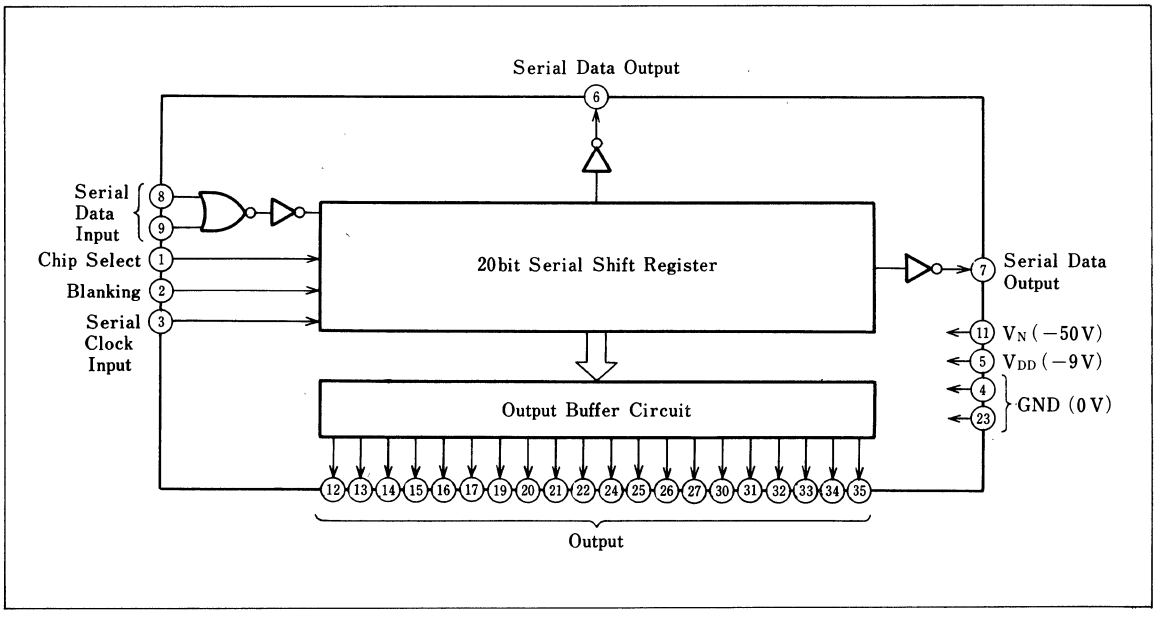
■ Features

1. Included 20-bit shift registers in a serial input
2. Data controlled by shift clock and chip select
3. Blanking input controlled by duty cycle
4. High output voltage : − 50V (MAX.)
5. High output current : 20mA (MAX.)
6. Built-in output load resistor
7. 36-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*	V_{DD}	−20～+0.3	V
	V_N	−55～+0.3	
	V_{IN}	−55～+0.3	
V_{SS} allowable current	I_{SS}	70	mA
Operating temperature	T_{opr}	−5～+55	℃
Storage temperature	T_{stg}	−55～+150	℃

* Referenced to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	−9.9		−8.1	V
Display voltage	V_N		−40		V

■ DC Characteristics

(V_{DD}=−9V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−1.1			V	
	V_{IL}				−4.2		
Output voltage	V_{OH}	I_{OH}=20mA	−1			V	1
	V_{OL}	V_N=−50V			−48		
Output current	I_{OH}	V_{OH}=−1.1V	50			μA	2
	I_{OL}	V_{OL}=−4.2V	3				
Current consumption	I_{DD}	V_{DD}=−9V		1.5	3	mA	
	I_N	V_N=−50V		4.0	8		

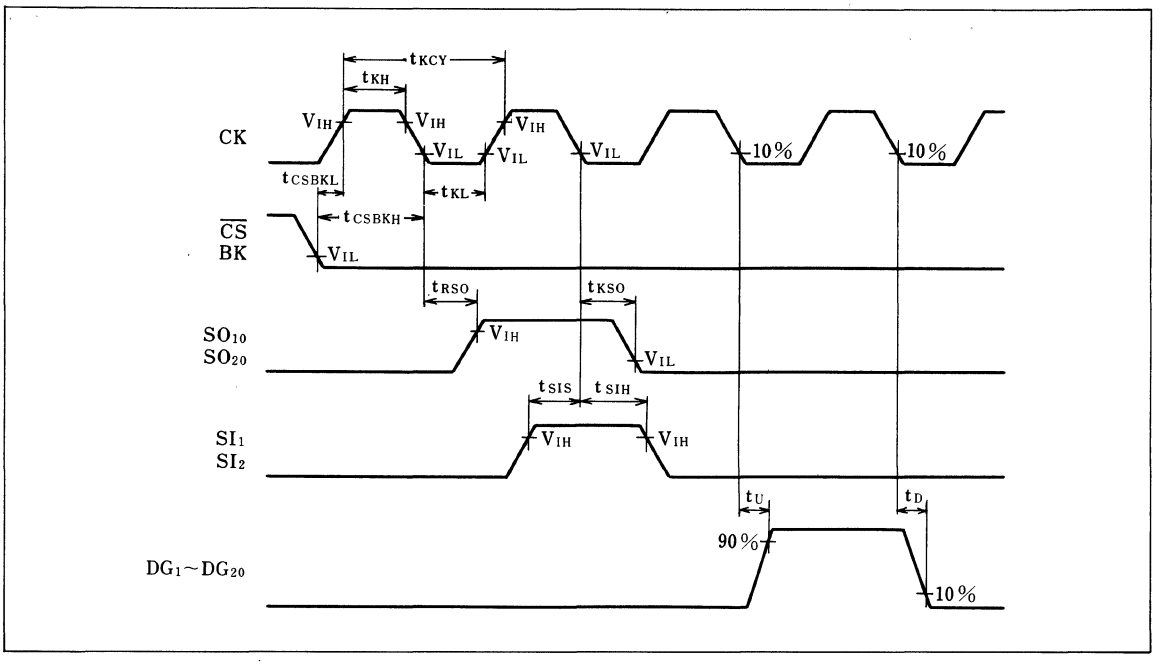
Note 1: Applied to pins DG_1～DG_{20}
Note 2: Applied to pins SO_{10}, SO_{20}

■ AC Characteristics

(V_{DD}=−9V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CK frequency	t_{CK}				40	kHz
CK cycle time	t_{KSY}		25			μs
CK high-level width	t_{KH}		12			μs
CK low-level width	t_{KL}		12			μs
SI setup time	t_{SIS}		6			μs
SI hold time	t_{SIH}		6			μs
CK high active time	t_{CSBKL}		0			μs
CK low active time	t_{CSBKH}		6			μs
CK ↓→SO delay time	t_{KSO}	C_L=10pF			20	μs
Output delay time	t_U	V_N=−50V, C_L=100pF		3	5	μs
	t_D			15	20	

■ AC Timing Diagram

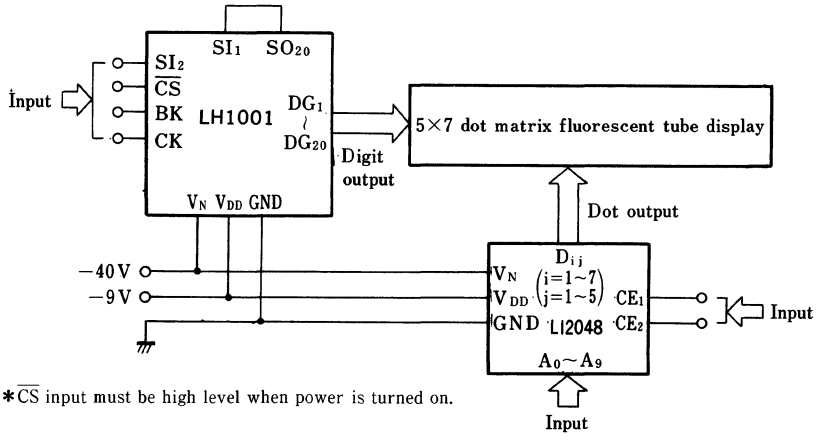


■ Pin Description

Pin name	No. of pins	I/O	Functions
V_{DD}, GND	3	I	Power supply for logic circuit
V_N	1		Power supply for display
$\overline{CS}$	1		Chip select ... select condition when $\overline{CS}$="Low"
BK	1		Blanking ..... blanking when BK="High"
CK	1		Serial clock
SI_1, SI_2	2		Serial data input
SO_{10}, SO_{20}	2	O	Serial data output
DG_1~DG_{20}	20		Digit output for fluorescent display tube

1="High" level, 0="Low" level

■ System Configuration



*$\overline{CS}$ input must be high level when power is turned on.

LH5010/LH5011 CMOS Driver

■ Description

The LH5010/LH5011 are 6-circuit CMOS drivers with 2-common INHIBIT inputs (A_{IN}, $\overline{B_{IN}}$). The LH5010 is a non-inverting type and the LH5011 is an inverting type.

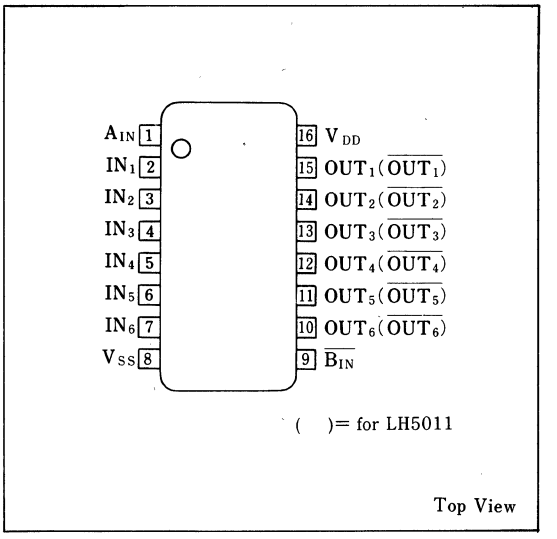
The outputs have an open drain construction fabricated using a P-channel MOS FET.

They are used as drivers for VFD and interfaces between CMOS LSI and high-voltage MOS LSI.

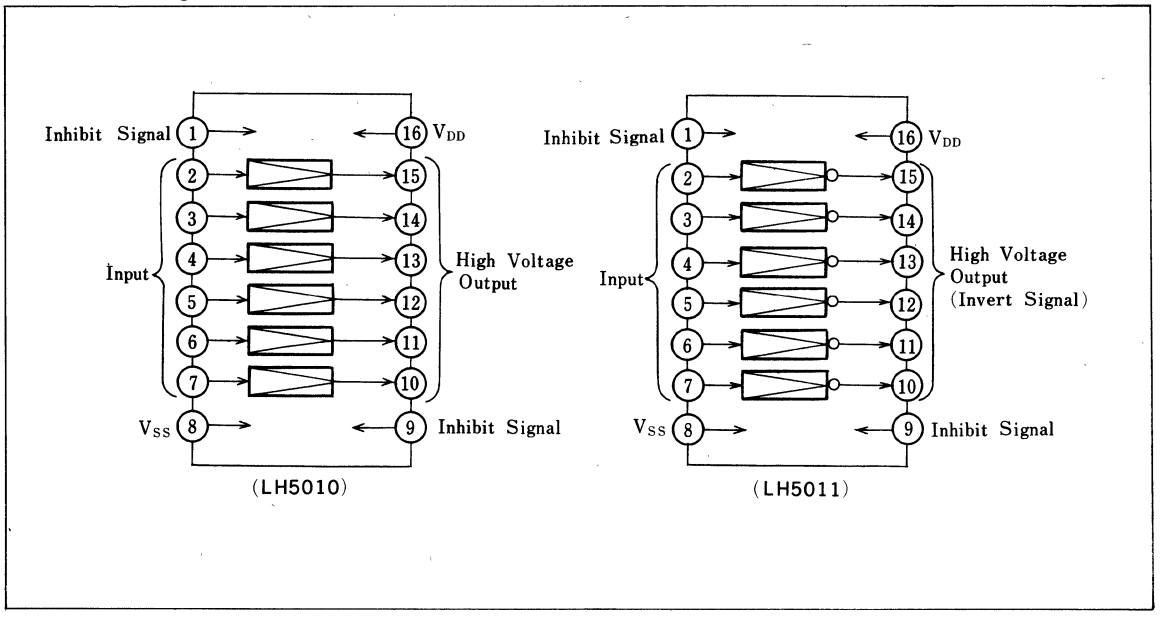
■ Features

1. CMOS process
2. 6 independent driver circuits
3. INHIBIT input port
4. Non-inverting type····· LH5010
   Inverting type ····· LH5011
5. 16-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output voltage	V_{OUT}	$V_{DD}-50 \sim V_{DD}+0.5$	V
Operating temperature	T_{opr}	$-40 \sim +85$	℃
Storage temperature	T_{stg}	$-55 \sim +125$	℃

■ Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3		18	V
Input voltage	V_{IN}	0		V_{DD}	V

■ Electrical Characteristics

Parameter	Symbol	Conditions	V_{DD} (V)	−40℃ MIN.	−40℃ MAX.	25℃ MIN.	25℃ TYP.	25℃ MAX.	80℃ MIN.	80℃ MAX.	Unit	Note
Output high voltage	V_{OH}	$\lvert I_{OUT} \rvert \leqq 1\ \mu A$ $V_{IN}=V_{SS}$ or V_{DD}	5	4.95		4.95	5.00		4.95		V	1
			10	9.95		9.95	10.00		9.95			
			15	14.95		14.95	15.00		14.95			
Output high current	I_{OH}	$V_{OH}=3V(V_{DD}-2V)$	5	−6		−5	−9		−4		mA	1
		$V_{OH}=2V(V_{DD}-3V)$	5	−9		−8	−11		−6			
		$V_{OH}=7V(V_{DD}-3V)$	10	−12		−10	−28		−8			
		$V_{OH}=12V(V_{DD}-3V)$	15	−17		−15	−39		−12			
Input voltage	V_{IH}	$V_{OUT}=0.5V, 4.5V$	5	3.5		3.5	2.75		3.5		V	2
		$V_{OUT}=1.0V, 9.0V$	10	7.0		7.0	5.5		7.0			
		$V_{OUT}=1.5V, 13.5V$	15	11.0		11.0	8.25		11.5			
	V_{IL}	$V_{OUT}=0.5V, 4.5V$	5		1.5		2.25	1.5		1.5	V	2
		$V_{OUT}=1.0V, 9.0V$	10		3.0		4.5	3.0		3.0		
		$V_{OUT}=1.5V, 13.5V$	15		4.0		6.75	4.0		4.0		
Input current	I_{IH}	$V_{IH}=18V$	18		0.3		10^{-5}	0.3		1.0	μA	3
	I_{IL}	$V_{IL}=0V$	18		−0.3		-10^{-5}	−0.3		−1.0		
Output leak-off current	I_{OFF}	$V_{OUT}=0V$	15		3			3		10	μA	1
		$V_{OUT}=V_{DD}-45V$	15		10			10		20		
Static current consumption	I_{DD}	$V_{IN}=V_{DD}, V_{SS}$ output open	5		4.0			4.0		30	μA	4
			10		8.0			8.0		60		
			15		16.0			16.0		120		

Note 1: Applicable pins $OUT_1 \sim OUT_6$
Note 2: $R_L=20k\Omega$, Applicable pins $IN_1 \sim IN_6$. AIN $\overline{B_{IN}}$
Note 3: Applicable pins $IN_1 \sim IN_6$ A_{IN}, B_{IN}
Note 4: No load condition

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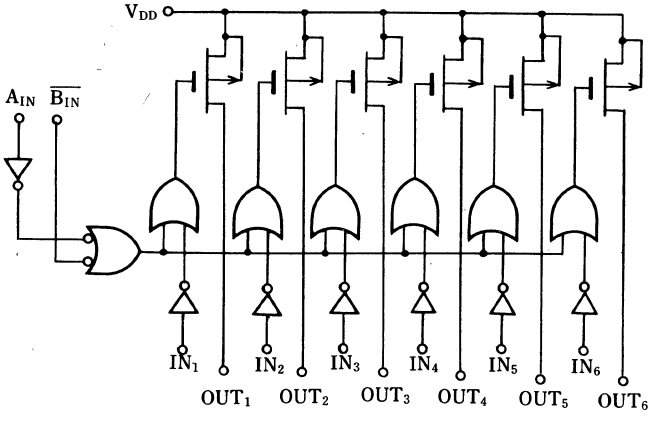
■ Truth Table

Input			Output	
A_{IN}	$\overline{B_{IN}}$	IN	LH5010	LH5011
L	H	L	HZ	High
L	H	H	High	HZ
*	L	*	HZ	HZ
H	*	*	HZ	HZ

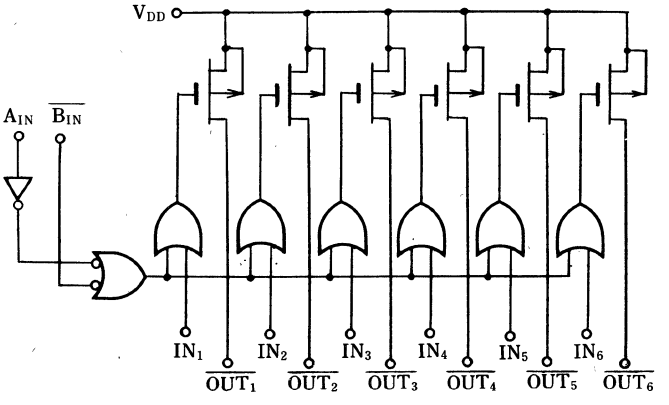
HZ : High impedance
* : Don't care

■ Logic Diagram

• **LH5010**



• **LH5011**



LH5010D/LH5011D CMOS Driver

■ Description

The LH5010D/LH5011D are 7-circuit CMOS drivers with 2 common INHIBIT inputs (A_{IN}, $\overline{B_{IN}}$). The LH5010D is a non-inverting type and the LH5011D is an inverting type.

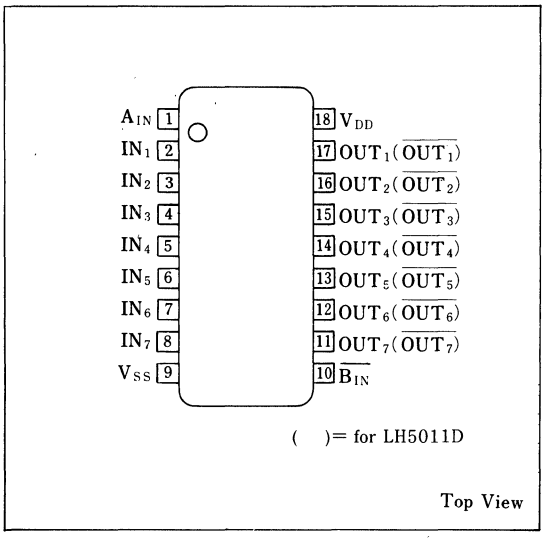
The outputs have an open drain construction fabricated using a P-channel MOS FET.

They are used as drivers for VFD and interfaces between CMOS LSI and high-voltage MOS LSI.

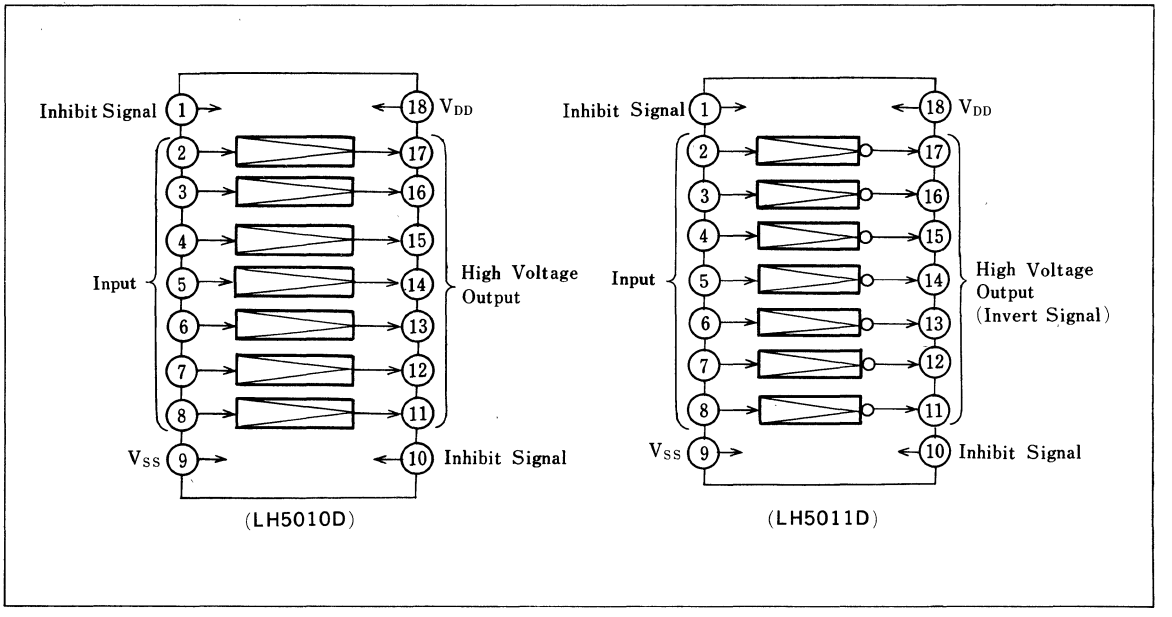
■ Features

1. CMOS process
2. 7-independent driver circuits
3. INHIBIT input port
4. Non-inverting type ····· LH5010D
   Inverting type ····· LH5011D
5. 18-pin dual-in-line package

■ Pin Connections



■ Block Diagram



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■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output voltage	V_{OUT}	$V_{DD}-50 \sim V_{DD}+0.5$	V
Operating temperature	T_{opr}	$-40 \sim +85$	℃
Storage temperature	T_{stg}	$-55 \sim +125$	℃

■ Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3		18	V
Input voltage	V_{IN}	0		V_{DD}	V

■ Electrical Characteristics

Parameter	Symbol	Conditions	V_{DD} (V)	−40℃ MIN.	−40℃ MAX.	25℃ MIN.	25℃ TYP.	25℃ MAX.	80℃ MIN.	80℃ MAX.	Unit	Note
Output high voltage	V_{OH}	$\lvert I_{OUT} \rvert \leqq 1\ \mu A$	5	4.95		4.95	5.00		4.95		V	1
			10	9.95		9.95	10.00		9.95			
			15	14.95		14.95	15.00		14.95			
Output high current	I_{OH}	$V_{OH}=3V(V_{DD}-2V)$	5	−6		−5	−9		−4		mA	1
		$V_{OH}=2V(V_{DD}-3V)$	5	−9		−8	−11		−6			
		$V_{OH}=7V(V_{DD}-3V)$	10	−12		−10	−28		−8			
		$V_{OH}=12V(V_{DD}-3V)$	15	−17		−15	−39		−12			
Input voltage	V_{IN}	$V_{OUT}=0.5V, 4.5V$	5	3.5		3.5	2.75		3.5		V	2
		$V_{OUT}=1.0V, 9.0V$	10	7.0		7.0	5.5		7.0			
		$V_{OUT}=1.5V, 13.5V$	15	11.0		11.0	8.25		11.5			
	V_{IL}	$V_{OUT}=0.5V, 4.5V$	5		1.5		2.25	1.5		1.5	V	2
		$V_{OUT}=1.0V, 9.0V$	10		3.0		4.5	3.0		3.0		
		$V_{OUT}=1.5V, 13.5V$	15		4.0		6.75	4.0		4.0		
Input current	I_{IH}	$V_{IH}=18V$	18		0.3		10^{-5}	0.3		1.0	μA	3
	I_{IL}	$V_{IL}=0V$	18		−0.3		-10^{-5}	−0.3		−1.0		
Output leak-off current	I_{OFF}	$V_{OUT}=0V$	15		3			3		10	μA	1
		$V_{OUT}=V_{DD}-45V$	15		10			10		20		
Static current consumption	I_{DD}	$V_{IN}=V_{DD}, V_{SS}$ output open	5		4.0			4.0		30	μA	4
			10		8.0			8.0		60		
			15		16.0			16.0		120		

Note 1: Applicable pins $OUT_1 \sim OUT_7$, $V_{IN}=V_{SS}$ or V_{DD}
Note 2: $R_L=20k\Omega$, Applicable pins $IN_1 \sim IN_7$, A_{IN}, B_{IN}
Note 3: Applicable pins $IN_1 \sim IN_7$, A_{IN}, B_{IN}
Note 4: No load condition

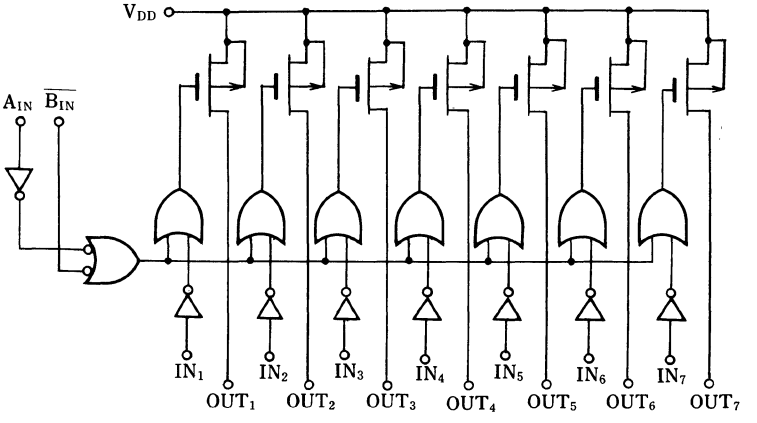
■ Truth Table

Input			Output	
A_{IN}	$\overline{B_{IN}}$	IN	LH5010D	LH5011D
L	H	L	HZ	High
L	H	H	High	HZ
*	L	*	HZ	HZ
H	*	*	HZ	HZ

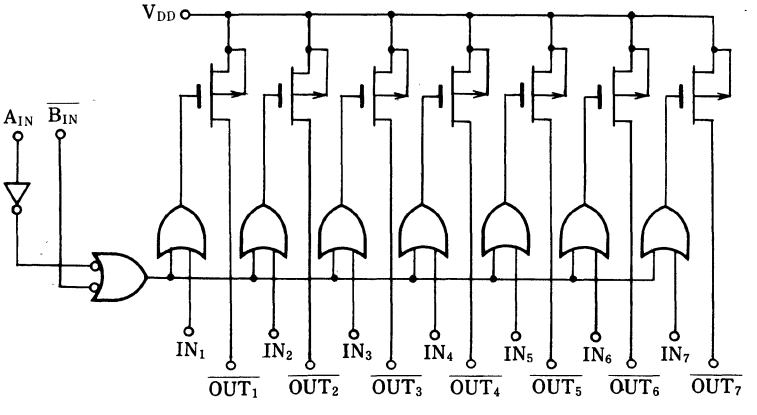
HZ : High impedance
* : Don't care

■ Logic Diagram

• LH5010D



• LH5011D



LH5012/LH5013 CMOS Driver

■ Description

The LH5012/LH5013 are 7-circuit CMOS drivers. The LH5012 is a non-inverting type and the LH5013 is an inverting type.

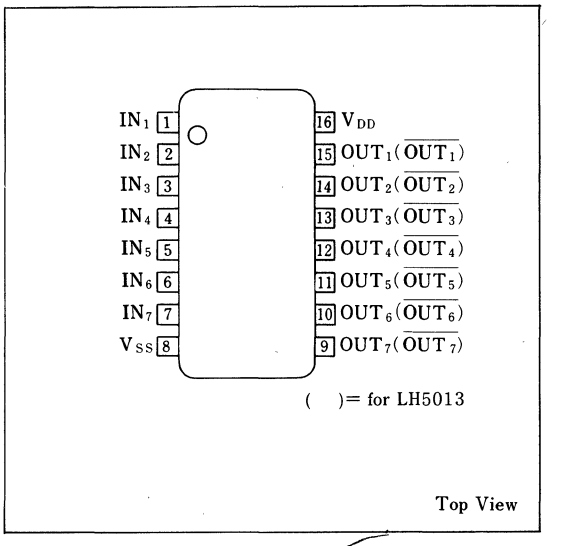
The outputs have an open drain construction fabricated using a P-channel MOS FET.

They are used as drivers for VFD and interfaces between CMOS LSI and high-voltage MOS LSI.

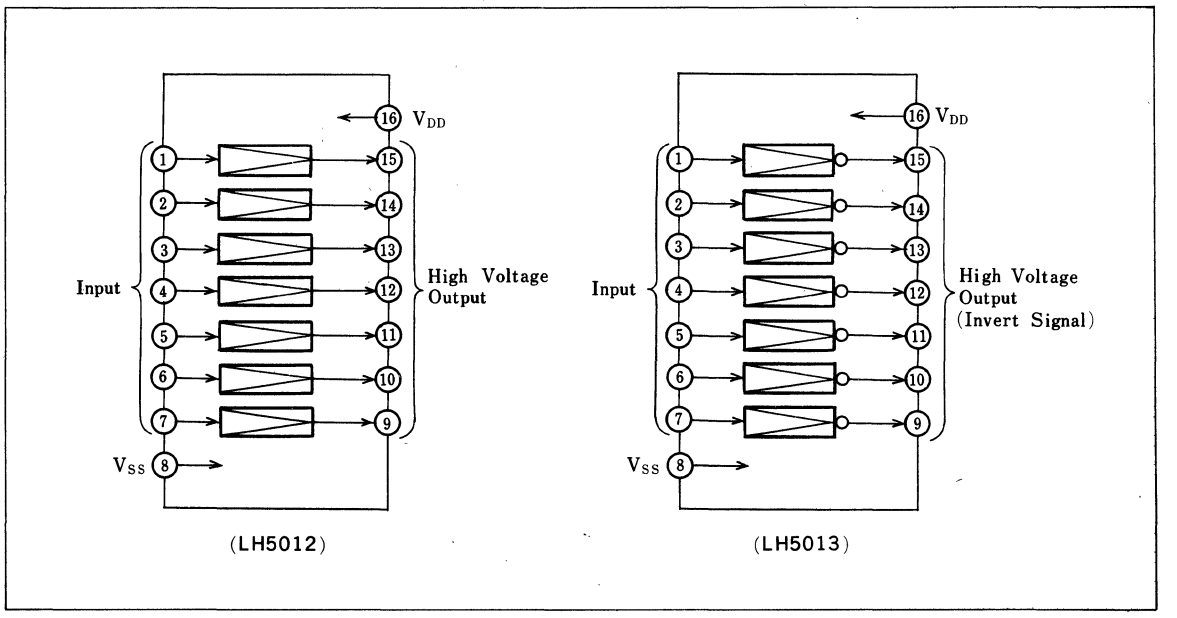
■ Features

1. CMOS process
2. 7 independent driver circuits
3. Non-inverting type ····· LH5012
   Inverting type ····· LH5013
4. 16-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output voltage	V_{OUT}	$V_{DD}-50 \sim V_{DD}+0.5$	V
Operating temperature	T_{opr}	$-40 \sim +85$	°C
Storage temperature	T_{stg}	$-55 \sim +125$	°C

■ Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3		18	V
Input voltage	V_{IN}	0		V_{DD}	V

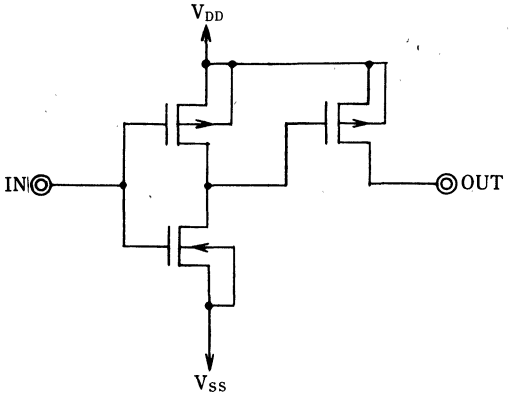
■ Electrical Characteristics

Parameter	Symbol	Conditions	V_{DD} (V)	−40℃ MIN.	−40℃ MAX.	25℃ MIN.	25℃ TYP.	25℃ MAX.	80℃ MIN.	80℃ MAX.	Unit	Note
Output high voltage	V_{OH}	$I_{OUT} \leqq 1\ \mu A$	5	4.95		4.95	5.00		4.95		V	1
			10	9.95		9.95	10.00		9.95			
			15	14.95		14.95	15.00		14.95			
Output high current	I_{OH}	$V_{OH}=3V(V_{DD}-2V)$	5	−6		−5	−9		−4		mA	1
		$V_{OH}=2V(V_{DD}-3V)$	5	−9		−8	−11		−6			
		$V_{OH}=7V(V_{DD}-3V)$	10	−12		−10	−28		−8			
		$V_{OH}=12V(V_{DD}-3V)$	15	−17		−15	−39		−12			
Input voltage (LH5012)	V_{IH}	$V_{OUT}=4.5V$	5	3.0		3.0			3.0		V	2
		$V_{OUT}=9.0V$	10	8.0		8.0			8.0			
		$V_{OUT}=13.5V$	15	12.5		12.5			12.5			
	V_{IL}	$V_{OUT}=0.5V$	5		1.0			1.0			V	2
		$V_{OUT}=1.0V$	10		2.0			2.0				
		$V_{OUT}=1.5V$	15		2.5			2.5				
Input voltage (LH5013)	V_{IH}	$V_{OUT}=0.5V$	5	3.5		3.5	2.75		3.5		V	2
		$V_{OUT}=1.0V$	10	7.0		7.0	5.5		7.0			
		$V_{OUT}=1.5V$	15	11.0		11.0	8.25		11.0			
	V_{IL}	$V_{OUT}=4.5V$	5		1.5		2.25	1.5		1.5	V	2
		$V_{OUT}=9.0V$	10		3.0		4.5	3.0		3.0		
		$V_{OUT}=13.5V$	15		4.0		6.75	4.0		4.0		
Input current	I_{IH}	$V_{IH}=18V$	18		0.3		10^{-5}	0.3		1.0	μA	3
	I_{IL}	$V_{IL}=0V$	18		−0.3		-10^{-5}	−0.3		−1.0		
Output leak-off current	I_{OFF}	$V_{OUT}=0V$	15		3			3		10	μA	1
		$V_{OUT}=V_{DD}-30V$	15		10			10		20		
Static current consumption	I_{DD}	$V_{IN}=V_{DD}$, V_{SS} output open	5		4.0			4.0		30	μA	4
			10		8.0			8.0		60		
			15		16.0			16.0		120		

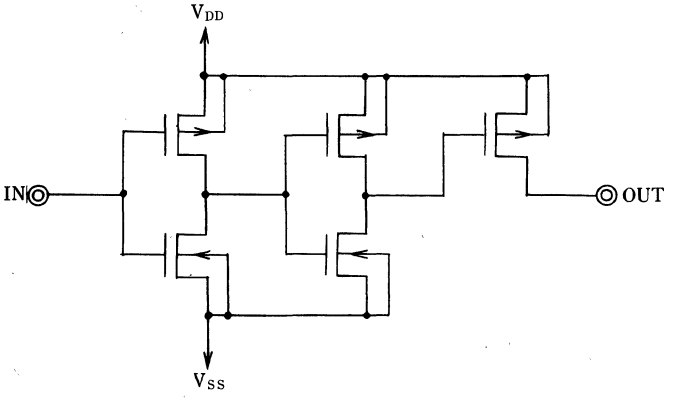
Note 1: Applicable pins $OUT_1 \sim OUT_7$, $V_{IN}=V_{SS}$ or V_{DD}
Note 2: $R_L=20k\Omega$, $I_{OUT} \leqq 1\ \mu A$, Applicable pins $IN_1 \sim IN_7$
Note 3: Applicable pins $IN_1 \sim IN_7$
Note 4: No load condition

■ Logic Diagram (1 circuit)

- LH5012



- LH5013



LH5012D/LH5013D CMOS Driver

■ Description

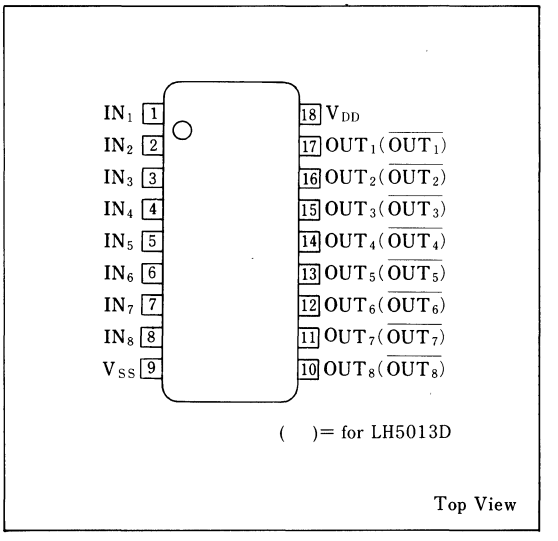
The LH5012D/LH5013D are 8-circuit CMOS drivers. The LH5012D is a non-inverting type and the LH5013D is an inverting type.

The outputs have an open drain construction fabricated using a P-channel MOS FET. They are used as drivers for VFD and interfaces between CMOS LSI and high-voltage MOS LSI.

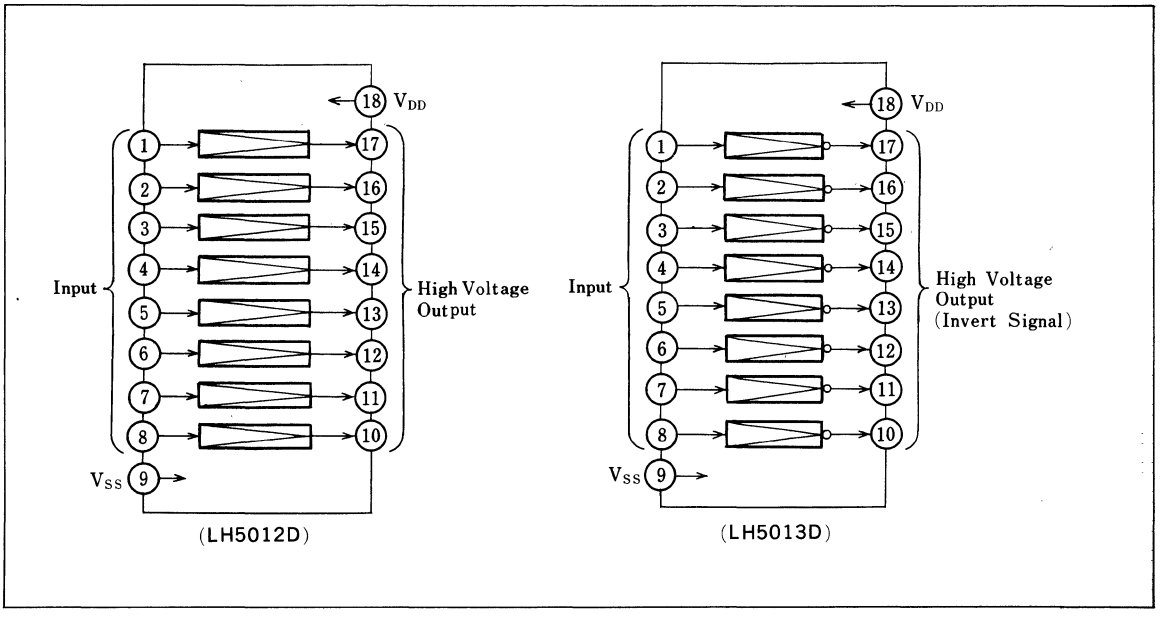
■ Features

1. CMOS process
2. 8 independent driver circuits
3. Non-inverting type ····· LH5012D
   Inverting type ····· LH5013D
4. 18-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output voltage	V_{OUT}	$V_{DD}-50 \sim V_{DD}+0.5$	V
Operating temperature	T_{opr}	$-40 \sim +85$	°C
Storage temperature	T_{stg}	$-55 \sim +125$	°C

■ Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3		18	V
Input voltage	V_{IN}	0		V_{DD}	V

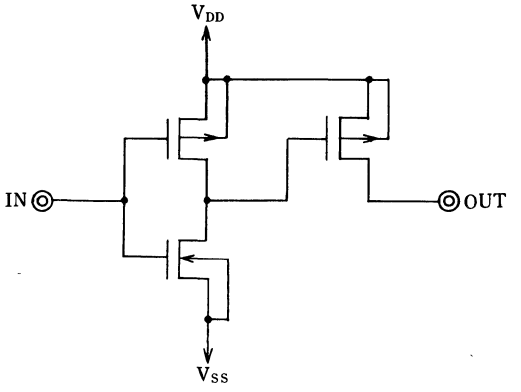
■ Electrical Characteristics

Parameter	Symbol	Conditions	V_{DD} (V)	−40℃ MIN.	−40℃ MAX.	25℃ MIN.	25℃ TYP.	25℃ MAX.	80℃ MIN.	80℃ MAX.	Unit	Note
Output high voltage	V_{OH}	$\lvert I_{OUT} \rvert \leqq 1\ \mu A$	5	4.95		4.95	5.00		4.95		V	1
			10	9.95		9.95	10.00		9.95			
			15	14.95		14.95	15.00		14.95			
Output low current	I_{OH}	$V_{OH}=3V(V_{DD}-2V)$	5	−6		−5	−9		−4		mA	1
		$V_{OH}=2V(V_{DD}-3V)$	5	−9		−8	−11		−6			
		$V_{OH}=7V(V_{DD}-3V)$	10	−12		−10	−28		−8			
		$V_{OH}=12V(V_{DD}-3V)$	15	−17		−15	−39		−12			
Input voltage (LH5012D)	V_{IH}	$V_{OUT}=4.5V$	5	3.0		3.0			3.0		V	2
		$V_{OUT}=9.0V$	10	8.0		8.0			8.0			
		$V_{OUT}=13.5V$	15	12.5		12.5			12.5			
	V_{IL}	$V_{OUT}=0.5V$	5		1.0			1.0			V	2
		$V_{OUT}=1.0V$	10		2.0			2.0				
		$V_{OUT}=1.5V$	15		2.5			2.5				
Input voltage (LH5013D)	V_{IH}	$V_{IH}=0.5V$	5	3.5		3.5	2.75		3.5		V	2
		$V_{OUT}=1.0V$	10	7.0		7.0	5.5		7.0			
		$V_{IL}=1.5V$	15	11.0		11.0	8.25		11.0			
	V_{IL}	$V_{OUT}=4.5V$	5		1.5		2.25	1.5		1.5	V	2
		$V_{OUT}=9.0V$	10		3.0		4.5	3.0		3.0		
		$V_{OUT}=13.5V$	15		4.0		6.75	4.0		4.0		
Input current	I_{IH}	$V_{IH}=18V$	18		0.3		10^{-5}	0.3		1.0	μA	3
	I_{IL}	$V_{IL}=0V$	18		−0.3		-10^{-5}	−0.3		−1.0		
Output leak-off current	I_{OFF}	$V_{OUT}=0V$	15		3			3		10	μA	1
		$V_{OUT}=V_{DD}-30V$	15		10			10		20		
Static current consumption	I_{DD}	$V_{IN}=V_{DD}, V_{SS}$ output open	5		4.0			4.0		30	μA	4
			10		8.0			8.0		60		
			15		16.0			16.0		120		

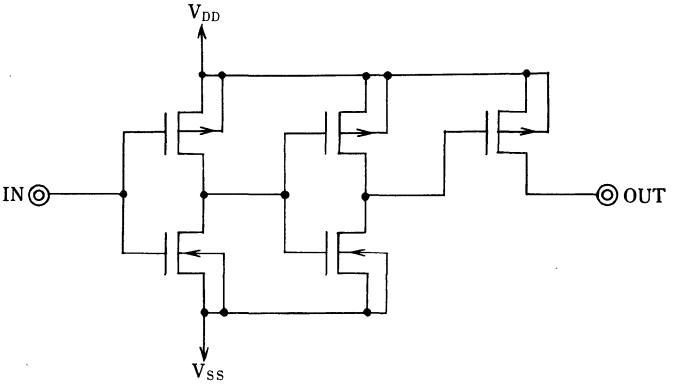
Note 1: Applicable pins $OUT_1 \sim OUT_8$, $V_{IN}=V_{SS}$ or V_{DD}
Note 2: $R_L=20k\Omega$, $I_{OUT} \leqq 1\ \mu A$, Applicable pins $IN_1 \sim IN_8$
Note 3: Applicable pins $IN_1 \sim IN_8$
Note 4: No load condition

■ Logic Diagram (1 circuit)

- LH5012D



- LH5013D



10

LR3428 Analog Clock CMOS IC

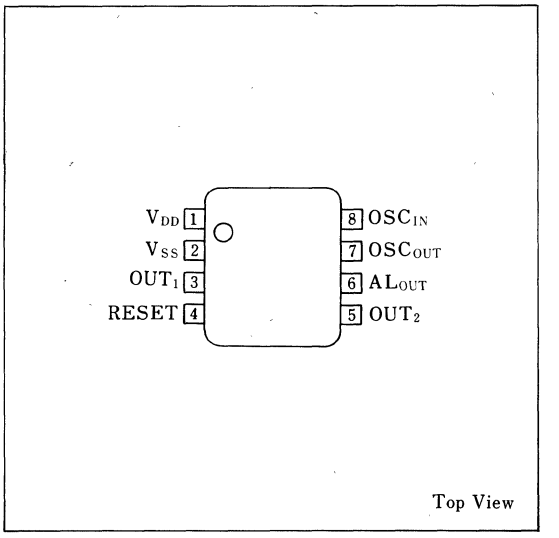
■ Description

The LR3428 is a CMOS IC for electronic clocks using a 4.19MHz crystal, 23-stage frequency divider, motor drive circuit and alarm output buffer.

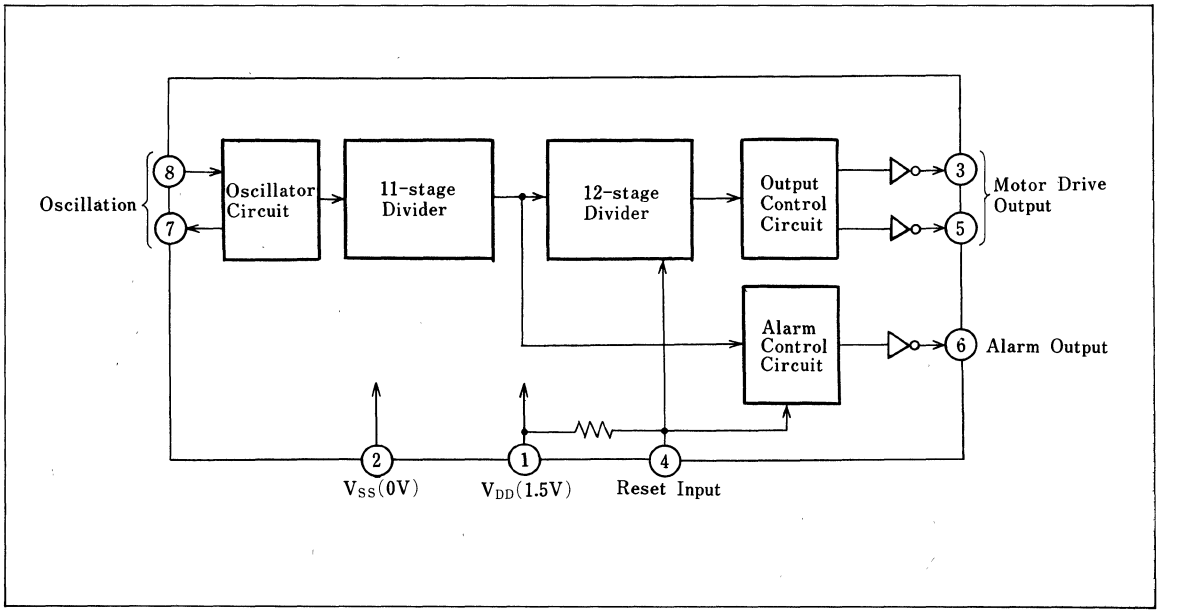
■ Features

1. Low power consumption
2. Low impedance output buffer
3. Modulated alarm output
4. Single power supply : + 1.5V
5. 1Hz stepper motor drive
6. 4.194304MHz crystal oscillator
7. 8-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*	V_{DD}	−0.3～+2.5	V
	V_{IN}	−0.3～V_{DD}+0.3	V
	V_{OUT}	−0.3～V_{DD}+0.3	V
Operating temperature	T_{opr}	−10～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* Referenced to V_{SS}

■ Operating Conditions

(Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	+1.15～+1.80	V
Oscillator frequency	f_{osc}	4.194304 (TYP.)	MHz
Oscillation start voltage	V_{osc}	1.15	V

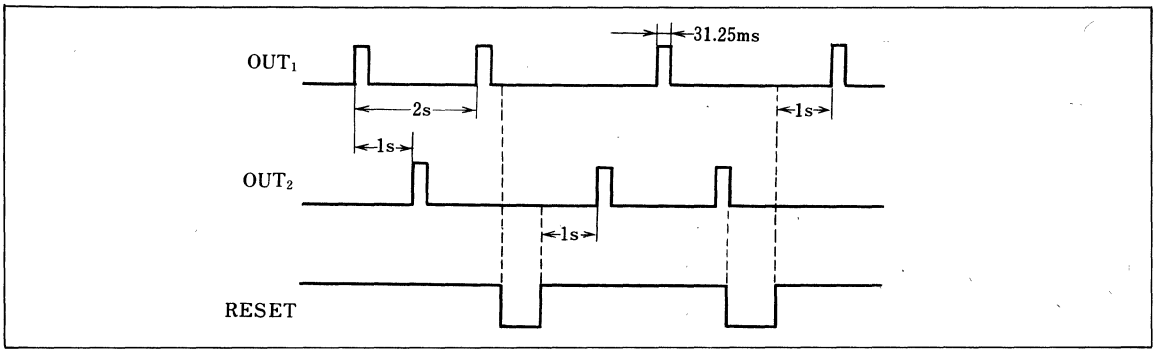
■ Electrical Characteristics

(f_{osc}=4.194MHz, C_G=C_D=15pF, C_1=40Ω, Ta=25℃)

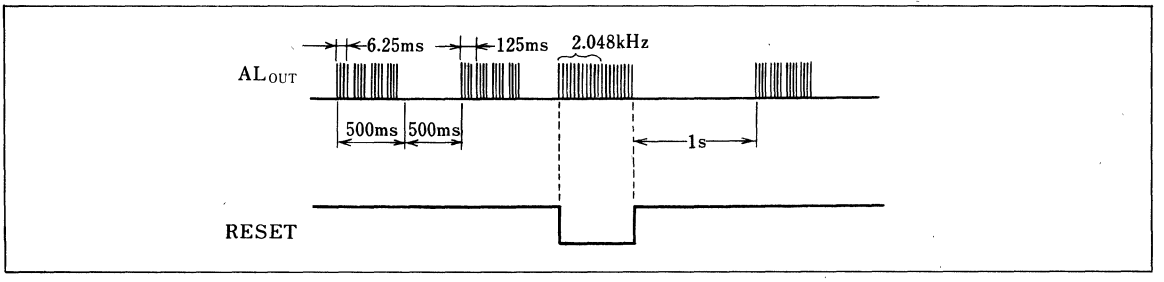
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Current consumption	I_{DD}	V_{DD}=1.5V		25	50	μA
Oscillation stability	Δf/f	V_{DD}=+1.2～+1.7V			1	ppm
Output on resistance	R_{sat1} (P+N)	V_{DD}=1.2V, R_L=180Ω		50	100	Ω
Alarm output on resistance	R_{sat2} (P or N)	V_{DD}=1.2V, R_L=900Ω		150	300	Ω
RESET pin pull up resistance	R_R	V_{DD}=1.5V, V_{IN}=0V		10		kΩ

■ Output Waveform

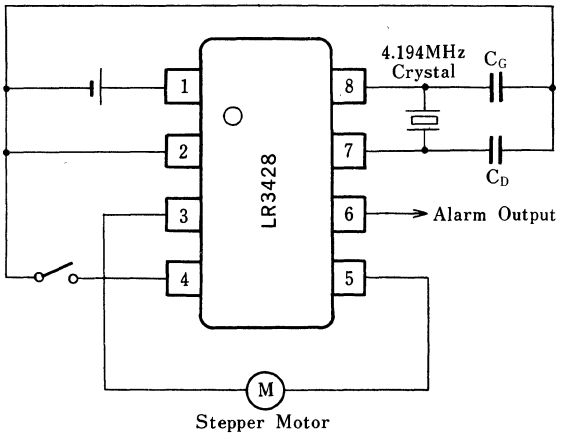
(1) OUT_1, OUT_2



(2) Alarm output



■ System Configuration



LR3429 Analog Clock CMOS IC

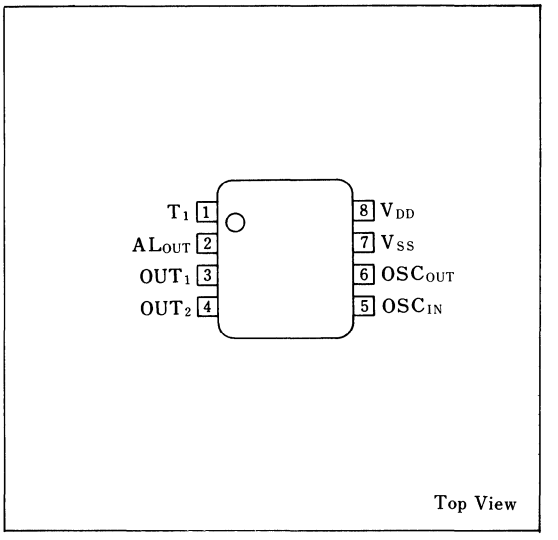
■ Description

The LR3429 is a CMOS IC for electronic clocks using a 4.19MHz crystal, 23-stage frequency divider, motor drive circuit and alarm output buffer.

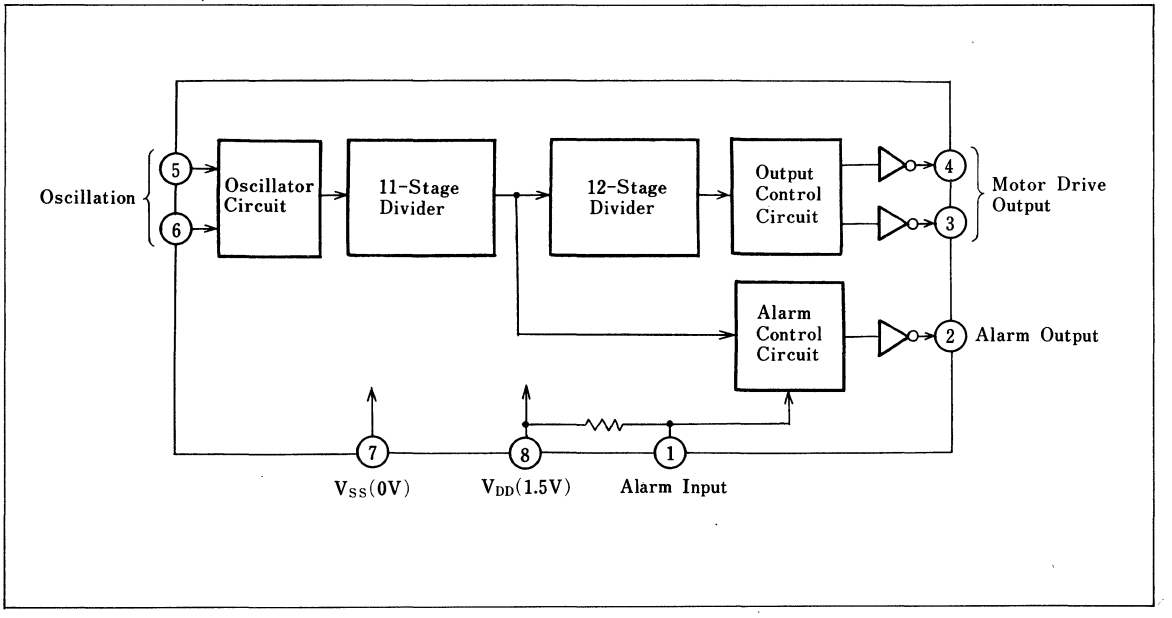
■ Features

1. Low power consumption
2. Low impedance output buffer
3. Modulated alarm output
4. Single power supply : + 1.5V
5. 1Hz stepper motor drive
6. 4.194304MHz crystal oscillator
7. 8-pin dual-in-line package

■ Pin Connections



■ Block Diagram



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■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*	V_{DD}	−0.3～+2.5	V
	V_{IN}	−0.3～V_{DD}+0.3	V
	V_{OUT}	−0.3～V_{DD}+0.3	V
Operating temperature	T_{opr}	−10～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* Referenced to V_{SS}

■ Operating Conditions

(Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	+1.15～+1.80	V
Oscillator frequency	f_{osc}	4.194304 (TYP.)	MHz
Oscillation start voltage	V_{osc}	1.15	V

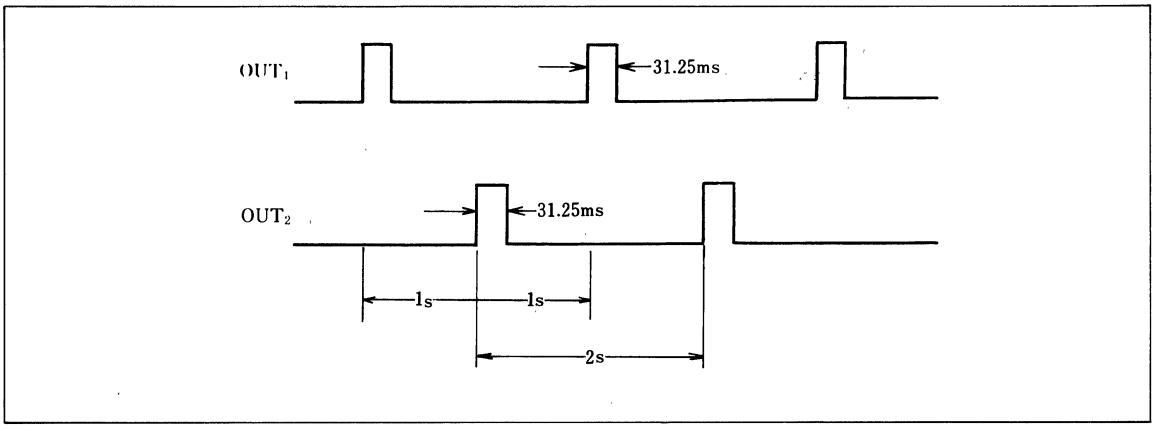
■ Electrical Characteristics

(f_{osc}=4.194MHz, C_G=C_D=15pF, C_1=40Ω, Ta=25℃)

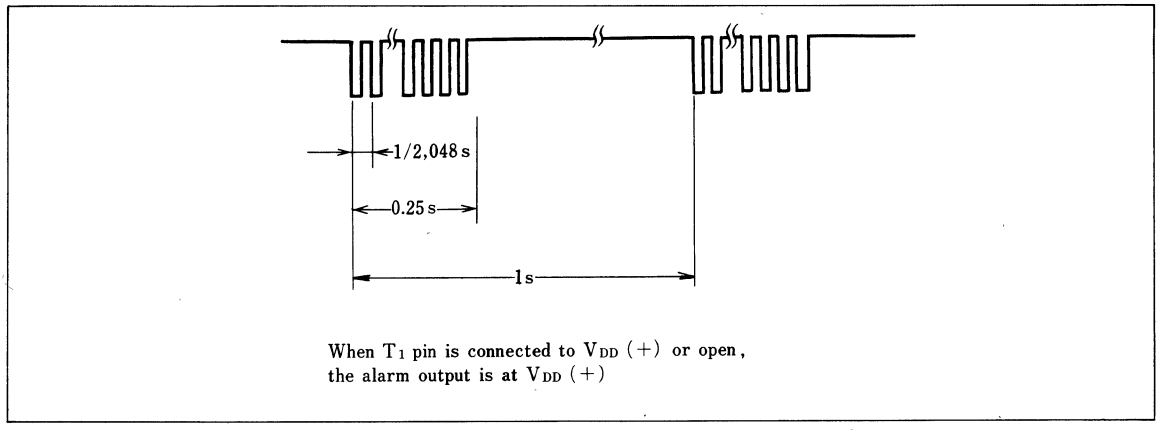
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Current consumption	I_{DD}	V_{DD}=1.5V		25	50	μA
Oscillation stability	Δf/f	V_{DD}=+1.2～+1.7V			1	ppm
Output on resistance	R_{sat1} (P+N)	V_{DD}=1.2V, R_L=180Ω		50	100	Ω
Alarm output on resistance	R_{sat2} (P or N)	V_{DD}=1.2V, R_L=900Ω		150	300	Ω
T_1 pin pull up resistance	R_T	V_{DD}=1.5V, V_{IN}=0V		10		kΩ

■ Output Waveform

(1) OUT_1, OUT_2

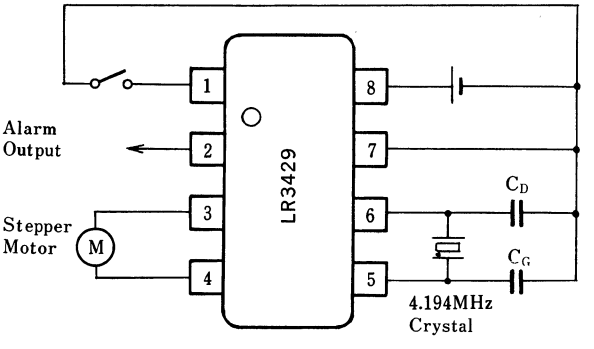


(2) Alarm output (T_1 pin connected to V_{SS})



When T_1 pin is connected to V_{DD} (+) or open, the alarm output is at V_{DD} (+)

■ System Configuration



LR3464 Analog Clock CMOS IC

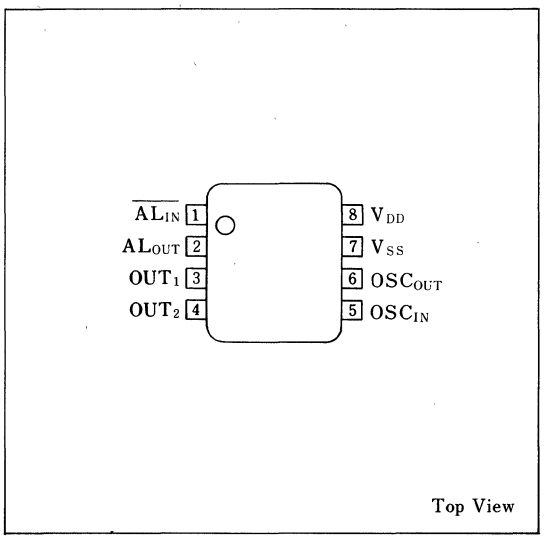
Description

The LR3464 is a CMOS IC for electronic clocks using a 32.768kHz crystal, 16-stage frequency divider, motor drive circuit and alarm output buffer.

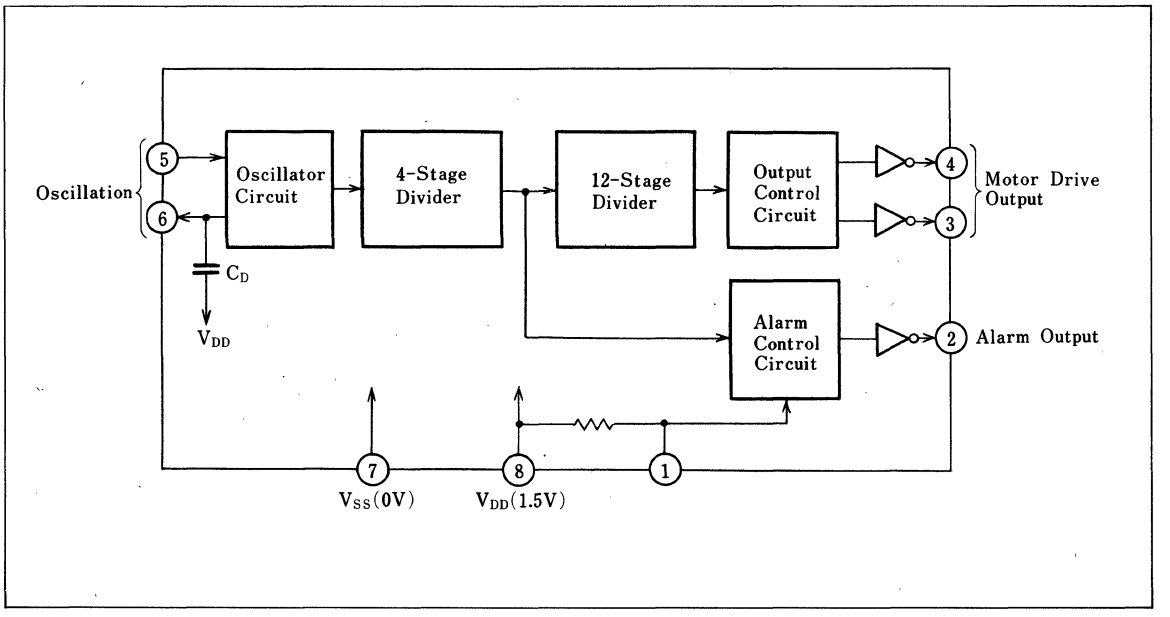
Features

1. Low power consumption
2. Low impedance output buffer
3. Modulated alarm output
4. Single power supply : + 1.5V
5. 1Hz stepper motor drive
6. Included oscillator output capacitor C_D
7. 32.768kHz crystal oscillator
8. 8-pin dual-in-line package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*	V_{DD}	−0.3～+3.0	V
	V_{IN}	−0.3～V_{DD}+0.3	V
	V_{OUT}	−0.3～V_{DD}+0.3	V
Operating temperature	T_{opr}	−10～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* Referenced to V_{DD}

■ Operating Conditions

(Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	+1.10～+1.80	V
Oscillator frequency	f_{osc}	32.768 (TYP.)	kHz
Oscillation start voltage	V_{osc}	1.2	V

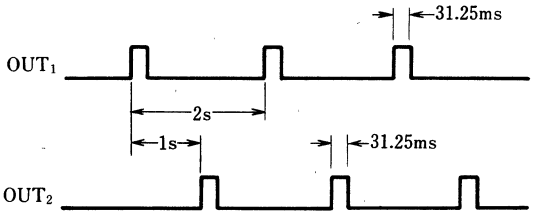
■ Electrical Characteristics

(f_{osc}=32.768kHz, C_G=22pF, C_1=20kΩ, Ta=25℃)

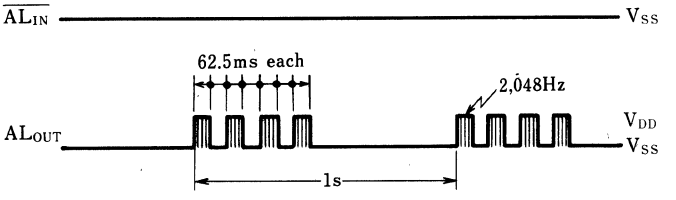
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Current consumption	I_{DD}	V_{DD}=1.5V		1	3	μA
Oscillation stability	Δf/f	V_{DD}=+1.2～+1.7V			6	ppm
Output on resistance	R_{sat1} (P+N)	V_{DD}=1.2V, R_L=300Ω		50	100	Ω
Alarm output on resistance	R_{sat2} (P or N)	V_{DD}=1.2V, R_L=900Ω		150	300	Ω
$\overline{AL_{IN}}$ pin pull up resistance	R_{AL}	V_{DD}=1.5V, V_{IN}=0V		10		kΩ
Oscillation start time	T_{osc}	V_{DD}=1.2V			10	s
Oscillation circuit built-in capacitance	C_D			25		pF
$\overline{AL_{IN}}$ input voltage	V_{IH}	V_{DD}=1.5V	1.35		1.5	V
	V_{IL}	V_{DD}=1.5V	0		0.15	V

■ Output Waveform

(1) OUT_1, OUT_2



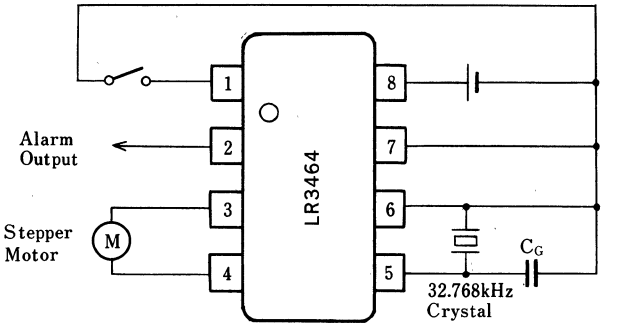
(2) Alarm output (AL_{IN} connected to V_{SS})



When the $\overline{AL_{IN}}$ input is connected to V_{DD} or open, the alarm output is at V_{SS}.

When the $\overline{AL_{IN}}$ input is set at approx. 1/2 V_{DD}, a continuous output of 2,048Hz appears at the alarm output.

■ System Configuration



LR3468 Analog Clock CMOS IC

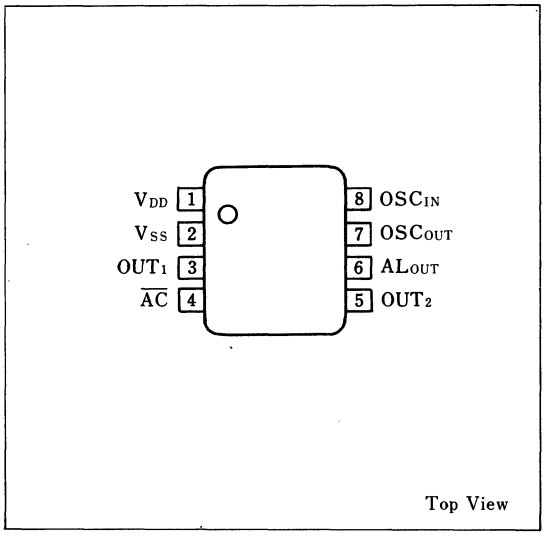
■ Description

The LR3468 is a CMOS IC for electronic clocks using a 32.768kHz crystal, 16-stage frequency divider, motor drive circuit and alarm output buffer.

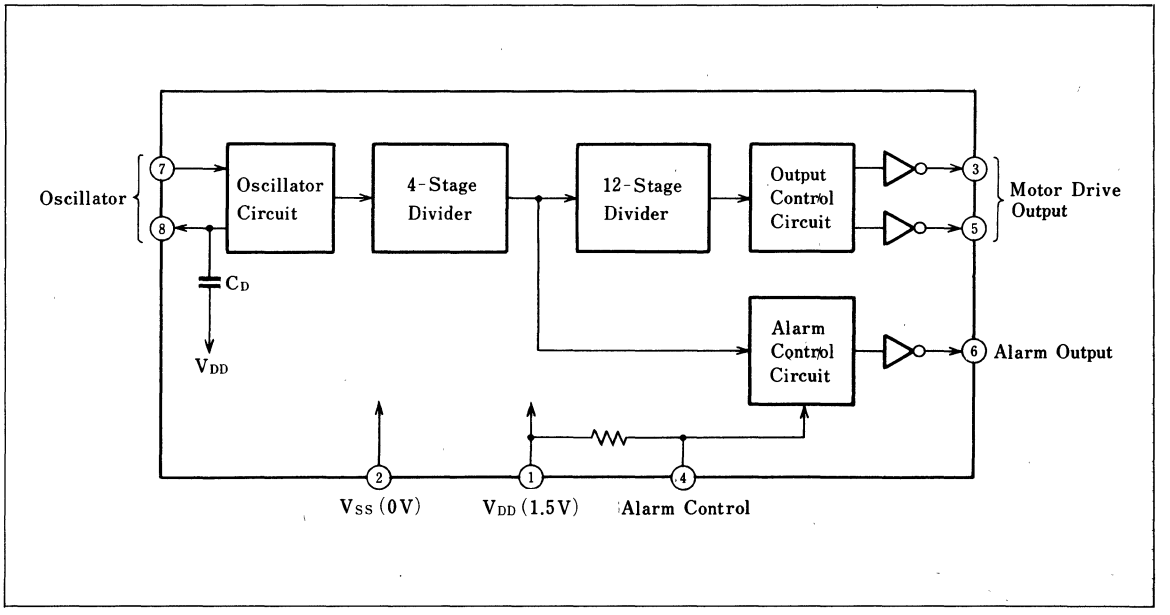
■ Features

1. Low power consumption
2. Low impedance output buffer
3. Modulated alarm output
4. Single power supply : + 1.5V
5. 1Hz stepper motor drive
6. Included oscillator output capacitor C_D
7. 32.768kHz crystal oscillator
8. 8-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*	V_{DD}	−0.3～+3.0	V
	V_{IN}	−0.3～V_{DD}+0.3	V
	V_{OUT}	−0.3～V_{DD}+0.3	V
Operating temperature	T_{opr}	−10～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

* Referenced to V_{DD}

■ Operating Conditions

(Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	+1.1～+1.9	V
Oscillator frequency	f_{osc}	32.768 (TYP.)	kHz
Oscillation start voltage	V_{osc}	1.3	V

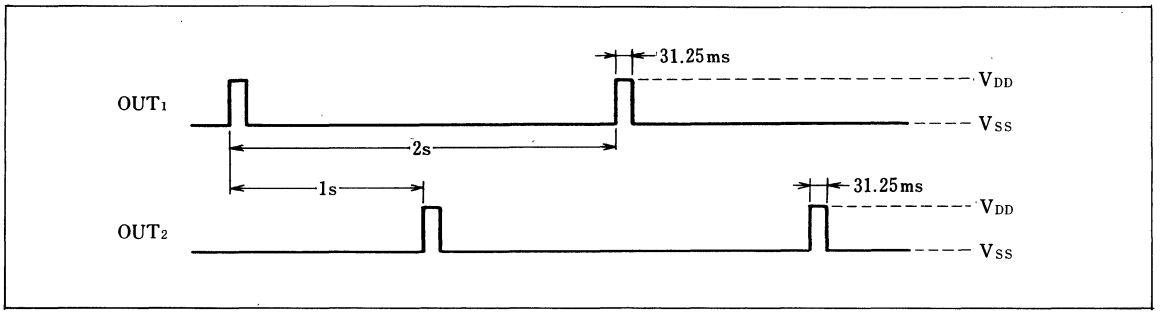
■ Electrical Characteristics

(f_{osc}=32.768kHz, C_G=22pF, C_I=20kΩ, Ta=25℃)

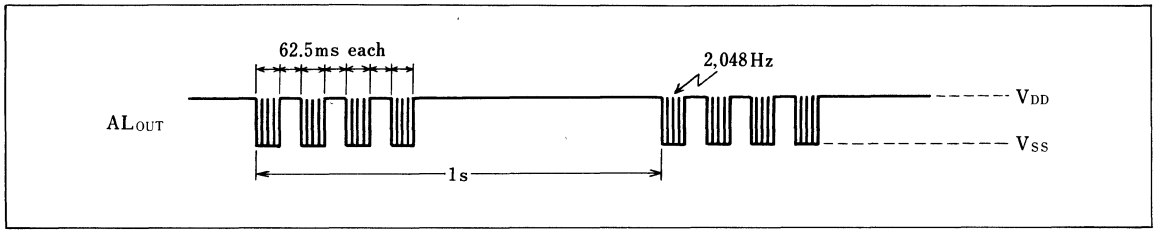
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Current consumption	I_{DD}	V_{DD}=1.5V			10	μA
Oscillation stability	Δf/f	V_{DD}=+1.1～+1.7V			2	ppm/0.1V
Output on resistance	R_{sat1} (P+N)	V_{DD}=1.2V, R_L=600Ω			120	Ω
Alarm output on resistance	R_{sat2} (P or N)	V_{DD}=1.5V, I_{OUT}=1mA		200	600	Ω
$\overline{AC}$ pin pull up resistance	R_{AL}	V_{DD}=1.5V, V_{IN}=0V		10		kΩ
Oscillation start time	T_{osc}	V_{DD}=1.5V			5	s
Oscillation circuit built-in capacitance	C_D			25		pF
$\overline{AC}$ input voltage	V_{IH}	V_{DD}=1.5V	1.4		1.5	V
	V_{IL}	V_{DD}=1.5V	0		0.1	V

■ Output Waveform

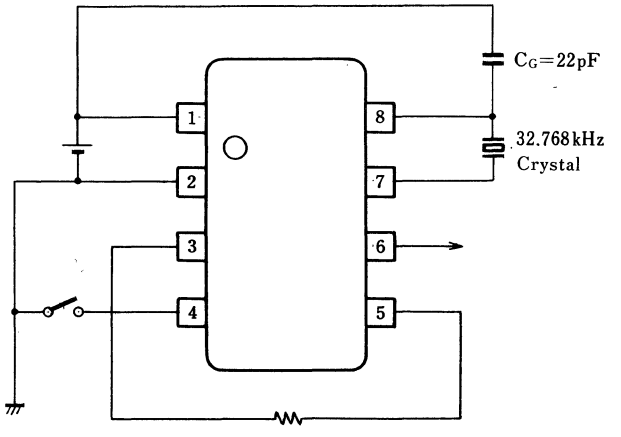
(1) OUT_1, OUT_2



(2) Alarm output ($\overline{AC}$ input open)



■ System Configuration



LR3465 Analog Clock CMOS LSI with Electronic Melody Generator

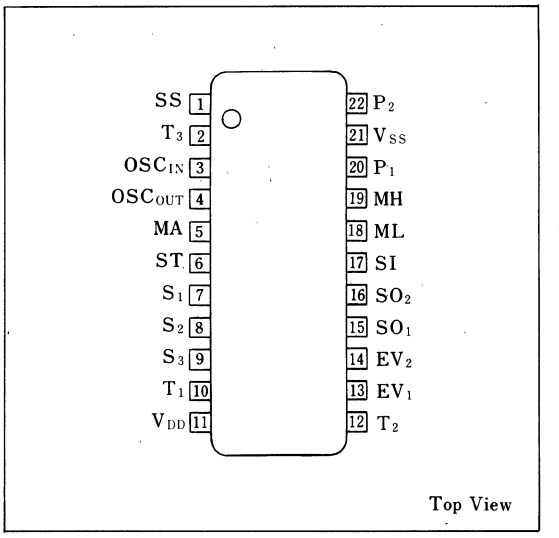
■ Description

The LR3465 is a CMOS IC for electronic clocks using a 32.768kHz crystal with stepper motor drive circuit and melodies, alarm functions.

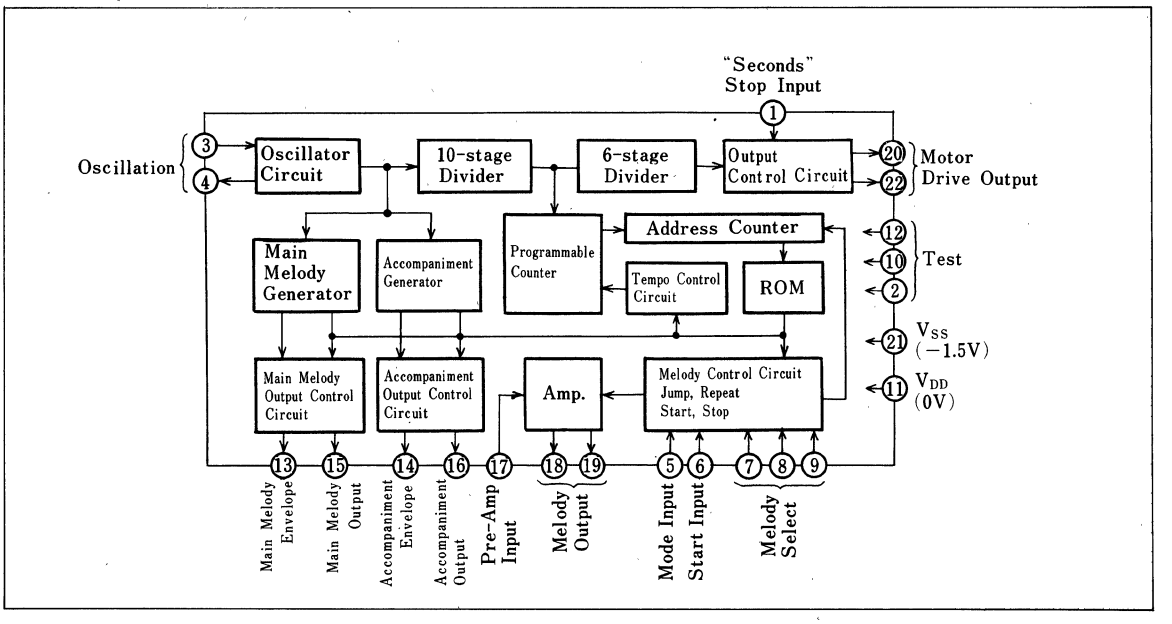
■ Features

1. Low resistance outputs for stepper motor
2. "Seconds" stop function
3. Melody performance with accompaniment
4. Mask ROM programmable
5. 8 melodies (3-melody select inputs)
6. Loudness volume control function
7. Melody envelope controlled by external CR circuit
8. 32.768kHz crystal oscillator
9. Single power supply : − 1.5V
10. CMOS process
11. 22-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Pin voltage*	V_{SS}	−0.3～+0.3	V
	V_{IN}	V_{SS}−0.3～+0.3	V
	V_{OUT}	V_{SS}−0.3～+0.3	V
Storage temperature	T_{stg}	−55～+150	℃
Operating temperature	T_{opr}	−10～+50	℃

* Referenced to V_{DD}

■ Operating Conditions

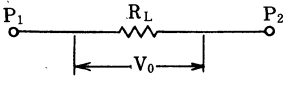
Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−2.0～−1.2	V
Oscillator frequency	f_{osc}	32.768 (TYP.)	kHz
Oscillation start voltage	V_{osc}	−1.4	V

■ Electrical Characteristics

(V_{DD}=0V, V_{SS}=−11.5V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Current consumption	I_{SSS}	Standby no load			5	μA	1
	I_{SSa}	Melody-ON no load			1	mA	
Oscillation start time	T_{osc}	V_{DD}=1.4V			10	s	1
Input voltage	V_{IH}		−0.3			V	2
	V_{IL}				−1.2	V	
Input current 1	I_{IH1}	V_{IN}=0V		2	10	μA	2
Input current 2	I_{IH2}	V_{IN}=0V	10		200	μA	3
Output current 1	I_{OH1}	V_{OUT}=−0.5V	250			μA	4
Output current 2	I_{OH2}	V_{OUT}=−0.5V	3			μA	5
	I_{OL2}	V_{OUT}=−1.0V	3			μA	
Output current 3	I_{OH3}	V_{OUT}=−0.5V	5			μA	6
	I_{OL3}	V_{OUT}=−1.0V	200			μA	
Output current 4	I_{OH4}	V_{OUT}=−0.5V	200			μA	7
	I_{OL4}	V_{OUT}=−1.0V	5			μA	
Output voltage	V_{OUT}	V_{SS}=−1.2V, R_L=300Ω	0.9			V	8
Output pulse width	t			31.25		ms	9
Output cycle	T_1			2		s	9
Output phase difference	T_2			1		s	9
Oscillation stability	Δf/f	V_{SS}=−1.7～1.2V			2.5	ppm/0.1V	1

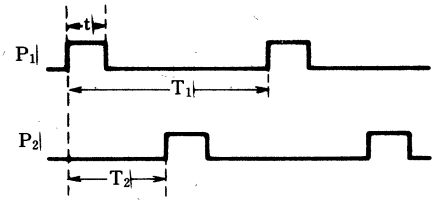
Note 1: C_D=C_C=22pF
Note 2: Applies to ST_1, ST_1～S_3, MA pins
Note 3: Applies to SI pin. Melody OFF time
Note 4: Applies to EV_1, EV_2 pins
Note 5: Applies to SO_1, SO_2 pins
Note 6: Applies to ML pin. The value of I_{OH} for melody OFF time.
Note 7: Applies to MH pin. The value of I_{OL} for melody OFF time.
Note 8: Applies to P_1, P_2 pins. R_L=300Ω (Refer to the right figure.
Note 9: Refer to clock specifications.



10

■ Clock Specifications

〈Step motor drive output〉



By altering PLA, the output pulse width t can be selected from the following : 15, 31, 46, 62, 78, 93, 109 (ms)

〈Second stop function〉

Second counting will be performed and the output for the step motor will turn off while the SS input is ON. On turning the SS input OFF, the second counter is enabled to start. (Maximum error : 31.25ms).

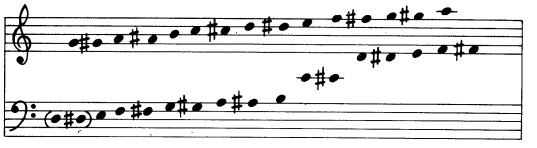
■ Melody Specifications

〈Number of music〉 Up to 8 pieces

〈ROM〉 600 steps × 13 bits

〈Sound source〉 2 sources

〈Range〉 2.5 octaves

For the sounds in parentheses ( ), only the attack sound output will be generated.

〈Tempo〉 15 speeds for each music (The minimum note length shall be selected from between 31 ~468ms).

〈Note length〉 2 kinds (Other notes of different length can be represented by the different number of steps.)

(Example) If the fastest note in a music is ♪, the kinds of note that can be specified by 1 step are ♪ and ♩. The note length control is by "1" and "0".

♩ = ♪ (1) + ♪ (0) ····· 2 steps

♩. = ♪ (1) + ♪ (0) + ♪ (0) ····· 3 steps

♪ = ♪ (1) + 𝅘𝅥𝅯 (0) ····· 2 steps

The number in parentheses ( ) represents envelop control.

〈Number of performances〉 1~15 times, endless

〈Commands〉 Melody command

Control command
- Snooze command
- Jump command
- Repetition number setting command
- End command

〈Command organization〉

I_1~I_5	Predominant melody interval
I_6	Predominant envelope control
I_7~I_{11}	Accompaniment interval
I_{12}	Accompaniment envelope control
I_{13}	Note length control

〈Music selection〉

According to the state of the music select input S_1~S_3, one music will be selected from the 8 pieces of music available. The pull-down resistor built into the music select pins allows the pins to be used either connected to V_{SS} or open.

If the music select input state is altered in the middle of performance, the music then specified will be performed from the start. A music selection for the LR34651 in which 8 pieces of music is written in is shown in the table below.

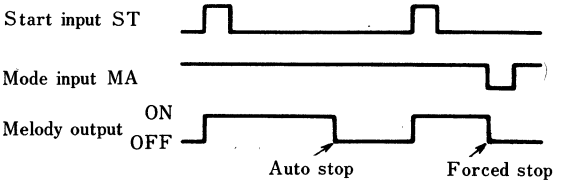
Music select input			Name of music	Tempo ♩ =	Number of repetitions	
S_1	S_2	S_3			$T_3=V_{DD}$	$T_3=V_{SS}$
H	H	H	Westminster	68.6	1	1
L	H	H	Westminster	96	1	1
H	L	H	*	96	8	1
L	L	H	Spring (Four seasons) Vivaldi	96	10	1
H	H	L	Autumn (Four seasons) Vivaldi	96	8	1
L	H	L	Winter (Four seasons) Vivaldi	40	5	1
H	L	L	Chime	192	Endless	Endless
L	L	L	Alarm	240	Endless	Endless

* Twinkle twinkle little star French music

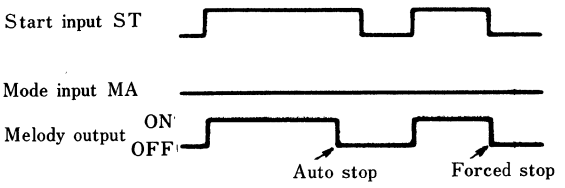
H : V_{DD} L : V_{SS} or open

〈Melody start, stop〉

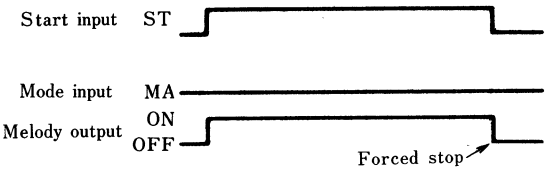
(1) One shot type



(2) Hold type (Number of repetitions 1~15 times)



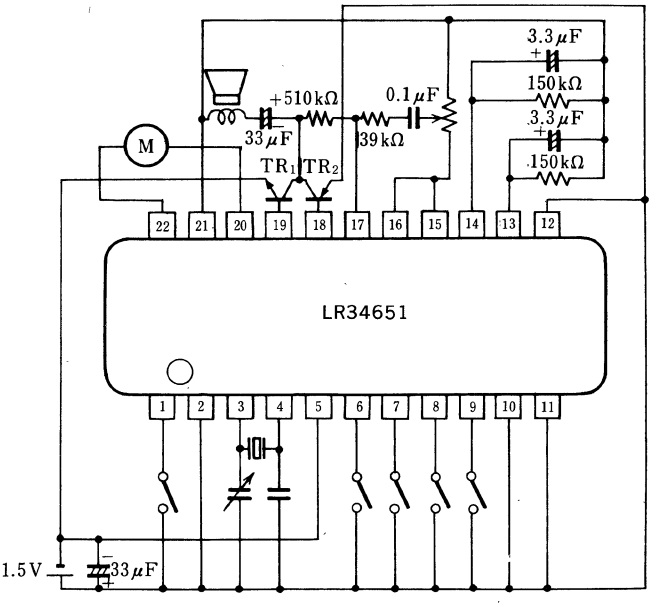
(3) Hold type (Number of repetition Endless)



〈Snooze function〉

Snooze function allows each music to be programmed into the mask ROM independently. However, the number of musics that can be selected will be reduced because a program in snooze function is one of the melody programs.

■ System Configuration (LR34651)



Note TR_1 : 2SC1383
TR_2 : 2SA683

Envelope waveform is determined by the value of R applied to pins No. 14 and No. 15.

Make sure that pins No. 10 and No. 12 are to be connected to No. 11.

Make sure that pin No. 2 is to be connected to pins No. 11 or No. 21.

LR3441 LCD Digital Clock CMOS LSI

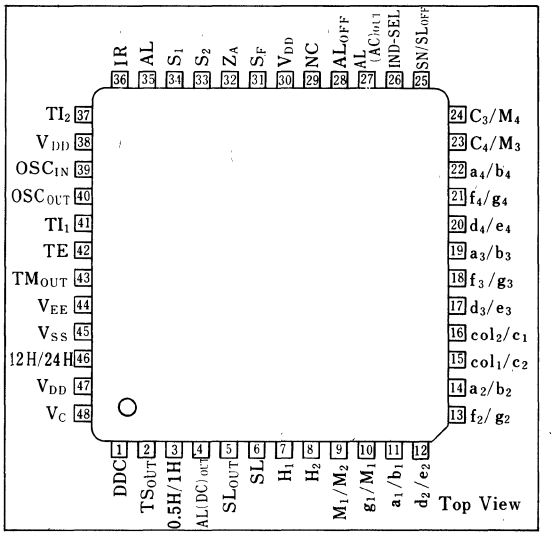
■ Description

The LR3441 is CMOS LSI for LCD display clocks with a basic three function, daily alarm, hourly alarm and timer.

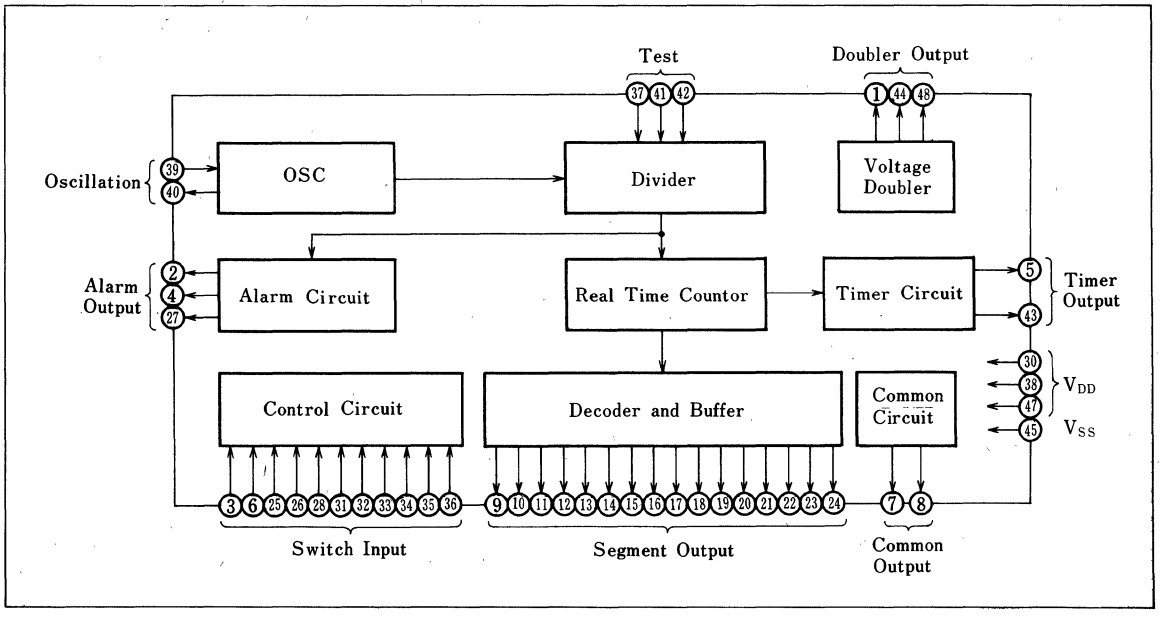
■ Features

1. Three functions ("Hour", "Minute", "Second") "Second" display by colon
2. Alarm function with Snooze function
3. Hourly alarm
4. Timer function
5. Instant second set function (1 ~ 59 sec..... No carry to the minute digit)
6. 3V dynamic LCD drive
7. 32.768kHz crystal oscillator
8. Single power supply : − 1.5V (with voltage doubler)

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage	V_{SS}	−2.0～+0.3	V	1
	V_{EE}	−4.0～+0.3	V	1
	V_{IN}	V_{SS}−0.3～+0.3	V	1,2
	V_{OUT1}	V_{SS}−0.3～+0.3	V	1,2
	V_{OUT2}	V_{EE}−0.3～+0.3	V	1,3
Operating temperature	T_{opr}	−10～+60	℃	
Storage temperature	T_{stg}	−5.5～+150	℃	

Note 1: Referenced to V_{DD}
Note 2: Applies to V_{SS} pins
Note 3: Applies to V_{EE} pins

■ Operating Conditions (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{SS}	−1.8～−1.2	V
	V_{EE}	$2V_{SS}$ (TYP.)	V
Oscillator frequency	f_{osc}	32.768 (TYP.)	kHz
Oscillation start voltage	V_{osc}	−1.4	V

■ Electrical Characteristics (V_{DD}=0V, V_{SS}=−1.5V, V_{EE}=−3.0V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Current consumption	I_{total}	No load		1.5	3.0	μA	4
Oscillation start time	T_{osc}	V_{SS}=−1.4V			10	s	4
Segment output current	I_{OS}	V_{DS}=0.5V	20			μA	
Common output current	I_{OC}	V_{DS}=0.5V	60			μA	
DDC output current	I_{OD}	V_{DS}=0.5V	60			μA	
V_C output current	I_{OV}	V_{DS}=0.5V	120			μA	
AL $(AC)_{OUT}$, TS_{OUT} Output current	I_{OH1}	V_{OUT}=−0.2V	200			μA	
AL $(DC)_{OUT}$, SL_{OUT}, TM_{OUT} Output current	I_{OH2}	V_{DS}=0.2V	100			μA	
Pull down resistance	R_{S1}	V_{IN}=0V		700		kΩ	5
	R_{S2}	V_{IN}=0V		500		kΩ	6
	R_T	V_{IN}=0V		100		kΩ	7
Input voltage	V_{IH}	V_{SS}=−1.8～−1.2V	−0.1		0	V	8
	V_{IL}	V_{SS}=−1.8～−1.2V	V_{SS}		V_{SS}+0.1	V	8

Note 4: C_D=C_C=22pF, C_1=C_2=0.1 μF
Note 5: Applies to 0.5H/1H, SF pins
Note 6: Applies to ZA, S_1, S_2, SN/SL_{OFF}, SL, AL pins
Note 7: Applies to TE, TI_1, TI_2, IR pins
Note 8: Applies to 0.5H/1H, SF, ZA, S_1, S_2, SN/SL_{OFF}, SL, AL, IND-SEL, AL_{OFF}, 12H/24H pins

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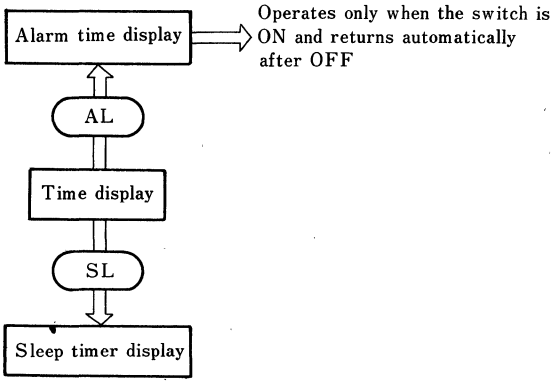
■ Specifications

(1) Input control

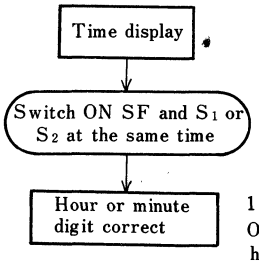
Symbol	Content	LR3441
S_1	"Hour" set	Pull down to V_{DD}
S_2	"Minute" set	Pull down to V_{DD}
SF	Safety	Pull down to V_{DD}
ZA	0 adjust	Pull down to V_{DD}
AL	Alarm mode switch	Pull down to V_{DD}
SL	Sleep timer mode switch	Pull down to V_{DD}
SN/SL_{OFF}	Snooze "ON" sleep "OFF"	Pull down to V_{DD}
AL_{OFF}	Alarm output "OFF"	Open・drain
12H/24H	12 hours/24 hours switch	Open・drain
IND_{SEL}	Indicator select	Open・drain
IR	Initial・reset	Pull down to V_{DD}
0.5H/1H	Sleep time 32 minutes/64 minutes switch	Pull down to V_{DD}

(2) Operation flow

(i) Function read operation



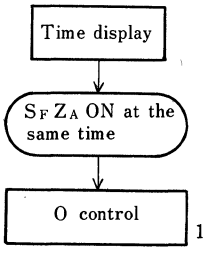
(ii) Time display adjust operation



1 push 1 word forward
ON more than 2 seconds
hour digit 1Hz forward
minute digit count up 5 minutes at a time

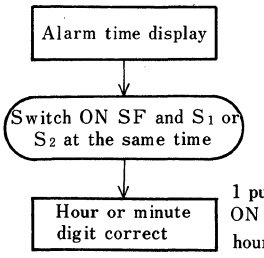
(Example) 2→3→5→10···

(iii) 0 adjust



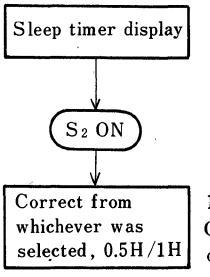
1~59 seconds are truncable

(iv) Alarm time display adjust operation



1 push 1 word forward
ON more than 2 seconds
hour digit 1Hz forward
minute digit count up 5 minutes at a time

(v) Sleep time display adjust operation



1 push 1 word count down
ON more than 2 seconds count down 5 minutes at a time

(vi) Mode display format

Mode		Display
Time display		HH : MM
Time display adjust operation	SF & S_1 ON	*1 : MM
	SF & S_2 ON	HH : *2
Alarm time	AL ON	HH : MM
	AL & S_1 ON	*1 : MM
	AL & S_2 ON	HH : *2
Sleep timer	SL ON	MM
	SL & S_2 ON	*3

1 Hz flashing
*1 S_1 1 count-up with each ON
*2 S_2 1 count-up with each ON. Rapid feed by 5 minutes if S_2 held ON for more than 2 seconds.
*3 S_2 1 count-down with each ON. Counts-down by 5 minutes if S_2 held ON for more than 2 seconds.

■ Functions

(1) Alarm function

(i) If the set alarm time coincides with the real time, the following outputs will be generated at each of the following outputs.

- At $AL(AC)_{OUT}$ 4 minute tone output of 2kHz × 8Hz × 1Hz
- At $AL(DC)_{OUT}$ approximately 32 (64) minute control output
- At TM_{OUT} approximately 32 (64) minute control output

(ii) When the SN/SL_{OFF} is turned ON while the alarm output is being generated, the output will be interrupted for approximately 7 minutes until the output generation is resumed. Called snooze function, it can be repeated for either approximately 32 minutes or 64 minutes.

(iii) The alarm indicator selected by the IND_{SEL} pin with the alarm timer being set can be displayed.

(iv) With AL_{OFF} switch connected to V_{SS}, the alarm indicator will not be displayed and alarm will not be output even if the alarm time and the real time coincide.

(v) The alarm control output time can be selected by the 0.5H/1H pin to either 32 or 64 minutes except when alarm output is being generated.

(2) Sleep timer function

(i) If the SL is depressed with no TM_{OUT} output, either 32 or 64 will be selected according to the state of the 0.5H/1H pin and TM_{OUT} and SL_{OUT} will be output.

(ii) The remainder of the time can be displayed if the SL is turned ON while the sleep timer is in operation.

(iii) Whenever the SN/SL_{OFF} pin is turned ON while the sleep timer is in operation, the sleep out will go OFF.

(iv) If the SL is turned ON during the alarm output, the TM_{OUT} and $AL(DC)_{OUT}$ will be output for another 32 or 64 minutes. The timer interval can be selected by the 0.5H/1H pin to either 32 or 64 minutes except in the sleep operation.

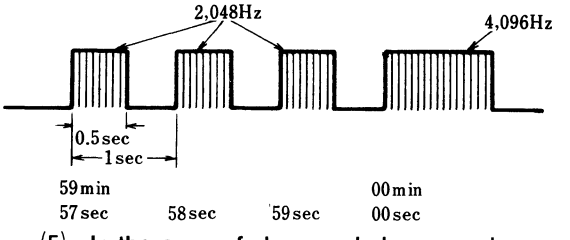
(v) When S_2 has been depressed to set the sleep timer to "0" in rapid feed, it will stay at "0" on further depression of S_2.

(3) Timer out

The TM output (DC) will be generated when either the sleep output or the alarm output (DC) is generated. The timer out is an OR-circuit of the sleep out and $AL(DC)_{OUT}$. If the AL_{OFF} is ON with only AL(DC) as the output, the timer out will also be turned OFF.

(4) Time signal

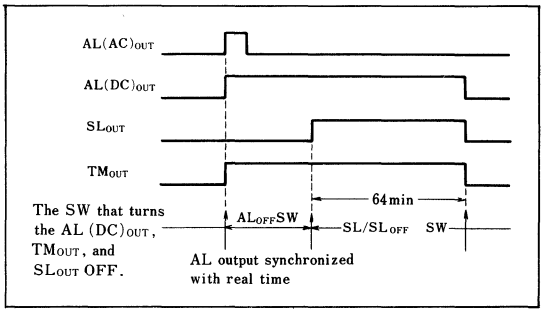
The TS_{OUT} pin that outputs time signal is provided. The output starts at 59 minutes 57 seoncds. (See the figure below.)



(5) In the case of alarm and sleep overlap

(i) The figure below shows the state of each output pin when the sleep timer goes into operation during the alarm output.

When the SL is turned ON, the $AL(DC)_{OUT}$ and TM_{OUT} intervals will be set to another 64 min/32 min. When the SN/SL_{OFF} is turned ON, the TM_{OUT}, AL_{OUT}, and SL_{OFF} will be turned OFF.



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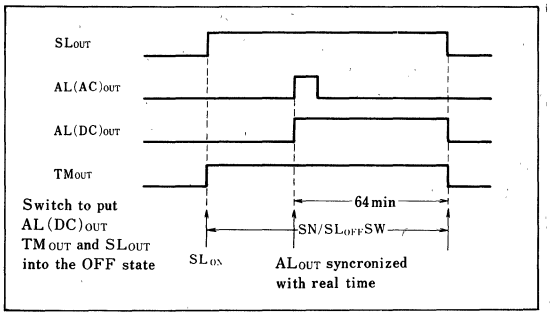
(ii) When the alarm time and the real time coincide while the sleep timer is in operation to generate the alarm output, the SL_{OUT} and TM_{OUT} intervals will be set for another 64 min/32 min.



In this case if the SN/SL_{OFF} is turned ON, the $AL(DC)_{OUT}$ and $AQ(AC)_{OUT}$ will go OFF never to be output even 7 minutes later. When the AL_{OFF} is turned ON, only the $AL(AC)_{OUT}$ will go OFF.

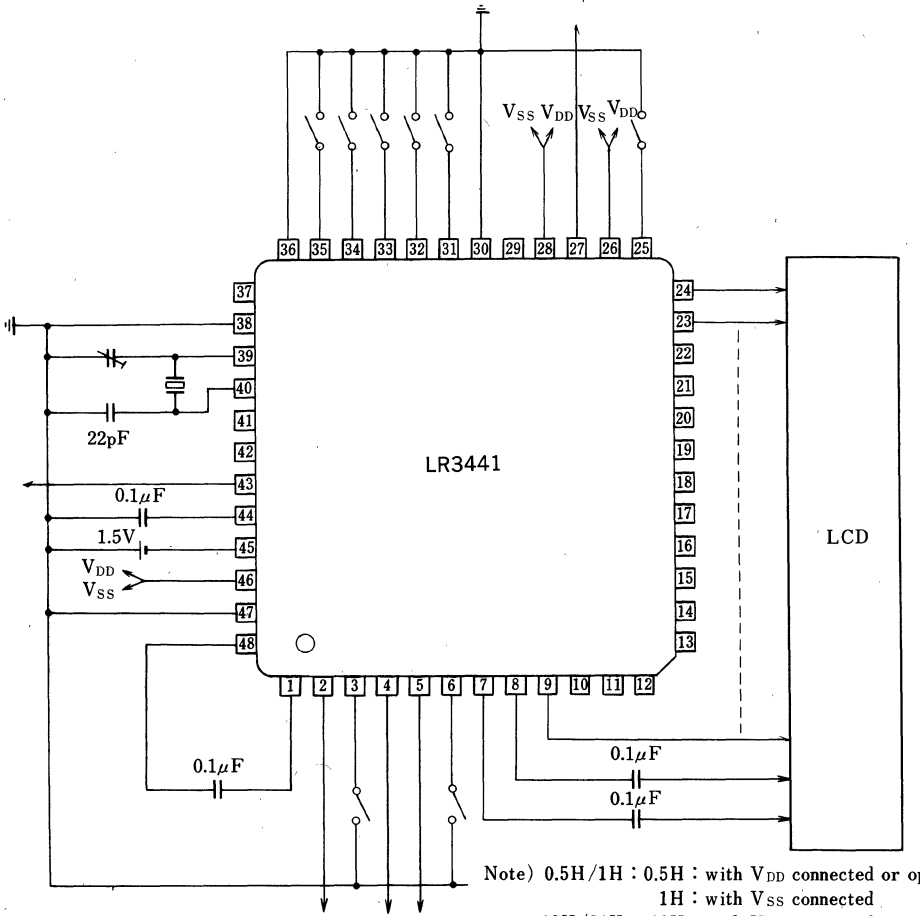
(6) Initial reset

If the IR pin is connected to V_{SS}, initial reset will be applied to immediately reset all the counters and AM 12 : 00 or 0 : 00 will be displayed depending on the 12H system in the case of the former, 24H system in the case of the latter.

(7) Indicator select

The IND_{SEL} pin can select either the bell mark or the note mark.
Note mark : with V_{DD} connected or open
Bell mark : with V_{SS} connected

■ System Configuration



LR3419 Digital ON/OFF Clock Timer CMOS LSI

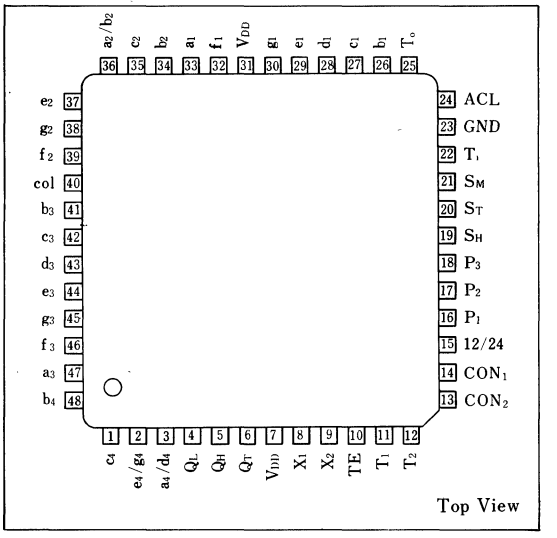
■ Description

The LR3419 is a CMOS LSI designed to provide clock and timer functions. The base frequency is selectable: 50 Hz or 60 Hz line input or 32.768kHz crystal. It is also capable of driving fluorescent displays tube (VFD) directly.

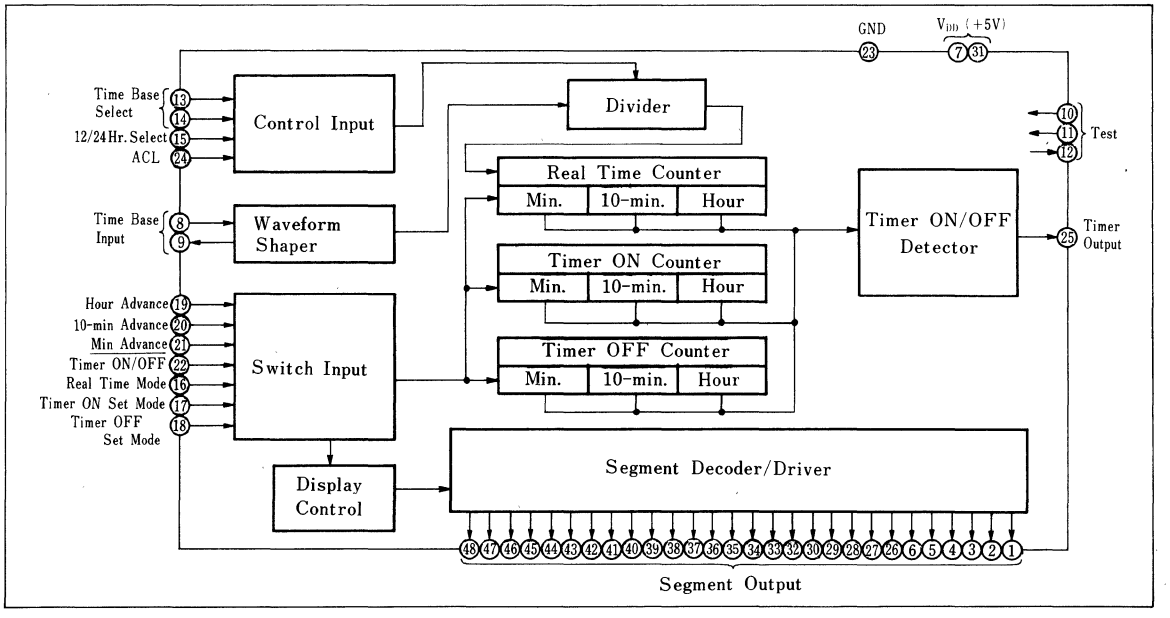
■ Features

1. "Hours-Minutes" display
2. Timer function that permits both ON/OFF times to be set
3. Power failure indication
4. Directly static-drive a VFD
5. Time base : 50/60Hz line or 32.768kHz crystal
6. Power supply voltage : +5V
7. CMOS process
8. 48-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit	Note
Supply voltage	V_{DD}	Referenced to GND	−0.3～+7.0	V	
Input voltage	V_{IN}	Referenced to GND	−0.3～(V_{DD}+0.3)	V	
Output voltage	BV	Referenced to GND	V_{DD}+0.3～−23	V	1
Power consumption	P_D	Ta≦+25℃	550	mW	
derating ratio		Ta>+25℃	5.4	mW/℃	
Pin current	I_I		±2.0	mA	1
			±1.0		2
Operating temperature	T_{opr}		−10～+60	℃	
Storage temperature	T_{stg}		−40～+100	℃	

Note 1: Applies to $a_{1\sim4}$, $b_{1\sim3}$, $c_{1\sim4}$, $d_{3\sim4}$, $e_{1\sim4}$, $f_{1\sim4}$, $g_{1\sim4}$, Q_L, Q_H, Q_T pins
Note 2: Applies to I/O pins except Note 1

■ Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	Referenced to GND	4.5	5.0	5.5	V
Input voltage	V_{IN}	Referenced to GND	0		V_{DD}	V
Output voltage	V_{OUT}	Referenced to GND	−21	−19	0	V

■ Electrical Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}	Applies to all input pins	4.0		V_{DD}	V	3～7
	V_{IL}	V_{DD}=5.0V	0		0.4		
Input current	I_{IH1}	$V_{IN}=V_{DD}$			1.0	μA	3
	I_{IL1}	V_{IN}=GND			−1.0		
	I_{IH2}	$V_{IN}=V_{DD}$		5.0	30	μA	4
	I_{IL2}	V_{IN}=GND			−1.0		
	I_{IH3}	$V_{IN}=V_{DD}$			1.0	μA	5
	I_{IL3}	V_{IN}=GND		−0.5	−3.0		
	I_{IH4}	$V_{IN}=V_{DD}$			1.0	μA	6
	I_{IL4}	V_{IN}=GND	−10	100			
	I_{IH5}	$V_{IN}=V_{DD}$		0.5	3.0	μA	7
	I_{IL5}	V_{IN}=GND		−0.5	−3.0		
Input amplitude	V_I	f=50 or 60Hz	4.0		V_{DD}	V_{p-p}	
Output voltage	V_{OH1}	I_{OH}=0.5mA, V_{DD}=5.0V	4.5	4.9		V	1
	V_{OL1}	Connects to −19V at R_L=100kΩ	−19.0		−18.0		
	V_{OH2}	I_{OH}=0.2mA, V_{DD}=5.0V	4.5	4.9		V	8
	V_{OL2}	I_{OL}=−0.2mA, V_{DD}=5.0V		0.1	0.5		
Time・base	f	CON_1=GND, CON_2=GND		50		kHz	
		$CON_1=V_{DD}$, CON_2=GND		60			
		CON_1=GND, $CON_2=V_{DD}$		32.768			
Current consumption	I_{DD}	f=50Hz, $V_I=V_{DD}V_{p-p}$			50	μA	1
		f=60Hz, $V_I=V_{DD}V_{p-p}$			50		8
		With 32.768kHz crystal			50		9

Note 3: Applies to CON_1, CON_2, 12/14 pins
Note 4: Applies to $P_{1\sim3}$, S_H, S_T, S_M, T_1 pins
Note 5: Applies to ACL pin
Note 6: Applies to TE, T_1 pins
Note 7: Applies to X_1 pin
Note 8: Applies to T_{OUT} pin
Note 9: Clock display mode

■ Specifications

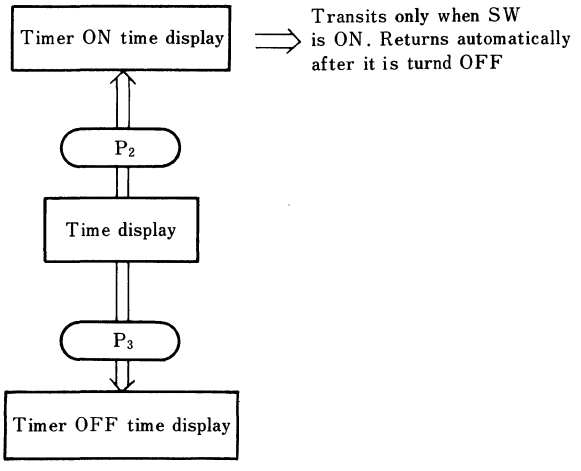
(1) Basic time base

Time base	Time base select input		Time base input pin	
	CON_1	CON_2	X_1	X_2
50Hz	0	0	50Hz	OPEN
60Hz	1	0	60Hz	OPEN
32.768kHz	0	1	*	
Disable	1	1		

* Oscillator feedback circuit that consists of crystal and capacitance

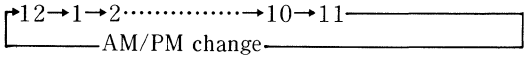
(2) Operation flow chart

(i) Function readout operation

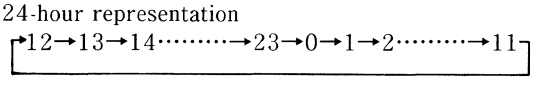


Note: Hour rapid feed (S_H) will proceed as follows.

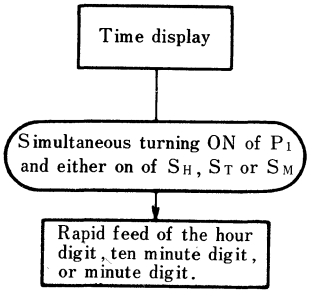
12-hour representation



24-hour representation



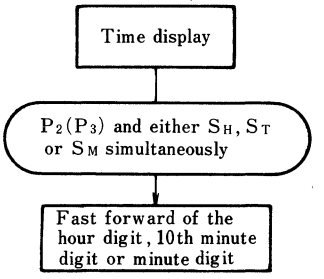
(ii) Hour display adjust operation



◦ Counter digit below second will be reset

- After P is turned OFF, timing starts from 00 second.
- While being adjusted, the 10 minute digit does not increment the hour digit, nor does the minute digit increment the 10 minute digit.

(iii) Timer ON (OFF) time setting operation



- Setting will be complete when $P_2(P_3)$ is OFF.
- While being adjusted, the 10 minute digit does not increment the hour digit, nor does the minute digit increment the 10 minute digit.
- In the timer ON (OFF) time set mode, timing will not stop.
- In the timer ON (OFF) time set mode, timer output will not be affected even if the timer ON (OFF) time coincides with the time display.

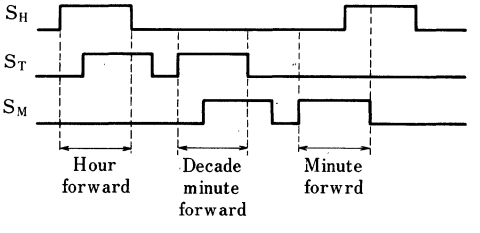
(iv) Simultaneous depression of setting switches

Normally only one of P_1, P_2, and P_3 goes ON. If more than two of these are depressed simultaneously, they enter no input and go into the time display mode.

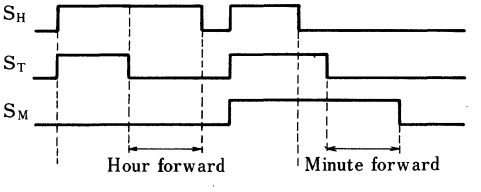
(v) Simultaneous depression of rapid feed switches

Normally only one of S_H, S_T, and S_M goes ON. If more than two of these are depressed simultaneously, the following operation will proceed.

(a) If one input goes ON followed by another input that ON



(b) More than 2 inputs go ON simultaneously



(vi) Power failure display function

In any mode, LSI will be initialized inside on application of ACL to display :

With 12 hour representation PM 12 : 00
With 24 hour representation 12 : 00

This whole display goes flashing, 0.5 second ON and 0.5 second OFF. The display stays in the initial state. To stop flashing, go into the time display mode (P_1 ON) and then timing starts with P_1 turned ON.

On application of ACL with P_1 set to ON, the display will stay in the initial state without flashing.

On the next P_1 ON, the display still in the initial state will go flashing. Then on the next P_1 ON, flashing will stop. And on the next P_1 ON, timing starts.

(vii) Auto clear circuit

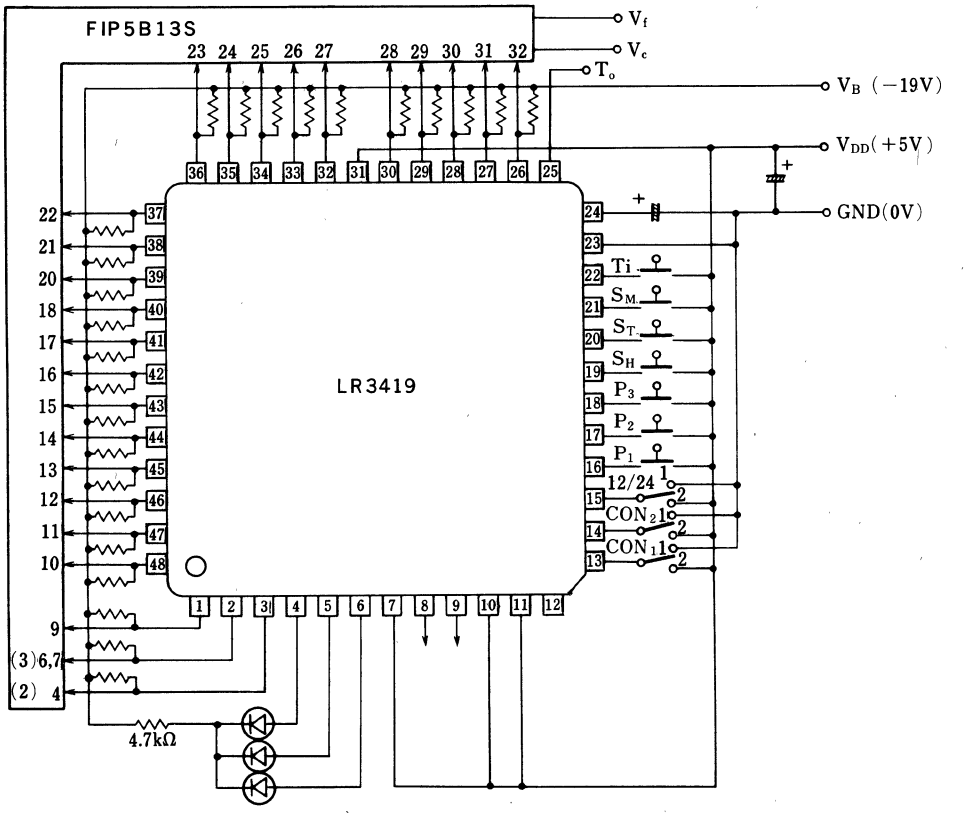
The internal state on power-up will be as follows.

(a) Time display
12 hour representation PM 12 : 00
24 hour representation 12 : 00

And the second counter will be reset. From the time when the auto clear input ceases to exist, it will operate according to the mode input (P_1, P_2, P_3).

(b) Time ON and Timer OFF time
With 12 hour representation PM 12 : 00
With 24 hour representation 12 : 00

■ System Configuration



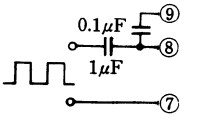
Note 1: Set to side 2 under 24 hour system, and set to side 1 under 12 hour system

Note 2: Time base selection

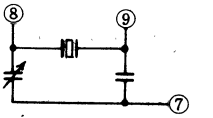
	CON_1	CON_2
50Hz	side 1	side 1
60Hz	side 2	side 1
32.758kHz	side 1	side 2

Note 3: Time base input circuit

(a)At 50Hz, 60Hz



(b)At 32.768kHz



Note 4: Fluorescent display tube FIP5B135
The number indicates the pin number.
The figure in ( ) is for 12 hour system.

LR3472 VTR Program Timer CMOS LSI

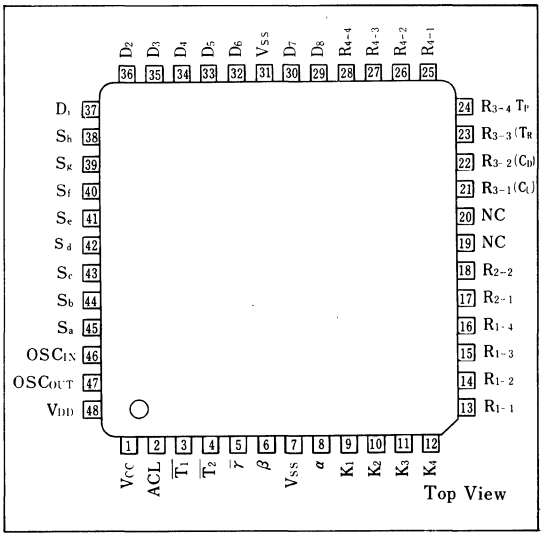
■ Description

The LR3472 is a CMOS LSI for a 6 events 1 week VTR program timer. It can directly drive a fluorescent display tube (VFD).

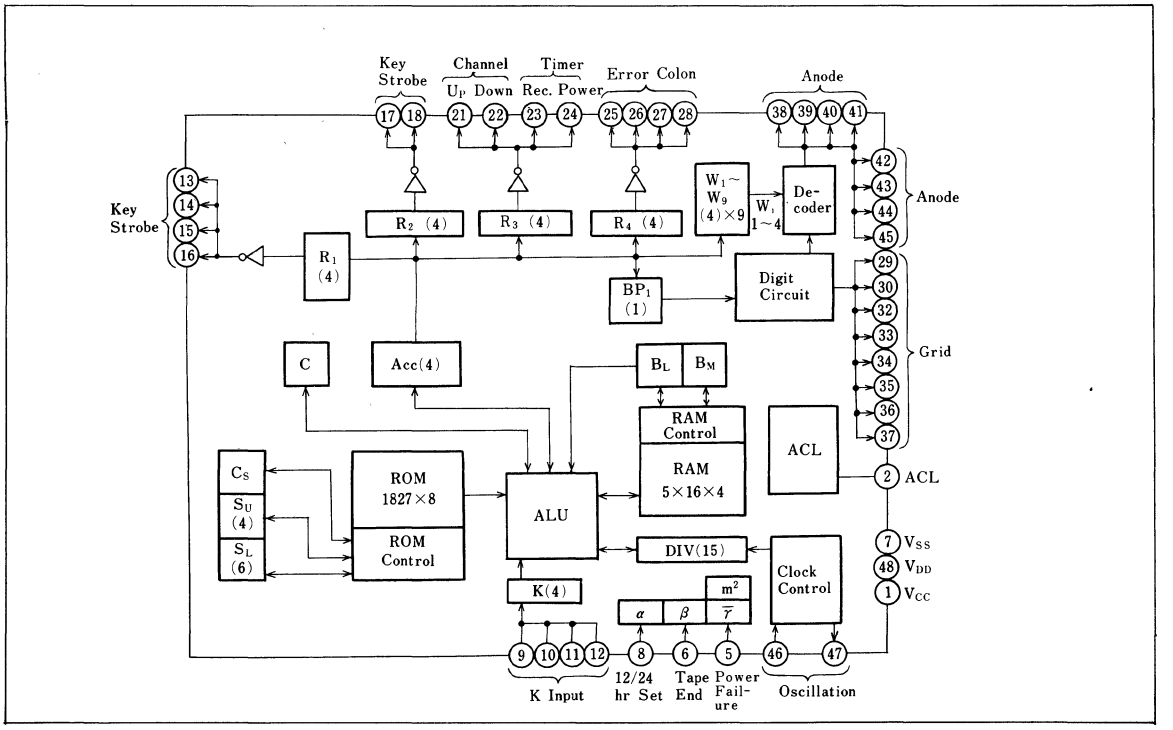
■ Features

1. "Hours-Minutes" display
2. Selectable 12/24 hr. format
3. Max. of 6 events 1 week
4. 6-daily and 1-weekly reservation
5. Directly drive a VFD
6. Time base : 32.768kHz crystal
7. Supply voltage : −5V
8. CMOS process
9. 48-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage *1	V_{DD}	+0.3～−7.0	V
Input voltage *1	V_{IN}	+0.3～V_{DD}−0.3	V
Output voltage *1,2	V_N	+0.3～−40	V
Operating temperature	T_{opr}	−10～+60	℃
Storage temperature	T_{stg}	−55～+150	℃

*1 Referenced to V_{SS}.
*2 Applies to R_{1-1}～R_{1-4}, D_1～D_8, S_a～S_h pins

■ Operating Conditions

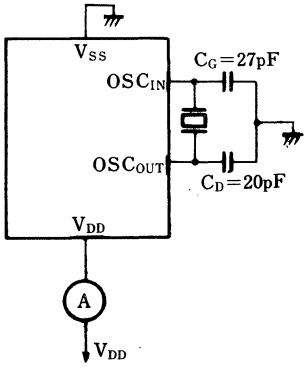
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage *1	V_{DD}	−5.5	−5.0	−4.5	V
Input voltage *1	V_{IN}	V_{DD}		0	V
Output voltage *1,2	V_N	−32			V

■ Electrical Characteristics

(V_{DD}=−5.0V±10%, V_N=−32V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		−0.5		0	V	1
	V_{IL}		V_{DD}		V_{DD}+0.5		
Input current	I_{IH1}	V_{IN}=0V			10	μA	2
	I_{IL1}	V_{IN}=V_{DD}	−1				
	I_{IH2}	V_{IN}=0V			5	μA	3
	I_{IL2}	V_{IN}=V_{DD}	−1				
	I_{IH3}	V_{IN}=0V			1	μA	4
	I_{IL3}	V_{IN}=V_{DD}	−5				
	I_{IH4}	V_{IN}=0V			4	μA	5
	I_{IL4}	V_{IN}=V_{DD}	−1				
Output voltage	V_{OH1}	I_{OH}=−6mA	−2.0			V	6
	V_{OL1}	R_L=120kΩ to V_N			V_N+1.2		
	V_{OH2}	I_{OH}=−12mA	−2.0			V	7
	V_{OL2}	R_L=120kΩ to V_N			V_N+1.2		
	V_{OH3}	I_{OH}=−2mA	−2.0			V	8
	V_{OL3}	R_L=120kΩ to V_N			V_N+1.2		
	V_{OH4}	I_{OH}=−3mA	−2.0			V	9
	V_{OL4}	R_L=120kΩ to V_N			V_N+1.2		
Oscillator frequency	f_{osc}			32.768		kHz	
Current consumption	I_{DD1}	No load, uniterrupted power condition			300	μA	10
	I_{DD2}	No load, interrupted power condition			40		

Note 1: Applies to Vcc, ACL, $\overline{T_1}$, $\overline{T_2}$, $\overline{\gamma}$, β, α, K_1～K_4 pins
Note 2: Applies to K_1～K_4 pins
Note 3: Applies to α, β pins
Note 4: Applies to Vcc, γ pins
Note 5: Applies to ACL pins
Note 6: Applies to S_a～S_h pins
Note 7: Applies to D_1～D_8, pins
Note 8: Applies to R_{1-1}～R_{1-4}, R_{2-1}～R_{2-4}
Note 9: Applies to R_{3-1}～R_{3-4}, R_{4-1}～R_{4-4}
Note 10: Test circuit (right figure)



■ Specifications

(1) Input keys and operations

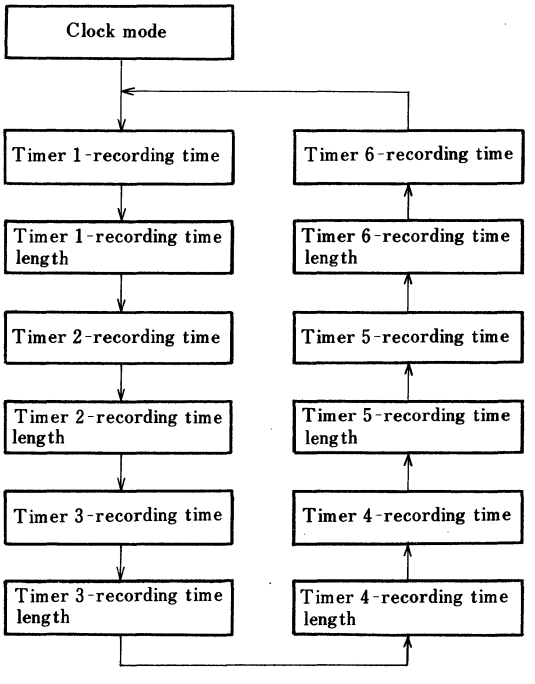
clock call	Timer call	Day	Hour	Min	Clear	
CH1	CH2	CH3	CH4	CH5	CH6	CH7
CH8	CH9	CH10	CH11	CH12	CH13	CH14

(i) Clock Call key

When to set the current time, depress the Day, Hour, and Min keys one after another while holding the key pressed. When both the Clock Call key and any one of the Day, Hour, and Min keys are released, the clock starts from 00 second. Depression of the Clock Call key in other mode (time set mode) causes the data that has been displayed on the fluorescent display tube stored and at the same time goes back into the clock mode.

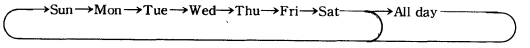
(ii) Timer Call key

This key is for calling the 6 timers in sequence. With each depression, this along with the symbol will be displayed on the fluorescent display tube in the order shown in the figure below. Only the data called by the Timer Call key to the fluorescent display tube can be altered in timer setting and clearing.



(iii) Day, Hour, Min key

To set the current time or set the timer, depress these keys to execute one by one the data being displayed on the fluorescent display tube. With each depression of these keys, the data gets renewed by 1. But if they are held pressed for longer than 0.5 second, the data gets renewed by 1 every 0.25 second.

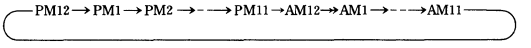


In current data setting, the Day key should be depressed 7 times to return to the origin. But in timer ON time setting, it should be depressed 8 times because of the additiona of "everyday".

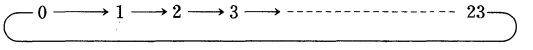
(iv) Data renewal by the Hour key

In current time setting or recording time setting, the data will be renewed in any of the following manners depending on whether the clock is under 12 hour system or 24 hour system.

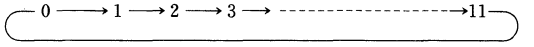
• Under 12 hour system



• Under 24 hour system

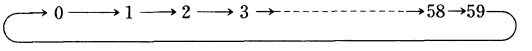


In recording time setting, the data is renewed in the following manner.



The recording time can be set to up to 11 hours and 59 minutes.

(v) Data renewal by the Min key



(vi) Clear key

This key is used to clear the data of the timer that is set. First depress the Timer Call key to call the timer then depress the Clear key to clear the stored data of the timer that was called to the flourescent display tube.

The recording time data can be cleared independently but if their recording start time is cleared, the recording time data of the same timer will also be cleared. This key has a function of stopping the execution of timer recording. In other words, while timer recording is being excuted, only this key along with the Timer Call key and the Clock key that are used to confirm the preset time can be accepted and clears in the clock mode only the data of the timer which is executing recording to bring it to a forced stop.

Simultaneous depression of any other key than the Clock Call cannot be accepted. A new key input cannot be recognized until all the keys are released.

(vii) **Other inputs**

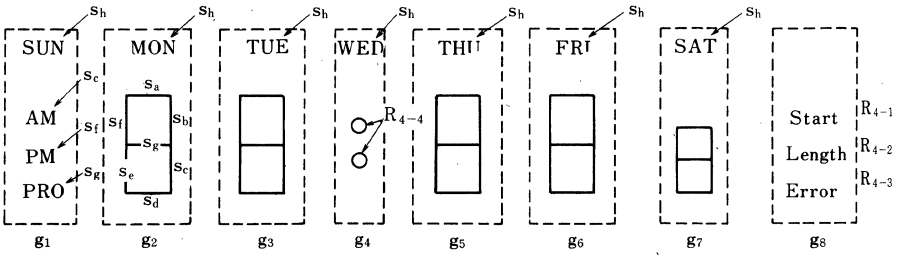
(a) 12 hour/24 hour swiching input

(b) Tape end input

This input gone "Low" is recognized as the tape end and causes the timer outputs T_P andT_R to go "Low" for the timer operation to come to an end. And unless this input is "High", tne timer output T_P and T_R will not go "High" even if the current time and the recording start time coincide in the clock mode.

(c) Power failure detect output

(2) Display and outputs



(i) **Display**

The clock has 12 hour system/24 hour system switching capability. Under the 12 hour system, AM/PM change-over occurs between 11 o'clock and 12 o'clock.

When the clock is under 24 hour system, so is the timer ON time. The display "PRO" indicates the time is set to the timer and lights up when setting.

The colon fashes 0.5 second ON and 0.5 second OFF while the clock is in operation. The character in the g_7 position indicates the timer number in recording start time setting and recording time setting. Error lights up when more than two timers overlap.

(ii) **Outputs**

The LR3472 has the following outputs.

Channel control output	2-bit C_U, C_D
Timer power output	1-bit T_P
Timer rec output	1-bit T_R

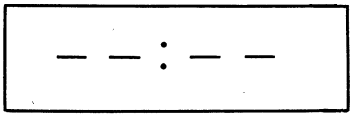
The channel control output is for controlling the channel selector IC. The timer output T_P goes "High" in recording start time and recording time setting. And in the clock mode, it goes "High" 1 minute before the recording start time. The timer output T_R in the clock mode goes "High" if the current time coincides with the timer ON time in the clock mode. Power failure causes all the displays to go blank and resets the output. When the power comes back on, the power failure indication will be displayed during the next 1 minute. If the power failure occurs while recording, T_P goes "High" (on channel 1 now) and another 1 minute later, T_R goes "High" (on the preset channel) to resume recording.

The power failure display is indicated by flashing 1 second ON and 1 second OFF. To stop the flashing, depress the Clock Call key.

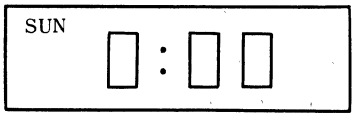
(3) Initial mode

- **CH1~CH14** key——Shift the channel by C_U, and C_D.
- **Clock Call** key ——For clock setting mode

Goes into this mode after auto clear is reset on power-up. This mode accepts only the CH1~CH14 keys and the Clock Call key for clock setting. Once the Clock Call key is deressed, timing of the clock, and timer operation are disabled. Timing cannot be performed until the clock is set.



Initial state display



Display after depression of the Clock Call key

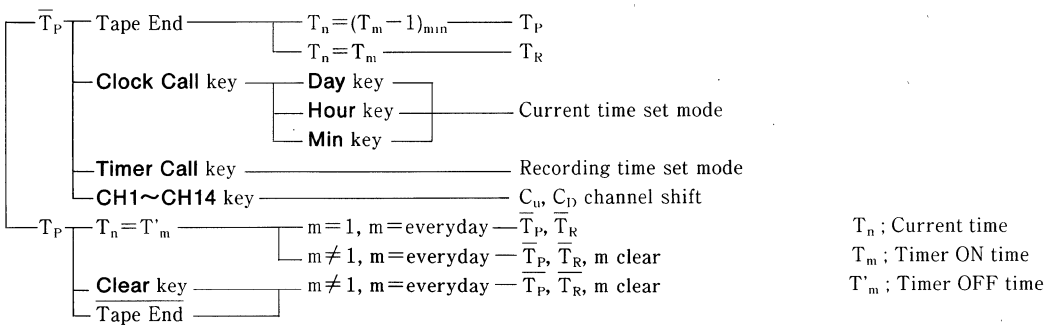
(Note) The colon is lit.

(4) Clock setting mode

- **Clock Call** key
  - **Day** key —— d+1 ⟶ d
  - **Hour** key —— h+1 ⟶ h
  - **Min** key —— m+1 ⟶ m
- **Clock Call, Day, Hour, Min** key

The LR3472 stays in this mode while the Clock Call key is held pressed. This mode accepts the Day, Hour, Min keys and allows for current time setting. Note that the minute digit does not increment the hour digit and the hour digit does not increment the day digit.

(5) Clock mode

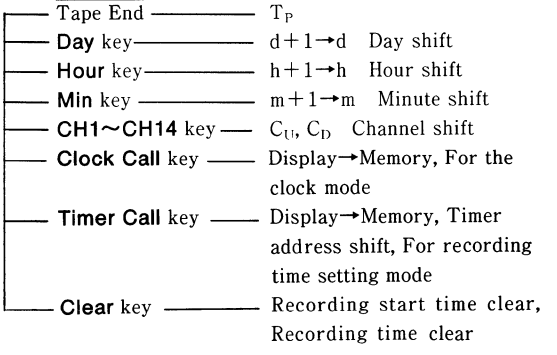


This mode is an ordinary timer operation mode in that the timer output T_P goes "High" 1 minute before the preset recording start time with the Tape End input "High" and when the current time coincides with the preset recording start time, the timer output T_R goes "High". Even when the current time reaches one minute before the preset recording start time or when it coincides with the recording start time, the timer outputs, T_P and T_R will not go "High", nor will preset content be cleared if the Tape End input is "Low".

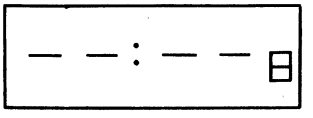
When the timer output T_P is "Low" (when timer recording is not being executed), if the Clock Call key and either of the Day, Hour, and Min key are depressed simultaneously to go into the current time setting mode, the current time can be adjusted. And when the timer recording is not being executed with the T_P "Low", the Timer Call key is depressed to go into the recording start time setting mode to allow what is now being displayed to be the recording start time and the preset channel for the timer 1. On reaching the time where there is no recording time left with the timer output T_R "High" (when timer recording is being executed), the timer outputs T_P and T_R go "Low" to have the corresponding memory content to be cleared except in the case that the memory content for the corresponding time happens to be "every day" and the corresponding timer happens to be the No.1 timer. This indicates that the timer 1 is preset for every week.

If either the Clear Key is depressed or the Tape End input goes "Low" with output T_P "High" (when timer recording is being executed), the timer outputs T_P and T_R go "Low" to have the memory content for the corresponding timer to be cleared except in the case that the preset content for the corresponding timer happens to be "every day" and the corresponding timer happens to be the No.1 timer. The CH1~CH14 keys can be accepted for the channel signal to be generated, while the timer output T_P is "Low".

(6) Recording start time set mode



This mode is the recording start setting time mode. The display in the state in which the called timer has been cleared or in which the non-set timer has been called is shown as below.



Day digits are all OFF.
The timer number is that of the timer called. (1~6)
The colon is flashing.

Timer display when the preset is cleared

The channel is set initially to channel 1. This can be adjusted by the CH1~CH14 keys. The CH1~CH14 keys and Day, Hour, and Min keys can be depressed in any order and if unnecessary need not be depressed at all.

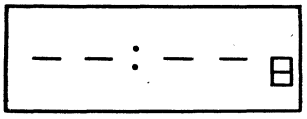
To exit for the mode in which to set recording time for the same timer, depress the Timer Call key. In which case the timer output T_P remains "High". In this mode, the recording time memory for the same timer will be cleared on depression of the clear key. This mode disables timer recording.

10

(7) Recording time set

$\overline{\text{Tape End}}$	T_P
Hour key	h+1→h Hour shift
Min key	m+1→m Minute shift
Clear key	Recording time clear
Clock Call key	Display→Memory, For the clock mode
Timer Call key	Display→Memory, Timer address shift. For recording time set mode

This mode is the mode in which to set the recording time. The display in the state in which the recording timer for the called timer has been cleared and in which the not-set timer has been called is shown as below.



The day digits are all OFF.
The timer number (1~6) displayed is that of the timer called.
The colon is flashing.

This mode does not respond to depression of any of the Day key, and CH1~CH14 keys. If not required, the recording time setting procedure by the Hour and Min key can be skipped so that the Clock Call key and the Timer Call key may be operated to proceed to the next step. If timer recording is attempted with the recording time cleared, either the Tape End signal goes "Low" or the recording will continue until the timer recording gets interrupted by the Clear key.

With the recording time set to 00 hour 00 minute, the T_P goes "High" 1 minute before the recording start time, but on reaching the recording start time, the T_P and T_R go "Low" to disable recording. In this mode, the T_P goes "Low" on transition by the Clock Call key to the clock mode. By the Timer Call key, this is the same operation as the recording start time setting for the next timer.

This mode disable timer recording.

(8) Others

(i) Error indication

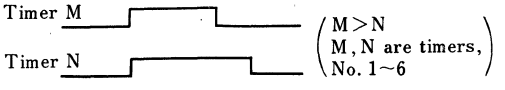
The error indication lights up when more than 2 of the preset timer contents overlap and the numbers overlapped will be alternately displayed as in the example.

(Example) When the timer No.1, No.2, and No.3 overlap
1→2→3→1→2→3→·····

Note that more than 2 sets of overlaps cannot be distinguished from each one of the sets.

If the recording time is not set, overlapped preset times give no error display.

Error indication does not prevent transition to the program that starts halfway through.

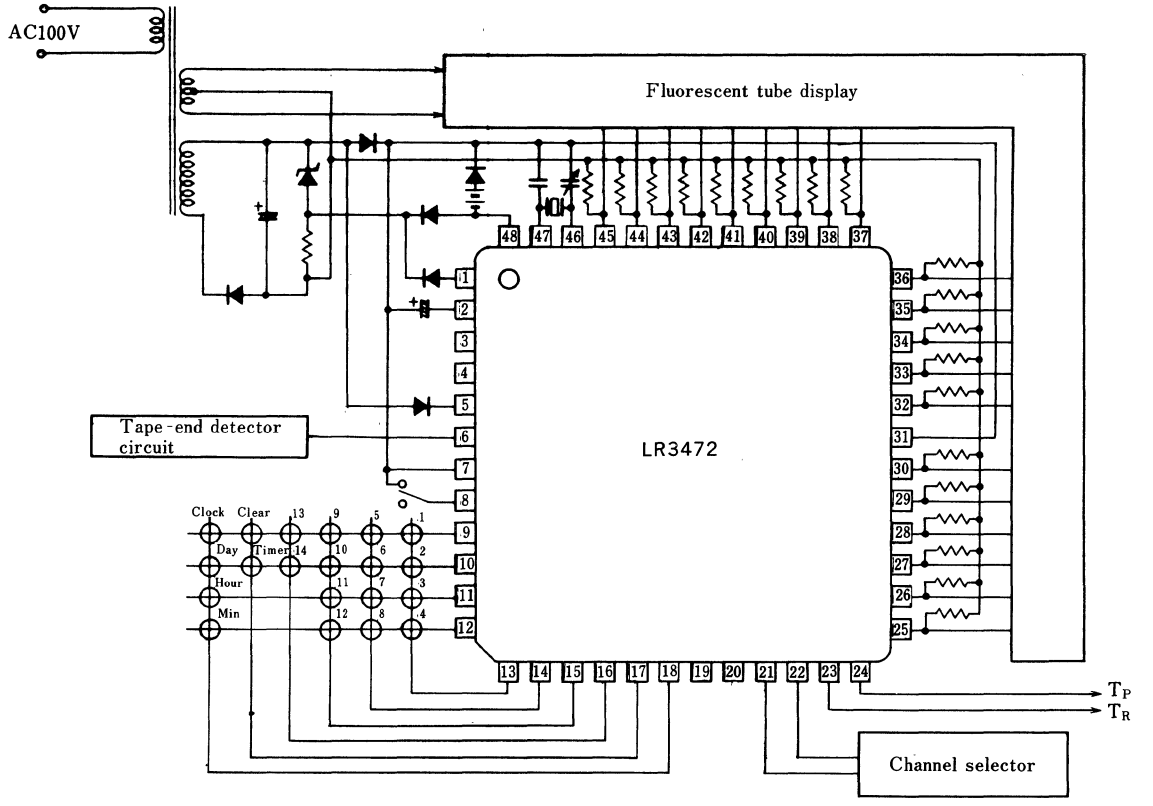


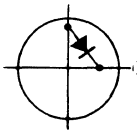
In the figure above, the timer M is the first to be executed. In which case the memory for the timer M gets cleared on completion of the timer M recording. The timer N completes recording the following week to be cleared.

(ii) Preset for the second week

If the current time is already past the recording start time, it is considered as the preset time for one week away.

■ System Configuration





R_{1-i} (i=1~4), R_{2-j} (j=1~2)

LR3715M Remote Control Transmitter CMOS LSI

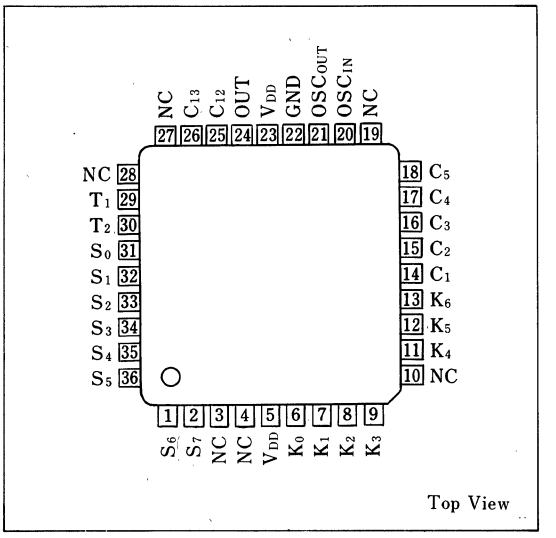
■ Description

The LR3715M is a CMOS LSI developed for use in infrared remote control transmitters.

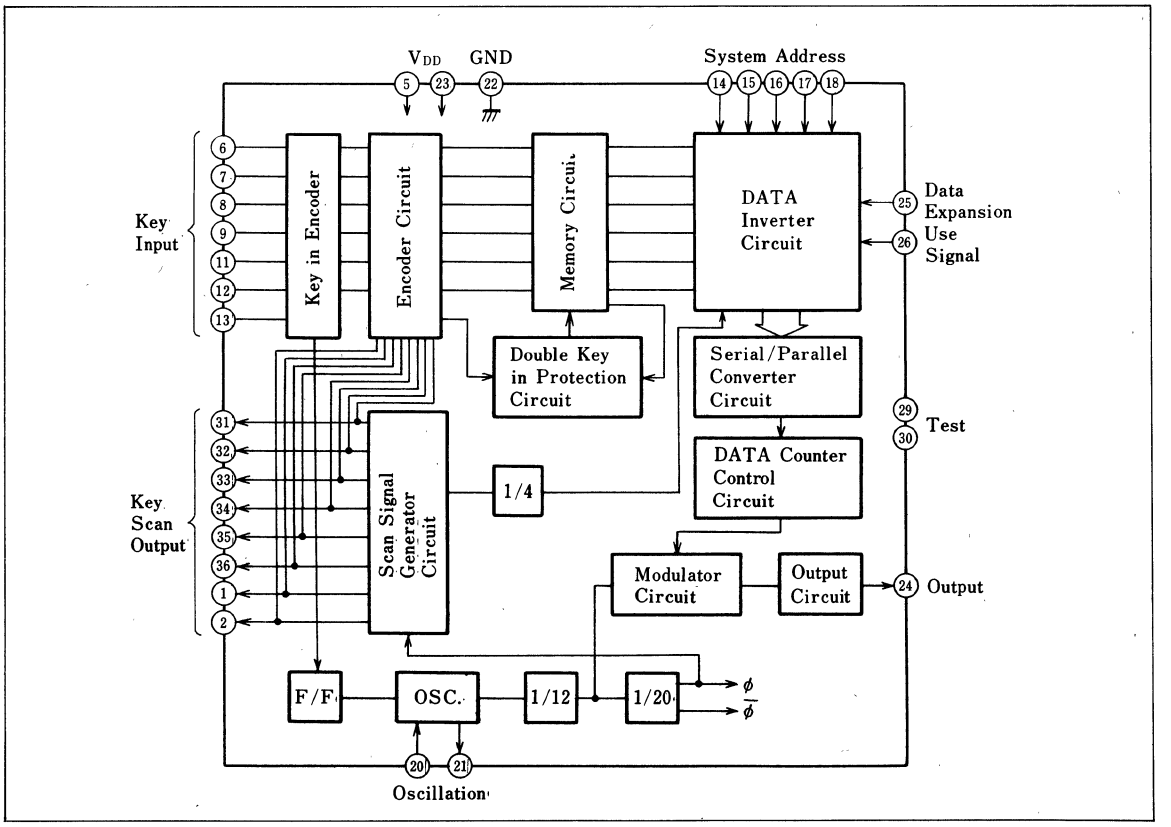
■ Features

1. 56-channel of data can be transmitted
2. Transmission code : PPM
3. Time base : 455kHz ceramic oscillator
4. Supply voltage : 3V
5. CMOS process
6. 36-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit	Note
Supply voltage	V_{DD}	Referenced to GND	−0.3～+6	V	
Input voltage	V_{IN}	Referenced to GND	−0.3～+6	V	
Supply current	I_{DD}, I_{EE}		±5	mA	1,2
Output current	I_{OUT}		±2	mA	2
Power consumption	P_D	Ta=25℃	483	mW	
Operating temperature	T_{opr}		−20～+70	℃	
Storage temperature	T_{stg}		−50～+125	℃	

Note 1: I_{DD} refers to the current that flows into the V_{DD} pin; I_{EE} refers to the current draining from the GND pin.
Note 2: The direction of current flowing into the device is defined as positive: that draining from the device is defined as negative. This definition is also applied to the electrical characteristics.

■ Recommended Operating Conditions

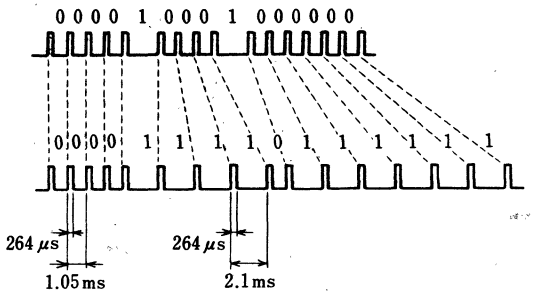
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	Referenced to GND	2.2	3	3.3	V
Input voltage	V_{IN}	Referenced to GND	0		V_{DD}	V
Oscillator frequency	fosc			455		kHz

■ Electrical Characteristics

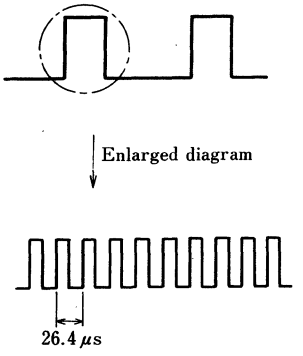
(V_{DD}=3V, Ta=25℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}			2.2	3	3.3	V	3
Current consumption	I_{DD}	All input pins open	fosc oscillated			0.5	mA	3
			fosc stopped			1	μA	
Input voltage	V_{IN}			V_{DD}−0.6		V_{DD}	V	4
	V_{IL}			0		0.6	V	5
Input current	I_{IH1}	V_{IN}=V_{DD}				1	μA	4
	I_{IL1}	V_{IN}=GND				−1		
	I_{IH2}	V_{IN}=V_{DD}				1	μA	5
	I_{IL2}	V_{IN}=GND				−150		
Output voltage	V_{OH1}	I_{OH}=−5 μA		V_{DD}−0.4		V_{DD}	V	6
	V_{OL1}	I_{OL}=400 μA		0		0.4		
	V_{OH2}	I_{OH}=−0.5mA		V_{DD}−0.4		V_{DD}	V	7
	V_{OL2}	I_{OL}=1mA		0		0.4		
Oscillator frequency	fosc				455		kHz	8
Feedback resistor	R_{fb}			1		5	MΩ	

Note 3: Applied to pin V_{DD}.
Note 4: Applied to pins C_1-C_5, C_{12}, C_{13}
Note 5: Applied to pins K_0-K_6, T_1, T_2
Note 6: Applied to pins S_0-S_7.
Note 7: Applied to pin OUT
Note 8: Applied to pin OSC_{IN}, OSC_{OUT}



④ Modulator circuit While it is possible to transmit serial 15-bit PPM signals directly, it causes the broadening of occupied bandwidth. To prevent this, the device samples the 15-bit PPM signa with a 37.9 kHz (When fo = 455 kHz) signal and transmits PPM signal at 100% amplitude modulation.



(3) Precautions in preparing a receiver

① Make sure that the non-inverse and inverse signals are transmitted alternately. Be sure to verify that bit number 15 (K) is alternately set to "1" and "0". It is not enough only to compare bits C_6-C_{14} either after inverting them or before inverthing them.

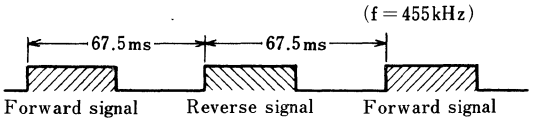
② The PPM signal status "1" or "0" may be identified by checking its pulse interval as follows (fo = 455 kHz):

$T_P < 0.42$ ms ... Non-PPM signal
$0.42 \text{ ms} \leqq T_P < 1.69$ ms ... "0"
$1.69 \text{ ms} \leqq T_P < 3.37$ ms ... "1"
$3.37 \text{ ms} \leqq T_P$ ... Non-PPM signal

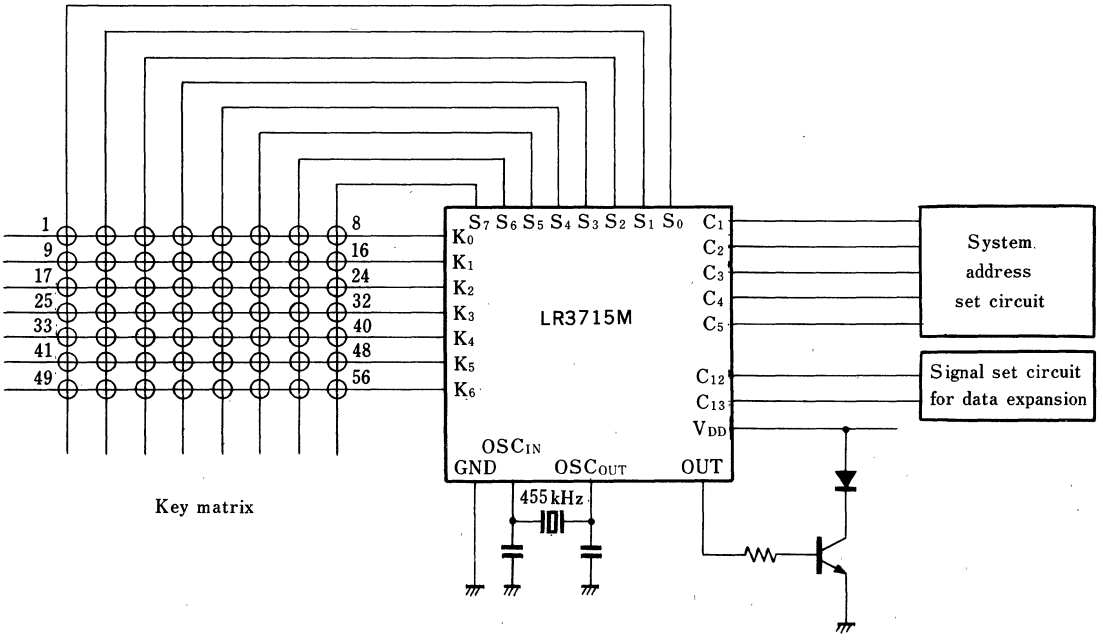
If a non-PPM signal is received, the device clears all bits and begins processing with the first bit again.

③ If 16 bits (17 pulses) or more of PPM signal are received, the device identifies it as a non-PPM signal, clears all bits, and begins processing with the first bit again.

④ The correct data should be identified by matching the system addresses and data expansion bits of the transmitter and receiver.



■ System Configuration



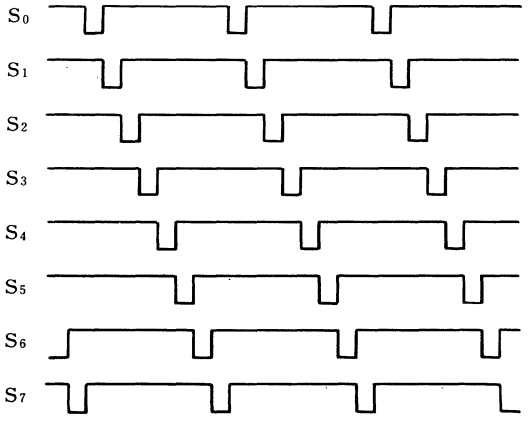
As shown in the above figure, the non-inverse and inverse signals alternately repeat in series at a certain interval. The receiver reconstructs the original data by identifying non-inverse or inverse signal according to the status of the data judging bit.

⑤ Mask bit C_{14} Fixed at "0" (low) within the device

(2) Device operation timing

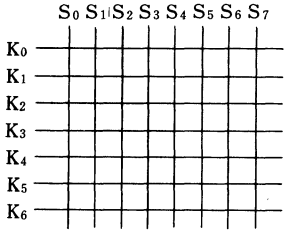
The LR3715M is a transmitter LSI device designed for use in an infrared remote control unit. It consists of an oscillator, key scan signal generator. key encoder, memory, data inverter, parallel/serial converter, and output circuit. The device can accept a 7x8 key matrix and transmit up to 56 types of commands in 6-bit code. For power saving, the internal oscillation is stopped when no key is pressed. If double key operation is made, the device stops transmission.

① Key scan signal generator When a key entry is made, a flip-flop reverses its status to reset the Oscillation Clear signal and start internal oscillation. The key scan outputs provide the signals shown below. Given fo = 455 kHz, the pulse period is 33.8 ms, and pulse width is 4.2 ms.



② Key encoder, encoder, and memory The key scan signal lines are combined with key input lines, K_0-K_6, to produce a 7x8 key matrix external to the device. The K_0-K_6 input pins have built-in pull-up resistors.

If a key at the matrix point, K_1-S_3, is pressed, the signal output at pin S_3 is input to pin K_1, to be encoded into a 6-bit binary code by the key encoder and encoder before storage into memory. If two keys are pressed at the same time, the double key prevention logic clears the data in the pertinent location of the memory. The following table shows the key arrangement and command numbers. If one desires to transmit command number 3, the key at the matrix point, K_0-S_2, can be pressed.



		Scan signal							
		S0	S1	S2	S3	S4	S5	S6	S7
Key input	K0	1	2	3	4	5	6	7	8
	K1	9	10	11	12	13	14	15	16
	K2	17	18	19	20	21	22	23	24
	K3	25	26	27	28	29	30	31	32
	K4	33	34	35	36	37	38	39	40
	K5	41	42	43	44	45	46	47	48
	K6	49	50	51	52	53	54	55	56

③ Data inverter If the 6-bit data is identified to be correct, it is transferred to the data inverter, where system address, data expansion bit, mask bit, and data judging bit are added to it to generate 15-bit data.

If the data judging bit is zero, the following data will be produced in the data inverter.

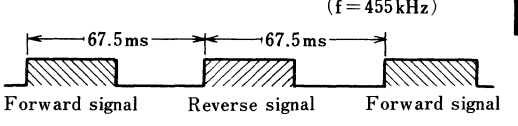
(Example) When the key numbered 8 is pressed:

C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	K
0	0	0	0	1	0	0	0	1	0	0	0	0	0	0

If the data judging bit is "1", the data except for the system address, is inverted by the inverter.

C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	K
0	0	0	0	1	1	1	1	0	1	1	1	1	1	1

The parallel 15-bit signal is then converted into serial PPM signal by the parallel/serial converter.



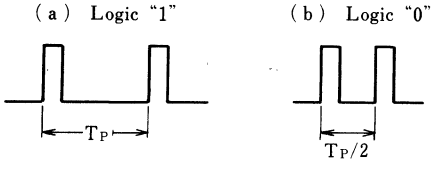
■ Function

(1) Transmission scheme

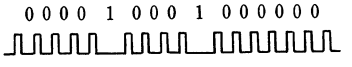
The LR3715M uses the PPM (pulse position modulation) system for 15-bit signal.

The device alternately transmits non-inverted 15-bit data and inverted 15-bit data (system-address bit 5 is not inverted, however) . The receiver re-inverts the inverted data into the original form and compares it with the preceding non-inverted data to be sure the two pieces of data are identical. Discrimination between inverted and non-inverted is achieved by checking the judging bit. Reception becomes valid only after the data pieces prove identical.

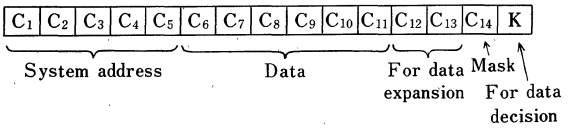
The PPM system arranges pulses as follows to discriminate logic "1" from "0".



If the interval between two pulses is T_P, the signal is identified to be logic "1", whereas if it is $T_P/2$, the signal is identified to be "0". the device thus constructs 15-bit serial data as follows. For example, a binary code "000010001000000" is converted into a pulse array as follows:



The following shows bit assignments to data:



① System address C_1-C_5 These bits are set up with switch and allocated to different system. Up to 56 types of commands and two expansion bit can be transmitted for each system. For system address allocation, be sure to contact us.

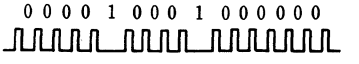
② Data code C_6-C_{11} The Data code C_6-C_{11} are allocated to key numbers as shown in the following table:

CH	C_6	C_7	C_8	C_9	C_{10}	C_{11}	CH	C_6	C_7	C_8	C_9	C_{10}	C_{11}
1	1	0	0	0	0	0	29	1	0	1	1	1	0
2	0	1	0	0	0	0	30	0	1	1	1	1	0
3	1	1	0	0	0	0	31	1	1	1	1	1	0
4	0	0	1	0	0	0	32	0	0	0	0	0	1
5	1	0	1	0	0	0	33	1	0	0	0	0	1
6	0	1	1	0	0	0	34	0	1	0	0	0	1
7	1	1	1	0	0	0	35	1	1	0	0	0	1
8	0	0	0	1	0	0	36	0	0	1	0	0	1
9	1	0	0	1	0	0	37	1	0	1	0	0	1
10	0	1	0	1	0	0	38	0	1	1	0	0	1
11	1	1	0	1	0	0	39	1	1	1	0	0	1
12	0	0	1	1	0	0	40	0	0	0	1	0	1
13	1	0	1	1	0	0	41	1	0	0	1	0	1
14	0	1	1	1	0	0	42	0	1	0	1	0	1
15	1	1	1	1	0	0	43	1	1	0	1	0	1
16	0	0	0	0	1	0	44	0	0	1	1	0	1
17	1	0	0	0	1	0	45	1	0	1	1	0	1
18	0	1	0	0	1	0	46	0	1	1	1	0	1
19	1	1	0	0	1	0	47	1	1	1	1	0	1
20	0	0	1	0	1	0	48	0	0	0	0	1	1
21	1	0	1	0	1	0	49	1	0	0	0	1	1
22	0	1	1	0	1	0	50	0	1	0	0	1	1
23	1	1	1	0	1	0	51	1	1	0	0	1	1
24	0	0	0	1	1	0	52	0	0	1	0	1	1
25	1	0	0	1	1	0	53	1	0	1	0	1	1
26	0	1	0	1	1	0	54	0	1	1	0	1	1
27	1	1	0	1	1	0	55	1	1	1	0	1	1
28	0	0	1	1	1	0	56	0	0	0	1	1	1

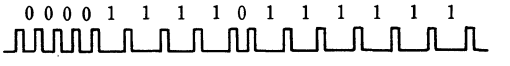
③ Data expansion bits C_{12}, C_{13} These bits are used to increase available command types.

④ Data judging bit K This bit K is unique to Sharp's remote control system, and is used to indicate whether the preceding data is inverted or non-inverted:

(a) Non-inverted data



(b) Inverted data



When the data judging bit is set to zero, the device transmits non-inverted data. When it is set to one, the device transmits inverted data (inversion of C_6-C_{14} and K) .

LU59001 Remote Control Receiver CMOS LSI

■ Description

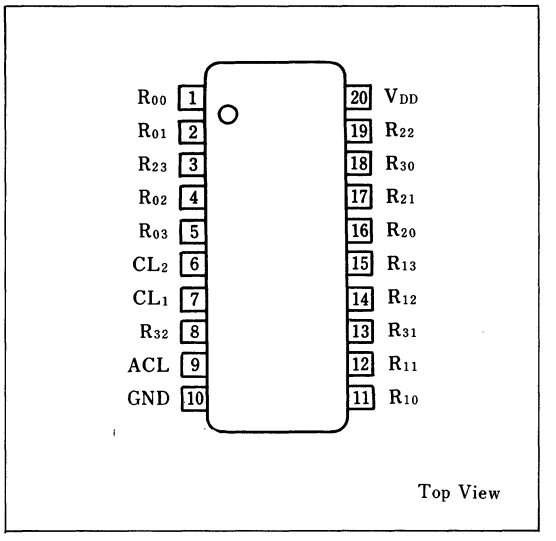
The LU59001 is a CMOS LSI developed for infrared remote contorol receivers.

Used together with the LR3715M transmitter, a remote control system can easily be realized.

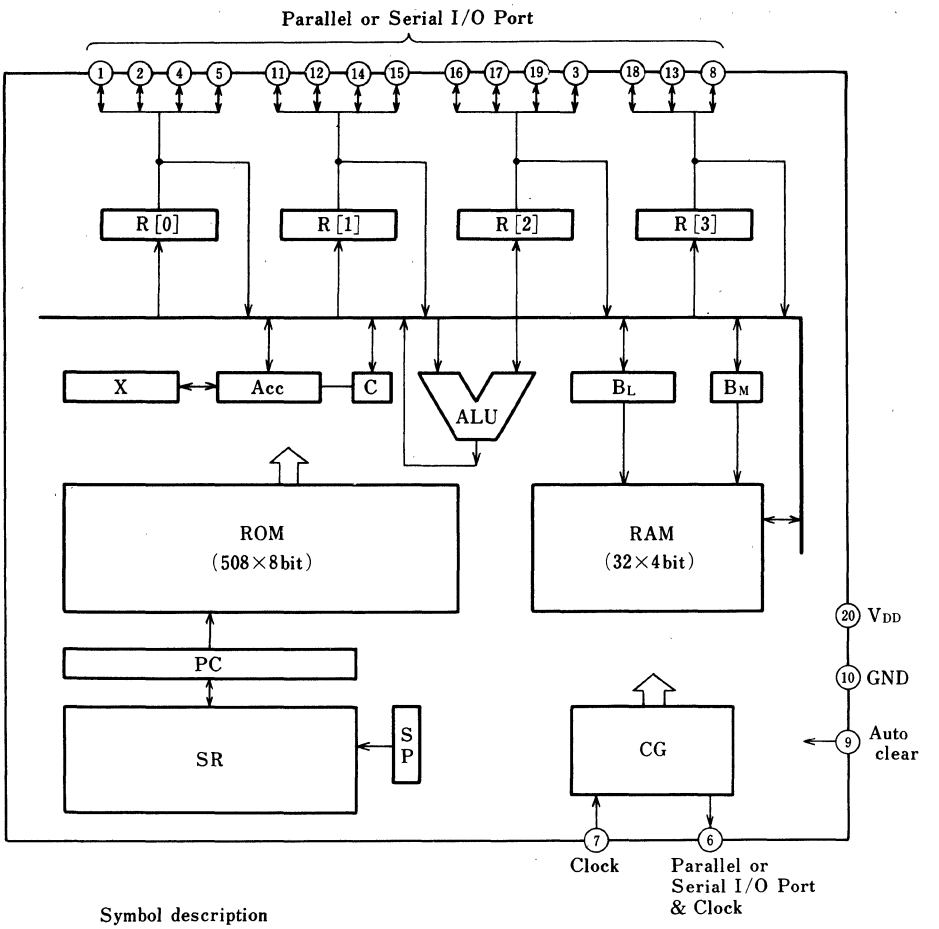
■ Features

1. 56-channel of data can be recognized
2. The serial or parallel data can be transfered to the external system
3. Time base : 455kHz ceramic oscillator
4. CMOS process
5. 20-pin dual-in-line package

■ Pin Connections



■ Block Diagram



Symbol description

Acc	: Accumulater	C	: Carry F/F
B_L, B_M	: RAM address register	PC	: Program counter
CG	: Clock generator	ALU	: Arithmetic logic unit
SR	: Stack register	SP	: Stack pointer
X	: Temporary register	R [0] ~ R [3]	: Output latch

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3~+7.5	V	
Input voltage	V_{IN}	−0.3~V_{DD}+0.3	V	
Output voltage	V_{OUT}	−0.3~V_{DD}+0.3	V	
Output current	I_{OH}	120	mA	1
	I_{OL}	20	mA	2
Operating temperature	T_{opr}	−10~+70	℃	
Storage temperature	T_{stg}	−55~+150	℃	

Note 1: Total output high current.
Note 2: Total output low current.

■ Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.7		5.5	V
Command execution time	t	V_{DD}=5V±10%	2		50	μs
		V_{DD}=3V±10%	4		50	

■ AC Characteristics of External Clock Input Signal

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input rise time	t_R	V_{DD}=2.7~5.5V			0.1	μs
Input fall time	t_F	V_{DD}=2.7~5.5V			0.1	μs
Clock pulse width	t_L	V_{DD}=5V±10%	0.2		6.3	μs
	t_H	V_{DD}=3V±10%	0.4		6.3	μs

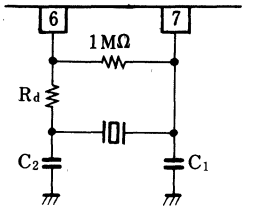
■ Electrical Characteristics

(V_{DD}=2.7V±5.5%, Ta=−10~+70℃)

Paramater	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		0.7V_{DD}		V_{DD}	V	3
	V_{IL1}		0		0.3V_{DD}	V	3
	V_{IH2}		V_{DD}−0.5		V_{DD}	V	4
	V_{IL2}		0		0.5	V	4
Input current	I_{IH1}	V_{IN}=V_{DD}, V_{DD}=5V±10%	70	250	750	μA	7
		V_{IN}=V_{DD}, V_{DD}=3V±10%	15	70	200	μA	8
	I_{IH2}	V_{IN}=V_{DD}, V_{DD}=5V±10%		20	60	μA	5
		V_{IN}=V_{DD}, V_{DD}=3V±10%		7	20	μA	5
Output current	I_{OH1}	V_{DD}=5V±10%, V_{OH}=V_{DD}−2V	10			mA	6
		V_{OH}=V_{DD}−0.5V	1			mA	7
	I_{OL1}	V_{DD}=5V±10%, V_{DD}=0.4V	1.6			mA	6
		V_{OL}=0.4V	0.8			mA	6
	I_{OH2}	V_{DD}=5V±10%, V_{OH}=V_{DD}−2V	4			mA	8
		V_{OH}=V_{DD}−0.5V	0.5			mA	8
	I_{OL2}	V_{DD}=5V±10%, V_{OL}=0.4V	15			μA	7
		V_{OL}=0.4V	8			μA	8
	I_{OH3}	V_{DD}=5V±10%, V_{OH}=V_{OH}=V_{DD}−2V	1			mA	9
		V_{OH}=V_{DD}−0.5V	0.15			mA	9
	I_{OL3}	V_{DD}=5V±10%, V_{OL}=0.4V	0.6			mA	9
		V_{OL}=0.4V	0.3			mA	9
Current consumption	I_{OP}	t=8,8 μs, V_{DD}=5V±10%		230	600	μA	10
		t=8.8 μs, V_{DD}=3V±10%		120	230	μA	10

Note 3: Applied to pins R_{03}, R_{10}–R_{13}, R_{20}–R_{23}, R_{30}–R_{32}.
Note 4: Applied to pins ACL, CL_1.
Note 5: Applied to pin ACL.
Note 6: Applied to pins R_{00}–R_{02}.
Note 7: Applied to pin R_{03}.
Note 8: Applied to pins R_{20}–R_{23}.
Note 9: Applied to pin CL_2.
Note 10: No load status.

■ Oscillator Circuit



Example using CSB455E (Murata)

$C_1=C_2=220pF$

$R_d=2.2k\Omega$

■ Switching Characteristics (OSC Frequency: 455 kHz)

(1) Receive signal (DIN)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Receive signal pulse width	t_{DIN}	250			μs

(2) Serial transfer (with internal clock)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
RDY ON time	t_{ON}			2	ms	
RDY OFF time (DIN→RDY)	t_{OFF1}	53			ms	
RDY OFF time (SDO→RDY)	t_{OFF2}	53			ms	
Duration of CKI at high	t_{CKIH}	1			ms	
CKI end time	t_{CKIE}	0			ms	
CKI standby time	t_{CKIS1}			52	ms	
CKO delay time	t_{CKOD}			635	μs	
Duration of CKO at high	t_{CKOH}			285	μs	
Duration of CKO at low 1	t_{CKOL1}			80	μs	11
Duration of CKO at low 2	t_{CKOL2}			825	μs	12
CKO setup time	t_{STOP1}			95	μs	

Note11: For transfer rate of 0.32 ms/bit.
Note12: For transfer rate of 1.05 ms/bit.

(3) Serial transfer (with external clock)

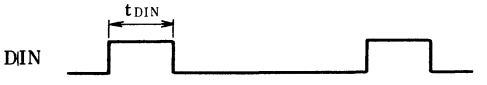
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
RDY ON time	t_{ON}	2.25			ms
RDY OFF time (DIN→RDY)	t_{OFF1}	53			ms
RDY OFF time (SDO→RDY)	t_{OFF2}	53			ms
CKI standby time	t_{CKIS2}	0.45		52	ms
Duration of CKI at high	t_{CKIH}	635			μs
Duration of CKI at low	t_{CKIL}	380			μs
CKI setup time	t_{STOP2}	255			μs
CKI clock frequency	f_{CKI}	100		920	Hz

(4) Parallel transfer

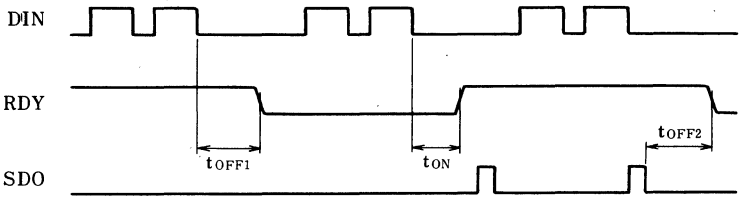
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Data ON time	t_{PDON}			2.65	ms
Data OFF time	t_{PDOFF}	53			ms

■ Timing Diagrams

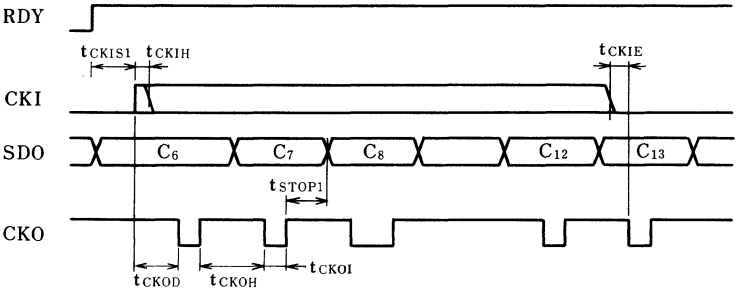
(1) Receive signal (DIN)



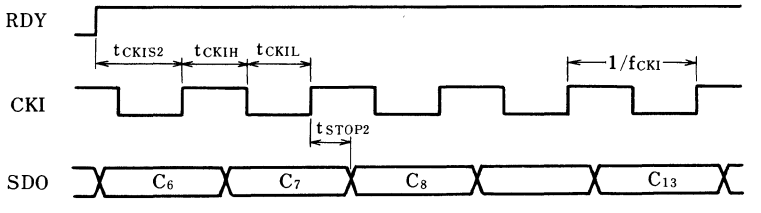
(2) RDY ON/OFF timing



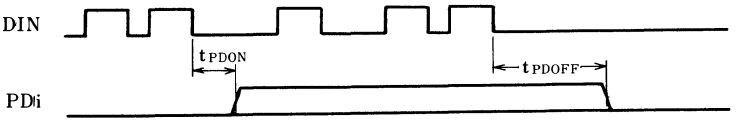
(3) Serial transfer (with internal clock)



(4) Serial transfer (with external clock)



(5) Parallel transfer



■ Functions

(1) Operation

The LU59001 is designed for 15-bit PPM signal reception. For more information, see the description of the LR3715M Remote Controller Transmitter. The LU59001 basically consists of a decoder which decodes PPM signal into binary data, formatter, system address check logic, and data transfer block.

(2) Decoder

Received signal (DIN) is converted into binary code according to the conditions shown in the following table. If an interval, T_P, between pulses is in the range of 2.95 ms $\leqq T_P \leqq$ 52.7 ms, it is identified as a separator between 15-bit data items. If T_P is equal to or larger than 52.7 ms, it is identified as the end of transmission.

Conditions	Identification
$T_P \leqq$ 0.85ms	Noise
0.85ms $\leqq T_P \leqq$ 1.69ms	Logic "0"
1.69ms $\leqq T_P \leqq$ 2.95ms	Logic "1"
2.95ms $\leqq T_P \leqq$ 52.7ms	End of 15-bit data
52.7ms $\leqq T_P$	End of transmission

OSC frequency: 455 KHz

(3) Coincidence judgment

When the device starts reception, it checks the system address and mask bit, and performs coincidence check on inverted and non-inverted data. It first checks if the received system address, C_1-C_5, matches the preset system address (SYS_1-SYS_5), and verifies that the mask bit is "0". Next the device checks coincidence of a non-inverted data item with its inverted counterpart.

If concidence is found, the device becomes ready for data transfer (C_6-C_{13}) to an external system. If coincidence is not found, comparison is made with the preceding or succeeding 15 bit data. Comparison is repeated until coincidence is not found. Once the device starts data transfer it no longer decodes subsequently received data.

(4) Data transfer

Data transfer formats include serial and parallel transfer. If the R_{03} and R_{22} pins are both connected to V_{DD}, serial transfer is selected when the device is reset. In any other case, parallel transfer is selected when the device is reset.

① Serial transfer

Serial transfer includes three modes. A mode is selected by the S_1 and S_2 signals applied to the R_{20} and R_{21} pins. The following table shows the modes versus S_1 and S_2 signals ($S_1=S_2=1$ is inhibited):

S_2	S_1	Transfer mode	Transfer rate	R_{01}(CKO)	R_{23}(CKI)
0	0	Internal Clock Mode	0.32ms/bit	Transfer Clock	Request to transmit signal
0	1		1.05ms/bit		
1	0	External Clock Mode	1.1~10ms /bit	High	Transfer clock

OSC frequency: 455 KHz

(a) Internal Clock mode If a Request to Transmit signal (CKI) is applied to the R_{23} pin when the device is in data transfer mode, it starts data transfer sequence. The R_{00} pin outputs serial data (SDO) in the order of C_6, C_7, ···, C_{13}, and the R_{01} pin provides a transfer clock (CKO). In the Internal Clock mode a transfer rate from 0.32 ms/bit to 1.05 ms/bit can be selected using the Mode Select signals S_1 and S_2.

(b) External Clock mode If an external transfer clock (CKI) is applied to the R_{23} pin when the device is in the data transfer mode, it starts serial data transfer. The R_{00} pin outputs serial data (SDO) in the order of C_6, C_7,···C_{13} in synchronicity with the external clock. The allowable transfer rate is limited to 1.1 to 10 ms/bit.

② Parallel transfer

When the device enters the data transfer mode, pins R_{00}, R_{01}, R_{02}, R_{03}, R_{20}, R_{21}, R_{22}, and R_{23} output parallel data (PD_0-PD_7). Parallel data bits correspond to received data bits as follows:

Pin	R_{00}	R_{01}	R_{02}	R_{03}	R_{20}	R_{21}	R_{22}	R_{23}
Parallel Data	PD_0	PD_1	PD_2	PD_3	PD_4	PD_5	PD_6	PD_7
Received Data	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}

③ Data transfer mode

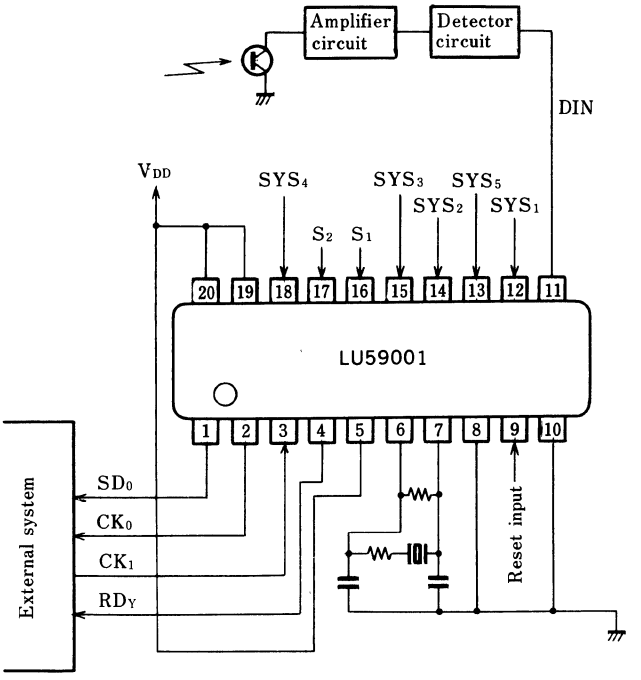
When the device completes decoding and coincidence check on received data, it enters the data transfer mode. Entry into the serial data transfer mode is indicated by the RDY signal appearing at the R_{02} pin.

That into the parallel data transfer mode is indicated by the OR output of the parallel data (PD_0-PD_7) (all bits of parallel data are not set at '0' at the same time).

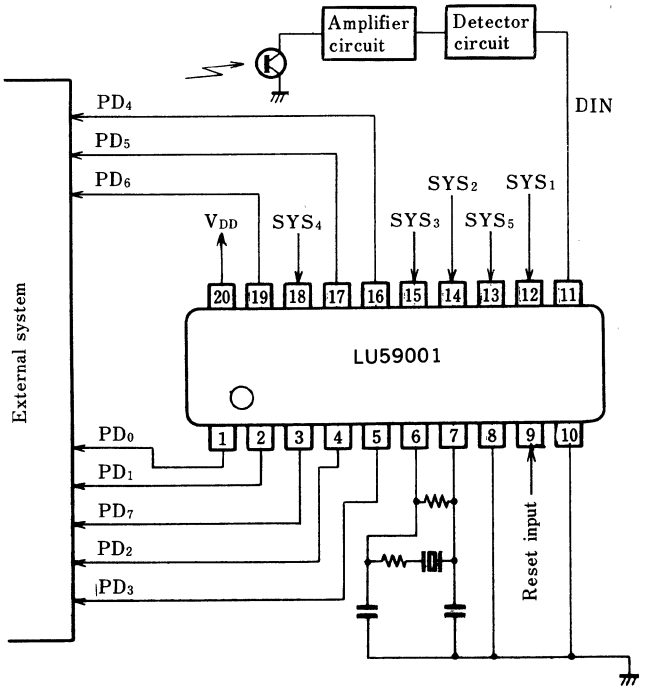
The data transfer mode continues until all data has been transferred or for 52.7 ms after serial data transfer has been completed. After that, the device waits for data reception.

■ System Configuration

(1) Serial transfer



(2) Parallel transfer



LR3617 Up / Down Counter CMOS LSI with LCD Decoder-Driver

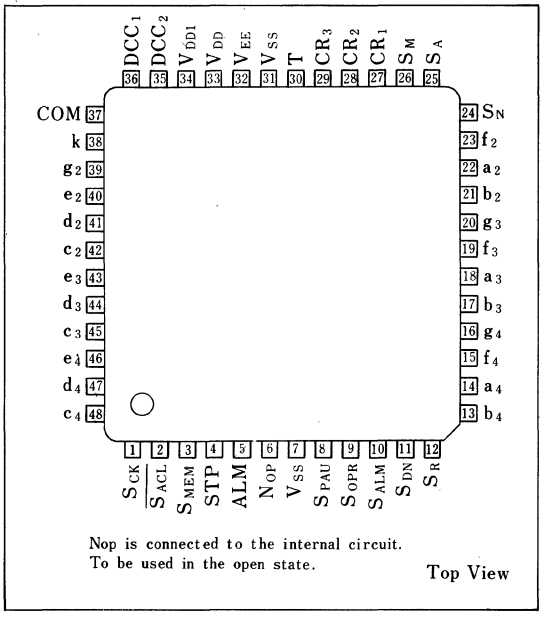
■ Description

The LR3617 isan up/down counter with a decoder driver for $3^1/_2$ digit LCDs. It is best suited to tape counters for use in micro cassette tape recorders and VTRs.

■ Features

1. $3^1/_2$ digit static LCD
2. Leading zero suppression
3. Minus sign floating position
4. Memory stop
5. End-of-tape stop
6. Single power supply : − 1.5V
7. CMOS process
8. 48-pin quad-flat package

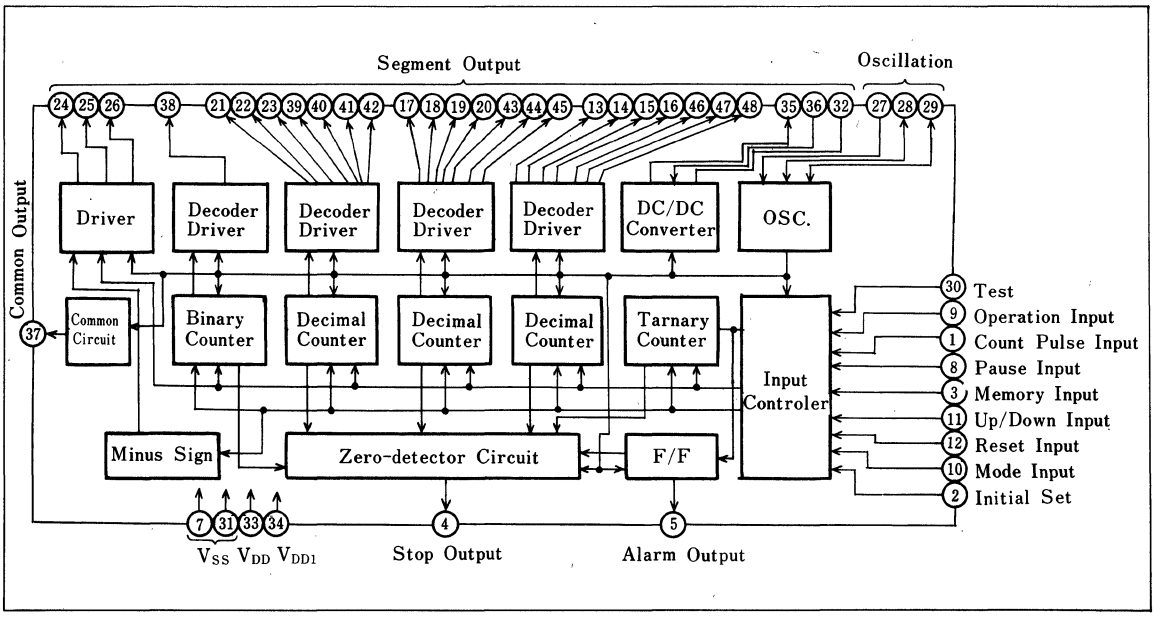
■ Pin Connections



Nop is connected to the internal circuit.
To be used in the open state.

Top View

■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage*	V_{T1}	0.3～−2.5	V	1
	V_{T2}	0.3～−5.0	V	2
	V_{T3}	+0.2～V_{DD}−0.2	V	3
Operating temperature	T_{opr}	−10～+60	℃	
Storage temperature	T_{stg}	−20～+100	℃	

*Referenced to V_{SS}

Note 1: Applies to V_{DD}, V_{DD1} pins
Note 2: Applies to V_{EE} pin
Note 3: Applies to all input pins except V_{SS}, V_{EE}, V_{DD}, V_{DD1} pins

■ Operating Conditions

Parameter	Symbol	Ratings	Unit	Note
Supply voltage*	V_{DD}, V_{DD1}	−1.3～−1.8	V	4
Input voltage*	V_{IN}	0～V_{DD}	V	5

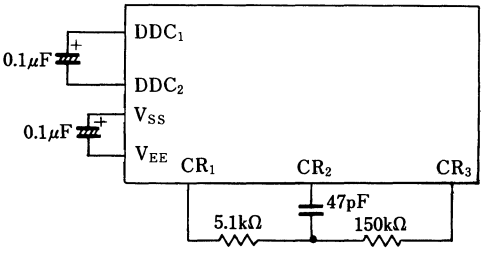
Note 4: Do not allow a sudden change to occur even within the rated value.
Note 5: Applies to SCK, SACL, SMEN, SPAU, SOPR, SALM, SDN, SR pins

■ Electrical Characteristics

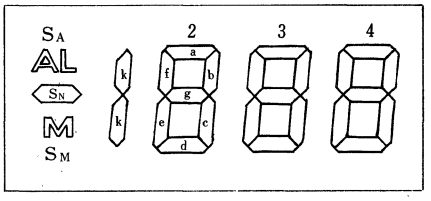
(V_{DD}=V_{DD1}=−1.5V, Ta=25℃)

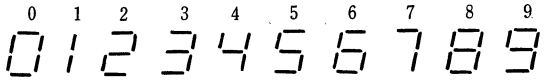
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Current consumption	(I_{DD}+I_{DD1})	All input pins V_{SS}, f_{OSC}=64kHz, with no load		13.5	25	μA	6
Input voltage	V_{IH}		−0.3			V	7
	V_{IL}				V_{DD}+0.3		
Input current	I_{IH}	V_{IH}=0V			5	μA	7
	I_{IL}	V_{IL}=V_{DD}			5		
CR oscillator frequency	f_{OSC}	R_1=5.1kΩ, R_2=150kΩ, C=47pF	32	48	64	kHz	8
Output current 1	I_{OH1}	V_{OH}=−0.5V, V_{EE}=−3.0V	10			μA	9
	I_{OL1}	V_{OL}=−2.5V, V_{ER}=−3.0V	10				
Output current 2	I_{OH2}	V_{OH}=−0.5V, V_{ER}=−3.0V	100			μA	10
	I_{OL2}	V_{OL}=−2.5V, V_E=−3.0V	100				
Output current 3	I_{OH3}	V_{OH}=−0.4V	10			μA	11
	I_{OL3}	V_{OL}=−1.1V	10				

Note 6: Total power consumption at fosc=64kHz
All output pins open
All input pins connected to the V_{SS} pin
V_{DD1} pin connected to V_{DD} pin
Note 7: Applies to all input pins except V_{SS}, V_{DD1}, V_{DD}, V_{EE}, CR_1, CR_2, CR_3, pins
Note 8: The constant values shown in the right figure are used in the oscillation circuit.
Note 9: Applies to segment output pins
Note 10: Applies to common output pins
Note 11: Applies to STP, ALM pins



■ Sample Displays and Font





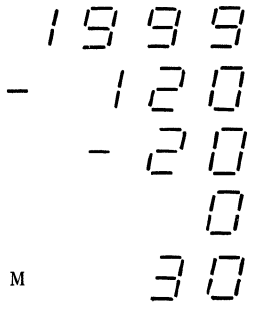
Sample display 1999

−120

−20

0

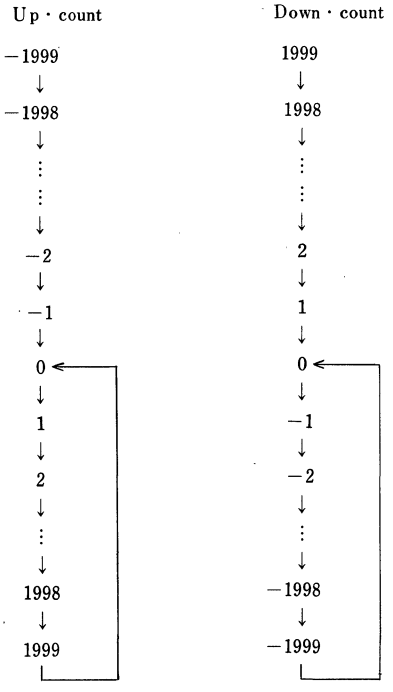
M30



■ Count Function

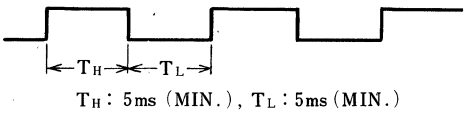
(1) Count range

Shown below are the count methods.



(2) Count input cycle

The count input signal waveform is as follows.



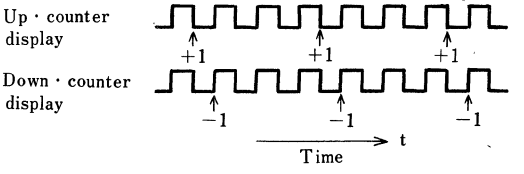
T_H : 5ms (MIN.), T_L : 5ms (MIN.)

(3) The relationship between count input, count content, and display

The LR3617 changes its display output each time 3 pulses get applied to the count input pin.

(4) Count input recognition

The LR3617 recognizes as one count pulse entered a transition that occurs in the up-counter mode when the counter input pin S_{CK} connected to V_{SS} is to be reconnected to V_{DD} (or open) or a transition that occurs in the down-counter mode when the count input pin S_{CK} connected to V_{DD} (or open) is to be reconnected to V_{SS}.



(5) Up/down input

The LR3617 works as a down-counter when the up/down input pin is connected to V_{SS}, and as an up-counter when the up/down input pin S_{DN} is connected to V_{DD} (or open).

With the stop signal output pin STP at V_{SS} level due to the tape end mode (discussed later) or the memory stop mode (discussed later) operation, when the up-down input pin S_{DN} connected to V_{DD} (or open) is to be reconnected to V_{SS}, the state of the stop signal output pin STP will be inverted to produce V_{DD} level output.

(6) Counter reset

Connecting the reset input pin S_R to V_{SS} resets the counter content to 0. Note that the counter does not operate with the reset input pin S_R connected to V_{SS}.

■ Memory Stop Mode

(1) Memory stop mode and its resetting

When the memory input pin S_{MEM} connected to V_{DD} (or open) is to be reconnected to V_{SS}, the memory stop mode will be entered, and M sign be displayed on LCD.

In memory stop mode, when the memory input pin S_{MEM} connected to V_{DD} (or open) is to be recon-

nected to V_{SS}, the memory stop mode will be reset and the M display on the LCD will disappear. Altering the memory input pin S_{MEM} connection does not affect the counter content.

(2) **Memory stop mode operation**

When the counter content changes in memory stop mode from the value other than 0 to 0 (when 2 pulses are applied to the count input pin after the display has turned 0, in the case of display changing from 1 to 0, or when the display turns 0 in the case of display changing from −1 to 0), the stop signal output pin STP will produce V_{SS} level output. However, in the case of counter content change from the value other than 0 to 0 due to reset input S_R., the stop signal output pin STP will not go V_{SS} level and stays at V_{DD} level instead.

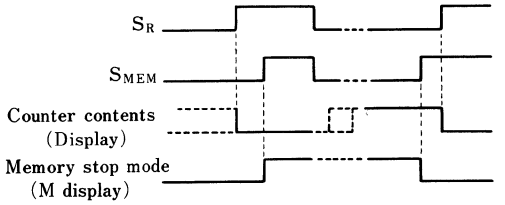
When the stop signal output pin STP produces V_{SS} level output due to the counter content change from the value other than 0 to 0, the memory stop mode will be reset and with it the M display on the LCD will disappear.

With the counter content at 0, the memory input pin S_{MEM} connected to V_{DD} (or open) is reconnected to V_{SS} to enter the memory stop mode.

And the stop signal output pin does not produce V_{SS} level output but stays at V_{DD} level.

The reset input S_R does not affect the memory stop mode.

The memory input pin S_{MEM} is always in effective operation as long as the LSI is supplied with power. The timing of the reset input S_R and the memory input S_{MEM} is as follows.



■ Tape End Detection Function

When no pulse has been applied to the counter input pin S_{CK} for 4～8 seconds with V_{SS} level input being applied to both the operation input pin S_{OPR}, and the pause input pin S_{PAU}, it will be decided that it is the tape end to be followed by the operations described below.

(1) **Tape end stop mode**

The tape end stop mode is a state in which the mode input pin S_{ALM} is connected to V_{DD} (or open). And when it is decided that it is the tape end, the stop signal output pin STP will produce V_{SS} level output. Changing the operation input pin S_{OPR} from V_{DD} to V_{SS} level with the stop signal output pin STP at V_{SS} level in the tape end stop mode, the state of the stop signal output pin will be inverted to produce V_{DD} level output.

(2) **Tape end alarm mode**

The tape end alarm mode will be entered when the mode input pin S_{ALM} is connected to V_{SS}. And if it is decided that it is the tape end, a 500～1000Hz pulse will be applied to the alarm signal output pin ALM.

When the operation input pin S_{OPR} is turned V_{DD} level with a 500～1000Hz pulse being applied to the alarm output pin ALM in the tape and alarm mode, the alarm signal output pin ALM produces V_{DD} level output. However with the STP at V_{SS} level output, the ALM output is disabled.

(3) **Operation input (S_{OPR})**

When the tape recorder is in PLAY, RECORD, FF, REW, CUE, REVIEW state, or in operation, V_{SS} level input is applied. And when the tape recorder is out of operation, V_{DD} level input is applied.

(4) **Pause input (S_{PAU})**

To be connected to V_{SS} when the tape recorder is in normal operation, or to be connected to V_{DD} (or open) when the tape recorder is out of operation or in the pause state.

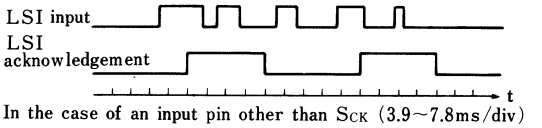
When no pulse has been applied to the count input pin S_{CK} for 4～8 seconds with the pause input pin connected to V_{DD} (or open), nor is it decided that it is the tape end.

(5) **Tape end alarm display**

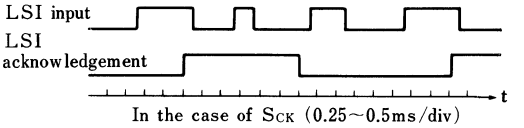
Tape end alarm mode allows for the mode indication in LCD static display.

(6) **Chatter killer**

The LR3617 has its operation input pin S_{OPR}, pause input pin S_{PAU}, mode input pin S_{ALM}, up-down input pin S_{DN}, memory input pin S_{MEM}, reset input pin S_R, and count input pin S_{CK} equipped with built-in chatter killers, the timing of which is shown in the figure below.



In the case of an input pin other than S_{CK} (3.9～7.8ms/div)



In the case of S_{CK} (0.25～0.5ms/div)

(7) Initial set

By connecting the initial set input pin $\overline{S_{ACL}}$ to V_{DD}, the internal LSI and each output will be initialized as follows.

Counter display 0

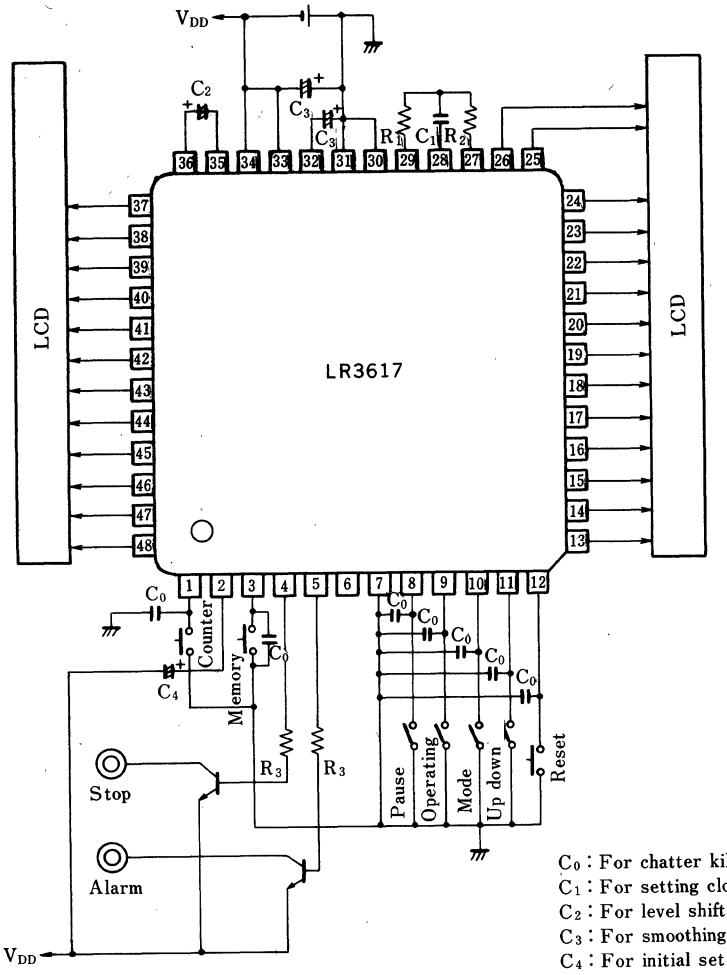
Memory stop function reset (therefore no M display)

Stop signal output pin STP V_{DD} level output

Alarm signal output pin ALM V_{DD} level output

The LSI retains the state as described above with the initial set input pin S_{ACL} connected to V_{DD}.

■ System Configuration



C_0 : For chatter killer of input signal
C_1 : For setting clock frequency
C_2 : For level shift coupling
C_3 : For smoothing after level shift
C_4 : For initial set
C_5 : For power supply hold
R_1 : For setting frequency
R_2 : For regulating current
R_3 : For regulating current

LR3727 VTR Data Back CMOS LSI

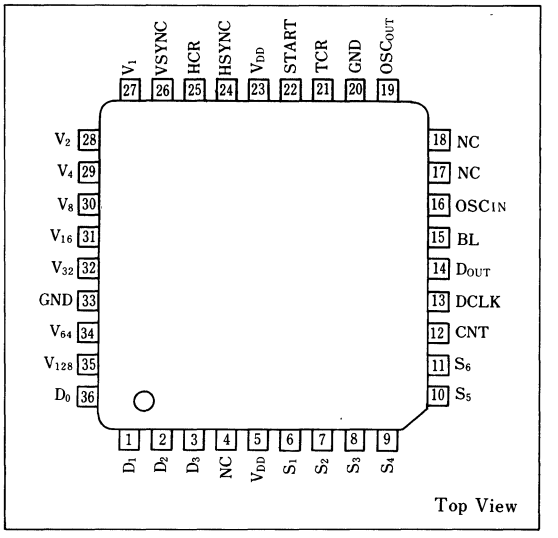
■ Description

The LR3727 is a CMOS LSI which provids date informations on video recordings.

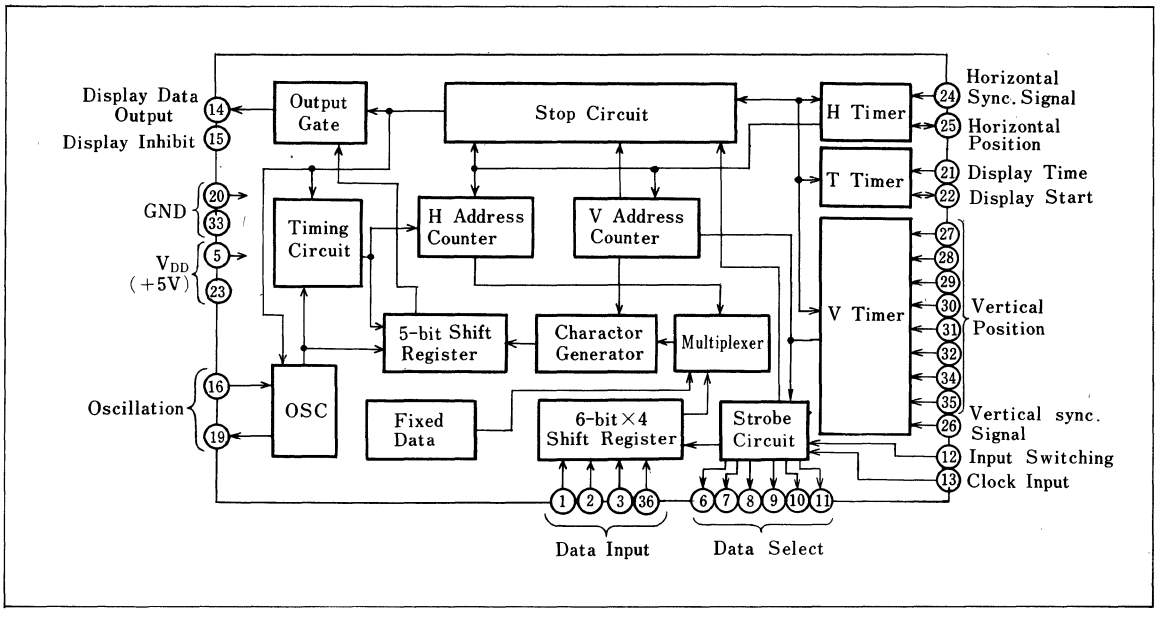
■ Features

1. Date information data store function (4-bit parallel BCD code)
2. Data display function
3. Single power supply : + 5V
4. CMOS process
5. 36-pin quad-flat package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage *1	V_{DD}	−0.3～+7.0	V
Input voltage *1	V_{IN}	−0.3～(V_{DD}+0.3)	V
Pin current	I	±10	mA
Power consumption *2	P_D	450	mW
Operating temperature	T_{opr}	−10～+60	℃
Storage temperature	T_{stg}	−55～+125	℃

*1 Referenced to GND
*2 Ta=60℃

■ Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage *1	V_{DD}	4.5	5.0	5.5	V
Input voltage *1	V_{IN}	0		V_{DD}	V
External oscillation resistance	R_{CP}		3.3		kΩ

■ Electrical Characteristics

(V_{DD}=5.0V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Current consumption	I_{DD}	In display mode, R_{CP}=3.3kΩ			5.0	mA	
		Standby mode			0.1		
Input voltage	V_{IH}		4.0		5.0	V	1
	V_{IL}		0.0		1.0		
Input current 1	I_{IH1}	V_{IN}=5.0V	0.0		1.0	μA	2
	I_{IL1}	V_{IN}=0V			−100		
Input current 2	I_{IH2}	V_{IN}=5.0V	0.0		1.0	μA	3
	I_{IL2}	V_{IN}=0V	0.0		−1.0		
Output voltage 1	V_{OH1}	5.0V at 1MΩ	4.0		5.0	V	4
	V_{OL1}	I_{OL}=1mA	0.0		0.5		
Output voltage 2	V_{OH2}	5.0V at 1MΩ	4.0		5.0	V	5
	V_{OL2}	I_{OL}=1mA	0.0		1.0		
Output voltage 3	V_{OH3}	I_{OH}=−1mA	4.5		5.0	V	6
	V_{OL3}	I_{OL}=1mA	0.0		0.5		
Clock oscillator frequency	f_{CP}	External resistance=3.3kΩ	2.5	3.0	3.5	MHz	

Note 1: Applies to all input pins
Note 2: Applies to D_0～D_3 pins
Note 3: Applies to input pins except D_0～D_3 pins
Note 4: Applies to HCR, TCR pins
Note 5: Applies to S_1～S_4 pins
Note 6: Applies to D_{OUT} pin

■ Operation

(1) Data store operation

(i) **Input data switch (CNT pin)** The input data switch input pin is a pin that switches the way the input data is taken in. As will be shown later, it is suited for data setting by digital switch when this input pin is "Low" and for reading in the data from the external LSI when it is "High".

(ii) **Input data select outputs (S_1~S_6 pins)** As will be shown later, these outputs produce the output of strobe signal for each digit when the CNT pin is "Low" and produce the output of interface signal for the external LSI when the CNT pin is "High".

(iii) **Data input (D_0~D_3 pins)** Enter the data selected by the data select outputs. The data inputs is by entering 6 times serially negative logic parallel BCD codes with each dight consisting of 4 bits. The data input is in the following order : 10 years' digit, 1 year's digit, 10 months' digit, 1 month's digit, 10 days' digit, and 1 day's digit.

Note that with each data, the D_0 pin is LSB, and the D_3 pin is MSB.

(iv) **Data clock input (DCLK pin)** Enters the fundamental clock input for data transfer when the CNT pin is "High". This clock sets up the data transfer timing. With the CNT pin "Low", zero blanking input for the 10 months' and 10 days' digit occurs. When the DCLK pin is "High", zero blank is enabled. And when it is "Low", no zero blank is enabled. Note that zero blank is disabled when the CNT pin is "High".

(2) Display operation

(i) **Horizontal sync signal and vertical sync signal input (HSYNC, VSYNC pin)**

To synchronize the picture, the positive-going horizontal sync pulse and vertical sync pulse are to be applied to these input signal pins. The pulse width required is more than 1 μs for the horizontal pulse, and more than twice the horizontal pulse width for the vertical pulse.

(ii) **Horizontal positioning (HCR pin)**

Input pin for the time constant of the one-shot multivibrator positions the horizonal display in the picture. By varying the time constant of the external CR, horizontal display position can be changed.

(iii) **Vertical positioning (V_1~V_{128} pins)**

Input pins for positioning. The level of this pin determines the vertical display position.

V_{128}	V_{64}	V_{32}	V_{16}	V_8	V_4	V_2	V_1	set value
L	L	L	L	L	L	L	H	1
L	L	L	L	L	L	H	L	2
L	H	H	L	L	L	H	H	99
L	H	H	L	L	H	L	L	100
H	H	H	H	H	H	H	L	254
H	H	H	H	H	H	H	H	255

Set value = 128 · V_{128} + 64 · V_{64} + 32 · V_{32} + 16 · V_{16} + 8 · V_8 + 4 · V_4 + 2 · V_2 + V_1

Through the combinations in the table above, any set value can be selected from 1 to 255. The display starts in the position (set value + 4) scan lines from the fall of VSYNC.

(iv) **Oscillator input and output (OSC_{IN}, OSC_{OUT} pins)** The frequency of the built-in oscillator is determined by the external resistor connected between these pins. The oscillator frequency of this oscillator determines the horizontal size of the character.

(v) **Display time input (TCR pin)** Input pin for time constant of one-shot multivibrator that determines how long the characters shall be displayed on the screen. By varying the time constant of the external CR, display time can be changed.

(vi) **Display data output (D_{OUT} pin)** Display data output pin that produces "Low" output when no character is being displayed and produces "High" or "Low" output according to the display when character(s) is(are) being displayed.

(vii) **Display blanking input (BL pin)** Input that disables the display data output (D_{OUT} pin). When this pin goes "High", the D_{OUT} pin always will go "Low" level. This pin only disables the D_{OUT} output and does not affect the internal working of the LSI.

(viii) **Display start input (START pin)** Input for not only starting to read external data into the LSI but also for displaying this data on the screen after the data is read.

When this input changes from "Low" to "High", the one-shot multivibrator that determines the display time will be triggered.

The data display time is determined by the time constant of the CR externally connected to the display time input pin.

■ Display

The display is a total 6-digit, 1-line display of year, month, and day each consisting of 2 digits. The character organization and character array are as follows.

D_3	D_2	D_1	D_0	Indication
High	High	High	High	
High	High	High	Low	
High	High	Low	High	
High	High	Low	Low	
High	Low	High	High	
High	Low	High	Low	
High	Low	Low	High	
High	Low	Low	Low	
Low	High	High	High	
Low	High	High	Low	
Low	Low	Low	Low	(blank)

(1) Character organization

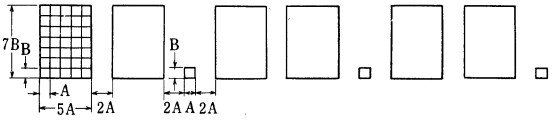
The display character is of 5×7 numerics and dots that separate year, month, and day. The dots are fixed and not erasable.

(2) Character array

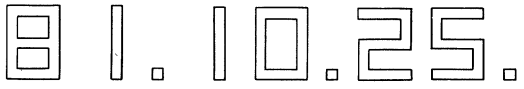
The character organized as described above will be displayed in array as follows. And the character size, and spacing are as shown in the figures A and B.

A : Approx. 550ns (when the frequency of the built-in oscillator is 1.8MHz)

B : Scan line.....3 lines/field



Character array



Display of October 25, '81

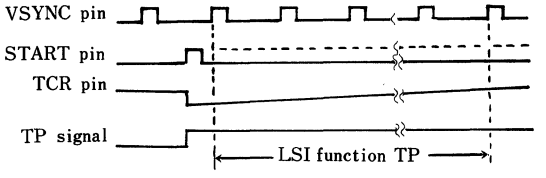
■ Description of Operation

(1) On application of the source voltage V_{DD}, the capacitor externally connected to the timer T starts charging. And when the pulse is applied to each of the VSYNC and HSYNC pins, display function is enabled. The display this time is not consistent, but most of the time, only the dots that separate the digits are displayed and the characters that would otherwise follow get blanked.

No input signal should be applied prior to power-up because the LR3727 is of CMOS structure. It should be remembered that source voltage should always be kept turned on because of the LSI's small current consumption except when displaying. When the capacitor externally connected to the timer T finishes charging, the LR3727 will go into the standby mode.

(2) Apply the horizontal sync pulse and vertical

sync pulse to the HSYNC and VSYNC pin respectively. Until the START signal is applied, the whole LSI is in static state and retains the initial state with the D_{OUT} pin "Low", oscillator in static state, $S_1 \sim S_6$ in high impedance state ("High"), and each of the time constant input pins (TCR pin, HCR pin) in high impedance state ("High").



(3) Vary the START input pin from "Low" to "High" to enter the START signal. As shown in the following figure, the TP signal is generated in the LSI while the TP signal is in sync with the VSYNC signal. More than 1 μs of the width START input signal is required. The TP signal width is determined by the time constant of the CR externally connected to the TCR pin. Therefore, if the TCR is left connected to GND, the operation time of the LSI will be infinitely long and go into continuous display. (However, if the CNT pin is "High", the display data will be read into the LSI only once immediately after the START signal input. Even in continuous display, the START signal should be entered again to alter the display.)

(4) On the top signal going "High", the external data will be read into the LSI with the timing as shown in Fig. 1 and Fig. 2. In the data read timing chart, the CR time constant of the TRC pin (or TP signal output time) is shown to be long enough compared to the vertical sync signal cycle (longer than 2 cycles). With the CR time constant of the TCR pin short (shorter than the vertical sync signal cycle), the complete external data cannot be read into the LSI.

The HP signal in the timing chart just discussed

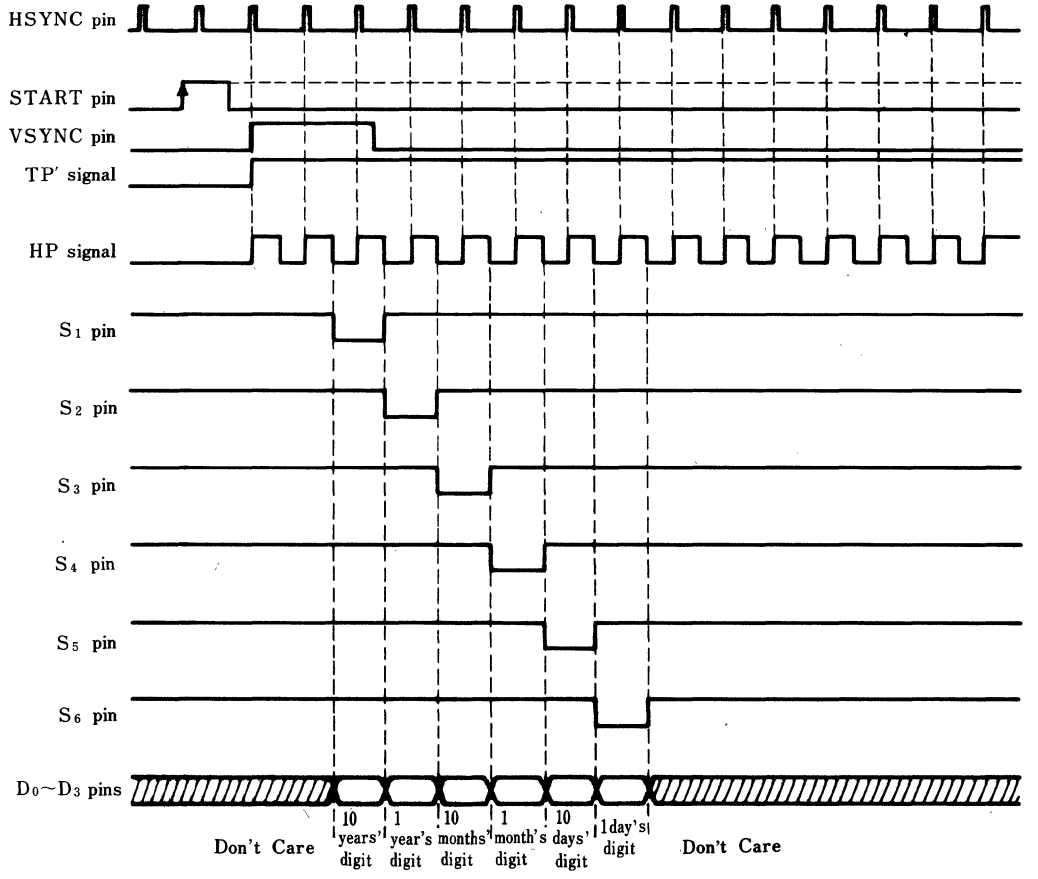


Fig. 1 Data read timing (CNT pin "Low")

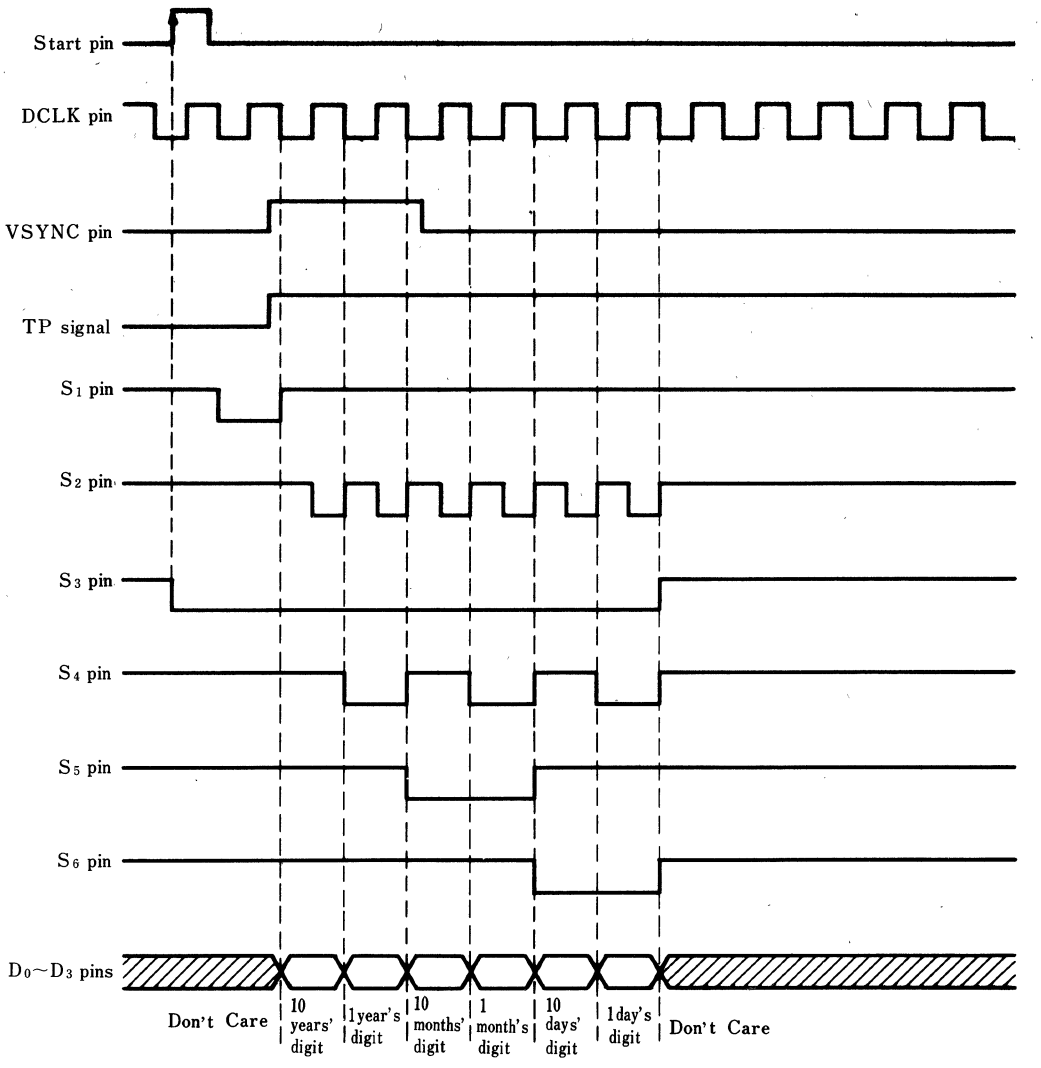


Fig. 2 Data read timing (CNT pin "High")

is a signal in sync with the rise of the horizontal sync signal applied to the HSYNC pin and has a pulse width that is determined by the time constant of the CR externally connected to the HCR pin. Duty varies with the horizontal display position on the screen.

The external data applied to $D_0 \sim D_3$ pins goes into sync with the rise of the horizontal sync signal applied to the HSYNC pin when the CNT pin is "Low", or goes into sync with the rise of the clock applied to the DCLK pin when the CNT pin is "High", to be read into the LSI. Note that while the LSI is reading external data, the display gets blanked and therefore the D_{OUT} pin maintains "Low".

The external data read into the LSI is a 6 character data and is stored in a 6 × 4 shift register. The data for the dots that separate each digit will be set up in the LSI as fixed data. These character data or fixed data are to be through the multiplexer to the character generator.

(5) The data read time is followed by the display time if the TP signal is "High". The display time lasts while the TP signal maintains "High" and comes to an end when the TP signal goes "Low".

During the display time, it is so designed, the V address counter counts the HP signals (the pulse width of which is determined by the time constant of the CR externally connected to the HCR pin) that is in sync with rise of the horizontal sync signal applied to the HSYNC pin, collects out of the character generator the character data output produced during each horizontal scan time, and produces

serially through the 5-bit shift register the character outputs one by one at the D_{OUT} pin.

In the meantime, the H address counter counts the timing pulses HC that occur during 1 horizontal time to construct a character address and transmit 6 character data and 2 dot data to the character generator.

The oscillator operates only part of the horizontal time (when HP is "Low") where display is to be performed, to generate not only 5-bit shift register data but also the clock for the timing circuit and load sequentially 6-character 2-dot data into the 5-bit shift register.

Fig. 3 shows the timing chart of the 1 field immediately after data read. One character is divided into 7 parts with each part displayed during the 3 horizontal scan lines per field so that vertical size of one character is 21 horizontal scan lines high per field. During the display time, this operation repeats with each input of vertical sync signal applied to VSYNC pin.

Fig. 4 shows the timing chart of 1 horizontal time during the display. One character is divided horizontally into 5 parts so that their signal outputs will be produced from the D_{OUT} pin.

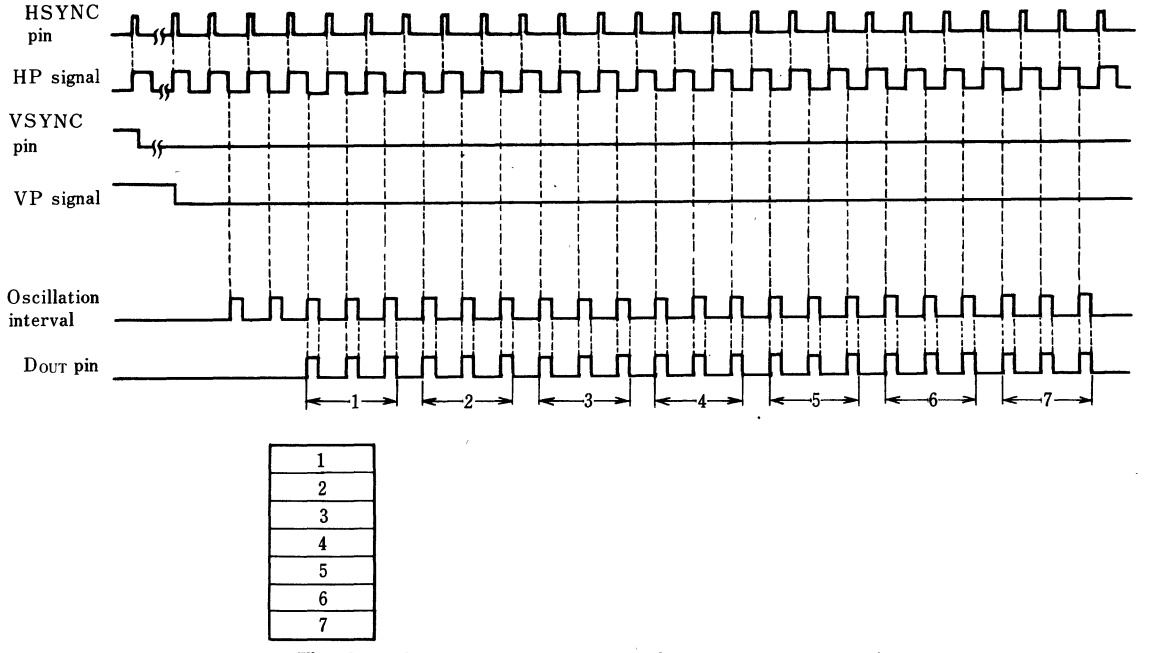


Fig. 3 Display timing in 1 field (TP signal = "High")

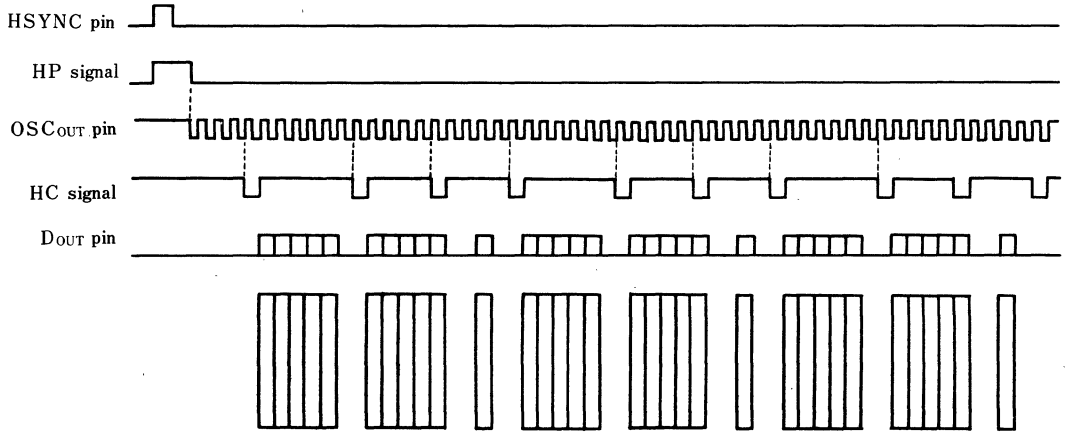
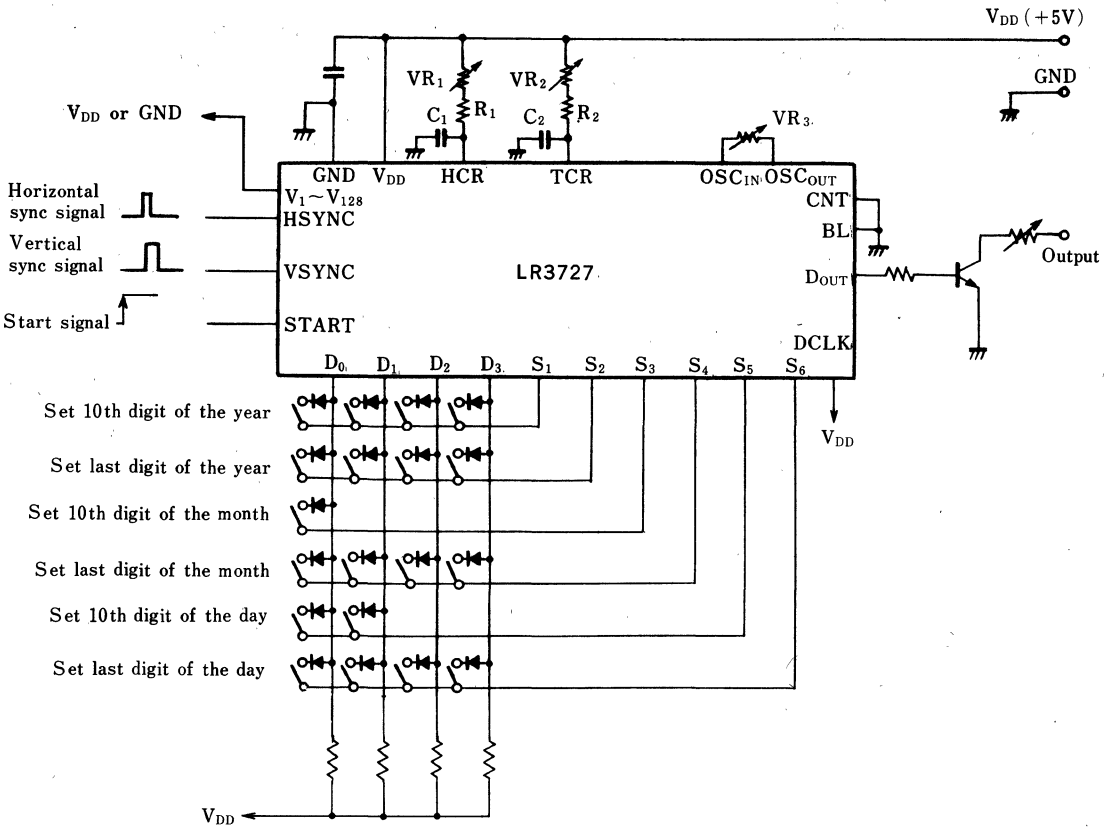


Fig. 4 Display timing in 1 horizonal time (TP signal = "High")

System Configuration



LR3652 Phase Locked Loop Frequency Synthesizer CMOS LSI

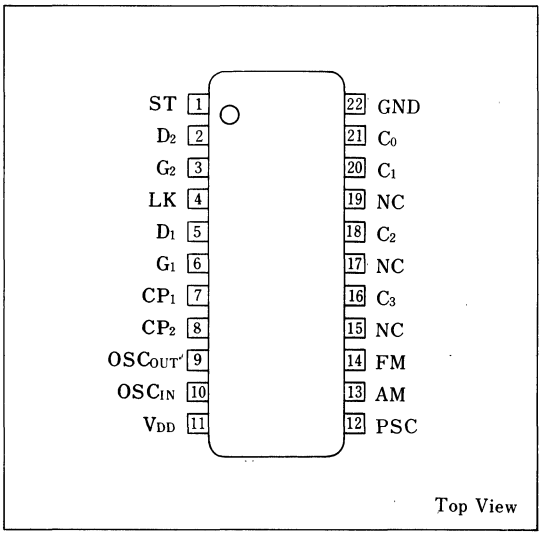
■ Description

The LR3652 is a CMOS LSI designed for PLL frequency synthesizer AM/FM radios. It can be controlled directly by the Sharp 4-bit 1-chip SM-4A or SM-5A microcomputers.

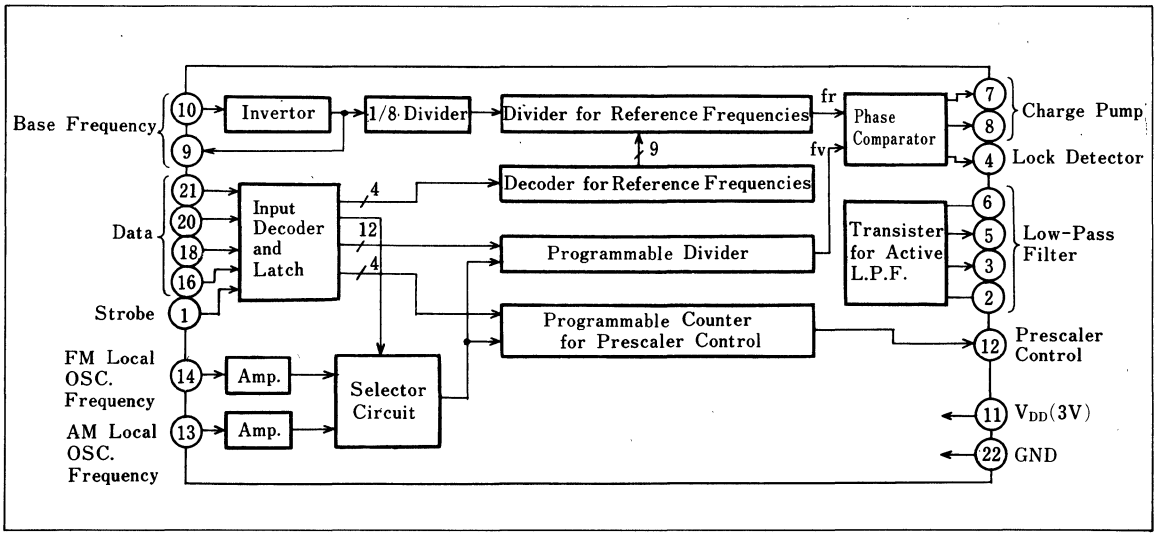
■ Features

1. Reference frequencies
   FM mode
   2.25kHz, 2.5kHz, 12.5kHz, 25kHz, 50kHz
   AM mode
   1kHz, 4.5kHz, 5kHz, 9kHz, 10kHz
2. Frequency division ratio : 1/3 ~ 1/999
3. FM mode : pulse-swallow type
4. Charge-pump output port and an N-channel open drain transistor are contained for use in LPF amp.
5. 5-bit input ports
6. Time base : 3.6MHz crystal
7. Single power supply : + 3V
8. CMOS process
9. 22-pin dual-in-line package

■ Pin Connections



■ Block Diagram



10

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3～+6.0	V	
External voltage	V_{CC}	−0.3～+18	V	1
Input voltage	V_{IN}	−0.3～+6.0	V	
Current consumption	I_{DD}	±10.0	mA	2
Output current	I_{OUT}	±2.0	mA	2,3
Operating temperature	T_{opr}	−20～+60	V	
Storage temperature	T_{stg}	−55～+125	V	

Note 1: Applies to D_1, D_2 pins.
Note 2: The direction of flowing into the LSI is defined as positive, and flowing out of the LSI as negative.
Note 3: Applies to output pins.

■ Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}	2.7	3.0	3.3	V	
External voltage	V_{CC}	0.0		15.0	V	1
Input voltage	V_{IN}	0.0		V_{DD}	V	
Oscillator frequency	f_{OSC}	3.6			MHz	

■ Electrical Characteristics

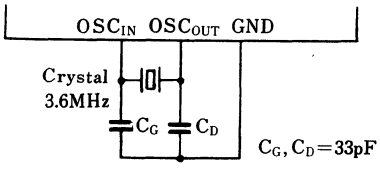
(V_{DD}=3.0V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}	f_{OSC}=3.6MHz FM or AM=3.0MHz, 0.3V_{P-P}	2.7	3.0	3.3	V	4
Current consumption	I_{DD}	f_{OSC}=3.6MHz, output pin open FM or AM=3.0MHz, 0.3V_{P-P}		2.5	5.0	mA	4
Input voltage	V_{IH}		2.6		3.0	V	5
	V_{IL}		0.0		0.4		
Input current	I_{IH}	V_{IN}=3.0V			1.0	μA	5
	I_{IL}				−1.0		
Input frequency	f_{IN}	Sine wave V_{IN}=0.3V_{P-P}	3.0			MHz	6
Output voltage	V_{OH1}	Connects to V_{DD} at 100kΩ	2.6		3.0	V	7
	V_{OL1}	I_{OL}=100 μA	0.0		0.4		
	V_{OH2}	I_{OH}=−200 μA	2.6		3.0	V	8
	V_{OL2}	I_{OL}=200 μA	0.0		0.4		
	V_{OH3}	I_{OH}=−200 μA	2.6		3.0	V	9
	V_{OL3}	I_{OL}=200 μA	0.0		0.4		
	V_{OH4}	V_{CC}=15V at 100kΩ with G_1 and G_2 grounded	14.80	14.95	15.00	V	1
	V_{OL4}	I_{OL}=1.0mA, with G_1 and G_2 grounded	0.0		0.4		
Oscillator frequency	f_{OSC}		3.6			MHz	10
PSC delay time	T_{LH}	V_{IN}=3.0MHz, sine wave			300	ns	8
	T_{HL}	0.5V_{P-P}			300		

Note 4: Applies to V_{DD} pin
Note 5: Applies to ST, C_0, C_1, C_2, C_3, pins
Note 6: Applies to AM, FM pins
Note 7: Applies to LK pin
Note 8: Applies to PSC pin
Note 9: Applies to CP, CP_2 pins
Note 10: Applies to OSC_{IN}, OSC_{OUT} pins

■ How to Use Pins

(1) OSC_{IN}, OSC_{OUT} (Crystal oscillation)



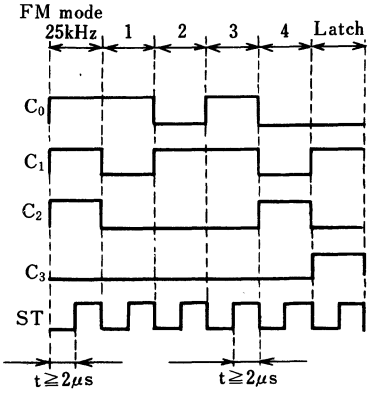
Programmable counter for prescaler control ..... counter range =4

If a prescaler with its frequency dividing ratio switchable between 1/40 and 1/44 is used :

Mode ..... FM
Channel space 100kHz
Frequency dividing ratio 1/123
Count range of the counter for prescaler 4

ST	C_0	C_1	C_2	C_3	Function
1	MF	M_1	M_2	M_3	With MF "Low" and "High", AM mode and FM mode respectively. For M_1~M_3, refer to the other table.
2	P_{31}	P_{32}	P_{33}	P_{34}	P_{31}~P_{34} set the frequency dividing ratio for the 100's digit of the programmable counter.
3	P_{21}	P_{22}	P_{23}	P_{24}	P_{21}~P_{24} set the frequency dividing ratio for the 10's digit of the programmable counter.
4	P_{11}	P_{12}	P_{13}	P_{14}	P_{11}~P_{14} set the frequency dividing ratio for the 1's digit of the programmable counter.
5	P_1	P_2	P_3	P_4	P_1~P_4 set the count range of programmable counter for pulse swallowing.
6	"Low"	"High"	"Low"	"High"	Indicate the end of data input and data latch.

M_1	M_2	M_3	Reference frequency (kHz)	
			FM mode (MF"High")	AM mode (MF"Low")
"Low"	"Low"	"Low"	2.25	1.0
"High"	"Low"	"Low"	2.50	4.5
"Low"	"High"	"Low"	12.50	5.0
"High"	"High"	"Low"	25.00	9.0
"Low"	"Low"	"High"	50.00	10.0



The input described above provides

Mode ..... FM
Phase comparision frequency 25kHz
Programmable counter for FM, AM input ..... frequency deviding ratio=1/123

(2) C_0, C_1, C_2, C_S, ST

These are the data input pins for selecting FM/AM, setting reference frequency, FM/AM input frequency dividing ratio, and the count range of programmable counter. The following 2 different data inputs are available.

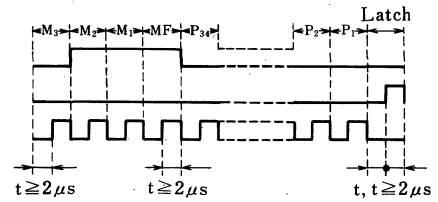
(i) **Using 4-bit data and strobe** The data will be read into LSI by strobe function after 4-bit data is set. It takes 6 times of strobe to complete data reading.

(ii) **Using one pin each for data, strobe, and latch** 20-bit data is entered serially through the data input pin C_0. With one strobe, the data is read one bit and will be latched by the C_1 input after data reading is completed. $\overline{C_2}$ and $\overline{C_3}$ shall always stay at "High" level.

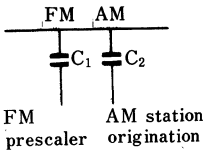
ST	1	2	3	4	5	6	7	8	9	10
C_0	M_3	M_2	M_1	MF	P_{34}	P_{33}	P_{32}	P_{31}	P_{24}	P_{23}

ST	11	12	13	14	15	16	17	18	19	20
C_0	P_{22}	P_{21}	P_{14}	P_{13}	P_{12}	P_{11}	P_4	P_3	P_2	P_1

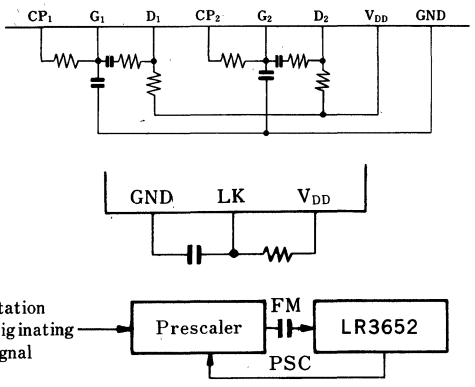
10



(iii) **FM, AM** (Station originatng input)



C_1, C_2 : 1000pF



(iv) **CP_1, CP_2, G_1, G_2, D_1, and D_2**

(Constitute a low pass filter circuit)

(v) **LK (lock output)**

Goes "High" (the transistor turns off) if the PLL loop is locked.

(vi) **PSC** (Prescaler control output)

■ Reception Frequency Range (1)

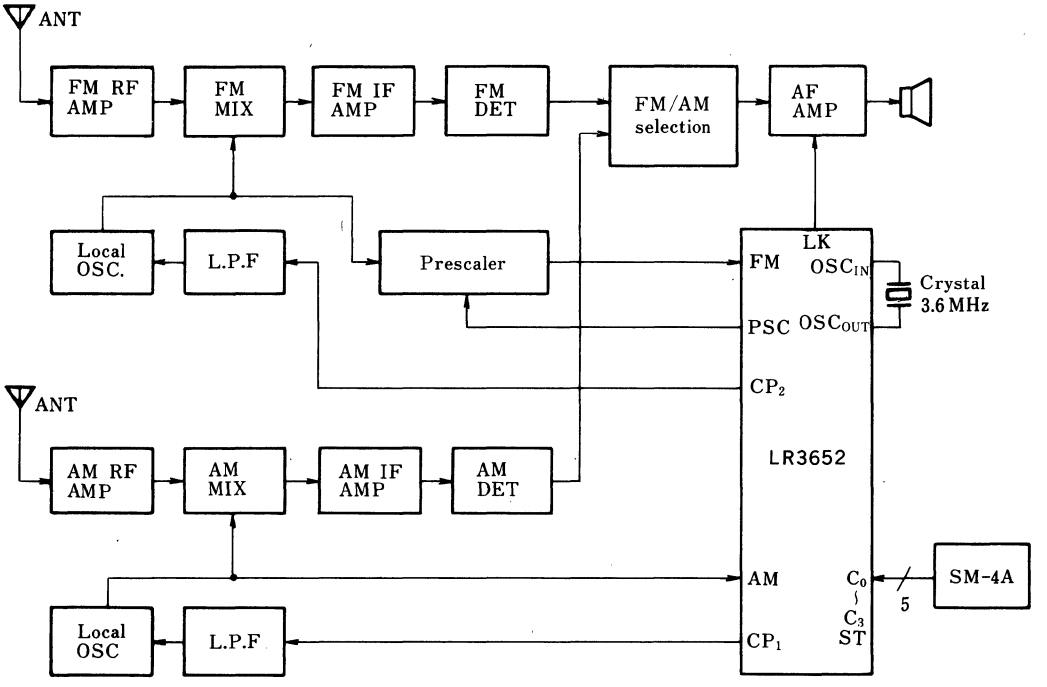
Band	Area	MF	M_1	M_2	M_3	Frequency dividing ratio	Comparison frequency
FM	Japan	"High"	"High"	"High"	"Low"	1/65~1/79 *2 (4~2) *1	25kHz
	USA	"High"	"Low"	"Low"	"High"	1/49~1/59 *2 (4~3) *1	50kHz
	Europe	"High"	"Low"	"High"	"Low"	1/196~1/229 *2 (6~0) *1	12.5kHz
AM	Japan	"Low"	"High"	"High"	"Low"	1/109~1/228	9kHz
	USA	"Low"	"Low"	"Low"	"High"	1/80~1/184	10kHz
	Europe	"Low"	"High"	"High"	"Low"	1/109~1/228	9kHz

*1 Count range of prescaler control counter
*2 When to be used in the FM mode, an IC that, as a prescaler, allows frequency dividing ratio to be switched between 1/40 and 1/44 is used.

■ Reception Frequency Range (2)

Band	Area	Reception frequency range	Intermediate frequency	Station originating frequency	Channel space
FM	Japan	76.1~89.9MHz	−10.7MHz	65.4~79.2MHz	100kHz
	USA	88.1~107.9MHz	+10.7MHz	98.8~118.6MHz	200kHz
	Europe	87.6~103.8MHz	+10.7MHz	98.3~114.5MHz	50kHz
AM	Japan	531~1,602MHz	+450MHz	981~2,052kHz	9kHz
	USA	540~1,580MHz	+260MHz	800~1,840kHz	10kHz
	Europe	531~1,602MHz	+450MHz	981~2,052kHz	9kHz

■ System Configuration



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SEMICONDUCTOR DATA BOOK

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REF. NO. HT-088C