ZX Spectrum Sound Chips and Programming Quick Reference Guide

Introduction: Sinclair reserved 2x I/O addresses for the ZX Spectrum 128's new PSG chip.

Since then, unofficial clones and upgrades to the sound hardware were proposed. Notably, early products such as the Explorer from Brazil, the Melodik from Czechoslovakia and others allowed the 48K ZX Spectrum and its' many clones worldwide to replicate the PSG experience, using the same basic circuitry and I/O ports:

I/O	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
FFFDh	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
BFFDh	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1

Sinclair ZX Spectrum 128 (1985): 1x PSG chip (General Instruments AY-3-8912) available, always active.

A PSG register is specified by loading the data bus while writing to address FFFDh in the I/O space. D3-D0 supply the octal address between 0 and 15, while D7-D4 should be all zero. In the PSG address mode, D7-D4 (with A8 pulled high) are decoded by the hardware to provide a 'chip select' signal to the PSG. The instruction code is then written to the register by writing to address BFFDh. A14, /RD, BDIR, BC1 (and BC2 pulled high) are decoded by the hardware to define the type of operation for the PSG as follows:

PSG	A14	/RD	BDIR	BC1	I/O ADDRESS	OPERATION
1	1	1	1	1	FFFDh	Write Register Address
1	1	0	0	1	FFFDh	Read Register Data (RS232C/MIDI)
1	0	1	1	0	BFFDh	Write Register Data
0	x	x	0	0	-	Inactive (D7-D0 at high impedance)

INSTRUCTION	OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
OUT (FFFDh)	Select a PSG register address (00h-1Fh)	0	0	0	0	x	x	x	x
IN (FFFDh)	Read the value stored in the selected PSG register	x	x	x	x	x	x	x	x
OUT (BFFDh)	Write a value to the selected PSG register	x	x	x	x	x	x	x	x

NedoPC Turbo Sound (2005): 2x SSG chips (Yamaha YM2149) available, 1 active at a time.

The clever TS expansion board replaces the AY-3-8910/8912 chip in any ZX Spectrum 128-based system with a pair of almost fully compatible YM2149 chips rebranded "SSG" by Yamaha. A new 'chip select' switch was introduced by writing to I/O address FFFDh with the data bus loaded with D7-D1 all set high and D0 selecting between the 1st and 2nd chip, effectively doubling the sound generation capability from 3 to 6 channels, while keeping compatiblity with software made for the original single-PSG hardware:

<sel>: D0=0 (FEh) selects the 1st YM2149 chip D0=1 (FFh) selects the 2nd YM2149 chip

INSTRUCTION	OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
OUT (FFFDh)	Select the active SSG chip (FEh/FFh)	1	1	1	1	1	1	1	sel
OUT (FFFDh)	Select a SSG register address (00h-1Fh)	0	0	0	0	x	x	x	x
IN (FFFDh)	Read the value stored in the selected SSG register	x	x	x	x	x	x	x	x
OUT (BFFDh)	Write a value to the selected SSG register	x	x	x	x	x	x	x	x

ZX Spectrum Next (2019): 3x PSG FPGA cores (AY/YM) available, 1 active at a time.

Taking advantage of the freedom and capacity allowed by its' FPGA, the ZXN included 3x PSG cores for effectively 9x PSG channels, expanding over the original TS scheme. It even allows choosing between PSG (AY) or SSG (YM) for maximum compatibility. Its' configuration is done writing to I/O address FFFDh with the data bus loaded with D7 and D4-D2 all set high, with D6-D5 controoling the stereo output channels, and D1-D0 selecting the active AY/YM chip:

<left channel output>: D6=1 enabled (default) / D6=0 disabled

<right channel output>: D5=1 enabled (default) / D5=0 disabled

<AY0 active>: D1=1 / D0=1 (default)

<AY1 active>: D1=1 / D0=0

<AY2 active>: D1=0 / D0=1

<reserved>: D1=0 / D0=0

While keeping backwards compatibility, the ZXN makes the I/O address BFFDh readable in the same way as FFFDh (only when video timing is set to +3/ZXN modes), and adds its' own AY Status readable from I/O address BFF5h:

D7-D6 = <currently active PSG>: 11 (AY0), 10 (AY1) or 01 (AY2)

D5 = <reserved>

D4-D0 = <currently selected PSG register>

INSTRUCTION	OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
OUT (FFFDh)	Select active PSG (D0-D1), enable R/L channel (D5/D6) output	1	x	x	1	1	1	x	x
OUT (FFFDh)	Select a PSG register address (00h-1Fh)	0	0	0	x	x	x	x	x
IN (FFFDh)	Read the value stored in the selected PSG register	x	x	x	x	x	x	x	x
OUT (BFFDh)	Write a value to the selected PSG register	x	x	x	x	x	x	x	x
IN (BFFDh)	Read the value stored in the selected register (+3/ZXN modes)	x	x	x	x	x	x	x	x
IN (BFF5h)	Read the value in the ZXN AY Status	x	x	x	x	x	x	x	x

NedoPC Turbo Sound FM (2007): 2x SSG+OPN chips (Yamaha YM2203) available, 1 active at a time.

The TS hardware was further upgraded while keeping backwards compatibility, now with a pair of YM2203 chips, each adding a new 3-channel OPN class FM synthesizer in addition to the SSG function, effectively allowing up to 6x FM channels + 6x SSG channels. The TSFM circuitry is still limited by the underneath system whose original PSG chip it replaces, but it's CPLD converts the legacy chip select decoding to the YM2203's new scheme:

/CS	/RD	/WR	A0	OPERATION
0	1	0	0	Write SSG/FM Register Address
0	1	0	1	Write SSG/FM Register Data
0	0	1	0	Read FM Status Register
0	0	1	1	Read SSG Register Data
1	x	x	x	Inactive (D7-D0 at high impedance)

Writing to I/O address FFFDh with the data bus loaded with D7-D3 all set high, D2-D0 will switch each of these 3 featues:

<sel>: D0=0 selects the 1st YM2203 chip D0=1 selects the 2nd YM2203 chip
<stat>: D1=0 reads from the FM status register D1=1 reads from the SSG registers (FM registers are write only)
<fm>: D2=0 enables the FM synthesizer output D2=1 disables the FM synthesizer output

After a system reset, TSFM defaults to D7-D1 all set high and D0 set low, keeping backwards compatibility with the previous TS.

INSTRUCTION	OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
OUT (FFFDh)	Select active chip (D0), read mode (D1) and FM mode (D2)	1	1	1	1	1	fm	stat	sel
OUT (FFFDh)	Select a SSG (00h-1Fh) or FM (21h-B2h) register address	x	x	x	x	x	x	x	x
IN (FFFDh)	Read the value in the FM Status or the selected SSG register	x	x	x	x	x	x	x	x
OUT (BFFDh)	Write a value to the selected SSG or FM register	x	x	x	x	x	x	x	x

Explorer FM (2023): 1x SSG+OPN3 chip (Yamaha YMF288) available, can be activated any time.

The ExFM aims to offer the best sound generation experience to a wide range of ZX Spectrum compatible systems with a plug-in solution, overcoming previous solutions' shortcomings such as the TSFM's need to hack into the original PSG istalled in some systems, or the lack of room for a FM synth in the amazing ZXN's FPGA. Systems based on the ZX Spectrum 128/+2/+3 still require a modification to disable its' internal PSG chip in order to avoid conflict with the ExFM, but otherwise any Speccy compatible system including 16K/48K models with a standard ZX expansion port can take the ExFM and enjoy all the features offered by Yamaha's latest chip from the SSG+OPN FM family, the YMF288:

- FM: OPN3 class, 4-operators, 6-channels (twice the YM2203), mixed to stereo digital output;
- Rythm: 6-instruments from embedded ADPCM sampled data, 6-channels, mixed to stereo digital output;
- SSG: compatible with YM2203 and YM2149 (I/O ports deleted), 3-channels, mixed to stereo digital output;

The YMF288 chip select decoding added an extra address bit (A1) over the YM2203 to handle the new features:

/CS	/RD	/WR	A1	A0	OPERATION
0	1	0	0	0	Write SSG/FM/Rythm Register Address
0	1	0	0	1	Write SSG/FM/Rythm Register Data
0	1	0	1	0	Write Alternate FM Register Address
0	1	0	1	1	Write Alternate FM Register Data
0	0	1	0	0	Read FM Status 0 Register
0	0	1	0	1	Read SSG/FM/Status 2 Register Data
0	0	1	1	0	Read FM Status 1 Register
0	0	1	1	0	Inactive (D7-D0 at high impedance)
1	x	x	x	x	" "

Writing to I/O address FFFDh with the data bus loaded with D7-D3 all set high, D2 and D0 will set the YMF288 operation mode:

<A1>: D0=0 access legacy YM2203 registers D0=1 access additional FM channels (Ch4~6) and status register
</CS>: D2=0 activates YMF288 for programming D2=1 deactivates YMF288, switching its' data bus to high impedance

Note: D1 is ignored, as the legacy FM status register can be read regardless of D1 state, as well as 2 new additional status registers.

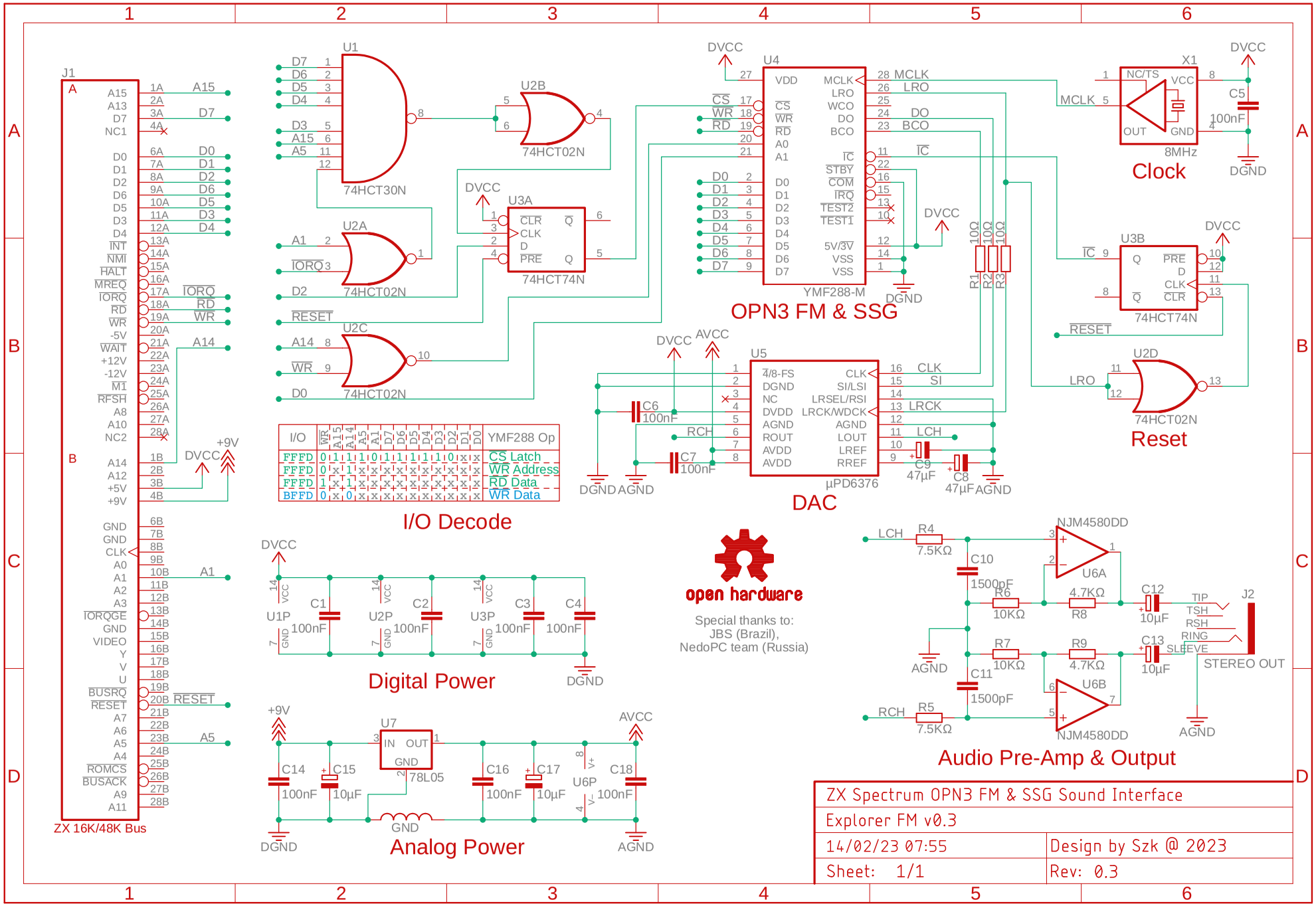
INSTRUCTION	OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
OUT (FFFDh)	Activate the YMF288 (D2) and its' alternate FM channels (D0)	1	1	1	1	1	/CS	x	A1
OUT (FFFDh)	Select a SSG, FM or Rythm (00h-B6h) register address	x	x	x	x	x	x	x	x
IN (FFFDh)	Read the value in any SSG, FM or Rythm register*	x	x	x	x	x	x	x	x
OUT (BFFDh)	Write a value to the selected SSG, FM or Rythm register	x	x	x	x	x	x	x	x

* See details in the YMF288 datasheet.

Yamaha SSG-OPN Sound Chips Lineage Quick Reference Guide

DATA BUS (D0~D7) CONTROL					SSG	OPN	OPNA	OPN2	OPN3	BINARY	ADDR.	REGISTERS
/CS	/RD	/WR	A1	A0	YM2149	YM2203	YM2608	YM2612	YMF288	ADDRESS	RANGE	
0	1	0	0	0=Addr 1=Data	3-Ch 2-I/O	3-Ch 2-I/O	3-Ch 2-I/O	-	3-Ch	0000xxxx	00~0F	SSG - Addr/Data Write
					●	●	●	-	●	00000000	00	Channel A Frequency (Fine)
					●	●	●	-	●	00000001	01	Channel A Frequency (Coarse)
					●	●	●	-	●	00000010	02	Channel B Frequency (Fine)
					●	●	●	-	●	00000011	03	Channel B Frequency (Coarse)
					●	●	●	-	●	00000100	04	Channel C Frequency (Fine)
					●	●	●	-	●	00000101	05	Channel C Frequency (Coarse)
					●	●	●	-	●	00000110	06	Noise Frequency
					●	●	●	-	●	00000111	07	I/O Ports & Mixer Settings
					●	●	●	-	●	00001000	08	Channel A Amplitude
					●	●	●	-	●	00001001	09	Channel B Amplitude
					●	●	●	-	●	00001010	0A	Channel C Amplitude
					●	●	●	-	●	00001011	0B	Envelope Frequency (Fine)
					●	●	●	-	●	00001100	0C	Envelope Frequency (Coarse)
					●	●	●	-	●	00001101	0D	Envelope Shape
					●	●	●	-	-	00001110	0E	I/O Port A Data
					●	●	●	-	-	00001111	0F	I/O Port B Data
0	1	0	0	0=Addr 1=Data	-	-	6-Ch	-	6-Ch	0001xxxx	10~1D	RHYTHM - Addr/Data Write
					-	-	●	-	●	00010000	10	Dump & Rythm Key ON
					-	-	●	-	●	00010001	11	Rythm Total Level
					-	-	●	-	●	00010010	12	LSI Test Data
					-	-	●	-	●	00011000	18	Bass Drum Select & Level
					-	-	●	-	●	00011001	19	Snare Drum Select & Level
					-	-	●	-	●	00011010	1A	Top Cymbal Select & Level
					-	-	●	-	●	00011011	1B	Hi-Hat Select & Level
					-	-	●	-	●	00011100	1C	Tom-Tom Select & Level
					-	-	●	-	●	00011101	1D	Rimshot Select & Level
0	1	0	0	0=Addr 1=Data	-	3-Ch	6-Ch	6-Ch	6-Ch	0010xxxx	20~2F	FM (Common) - Addr/Data Write
					-	-	-	-	●	00100000	20	STBY, YMF288*/YM2608B Modes
					-	●	●	●	●	00100001	21	LSI Test Data
					-	-	●	●	●	00100010	22	LFO Frequency Control
					-	●	●	●	●	00100100	24	Timer-A Upper 8 bits
					-	●	●	●	●	00100101	25	Timer-A Lower 2 bits
					-	●	●	●	●	00100110	26	Timer-B Data
					-	●	●	●	●	00100111	27	Timer-A/B Control & 3Ch Mode
					-	●	●	●	●	00101000	28	Key-On/Off
					-	-	●	-	●	00101001	29	SCH & IRQ Enable
					-	-	-	●	●	00101010	2A	DAC Data / LSI Test Data
					-	-	-	●	●	00101011	2B	DAC Select / LSI Test Data
					-	-	-	●	●	00101100	2C	LSI Test Data
					-	●	●	-	-	00101101	2D	Set Prescaler
					-	●	●	-	-	00101110	2E	Select 1/3 & 1/6 of Frequency
					-	●	●	-	-	00101111	2F	Set 1/2 of Frequency
0	1	0	0=Ch1~3 1=Ch4~6	0=Addr 1=Data	-	3-Ch	6-Ch	6-Ch	6-Ch	xxxxxxxx	30~B6	FM (Alternate) - Addr/Data Write
					-	●	●	●	●	0011xxxx	30~3E	Detune & Multiple
					-	●	●	●	●	0100xxxx	40~4E	Total Level
					-	●	●	●	●	0101xxxx	50~5E	Key Scale & Attack Rate
					-	●	●	●	●	0110xxxx	60~6E	AM On & Decay Rate
					-	●	●	●	●	0111xxxx	70~7E	Sustain Rate
					-	●	●	●	●	1000xxxx	80~8E	Sustain Level & Release Rate
					-	●	●	●	●	1001xxxx	90~9E	SSG-Type Envelope Control
					-	●	●	●	●	101000xx	A0~A2	F-Number & Block
					-	●	●	●	●	101001xx	A4~A6	
					-	●	●	●	●	101010xx	A8~AA	3Ch-3Slot F-Number & Block
					-	●	●	●	●	101011xx	AC~AE	
					-	●	●	●	●	101100xx	B0~B2	Self-Feedback & Connection
					-	-	●	●	●	101101xx	B4~B6	L, R, AMS & PMS

					-	**-**	**1-Ch**	**-**	**-**	**000xxxxx**	**00~10**	**ADPCM - Addr/Data Write**
					-	-	●	-	-	00000000	00	Control 1
					-	-	●	-	-	00000001	01	Control 2
					-	-	●	-	-	00000010	02	Start Address (L)
					-	-	●	-	-	00000011	03	Start Address (H)
					-	-	●	-	-	00000100	04	Stop Address (L)
					-	-	●	-	-	00000101	05	Stop Address (H)
					-	-	●	-	-	00000110	06	Prescale (L)
0	**1**	**0**	**1**	**0=Addr 1=Data**	-	-	●	-	-	00000111	07	Prescale (H)
					-	-	●	-	-	00001000	08	ADPCM Data
					-	-	●	-	-	00001001	09	Delta-N (L)
					-	-	●	-	-	00001010	0A	Delta-N (H)
					-	-	●	-	-	00001011	0B	Level Control
					-	-	●	-	-	00001100	0C	Limit Address (L)
					-	-	●	-	-	00001101	0D	Limit Address (H)
					-	-	●	-	-	00001110	0E	DAC Data
					-	-	●	-	-	00001111	0F	(PCM Data)
					-	-	●	-	●	00010000	10	Flag Control
0	**0**	**1**	**1**	**1=Read**	**-**	**-**	●	**-**	**-**	**00001xxx**	**08, 0F**	**ADPCM & PCM - Data Read**
0	**0**	**1**	**0**	**1=Read**	**SSG**	**(SSG)**	**(SSG)**	**-**	**ALL***	**00001xxx**	**00~B6**	**REGISTERS - Data Read**
					-	**-**	●	**-**	●	**11111111**	**FF**	**STATUS 2 (Device Id) - Read**
0	**0**	**1**	**1**	**0=Read**	**-**	**-**	●	**-**	●	**xxxxxxxx**	**xx**	**STATUS 1 - Read**
0	**0**	**1**	**0**	**0=Read**	●	●	●	●	●	**xxxxxxxx**	**xx**	**STATUS 0 - Read**
1	**x**	**x**	**x**	**x**	●	●	●	●	●	**xxxxxxxx**	**xx**	**INACTIVE (High Impedance)**


J1
ZX 16K/48K Bus
U1
74HCT30N
U2A
74HCT02N
U2B
74HCT02N
U2C
74HCT02N
U3A
74HCT74N
U4
YMF288-M
OPN3 FM & SSG
X1
8MHz
Clock
U3B
74HCT74N
U2D
74HCT02N
Reset
U5
µPD6376
DAC
I/O Decode
Digital Power
Analog Power
U7
78L05
U6P
open hardware
Special thanks to:
JBS (Brazil),
NedoPC team (Russia)
NJM4580DD
U6A
U6B
Audio Pre-Amp & Output
J2
STEREO OUT
ZX Spectrum OPN3 FM & SSG Sound Interface
Explorer FM v0.3
14/02/23 07:55
Design by Szk @ 2023
Sheet: 1/1
Rev: 0.3