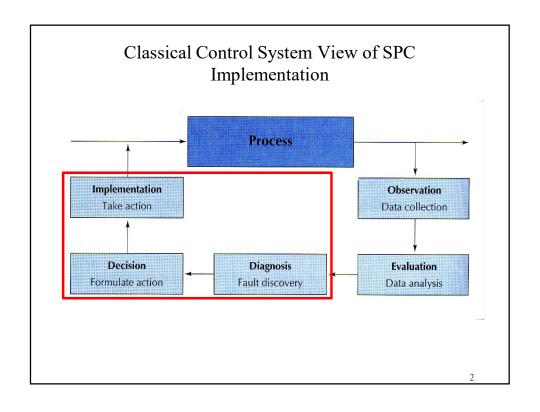
# Corrective Actions and Process Capability Index

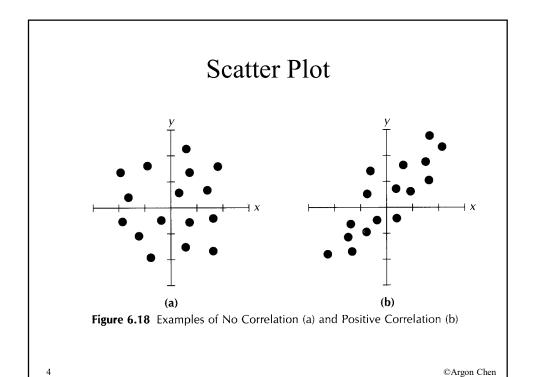
#### Argon Chen Graduate Institute of Industrial Eng'g National Taiwan University



#### Closing Control Loop: Causes and Actions

- Step 1: Find the relevant causes/factors:
  - Scatter Plot
  - Regression Analysis and Classification Tree
  - Machine learning
- Step 2: Prioritize defects/causes
  - Pareto Diagram
- Step 3: Find the root causes
  - Cause-and-Effect Diagram
- Step 4: Close the control loop
  - Out-of-Control Action Plans (OCAPS)
  - Advanced Process Control (APC/Run-to-Run Control)

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# Regression Analysis and Decision Trees Learning

- Regression analysis:
  - Simple and multiple regression will be covered
  - Stepwise, ridge, LASSO, etc.
- Decision trees: Data Mining courses
  - CART classification and Regression Tree
    - Gini Index/variance reduction
  - ID3/C4.5
    - Information Entropy/Information Gain/Information Gain Ratio
- Supervised machine learning

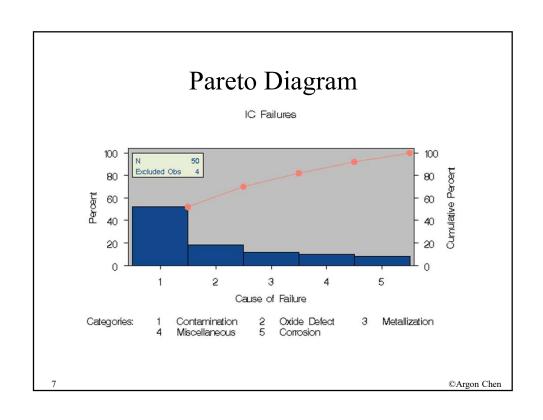
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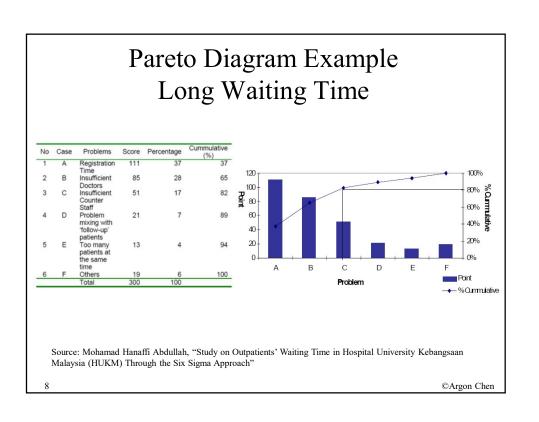
#### Pareto Principle

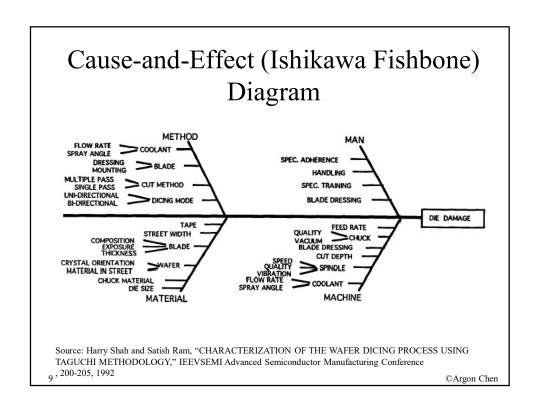
- Also known as the 80/20 rule, the law of the vital few, or the principle of factor sparsity
- Named after Italian economist Vilfredo Pareto who noted the 80/20 connection by showing that approximately 80% of the land in Italy was owned by 20% of the population
- Axiom of business management: "80% of sales come from 20% of clients"
- In computer science, Microsoft noted that by fixing the top 20% of the most-reported bugs, 80% of the related errors and crashes in a given system would be eliminated.

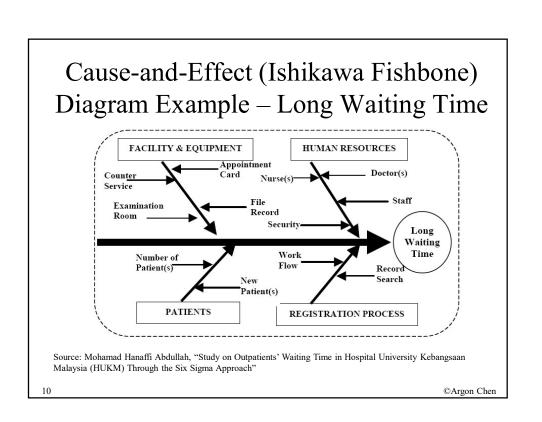
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3









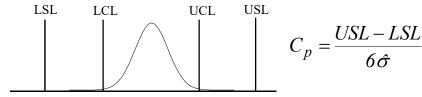
#### Taking Actions and Making Adjustments

- Out-of-Control Action Plans (OCAPS)
  - Detail the action to be taken once an out-ofcontrol situation is detected.
  - A specific flowchart, that leads the process engineer through the corrective procedure, may be provided for each unique process
- Advanced Process Control: Run-to-Run adjustments made to the process that are programmed to compensate for the size of the out-of-control measurement

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#### **Process Capability Assessment**

- What is a capable process?
- Assess process capability in terms of control chart application
- Comparing 6-s control window of *X*-chart to the specification window:



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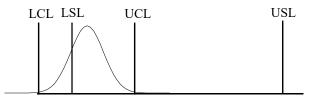
#### **Process Capability**

- The ability of the process to produce parts that conform to the engineering specifications (spec).
- A good process should
  - maintain a good statistical control
  - conform to engineering spec
- A process in statistical control but not meeting the spec?
  - the process is off-center from the nominal
  - the process variation is too large

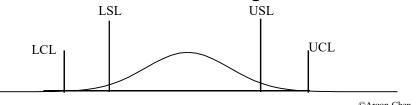
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• Process is off-center from the nominal



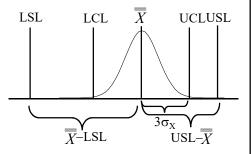
• Process variation is too large



#### **Process Capability Index**

$$C_{p} = \frac{USL - LSL}{6\sigma_{X}}$$

$$C_{pk} = min \left[ \frac{\overline{\overline{X}} - LSL}{3\sigma_{X}}, \frac{USL - \overline{\overline{X}}}{3\sigma_{X}} \right]$$



- Cp index measures potential capability (variation)
   Cpk index reflects the current process performance (mean and variation) and for process with asymmetric spec limits
- $C_{pk} \le C_p [C_{pk} = C_p \text{ when } \overline{\overline{X}} = (USL + LSL)/2]$

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#### Estimating Cp from Control Chart

• If a process is in statistical control,

$$C_p = \frac{USL - LSL}{6\hat{\sigma}_x} \qquad \hat{\sigma}_x = S_x$$

• Example:  $s_x$ = 0.00237, n=6, spec=(0.253, 0.263)

$$\hat{\sigma}_x = s_x = 0.00237$$

$$C_p = \frac{USL - LSL}{6\hat{\sigma}_X} = \frac{0.263 - 0.253}{6 \cdot 0.00237} = 0.72$$

## An Integrated PCI - $C_{pm}$

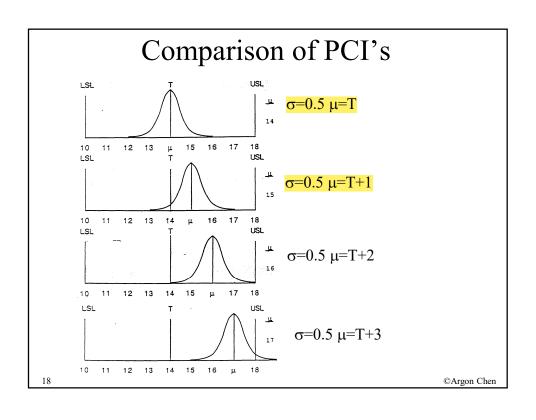
$$C_{pm} = \frac{USL - LSL}{6\widetilde{\sigma}}$$

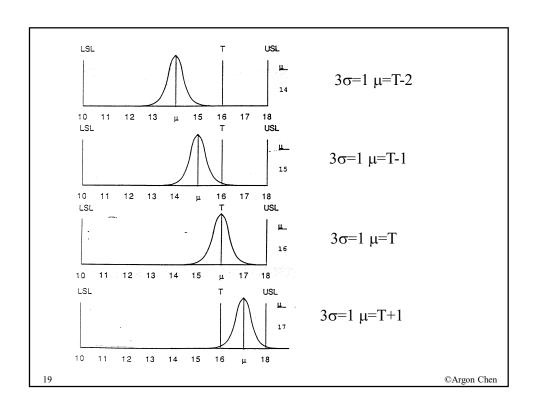
where 
$$\widetilde{\sigma} = \sqrt{E(X-T)^2} = \sqrt{\sigma^2 + (\mu - T)^2}$$

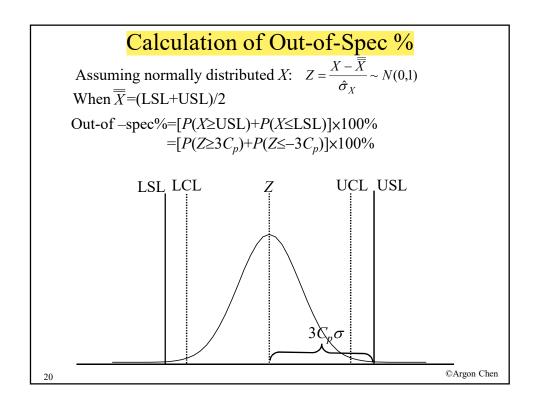
$$\hat{\sigma} = \sqrt{\frac{\sum_{i=1}^{n} (X_i - T)^2}{n}} = \sqrt{\hat{\sigma}^2 + (T - \overline{X})^2}$$

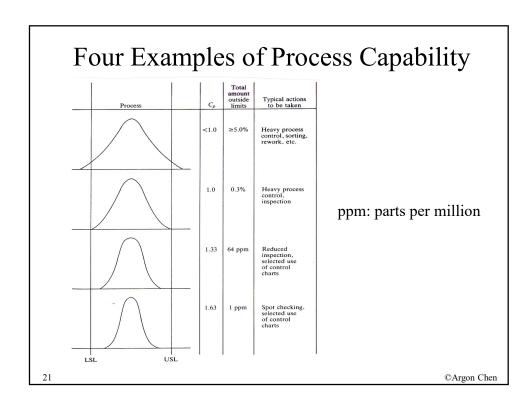
$$C_{pm}^* = \frac{\min[USL - T, T - LSL]}{3\widetilde{\sigma}}$$

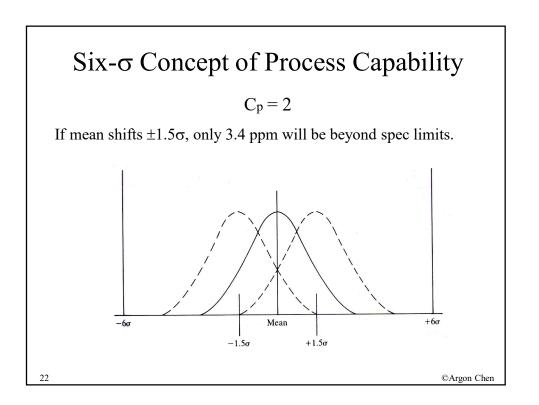
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#### How to improve Cpk?

- Reduce variation
  - remove special variation (SPC)
  - reduce common variation (process improvement, robust design)
- Adjust mean to nominal value

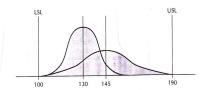
If 
$$\sigma_x = 10$$
 then  $Cpk = 1.0$  (mean = 130)

$$mean = 145, \, \sigma_x = 15$$

$$mean = 130, \, \sigma_x = 10$$

$$Cpk = 1.5 \text{ (mean = 145)}$$





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#### Steps in Assessment of Process Capability

- estimate  $\sigma_x = s_x$
- calculate  $C_p$ ,  $C_{pk}$
- calculate out-of-spec percentage using

$$Z = \frac{X - \overline{\overline{X}}}{\hat{\sigma}_X}$$

24

Evon	nla	• D	0.15		٦,	D D	roce	<b>N</b> GG
Exam	_		•	CD site4		within-wafer	within-wafer	288
					_	average	stdev	
wafer 1	60.52	59.84	59.34	60.62	59.59	59.98	0.57	
wafer 2	61.11	60.23	60.08	61.04	60.07	60.50	0.52	
wafer 3	60.43	60.09	59.58	59.67	59.67	59.89	0.36	
wafer 4	60.46	60.16	59.51	60.53	59.50	60.03	0.50	
wafer 5	61.08	60.10	59.87	61.02	60.17	60.45	0.56	
wafer 6	60.73	60.66	59.89	60.12	60.03	60.29	0.38	
wafer 7	60.17	59.46	58.84	60.26	59.64	59.67	0.58	
wafer 8	60.52	59.73	59.35	60.47	59.78	59.97	0.51	
wafer 9	60.28	60.02	59.15	59.59	59.39	59.69	0.46	
wafer 10	60.22	59.81	59.19	60.52	59.82	59.91	0.50	USL=62
wafer 11	60.61	59.69	59.51	60.46	59.69	59.99	0.50	_
wafer 12	60.06	60.00	59.28	59.55	59.43	59.67	0.35	LSL=58
wafer 13	60.37	59.93	59.15	60.49	59.71	59.93	0.54	LSL-36
wafer 14	60.77	60.02	59.97	60.84	59.77	60.27	0.49	
wafer 15	60.22	59.92	59.12	59.58	59.63	59.69	0.41	
wafer 16	60.13	59.73	59.07	60.59	60.04	59.91	0.56	
wafer 17	60.82	60.13	59.63	60.74	59.72	60.21	0.56	
wafer 18	60.60	60.57	59.84	60.22	60.03	60.25	0.33	
wafer 19	60.15	59.48	59.07	60.29	59.44	59.69	0.51	
wafer 20	60.73	60.00	59.58	60.83	60.11	60.25	0.52	
wafer 21	60.44	60.28	59.37	59.85	59.67	59.92	0.44	
wafer 22	60.56	60.23	59.59	60.63	59.58	60.12	0.51	
wafer 23	60.55	59.66	59.53	60.44	59.72	59.98	0.48	
wafer 24	60.18	60.16	59.46	59.83	59.58	59.84	0.33	
wafer 25	60.47	59.75	59.23	60.38	59.58	59.88	0.53	
wafer 26	60.22	59.79	59.20	60.15	59.47	59.77	0.44	
wafer 27	60.68	60.03	59.68	60.69	59.75	60.17	0.49	
wafer 28	60.29	60.54	59.43	59.75	60.00	60.00	0.44	
wafer 29	60.13	59.53	58.83	60.11	59.31	59.58	0.55	
wafer 30	60.33	59.69	59.60	60.40	59.73	59.95	0.38	
site average wafer-to-wafer site Stdev	60.46 0.27	59.97 0.31	59.43 0.32	60.32 0.43	59.72 0.23			
25					!			©Argon Chen

### **Overall Process Capability**

$$\hat{\sigma}_x = s_x = 0.49$$

$$C_p = \frac{USL - LSL}{6\sigma_X} = \frac{62 - 58}{6 \cdot 0.49} = 1.36$$

$$C_{pk} = \min\left[\frac{\overline{\overline{X}} - LSL}{3\sigma_X}, \frac{USL - \overline{\overline{X}}}{3\sigma_X}\right] = \min\left[\frac{59.98 - 58}{3 \cdot 0.49}, \frac{62 - 59.98}{3 \cdot 0.49}\right] = 1.347$$

#### Out-of-Spec Calculation

- $Z_L = \frac{LSL \overline{\overline{X}}}{\sigma_x} = \frac{58 59.98}{0.49} = -4.041 \implies P(X \le 58) \text{ is } \Psi(-4.041) = 2.66E-5$
- $Z_U = \frac{USL \overline{X}}{\sigma_x} = \frac{62 59.98}{0.49} = 4.122 \implies P(X \ge 62) \text{ is } 1-\Psi(4.122) = 1.88E-5$
- out-of-spec percentage = 2.66E-5+1.88E-5=4.54E-5=0.0045%

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### Site-1 Process Capability

$$\hat{\sigma}_x = s_{\text{site-1}} = 0.27$$

$$C_p = \frac{USL - LSL}{6\sigma_x} = \frac{62 - 58}{6 \cdot 0.27} = 2.47$$

$$C_{pk} = \min \left[ \frac{\overline{X} - LSL}{3\sigma_X}, \frac{USL - \overline{X}}{3\sigma_X} \right] = \min \left[ \frac{60.46 - 58}{3 \cdot 0.27}, \frac{62 - 60.46}{3 \cdot 0.27} \right] = 1.9$$