Yi-Hua Chung

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EDUCATION

Ph.D. Engineering in Electrical and Computer Engineering 09/2023 – Present
University of Wisconsin-Madison
- GPA: 4.00/4.00 (Fall 23 - Present)

Master of Science in Computer Science 02/2021 – 08/2022
Graduate Institute of Networking and Multimedia, National Taiwan University
- Thesis: Enlarging Quantum Circuit Simulation and Analysis with Non-Volatile Memories
- GPA: 4.25/4.30, Rank: 1/47

Bachelor of Science in Engineering 09/2016 – 01/2021
Biomechatronics Engineering, National Taiwan University
- Thesis: Development of a Small Intelligent Weather Station for Agricultural Applications
- GPA: 3.72/4.30

PUBLICATIONS

- Wan-Luan Lee, Shui Jiang, Dian-Lun Lin, Che Chang, Boyang Zhang, **Yi-Hua Chung**, Ulf Schlichtmann, Tsung-Yi Ho, and Tsung-Wei Huang, "iG-kway: Incremental k-way Graph Partitioning on GPU," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2025
- Cheng-Hsiang Chiu, Wan-Luan Lee, Boyang Zhang, **Yi-Hua Chung**, Che Chang, and Tsung-Wei Huang, "A Task-parallel Pipeline Programming Model with Token Dependency," *Workshop on Asynchronous Many-Task Systems and Applications (WAMTA)*, St. Louis, MO, 2025
- Shui Jiang, **Yi-Hua Chung**, Chih-Chun Chang, Tsung-Yi Ho, and Tsung-Wei Huang, "BQSim: GPU-accelerated Batch Quantum Circuit Simulation using Decision Diagram," *ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Rotterdam, Netherlands, 2025
- Boyang Zhang, Che Chang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yang Sui, Chih-Chun Chang, **Yi-Hua Chung**, Wan-Luan Lee, Zizheng Guo, Yibo Lin, and Tsung-Wei Huang, "iTAP: An Incremental Task Graph Partitioner for Task-parallel Static Timing Analysis," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, 2025
- Che Chang, Boyang Zhang, Cheng-Hsiang Chiu, Dian-Lun Lin, **Yi-Hua Chung**, Wan-Luan Lee, Zizheng Guo, Yibo Lin, and Tsung-Wei Huang, "PathGen: An Efficient Parallel Critical Path Generation Algorithm," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, 2025
- Chen, Han-Ting, **Yi-Hua Chung**, Vincent Hwang, and Bo-Yin Yang. "Algorithmic Views of Vectorized Polynomial Multipliers–NTRU." In *International Conference on Cryptology in India*, pp. 177-196. Cham: Springer Nature Switzerland, 2023
- Chen, Han-Ting, **Yi-Hua Chung**, Vincent Hwang, Chi-Ting Liu, and Bo-Yin Yang. "Algorithmic Views of Vectorized Polynomial Multipliers for NTRU and NTRU Prime (Long Paper)." *Cryptology ePrint Archive*, Report 2023/541, 2023. https://eprint.iacr.org/2023/541
- **Chung, Yi-Hua**. "Enlarging Quantum Circuit Simulation and Analysis with Non-Volatile Memories." Master's thesis, National Taiwan University, 2022
- **Chung, Yi-Hua**, Cheng-Jhih Shih, and Shih-Hao Hung. "Accelerating simulated quantum annealing with gpu and tensor cores." In *International Conference on High Performance Computing*, pp. 174-191. Cham: Springer International Publishing, 2022
- **Yi-Hua, Chung**, Huang Jun-Fu, Hu Yuan-Chen, and Huang Chen-Kang. "Development of a Small Intelligent Weather Station for Agricultural Applications." *Advances in Technology Innovation* 6, no. 2 (2021): 74

WORK EXPERIENCE

Graduate Research Assistant, supervised by Prof. Tsung-Wei Huang 08/2023 – present
University of Wisconsin-Madison
- Researched GPU-accelerated testing and verification algorithms, especially on fault simulation.
- Researched parallel and heterogeneous gate-sizing algorithms in timing-driven optimization.

Technical Intern; R&D Team, EDA Group 06/2024 – 12/2024
Synopsys Inc; CA
- Leveraging hybrid-computing of CPU-GPU co-processing into the Fusion Compiler tool.
- Accelerating Gate-sizing problem by adopting GPUs in Fusion Compiler tool with 4x-8x compared with 64 cores CPU version.

Full-time Research Assistant, supervised by Prof. Bo-Yin Yang 08/2022 – 03/2023
Institute of Information Science, Academia Sinica
- Accelerated big-integer multiplication by adopting the Fast NTT algorithm with warp primitive and inline PTX on GPU.
- Implemented lattice-based cryptosystems, including NTRU and NTRU Prime, on Cortex-A72 and accelerated the program by adopting fast NTT, Toom-Cook algorithm, and Schönhage-Strassen algorithm under the ARMv8-A architecture.

Research Assistant, supervised by Prof. Shih-Hao Hung 07/2021 – 08/2022
Performance, Applications, and Security Lab, National Taiwan University
- Researched quantum-related topics, including quantum annealing, quantum simulation, and quantum machine learning.
- Led a study group and assisted labmates on large-scale simulated quantum annealing (SQA) on multi-GPU.

Teaching Assistant, Computer Architecture
National Taiwan University
- Designed laboratories for students to implement simple ALU, FPU, CPU (Verilog), and pipelined CPU (RISC-V).

PROJECTS AND AWARDS

Variational Neural Annealing - Recurrent Neural Network Wave Functions
- Reproduced works from Waterloo University on solving 1D and 2D Ising problems with 1D and 2D RNN models and
- Compared performance and solution quality between variational neural annealing with classical SQA (Repo, Report).

2022 Quantum Computing Mentorship Program (QOSF) Cohort-5
- Designed and constructed oracle and diffuse functions of Grover's algorithm for solving quantum tic-tac-toe problems (Repo).

2D Pattern Matching for DNA sequences
NTU-IBM Q System Q-Camp, 2020.
- Received **Outstanding Performance Award** in a hackathon organized by IBM and National Taiwan University (Repo1, 2).

AWARDS

ACM/IEEE DAC Young Student Fellowship, 2024

NTUEE-1975 Innovation and Entrepreneurship Fund Award
College of Electrical Engineering and Computer Science, National Taiwan University

2022 Future Tech Awards,
National Science and Technology Council, R.O.C.

Best Paper Award
9th International Multi-Conference on Engineering and Technology Innovation 2020

Outstanding Performance Award
NTU-IBM Q System 2020 Q-Camp, Hackathon, Sep 2020

SKILLS

C/C++, CUDA C/C++, OpenMP, ARM Intrinsic, ARM Assembly, Linux, Shell — *Expert*

Python, C#, Qiskit, JavaScript, WebGL — *Experienced*