753 F.3d 1253
United States Court of Appeals,
Federal Circuit.

In re RAMBUS, INC.

No. 2013–1192.
|
June 4, 2014.

Synopsis
Background: Patent Trial and Appeal Board found in an inter partes reexamination that the claims of a patent that disclosed a method and system for improving the efficiency of computer memory had been anticipated. Patentee appealed.

[Holding:] The Court of Appeals, Reyna, Circuit Judge, held that prior art did not disclose "a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data," and thus did not anticipate patent.

Reversed.

West Headnotes (8)

[1] Patents Other Postissuance Proceedings

Live controversy existed regarding patentability of patentee's claims that remained before the Court of Appeals for resolution, even after withdrawal of requestor of inter partes reexamination. 35 U.S.C.A. § 315(a)(1).

Cases that cite this headnote

[2] Patents Construction and Operation of Reexamined Patents

Patent claims are generally given their broadest reasonable interpretation consistent with the specification during reexamination; this claim construction standard is justified, at least in part, because a patentee is able to amend its claims during reexamination.

15 Cases that cite this headnote

[3] Patents Request for reexamination

If a reexamination involves claims of an expired patent, a patentee is unable to make claim amendments and the Patent and Trademark Office (PTO) applies the claim construction principles outlined in *Phillips v. AWH*.

8 Cases that cite this headnote

[4] Patents Single reference disclosing every element or limitation of claim

A **patent** is anticipated if a single prior art reference discloses each and every limitation of the claimed invention.

4 Cases that cite this headnote

[5] **Patents** Novelty;anticipation

Patent anticipation is a question of fact reviewed for substantial evidence, where substantial evidence is more than a "mere scintilla of evidence" but something less than the "weight of the evidence."

7 Cases that cite this headnote

[6] **Patents** Computers and Software

Prior art did not disclose "a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data," and thus did not anticipate **patent** that disclosed a method and system for improving the efficiency of computer memory, since prior art did not include known delay time, but rather had indefinite delay time based upon arbitration, busy memory devices, and other functions.

Cases that cite this headnote

[7] **Patents** In general;utility

US **Patent** 4,734,909. Cited as Prior Art.

1 Cases that cite this headnote

[8] **Patents** In general;utility

US **Patent** 6,426,916. Cited.

Cases that cite this headnote

Attorneys and Law Firms

***1254** James R. Barney, Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, of Washington, DC, argued for appellant. With him on the brief were J. Michael Jakes, Molly R. Silfen, and Aidan C. Skoyles. Of counsel was Kathleen Daley.

Before RADER, [*] MOORE and REYNA, Circuit Judges.

Opinion

REYNA, Circuit Judge.

This is an appeal from an inter partes reexamination of claims 26 and 28 of U.S. **Patent** No. 6,426,916 ("the #916 **patent**"). The **Patent** Trial and Appeal Board ("Board") at the United States **Patent** and Trademark Office ("PTO") found that the claims were anticipated by U.S. **Patent** No. 4,734,909 to Bennett ("Bennett"). **Patent** owner Rambus, Inc. ("Rambus") appeals the Board's anticipation decision, arguing that Bennett does not disclose the claimed "value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data."

[1] After oral argument, requestor Micron Technology, Inc. ("Micron") moved to withdraw from this case, which we granted in a separate order. Rambus has the right to appeal the Board's rejection of its claims irrespective of Micron's participation in this appeal. *See* 35 U.S.C. § 315(a)(1) (2006). Thus, despite Micron's withdrawal, a live controversy regarding the **patentability** of Rambus's claims remains before us for resolution. [1] We do not reach Micron's alternate grounds for affirming the Board, because these arguments have been withdrawn. As discussed below, we reverse the Board's anticipation decision as unsupported by substantial evidence.

BACKGROUND

The #916 **patent** discloses a method and system for improving the efficiency of computer memory. Broadly speaking, a computer may need to transfer data between different memory devices, such as between a memory controller (sometimes called a master) and a memory device that stores data (sometimes called a slave). This data may be transferred via a "bus," such as a series of wires, or "lines," that connect the memory device and the controller. Some memory systems include a wait signal that is sent, sometimes over a wait line, from a memory device to a memory controller that says the memory device is not ready to receive or send data. The wait signal may also indicate when the memory device will be ready to send data.

Relevant to this appeal, signals may be transferred via a bus using either "dedicated" lines or "multiplexed" lines. If a signal has a dedicated line on the bus it means that this signal does not share its line with other signals. This can be analogized to a multiple lane road where each car (signal) has its own lane, which it can travel on at any time without interfering with a car on another lane. By contrast, ***1255** two signals may be multiplexed on a single line. For example, if a "wait" signal and a "data" signal are time-division multiplexed, they share a single line on the bus in a time based manner and cannot use the line at the same time. This may be analogized to a one lane road that cars cannot drive on at the same time.

If two memory devices want to use the bus at the same time but, for technical reasons not relevant here, they cannot, the process by which the computer chooses which device goes first is called "arbitration." A memory device may be ready to send data to a memory controller but, if it "loses" arbitration, it will have to wait until the device that won arbitration has finished using the bus.

The #916 **patent** attempts to improve this general memory transfer system with the addition of two features: (1) an external clock to synchronize the timing of the data transfer and, (2) for a particular memory transfer request, delaying the transfer by a specific, known amount of time. For example, when a memory controller requests data from a memory device, the controller will ask the memory device to begin transferring the data after a certain number of clock cycles (the specification refers to this as a "delay"). Because the controller will know precisely when the data will be transferred on the bus, it can be prepared to receive it and can also use the bus during the delay to perform other tasks.

While there are two necessary features of the design disclosed in the #916 **patent** (the external clock and the known delay time), only the delay time is at issue in this appeal. With the relevant language emphasized, claim 26 recites:

> A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:
>
> clock receiver circuitry to receive an external clock signal;
>
> first input receiver circuitry to sample block size information synchronously with respect to the external clock signal, wherein the block size information is representative of an amount of data to be output by the memory device in response to a first operation code;

a register which stores a *value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data;*

and a plurality of output drivers to output the amount of data in response to the first operation code and after the amount of time transpires.

(emphasis added). Claim 28 depends on 26 and recites:

> The memory device of claim 26 wherein in response to a second operation code, the value is stored in the register.

The parties disputed before the PTO whether Bennett discloses "a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data." The examiner found this limitation lacking in Bennett. The Board disagreed and found that "Parameter VI" in Bennett discloses the claimed "value." Because the Board's conclusion is not supported by substantial evidence, we reverse.

DISCUSSION

[2] **[3]** Claims are generally given their "broadest reasonable interpretation" consistent with the specification during reexamination. *See, e.g., In re Yamamoto,* 740 F.2d 1569 (Fed.Cir.1984). This claim construction standard is justified, at least in part, because a patentee is able to amend its claims during reexamination. *See, e.g., Exxon Research & Eng'g Co. v. United States,* 265 F.3d 1371, 1380 (Fed.Cir.2001). ***1256** If, as is the case here, a reexamination involves claims of an expired **patent**, a patentee is unable to make claim amendments and the PTO applies the claim construction principles outlined by this court in *Phillips v. AWH Corp.,* 415 F.3d 1303 (Fed.Cir.2005). *See, e.g., In re Rambus, Inc.,* 694 F.3d 42, 46 (Fed.Cir.2012); *see also* M.P.E.P. § 2258(G) ("In a reexamination proceeding involving claims of an expired **patent**, claim construction pursuant to the principle[s] set forth by the court in *Phillips,* ... should be applied since the expired claim[s] are not subject to amendment."); 1 **Patent** Office Litigation § 4:70 (justifying the shift from the broadest reasonable interpretation to the standard used by district courts because "claims may not be amended in an expired **patent** and the sole basis for the 'broadest reasonable interpretation' rubric is the ability to amend claims"). In this appeal, we apply the *Phillips* claim construction standards.

[4] **[5]** A **patent** is anticipated "if a single prior art reference discloses each and every limitation of the claimed invention." *Schering Corp. v. Geneva Pharm.,* 339 F.3d 1373, 1377 (Fed.Cir.2003) (citing *Lewmar Marine, Inc. v. Barient, Inc.,* 827 F.2d 744, 747 (Fed.Cir.1987). Anticipation is a question of fact reviewed for substantial evidence. *See In re Baxter Travenol Labs.,* 952 F.2d 388, 390 (Fed.Cir.1991). Substantial evidence is more than a "mere scintilla of evidence" but something less than the "weight of the evidence." *In re Kotzab,* 217 F.3d 1365, 1369 (Fed.Cir.2000) (*citing in re Gartside,* 203 F.3d 1305, 1316 (Fed.Cir.2000)).

ANTICIPATION

[6] The Board relied on Figs. 25a and 25b in Bennett, and the related "Parameter VI." These figures are schematic representations of operations occurring on a memory bus. Parameter VI is the internal parameter in Bennett that determines whether the data and wait lines in these figures are dedicated or multiplexed. Specifically, when Parameter VI is 1 (as in Fig. 25a), these lines are multiplexed, and when it is 3 (as in Fig. 25b), each signal has a dedicated line. As explained in more detail below, the data transfer in Fig. 25a takes place one clock cycle later than the data transfer in Fig. 25b.

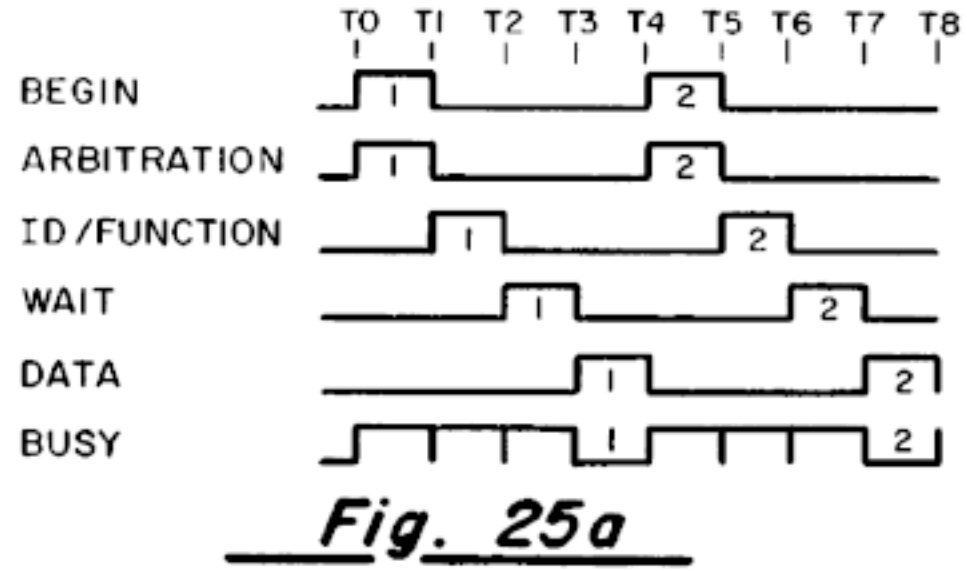

Fig. 25a

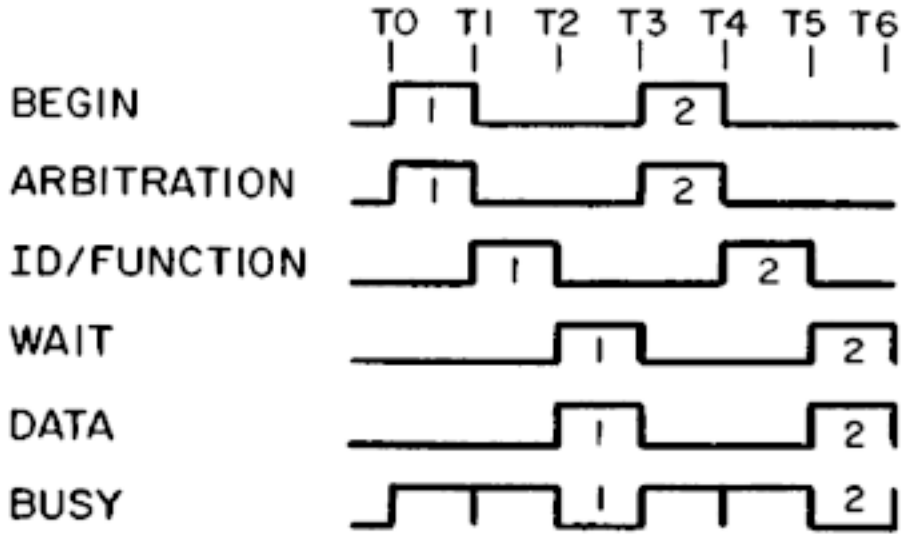

Fig. 25b

***1257** The labels at the top of Figs. 25a and b (T0, T1, T2, etc.) refer to clock cycles. Bennett has assumed for simplicity that each operation in the figures (begin signal, arbitration, wait signal, data transfer, etc.) takes exactly one clock cycle.

In Fig. 25b, the wait and data signals each have dedicated lines. As such, these signals can both be sent on the bus at the same time. Specifically, the first wait and data signals are both sent between the T2 and T3 clock cycles. In Fig. 25a, by contrast, the wait and data signals are multiplexed, so they cannot use the bus at the same time. As a result, the first wait signal is sent between T2 and T3 but the first data signal is sent one clock cycle later, between T3 and T4.

Micron's argument below, with which the Board agreed, is as follows. The multiplexed lines in Fig. 25a cause a delay of known value (one clock cycle) before data transfer. Setting Parameter VI to 1 causes the lines to be multiplexed. Therefore, Parameter VI is a "value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data."

Rambus responds that these figures are simplified, hypothetical, illustrations of how the invention in Bennett works in theory and not schematics of how Bennett works. For instance, Rambus points out that, in practice, arbitration takes an unknown amount of time because a device may lose arbitration a number of times in a row. Rambus argues that the wait signal may also delay the data transfer for an indeterminate amount of time if it indicates that the memory device is busy. Thus, according to Rambus, when the invention disclosed in Bennett actually functions, it does not include a known delay time; rather, it has an indefinite delay ***1258** time based upon arbitration, busy memory devices, and other functions.

We agree with Rambus. In Figs. 25a and b of Bennett, Parameter VI is only "representative" of one source of delay because the actual delay can be longer due to other factors. Switching this parameter from 1 to 3 does not necessarily create a one clock cycle delay before data is transferred due to further potential delay that may result from arbitration. As such, Parameter VI is not a "value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data."

As Rambus points out, arbitration may take an indeterminate amount of time because a memory device may "lose" arbitration on successive occasions. If arbitration in Fig. 25b happens to take longer than in Fig 25a, the memory system with multiplexed lines (Fig.25a) may actually have less delay before data transfer. Similarly, a busy memory device with dedicated lines may have a longer delay, due to wait signals, than an available device with multiplexed lines. Because of these two additional, indefinite, sources of delay, changing Parameter VI from 1 to 3 will not produce a set amount of time after which data is transferred. Therefore, Parameter VI is not "representative" of an amount of time after which data is transferred.

The Board found that, in at least some embodiments in Bennett, Parameter VI meets the claim limitation at issue. Specifically, when the embodiments in Fig. 25a and b both (1) win arbitration on the first attempt and (2) are not busy for an indeterminate amount of time, then Parameter VI is a "value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data." We disagree. A value cannot "represent" an "amount of time" if there are additional factors, wholly unrepresented by that value, that necessarily impact, or represent, the "amount of time." Certainly, Parameter VI is one factor that may affect the amount of time that passes before data is transferred but it does not represent that time. Accordingly, we reverse the Board's decision that Bennett anticipates claims 26 and 28 of the #916 **patent**.

REVERSED

All Citations

753 F.3d 1253, 111 U.S.P.Q.2d 1077

Footnotes

* Randall R. Rader vacated the position of Chief Judge on May 30, 2014.

1 We note that the PTO does not seek to intervene in this case.