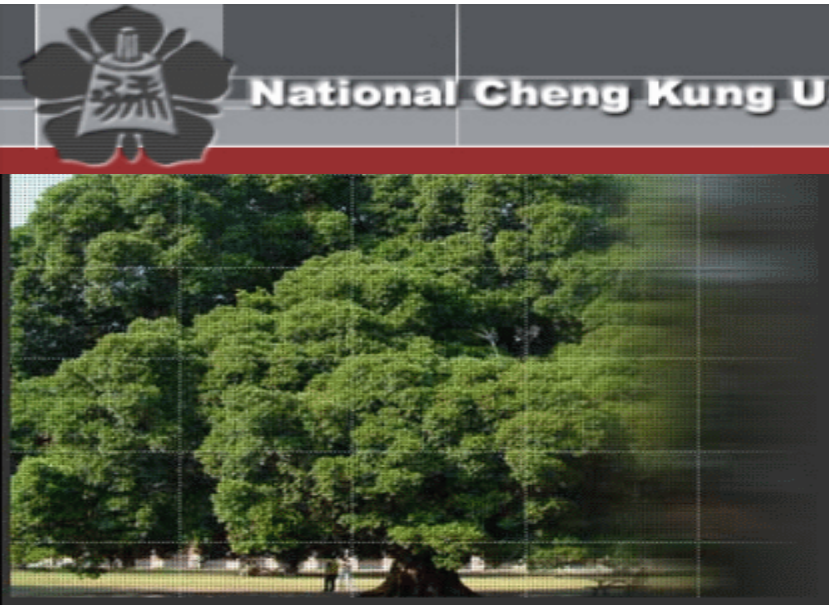
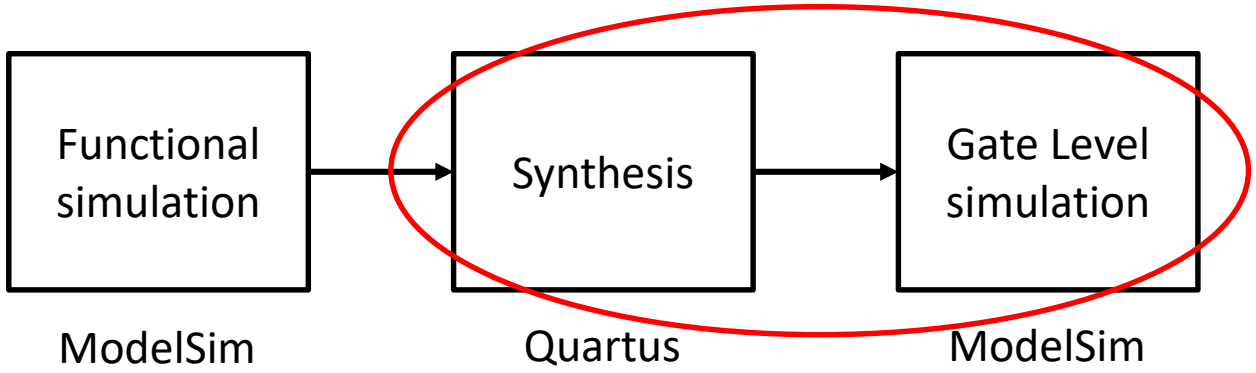


數位IC設計 Tool安裝&作業模擬教學

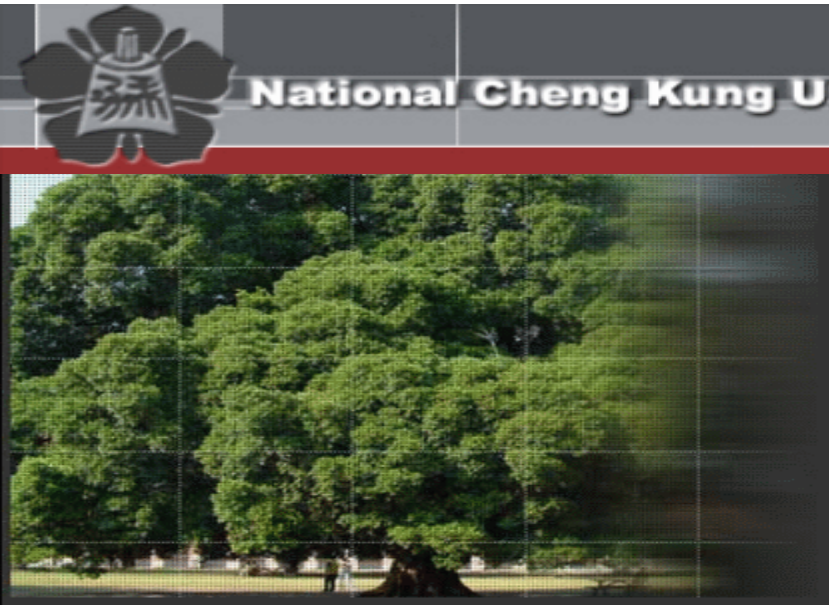
NCKU CSIE DICLAB

The simulation process

- The simulation process and the necessary tools in this class



- The tools can be downloaded from :
  - https://www.intel.com/content/www/us/en/software/programmable/quartus-prime/download.html#



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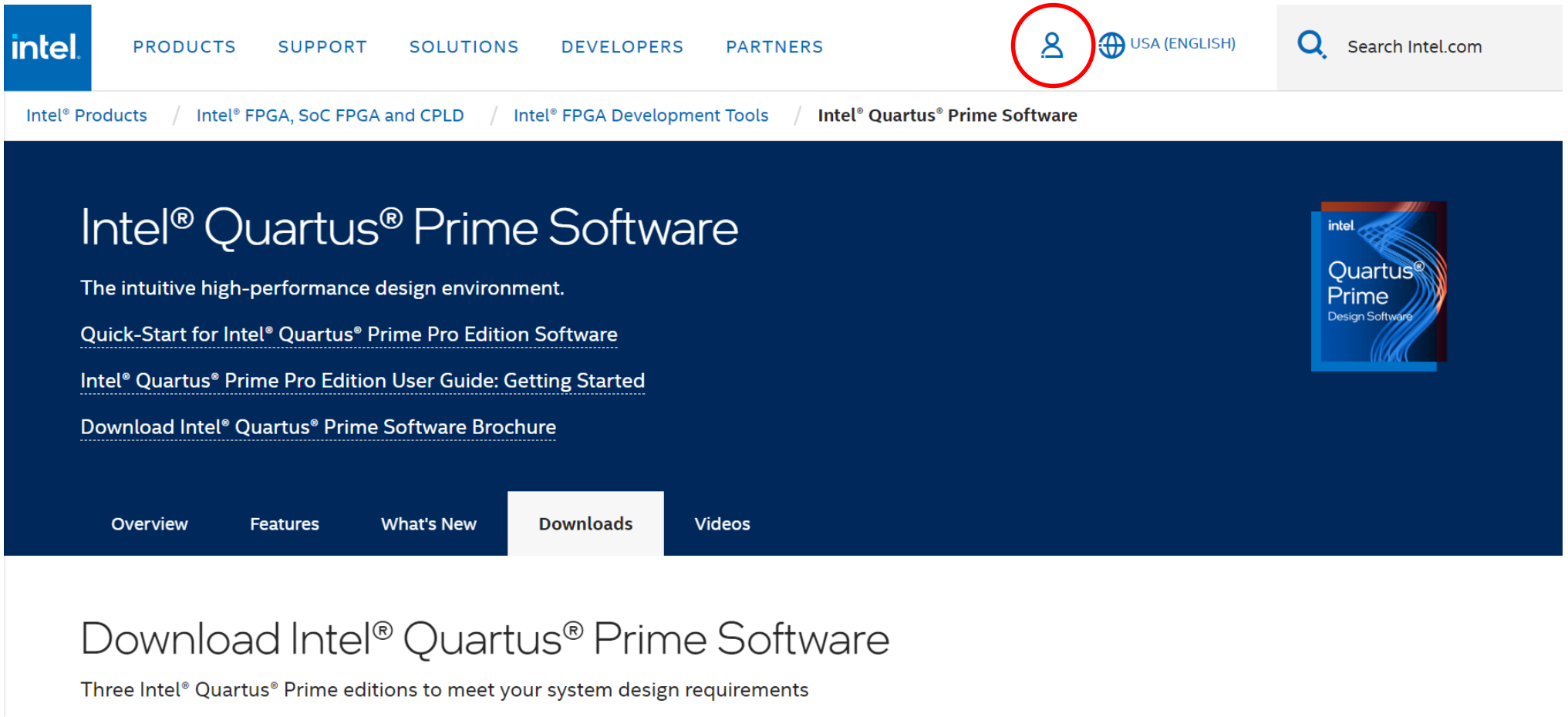
Download and install Quartus

Download and install Quartus

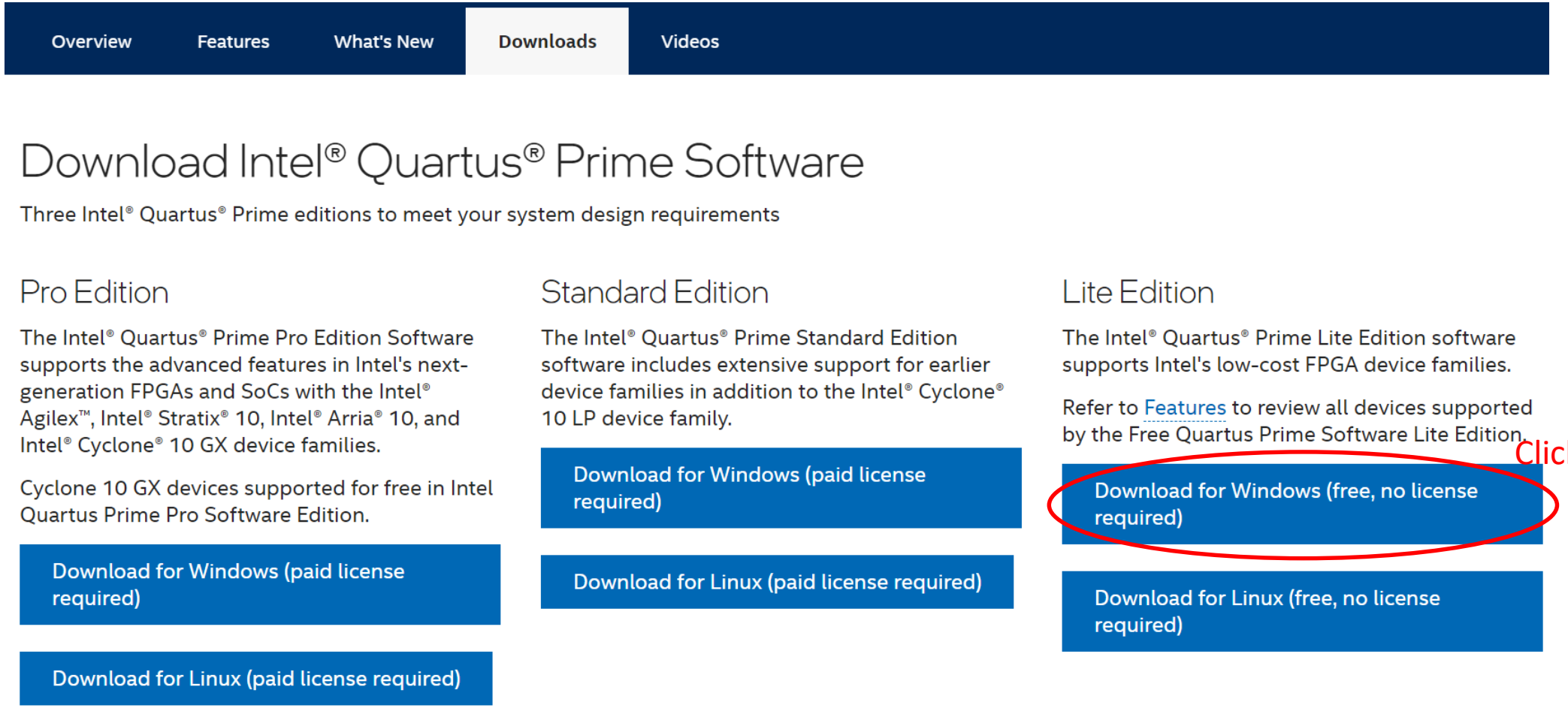
- Step 1: Register and sign in

Click here to create an account and sign in



Download and install Quartus

- Step 2: Click “ Download for Windows(free, no license required)“



Download and install Quartus

- Step 3: Select software version (20.1.1)

Intel® Quartus® Prime Lite Edition Design Software Version 20.1.1 for Windows

ID	Date	Version
660907	11/22/2020	20.1.1

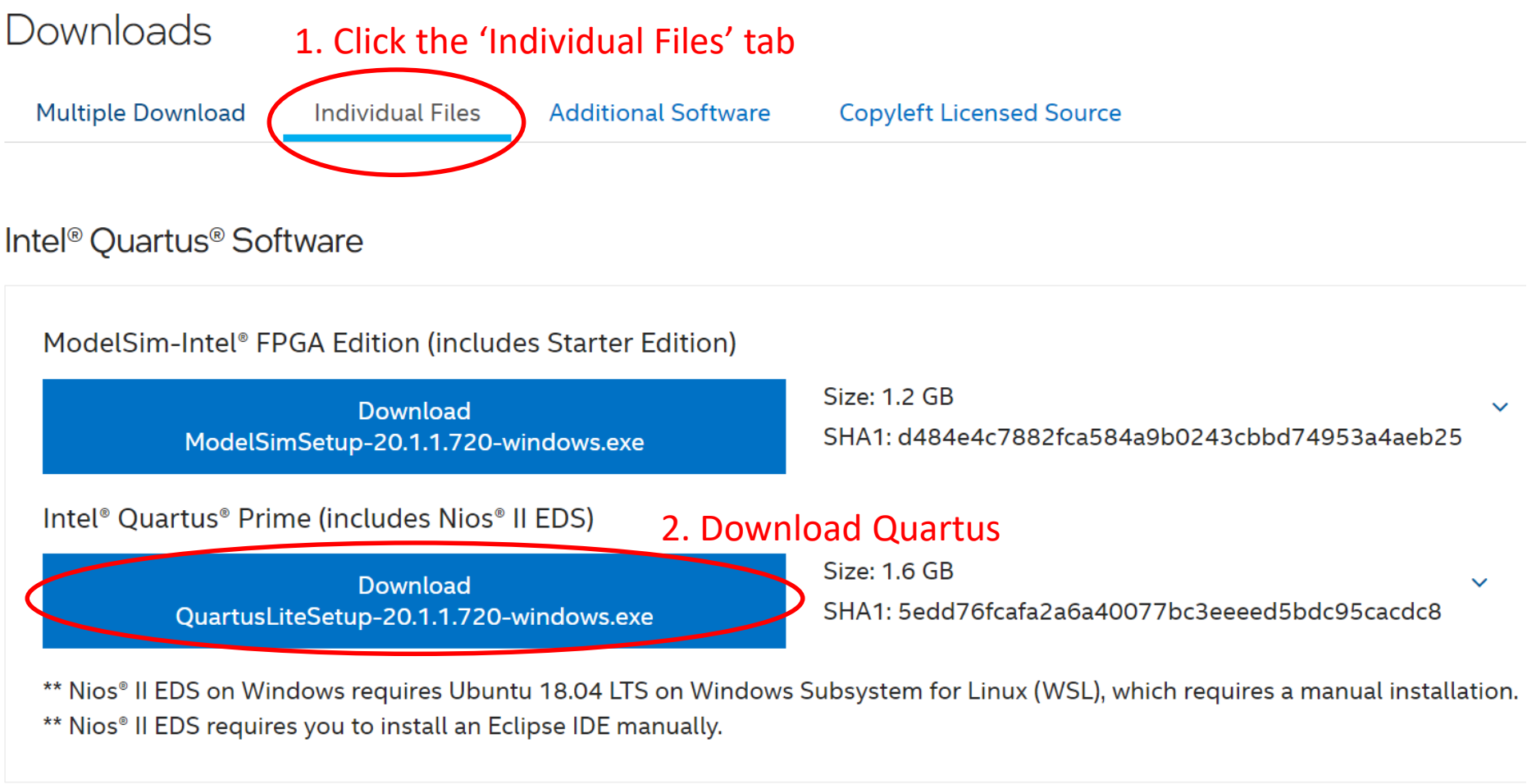
Select version 20.1.1

A newer version of this software is available, which includes functional and security updates. Customers should click here to update to the latest version.

Users should upgrade to the latest version of the Intel® Quartus® Prime Design Software. The selected version does not include the latest functional and security updates. If you must use this version of software, follow the technical recommendations to help improve security. For critical support requests, please contact our support team.

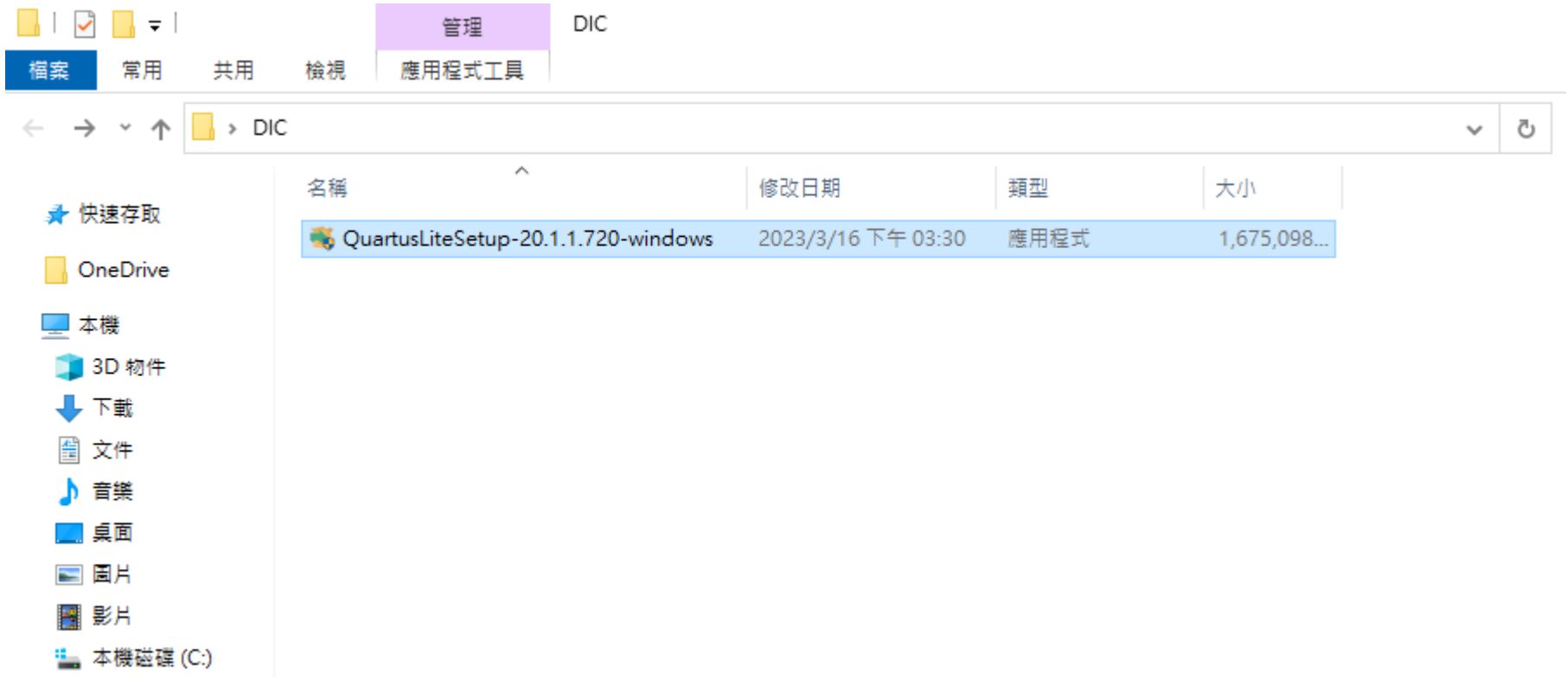
Download and install Quartus

- Step 4: Download Quartus setup execution file



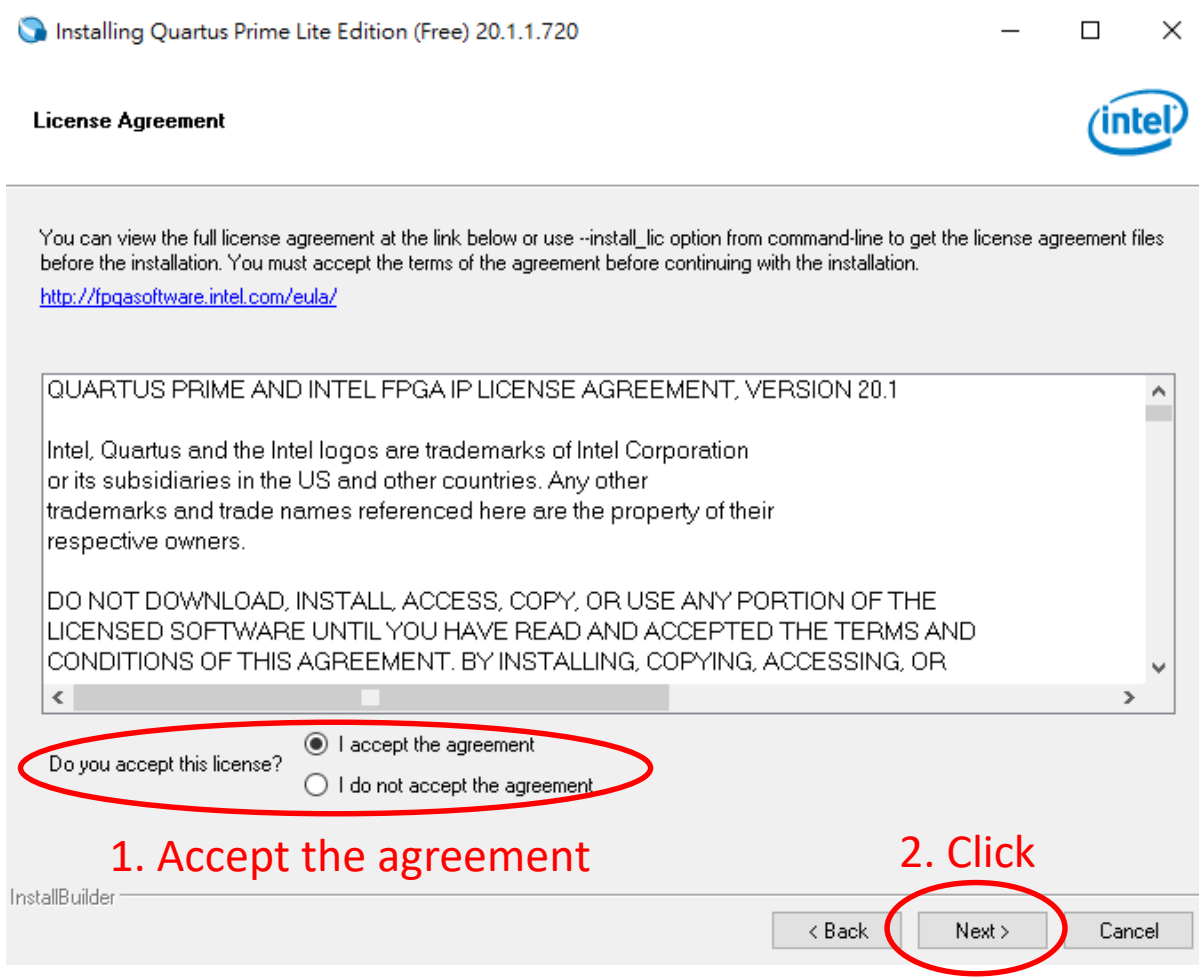
Download and install Quartus

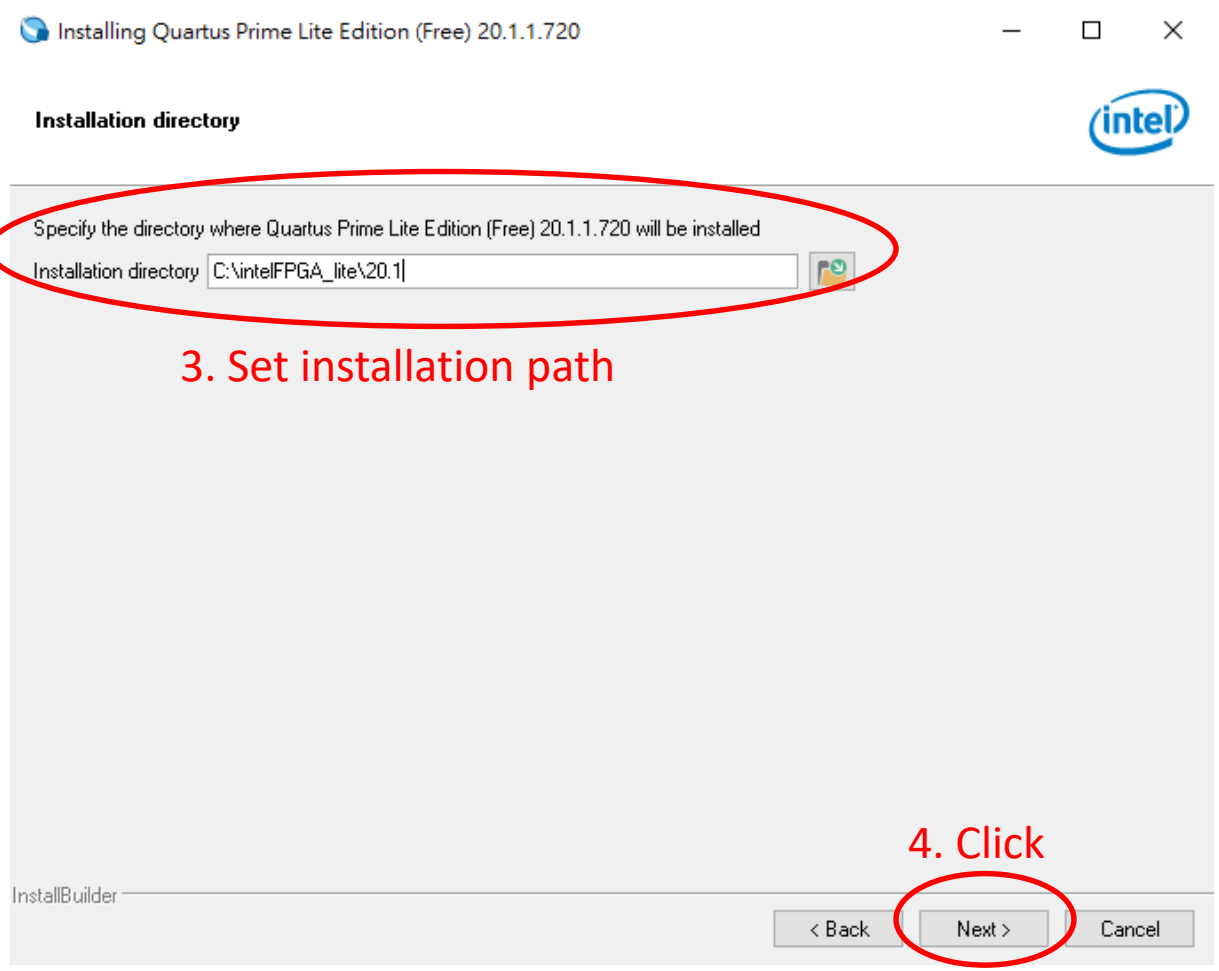
- Step 5: Installation



Download and install Quartus

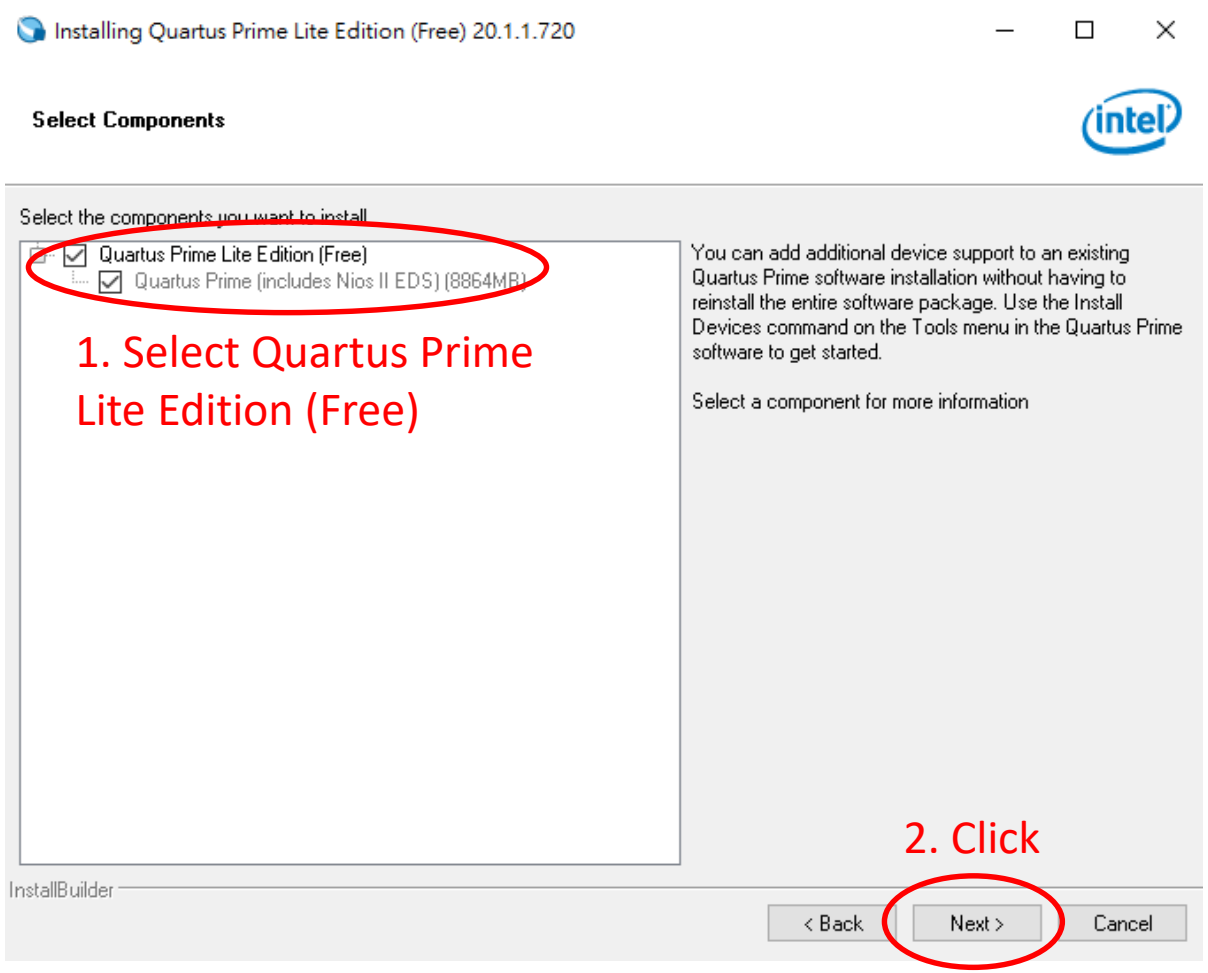
- Step 5: Installation

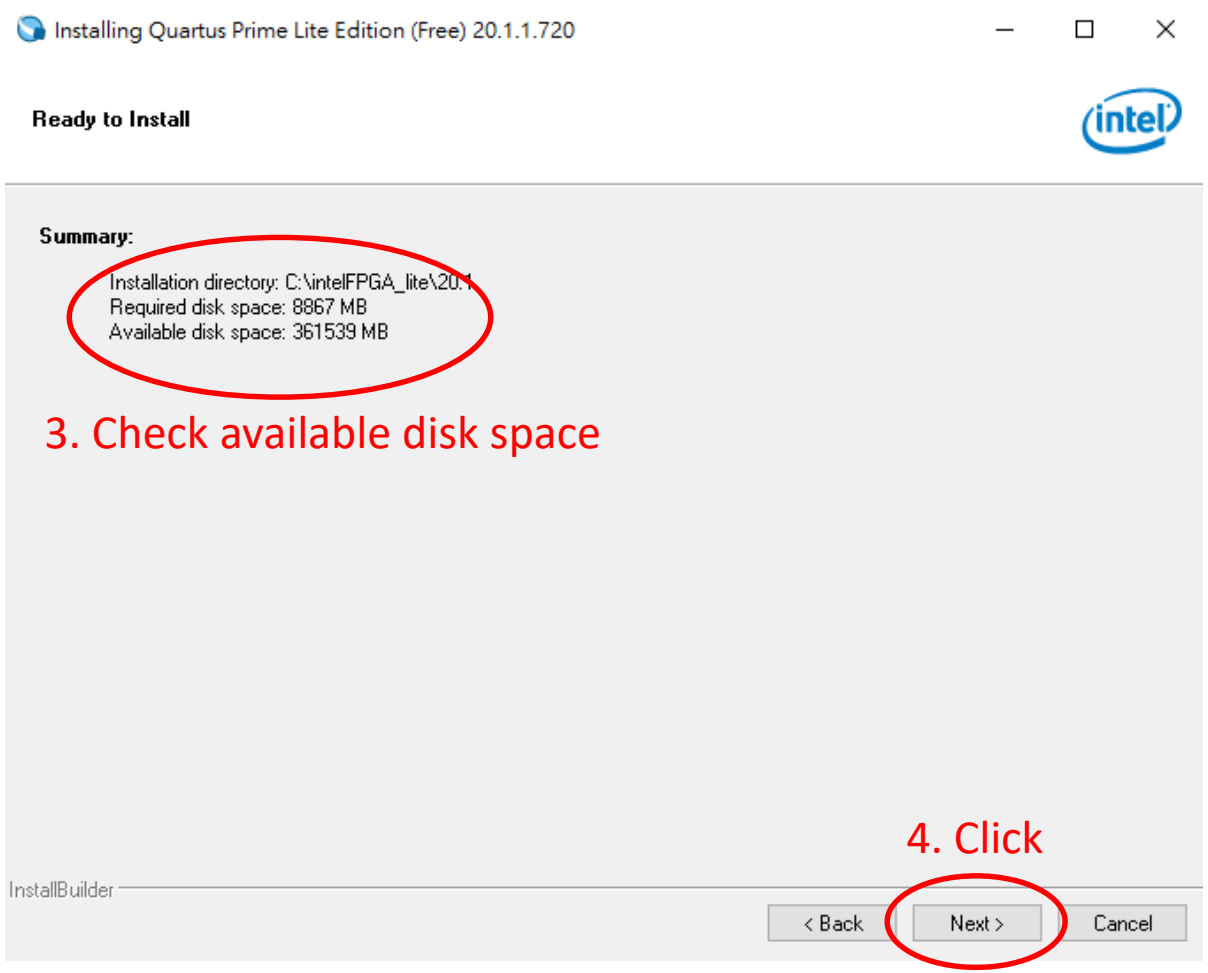




Download and install Quartus

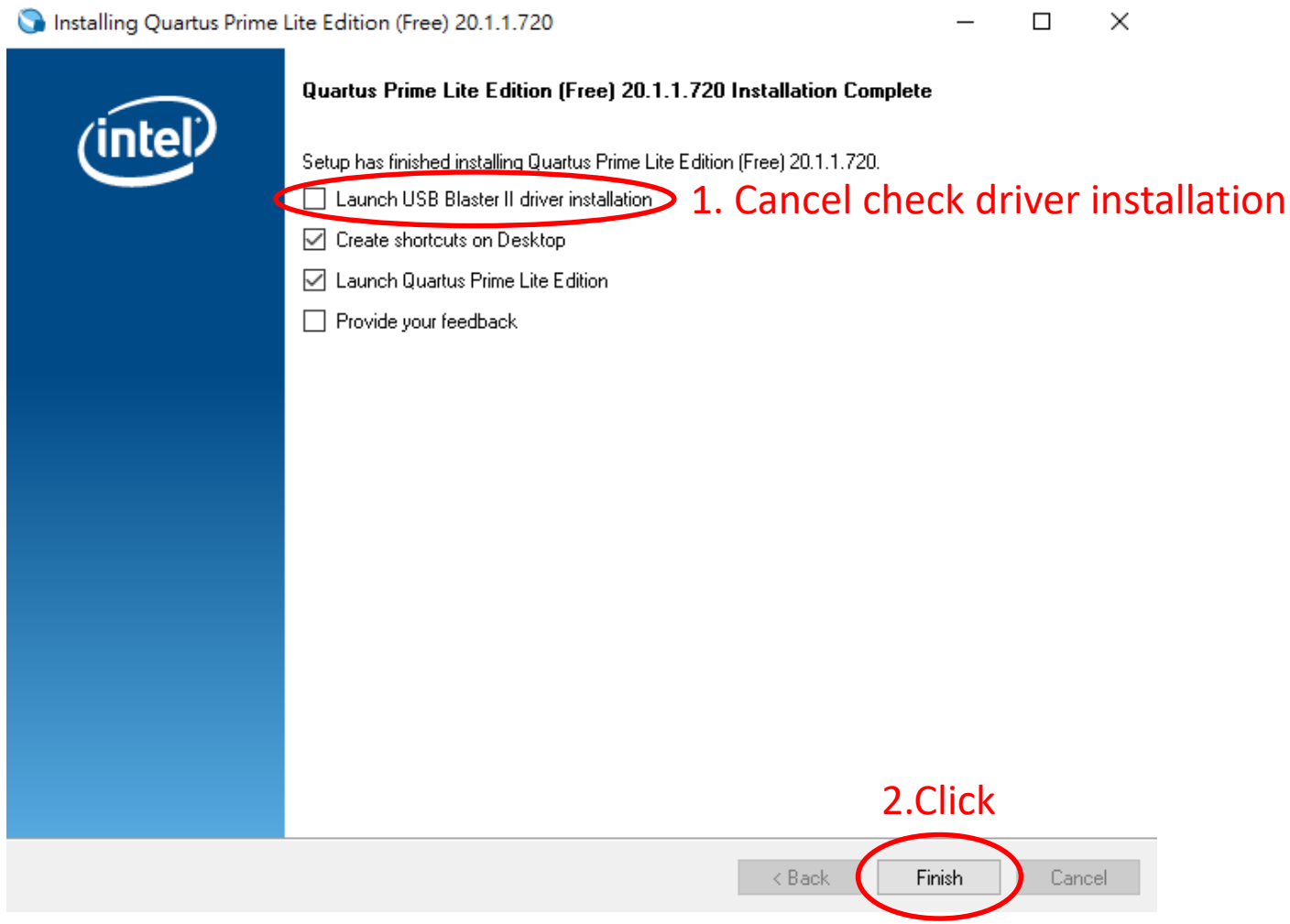
- Step 5: Installation





Download and install Quartus

- Step 5: Installation



Download and install Quartus

- Step 6: Download device support file

Devices

Intel® Arria® II Device Support

Download
arria_lite-20.1.1.720.qdz

Size: 499.1 MB
SHA1: e0508f997e1f395e247a6490f1710e36a1f528d1

Intel® Cyclone® IV Device Support

Download Cyclone IV Device Support

Download
cyclone-20.1.1.720.qdz

Size: 466 MB
SHA1: 5447aa416749edf5bae5f68dcc734c43e8db6a67

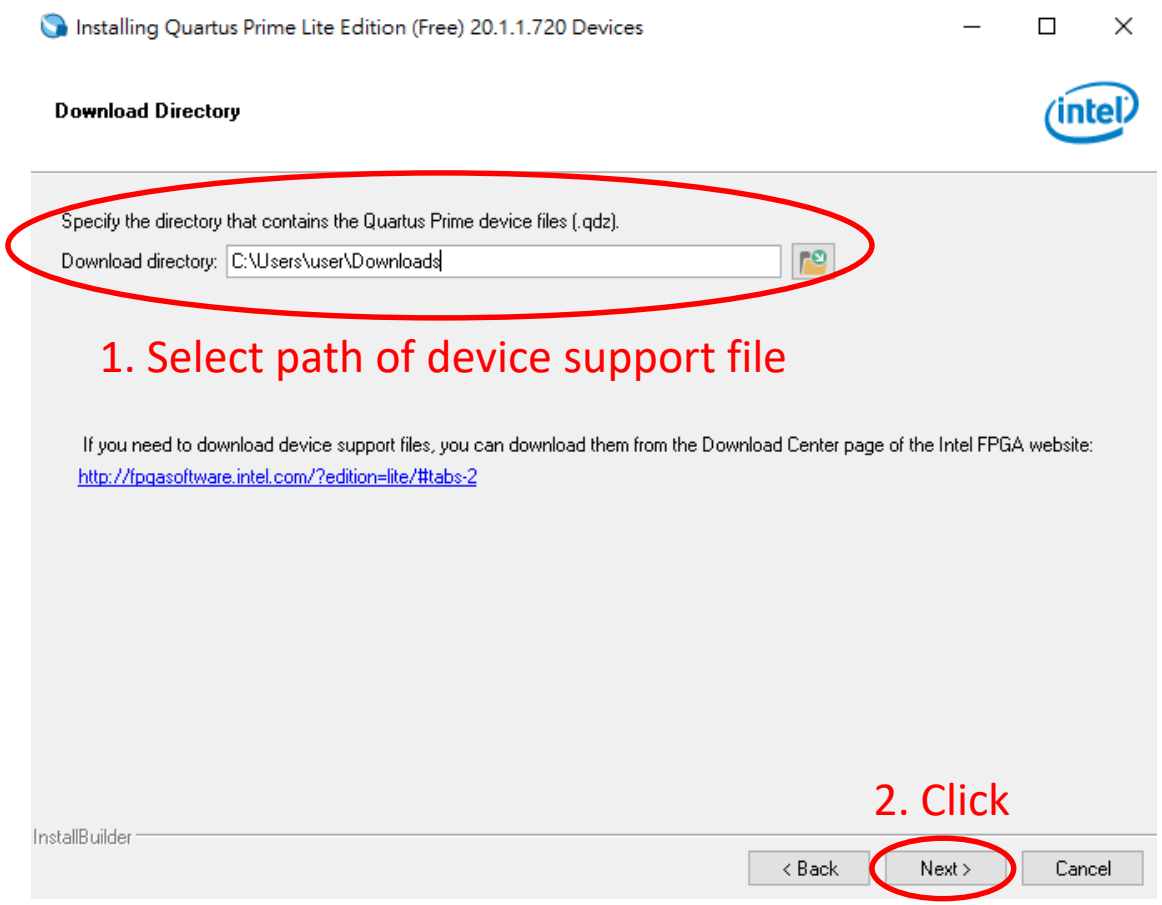
Intel® Cyclone® 10 LP Device Support

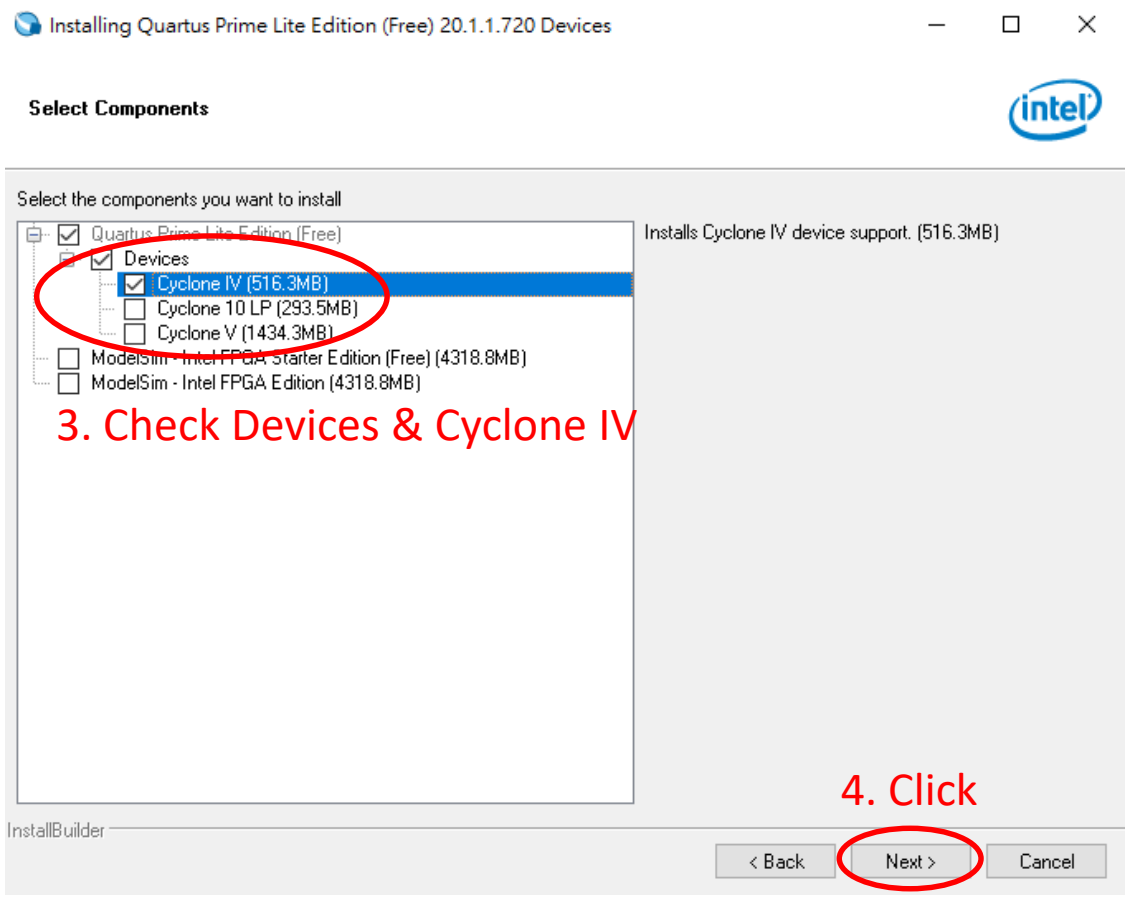
Download
cyclone10lp-20.1.1.720.qdz

Size: 265.7 MB
SHA1: 93ab293a69b1760847f26b996d043e20bd465f26

Download and install Quartus

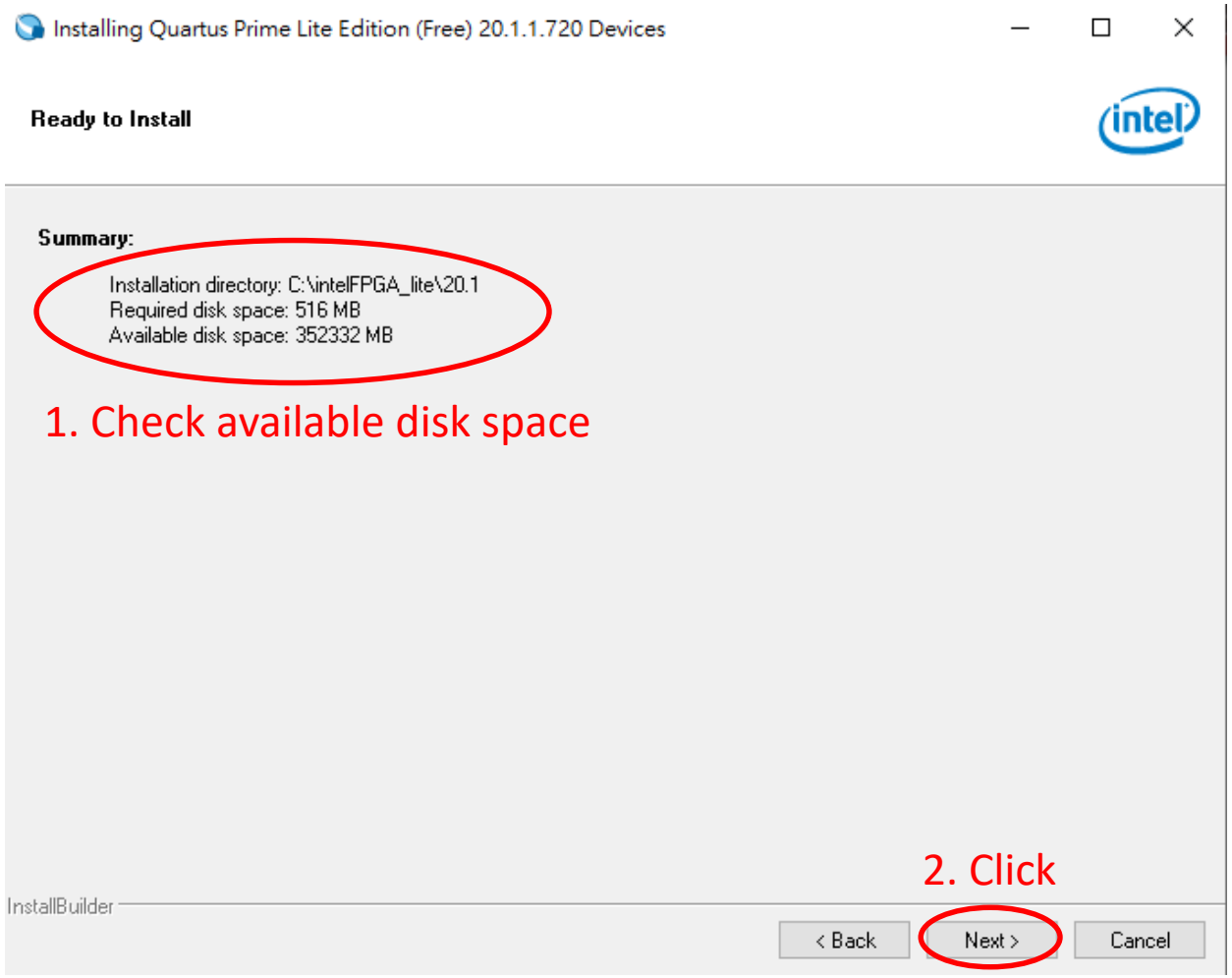
- Step 7: Install Device
  - Windows搜尋 > Device Installer

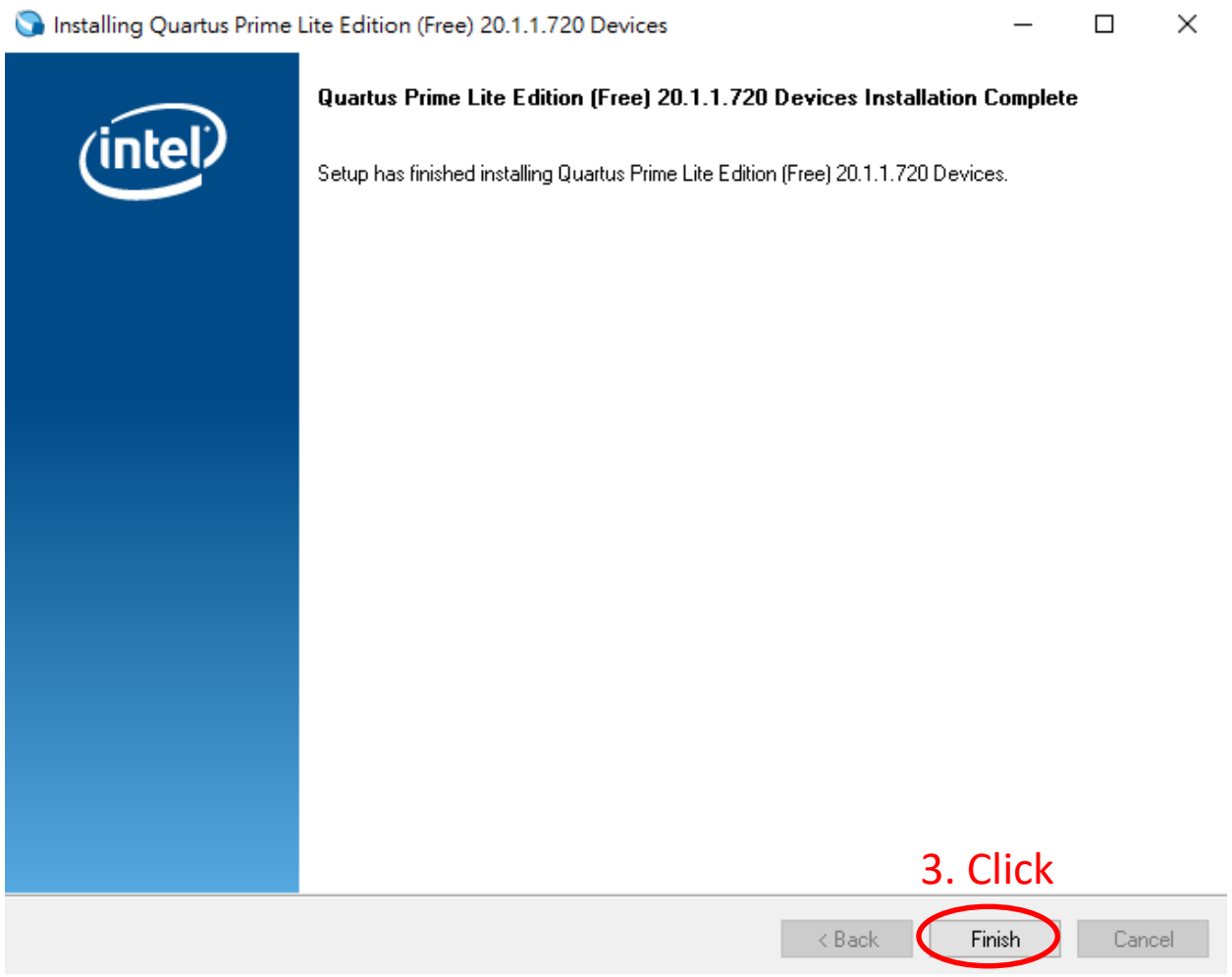


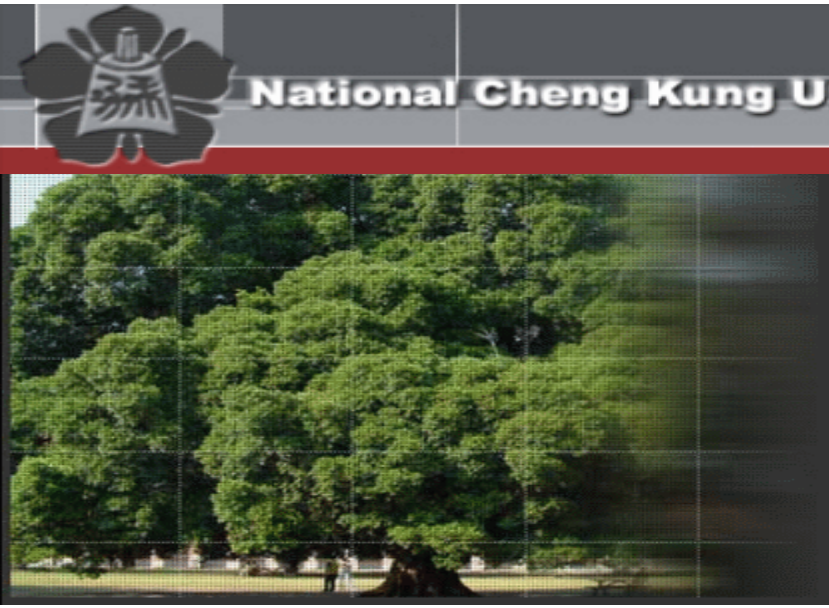


Download and install Quartus

- Step 7: Install Device







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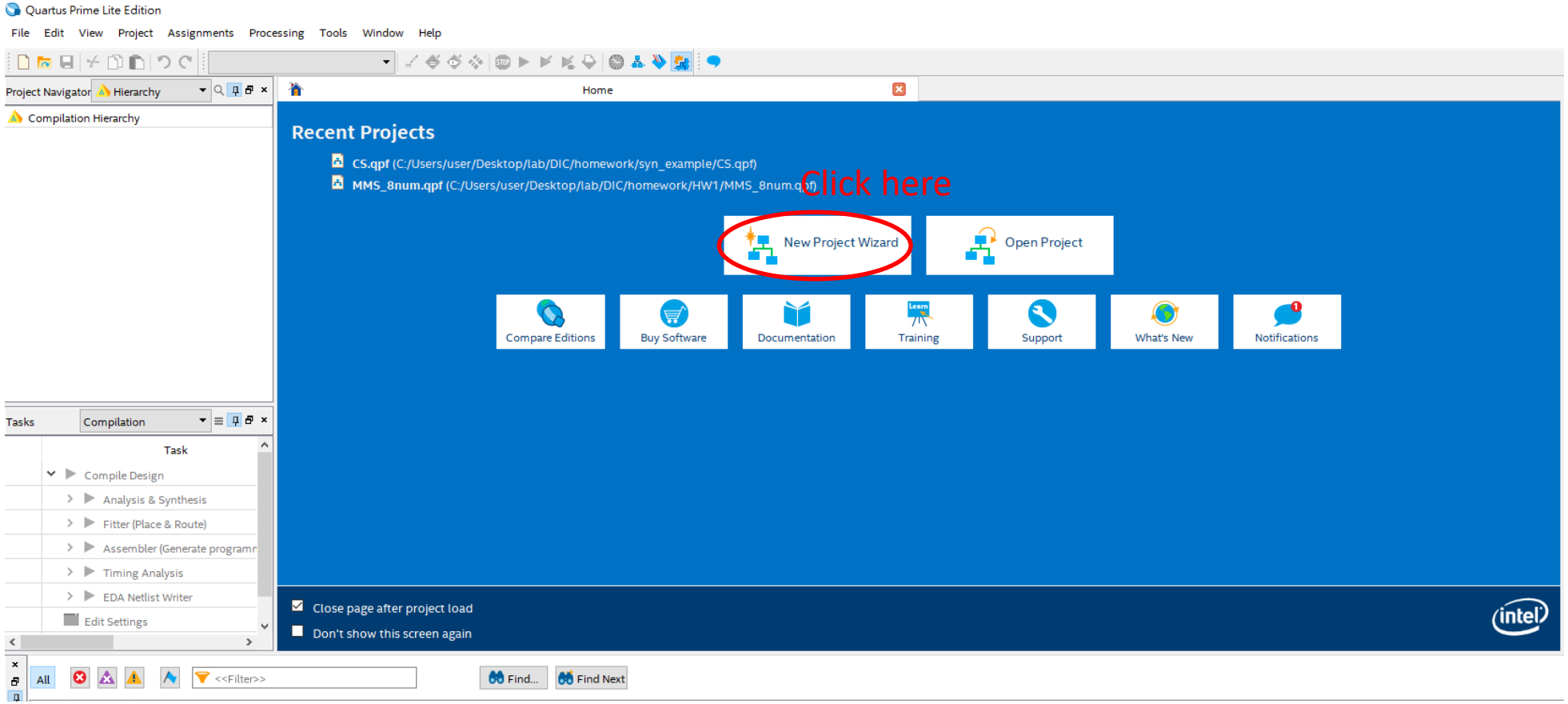
Synthesis by Quartus

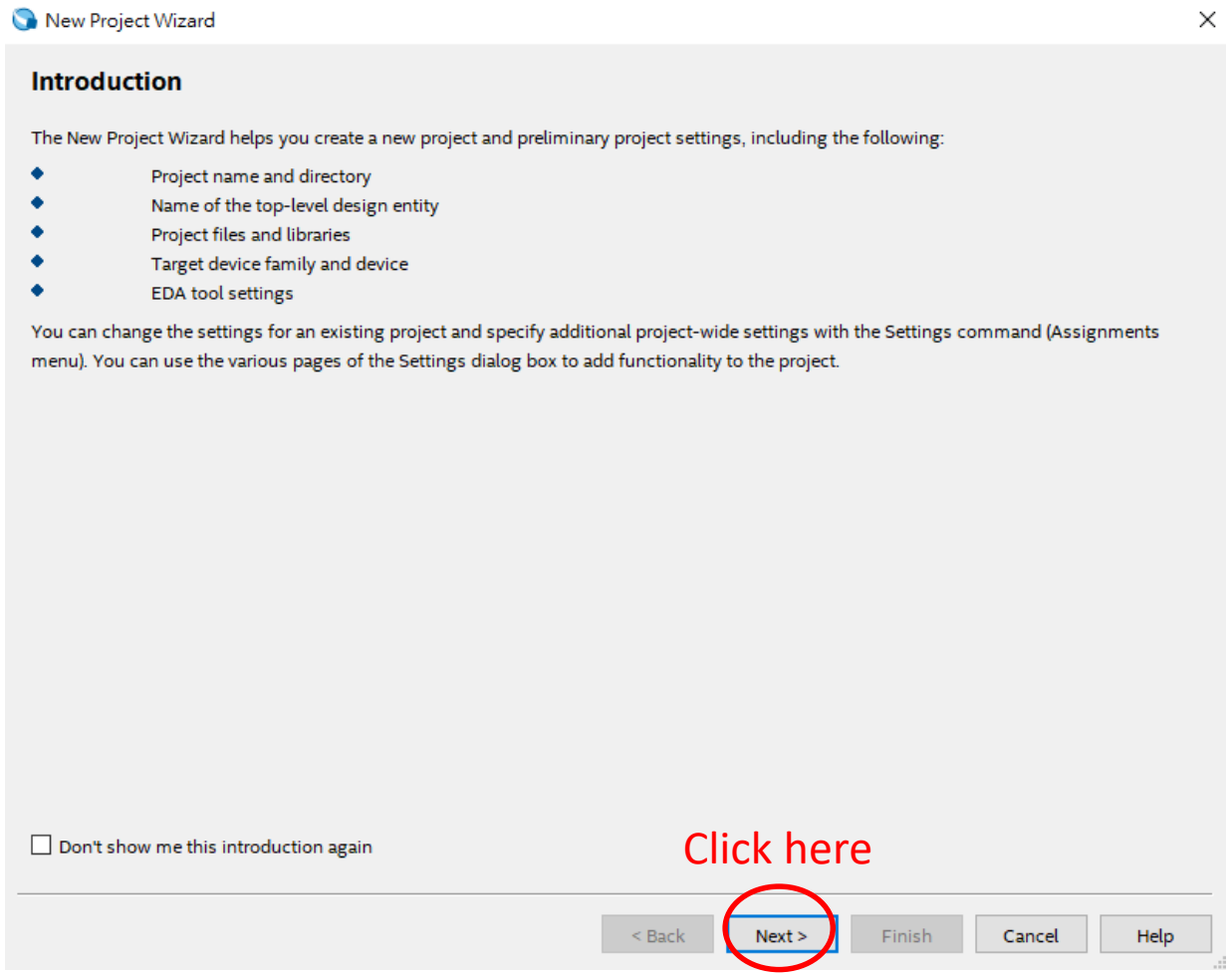
Synthesis by Quartus

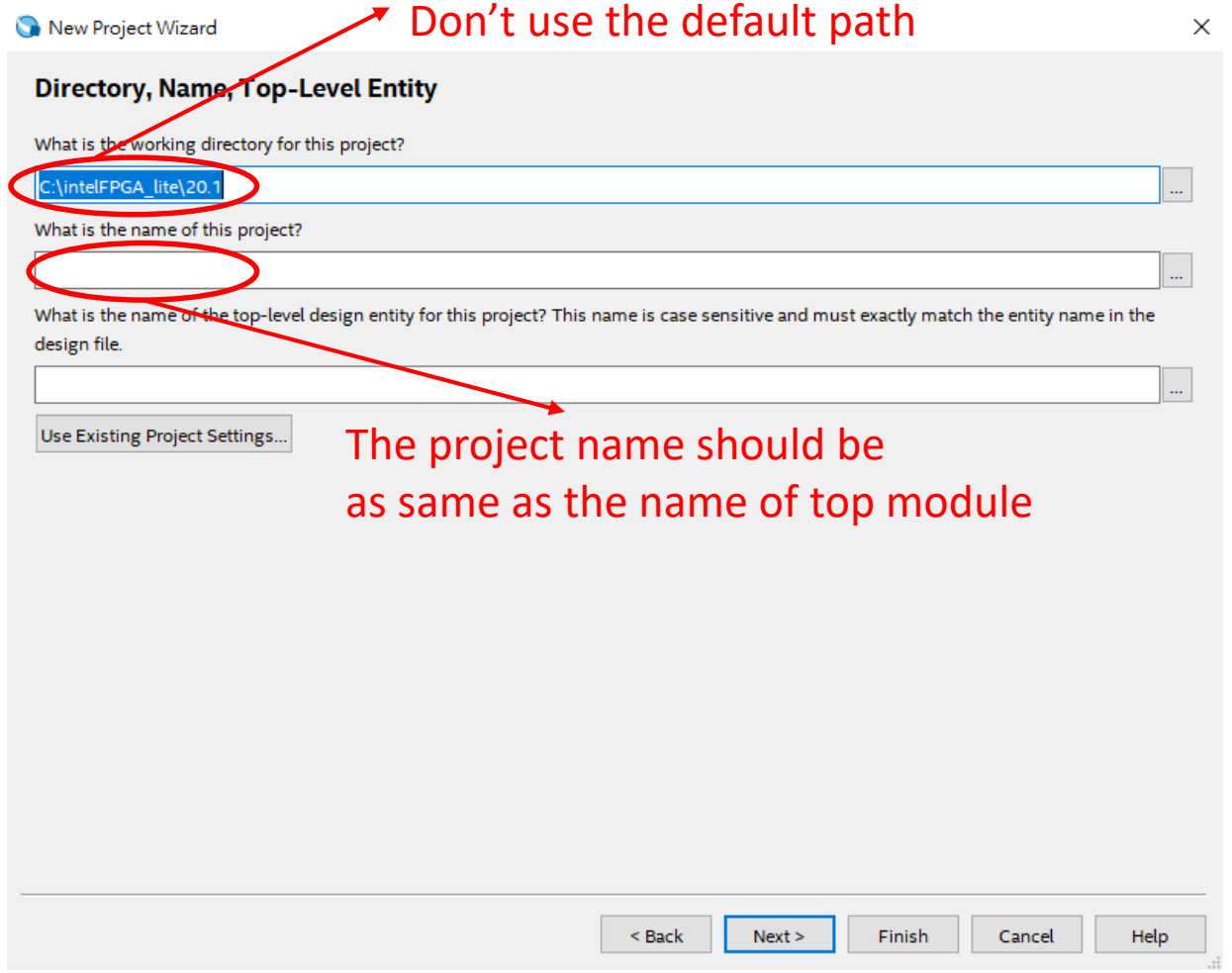
- Step1: Create a new project
  - File -> new project wizard



Synthesis by Quartus

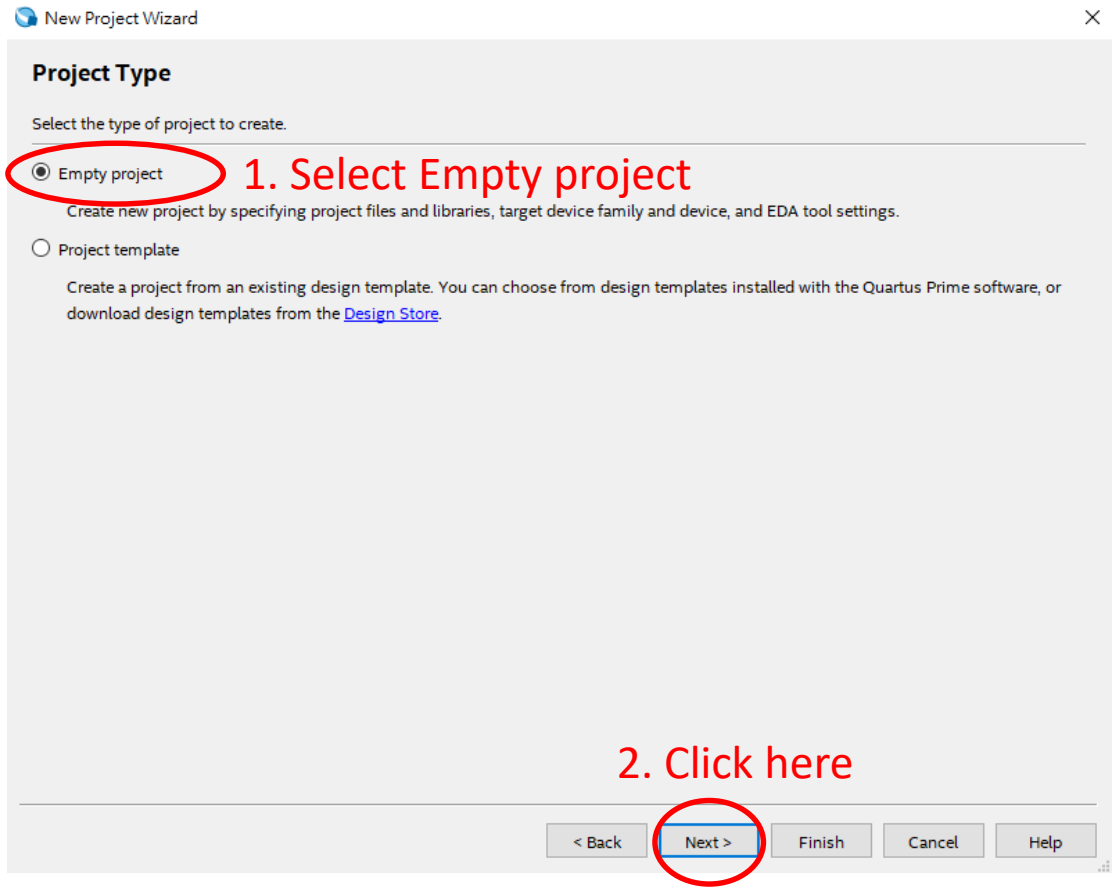
- Step1: Create a new project

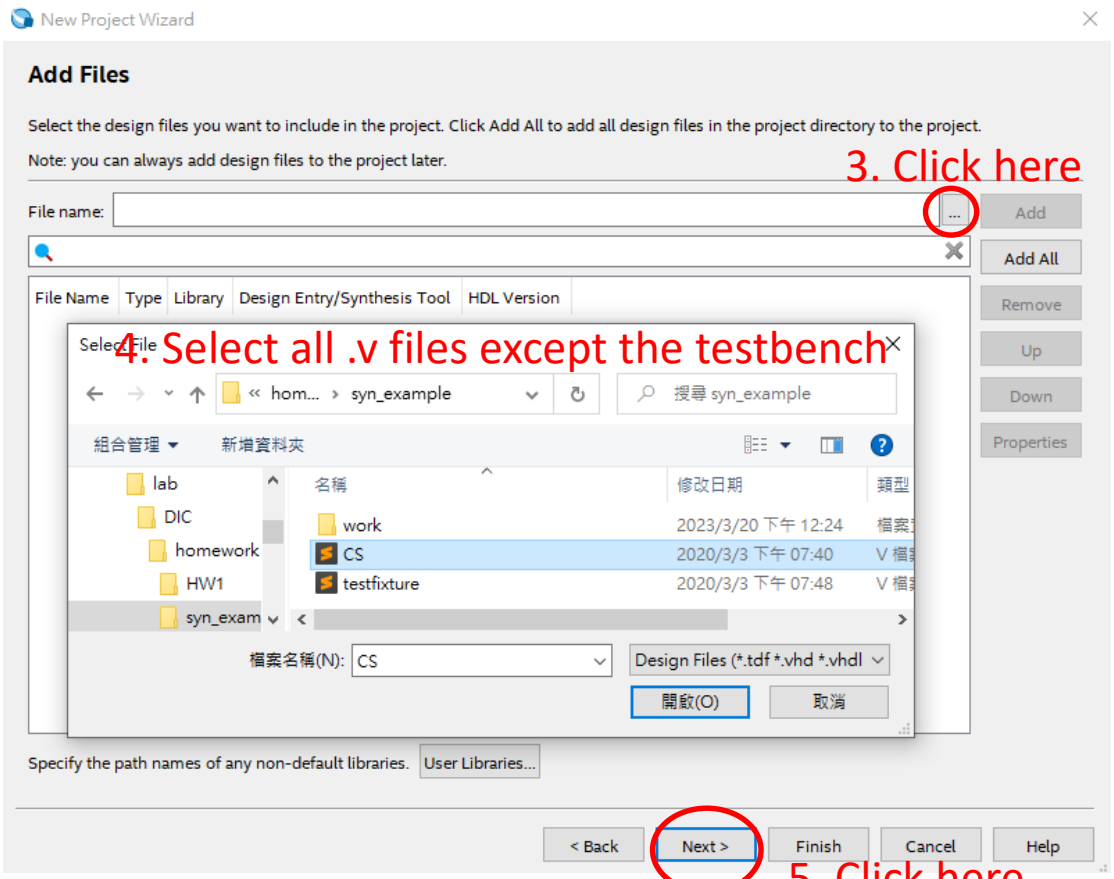




Synthesis by Quartus

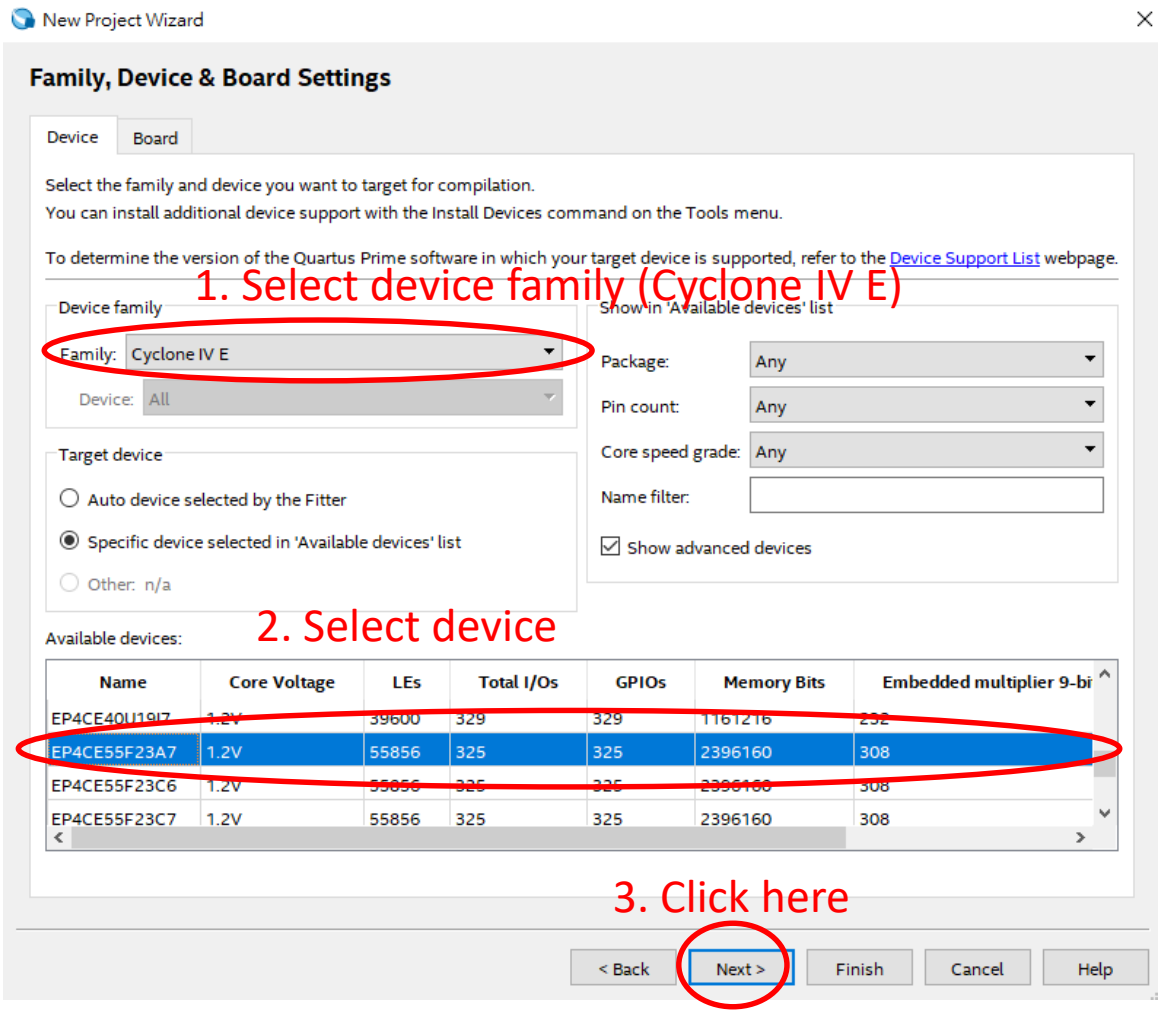
- Step1: Create a new project
  - Add the file excepting the testbench





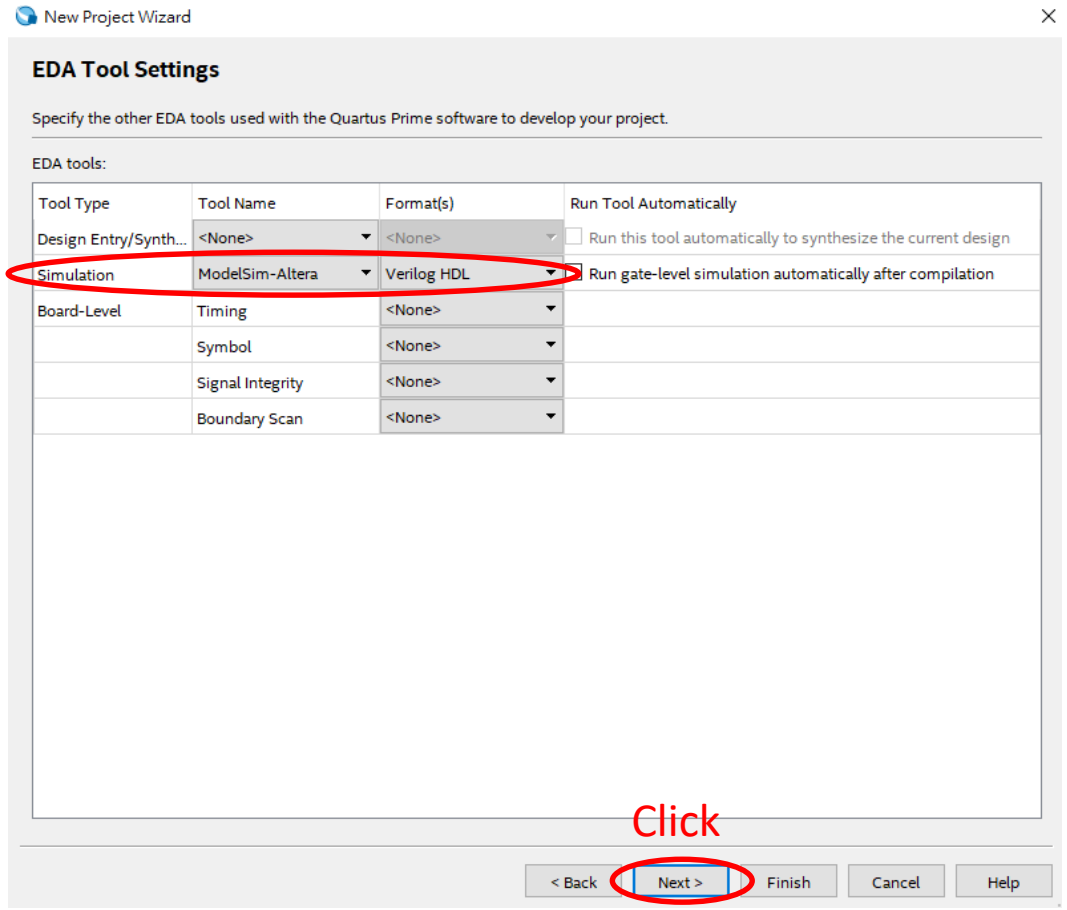
Synthesis by Quartus

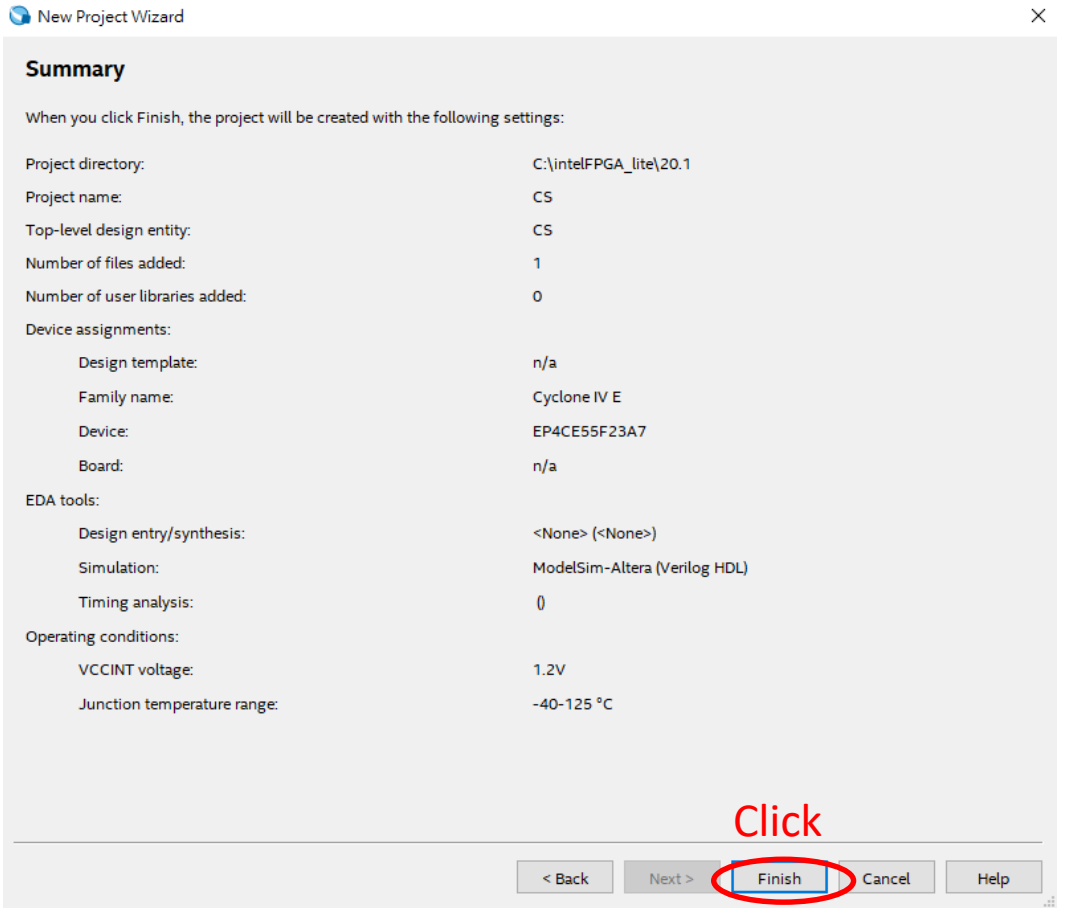
- Step2: Select the device : EP4CE55F23A7



Synthesis by Quartus

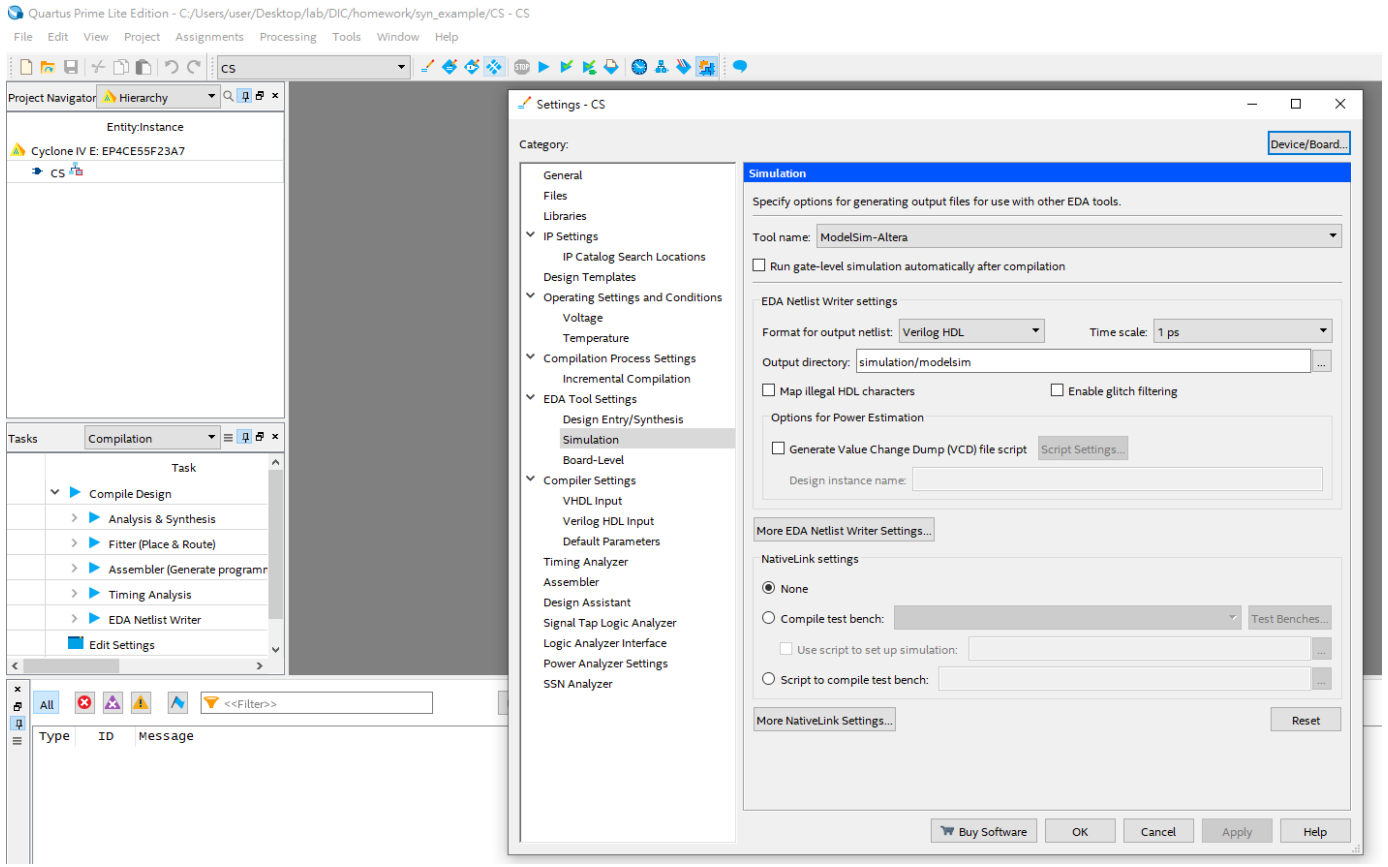
- Step 3 : Gate level simulation configuration
  - select ModelSim-Altera and Verilog HDL

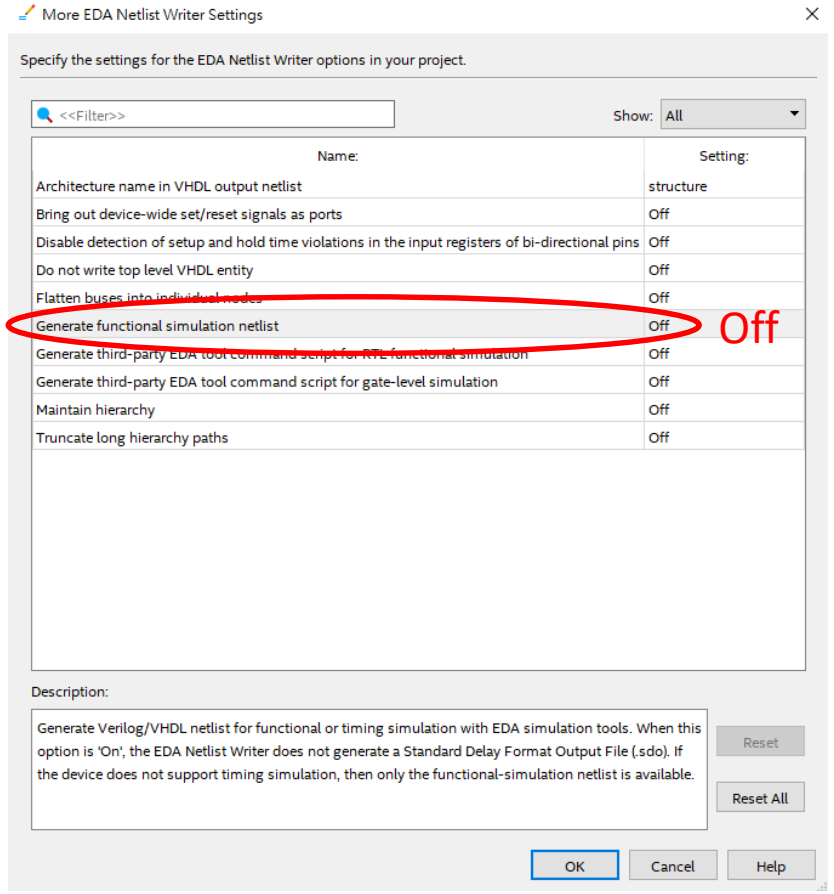




Synthesis by Quartus

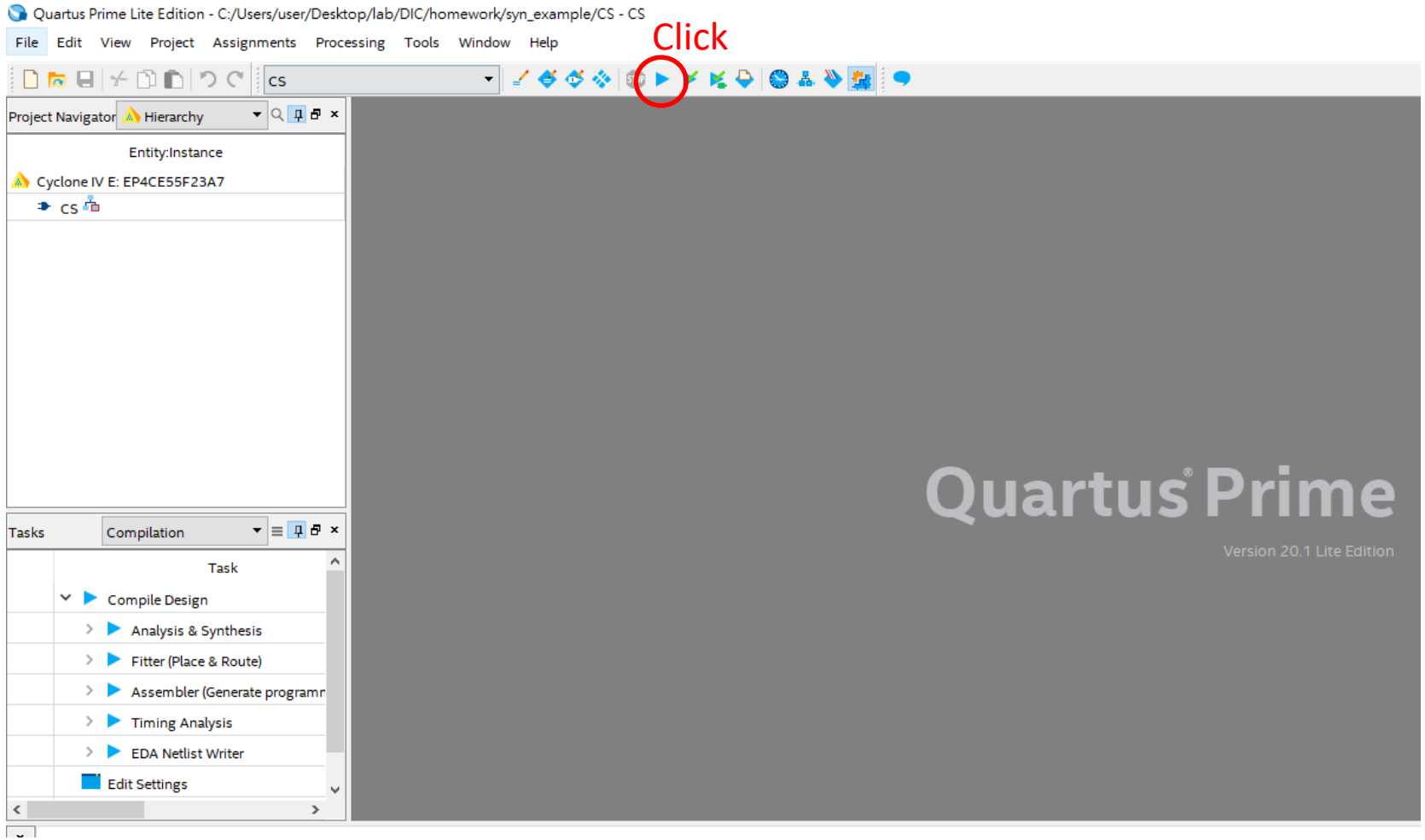
- Step 4 : compile
  - Assignment > Settings > Simulation > More EDA Writer Settings





Synthesis by Quartus

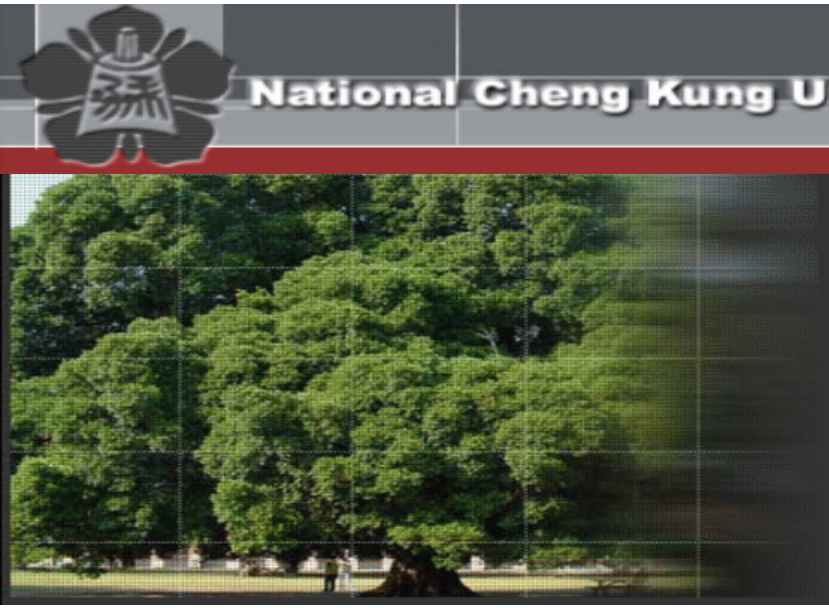
- Step 4 : compile



Flow Summary

<<Filter>>

Flow Status	Successful - Tue Mar 21 10:12:45 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	CS
Top-level Entity Name	CS
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	576 / 55,856 (1 %)
Total registers	88
Total pins	20 / 325 (6 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	0 / 308 (0 %)
Total PLLs	0 / 4 (0 %)



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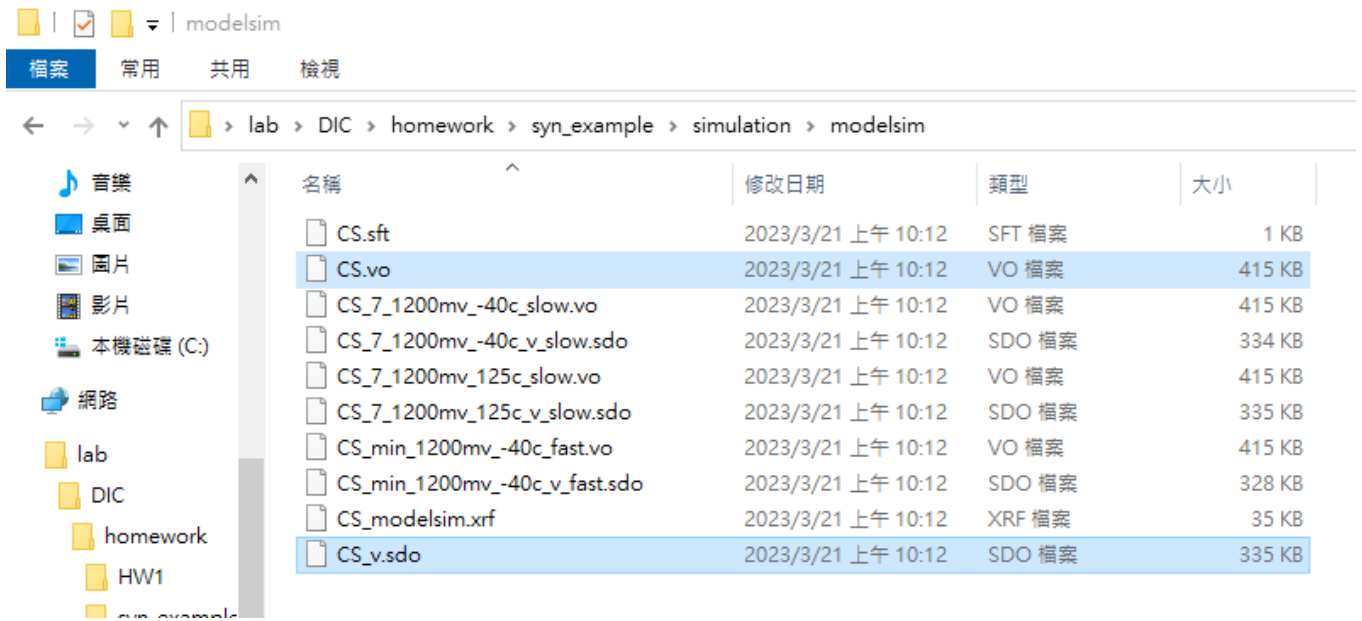
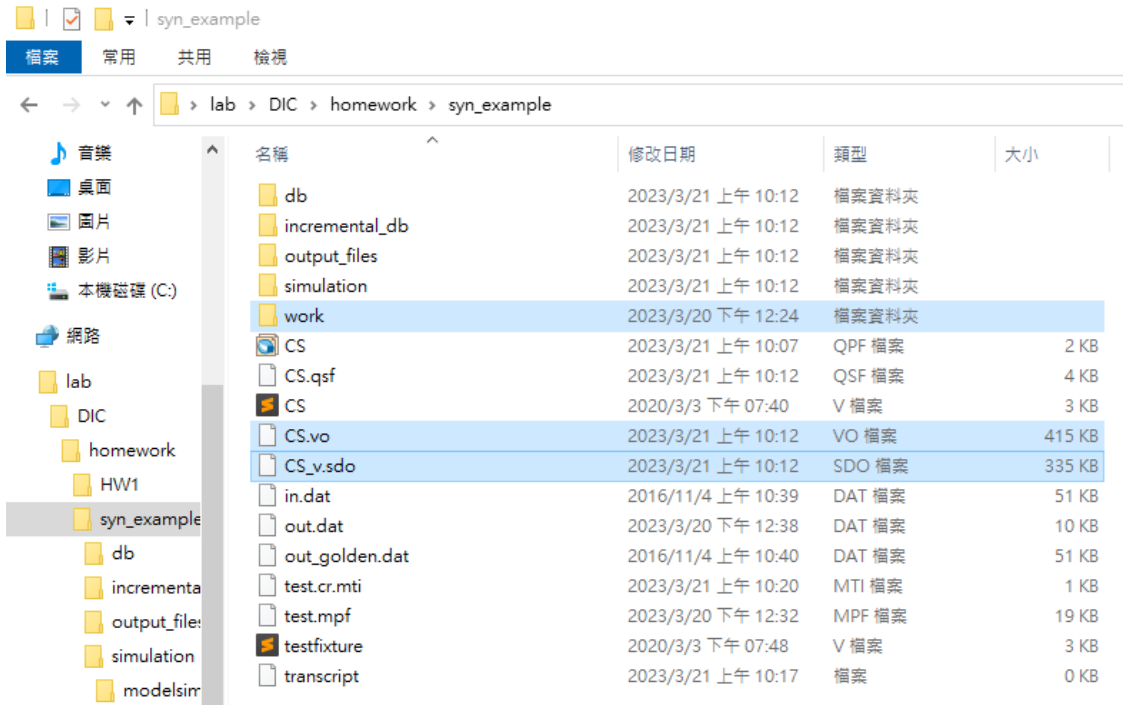
Gate-Level Simulation by ModelSim

Gate-Level Simulation by ModelSim

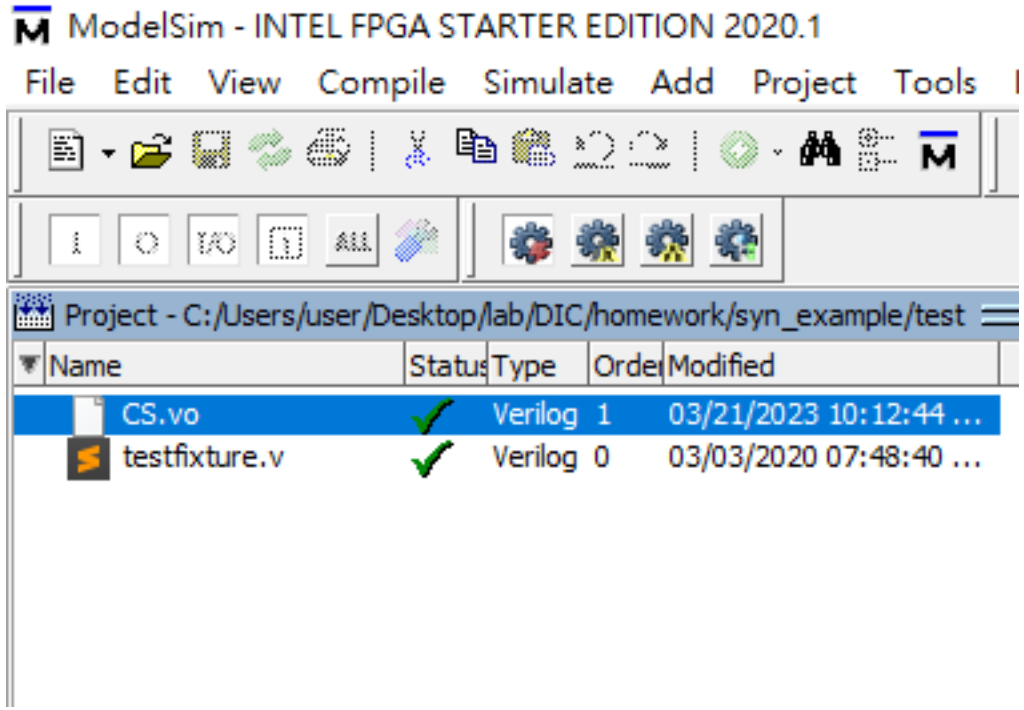
- Step 1 : the gate level file (*.vo,*.sdo) can be found in *simulation/modelsim* folder, and put them into modelsim project directory created in functional simulation section.
  - Simulation folder is in the Quartus project directory created in the synthesis section.

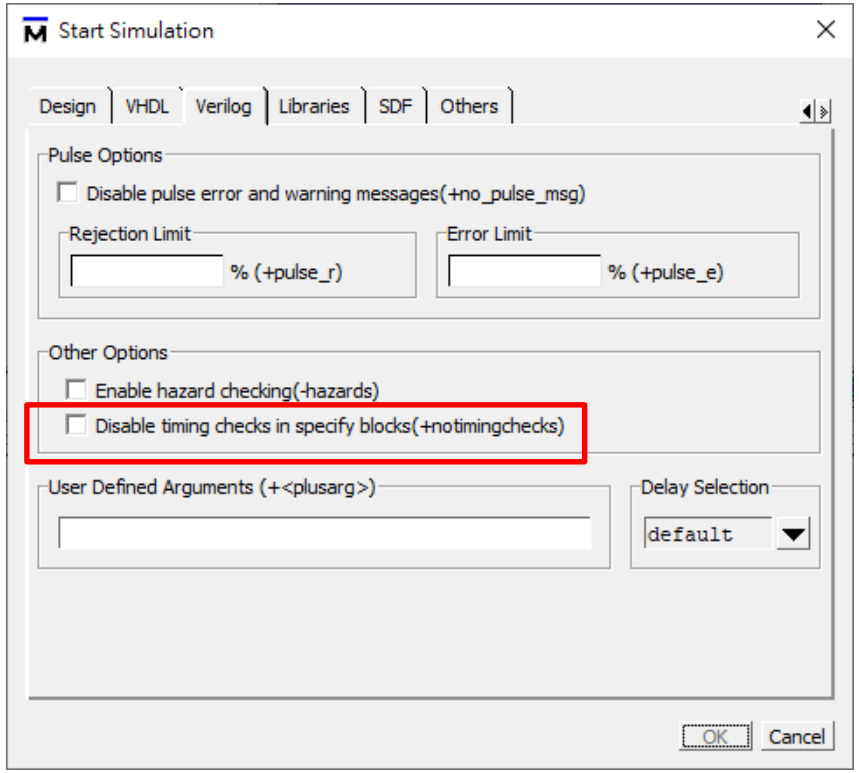




Gate-Level Simulation by ModelSim

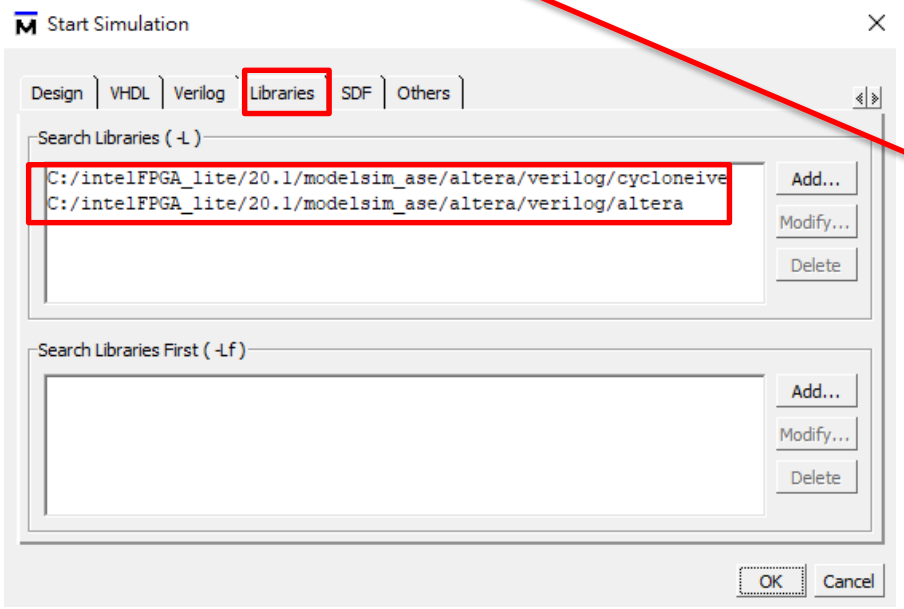
- Step 2 : gate level simulation
  - (Simulate -> Start Simulation Window)
  - This time, use the *.vo for simulation (Replace the original top_module.v with *.vo)
  - Repeat the steps of functional simulation. (Need to cancel the no timingchecks.)

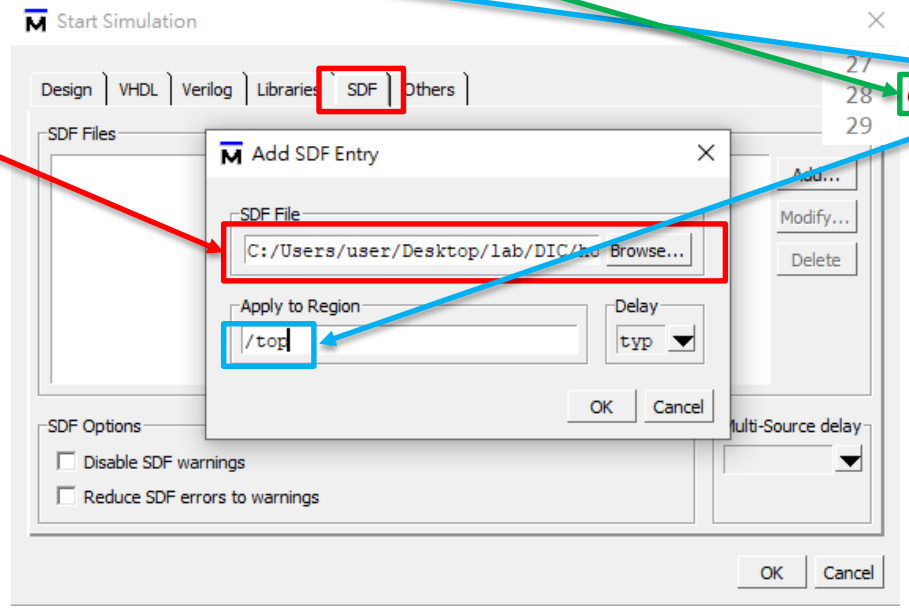




Gate-Level Simulation by ModelSim

- Step 2: Gate Level Simulation
  - Add cycloneive and altera library to search libraries (click Libraries to add)
    - your quartus installation disk/altera/13.0sp1/modelsim_ase/altera/Verilog/cycloneii
  - Add *.sdo to SDF Files and fill the instance name of your design in testbench.v in “apply to region” (click SDF to add)





Testbench file

```
27
28  CS top (.Y(Y), .X(X), .reset(reset), .clk(clk));
29
```