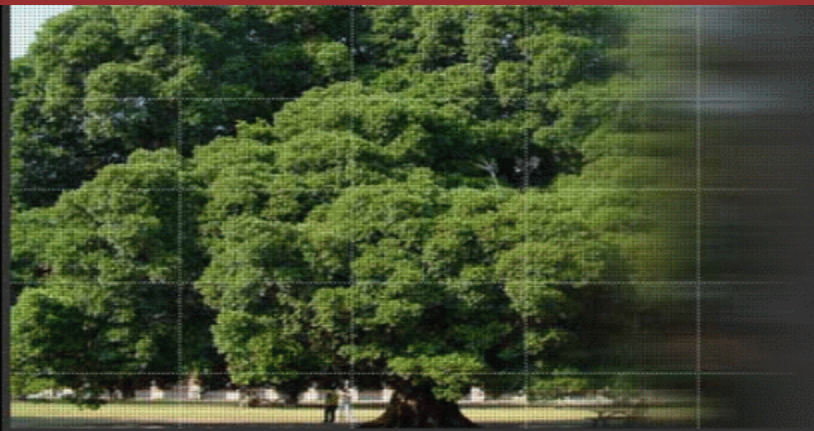




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# 數位IC設計 Tool安裝&作業模擬教學

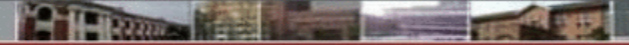
**NCKU CSIE DICLAB**

# The simulation process

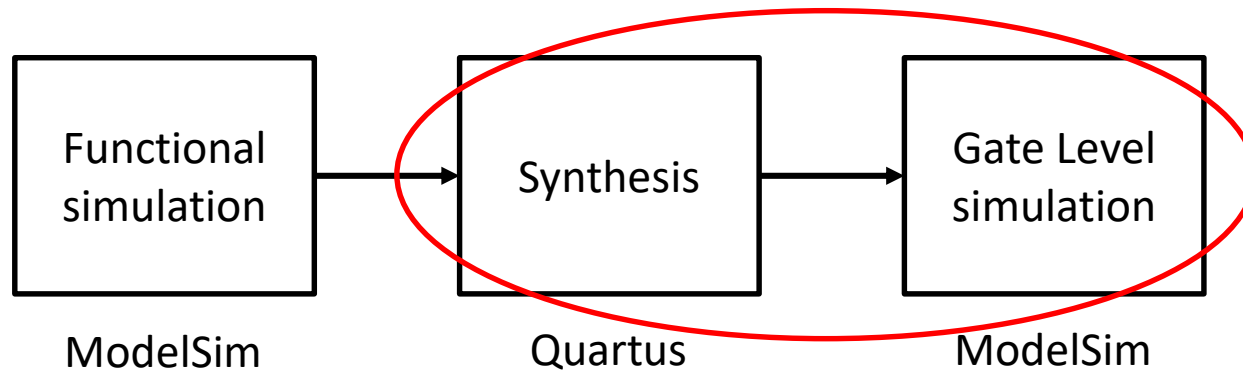


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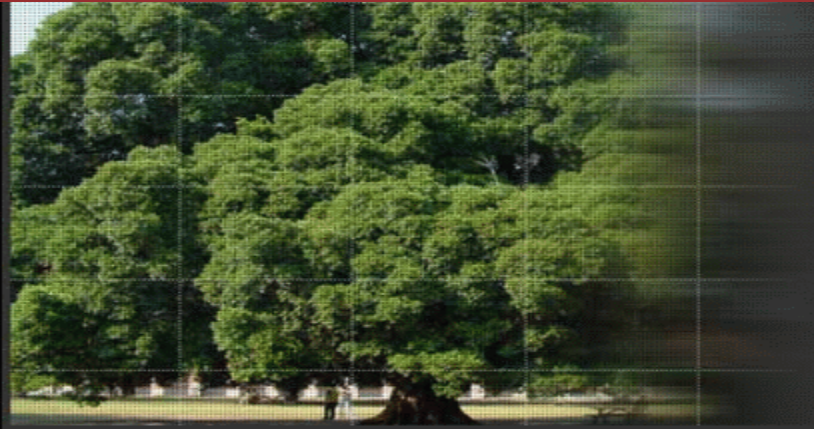
- ▶ The simulation process and the necessary tools in this class



- ▶ The tools can be downloaded from :
  - ▷ <https://www.intel.com/content/www/us/en/software/programmable/quartus-prime/download.html#>



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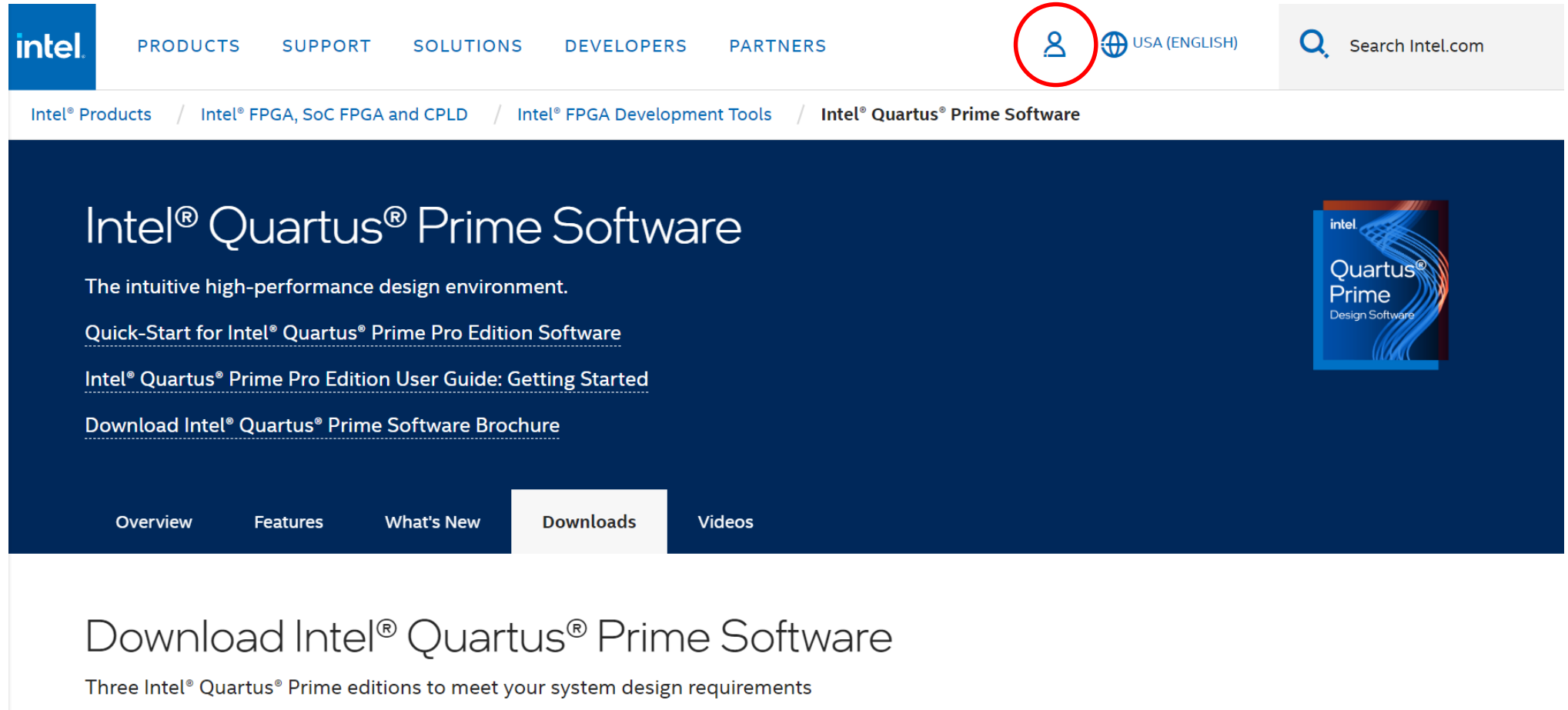


# Download and install Quartus

# Download and install Quartus

## ► Step 1: Register and sign in

Click here to create an account and sign in



The screenshot shows the Intel Quartus Prime Software website. The top navigation bar includes the Intel logo, links for PRODUCTS, SUPPORT, SOLUTIONS, DEVELOPERS, and PARTNERS, a user account icon (circled in red), a globe icon for USA (ENGLISH), and a search bar. Below the navigation bar is a breadcrumb trail: Intel® Products / Intel® FPGA, SoC FPGA and CPLD / Intel® FPGA Development Tools / Intel® Quartus® Prime Software. The main content area has a dark blue background with the text "Intel® Quartus® Prime Software" and "The intuitive high-performance design environment." It also features links for "Quick-Start for Intel® Quartus® Prime Pro Edition Software", "Intel® Quartus® Prime Pro Edition User Guide: Getting Started", and "Download Intel® Quartus® Prime Software Brochure". A sidebar on the right shows the Quartus Prime Design Software logo. At the bottom, there is a navigation bar with links for Overview, Features, What's New, Downloads (highlighted), and Videos. Below this, the text "Download Intel® Quartus® Prime Software" is displayed, followed by "Three Intel® Quartus® Prime editions to meet your system design requirements".

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Intel® Products / Intel® FPGA, SoC FPGA and CPLD / Intel® FPGA Development Tools / Intel® Quartus® Prime Software

## Intel® Quartus® Prime Software

The intuitive high-performance design environment.

[Quick-Start for Intel® Quartus® Prime Pro Edition Software](#)

[Intel® Quartus® Prime Pro Edition User Guide: Getting Started](#)

[Download Intel® Quartus® Prime Software Brochure](#)

Overview Features What's New Downloads Videos

## Download Intel® Quartus® Prime Software

Three Intel® Quartus® Prime editions to meet your system design requirements



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# Download and install Quartus

- Step 2: Click “Download for Windows(free, no license required)”

[Overview](#) [Features](#) [What's New](#) [Downloads](#) [Videos](#)

## Download Intel® Quartus® Prime Software

Three Intel® Quartus® Prime editions to meet your system design requirements

### Pro Edition

The Intel® Quartus® Prime Pro Edition Software supports the advanced features in Intel's next-generation FPGAs and SoCs with the Intel® Agilex™, Intel® Stratix® 10, Intel® Arria® 10, and Intel® Cyclone® 10 GX device families.

Cyclone 10 GX devices supported for free in Intel Quartus Prime Pro Software Edition.

Download for Windows (paid license required)

Download for Linux (paid license required)

### Standard Edition

The Intel® Quartus® Prime Standard Edition software includes extensive support for earlier device families in addition to the Intel® Cyclone® 10 LP device family.

Download for Windows (paid license required)

Download for Linux (paid license required)

### Lite Edition

The Intel® Quartus® Prime Lite Edition software supports Intel's low-cost FPGA device families.

Refer to [Features](#) to review all devices supported by the Free Quartus Prime Software Lite Edition.

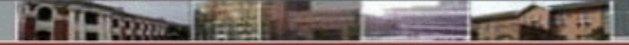
Download for Windows (free, no license required)

Download for Linux (free, no license required)

Click Here



# Download and install Quartus



## ► Step 3: Select software version (20.1.1)

Intel® Quartus® Prime Lite Edition Design Software Version 20.1.1 for Windows

ID	Date	Version	Select version 20.1.1
660907	11/22/2020	20.1.1	▼

A newer version of this software is available, which includes functional and security updates. Customers should [click here](#) to update to the latest version.

Users should upgrade to the latest version of the Intel® Quartus® Prime Design Software. The selected version does not include the latest functional and security updates. If you must use this version of software, follow the [technical recommendations](#) to help improve security. For critical support requests, please contact our [support team](#).



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# Download and install Quartus

## ► Step 4: Download Quartus setup execution file

Downloads

1. Click the 'Individual Files' tab

Multiple Download

Individual Files

Additional Software

Copyright Licensed Source

Intel® Quartus® Software

ModelSim-Intel® FPGA Edition (includes Starter Edition)

Download

ModelSimSetup-20.1.1.720-windows.exe

Size: 1.2 GB

SHA1: d484e4c7882fca584a9b0243cbbd74953a4aeb25

Intel® Quartus® Prime (includes Nios® II EDS)

2. Download Quartus

Download

QuartusLiteSetup-20.1.1.720-windows.exe

Size: 1.6 GB

SHA1: 5edd76cfa2a6a40077bc3eeed5bdc95cacdc8

\*\* Nios® II EDS on Windows requires Ubuntu 18.04 LTS on Windows Subsystem for Linux (WSL), which requires a manual installation.

\*\* Nios® II EDS requires you to install an Eclipse IDE manually.



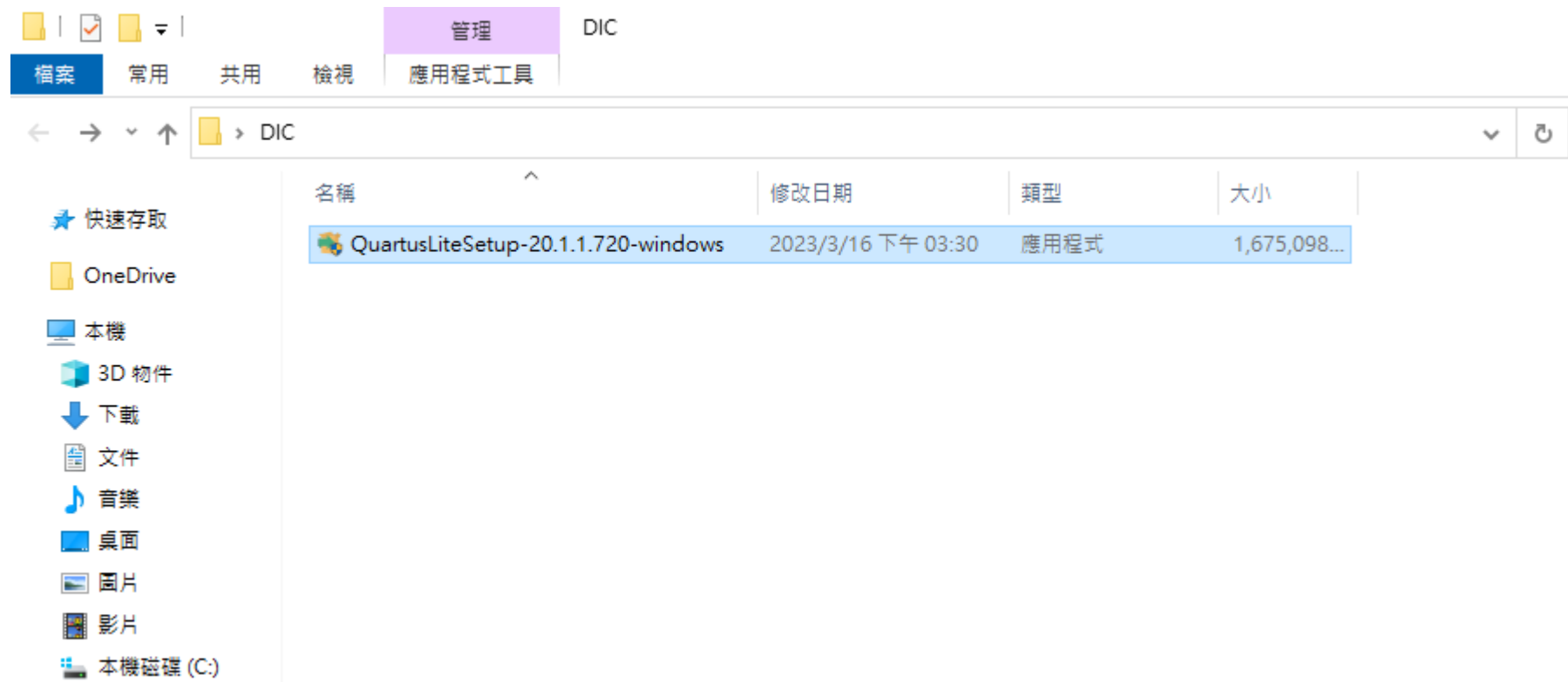
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# Download and install Quartus

## ► Step 5: Installation





# Download and install Quartus

## ► Step 5: Installation

Installing Quartus Prime Lite Edition (Free) 20.1.1.720

### License Agreement



You can view the full license agreement at the link below or use --install\_lic option from command-line to get the license agreement files before the installation. You must accept the terms of the agreement before continuing with the installation.

<http://fpgasoftware.intel.com/eula/>

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Do you accept this license?  
☒ I accept the agreement  
☐ I do not accept the agreement

1. Accept the agreement

2. Click

< Back

Next >

Cancel

Installing Quartus Prime Lite Edition (Free) 20.1.1.720

### Installation directory



Specify the directory where Quartus Prime Lite Edition (Free) 20.1.1.720 will be installed

Installation directory C:\intelFPGA\_lite\20.1

3. Set installation path

4. Click

< Back

Next >

Cancel



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# Download and install Quartus

## ► Step 5: Installation

Installing Quartus Prime Lite Edition (Free) 20.1.1.720



Select Components



Select the components you want to install

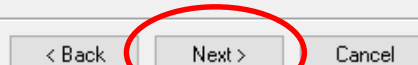
- ☒ Quartus Prime Lite Edition (Free)
- ☒ Quartus Prime (includes Nios II EDS) (8864MB)

1. Select Quartus Prime Lite Edition (Free)

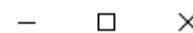
You can add additional device support to an existing Quartus Prime software installation without having to reinstall the entire software package. Use the Install Devices command on the Tools menu in the Quartus Prime software to get started.

Select a component for more information

2. Click



Installing Quartus Prime Lite Edition (Free) 20.1.1.720



Ready to Install

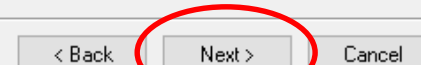


Summary:

Installation directory: C:\intelFPGA\_lite\20.1  
Required disk space: 8867 MB  
Available disk space: 361539 MB

3. Check available disk space

4. Click





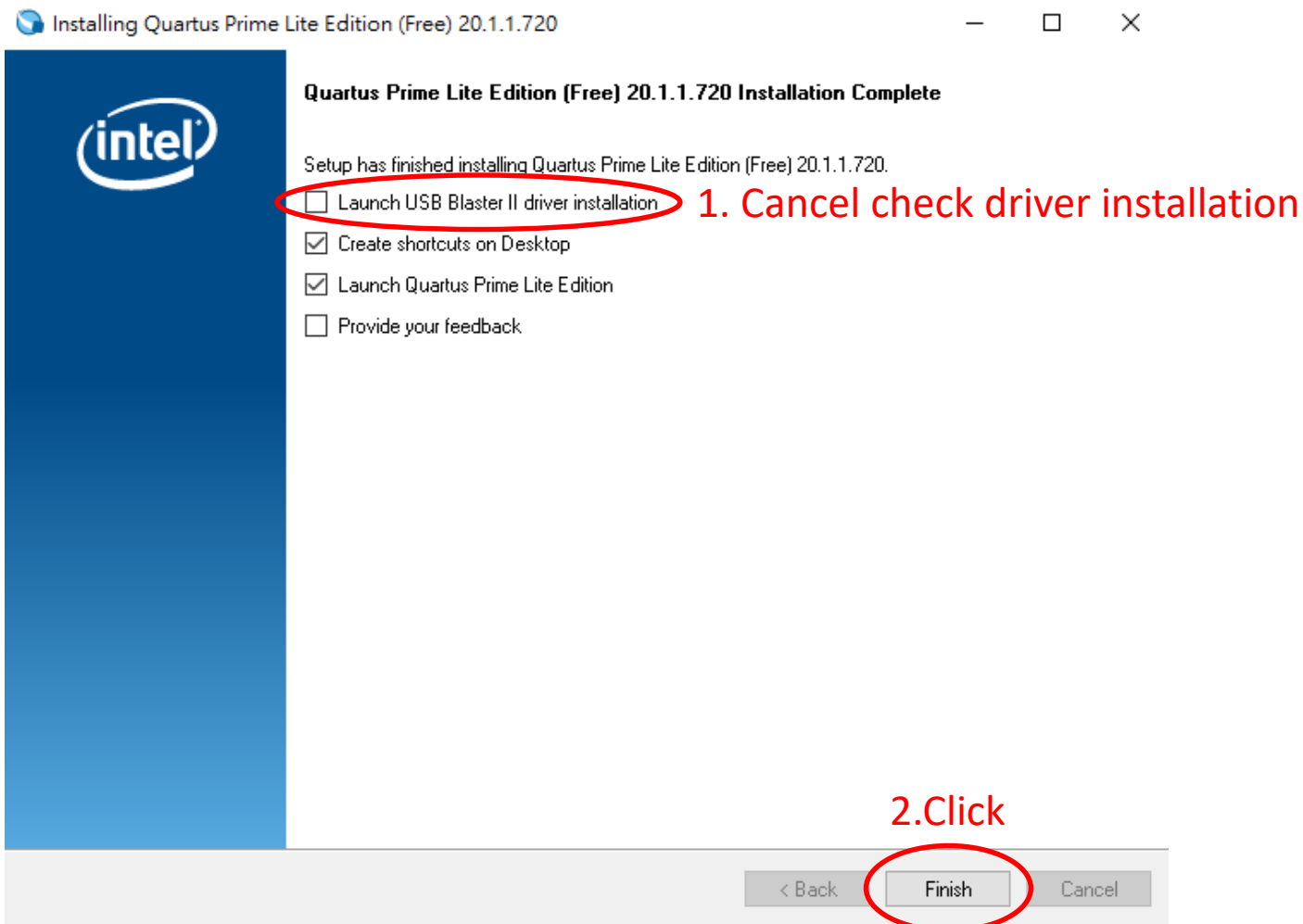
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# Download and install Quartus

## ► Step 5: Installation





# Download and install Quartus

## ► Step 6: Download device support file

### Devices

#### Intel® Arria® II Device Support

Download  
arria\_lite-20.1.1.720.qdz

Size: 499.1 MB

SHA1: e0508f997e1f395e247a6490f1710e36a1f528d1



#### Intel® Cyclone® IV Device Support

Download Cyclone IV Device Support

Download  
cyclone-20.1.1.720.qdz

Size: 466 MB

SHA1: 5447aa416749edf5bae5f68dcc734c43e8db6a67



#### Intel® Cyclone® 10 LP Device Support

Download  
cyclone10lp-20.1.1.720.qdz

Size: 265.7 MB

SHA1: 93ab293a69b1760847f26b996d043e20bd465f26



# Download and install Quartus



## ► Step 7: Install Device

▷ Windows搜尋 > Device Installer

Installing Quartus Prime Lite Edition (Free) 20.1.1.720 Devices

### Download Directory

Specify the directory that contains the Quartus Prime device files (.qdz).

Download directory: C:\Users\user\Downloads

1. Select path of device support file

If you need to download device support files, you can download them from the Download Center page of the Intel FPGA website:

<http://fpgasoftware.intel.com/?edition=lite/#tabs-2>

InstallBuilder

< Back

Next >

Cancel



Installing Quartus Prime Lite Edition (Free) 20.1.1.720 Devices

### Select Components

Select the components you want to install

- ☒ Quartus Prime Lite Edition (Free)
- ☒ Devices
  - ☒ Cyclone IV (516.3MB)
  - ☐ Cyclone 10 LP (293.5MB)
  - ☐ Cyclone V (1434.3MB)
- ☐ ModelSim - Intel FPGA Starter Edition (Free) (4318.8MB)
- ☐ ModelSim - Intel FPGA Edition (4318.8MB)

Installs Cyclone IV device support. (516.3MB)

3. Check Devices & Cyclone IV

InstallBuilder

< Back

Next >

Cancel

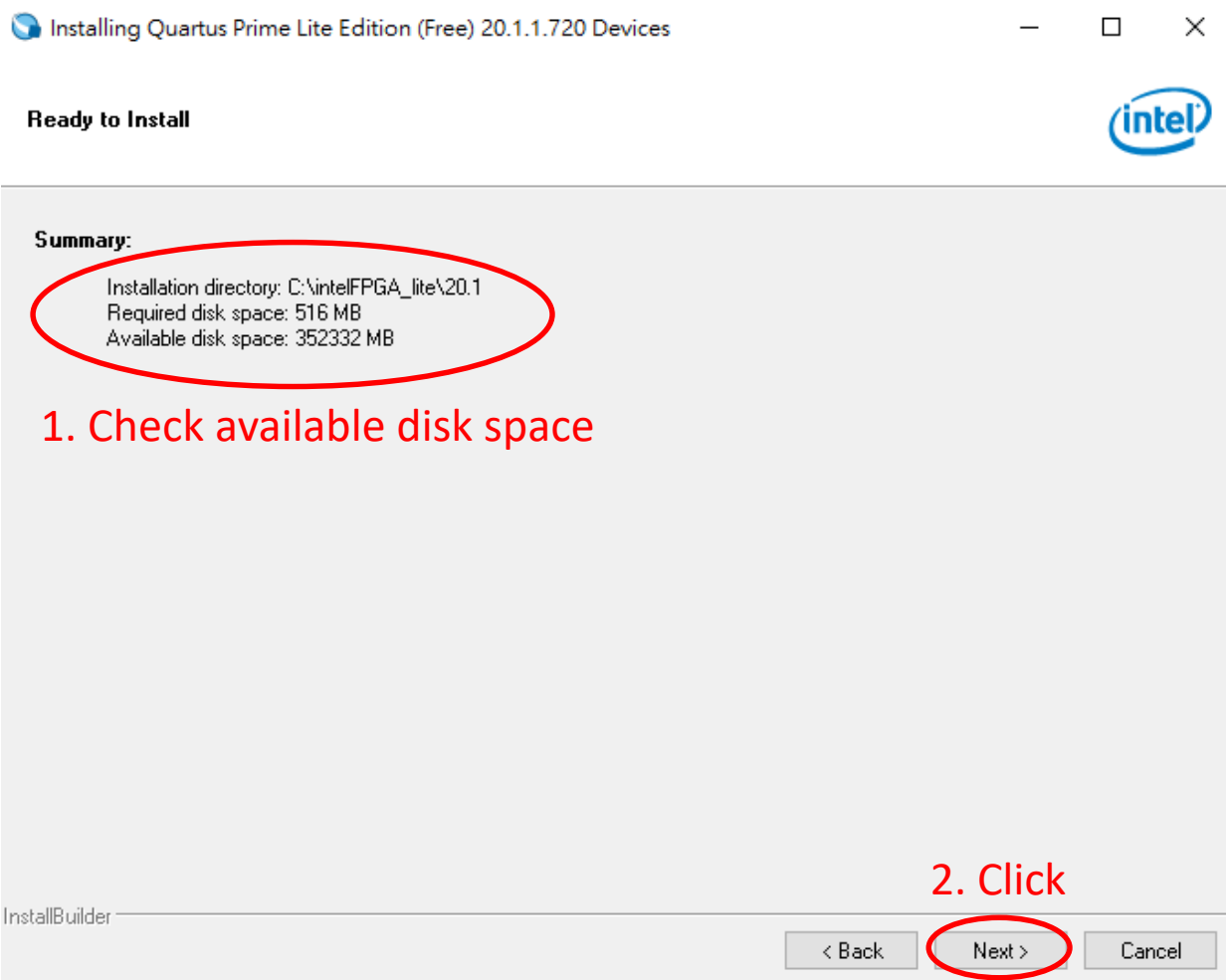


4. Click

# Download and install Quartus



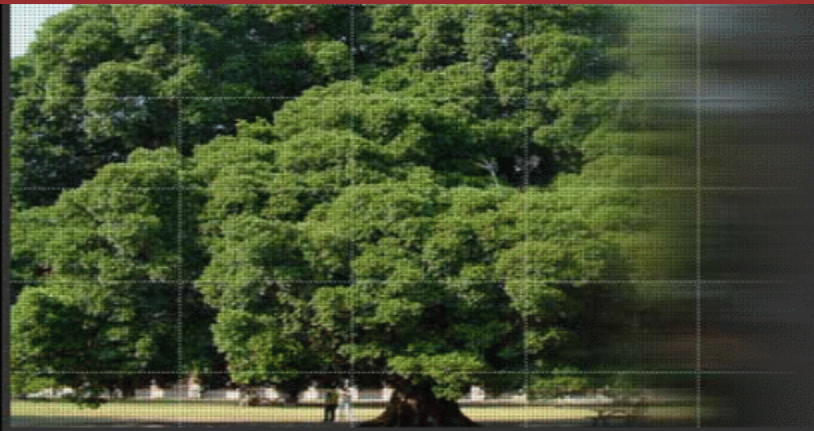
## ► Step 7: Install Device





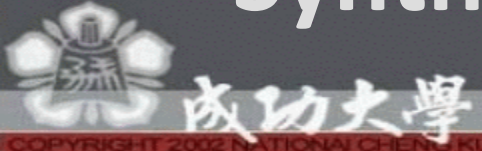


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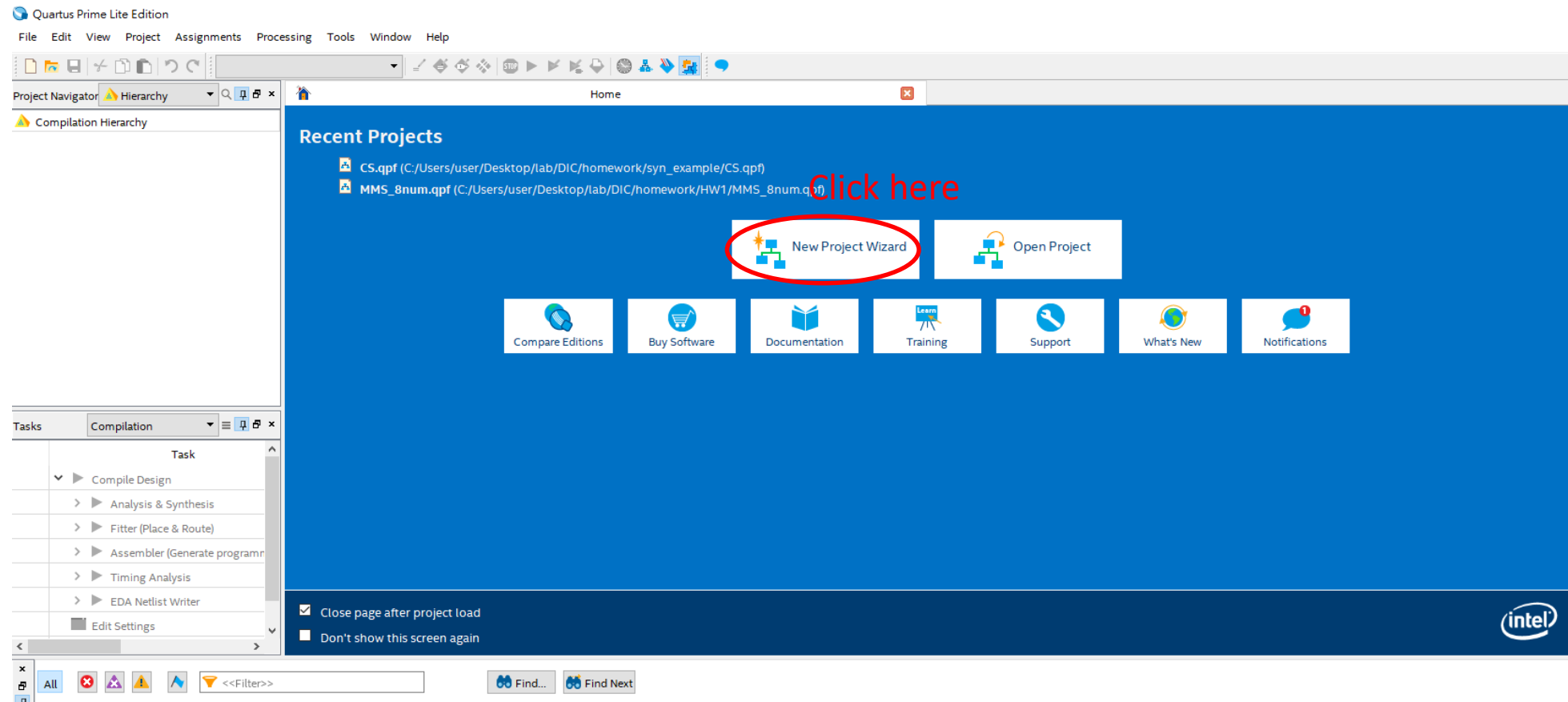


# Synthesis by Quartus

# Synthesis by Quartus



- ▶ Step1: Create a new project
  - ▷ File -> new project wizard





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# Synthesis by Quartus

## ► Step1: Create a new project

New Project Wizard

### Introduction

The New Project Wizard helps you create a new project and preliminary project settings, including the following:

- ◆ Project name and directory
- ◆ Name of the top-level design entity
- ◆ Project files and libraries
- ◆ Target device family and device
- ◆ EDA tool settings

You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.

☐ Don't show me this introduction again

Click here

< Back

Next >

Finish

Cancel

Help

X

New Project Wizard

### Directory, Name, Top-Level Entity

What is the working directory for this project?

C:\intelFPGA\_lite\20.1

What is the name of this project?

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

Use Existing Project Settings...

Modify the project path  
Don't use the default path

The project name should be  
as same as the name of top module

< Back

Next >

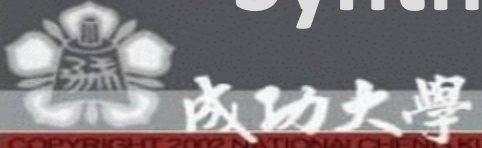
Finish

Cancel

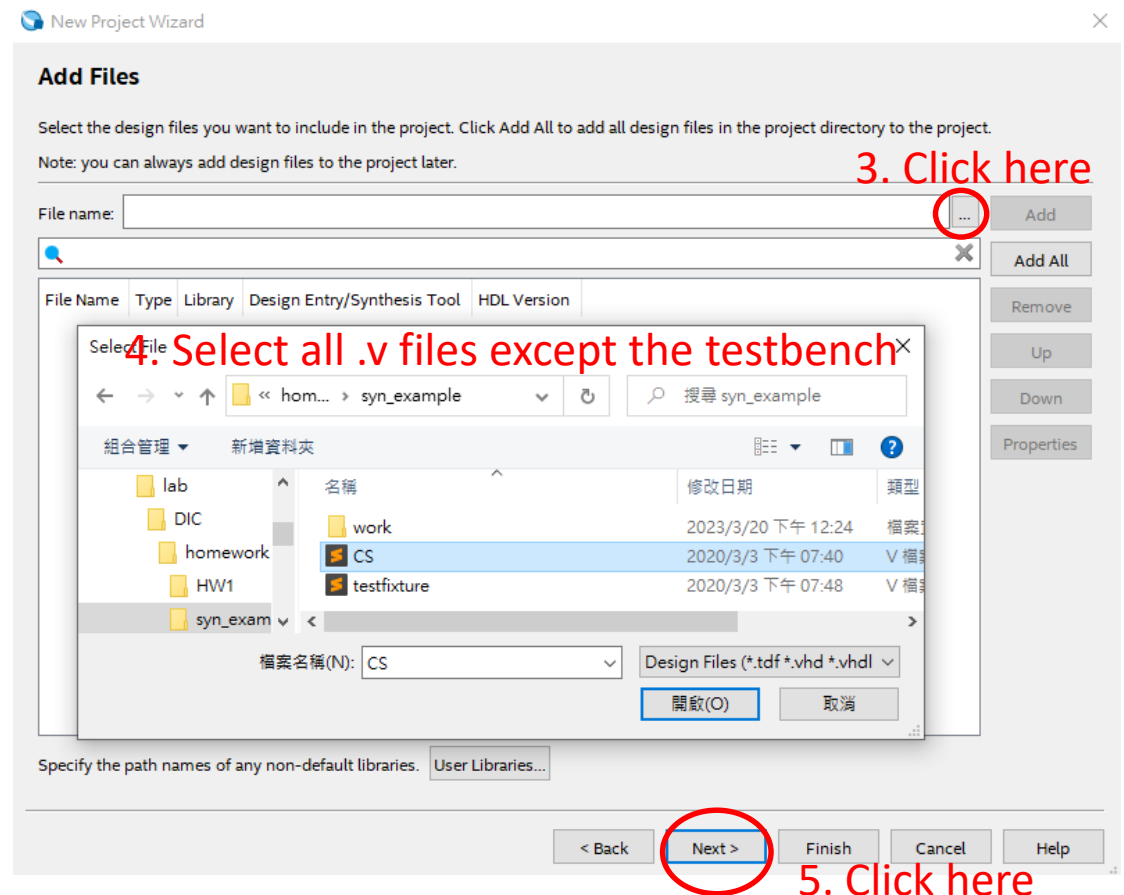
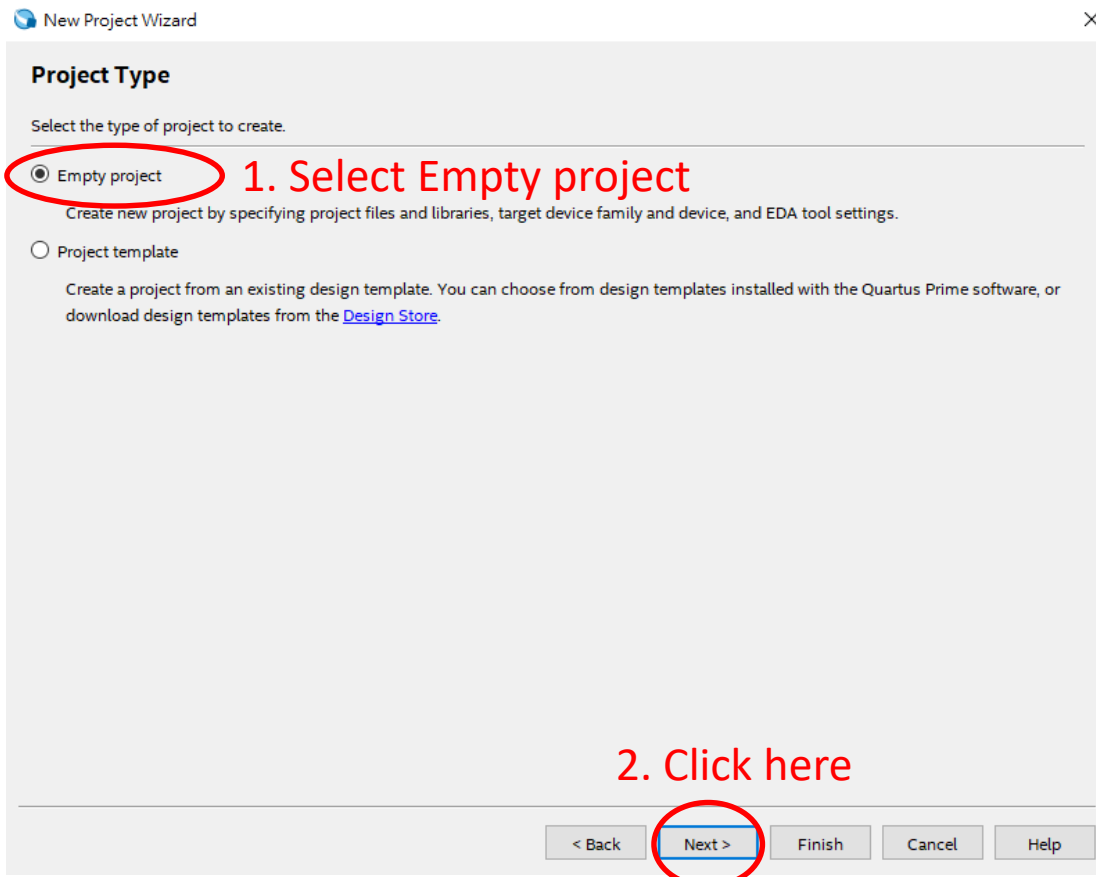
Help

X

# Synthesis by Quartus



- Step1: Create a new project
  - ▷ Add the file excepting the testbench





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# Synthesis by Quartus

- Step2: Select the device : **EP4CE55F23A7**

New Project Wizard

### Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

1. Select device family (Cyclone IV E)

Device family: Family: Cyclone IV E Device: All

Package: Any Pin count: Any Core speed grade: Any Name filter: Show advanced devices ☒

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

2. Select device

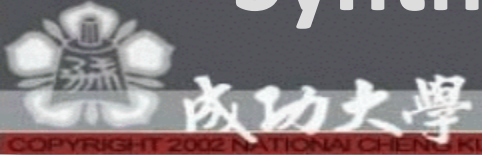
Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9-bit
EP4CE40U19I7	1.2V	39600	329	329	1161216	202
EP4CE55F23A7	1.2V	55856	325	325	2396160	308
EP4CE55F23C6	1.2V	55856	325	325	2396160	308
EP4CE55F23C7	1.2V	55856	325	325	2396160	308

3. Click here

< Back Next > Finish Cancel Help

# Synthesis by Quartus



## ► Step 3 : Gate level simulation configuration

### ▷ select ModelSim-Altera and Verilog HDL

New Project Wizard

### EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synth...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	Verilog HDL	<input checked="" type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

Click

< Back Next > Finish Cancel Help

New Project Wizard

### Summary

When you click Finish, the project will be created with the following settings:

Project directory: C:\intelFPGA\_lite\20.1

Project name: CS

Top-level design entity: CS

Number of files added: 1

Number of user libraries added: 0

Device assignments:

- Design template: n/a
- Family name: Cyclone IV E
- Device: EP4CE55F23A7
- Board: n/a

EDA tools:

- Design entry/synthesis: <None> (<None>)
- Simulation: ModelSim-Altera (Verilog HDL)
- Timing analysis: 0

Operating conditions:

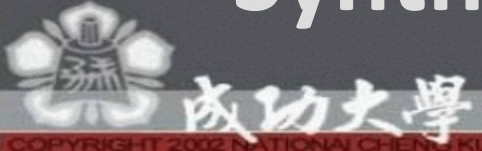
- VCCINT voltage: 1.2V
- Junction temperature range: -40-125 °C

Click

< Back Next > Finish Cancel Help

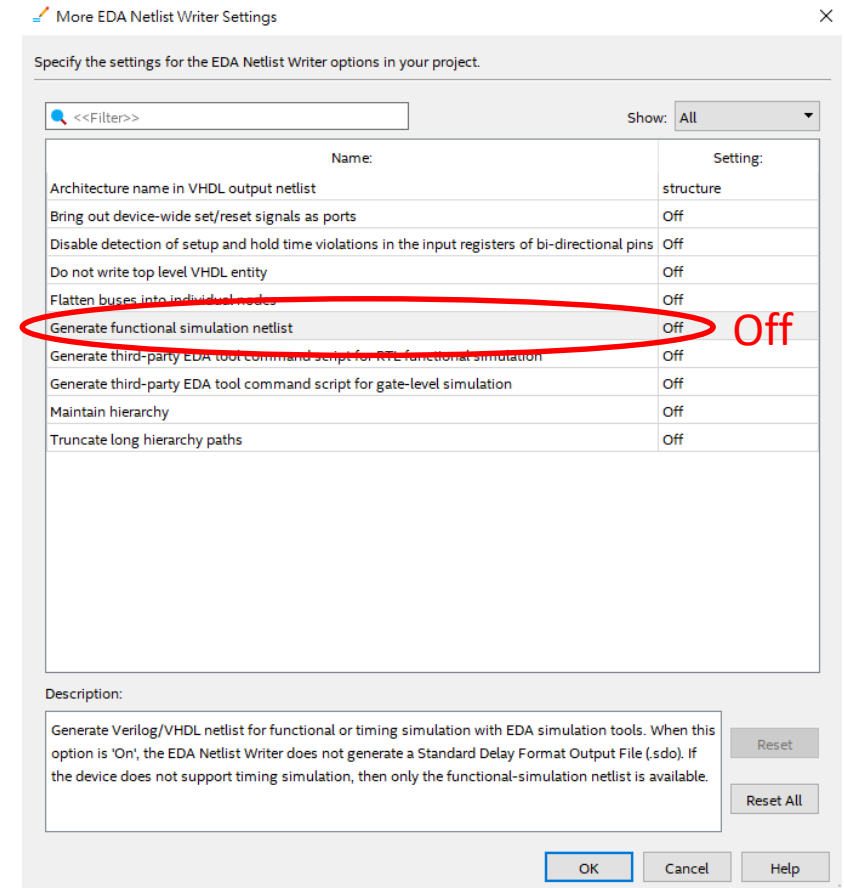
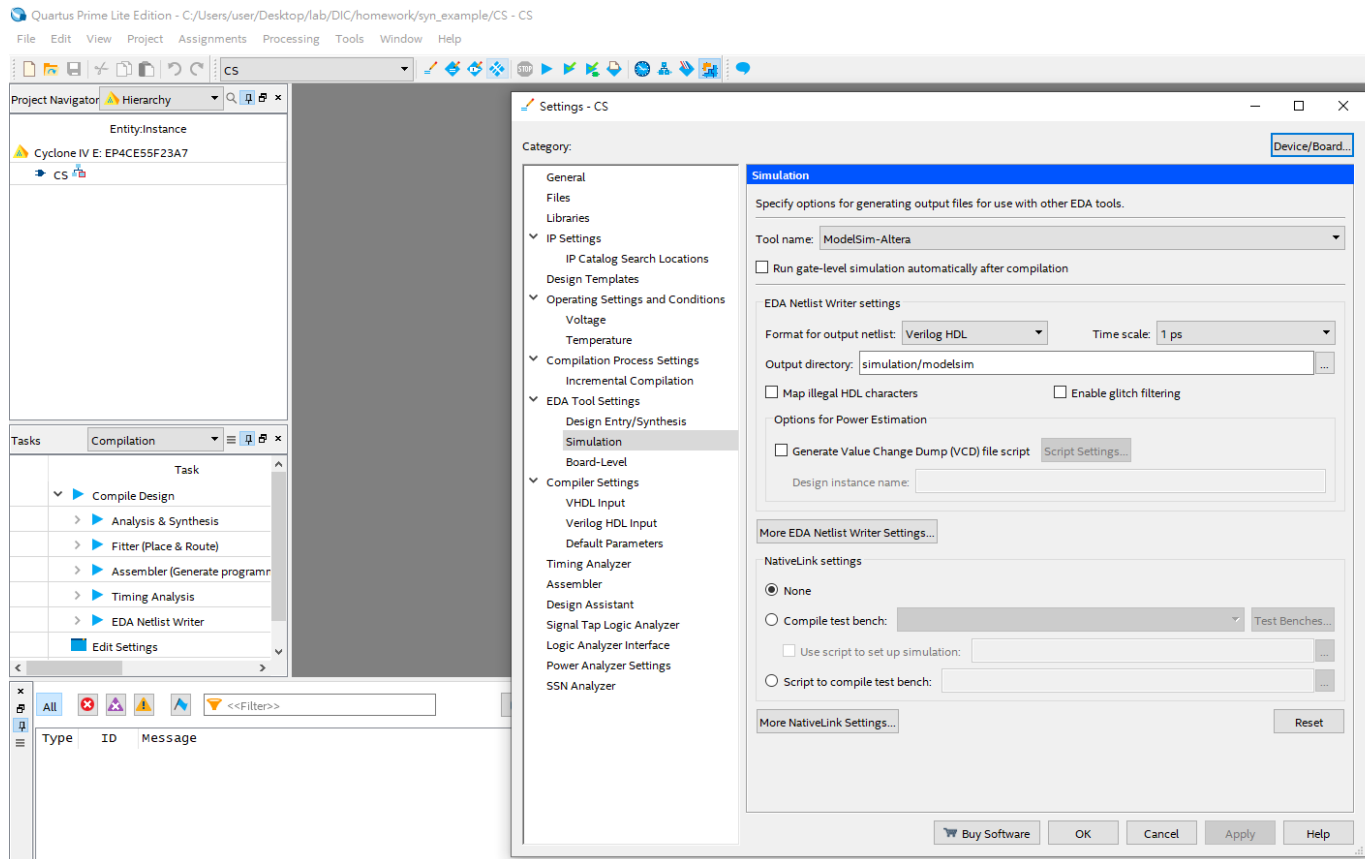


# Synthesis by Quartus

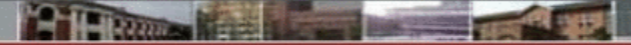


## ► Step 4 : compile

### ▷ Assignment > Settings > Simulation > More EDA Writer Settings



# Synthesis by Quartus



## ► Step 4 : compile

Quartus Prime Lite Edition - C:/Users/user/Desktop/lab/DIC/homework/syn\_example/CS - CS

File Edit View Project Assignments Processing Tools Window Help

Click

The screenshot shows the Quartus Prime IDE interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. Below the menu is a toolbar with various icons; a red circle highlights the 'Run' or 'Compile' icon (a blue play button). The left sidebar contains the 'Project Navigator' with a 'Hierarchy' view showing 'Entity: Instance' and 'Cyclone IV E: EP4CE55F23A7'. Below this is the 'Tasks' panel, which is set to 'Compilation'. It lists several tasks: 'Compile Design' (expanded), 'Analysis &amp; Synthesis', 'Fitter (Place &amp; Route)', 'Assembler (Generate program)', 'Timing Analysis', 'EDA Netlist Writer', and 'Edit Settings'. The main workspace area is mostly empty, displaying the 'Quartus Prime' logo and 'Version 20.1 Lite Edition'.

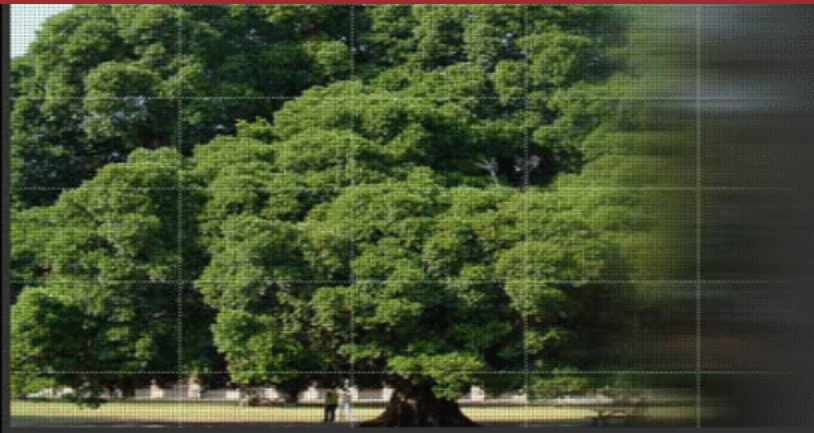
### Flow Summary

<<Filter>>

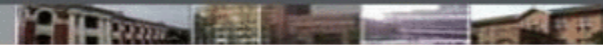
Flow Status	Successful - Tue Mar 21 10:12:45 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	CS
Top-level Entity Name	CS
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	576 / 55,856 ( 1 % )
Total registers	88
Total pins	20 / 325 ( 6 % )
Total virtual pins	0
Total memory bits	0 / 2,396,160 ( 0 % )
Embedded Multiplier 9-bit elements	0 / 308 ( 0 % )
Total PLLs	0 / 4 ( 0 % )



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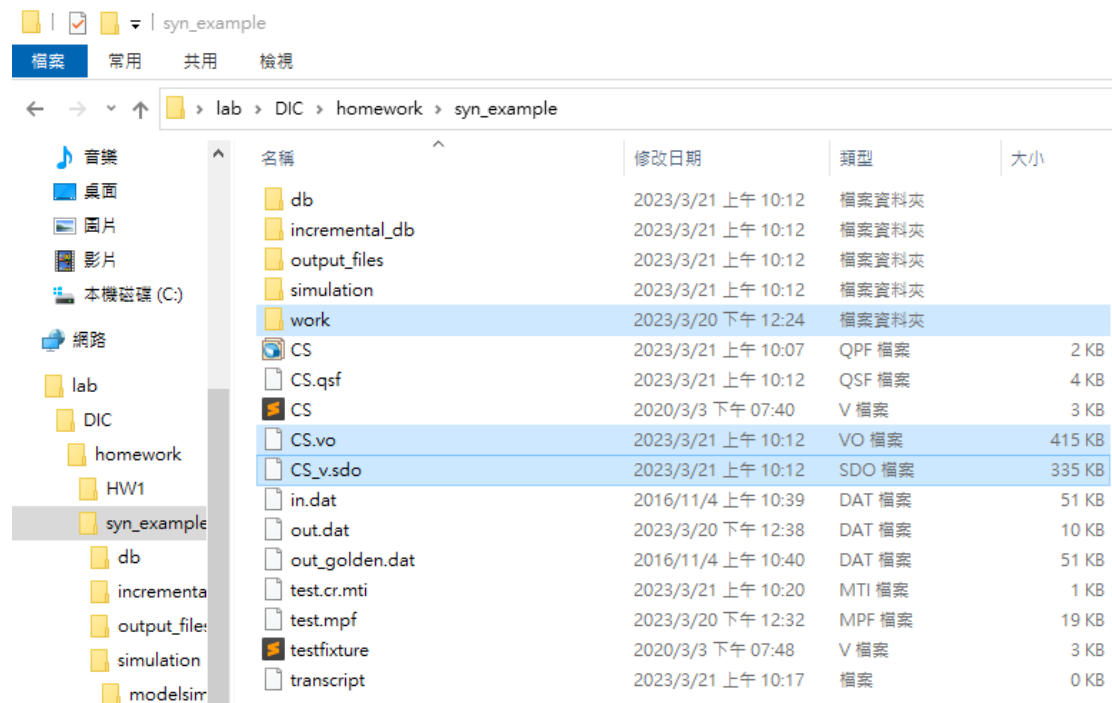
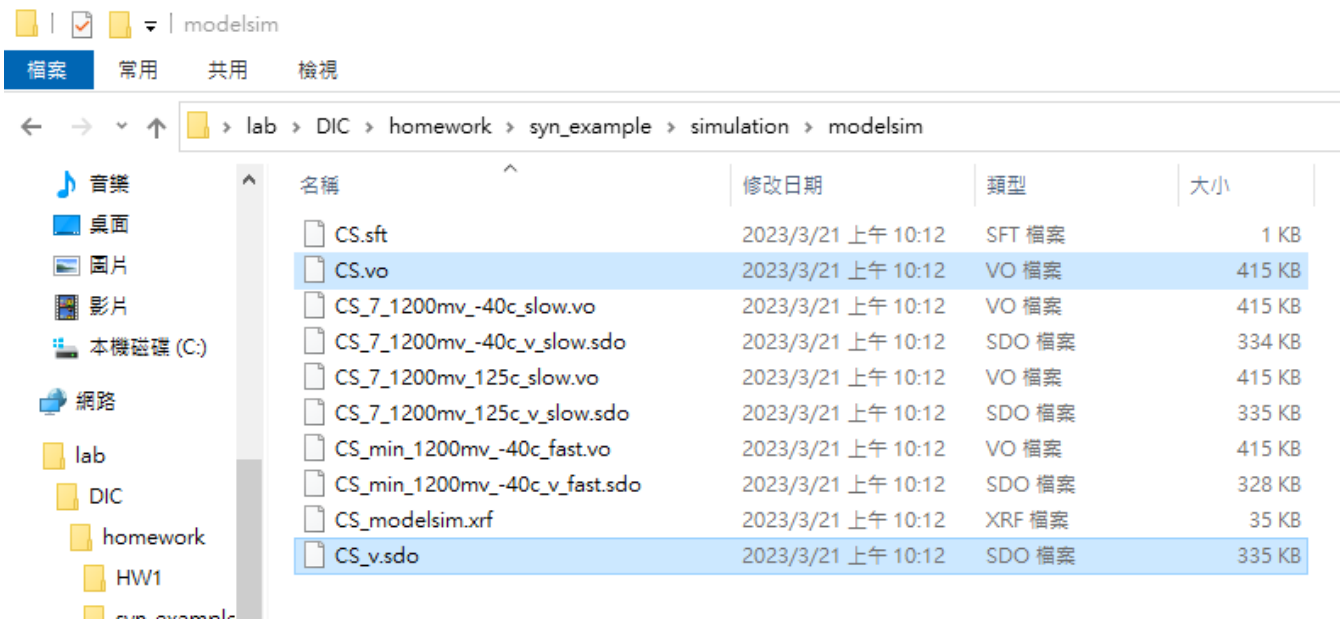


# Gate-Level Simulation by ModelSim



# Gate-Level Simulation by ModelSim

- ▶ Step 1 : the gate level file (\*.vo,\*.sdo) can be found in *simulation/modelsim* folder, and put them into **modelsim project directory** created in functional simulation section.
- ▶ **Simulation folder** is in the **Quartus project** directory created in the synthesis section.

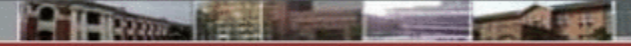


# Gate-Level Simulation by ModelSim



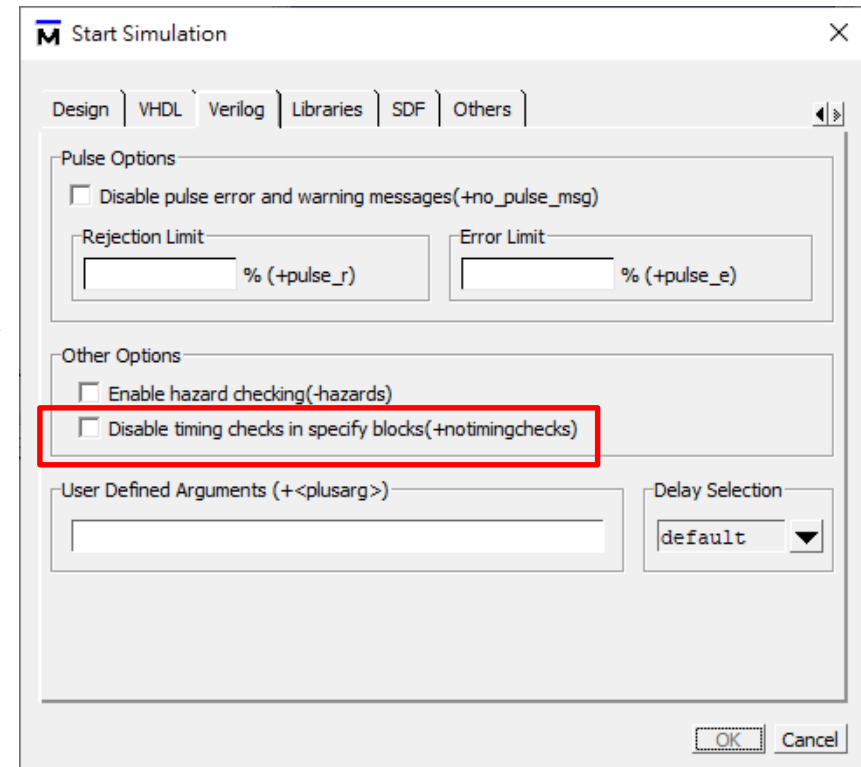
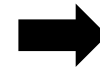
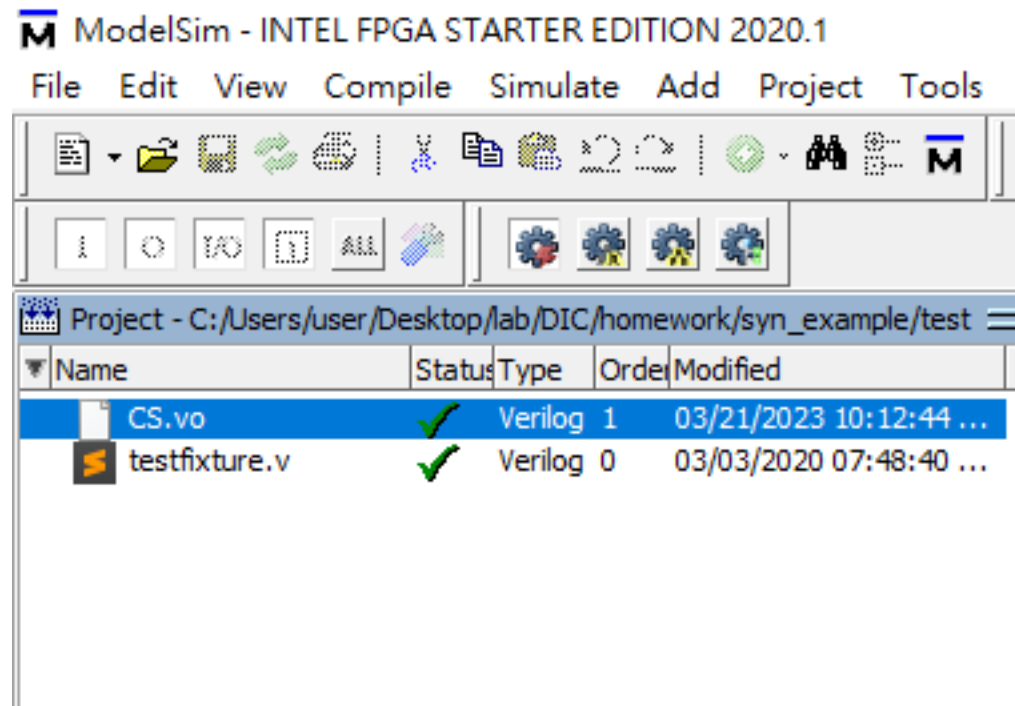
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## ► Step 2 : gate level simulation

- ▷ (Simulate -> Start Simulation Window)
- ▷ This time, use the \*.vo for simulation ( Replace the original top\_module.v with \*.vo )
- ▷ Repeat the steps of functional simulation. ( Need to cancel the no timingchecks. )



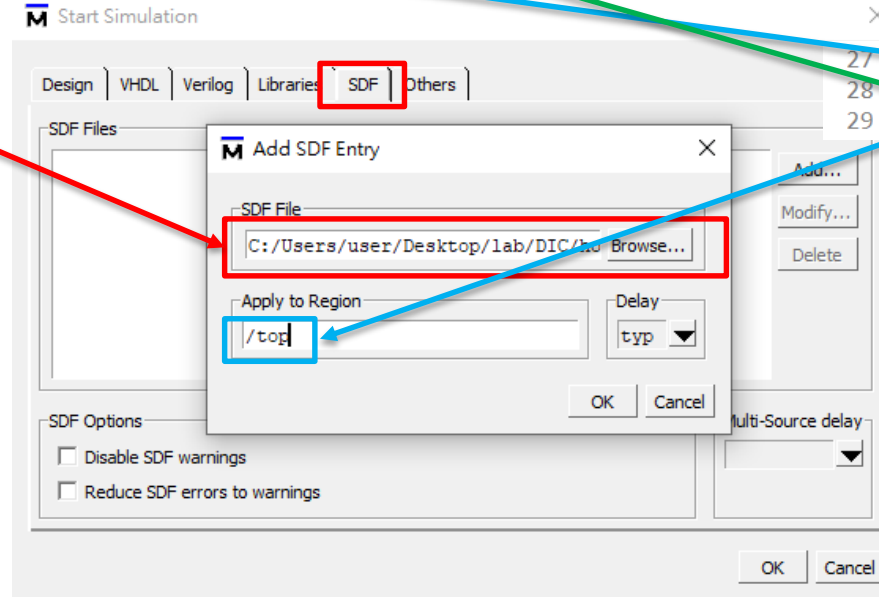
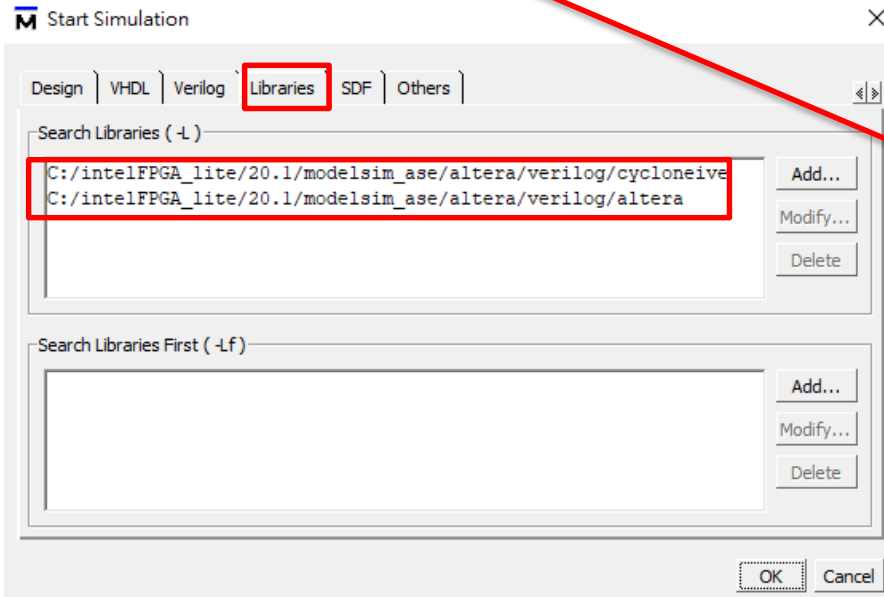


# Gate-Level Simulation by ModelSim



## ► Step 2: Gate Level Simulation

- Add **cycloneive** and **altera** library to search libraries ( click Libraries to add )
  - your quartus installation disk/altera/13.0sp1/modelsim\_ase/altera/Verilog/cycloneii
- Add **\*.sdo** to SDF Files and fill **the instance name of your design in testbench.v** in “apply to region” (click SDF to add)



Testbench file

```
27 CS top (.Y(Y), .X(X), .reset(reset), .clk(clk));  
28  
29
```