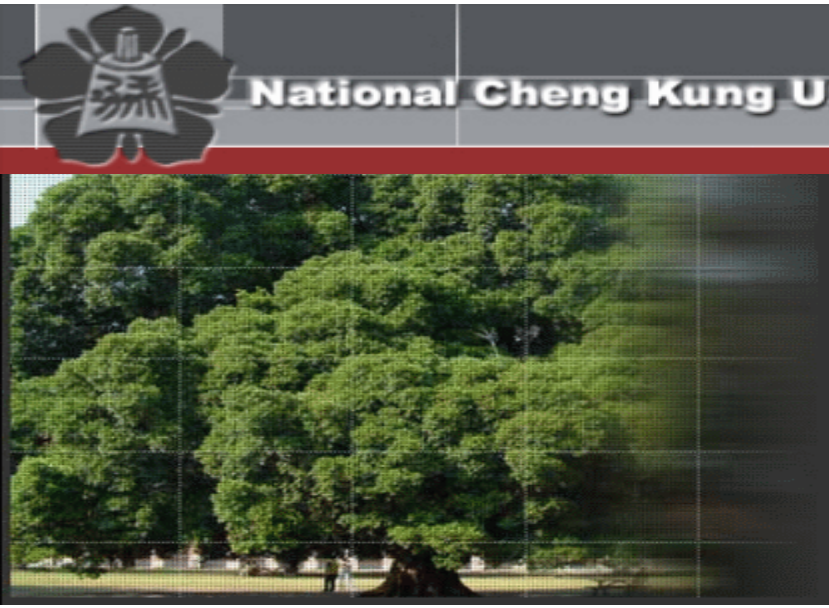

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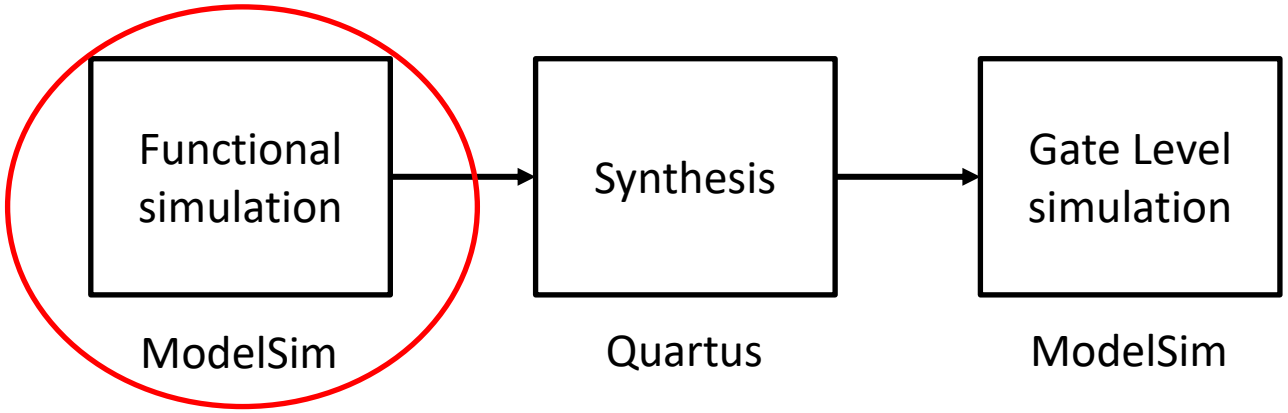
數位IC設計 Tool安裝&作業模擬教學

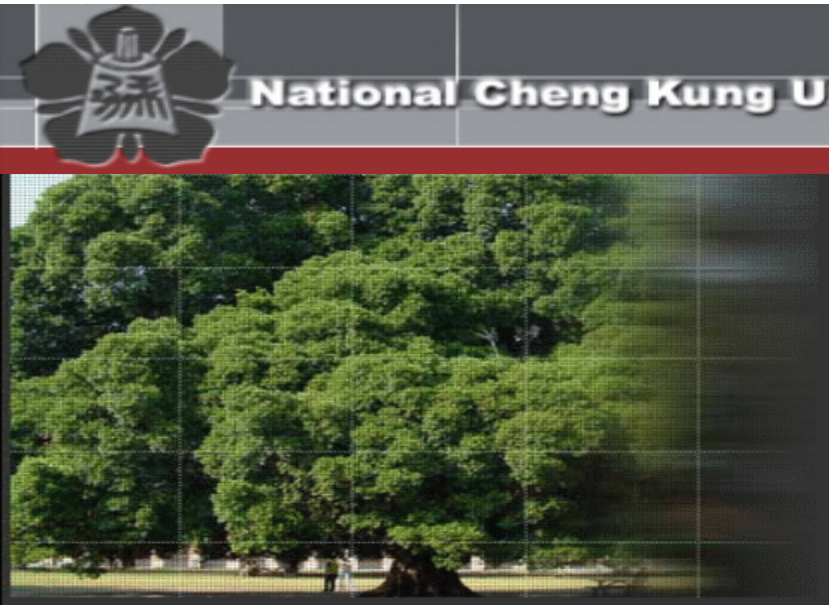
NCKU CSIE DICLAB

The simulation process

- The simulation process and the necessary tools in this class



- The tools can be downloaded from :
  - https://www.intel.com/content/www/us/en/software/programmable/quartus-prime/download.html#



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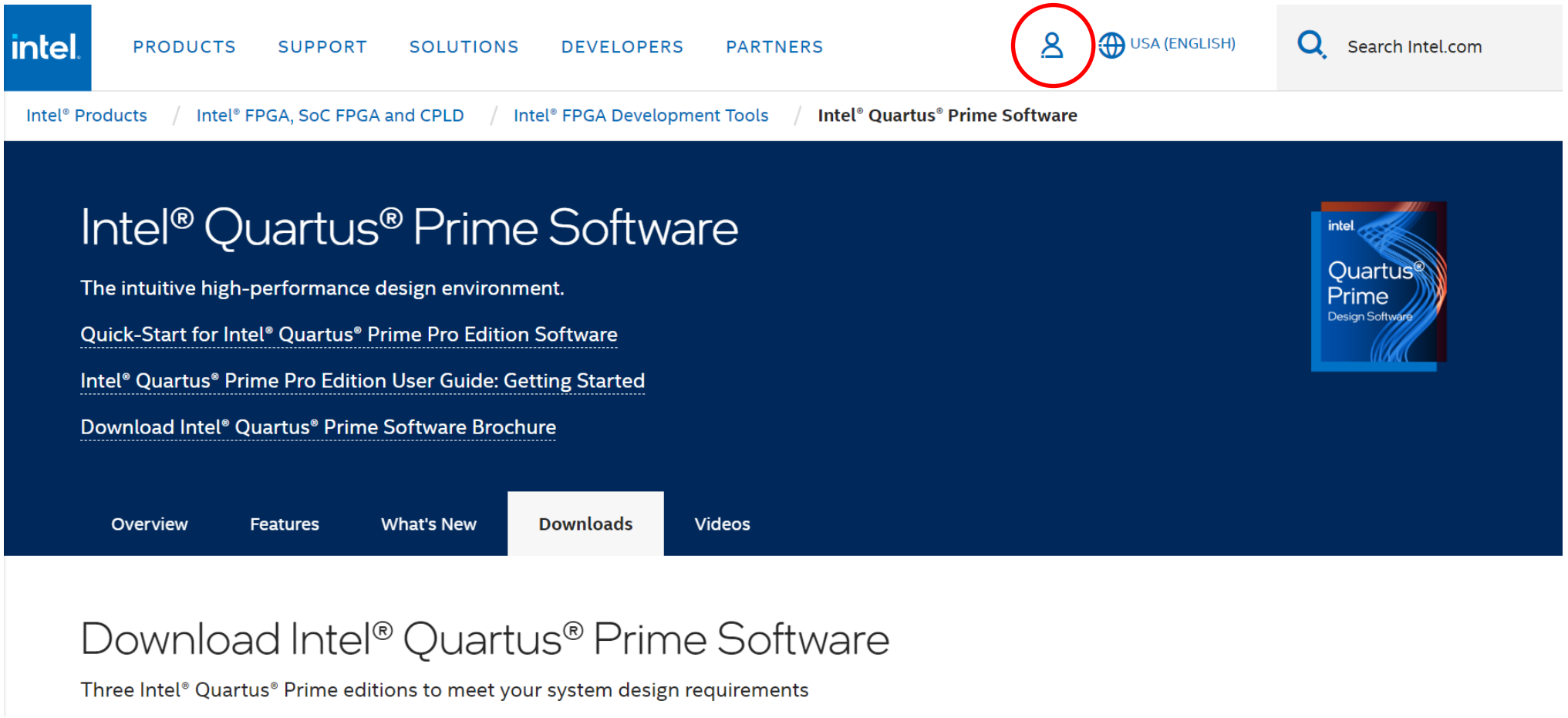
Download and install Modelsim

Download and install Modelsim

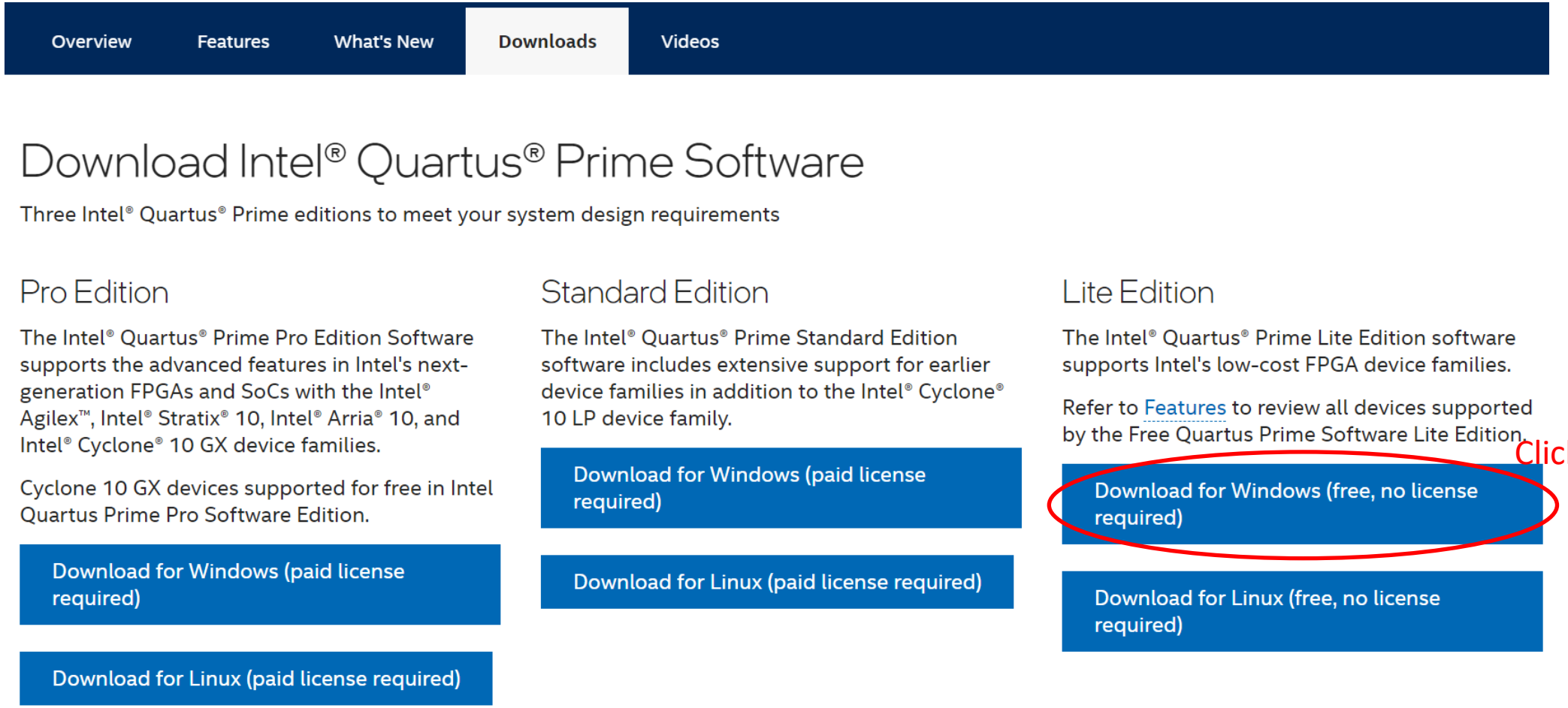
- Step 1: Register and sign in

Click here to create an account and sign in



Download and install Modelsim

- Step 2: Click “ Download for Windows(free, no license required)“



Download and install Modelsim

- Step 3: Select software version (20.1.1)

Intel® Quartus® Prime Lite Edition Design Software Version 20.1.1 for Windows

ID	Date	Version
660907	11/22/2020	20.1.1

Select version 20.1.1

A newer version of this software is available, which includes functional and security updates. Customers should click here to update to the latest version.

Users should upgrade to the latest version of the Intel® Quartus® Prime Design Software. The selected version does not include the latest functional and security updates. If you must use this version of software, follow the technical recommendations to help improve security. For critical support requests, please contact our support team.

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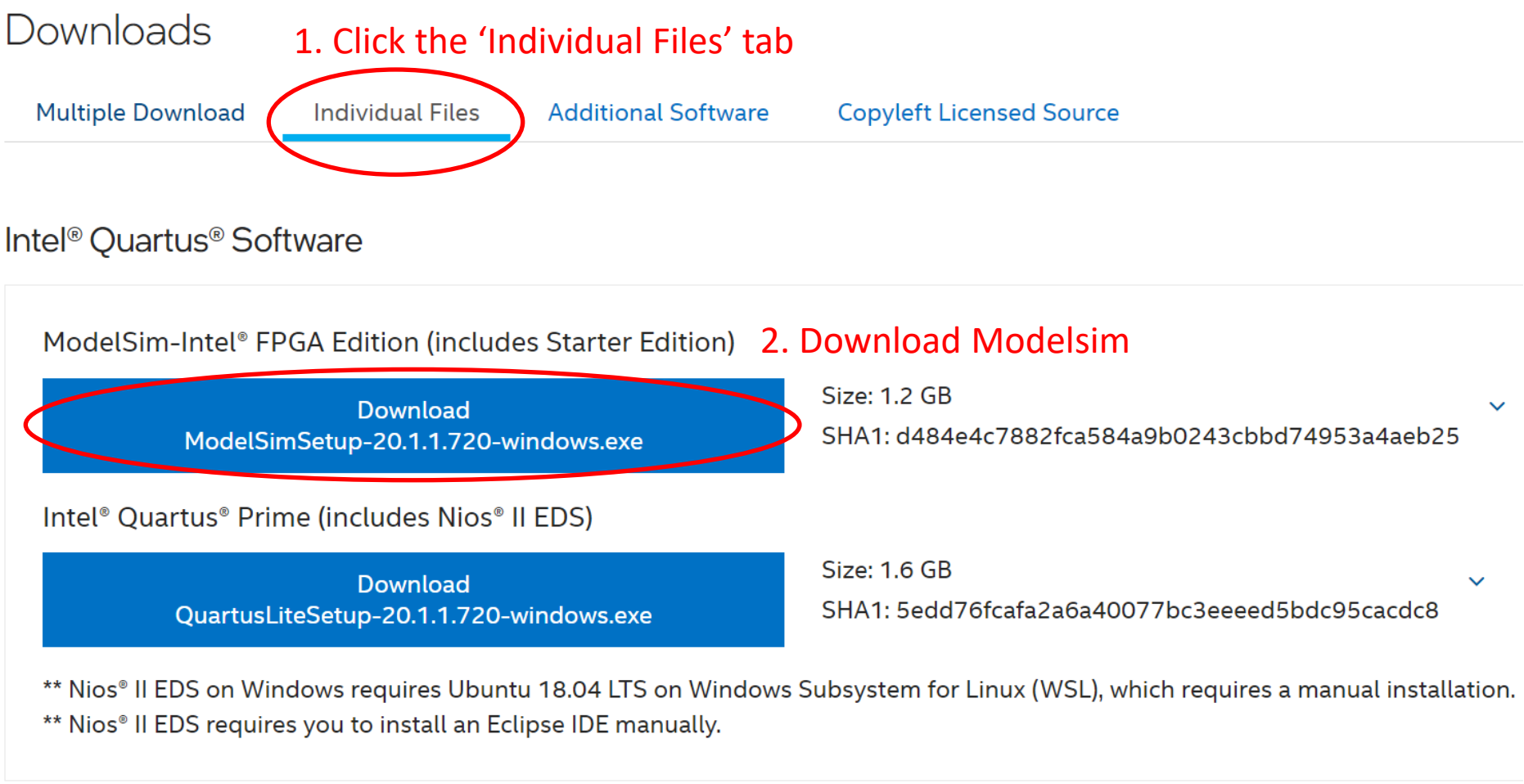
- Step 4: Download Modelsim setup execution file



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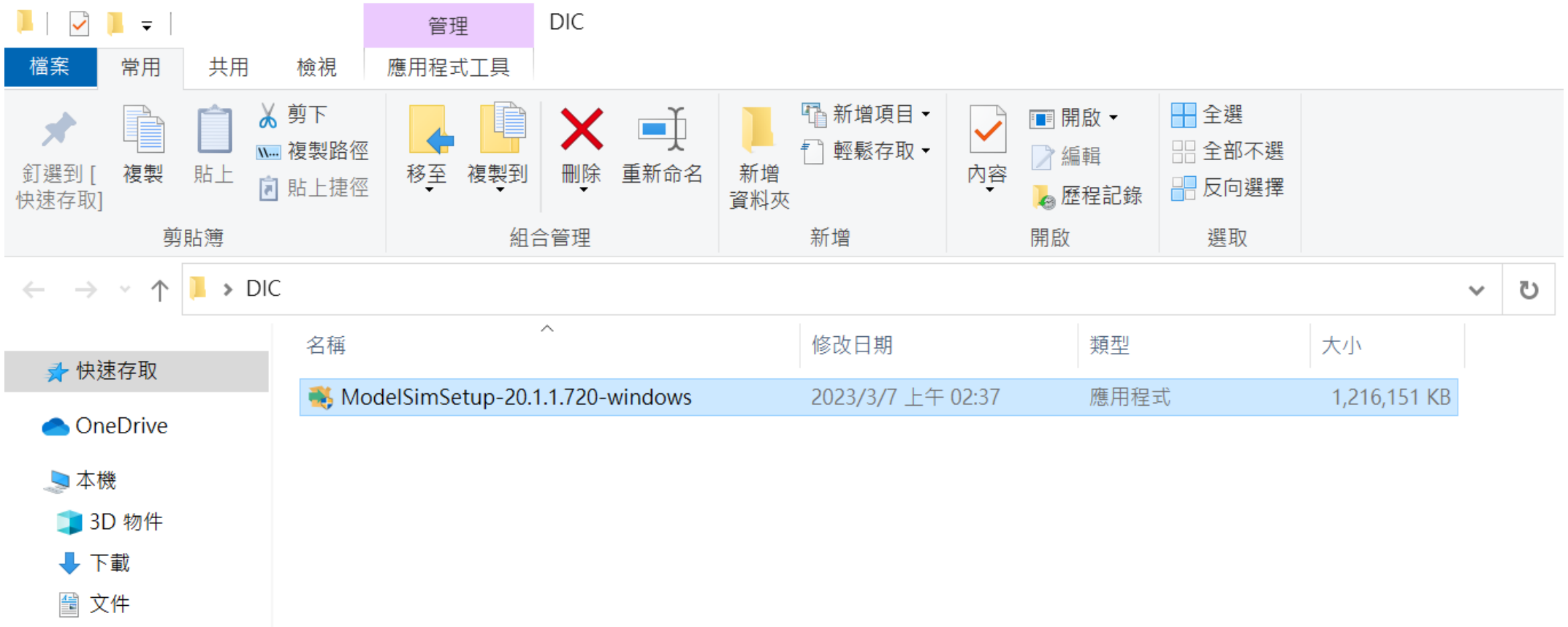
- Step 5: Installation



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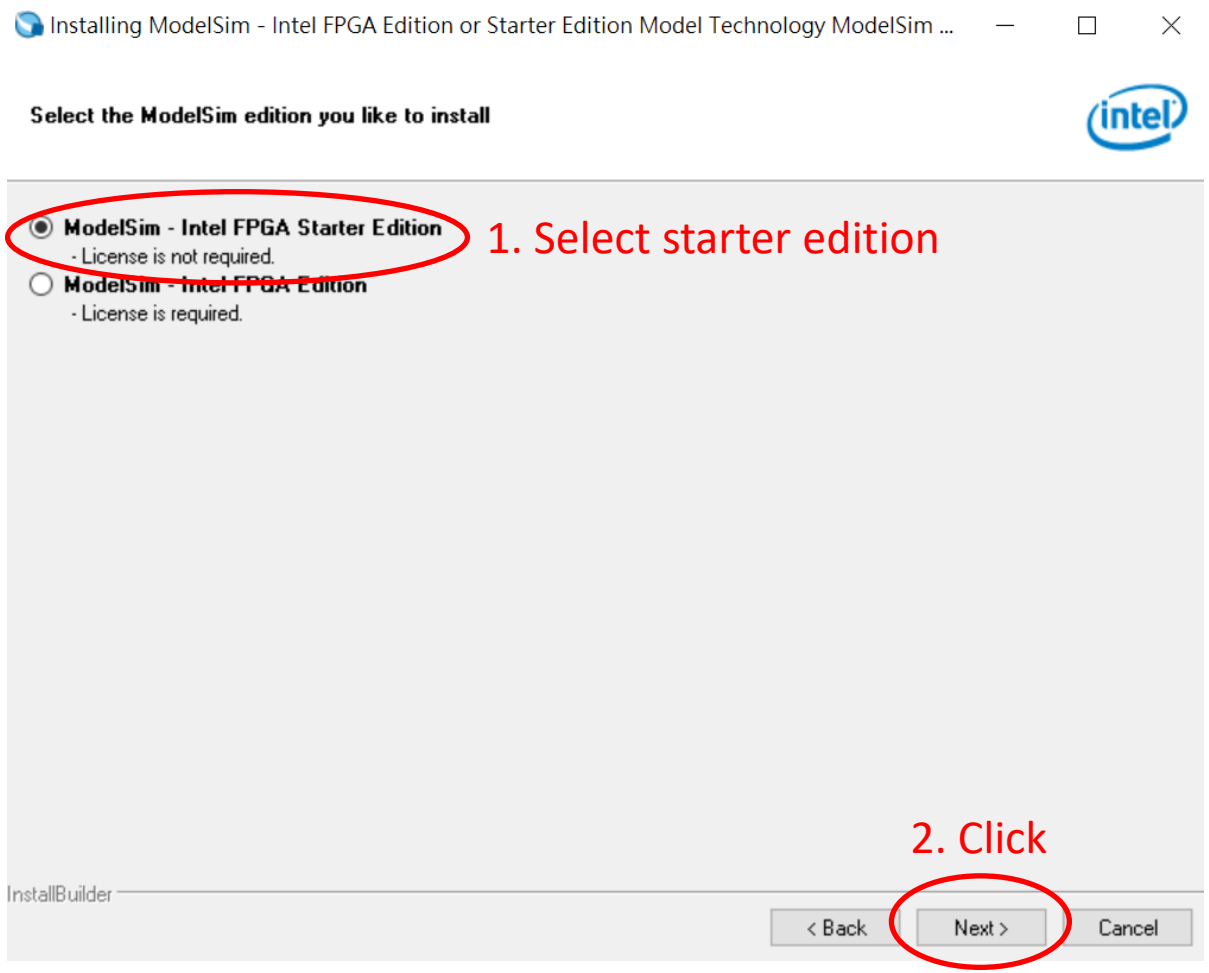
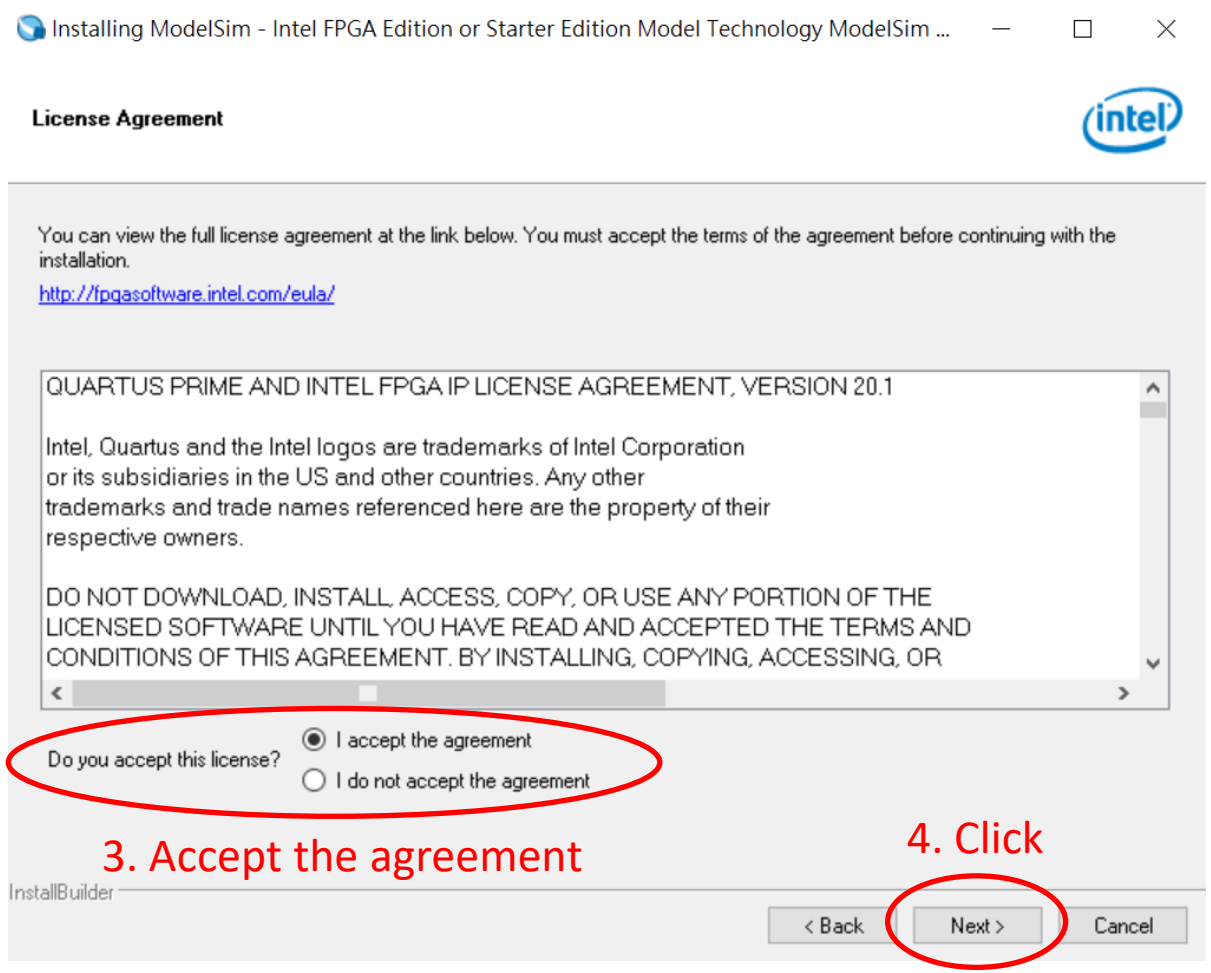
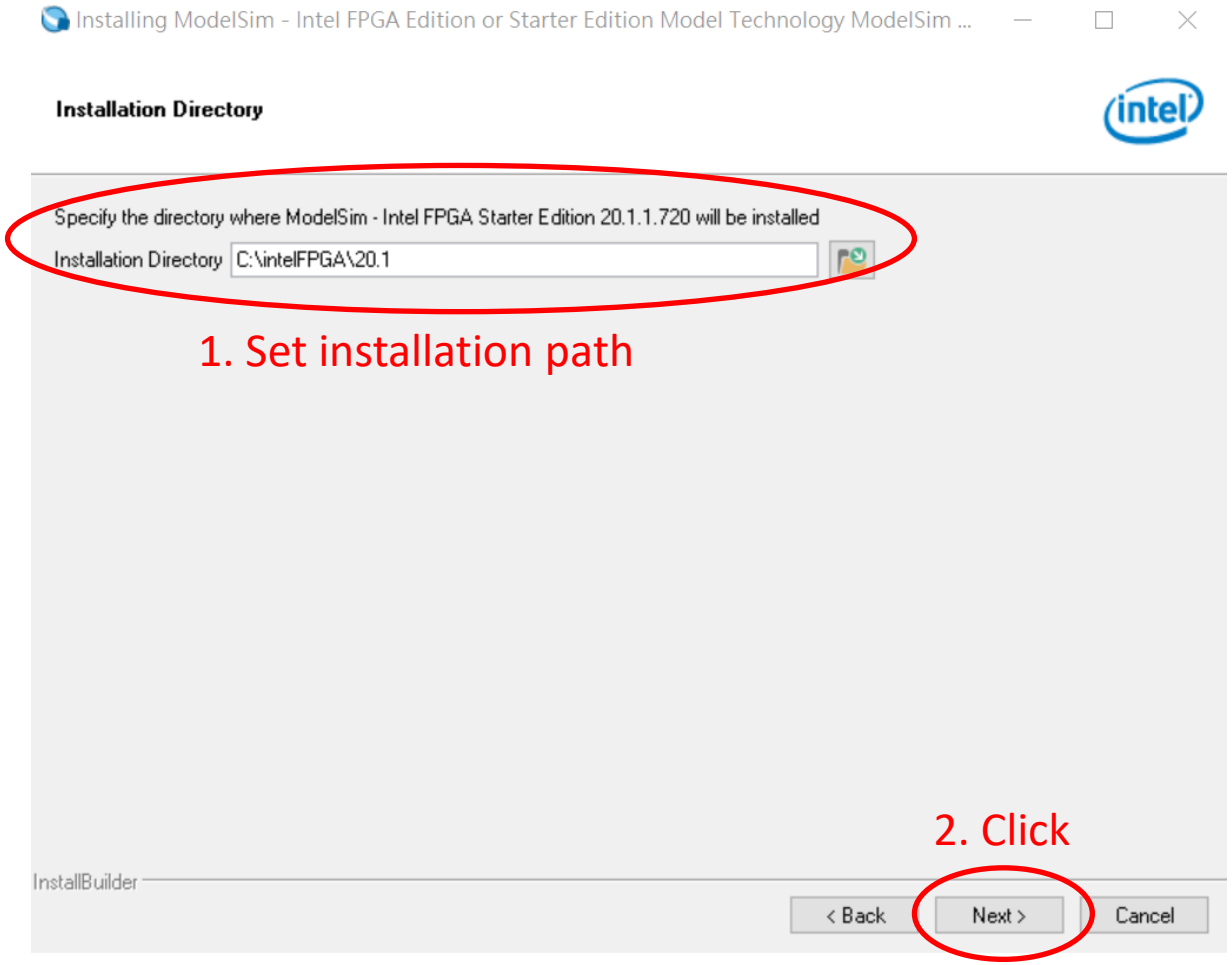
Step 5: Installation

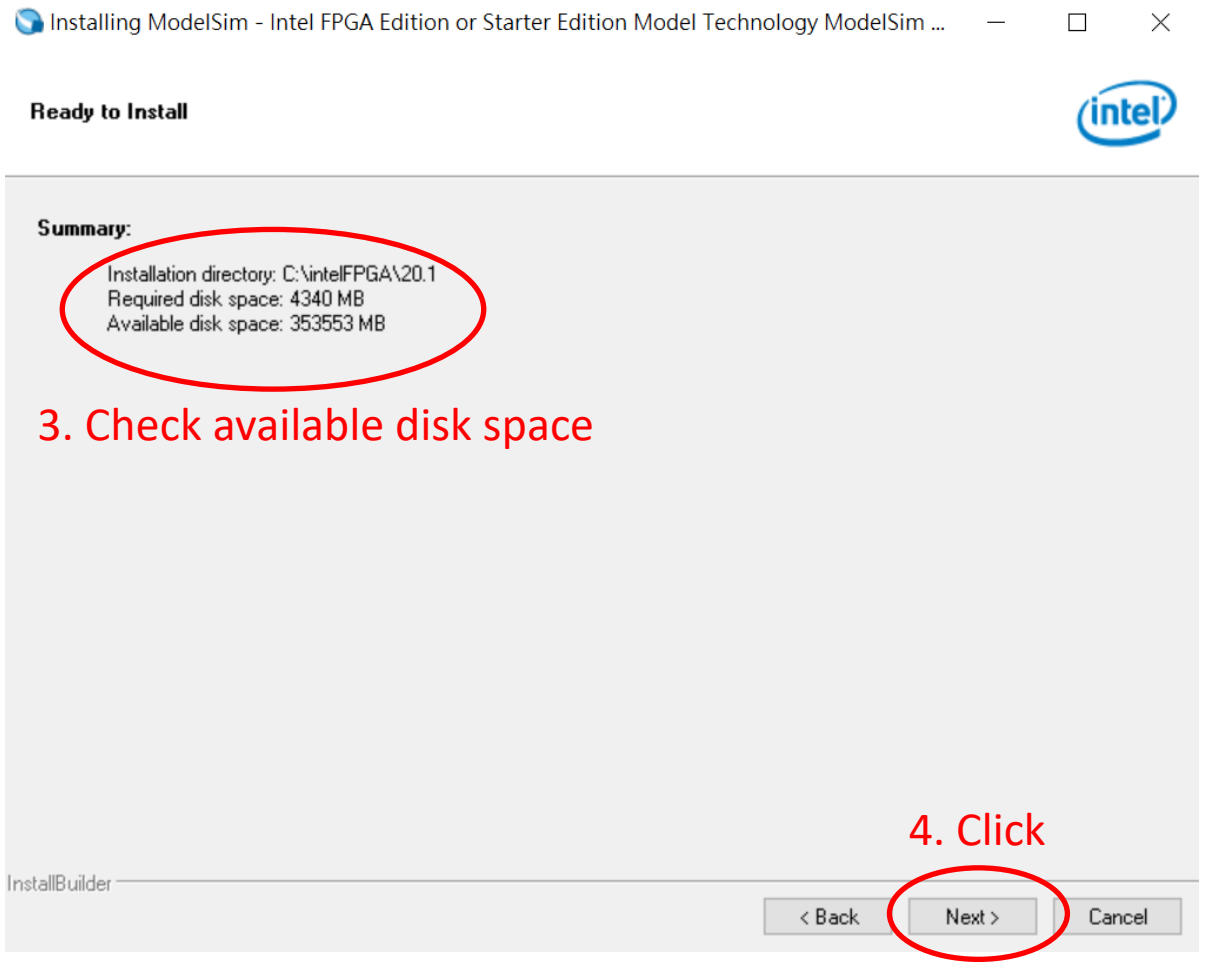




Download and install Modelsim

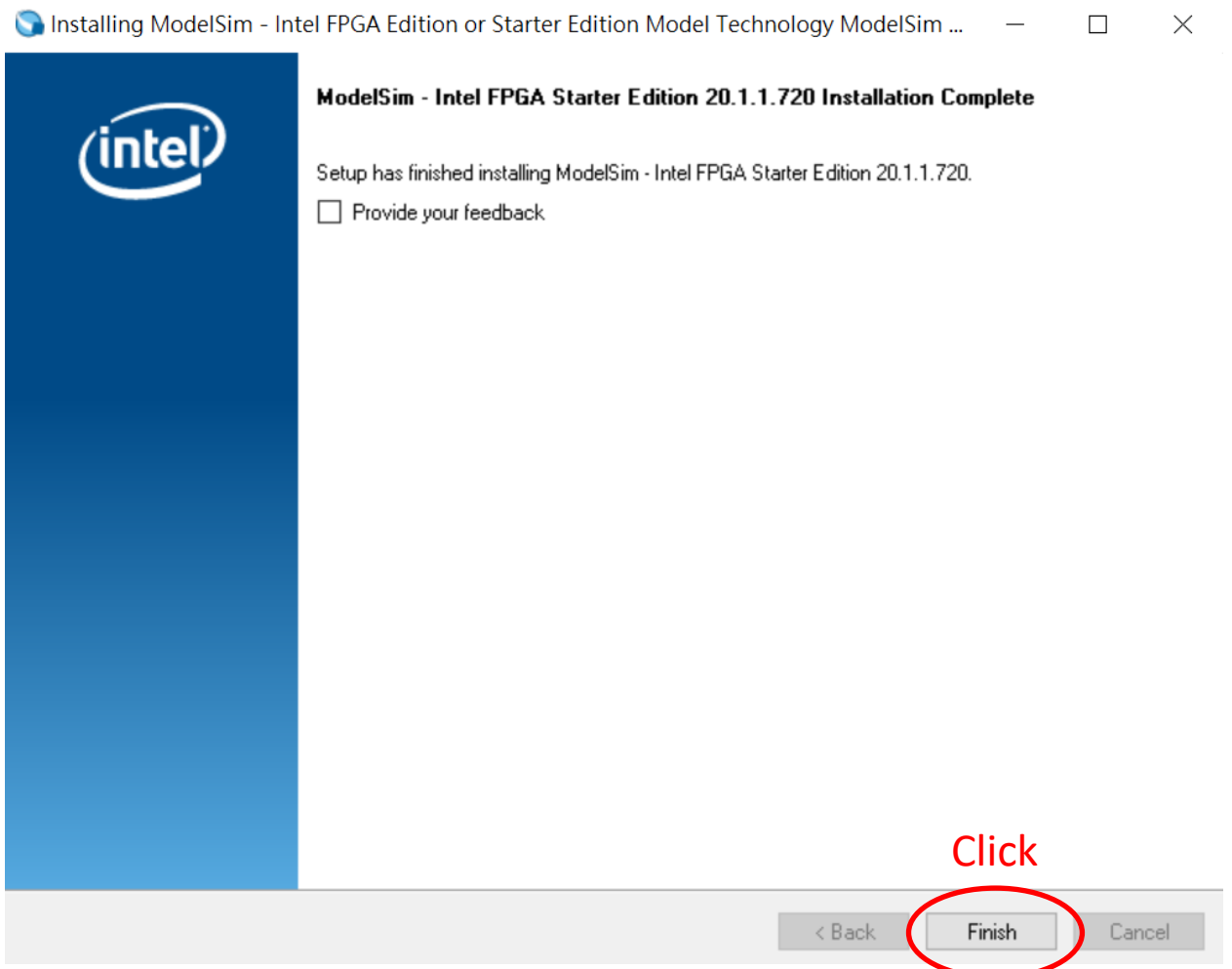
- Step 5: Installation

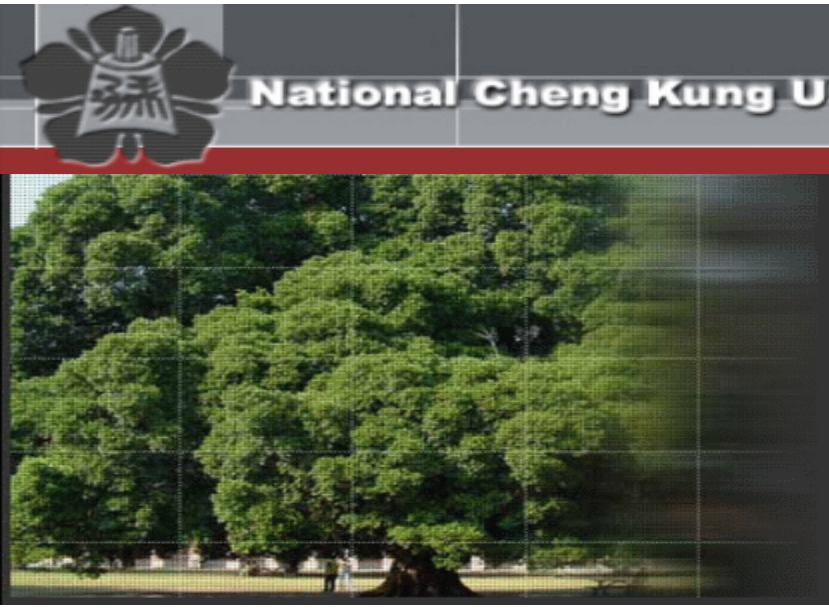




Download and install Modelsim

- Step 5: Installation





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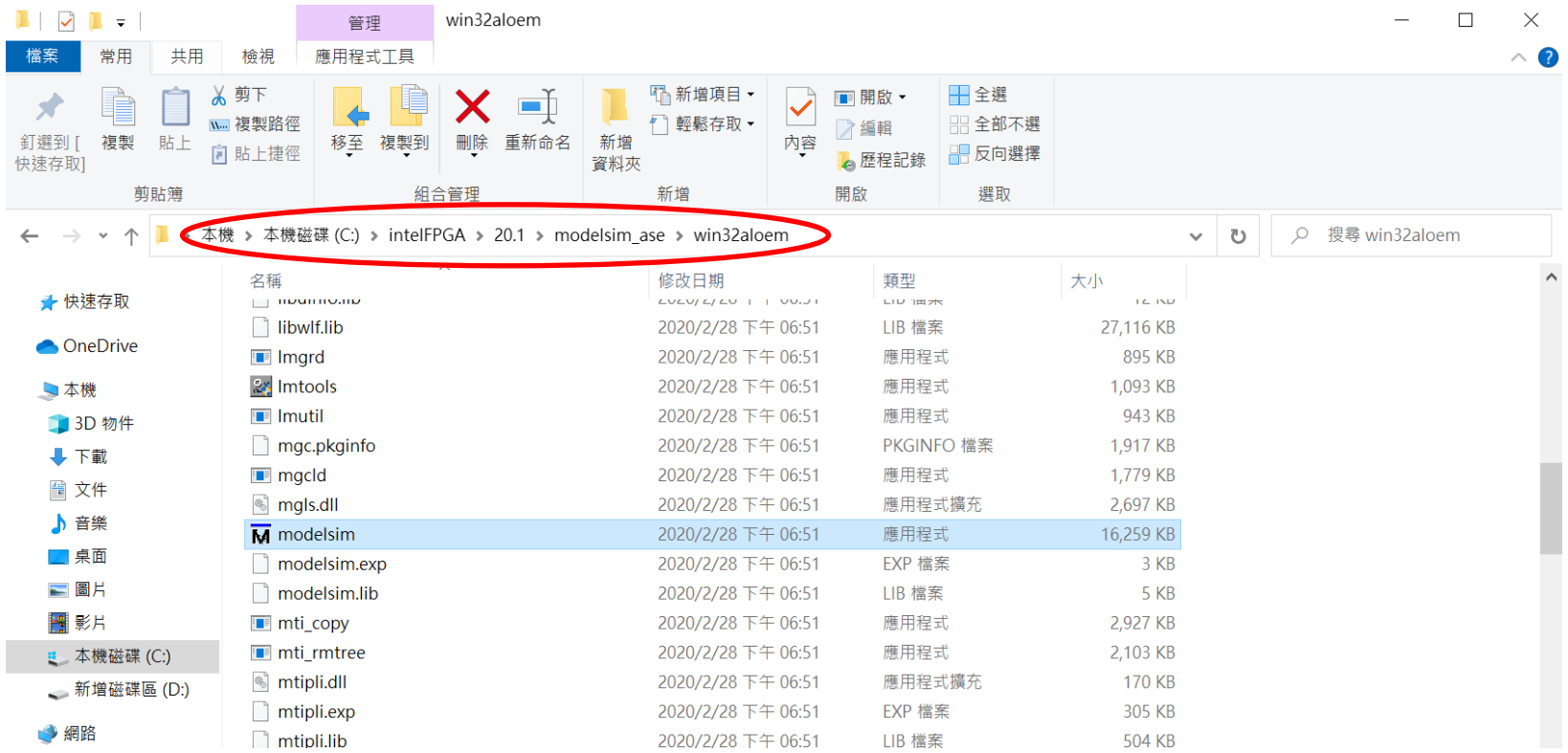
Functional Simulation by ModelSim

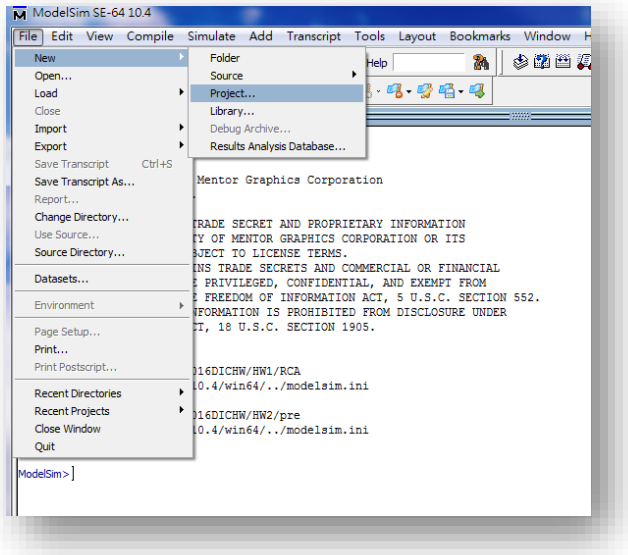
Functional Simulation by ModelSim

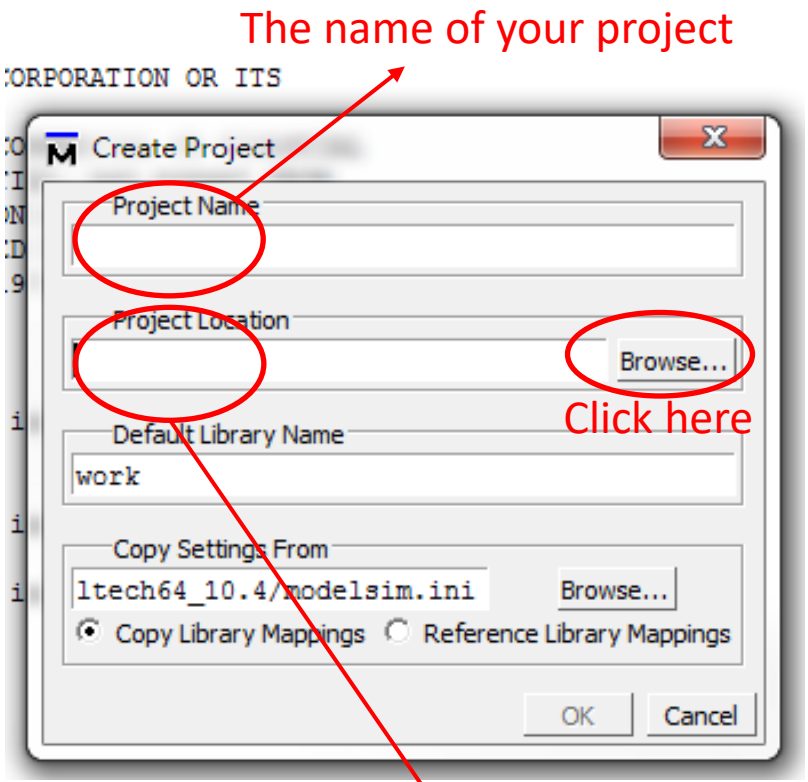
- Step 1: Run modelsim.exe
  - Your installation path
    - Ex: C:\intelFPGA\20.1\modelsim_ase\win32aloem\modelsim.exe

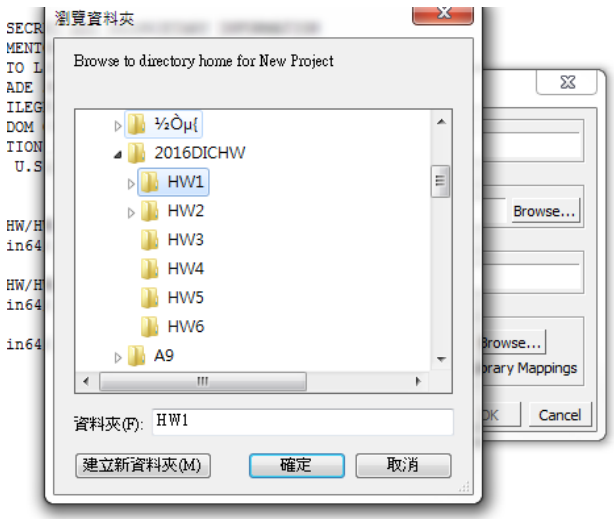


Functional Simulation by ModelSim

- Step 2: Create a new project
  - File -> New -> Project
  - Click “Browse…”



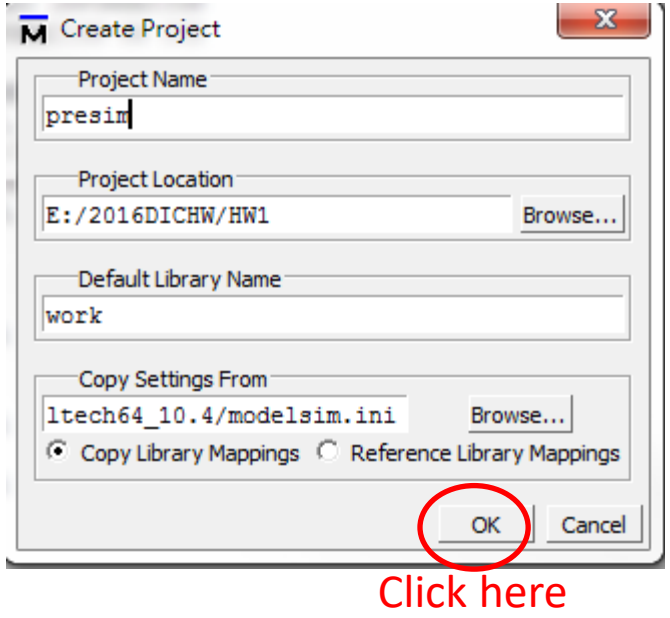


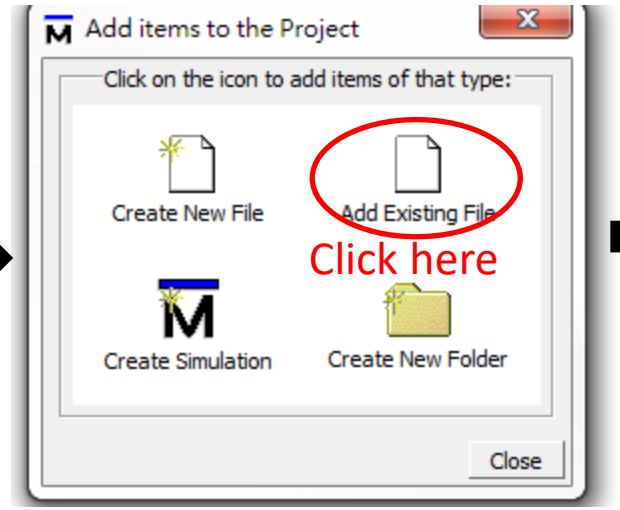


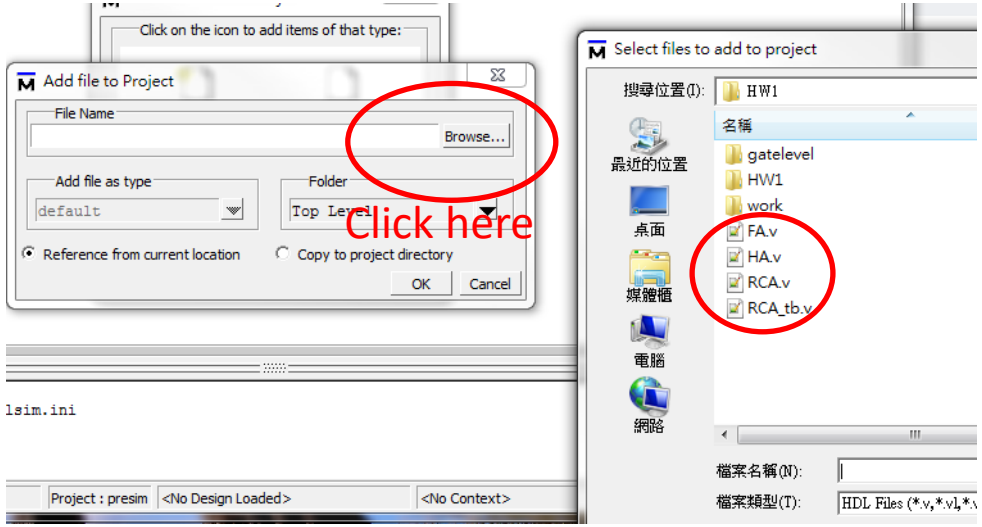
The file path should be ALL ENGLISH

Functional Simulation by ModelSim

- Step 2: Add the files
  - Select all the .v files including the testbench
    - Verilog code could be stored in any location , “add existing file” would refer to the file location automatically .
    - Remember to put the test data and golden data at the same directory of the testbench file.

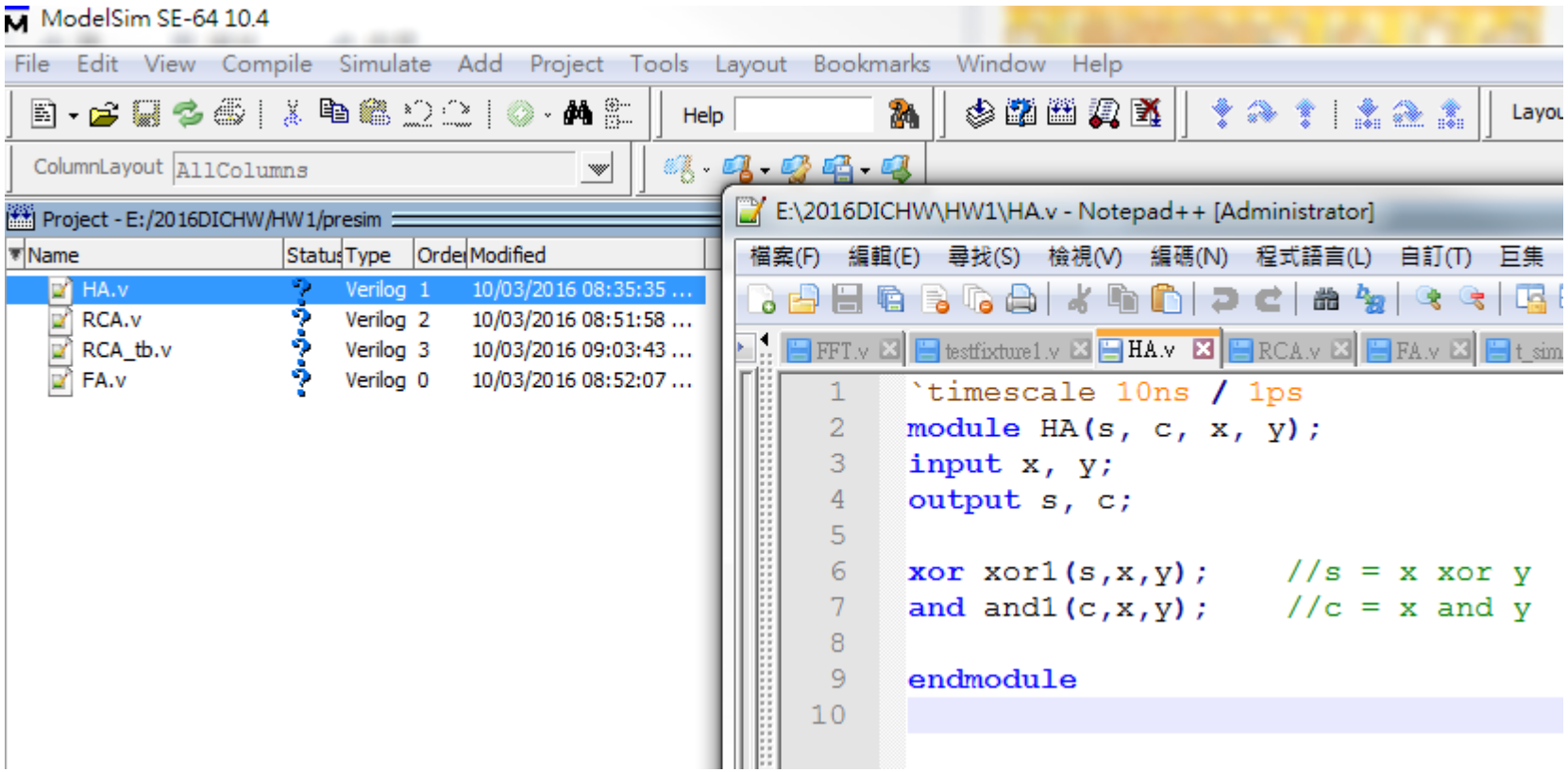






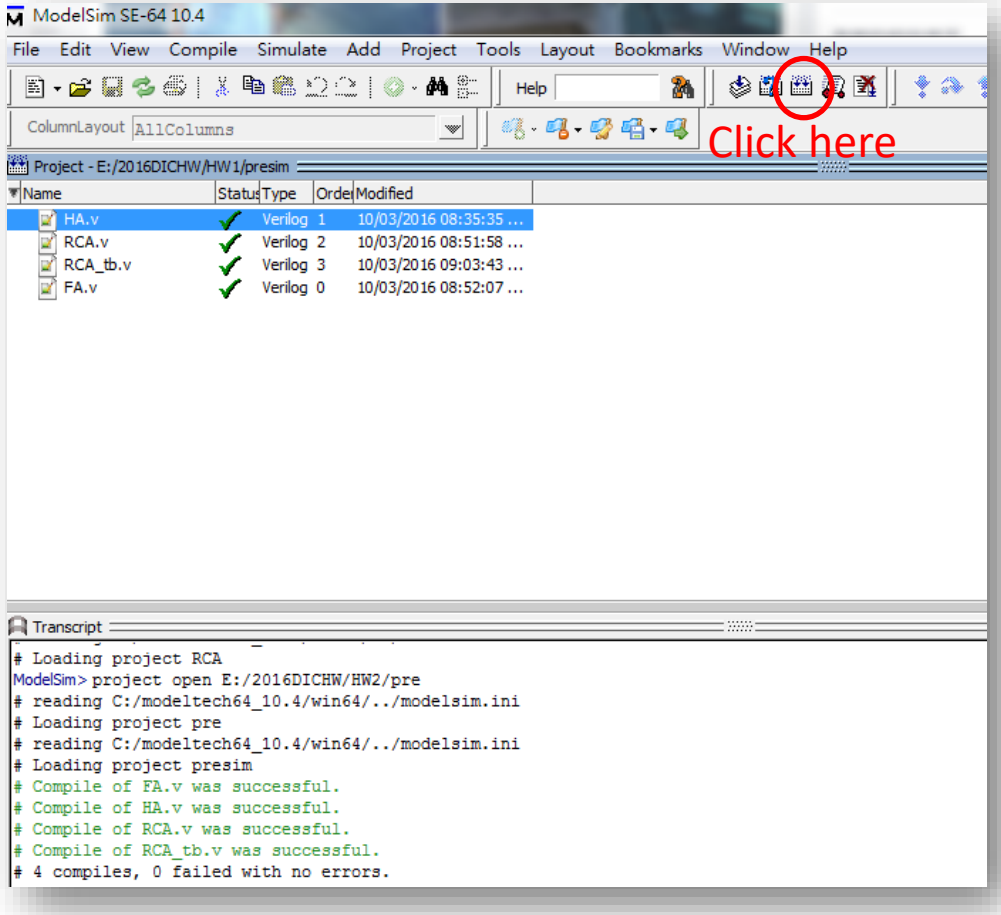
Functional Simulation by ModelSim

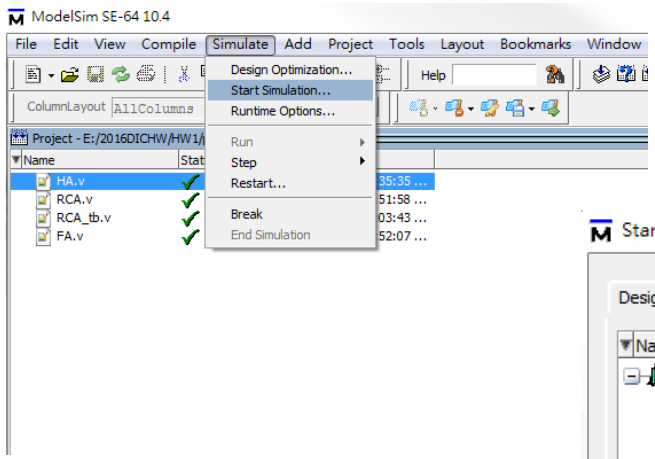
- Step 3 : Start coding…

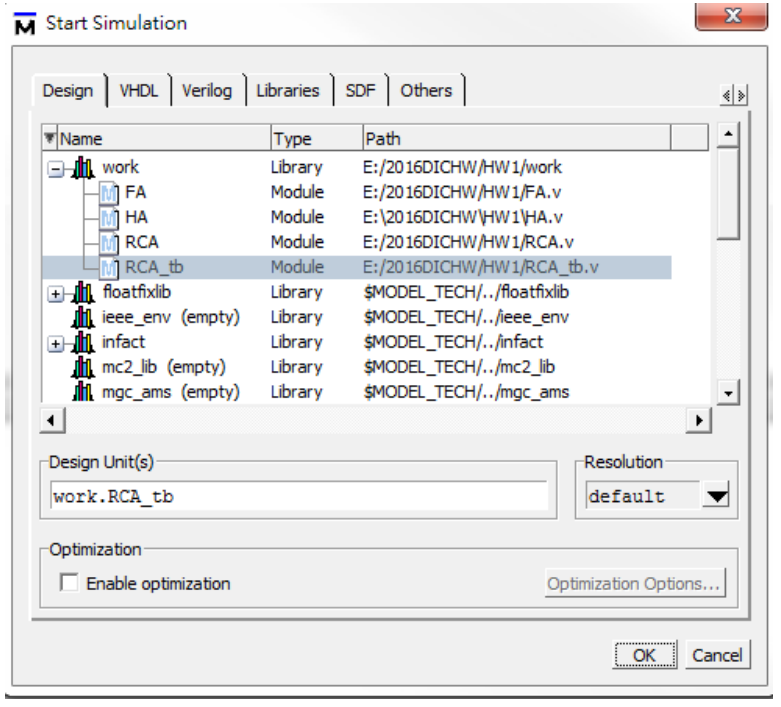


Functional Simulation by ModelSim

- Step 4: Compile & Start simulation
  - Compile -> Simulate -> Start Simulation->work->testbench file

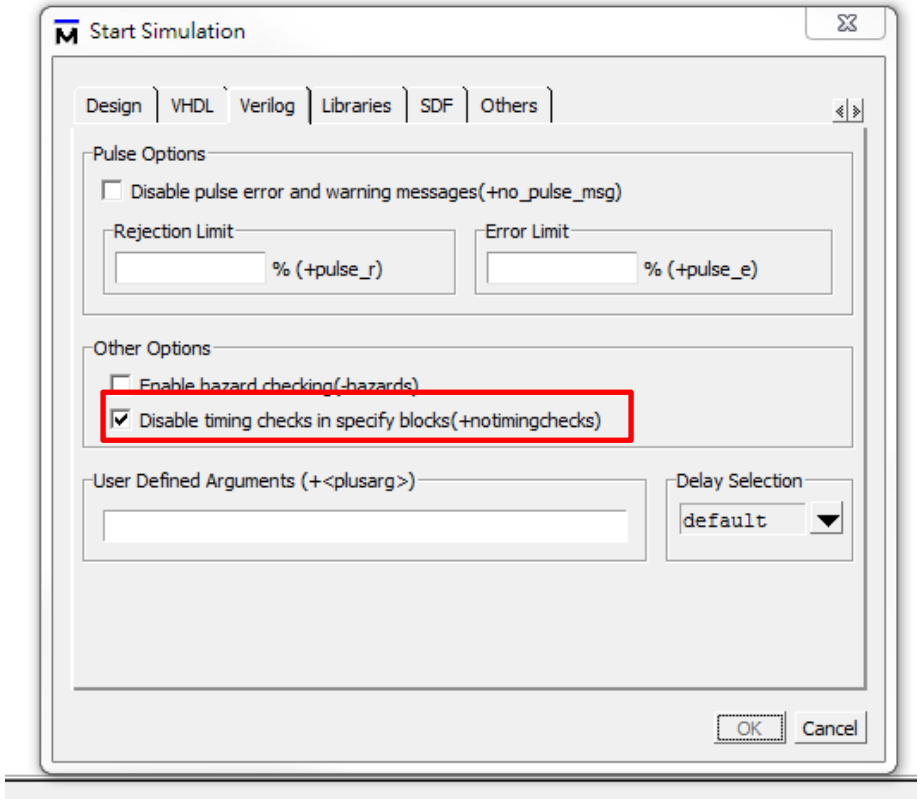






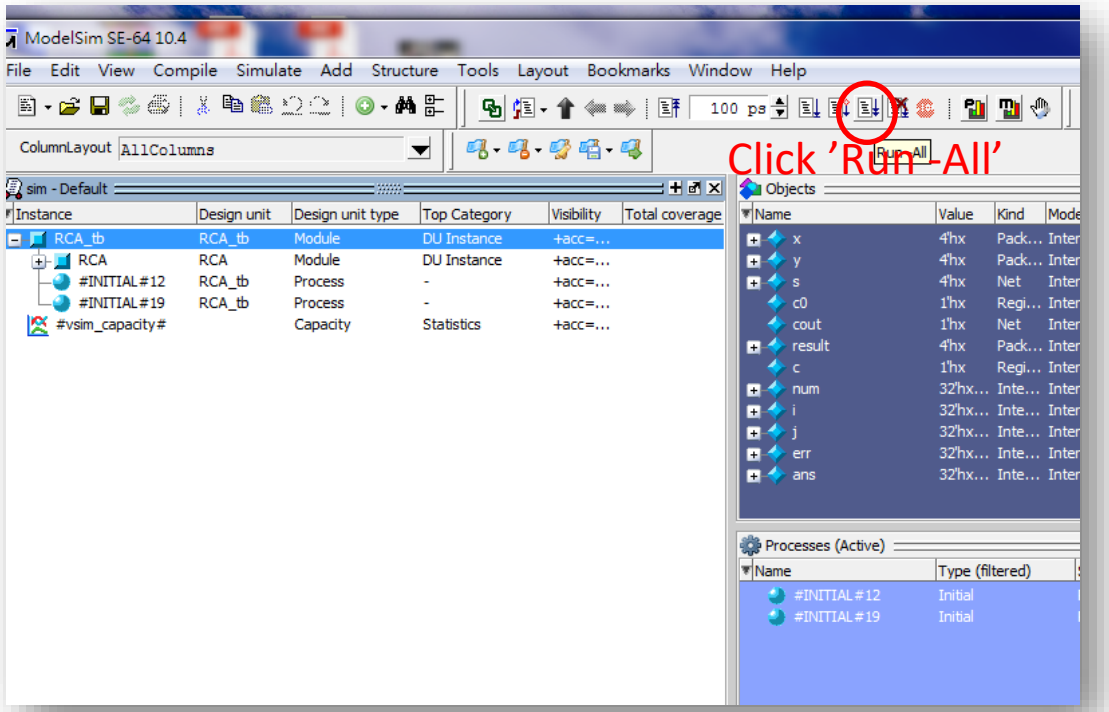
Functional Simulation by ModelSim

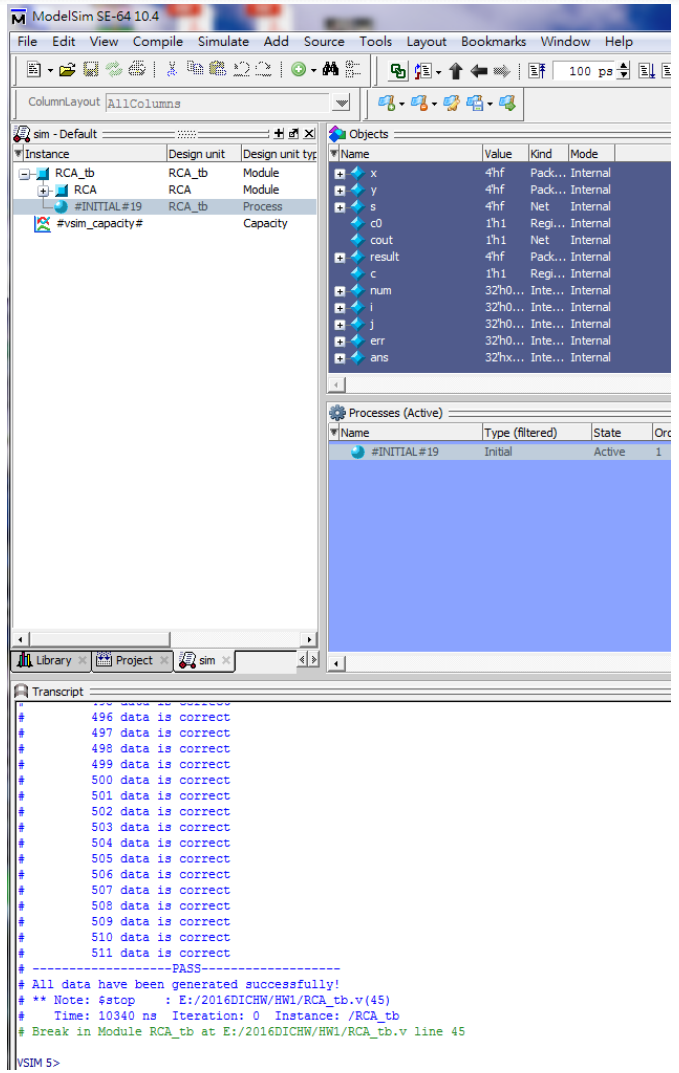
- Step 4: Start simulation
  - Check +notimingchecks

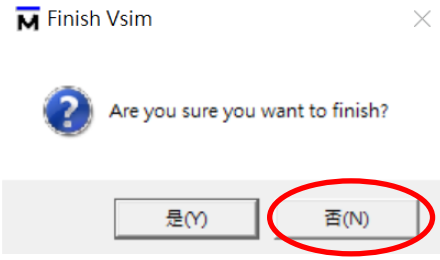


Functional Simulation by ModelSim

- Step 5 : Simulation





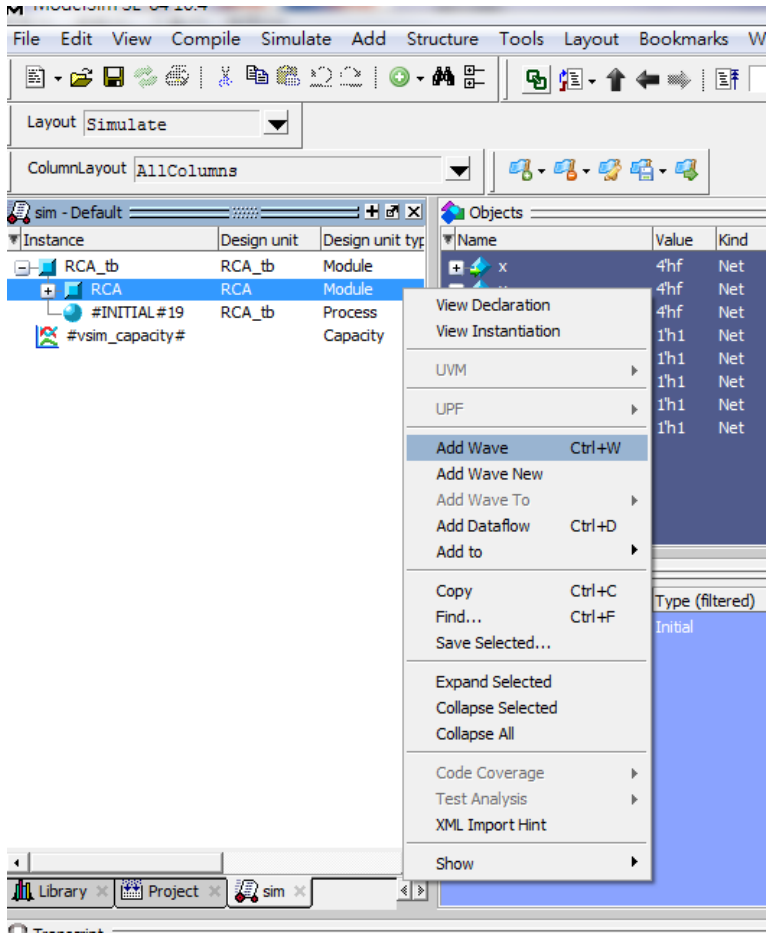


Click '否(N)'

*If you click '是(Y)', Modelsim will be closed

Functional Simulation by ModelSim

- Step 6 : Show waveform



You have to “restart” before a new simulation