Notes for *Fundamentals of Microelectronics (Razavi) (2nd edition, 2014)*

《微电子基础》笔记

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Preface

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序言

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Contents

Chapter 1 Introduction to Microelectronics

Table 1.1: Frequently used physical constant

Symbol	Note	Value	Unit
k	Boltzmann constant	1.38×10^{-23}	J
c	velocity of light	2.9979×10^{8}	m/s
h	velocity of light	$6.\ 626\ 070\ 15 \times 10^{-34}$	J · s
R	universal gas constant	8.31	J / (mol · K)
ε_0	permittivity of vacuum	8.85×10^{-14}	F/cm
e	electron charge	$1.\ 602 \times 10^{-19}$	C
m_e	electronic mass	$9.\ 109\ 382\ 15\ (45) \times 10^{-31}$	kg
m_e	electronic mass	$0.\ 510\ 998\ 910\ (13)$	MeV/c^2
m_p	proton mass	$1.\ 672\ 621\ 637\ (83) \times 10^{-27}$	kg
m_p	proton mass	$938.\ 272\ 013\ (23)$	MeV/c^2
m_p	proton mass	$1.\ 007\ 276\ 466\ 77\ (10)$	u
m_p/m_e	proton-electron mass ratio	1836.152 672 47 (80)	1
N_A	avogadro's constant	6.02×10^{23}	mol^{-1}
hc		1.9864×10^{-25}	m · J
hc		1242	nm · eV
$\overline{h}c$		197	nm · eV

Table 1.2: Frequently used physical unit conversion

Unit	New Unit
1 eV	1.60218×10^{-19} J
1 J	6.25×10^{18} eV
1 u	931.5 MeV/c^2
1 u	1.66×10^{-27} kg
8 Å	1.66×10^{-27} kg

Chapter 2 Basic Physics of Semiconductors

One cannot design a high-performance analog circuits without a detailed knowledge of the analog devices and their limitations. However, we do face a dilemma. Our treatment of device physics must contain enough depth to provide adequate understanding, but must also be sufficiently brief to allow quick entry into circuits. This chapter accomplishes this task.

In this chapter, we begin with the concept of semiconductors and study the movement of charge (i.e., the flow of current) in them. Then, we deal with the "pn junction," which also serves as diode, and formulate its behavior.

2.1 Semiconductor Materials

The intrinsic concentration n_i (the number of electrons per unit volume in intrinsic silicon) is given by:

$$n_i = A \cdot T^{\frac{3}{2}} \exp \frac{-E_{g0}}{2kT} \quad (\text{electrons}/\text{cm}^3) \tag{2.1}$$

where:

(1) A is a constant of $5.2 \times 10^{15}\ \text{cm}^{-3}\text{K}^{-\frac{3}{2}}$ (Razavi) or $3.88 \times 10^{16}\ \text{cm}^{-3}\text{K}^{-\frac{3}{2}}$ (Feng) for silicon. For germanium (锗 Ge), $A = 1.76 \times 10^{16}\ \text{cm}^{-3}\text{K}^{-\frac{3}{2}}$ (Feng).

(2) $k = 1.38 \times 10^{-23}\ \text{J/K}$ is the Boltzmann constant.

(3) E_{g0} is the energy gap at $T = 0$ K. For silicon, $E_{g0} = 1.12$ eV (Razavi) or 1.21 eV (Feng); for germanium, $E_{g0} = 0.785$ eV (Feng). Note 1 eV $= 1.60218 \times 10^{-19}$ J.

yielding:

$$\text{Razavi: } n_i = \begin{cases} 1.08 \times 10^{10}\ \text{cm}^{-3}, & T = 300\ \text{K} \\ 1.54 \times 10^{15}\ \text{cm}^{-3}, & T = 600\ \text{K} \end{cases} \tag{2.2}$$

The free electron concentration n, hole concentration p and n-type doping density N_D satisfy the relation:

$$np = n_i^2, \quad n = N_D + p \tag{2.3}$$

The velocity of charge carrier is proportional to the electric field:

$$v = \mu E \ \ (v_e = -\mu_n E,\ v_h = \mu_p E) \tag{2.4}$$

where the mobility μ is given by $\mu_n = 1350\ \text{cm}^2 \cdot \text{s}^{-1} \cdot \text{V}^{-1}$ and $\mu_p = 480\ \text{cm}^2 \cdot \text{s}^{-1} \cdot \text{V}^{-1}$ for silicon at $T = 300$ K. Note that $\mu = \frac{\mu_0}{1+\frac{\mu_0 E}{v_{sat}}}$ is a function of E.

We can write the drift current density as:

$$J_n = n(-q_e)(-\mu_n E), \quad J_p = pq_h\mu_p E \tag{2.5}$$

$$\Longrightarrow J_{\text{drift}} = (\mu_n n + \mu_p p) q_e E \tag{2.6}$$

Equivalently, rewrite it as the electrical conductivity of the material:

$$\rho = \frac{E}{J} = \frac{1}{\sigma} \Longrightarrow \sigma = \frac{J}{E} = (\mu_n n + \mu_p p) q_e \tag{2.7}$$

Concentration gradient leads to diffusion current density:

$$J_n = (-q_e) D_n \left(-\frac{\mathrm{d}n}{\mathrm{d}x}\right) = q_e D_n \frac{\mathrm{d}n}{\mathrm{d}x} \tag{2.8}$$

$$J_p = (+q_e) D_p \left(-\frac{\mathrm{d}p}{\mathrm{d}x}\right) = -q_e D_p \frac{\mathrm{d}p}{\mathrm{d}x} \tag{2.9}$$

In intrinsic silicon at $T = 300$ K, $D_n = 34\ \text{cm}^2/\text{s}$ and $D_p = 12\ \text{cm}^2/\text{s}$.

2.2 pn Junction

2.2.1 pn Junction in Equilibrium

It can be proved that D and μ satisfy the Einstein relation:

$$\frac{D}{n} = \frac{kT}{q_e}\mu = V_T \tag{2.10}$$

we call V_T the thermal voltage, which is 26 mV at 300 K. The built-in potential V_B (or denoted as V_0) of a pn junction is given by:

$$V_B = V_T \ln \frac{N_A N_D}{n_i^2} \tag{2.11}$$

The typical value of V_B is between 0.5 V and 0.8 V. Since V_T and n_i varies with temperature, V_B decreases about 2.5 mV per 1 K increase in temperature.

As the depletion region in pn junction must be charge neutral, we have:

$$Q_- = (-q_e) S x_p N_A, \quad Q_+ = (+q_e) S x_n N_D \tag{2.12}$$

$$\Longrightarrow x_n N_D = x_p N_A \tag{2.13}$$

It can be proved that the width of the depletion region is:

$$l_0 = x_n + x_p = \sqrt{\frac{2\varepsilon}{q_e} \cdot \frac{N_A + N_D}{N_A N_D} \cdot V_B} = \frac{C_{j0} V_B}{q_e} \tag{2.14}$$

where $\varepsilon = \varepsilon_0 \varepsilon_r = 11.7\, \varepsilon_0$ is the permittivity of silicon.

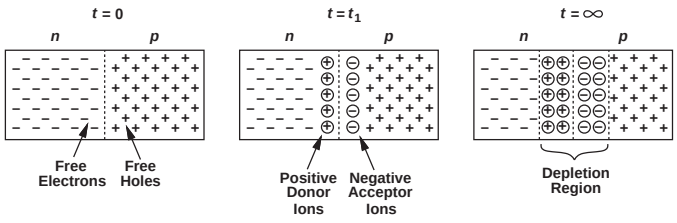


Figure 2.1: Evolution of the depletion region in a pn junction

2.2.2 pn Junction Under Reverse Bias

From eq (2.14), we can see the junction capacitance C_j is given by:

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{V_B}\right)^n} \tag{2.15}$$

$$C_{j0} = \sqrt{\frac{\varepsilon q_e}{2} \cdot \frac{N_A N_D}{N_A + N_D} \cdot \frac{1}{V_B}} \tag{2.16}$$

where n is the modified factor, which is typically $\frac{1}{2}$ for abrupt junctions, $\frac{1}{3}$ for linearly graded junctions and $\frac{1}{2} \sim 6$ to super-abrupt junctions.

A low-doping junction has a relatively high breakdown voltage (avalanche breakdown), while a high-doping junction has a relatively low breakdown voltage (Zener breakdown).

2.2.3 pn Junction Under Forward Bias

For every $V_T \ln 10 \approx 60$ mV increase in the forward voltage, I_D becomes ten times the original.

Note that the current-voltage characteristic is relatively sensitive to temperature, i.e., for every 1℃ increase in temperature, the curve shifts to the left by 2 mV $\sim$ 2.5 mV.

In some cases, the static characteristic of a diode needs to be modified for better accuracy:

$$I_D = I_S \left[\exp\left(\frac{V}{nV_T}\right) - 1\right] \tag{2.17}$$

where r_S is the parasitic resistance and n (typically $1 \sim 2$) is the correction factor.

2.2.4 Temperature Dependence

Table 2.1: Temperature Dependence of Junction Parameters

Parameter	temp coefficient
V_B	-
I_S	+
$V_{BR,\text{Zener}}$	-
$V_{BR,\text{Avalanche}}$	+

Chapter 3 Diode Models and Circuits

Chapter 4 Physics of Bipolar Transistors

In this chapter, we analyze the structure and operation of bipolar transistors, preparing ourselves for the study of circuits employing such devices.

we aim to understand the physics of the transistor, derive equations that represent its I/V characteristics, and develop an equivalent model that can be used in circuit analysis and design.

4.1 Structure of Bipolar Transistors

Note that all of the operation principles and equations described for npn transistors apply to pnp devices as well.

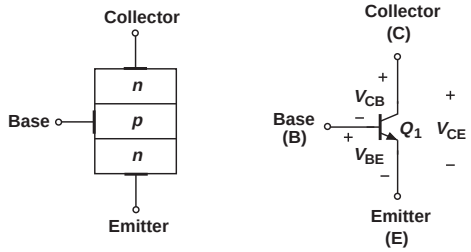


Figure 4.1: (a) Structure and (b) circuit symbol of a bipolar junction transistor (BJT)

In reality, the dimensions and doping levels of the emitter and the collector are quite different to achieve the desired characteristics. For transistors in active mode, i.e., $V_C > V_B > V_E$, we have:

$$I_C = I_S \left(\exp \frac{V_{BE}}{V_T} - 1\right)\left(1 + \frac{V_{CE}}{V_A}\right) \tag{4.1}$$

$$\approx I_S \exp \frac{V_{BE}}{V_T} \quad (V_{BE} > 5V_T = 130\ \text{mV}) \tag{4.2}$$

where:

(1) $I_S = \frac{A_E q_e D_n n_i^2}{N_B W_B}$;
(2) A_E: emitter cross-sectional area;
(3) q_e: electron charge;
(4) D_n: electron diffusion coefficient (34 cm^2/s for D_n, 12 cm^2/s for D_p);
(5) N_B: base doping level;
(6) W_B: base width;

Due to the exponential dependence of I_C on V_{BE}, for every 60 mV ($V_T \ln 10$ at $T = 300$ K) increase in V_{BE}, I_C increases by a factor of 10.

In practice, the BE voltage of Integrated devices $V_{BE,int}$ is 100 mV $\sim$ 150 mV greater than that of discrete devices $V_{BE,dis}$, due to the diffferent base width and other parameters (otherwise it should be about 380mV).

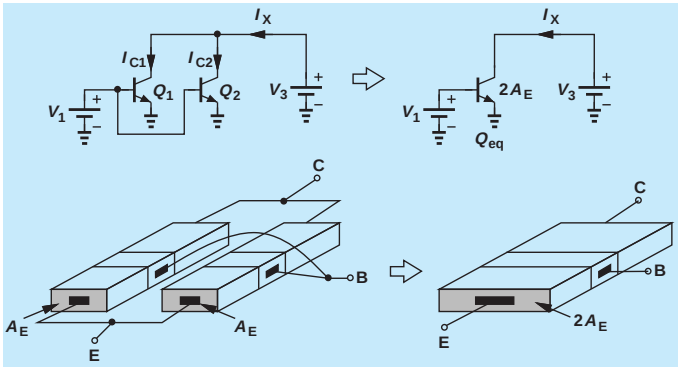


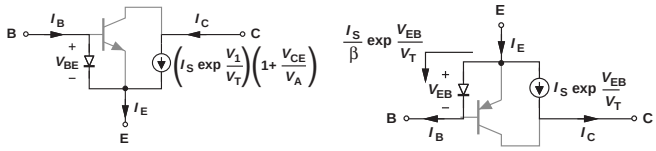
Figure 4.2: Two parallel transistors and the equivalence to a single transistor having twice area

4.2 Bipolar Transistor Models

For a bipolar transistor in active mode, we have the large-signal model:

$$I_C = I_S \exp \frac{V_{BE}}{V_T}\left(1 + \frac{V_{CE}}{V_A}\right) \approx I_S \exp \frac{V_{BE}}{V_T} \tag{4.3}$$

$$I_B = \frac{I_C}{\beta}, \quad I_E = I_C + I_E = \frac{\beta + 1}{\beta} I_C = \alpha I_C \tag{4.4}$$



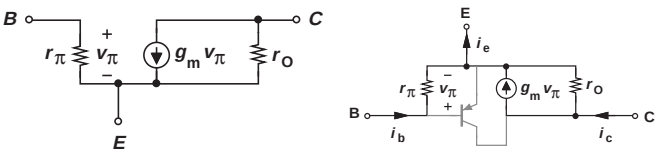
(a) npn **(b) pnp**

Figure 4.3: Large-signal

And the small-signal model is:

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_T}, \quad r_\pi = \frac{\partial V_{BE}}{\partial I_B} = \frac{\beta}{g_m} \tag{4.5}$$

$$r_O = \frac{\partial V_{CE}}{\partial I_C} = \frac{V_A + V_{CE}}{I_C} \approx \frac{V_A}{I_C} \tag{4.6}$$



(a) npn **(b) pnp**

Figure 4.4: Small-signal

4.3 Bipolar Transistor in Saturation

The term “saturation” is used because increasing the base current in this region of operation leads to little change in the collector current.

Heavy saturation leads to a sharp rise in the base current and hence a rapid fall in β. In addition to a drop in β, the speed of bipolar transistors also degrades in saturation.

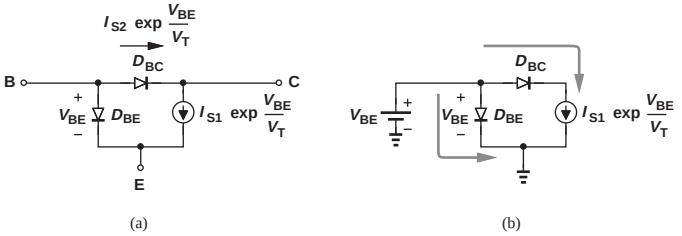


Figure 4.5: BJT in (a) saturation region and (b) with collector open

As a rule of thumb, we permit soft saturation with $V_{BC} < 400$ mV because the current in the B-C junction is negligible.

Chapter 5 Bipolar Amplifiers

With the physics and operation of bipolar transistors described in Chapter 4, we now deal with amplifier circuits employing such devices. There is an extremely wide usage of amplification in microelectronics, motivating us to master the analysis and design of such building blocks.

5.1 BJT's Terminal Impedances

When determining the transfer of signals from one stage to the next, the I/O impedances are usually regarded as small-signal quantities, with the tacit assumption that the signal levels are indeed small.

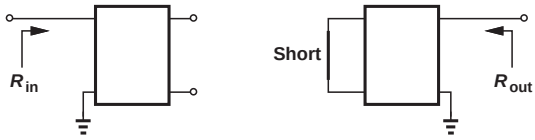


Figure 5.1: Impedance seen at a node

We summarize the small-signal impedances of the BJT in Table 5.1. Remark that the impedance here denotes to the small-signal impedance, while we use an upper case here.

5.2 Biasing Techniques

5.2.1 Simple Biasing

The biasing scheme above is simple, but suffering from the low stability and accuracy.

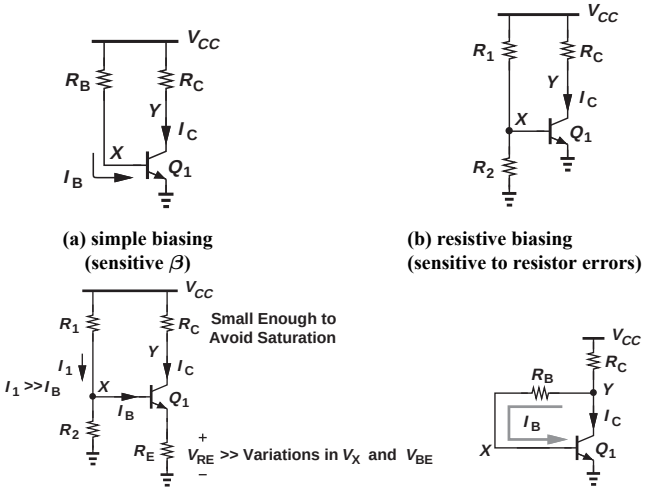


Figure 5.2: Basic biasing techniques

First, the uncertainty of V_{BE} becomes significant because the bias is sensitive to V_{BE} variations. Second, I_C heavily depends on β, a parameter that may change considerably with temperature and transistor mismatch. For these reasons, the topology is rarely used in practice.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, \quad I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B} \tag{5.1}$$

$$V_{CE} = V_{CC} - \beta \frac{V_{CC} - V_{BE}}{R_B} R_C \tag{5.2}$$

5.2.2 Resistive Divider Biasing

As shown in Figure 5.2 (b), the resistive divider biasing constructs a relatively stable base bias current.

$$R_{Thev} = R_1 \parallel R_2, \quad V_{Thev} = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{5.3}$$

$$V_{BE} = V_{Thev} - I_B R_{Thev} \tag{5.4}$$

However, this circuit is significantly sensitive to the resistor values. A 1% error in R_2 introduces a 31% $\sim$ 36% error (typ.) in the collector current (and base current), making it hard to define the operation point. The circuit is therefore still of little practical value.

5.2.3 Biasing with Emitter Degeneration

In the circuit shown in Figure 5.2 (c), a relatively large variation in V_X causes negligible change in V_{BE}, hence the collector current becomes more stable.

For example, a 1% error in R_2 introduces only 4% $\sim$ 8% error (typ.) in the collector current, which is a significant improvement over the preceding circuits.

$$I_C \approx I_E = \frac{V_P}{R_E} = \frac{V_X - V_{BE}}{R_E} \tag{5.5}$$

$$\Delta I_C = \frac{\Delta V_X}{R_E} - \frac{\Delta V_{BE}}{R_E} \tag{5.6}$$

In this circuit, two rules are typically followed:

(1) $I_1 \gg I_B$ to lower the sensitivity to β, or use the Thevenin equivalent to gain a more precise bias current.

(2) V_{RE} must be large enough (100 mV to several hundred mV) to suppress the effect of uncertainties in V_X and V_{BE} due to resistance mismatch.

5.2.4 Self-Biasing

Another frequently used biasing technique is the self-biasing circuit, as shown in Figure 5.2 (d).

The most important property is that it guarantees Q_1 to operate in active mode (because $V_C \geqslant V_B$), regardless of the device and circuit parameters.

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta}}, \quad I_B = \frac{I_C}{\beta} \tag{5.7}$$

In this stage, $V_{CC} - V_{BE}$ must be much greater than ΔV_{BE} to stabilize the bias point, and R_C must be much greater than $\frac{R_B}{\beta}$ ($R_C > 10\frac{R_B}{\beta}$) to lower the sensitivity to β.

Table 5.1: BJT's small-signal terminal resistances

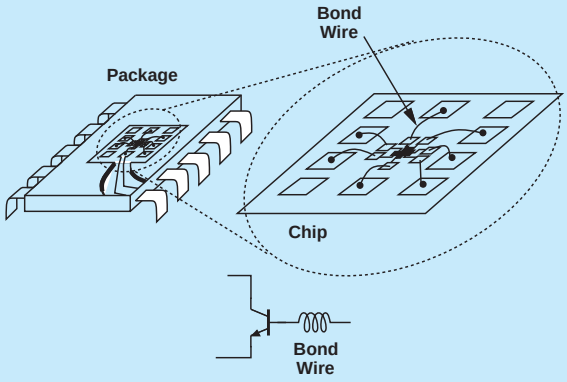
Collector Resistance	Base Resistance	Emitter Resistance
$R_{coll} = r_O \cdot \left[1 + \left(\frac{\beta}{r_\pi + R_B} + \frac{1}{r_O}\right) \cdot (R_E \parallel (r_\pi + R_B))\right]$	$R_{base} = r_\pi + R_E \cdot \frac{\beta r_O + (r_O + R_C)}{R_E + (r_O + R_C)}$	$R_{emit} = \left(1 + \frac{R_C}{r_O}\right) \cdot \left(\frac{r_\pi + R_B}{1 + \frac{R_C}{r_O}} \parallel \frac{r_\pi + R_B}{\beta} \parallel r_O\right)$
$R_{coll}\vert_{R_B=0} = r_O \cdot \left[1 + \left(\frac{\beta}{r_\pi} + \frac{1}{r_O}\right) \cdot (R_E \parallel r_\pi)\right]$	$R_{base}\vert_{R_C=0} = r_\pi + (\beta + 1)(R_E \parallel r_O)$	$R_{emit}\vert_{R_C=0} = \frac{r_\pi + R_B}{\beta + 1} \parallel r_O$
$R_{coll}\vert_{R_E=0} = r_O$	$R_{base}\vert_{R_E=0} = r_\pi$	$R_{emit}\vert_{R_B=0} = \left(1 + \frac{R_C}{r_O}\right) \cdot \left(\frac{r_\pi}{\beta + 1 + \frac{R_C}{r_O}} \parallel r_O\right)$
$R_{coll}\vert_{r_O \to \infty} = \infty$	$R_{base}\vert_{r_O \to \infty} = r_\pi + (\beta + 1)R_E$	$R_{emit}\vert_{r_O \to \infty} = \frac{r_\pi + R_B}{\beta + 1}$

Table 5.2: Three basic types of BJT amplifiers

Parameter	CE (Common Emitter)	CC (Common Collector, EF)	CB (Common Base)
R_{out}	$R_C \parallel R_{coll}$	$R_E \parallel R_{emit}$	$R_C \parallel R_{coll}$
G_m	$\frac{\beta}{r_\pi + R_B} \cdot \frac{1}{R_E} \cdot \left(R_E \parallel \frac{r_\pi + R_B}{\beta + 1} \parallel r_O\right)$	$\frac{-g_m}{\left(1 + \frac{R_B}{r_\pi}\right)\left(1 + \frac{R_C}{r_O}\right)}$	$\frac{-1}{R_E + \frac{r_\pi + R_B}{\beta + 1} \parallel r_O}$
$G_m\vert$	$G_m\vert_{R_E=0} = \frac{\beta}{r_\pi + R_B}$	$G_m\vert_{R_C=0} = \frac{-\beta}{r_\pi + R_B}$	$G_m\vert_{R_E=0} = -\left(\frac{\beta + 1}{r_\pi + R_B} + \frac{1}{r_O}\right)$
$G_m\vert$	$G_m\vert_{R_B=0} = g_m \cdot \frac{R_E \parallel \frac{r_\pi}{\beta + 1} \parallel r_O}{R_E}$	$G_m\vert_{R_B=0} = \frac{-g_m}{1 + \frac{R_C}{r_O}}$	$G_m\vert_{R_B=0} = \frac{-1}{R_E + \frac{r_\pi}{\beta + 1}} \parallel r_O$
$R_{out}\vert_{r_O \to \infty}$	R_C	$R_E \parallel \frac{r_\pi + R_B}{\beta + 1}$	R_C
$G_m\vert_{r_O \to \infty}$	$\frac{\beta}{(\beta+1)R_E + r_\pi + R_B} \approx \frac{1}{R_E + \frac{1}{g_m} + \frac{R_B}{\beta+1}}$	$\frac{-\beta}{r_\pi + R_B}$	$\frac{-(\beta+1)}{(\beta+1)R_E + r_\pi + R_B} \approx \frac{-1}{R_E + \frac{1}{g_m} + \frac{R_B}{\beta+1}}$
$A_v\vert_{r_O \to \infty}$	$\frac{-\beta R_C}{(\beta+1)R_E + r_\pi + R_B} \approx \frac{-R_C}{R_E + \frac{1}{g_m} + \frac{R_B}{\beta+1}}$	$\frac{\beta R_E}{(\beta+1)R_E + r_\pi + R_B} \approx \frac{1}{1 + \frac{r_\pi + R_B}{\beta R_E}}$	$\frac{-(\beta+1)R_C}{(\beta+1)R_E + r_\pi + R_B} \approx \frac{-R_C}{R_E + \frac{1}{g_m} + \frac{R_B}{\beta+1}}$

Did you know?

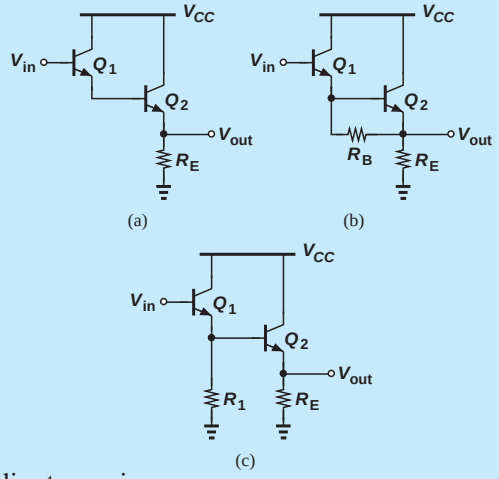
The CB gain reduction as a result of an impedance in series with the base has stumbled many a designer. This effect is especially pronounced at high frequencies because the parasitic inductances of the package (which contains the chip) may introduce a significant impedance ($= L\omega$). As shown below, the "bond wires" connecting the chip to the package behave like inductors, thus degrading the performance. For example, a 5-mm bond wire has an inductance of about 5 nH, exhibiting an impedance of 157 Ω at 5 GHz.



Effect of bond wire inductance in a CB stage.

Did you know?

Shortly after the invention of the bipolar transistor, a Bell Labs engineer named Sidney Darlington borrowed a few transistors from his boss and took them home for the weekend. It was over that weekend that he came up with what is known as the "Darlington Pair" [Fig. (a)]. Here, Q_1 and Q_2 can be viewed as two emitter followers in a cascade. The circuit provides a high input impedance but since I_{C1} is small ($= I_{B2}$), Q_1 is quite slow. For this reason, the modified topologies in Figs. (b) and (c) are preferred.



Darlington pairs.

5.2.5 Biasing Design Procedure

It is possible to prescribe a design procedure for the resistive divider biasing with emitter degeneration, which serves most applications.

(1) Calculate I_C by the required small-signal quantities such as g_m and r_π;
(2) Get g$V_{BE} = V_T \ln \frac{I_C}{I_S}$ and $I_B = \frac{I_C}{\beta}$, or from the datasheet;
(3) Choose $V_{RE} \gg \Delta V_X$, hence $R_E = \frac{V_{RE}}{I_C}$;
(4) Calculate $V_X = V_{BE} + V_{RE}$, R_1 and R_2, ensuring that $I_1 \gg I_B$ (or use the Thevenin equivalent to gain a more precise result);
(5) Determine R_C as large as possible to obtain a high gain, but not too large to avoid saturation.

5.3 Bipolar Amplifier Topologies

The common parameters of the three basic types of BJT amplifiers are summarized in Table 5.2.

From the CE and CB stages, we know that $|A_v| \approx g_m R_C$, limited by the supply voltage (and the minimum $V_{CE,\text{min}} = V_{BE}$):

$$|A_v| \approx \frac{I_C R_C}{V_T} = \frac{V_{R_C}}{V_T} < \frac{V_{CC} - V_{BE}}{V_T} \tag{5.8}$$

For example, if $V_{CC} - V_{BE} = 1$ V, then $|A_v| < 38.5 \approx 40$.

The intrinsic gain of the BJT is defined as:

$$A_{int} = g_m r_O = \frac{\frac{I_C}{V_T}}{\frac{V_A + V_{CE}}{I_C}} \approx \frac{V_A}{V_T} \tag{5.9}$$

In modern integrated BJT, V_A falls in the vicinity of 5 V ($A_{int} = 200$), and A_{int} falls to about 50 because of a series of second-order effects.

5.4 Bipolar Amplifier with Biasing and Coupling Circuit

When adding the input to the amplifier, we usually use a coupling capacitor, isolating the bias condition and injecting the ac signal. In this case, we say the stage is "ac-coupled" or "capacitively coupled" (but op amp is usually dc-coupled).

The value of capacitor is chosen so that it provides a relatively low impedance (almost a short circuit) for the frequencies of interest.

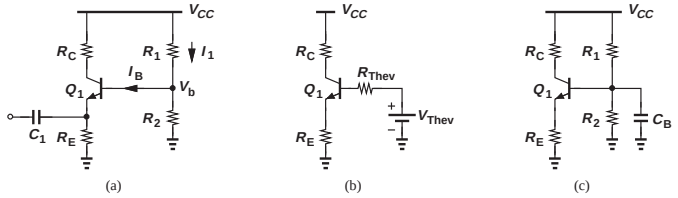


Figure 5.3: (a) CB stage with base bias network, (b) use of Thevenin equivalent, (c) effect of bypass capacitor.

Chapter 6 Physics of MOS Transistors

> See Razavi CMOS for more details.

Chapter 7 CMOS Amplifiers

> See Razavi CMOS for more details.

Table 7.1: Three basic types of CMOS amplifiers

Parameter	CS (Common Source)	CD (SF, Source Follower)	CG (Common Gate)
R_{out}	$R_D \parallel R_{drain}$	$R_S \parallel R_{source}$	$R_D \parallel R_{drain}$
G_m	$g_m \cdot \frac{r_O}{R_{drain}} = g_m \cdot \frac{1}{1+\frac{R_S}{R_{S0}}}$	$\frac{-g_m}{1+\frac{R_D}{r_O}}$	$\frac{-1}{R_S+R_{S0}}$
$R_{out}\|_{r_O\to\infty}$	R_D	$R_S \parallel \frac{1}{g_m}$	R_D
$G_m\|_{r_O\to\infty}$	$\frac{g_m}{1+g_m R_S}$	$-g_m$	$\frac{-1}{R_S+\frac{1}{g_m}} = \frac{-g_m}{1+g_m R_S}$
$A_v\|_{r_O\to\infty}$	$\frac{-R_D}{\frac{1}{g_m}+R_S}$	$\frac{g_m R_S}{g_m R_S+1}$	$\frac{R_D}{\frac{1}{g_m}+R_S}$

Table 7.2: Three basic types of CMOS amplifiers

Parameter	CS (Common Source)	CD (SF, Source Follower)	CG (Common Gate)
R_{out}	$R_D \parallel R_{drain}$	$R_S \parallel R_{source}$	$R_D \parallel R_{drain}$
G_m	$g_m \cdot \frac{r_O}{R_{drain}} = g_m \cdot \frac{1}{1+\frac{R_S}{R_{S0}}}$	$\frac{-g_m}{1+\frac{R_D}{r_O}}$	$\frac{-1}{R_S+R_{S0}}$
$R_{out}\|_{r_O\to\infty}$	R_D	$R_S \parallel \frac{1}{g_m}$	R_D
$G_m\|_{r_O\to\infty}$	$\frac{g_m}{1+g_m R_S}$	$-g_m$	$\frac{-1}{R_S+\frac{1}{g_m}} = \frac{-g_m}{1+g_m R_S}$
$A_v\|_{r_O\to\infty}$	$\frac{-R_D}{\frac{1}{g_m}+R_S}$	$\frac{g_m R_S}{g_m R_S+1}$	$\frac{R_D}{\frac{1}{g_m}+R_S}$

Chapter 8 Operation Amplifier as a Black Box

> To be completed.

Chapter 9 Cascode Stages and Current Mirrors

> The "cascode" stage is a modified version of common-emitter or common-source topologies and proves useful in high-performance circuit design, and the "current mirror" is an interesting and versatile technique employed extensively in integrated circuits.

9.1 Cascode Stage

9.1.1 Cascode as a Current Source

We have already noticed that emitter (or source) degeneration boosts the small-signal impedance seen at the collector (or drain). For the circuits shown in Figure 9.1, we have:

$$\begin{aligned} R_{out1} &= r_O + (1+g_m r_O)(R_E \parallel r_\pi) &&\approx g_m r_O (R_E \parallel r_\pi) \\ R_{out2} &= r_O + (1+g_m r_O) R_S &&\approx g_m r_O R_S \end{aligned}$$

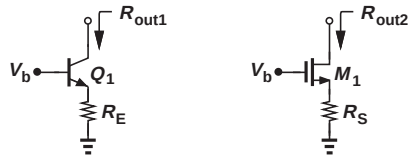


Figure 9.1: Output impedance of degenerated transistors

The cascode[①] stage, i.e., replacing the degeneration resistance with a biased transistor in Figure 9.1, exhibits a small-signal impedance of:

$$R_{out,BJT} \approx g_{m1} r_{O1} (r_{O2} \parallel r_{\pi 1}) \tag{9.1}$$

$$R_{out,MOS} \approx g_{m1} r_{O1} r_{O2} \tag{9.2}$$

It is interesting to note that the maximum R_{out} provided by a bipolar cascode is $R_{out,max} \approx g_{m1} r_{O1} r_{\pi 1} = \beta_1 r_{O1}$.

(a) bipolar cascode **(b) MOSFET cascode**

Figure 9.2: Cascode current source

9.1.2 Cascode as an Amplifier

The high voltage gain of the cascode topology shown in Figure **??** makes it attractive for many applications. In Figure **??** (b), the overall voltage gain is given by:

$$R_{out} = R_{out,p} \parallel R_{out,n}, \tag{9.3}$$

$$R_{out,p} \approx g_{m3} r_{O3} (r_{\pi 3} \parallel r_{O4}) \tag{9.4}$$

$$R_{out,n} \approx g_{m2} r_{O2} (r_{\pi 2} \parallel r_{O1}) \tag{9.5}$$

[①] The term "cascode" is believed to be an abbreviation of "cascaded triodes".

Acting as a pure resistance, Q_2 does not affect the transconductance since its base and collector are tied to ac-ground (in G_m calculation). Therefore, we still have:

$$G_m = g_m, \quad A_v = -g_m (R_{out,p} \parallel R_{out,n}) \tag{9.6}$$

However, the biasing circuit of cascode amplifier can be quite complex, limiting its applications in reality.

9.2 Current Mirrors

Chapter 10 Differential Amplifiers

This chapter describes bipolar and MOS differential amplifiers and formulates their large-signal and small-signal properties.

10.1 The Five-Transistor OTA

10.1.1 Large-Signal Analysis

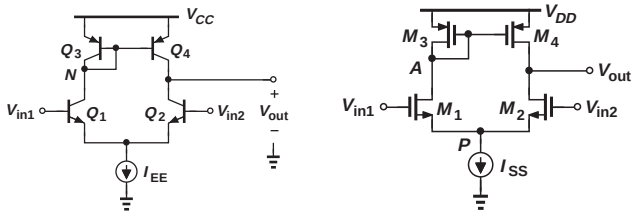
Different from differential amplifiers, though $V_{in,CM}$ has negligible effect on small-signal gain for the five-transistor OTA, it does affect the output swing. Concretely speaking, the input and output range is limited by:

$$V_{out} \in [V_{in,CM} + V_{TH},\ \ V_{DD}] \tag{10.1}$$

$$V_{in,CM} < V_{OV}(I_{SS}) + V_{GS}(\frac{1}{2}I_{SS}) \tag{10.2}$$

$$V_{in,CM} > V_{DD} - V_{OV}(\frac{1}{2}I_{SS}) \tag{10.3}$$

where $V_{OV} = V_{OV}(I_{SS})$ denotes the overdrive voltage at $I_D = I_{SS}$.



(a) using BJT (b) using MOSFET

Figure 10.1: Differential pair with active load

10.1.2 Small-Signal Analysis

Below is the small-signal equivalent for the five-transistor OTA (ignoring R_{SS}):

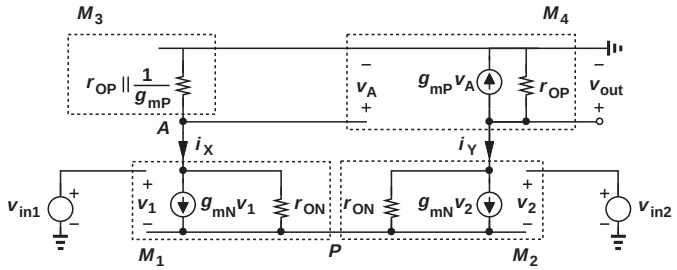


Figure 10.2: Small-signal equivalent for MOS OTA

For a MOS OTA, assuming $g_{mP}r_{OP},\ g_{mN}r_{ON} \gg 1$ and $R_{SS} \gg \frac{1}{g_{mN}}$, it can be proved that[①]:

$$R_{out} \approx r_{ON} \parallel r_{OP} \tag{10.4}$$

$$A_{DM} \approx g_{mN}\,(r_{ON} \parallel r_{OP}) \tag{10.5}$$

$$A_{CM} \approx \frac{-g_{mN}r_{ON}}{2A_{DM} \cdot g_{mP}R_{SS}} \tag{10.6}$$

$$\text{CMRR} \approx 2A_{DM}^2 \cdot \frac{g_{mP}R_{SS}}{g_{mN}r_{ON}} < 2A_{DM}\,(g_{mP}R_{SS}) \tag{10.7}$$

[①] see YiDingg's Website > Blogs > The Five-Transistor OTA (https://yidingg.github.io/YiDingg/#/Blogs/Electronics/The%20Five-Transistor%20OTA)

Chapter 11 Frequency Response

> To be completed.

Chapter 12 Feedback

> To be completed.

Chapter 13 Oscillators

> To be completed.

Chapter 14 Output Stages and Power Amplifiers

This chapter deals with circuits that can provide a high output power. We first reexamine circuits studied in previous chapters to understand their shortcomings for this task. Next, we introduce the "push-pull" stage and various modifications to improve its performance.

14.1 Emitter follower as power amp

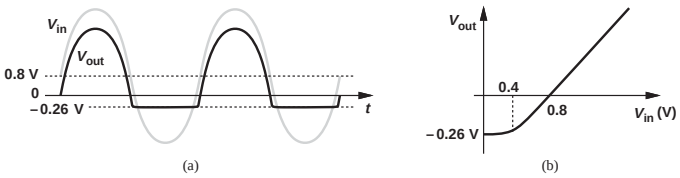


Figure 14.1: Emitter follower as power amplifier

14.2 Push-Pull Stage

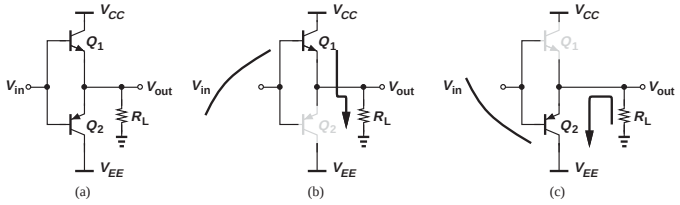
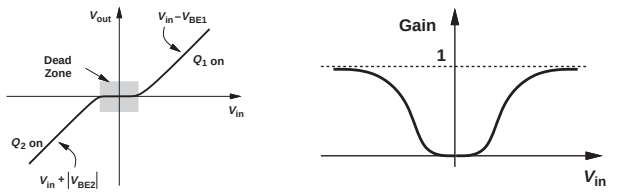


Figure 14.2: Basic push-pull stage



(a) The dead zone of basic push-pull **(b) Voltage gain of basic push-pull**

Figure 14.3: Basic push-pull stage characteristics

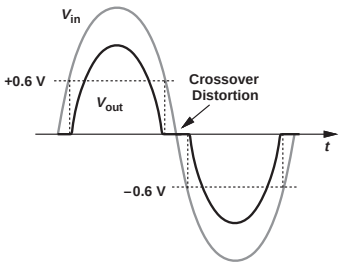


Figure 14.4: Input-output waveform of push-pull stage

14.3 Improved Push-Pull Stage

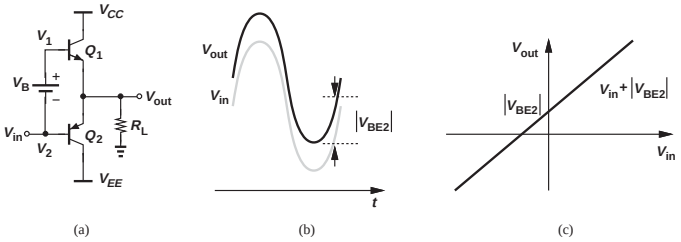


Figure 14.5: Improved push-pull stage

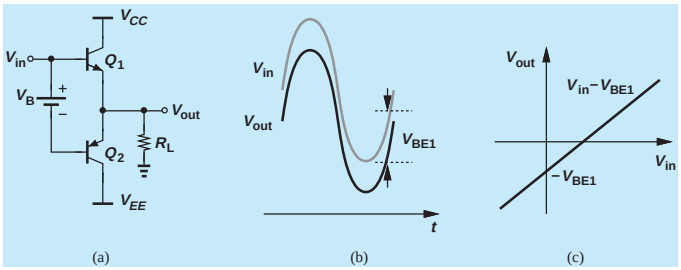


Figure 14.6: Improved push-pull stage with Q_1 input

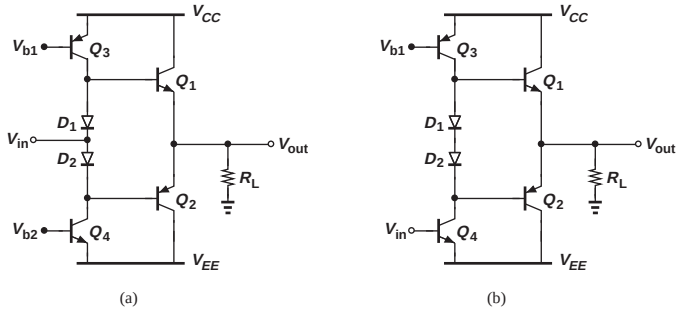


Figure 14.7: Addition of CE stage for push-pull stage

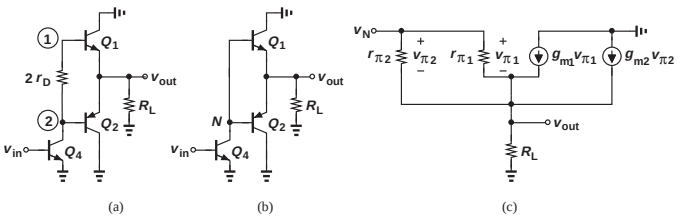


Figure 14.8: Overall voltage gain of improved push-pull stage

14.3.1 Small-Signal Analysis

Note that Q_1 and Q_2 are connected in parallel, because their collectors are tied to ac-ground and the emitters are tied together (if r_{D1} and r_{D2} is sufficiently small).

Therefore, in small-signal analysis, we can combine Q_1 and Q_2 as a single transistor $Q_1 + Q_2$ with the following

parameters:

$$g_m = g_{m1} + g_{m2}, \quad r_\pi = r_{\pi1} \parallel r_{\pi2}, \quad r_o = r_{O1} \parallel r_{O2}$$
$$\beta = g_m r_\pi = (g_{m1} + g_{m2})\,(r_{\pi1} \parallel r_{\pi2})$$

yielding the voltage gain and output impedance[①]:

$$A_1 = -g_{m4}\,(r_{O3} \parallel r_{O4}) \tag{14.1}$$
$$A_2 = \frac{\beta r_O}{(\beta+1)r_O + r_\pi + R_B} \tag{14.2}$$
$$A_v \approx -g_{m4}\,(r_{O3} \parallel r_{O4}) \tag{14.3}$$
$$R_{out} \approx \frac{1}{g_{m1}+g_{m2}} + \frac{r_{O3} \parallel r_{O4}}{(g_{m1}+g_{m2})\,(r_{\pi1} \parallel r_{\pi2})} \tag{14.4}$$

14.3.2 Large-Signal Analysis

It is obvious that the push-pull stage operates in a large-signal mode so that the small-signal analysis is of limited value, meriting an analysis of the large-signal behavior.

14.3.3 Power Dissipation and Efficiency

We only consider the approximate power dissipation and efficiency of the improved push-pull stage, and they are given by:

$$P_{Q,av} = P_{S,av} - P_{O,av} \tag{14.5}$$
$$P_{S,av} = \frac{2V_P V_{CC}}{\pi R_L}, \quad P_{O,av} = \frac{V_P^2}{2R_L} \tag{14.6}$$
$$\eta = \frac{P_{O,av}}{P_{S,av}} = \frac{\pi V_P}{4\,V_{CC}} < \frac{\pi}{4} \approx 78.5\,\% \quad (V_P \approx V_{CC}) \tag{14.7}$$
$$P_{Q,peak} = \frac{V_{CC}^2}{\pi^2 R_L} \quad \left(V_P = \frac{2}{\pi}V_{CC} \approx V_{CC} \times 64\,\%\right) \tag{14.8}$$

[①] See Yi Ding's Website > Blogs > Electronics > Improved Push-Pull Stage (https://yidingg.github.io/YiDingg/#/Blogs/Electronics/Improved%20Push-Pull%20Stage)

Chapter 15 Analog Filters

> To be completed.

Chapter 16 Digital CMOS Circuits

> To be completed.