Notes for *Fundamentals of Microelectronics (Razavi) (2nd edition, 2014)*

《微电子基础》笔记

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Preface

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序言

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Chapter 1 Introduction to Microelectronics

Table 1.1: Frequently used physical constant

Symbol	Note	Value	Unit
k	Boltzmann constant	1.38×10^{-23}	J
c	velocity of light	2.9979×10^{8}	m/s
h	velocity of light	$6.\ 626\ 070\ 15 \times 10^{-34}$	J · s
R	universal gas constant	8.31	J / (mol · K)
ε_0	permittivity of vacuum	8.85×10^{-14}	F/cm
e	electron charge	$1.\ 602 \times 10^{-19}$	C
m_e	electronic mass	$9.\ 109\ 382\ 15\ (45) \times 10^{-31}$	kg
m_e	electronic mass	0. 510 998 910 (13)	MeV/c^2
m_p	proton mass	$1.\ 672\ 621\ 637\ (83) \times 10^{-27}$	kg
m_p	proton mass	938. 272 013 (23)	MeV/c^2
m_p	proton mass	1. 007 276 466 77 (10)	u
m_p/m_e	proton-electron mass ratio	1836.152 672 47 (80)	1
N_A	avogadro's constant	6.02×10^{23}	mol^{-1}
hc		1.9864×10^{-25}	m · J
hc		1242	nm · eV
$\hbar c$		197	nm · eV

Table 1.2: Frequently used physical unit conversion

Unit	New Unit
1 eV	1.60218×10^{-19} J
1 J	6.25×10^{18} eV
1 u	931.5 MeV/c^2
1 u	1.66×10^{-27} kg
8 Å	1.66×10^{-27} kg

Chapter 2 Basic Physics of Semiconductors

One cannot design a high-performance analog circuits without a detailed knowledge of the analog devices and their limitations. However, we do face a dilemma. Our treatment of device physics must contain enough depth to provide adequate understanding, but must also be sufficiently brief to allow quick entry into circuits. This chapter accomplishes this task.

In this chapter, we begin with the concept of semiconductors and study the movement of charge (i.e., the flow of current) in them. Then, we deal with the "pn junction," which also serves as diode, and formulate its behavior.

2.1 Semiconductor Materials

The intrinsic concentration n_i (the number of electrons per unit volume in intrinsic silicon) is given by:

$$n_i = A \cdot T^{\frac{3}{2}} \exp \frac{-E_{g0}}{2kT} \quad (\text{electrons}/\text{cm}^3) \tag{2.1}$$

where:

(1) A is a constant of $5.2 \times 10^{15}\ \text{cm}^{-3}\text{K}^{-\frac{3}{2}}$ (Razavi) or $3.88 \times 10^{16}\ \text{cm}^{-3}\text{K}^{-\frac{3}{2}}$ (Feng) for silicon. For germanium (锗 Ge), $A = 1.76 \times 10^{16}\ \text{cm}^{-3}\text{K}^{-\frac{3}{2}}$ (Feng).

(2) $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant.

(3) E_{g0} is the energy gap at $T = 0$ K. For silicon, $E_{g0} = 1.12$ eV (Razavi) or 1.21 eV (Feng); for germanium, $E_{g0} = 0.785$ eV (Feng). Note 1 eV $= 1.60218 \times 10^{-19}$ J.

yielding:

$$\text{Razavi: } n_i = \begin{cases} 1.08 \times 10^{10}\ \text{cm}^{-3}, & T = 300\ \text{K} \\ 1.54 \times 10^{15}\ \text{cm}^{-3}, & T = 600\ \text{K} \end{cases} \tag{2.2}$$

The free electron concentration n, hole concentration p and n-type doping density N_D satisfy the relation:

$$np = n_i^2, \quad n = N_D + p \tag{2.3}$$

The velocity of charge carrier is proportional to the electric field:

$$v = \mu E \ \ (v_e = -\mu_n E,\ v_h = \mu_p E) \tag{2.4}$$

where the mobility μ is given by $\mu_n = 1350\ \text{cm}^2 \cdot \text{s}^{-1} \cdot \text{V}^{-1}$ and $\mu_p = 480\ \text{cm}^2 \cdot \text{s}^{-1} \cdot \text{V}^{-1}$ for silicon at $T = 300$ K. Note that $\mu = \frac{\mu_0}{1+\frac{\mu_0 E}{v_{sat}}}$ is a function of E.

We can write the drift current density as:

$$J_n = n(-q_e)(-\mu_n E), \quad J_p = pq_h\mu_p E \tag{2.5}$$
$$\Longrightarrow J_{\text{drift}} = (\mu_n n + \mu_p p) q_e E \tag{2.6}$$

Equivalently, rewrite it as the electrical conductivity of the material:

$$\rho = \frac{E}{J} = \frac{1}{\sigma} \Longrightarrow \sigma = \frac{J}{E} = (\mu_n n + \mu_p p) q_e \tag{2.7}$$

Concentration gradient leads to diffusion current density:

$$J_n = (-q_e) D_n \left(-\frac{\mathrm{d}n}{\mathrm{d}x}\right) = q_e D_n \frac{\mathrm{d}n}{\mathrm{d}x} \tag{2.8}$$
$$J_p = (+q_e) D_p \left(-\frac{\mathrm{d}p}{\mathrm{d}x}\right) = -q_e D_p \frac{\mathrm{d}p}{\mathrm{d}x} \tag{2.9}$$

In intrinsic silicon at $T = 300$ K, $D_n = 34\ \text{cm}^2/\text{s}$ and $D_p = 12\ \text{cm}^2/\text{s}$.

2.2 pn Junction

2.2.1 pn Junction in Equilibrium

It can be proved that D and μ satisfy the Einstein relation:

$$\frac{D}{n} = \frac{kT}{q_e}\mu = V_T \tag{2.10}$$

we call V_T the thermal voltage, which is 26 mV at 300 K. The built-in potential V_B (or denoted as V_0) of a pn junction is given by:

$$V_B = V_T \ln \frac{N_A N_D}{n_i^2} \tag{2.11}$$

The typical value of V_B is between 0.5 V and 0.8 V. Since V_T and n_i varies with temperature, V_B decreases about 2.5 mV per 1 K increase in temperature.

As the depletion region in pn junction must be charge neutral, we have:

$$Q_- = (-q_e) S x_p N_A, \quad Q_+ = (+q_e) S x_n N_D \tag{2.12}$$
$$\Longrightarrow x_n N_D = x_p N_A \tag{2.13}$$

It can be proved that the width of the depletion region is:

$$l_0 = x_n + x_p = \sqrt{\frac{2\varepsilon}{q_e} \cdot \frac{N_A + N_D}{N_A N_D} \cdot V_B} = \frac{C_{j0} V_B}{q_e} \tag{2.14}$$

where $\varepsilon = \varepsilon_0 \varepsilon_r = 11.7\,\varepsilon_0$ is the permittivity of silicon.

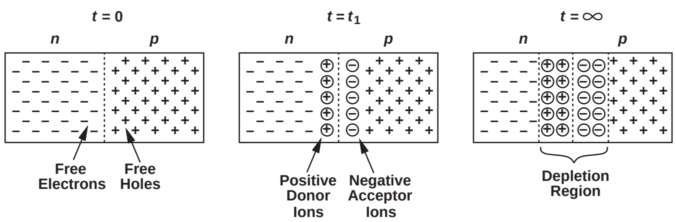

Figure 2.1: Evolution of the depletion region in a pn junction

2.2.2 pn Junction Under Reverse Bias

From eq (2.14), we can see the junction capacitance C_j is given by:

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{V_B}\right)^n} \tag{2.15}$$

$$C_{j0} = \sqrt{\frac{\varepsilon q_e}{2} \cdot \frac{N_A N_D}{N_A + N_D} \cdot \frac{1}{V_B}} \tag{2.16}$$

where n is the modified factor, which is typically $\frac{1}{2}$ for abrupt junctions, $\frac{1}{3}$ for linearly graded junctions and $\frac{1}{2} \sim 6$ to super-abrupt junctions.

A low-doping junction has a relatively high breakdown voltage (avalanche breakdown), while a high-doping junction has a relatively low breakdown voltage (Zener breakdown).

2.2.3 pn Junction Under Forward Bias

For every $V_T \ln 10 \approx 60$ mV increase in the forward voltage, I_D becomes ten times the original.

Note that the current-voltage characteristic is relatively sensitive to temperature, i.e., for every 1°C increase in temperature, the curve shifts to the left by 2 mV $\sim$ 2.5 mV.

In some cases, the static characteristic of a diode needs to be modified for better accuracy:

$$I_D = I_S \left[\exp\left(\frac{V}{nV_T}\right) - 1\right] \tag{2.17}$$

where r_S is the parasitic resistance and n (typically $1 \sim 2$) is the correction factor.

2.2.4 Temperature Dependence

Table 2.1: Temperature Dependence of Junction Parameters

Parameter	temp coefficient
V_B	-
I_S	+
$V_{BR,\text{Zener}}$	-
$V_{BR,\text{Avalanche}}$	+

Chapter 3 Diode Models and Circuits

Chapter 4 Physics of Bipolar Transistors

In this chapter, we analyze the structure and operation of bipolar transistors, preparing ourselves for the study of circuits employing such devices.

we aim to understand the physics of the transistor, derive equations that represent its I/V characteristics, and develop an equivalent model that can be used in circuit analysis and design.

4.1 Structure of Bipolar Transistors

Note that all of the operation principles and equations described for npn transistors apply to pnp devices as well.

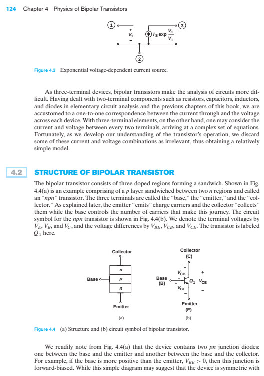
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Figure 4.3 Exponential voltage-dependent current source.

As three-terminal devices, bipolar transistors make the analysis of circuits more difficult. Having dealt with two-terminal components such as resistors, capacitors, inductors, and diodes in elementary circuit analysis and the previous chapters of this book, we are accustomed to a one-to-one correspondence between the current through and the voltage across each device. With three-terminal elements, on the other hand, one may consider the current and voltage between every two terminals, arriving at a complex set of equations. Fortunately, as we develop our understanding of the transistor's operation, we discard some of these current and voltage combinations as irrelevant, thus obtaining a relatively simple model.

4.2 STRUCTURE OF BIPOLAR TRANSISTOR

The bipolar transistor consists of three doped regions forming a sandwich. Shown in Fig. 4.4(a) is an example comprising of a *p* layer sandwiched between two *n* regions and called an "*npn*" transistor. The three terminals are called the "base," the "emitter," and the "collector." As explained later, the emitter "emits" charge carriers and the collector "collects" them while the base controls the number of carriers that make this journey. The circuit symbol for the *npn* transistor is shown in Fig. 4.4(b). We denote the terminal voltages by V_E, V_B, and V_C, and the voltage differences by V_{BE}, V_{CB}, and V_{CE}. The transistor is labeled Q_1 here.

Figure 4.4 (a) Structure and (b) circuit symbol of bipolar transistor.

We readily note from Fig. 4.4(a) that the device contains two *pn* junction diodes: one between the base and the emitter and another between the base and the collector. For example, if the base is more positive than the emitter, $V_{BE} > 0$, then this junction is forward-biased. While this simple diagram may suggest that the device is symmetric with

Figure 4.1: Structure and circuit symbol of a bipolar junction transistor (BJT)

In reality, the dimensions and doping levels of the emitter and the collector are quite different to achieve the desired characteristics. For transistors in active mode, i.e., $V_C > V_B > V_E$, we have:

$$I_C = I_S\left(\exp\frac{V_{BE}}{V_T} - 1\right)\left(1 + \frac{V_{CE}}{V_A}\right) \tag{4.1}$$

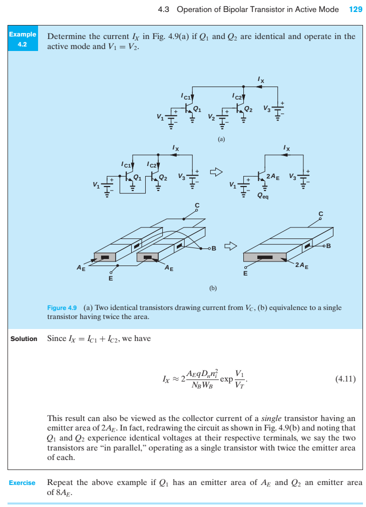
$$\approx I_S \exp\frac{V_{BE}}{V_T} \quad (V_{BE} > 5V_T = 130\ \text{mV}) \tag{4.2}$$

where:

(1) $I_S = \frac{A_E q_e D_n n_i^2}{N_B W_B}$;
(2) A_E: emitter cross-sectional area;
(3) q_e: electron charge;
(4) D_n: electron diffusion coefficient (34 cm^2/s for D_n, 12 cm^2/s for D_p);
(5) N_B: base doping level;
(6) W_B: base width;

Due to the exponential dependence of I_C on V_{BE}, for every 60 mV ($V_T \ln 10$ at T = 300 K) increase in V_{BE}, I_C increases by a factor of 10.

In practice, the BE voltage of Integrated devices $V_{BE,int}$ is 100 mV $\sim$ 150 mV greater than that of discrete devices $V_{BE,dis}$, due to the diffferent base width and other parameters (otherwise it should be about 380mV).


4.3 Operation of Bipolar Transistor in Active Mode 129

Example 4.2 Determine the current I_X in Fig. 4.9(a) if Q_1 and Q_2 are identical and operate in the active mode and $V_1 = V_2$.

Figure 4.9 (a) Two identical transistors drawing current from V_C. (b) equivalence to a single transistor having twice the area.

Solution Since $I_X = I_{C1} + I_{C2}$, we have

$$I_X \approx 2\frac{A_E q D_n n_i^2}{N_B W_B}\exp\frac{V_1}{V_T}. \tag{4.11}$$

This result can also be viewed as the collector current of a *single* transistor having an emitter area of $2A_E$. In fact, redrawing the circuit as shown in Fig. 4.9(b) and noting that Q_1 and Q_2 experience identical voltages at their respective terminals, we say the two transistors are "in parallel," operating as a single transistor with twice the emitter area of each.

Exercise Repeat the above example if Q_1 has an emitter area of A_E and Q_2 an emitter area of $8A_E$.

Figure 4.2: Two parallel transistors and the equivalence to a single transistor having twice area

4.2 Bipolar Transistor Models

For a bipolar transistor in active mode, we have the large-signal model:

$$I_C = I_S \exp\frac{V_{BE}}{V_T}\left(1 + \frac{V_{CE}}{V_A}\right) \approx I_S \exp\frac{V_{BE}}{V_T} \tag{4.3}$$

$$I_B = \frac{I_C}{\beta}, \quad I_E = I_C + I_E = \frac{\beta + 1}{\beta}I_C = \alpha I_C \tag{4.4}$$

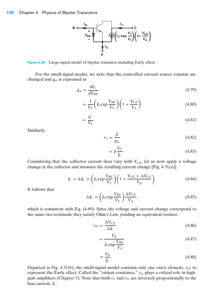

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Figure 4.30 Large-signal model of bipolar transistor including Early effect.

For the small-signal model, we note that the controlled current source remains unchanged and g_m is expressed as

$$g_m = \frac{dI_C}{dV_{BE}} \tag{4.79}$$
$$= \frac{1}{V_T}\left(I_S \exp\frac{V_{BE}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right) \tag{4.80}$$
$$= \frac{I_C}{V_T}. \tag{4.81}$$

Similarly,

$$r_\pi = \frac{\beta}{g_m} \tag{4.82}$$
$$= \beta\frac{V_T}{I_C}. \tag{4.83}$$

Considering that the collector current does vary with V_{CE}, let us now apply a voltage change at the collector and measure the resulting current change [Fig. 4.31(a)]:

$$I_C + \Delta I_C = \left(I_S \exp\frac{V_{BE}}{V_T}\right)\left(1 + \frac{V_{CE} + \Delta V_{CE}}{V_A}\right). \tag{4.84}$$

It follows that

$$\Delta I_C = \left(I_S \exp\frac{V_{BE}}{V_T}\right)\frac{\Delta V_{CE}}{V_A}, \tag{4.85}$$

which is consistent with Eq. (4.69). Since the voltage and current change correspond to the same two terminals, they satisfy Ohm's Law, yielding an equivalent resistor:

$$r_O = \frac{\Delta V_{CE}}{\Delta I_C} \tag{4.86}$$
$$= \frac{V_A}{I_S \exp\frac{V_{BE}}{V_T}} \tag{4.87}$$
$$\approx \frac{V_A}{I_C}. \tag{4.88}$$

Depicted in Fig. 4.31(b), the small-signal model contains only one extra element, r_O, to represent the Early effect. Called the "output resistance," r_O plays a critical role in high-gain amplifiers (Chapter 5). Note that both r_π and r_O are inversely proportionally to the bias current, I_C.

(a) npn

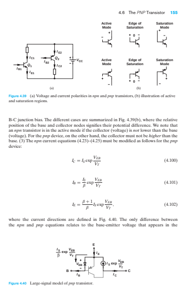

4.6 The *PNP* Transistor 155

Figure 4.39 (a) Voltage and current polarities in *npn* and *pnp* transistors, (b) illustration of active and saturation regions.

B-C junction bias. The different cases are summarized in Fig. 4.39(b), where the relative position of the base and collector nodes signifies their potential difference. We note that an *npn* transistor is in the active mode if the collector (voltage) is *not* lower than the base (voltage). For the *pnp* device, on the other hand, the collector must not be *higher* than the base. (3) The *npn* current equations (4.23)–(4.25) must be modified as follows for the *pnp* device:

$$I_C = I_S \exp\frac{V_{EB}}{V_T} \tag{4.100}$$

$$I_B = \frac{I_S}{\beta}\exp\frac{V_{EB}}{V_T} \tag{4.101}$$

$$I_E = \frac{\beta+1}{\beta}I_S \exp\frac{V_{EB}}{V_T}, \tag{4.102}$$

where the current directions are defined in Fig. 4.40. The only difference between the *npn* and *pnp* equations relates to the base-emitter voltage that appears in the

Figure 4.40 Large-signal model of *pnp* transistor.

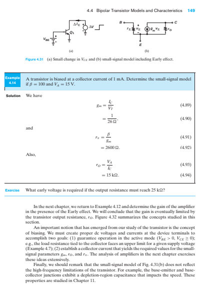
(b) pnp

Figure 4.3: Large-signal

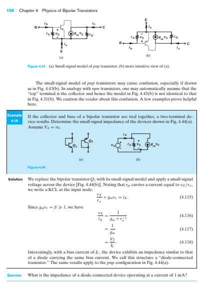
And the small-signal model is:

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_T}, \quad r_\pi = \frac{\partial V_{BE}}{\partial I_B} = \frac{\beta}{g_m} \tag{4.5}$$

$$r_O = \frac{\partial V_{CE}}{\partial I_C} = \frac{I_C}{V_A + V_{CE}} \approx \frac{I_C}{V_A} \tag{4.6}$$



(a) npn



(b) pnp

Figure 4.4: Small-signal

4.3 Bipolar Transistor in Saturation

The term “saturation” is used because increasing the base current in this region of operation leads to little change in the collector current.

Heavy saturation leads to a sharp rise in the base current and hence a rapid fall in β. In addition to a drop in β, the speed of bipolar transistors also degrades in saturation.

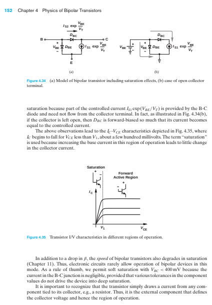


Figure 4.5

As a rule of thumb, we permit soft saturation with $V_{BC} < 400$ mV because the current in the B-C junction is negligible.

Chapter 5 Bipolar Amplifiers

With the physics and operation of bipolar transistors described in Chapter 4, we now deal with amplifier circuits employing such devices. There is an extremely wide usage of amplification in microelectronics, motivating us to master the analysis and design of such building blocks.

5.1 BJT's Terminal Impedances

When determining the transfer of signals from one stage to the next, the I/O impedances are usually regarded as small-signal quantities, with the tacit assumption that the signal levels are indeed small.

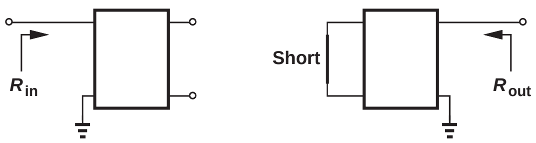
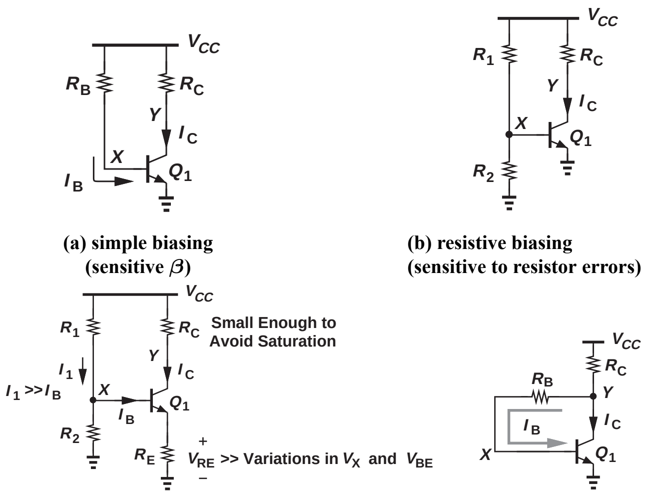


Figure 5.1: Impedance seen at a node

We summarize the small-signal impedances of the BJT in Table 5.1. Remark that the impedance here denotes to the small-signal impedance, while we use an upper case here.

5.2 Biasing Techniques



(a) simple biasing (sensitive β)

(b) resistive biasing (sensitive to resistor errors)

(c) emitter degeneration (the most commonly used)

(d) self-biased stage (always in active mode)

Figure 5.2: Basic biasing techniques

5.2.1 Simple Biasing

The biasing scheme above is simple, but suffering from the low stability and accuracy.

First, the uncertainty of V_{BE} becomes significant because the bias is sensitive to V_{BE} variations. Second, I_C heavily depends on β, a parameter that may change considerably with temperature and transistor mismatch. For these reasons, the topology is rarely used in practice.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, \quad I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B} \tag{5.1}$$

$$V_{CE} = V_{CC} - \beta \frac{V_{CC} - V_{BE}}{R_B} R_C \tag{5.2}$$

5.2.2 Resistive Divider Biasing

As shown in Figure 5.2 (b), the resistive divider biasing constructs a relatively stable base bias current.

$$R_{Thev} = R_1 \parallel R_2, \quad V_{Thev} = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{5.3}$$

$$V_{BE} = V_{Thev} - I_B R_{Thev} \tag{5.4}$$

However, this circuit is significantly sensitive to the resistor values. A 1% error in R_2 introduces a 31% $\sim$ 36% error (typ.) in the collector current (and base current), making it hard to define the operation point. The circuit is therefore still of little practical value.

5.2.3 Biasing with Emitter Degeneration

In the circuit shown in Figure 5.2 (c), a relatively large variation in V_X causes negligible change in V_{BE}, hence the collector current becomes more stable.

For example, a 1% error in R_2 introduces only 4% $\sim$ 8% error (typ.) in the collector current, which is a significant improvement over the preceding circuits.

$$I_C \approx I_E = \frac{V_P}{R_E} = \frac{V_X - V_{BE}}{R_E} \tag{5.5}$$

$$\Delta I_C = \frac{\Delta V_X}{R_E} - \frac{\Delta V_{BE}}{R_E} \tag{5.6}$$

In this circuit, two rules are typically followed:

(1) $I_1 \gg I_B$ to lower the sensitivity to β, or use the Thevenin equivalent to gain a more precise bias current.

(2) V_{RE} must be large enough (100 mV to several hundred mV) to suppress the effect of uncertainties in V_X and V_{BE} due to resistance mismatch.

5.2.4 Self-Biasing

Another frequently used biasing technique is the self-biasing circuit, as shown in Figure 5.2 (d).

The most important property is that it guarantees Q_1 to operate in active mode (because $V_C \geqslant V_B$), regardless of the device and circuit parameters.

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta}}, \quad I_B = \frac{I_C}{\beta} \tag{5.7}$$

In this stage, $V_{CC} - V_{BE}$ must be much greater than ΔV_{BE} to stabilize the bias point, and R_C must be much greater than $\frac{R_B}{\beta}$ ($R_C > 10\frac{R_B}{\beta}$) to lower the sensitivity to β.

Table 5.1: BJT's Small-Signal Terminal Resistances

Collector Resistance	Base Resistance	Emitter Resistance
$R_{coll} = r_O \cdot \left[1 + \left(\frac{\beta}{r_\pi + R_B} + \frac{1}{r_O}\right) \cdot (R_E \parallel (r_\pi + R_B))\right]$	$R_{base} = r_\pi + R_E \cdot \frac{\beta r_O + (r_O + R_C)}{R_E + (r_O + R_C)}$	$R_{emit} = \left(1 + \frac{R_C}{r_O}\right) \cdot \left(\frac{r_\pi + R_B}{1 + \frac{R_C}{r_O}} \parallel \frac{r_\pi + R_B}{\beta} \parallel r_O\right)$
$R_{coll}\vert_{R_B=0} = r_O \cdot \left[1 + \left(\frac{\beta}{r_\pi} + \frac{1}{r_O}\right) \cdot (R_E \parallel r_\pi)\right]$	$R_{base}\vert_{R_C=0} = r_\pi + (\beta+1)(R_E \parallel r_O)$	$R_{emit}\vert_{R_C=0} = \frac{r_\pi + R_B}{\beta+1} \parallel r_O$
$R_{coll}\vert_{R_E=0} = r_O$	$R_{base}\vert_{R_E=0} = r_\pi$	$R_{emit}\vert_{R_B=0} = \left(1 + \frac{R_C}{r_O}\right) \cdot \left(\frac{r_\pi}{1 + \frac{R_C}{r_O}} \parallel \frac{r_\pi}{\beta} \parallel r_O\right)$
$\lim\limits_{r_O \to \infty} R_{coll} = \infty$	$\lim\limits_{r_O \to \infty} R_{base} = r_\pi + (\beta+1)R_E$	$\lim\limits_{r_O \to \infty} R_{emit} = \dfrac{r_\pi + R_B}{\beta + 1}$

5.2.5 Biasing Design Procedure

It is possible to prescribe a design procedure for the resistive divider biasing with emitter degeneration, which serves most applications.

(1) Calculate I_C by the required small-signal quantities such as g_m and r_π;
(2) Get g$V_{BE} = V_T \ln \frac{I_C}{I_S}$ and $I_B = \frac{I_C}{\beta}$, or from the datasheet;
(3) Choose $V_{RE} \gg \Delta V_X$, hence $R_E = \frac{V_{RE}}{I_C}$;
(4) Calculate $V_X = V_{BE} + V_{RE}$, R_1 and R_2, ensuring that $I_1 \gg I_B$ (or use the Thevenin equivalent to gain a more precise result);
(5) Determine R_C as large as possible to obtain a high gain, but not too large to avoid saturation.

5.3 Bipolar Amplifier Topologies

5.3.1 Common-Emitter Core

5.4 Bipolar Amplifier with Biasing and Coupling Circuit