YIKANG OUYANG

PhD Student ⋄ Microelectronics Thrust
The Hong Kong University of Science and Technology (Guangzhou)
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RESEARCH INTERESTS

- Electronic Design Automation (EDA), AI-aided VLSI design,VLSI modeling and optimization

EDUCATION

The Hong Kong University of Science and Technology (Guangzhou), China Aug. 2022 – present
Ph.D. student Microelectronics

Sun Yat-Sen University, Guangzhou, China Sep. 2018 – Jul. 2022
B.Eng. Microelectronics

AWARDS AND HONORS

[A2] **Best Paper Award Nomination** IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), 2025

[A2] **Best Paper Award**, ACM/IEEE International Workshop on Machine Learning for CAD (MLCAD), 2023.

[A1] Full Postgraduate Scholarship, HKUST(GZ), 2022-present.

PROJECTS

Glitch Power Modeling & Optimization
Advisor: Prof. Yuzhe Ma
The Hong Kong University of Science and Technology (Guangzhou)

- Proposed a sensitivity-measurement gate-sizing method that significantly reduces glitch power.
- Proposed a fast glitch power estimation method by simulation trace sampling for efficient optimization.
- Publication: ASP-DAC25

Logic Synthesis Modeling and Optimization
Advisor: Prof. Yuzhe Ma
The Hong Kong University of Science and Technology (Guangzhou)

- Proposed a multi-task learning model to predict circuit delay and area.
- Proposed an inverse-design framework that optimizes synthesis sequence with diffusion model.
- Publications: MLCAD‘23, DAC‘25

Mask Optimization in VLSI Manufacturing
Advisor: Prof. Yuzhe Ma
The Hong Kong University of Science and Technology (Guangzhou)

- Use ResNet to predict mask offsets to optimize design quality.
- Publications: TCAD‘24

Multiplier Design Space Exploration
Advisor: Prof. Yuzhe Ma
The Hong Kong University of Science and Technology (Guangzhou)

- Design multipliers with different encodings and structures.
- Publications:DAC’23, TODAES’25

PUBLICATIONS

Journal Papers

[J2] Dongsheng Zuo, Jiadong Zhu, **Yikang Ouyang**, and Yuzhe Ma. 2025. RL-MUL 2.0: Multiplier Design Optimization with Parallel Deep Reinforcement Learning and Space Reduction. ACM Trans. Des. Autom. Electron. Syst. (**TODAES**) 2025.

[J1] Xiaoxiao Liang, **Yikang Ouyang**, Haoyu Yang, Bei Yu, Yuzhe Ma, "RL-OPC: Mask Optimization with Deep Reinforcement Learning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 01, pp. 340–351, 2024.

Conference Papers

$*$ denotes equal contribution.

[C4] **Yikang Ouyang***, Xiaofei Yu*, Jiadong Zhu, Yuzhe Ma, "Efficient Continuous Logic Optimization with Diffusion Model", IEEE/ACM Chips to Systems Conference (DAC), San Francisco, Jun. 2025.

[C3] **Yikang Ouyang**, Yuchao Wu, Dongsheng Zuo, Subhendu Roy, Tinghuan Chen, Zhiyao Xie, Yuzhe Ma, "SMART-GPO: Gate-Level Sensitivity Measurement with Accurate Estimation for Glitch Power Optimization", IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), Tokyo, Jan. 2025.**(Best Paper Award Nomination)**

[C2] **Yikang Ouyang**, Sicheng Li, Dongsheng Zuo, Hanwei Fan, Yuzhe Ma, "ASAP: Accurate Synthesis Analysis and Prediction with Multi-task Learning", ACM/IEEE Workshop on Machine Learning for CAD (**MLCAD**), Utah, Sep. 2023. **(Best Paper Award)**

[C1] Dongsheng Zuo, **Yikang Ouyang**, Yuzhe Ma, "RL-MUL: Multiplier Design Optimization with Deep Reinforcement Learning", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, Jul. 09-13, 2023.

SKILLS

- Language: English, Chinese, Cantonese
- Programming Language: Python, C/C++, MATLAB
- Hardware Design Language: Verilog, CHISEL