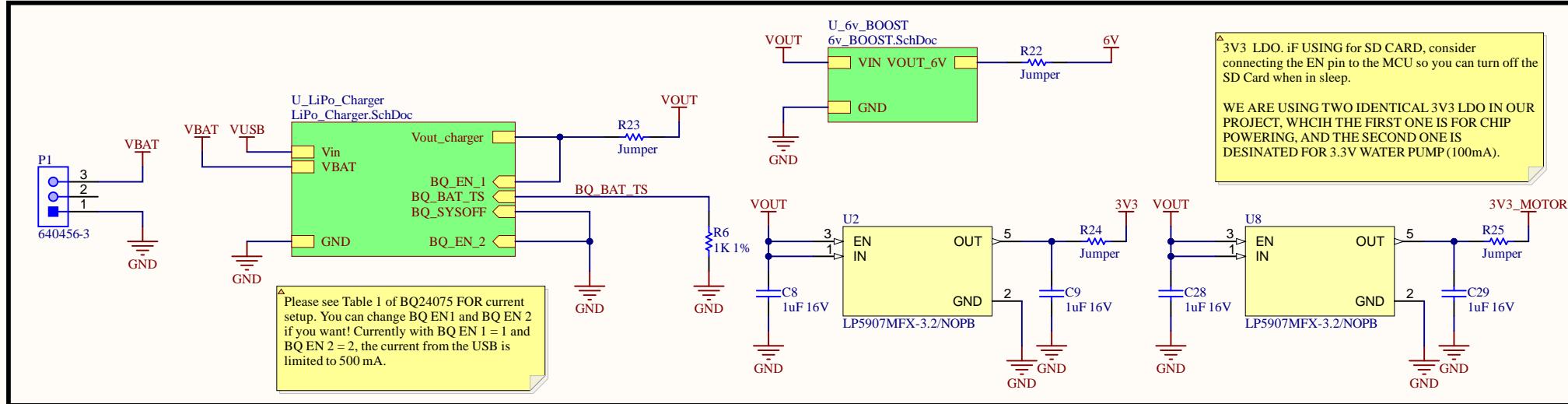


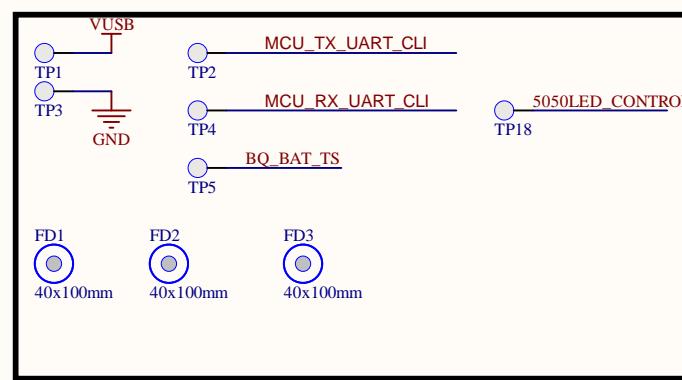
## POWER SUPPLY - CHANGE ME TO YOUR POWER ARCHITECTURE



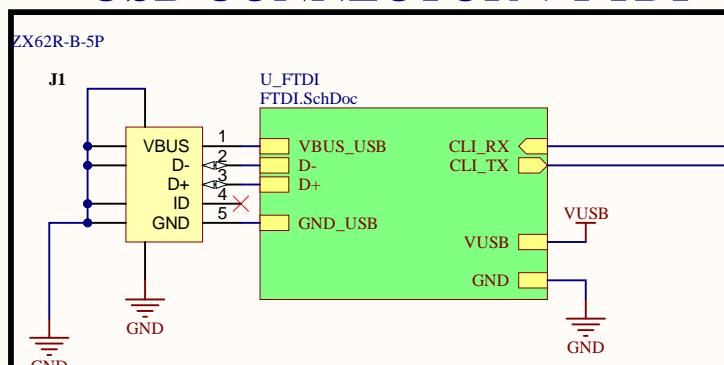
## NOTES

In my project, the 4 components I have are the ambient light sensor, water pump, soil moisture sensor, and a led module. Within that range, the only component that will be soldered to board is the ambient light sensor. So I created a subsheet for that module and created three headers for the rest three components.

## TEST POINTS AND FIDUCIALS

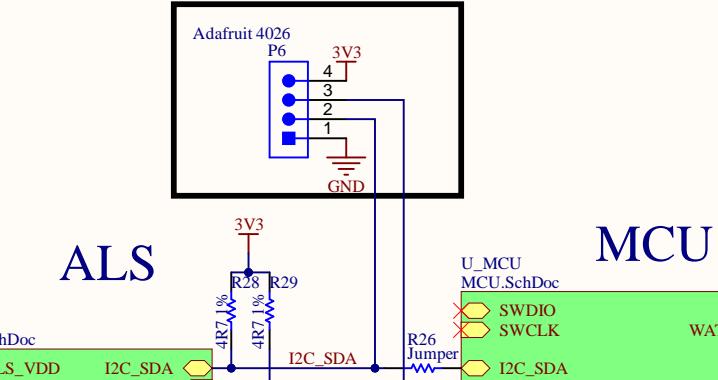


## USB CONNECTOR + FTI

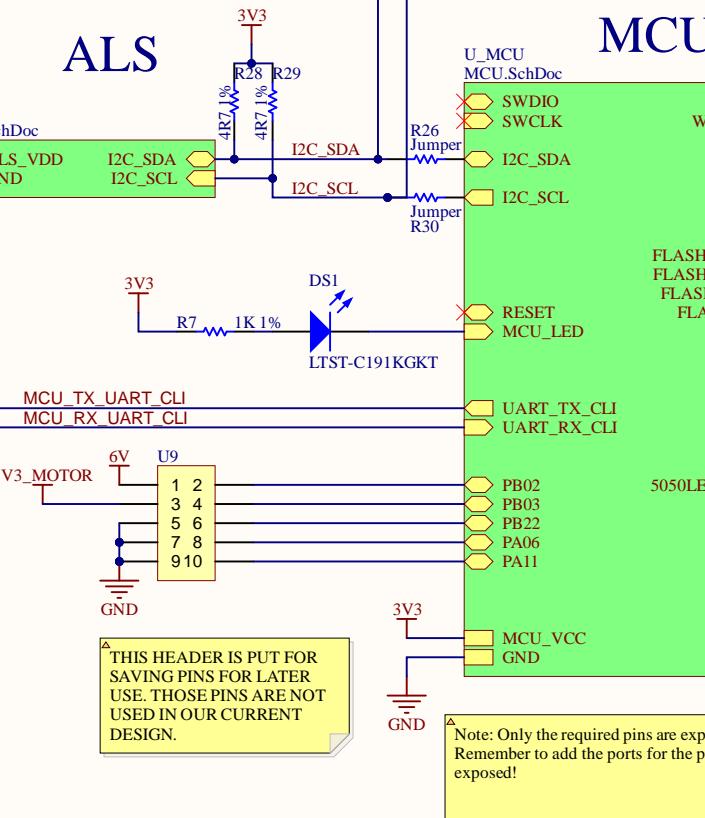


**NOTE:**  
The FTDI Chip is an useful chip that allows us to convert USART messages into USB signals. It allows us to connect the MCU directly to the USB port of a computer and use the serial terminal (it is the same bridge used on the SAMW25 Xplained Board). The FTDI device also contains protection circuitry for the USB.

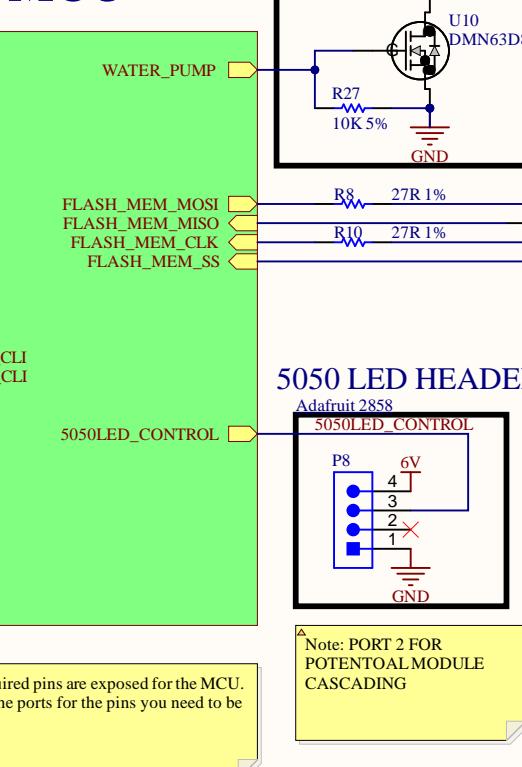
## SOIL MOISTURE SENSOR HEADER



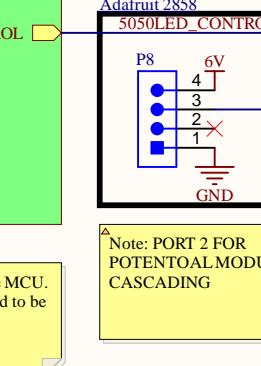
## ALS



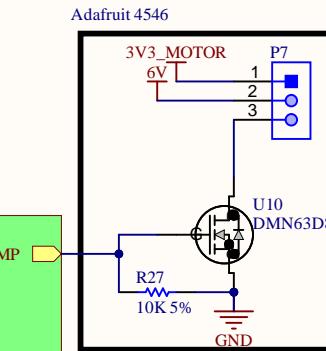
## MCU



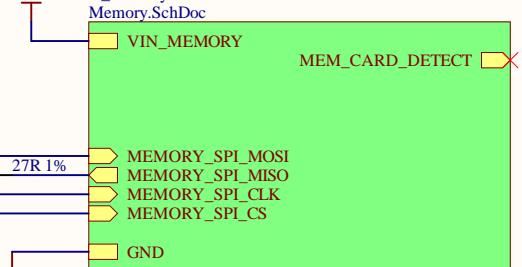
## 5050 LED HEADER



## WATER PUMP HEADER



## SD CARD MEMORY



**Note:**  
This is the SD Card, which we will use for our project.  
PLEASE DO NOT ERASE! Connect a 3V3 rail to this SD Card.  
  
The SD CARD needs 100 mA (worst case, most common is 30mA). If your existing power supply cannot handle this added current, please use the 3V3 LDO found in this project to power your SD Card.

| APPROVALS                     | DATE | PROJECT                      | Penn Engineering | 200 S 33rd St Philadelphia PA, 19104 |
|-------------------------------|------|------------------------------|------------------|--------------------------------------|
| ENG: Yiang Gong & Jianxu Chai |      | ESE516                       |                  |                                      |
| DSN: Yiang Gong & Jianxu Chai |      |                              |                  |                                      |
| CHK: Yiang Gong & Jianxu Chai |      |                              |                  |                                      |
| BOM:                          |      | REFERENCE DOCUMENTS          |                  |                                      |
| ASSY DWG:                     |      |                              |                  |                                      |
| FAB DWG:                      |      |                              |                  |                                      |
| PCB DWG:                      |      | SCALE: FILE NAME MAIN.SchDoc |                  |                                      |
|                               |      |                              |                  | SIZE: CAGE CODE DWG NO. REV. 1.0     |
|                               |      |                              |                  | 1 OF 7                               |

## Main Schematics

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| DWG. NO. | 1.0 | REV.        | SHT. | 1        |
| REVISION |     | DESCRIPTION | DATE | APPROVED |

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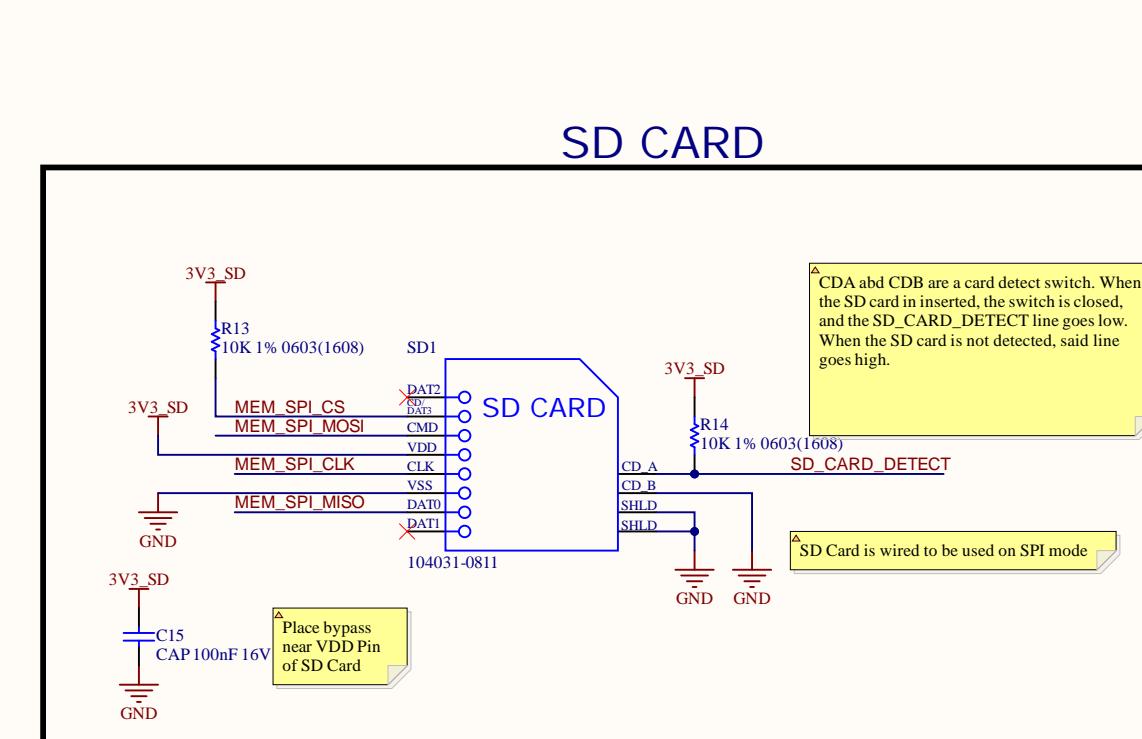
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## TESTPOINTS

|      |                |
|------|----------------|
| TP6  | 3V3_SD         |
| TP7  | SD_CARD_DETECT |
| TP8  | MEM_SPI_MOSI   |
| TP9  | MEM_SPI_MISO   |
| TP10 | MEM_SPI_CLK    |
| TP11 | MEM_SPI_CS     |



|                               |           |               |                  |                                      |
|-------------------------------|-----------|---------------|------------------|--------------------------------------|
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| DSN: Yiang Gong & Jianxu Chai |           |               |                  |                                      |
| CHK: Yiang Gong & Jianxu Chai |           |               |                  |                                      |
| REFERENCE DOCUMENTS           |           |               |                  |                                      |
| BOM:                          |           |               |                  |                                      |
| ASSY DWG:                     |           |               |                  |                                      |
| FAB DWG:                      |           |               |                  |                                      |
| PCB DWG:                      |           |               |                  |                                      |
| SCALE:                        | FILE NAME | Memory.SchDoc | SHEET            | 2 OF 7                               |

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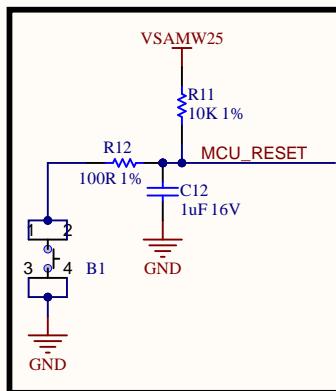
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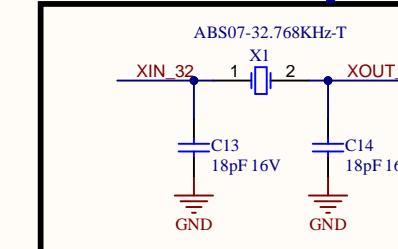
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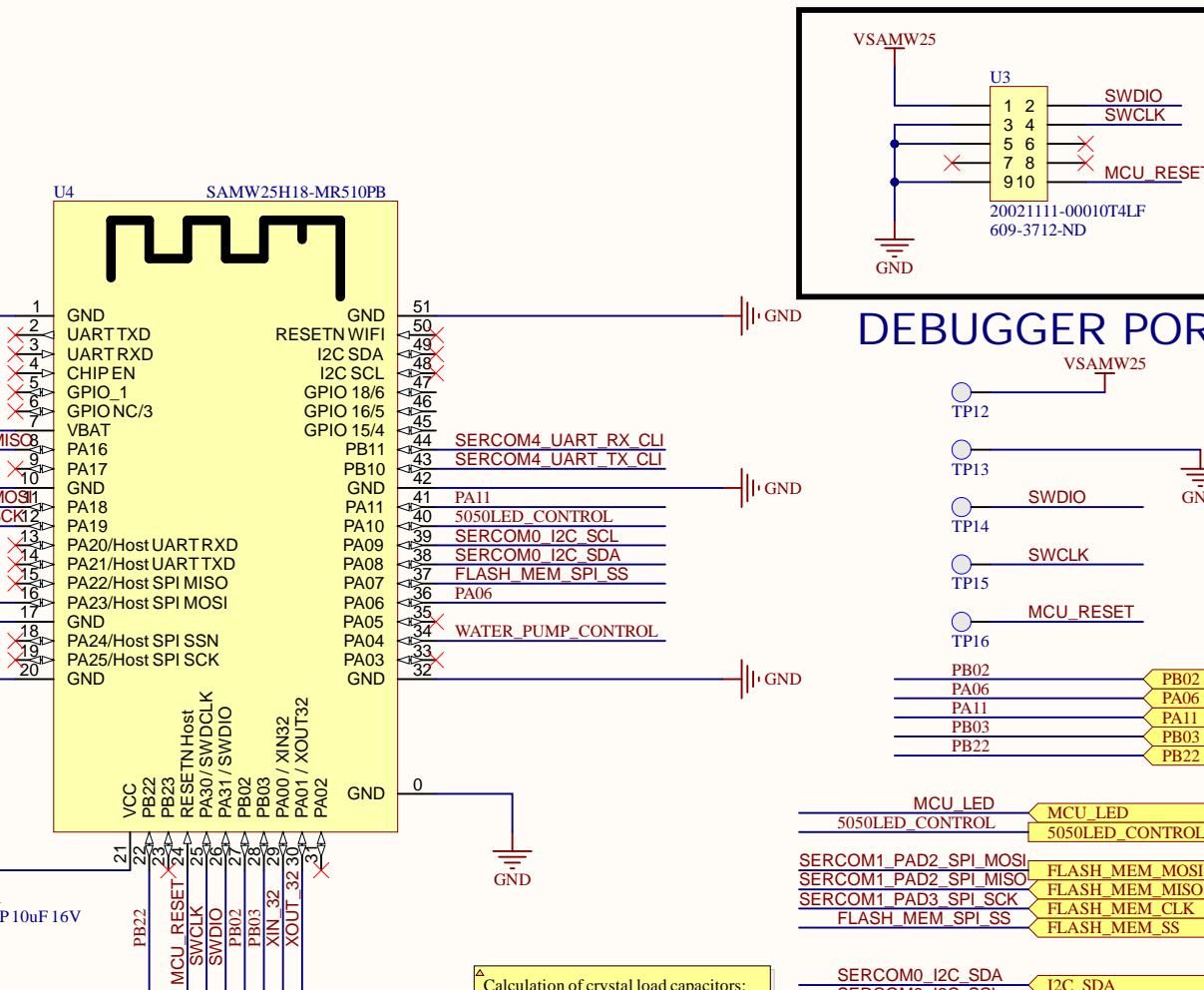
## Reset Button



## 32.768 Crystal



△ Calculation of crystal load capacitors:  
 $C_{ext} = 2 \times (C_{crystal} - C_{para} - C_{pcb})$   
 Ccrystal = 12.5pF (from crystal datasheet)  
 Cpara = 3.15pF (from MCU datasheet)  
 Cpcb = 0.5pF (estimate)  
 $C_{ext} = 2 \times (12.5pF - 3.15pF - 0.5pF) = 17.7pF$



| APPROVALS                     | DATE | PROJECT | Penn Engineering | 200 S 33rd St Philadelphia PA, 19104 |
|-------------------------------|------|---------|------------------|--------------------------------------|
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| DSN: Yiang Gong & Jianxu Chai |      |         |                  |                                      |
| CHK: Yiang Gong & Jianxu Chai |      |         |                  |                                      |
| BOM:                          |      | TITLE   | MCU              |                                      |
| ASSY DWG:                     |      | SIZE    | CAGE CODE        | DWG NO.                              |
| FAB DWG:                      |      | B       |                  | 1.0                                  |
| PCB DWG:                      |      | SCALE:  | FILE NAME        | MCU.SchDoc                           |
|                               |      | SHEET   | 3                | OF 7                                 |

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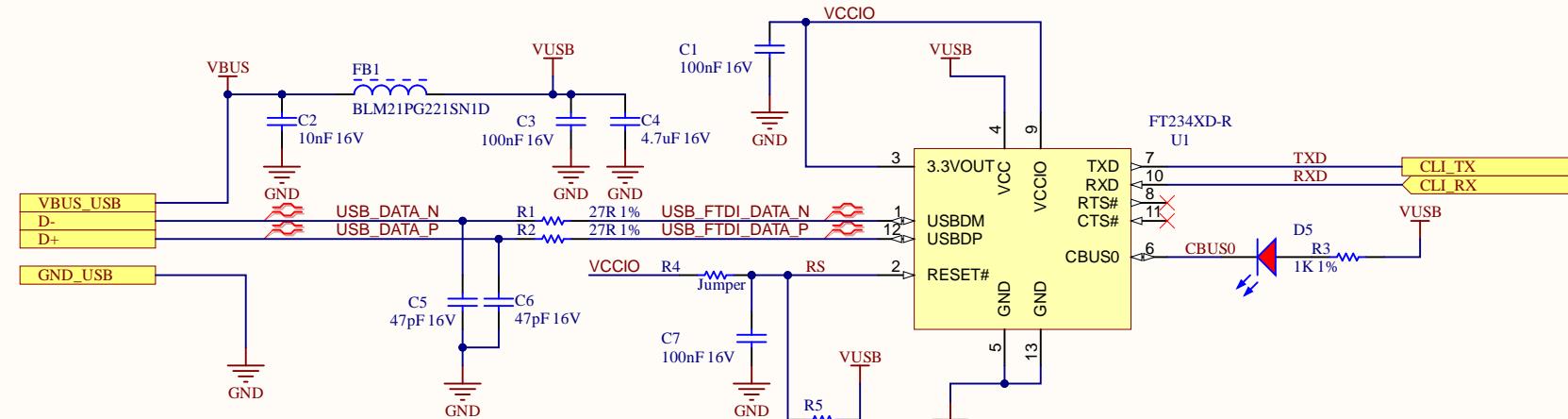
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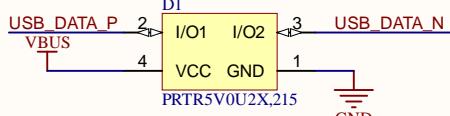
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## FTDI CHIP



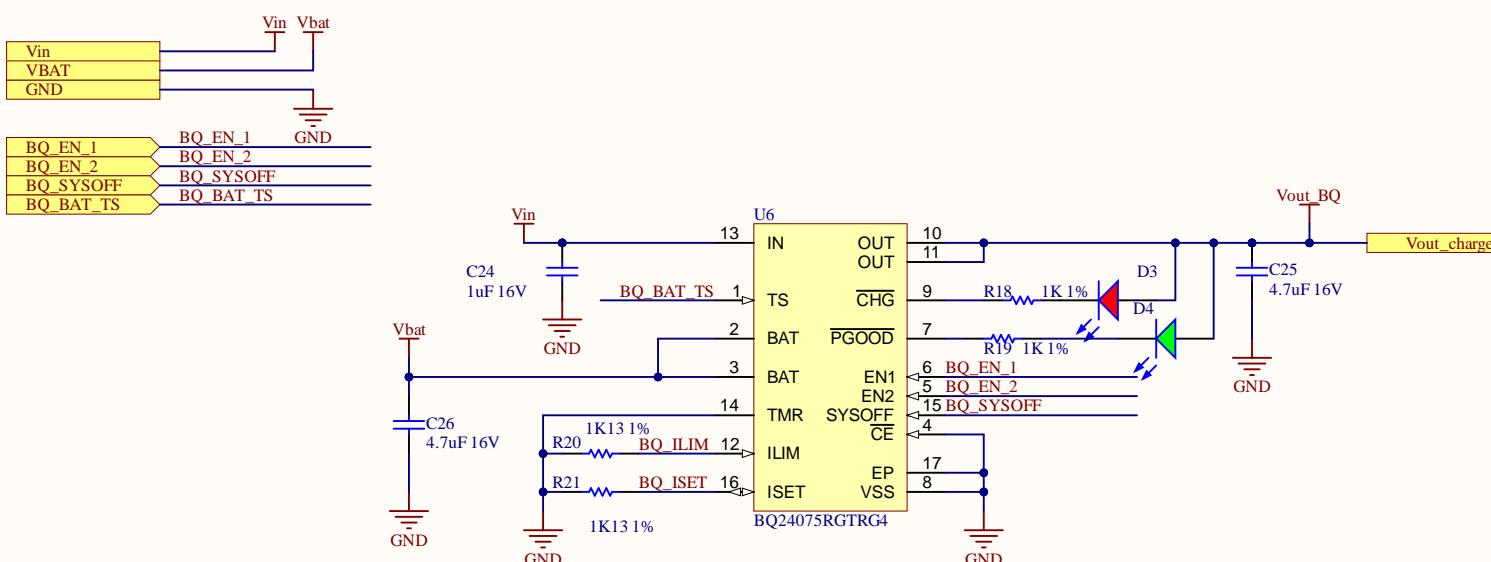
## USB ESD PROTECTION



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| DSN: Yiang Gong & Jianxu Chai |           |             |                  |   |
| CHK: Yiang Gong & Jianxu Chai |           |             |                  |   |
| REFERENCE DOCUMENTS           |           |             |                  |   |
| BOM:                          |           |             |                  |   |
| ASSY DWG:                     |           |             |                  |   |
| FAB DWG:                      |           |             |                  |   |
| PCB DWG:                      |           |             |                  |   |
| SCALE:                        | FILE NAME | FTDI.SchDoc |                  | SHEET 4 OF 7                                  |
|                               |           |             |                  | REV 1.0                                       |

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| DWG. NO. | * REV. | 5 | SHT. | REVISION | DESCRIPTION | DATE | APPROVED |
|----------|--------|---|------|----------|-------------|------|----------|
|          |        |   |      |          |             |      |          |



ilim = Kilim/Rilim #NAME? 1610/1130 = 1.42A (if EN2=1, EN1=0)  
ISET = KISET/RSET #NAME? 890/1130 = 0.788A

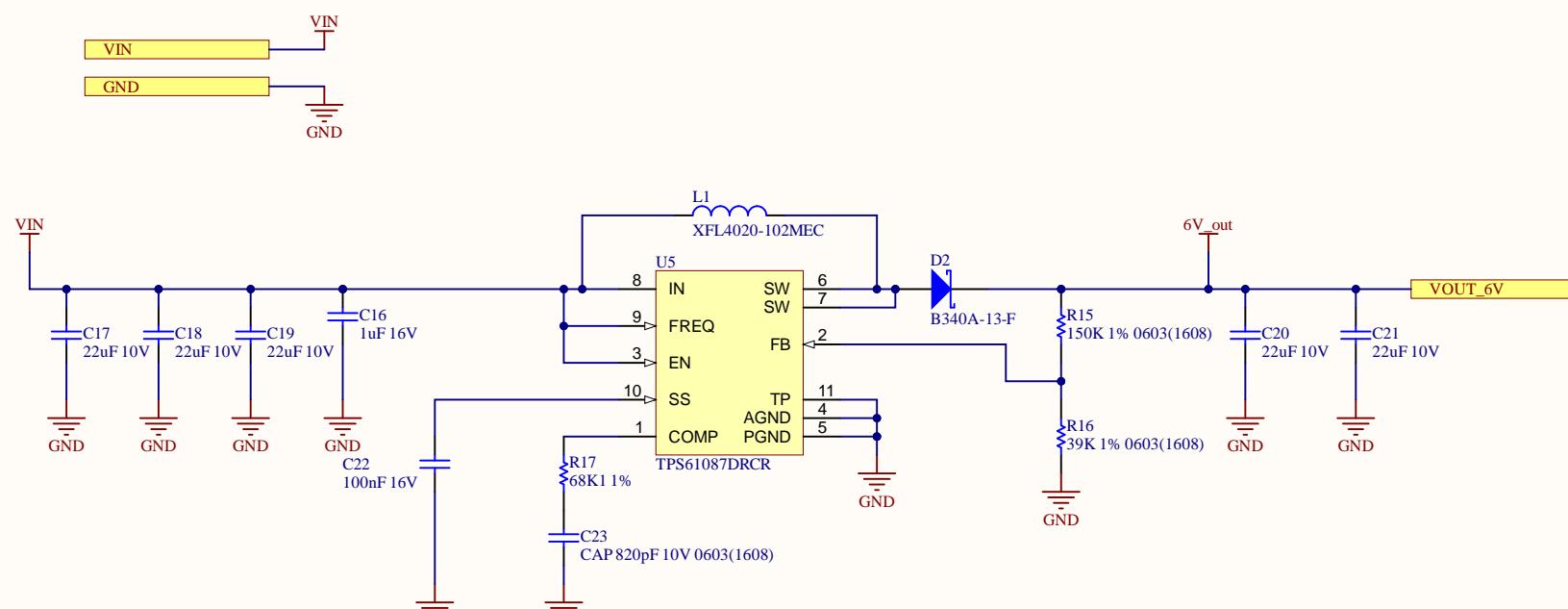
| APPROVALS                     | DATE | PROJECT   | Penn Engineering | 200 S 33rd St Philadelphia PA, 19104       |
|-------------------------------|------|-----------|------------------|--|
| ENG: Yiang Gong & Jianxu Chai |      | ESE516    |                  |  |
| DSN: Yiang Gong & Jianxu Chai |      |           |                  |  |
| CHK: Yiang Gong & Jianxu Chai |      |           |                  |  |
| REFERENCE DOCUMENTS           | BOM: | TITLE     | LIPO_Chaerger    |  |
|                               |      | ASSY DWG: |                  |  |
|                               |      | FAB DWG:  |                  |  |
|                               |      | PCB DWG:  | SCALE: 1         | FILE NAME LiPo_Charger.SchDoc SHEET 5 OF 7 |

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TPS61087DSCR  
VIN: 3.3V to 5.5V  
OUT: 6V up to 1A

| APPROVALS                     | DATE      | PROJECT         | Penn Engineering | 200 S<br>33rd St<br>Philadelphia<br>PA, 19104 |
|-------------------------------|-----------|-----------------|------------------|---|
| ENG: Yiang Gong & Jianxu Chai |           | ESE516          |                  |   |
| DSN: Yiang Gong & Jianxu Chai |           |                 |                  |   |
| CHK: Yiang Gong & Jianxu Chai |           |                 |                  |   |
| <b>REFERENCE DOCUMENTS</b>    |           |                 |                  |   |
| BOM:                          |           |                 |                  |   |
| ASSY DWG:                     |           |                 |                  |   |
| FAB DWG:                      |           |                 |                  |   |
| PCB DWG:                      |           |                 |                  |   |
| SCALE:                        | FILE NAME | 6v_BOOST.SchDoc | SHEET            | 6 OF 7  |

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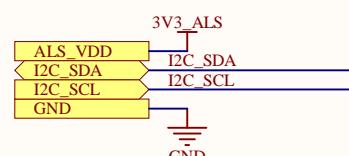
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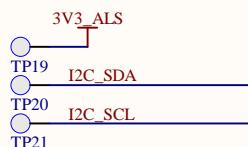
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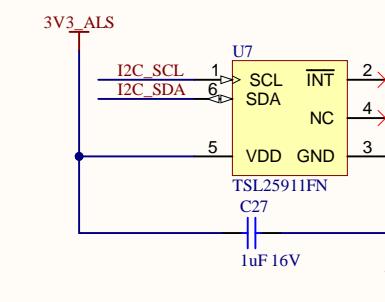
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### TEST POINTS



### AMBIENT LIGHT SENSOR

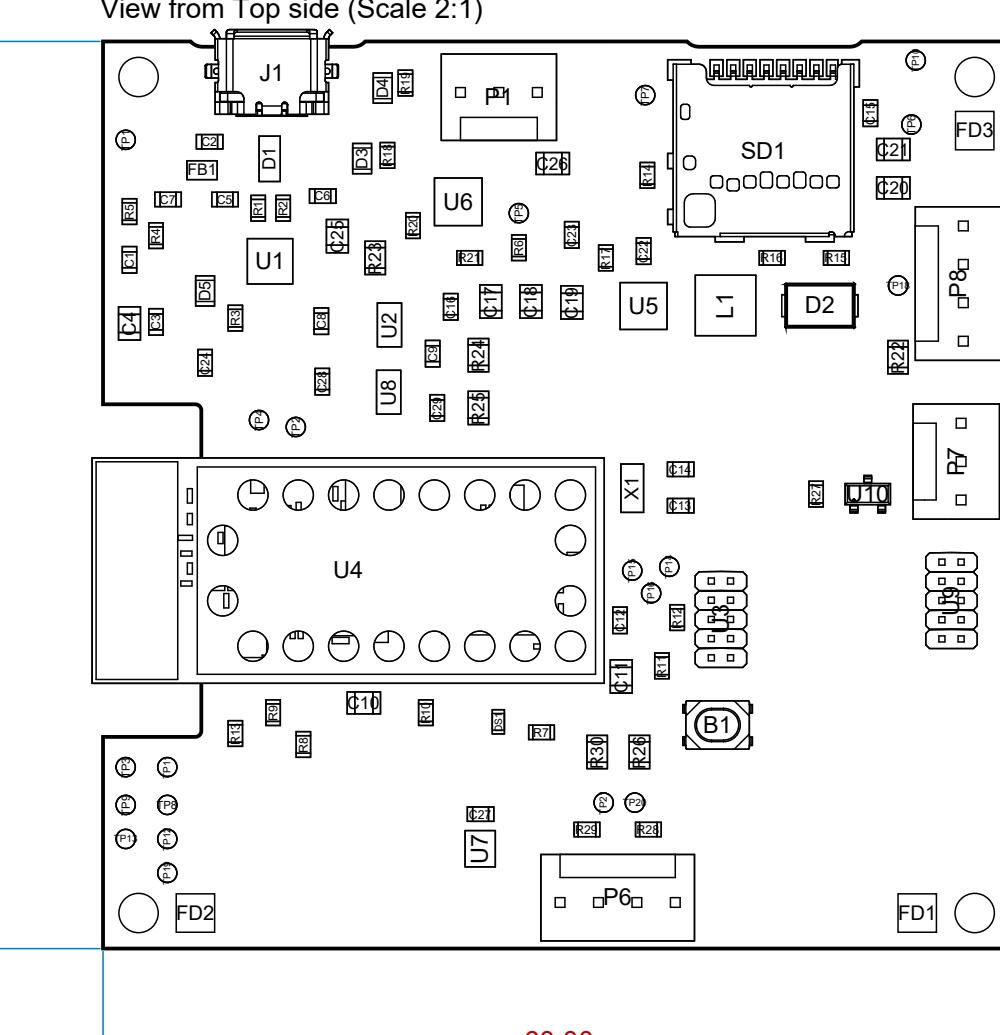


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| APPROVALS                   | DATE                     | PROJECT           | Penn Engineering   | 200 S<br>33rd St<br>Philadelphia<br>PA, 19104 |
| ENG:                        | Yiang Gong & Jianxu Chai | ESE516            |                    |   |
| DSN:                        | Yiang Gong & Jianxu Chai | PROJECT REVISION: | DOCUMENT REVISION: | DESIGN ITEM:                                  |
| <b>Ambient Light Sensor</b> |                          |                   |                    |   |
| REFERENCE DOCUMENTS         | BOM:                     | ASSY DWG:         | CAGE CODE          | DWG NO.                                       |
| CHK:                        | Yiang Gong & Jianxu Chai | FAB DWG:          |                    |   |
| PCB DWG:                    |                          | PCB DWG:          | FILE NAME          | SCALE: ALS.SchDoc SHEET 7 OF 7                |

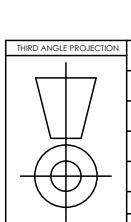


## Manufacture Notes

Four (4) layers  
Dimensions: 60mm x 60mm  
Thickness: 0.062"  
Material: FR4  
Surface Finish: ENEPIG  
Minimum Hole Diameter: 8 mils  
Minimum Trace: 6 mils  
Minimum Distance between Copper features: 10 mils  
Solder Mask Color: Red



## Layer Stack Legend



|                           |                 |                                     |                |
|---------------------------|-----------------|-------------------------------------|----------------|
| PART NO: =PCB_PART_NUMBER |                 |                                     |                |
| APPROVALS                 |                 | DATE                                |                |
| ENGINEER:                 | YG & JC         | YG &                                |                |
| DESIGNER:                 | YG & JC         | YG &                                |                |
| CHECKER:                  | =PCB_CHECKER    | =PCB_CHECKER                        |                |
| Reference Documents       |                 |                                     |                |
| BOM DOC:                  | =DOC_NO_BOM     |                                     |                |
| ASSY DOC:                 | =DOC_NO_FAB_DWG |                                     |                |
| SCH DOC:                  | =DOC_NO_SCH_DWG |                                     |                |
| PCB DOC:                  | =PCB_DWG_NO     |                                     |                |
|                           |                 | DESIGN ITEM: .Item                  |                |
|                           |                 | DESIGN ITEM REVISION: .ItemRevision |                |
| TITLE: ESE516<br>PROJECT  |                 |                                     |                |
| SIZE:                     | CAGE CODE:      | DWG NO:                             | REV:           |
| <b>B</b>                  | =CAGE_CO        |                                     |                |
| SCALE:                    | FILE NAME:      | StarterBoardFabrication.PCDBdwf     | SHEET: 1 OF 12 |

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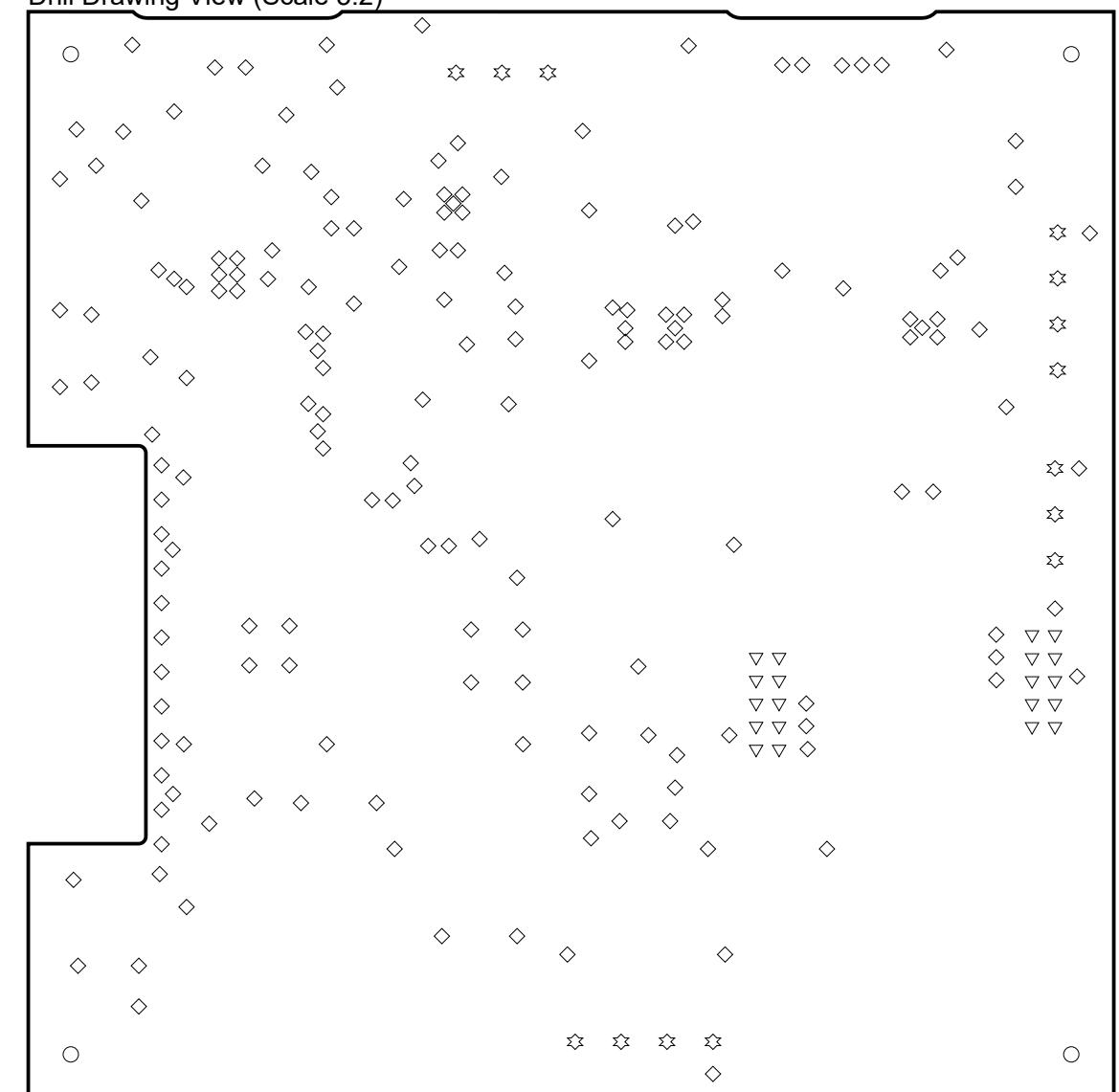
| REV STATUS OF SHEETS |  |  |  | REV |  |  |  |  | DWG NO: =DOC_NO_ASSY_DWG | REV: .lfe |
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| SHEET                |  |  |  |     |  |  |  |  |                          |           |
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| REVISIONS   |      |          |
|-------------|------|----------|
| DESCRIPTION | DATE | APPROVED |
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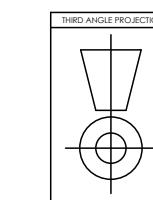
Drill Table

| Symbol    | Count | Hole Size | Plated | Hole Tolerance |
|-----------|-------|-----------|--------|----------------|
| ◇         | 177   | 0.20mm    | Plated |                |
| ▽         | 20    | 0.65mm    | Plated |                |
| ❖         | 14    | 1.27mm    | Plated |                |
| ○         | 4     | 2.70mm    | Plated |                |
| 215 Total |       |           |        |                |

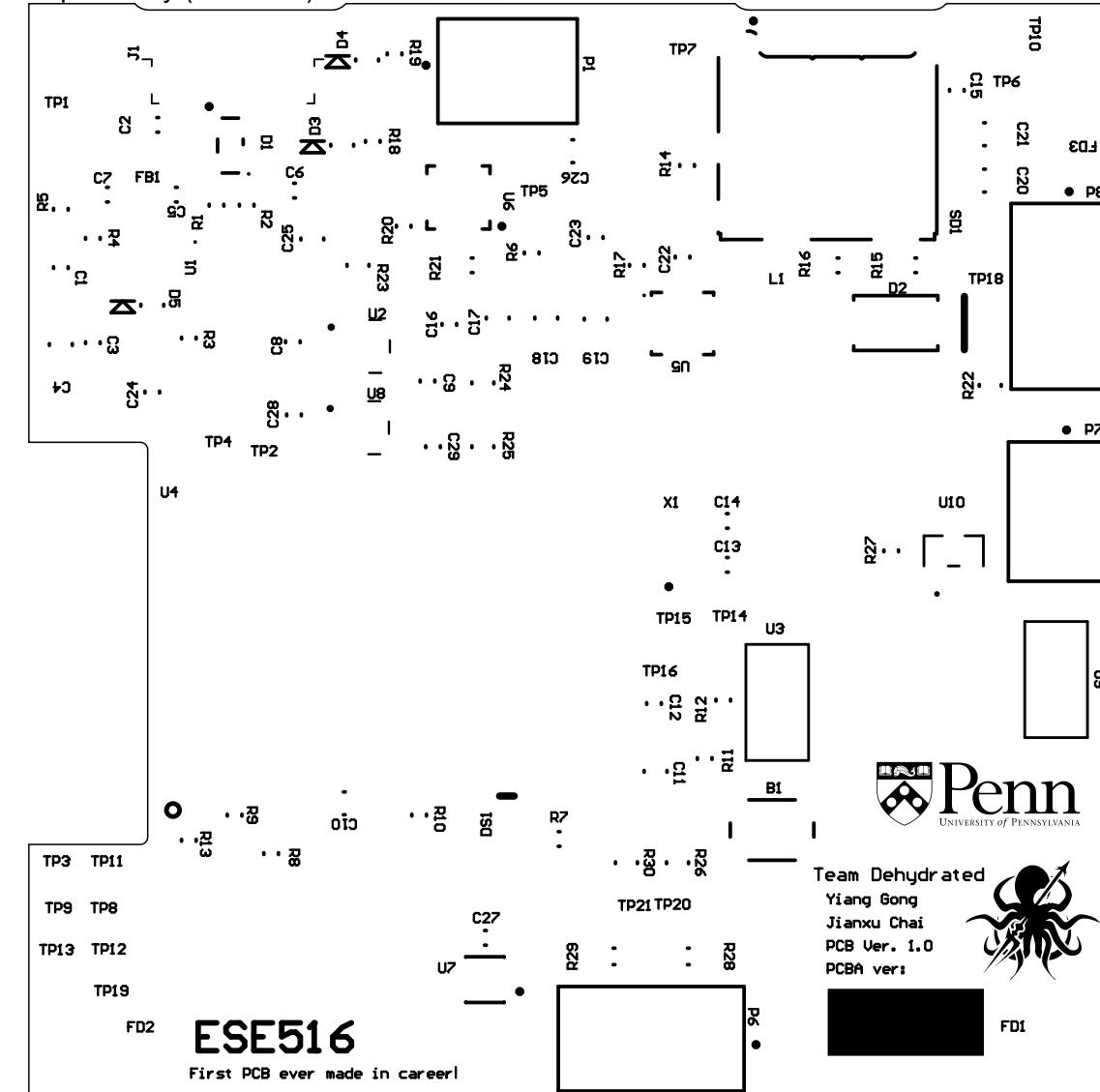
Drill Drawing View (Scale 5:2)



|                           |              |                     |                       |  |  |
|---------------------------|--------------|---------------------|-----------------------|--|--|
| PART NO: =PCB_PART_NUMBER |              | APPROVALS           |                       | DATE                                       | <b>Altium</b><br>200 S<br>33rd St<br>Philadelphia<br>PA, 19104 |
| ENGINEER:                 | YG & JC      | REFERENCE           | YG &                  |  |  |
| DESIGNER:                 | YG & JC      | REFERENCE           | YG &                  |  |  |
| CHECKER:                  | =PCB_CHECKER | =PCB_CHECKER        |                       |  |  |
| BOM DOC:                  |              | Reference Documents |                       | DESIGN ITEM: .Item                         |  |
| ASSY DOC:                 |              | =DOC_NO_BOM         |                       | DESIGN ITEM REVISION: .ItemRevision        |  |
| SCH DOC:                  |              | =DOC_NO_FAB_DWG     |                       | TITLE: ESE516                              |  |
| PCB DOC:                  |              | =DOC_NO_SCH_DWG     |                       | PROJECT                                    |  |
| NEXT ASSY                 |              | USED ON             | CAGE CODE: B =CAGE_CO |  | DWG NO: .  |
| APPLICATION               |              |                     | SCALE: 2 OF 12        | FILE NAME: StarterBoardFabrication.PCDBdwf | REV: .   |



## Top Overlay (Scale 5)



02 ESE51

First PCB ever made in c



Penn  
UNIVERSITY OF PENNSYLVANIA

Team Dehyd  
Yiang Gong  
Jianxu Chai  
PCB Ver. 1.0

|                           |              |                           |              |   |              |
|---------------------------|--------------|---------------------------|--------------|---|--------------|
| PART NO: =PCB_PART_NUMBER |              |                           |              |   |              |
| APPROVALS                 |              | DATE                      |              |   |              |
| ENGINEER:                 | YG & JC      | YG &                      |              |   |              |
| DESIGNER:                 | YG & JC      | YG &                      |              |   |              |
| CHECKER:                  | =PCB_CHECKER | =PCB_CHECKE               | DESIGN ITEM: | .Item                                     |              |
|                           |              | Reference Documents       | TITLE:       | .ItemRevision                             |              |
|                           |              | BOM DOC: =DOC_NO_BOM      | ESE516       |   |              |
|                           |              | ASSY DOC: =DOC_NO_FAB_DWG | PROJECT      |   |              |
|                           |              | SCH DOC: =DOC_NO_SCH_DWG  | SIZE: B      | CAGE CODE: =CAGE_CO                       | DWG NO:      |
| NEXT ASSY                 | USED ON      | PCB DOC: =PCB_DWG_NO      | SCALE:       | FILE NAME: StarterBoardFabrication.PCBDwf | REV: 3 OF 12 |
| APPLICATION               |              |                           |              |   |              |

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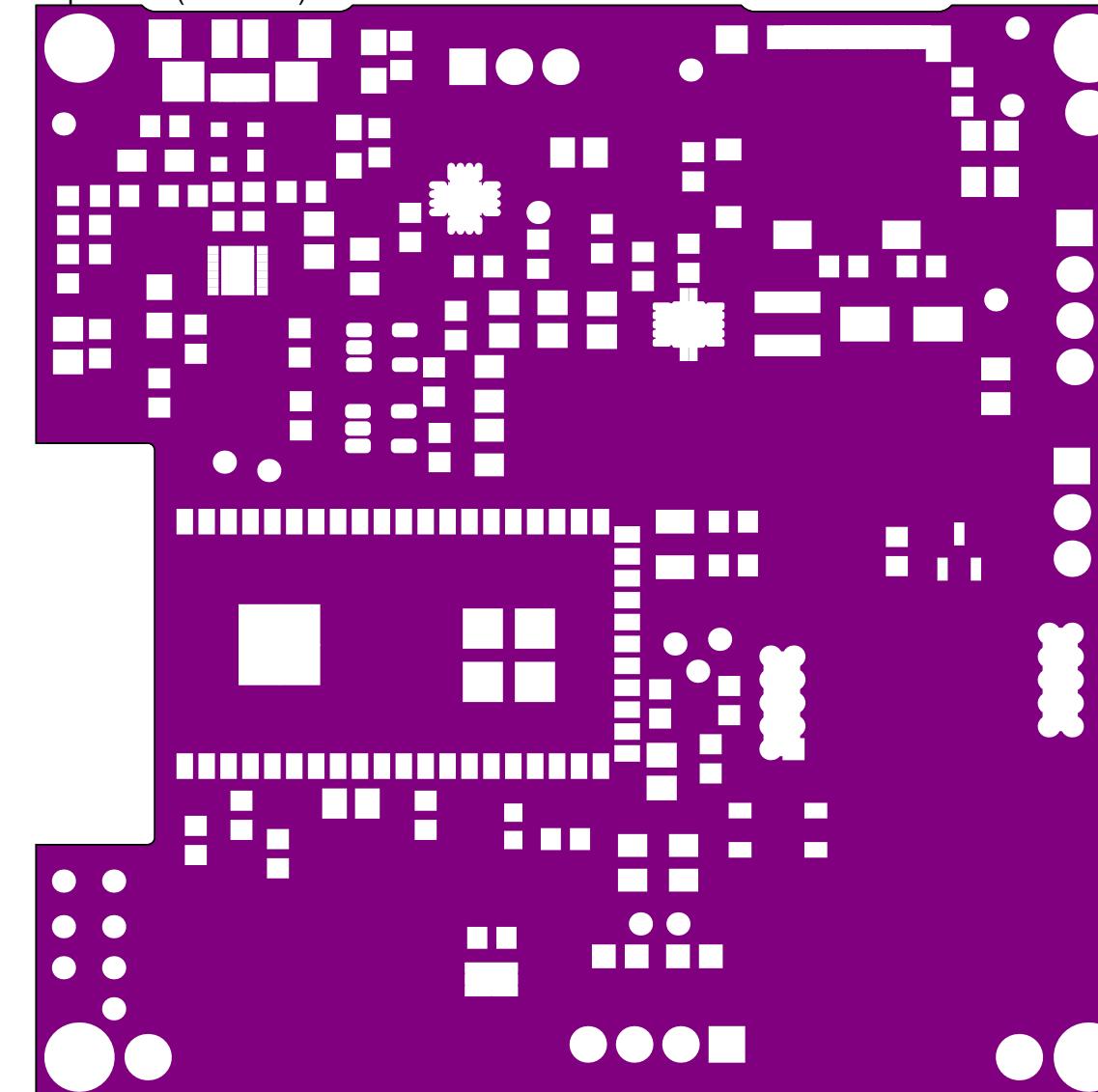
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| DWG NO:<br>=DOC_NO_ASSY_DWG | REV:<br>.lfe |
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|                             |              |

| REVISIONS |  | DESCRIPTION | DATE | APPROVED |
|-----------|--|-------------|------|----------|
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|           |  |             |      |          |
|           |  |             |      |          |
|           |  |             |      |          |

Top Solder (Scale 5:2)



|                           |                     |              |   |  |
|---------------------------|---------------------|--------------|---|--|
| PART NO: =PCB_PART_NUMBER |                     | APPROVALS    | DATE                                      | <b>Altium</b><br>200 S<br>33rd St<br>Philadelphia<br>PA, 19104 |
| ENGINEER:                 | YG & JC             | YG &         |   |  |
| DESIGNER:                 | YG & JC             | YG &         |   |  |
| CHECKER:                  | =PCB_CHECKER        | =PCB_CHECKER |   |  |
| BOM DOC:                  | Reference Documents |              |   |  |
| ASSY DOC:                 | =DOC_NO_BOM         |              |   |  |
| SCH DOC:                  | =DOC_NO_FAB_DWG     |              |   |  |
| NEXT ASSY                 | USED ON             | PCB DOC:     | =PCB_DWG_NO                               |  |
| APPLICATION               |                     | SCALE:       | FILE NAME: StarterBoardFabrication.PCBDwf |  |
|                           |                     | REV:         | 4 OF 12                                   |  |

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: ESE516 PROJECT

SIZE: CAGE CODE: DWG NO: B =CAGE\_CO

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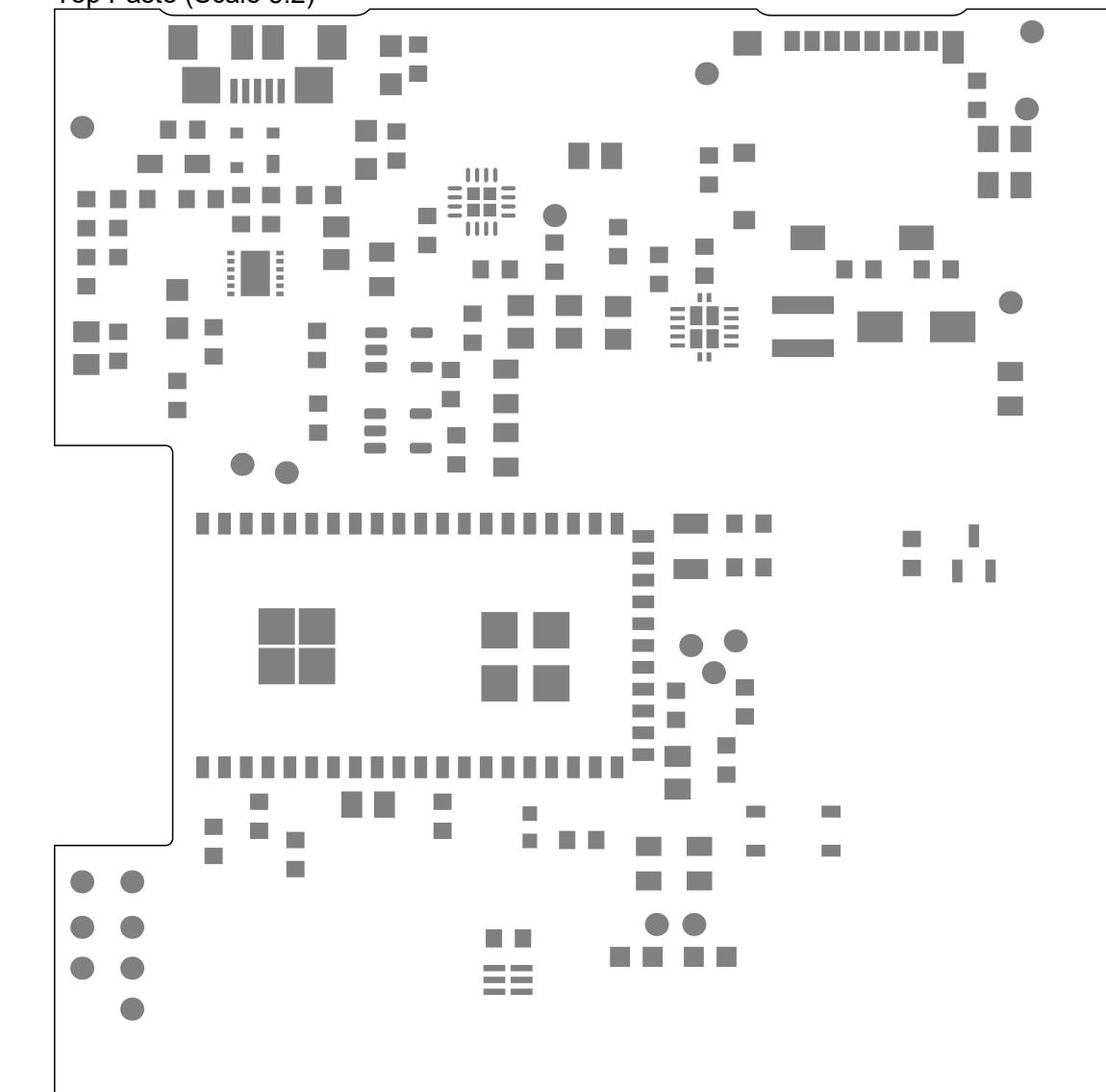
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| REVISIONS   |      |          |
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Top Paste (Scale 5:2)

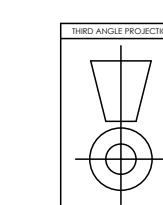


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| DESIGNER:                 | YG & JC                                   | YG &         |  |
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| SCH DOC:                  | =DOC_NO_FAB_DWG                           |              |  |
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| SCALE: 5 OF 12            | FILE NAME: StarterBoardFabrication.PCBDwf | REV: .lfe    |  |

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: ESE516 PROJECT

ITEM: .Item



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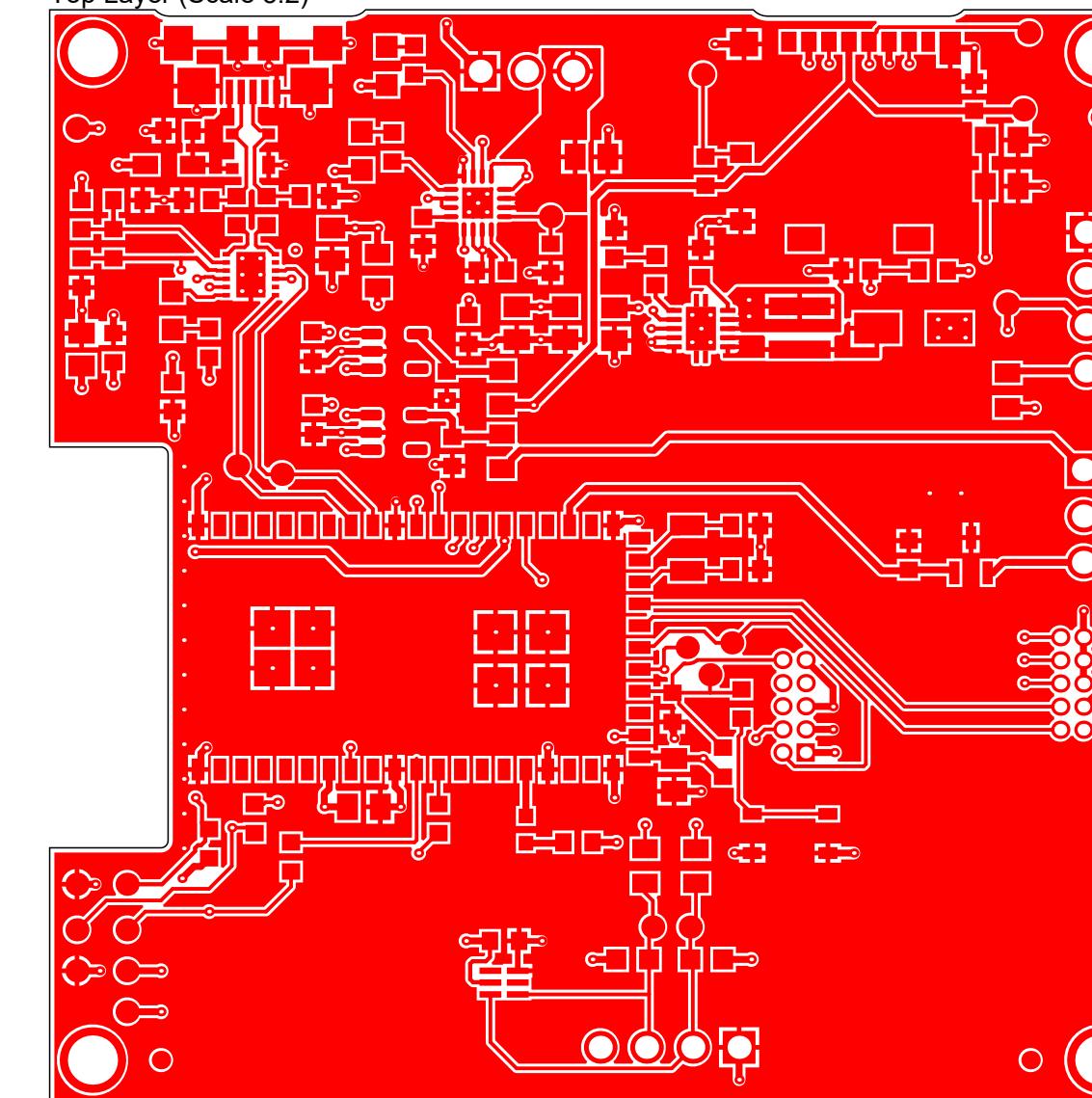
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Top Layer (Scale 5:2)



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PART NO: =PCB\_PART\_NUMBER

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| APPROVALS             | DATE            |
| ENGINEER: YG & JC     | YG &            |
| DESIGNER: YG & JC     | YG &            |
| CHECKER: =PCB_CHECKER | =PCB_CHECKER    |
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| ASSY DOC:             | =DOC_NO_FAB_DWG |
| SCH DOC:              | =DOC_NO_SCH_DWG |
| NEXT ASSY             | USED ON         |
| PCB DOC:              | =PCB_DWG_NO     |
| APPLICATION           |                 |

200 S  
33rd St  
Philadelphia  
PA, 19104

**Altium**  
DESIGN ITEM: .Item  
DESIGN ITEM REVISION: .ItemRevision

ESE516  
PROJECT

SIZE: CAGE CODE: DWG NO: REV:  
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SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 6 OF 12

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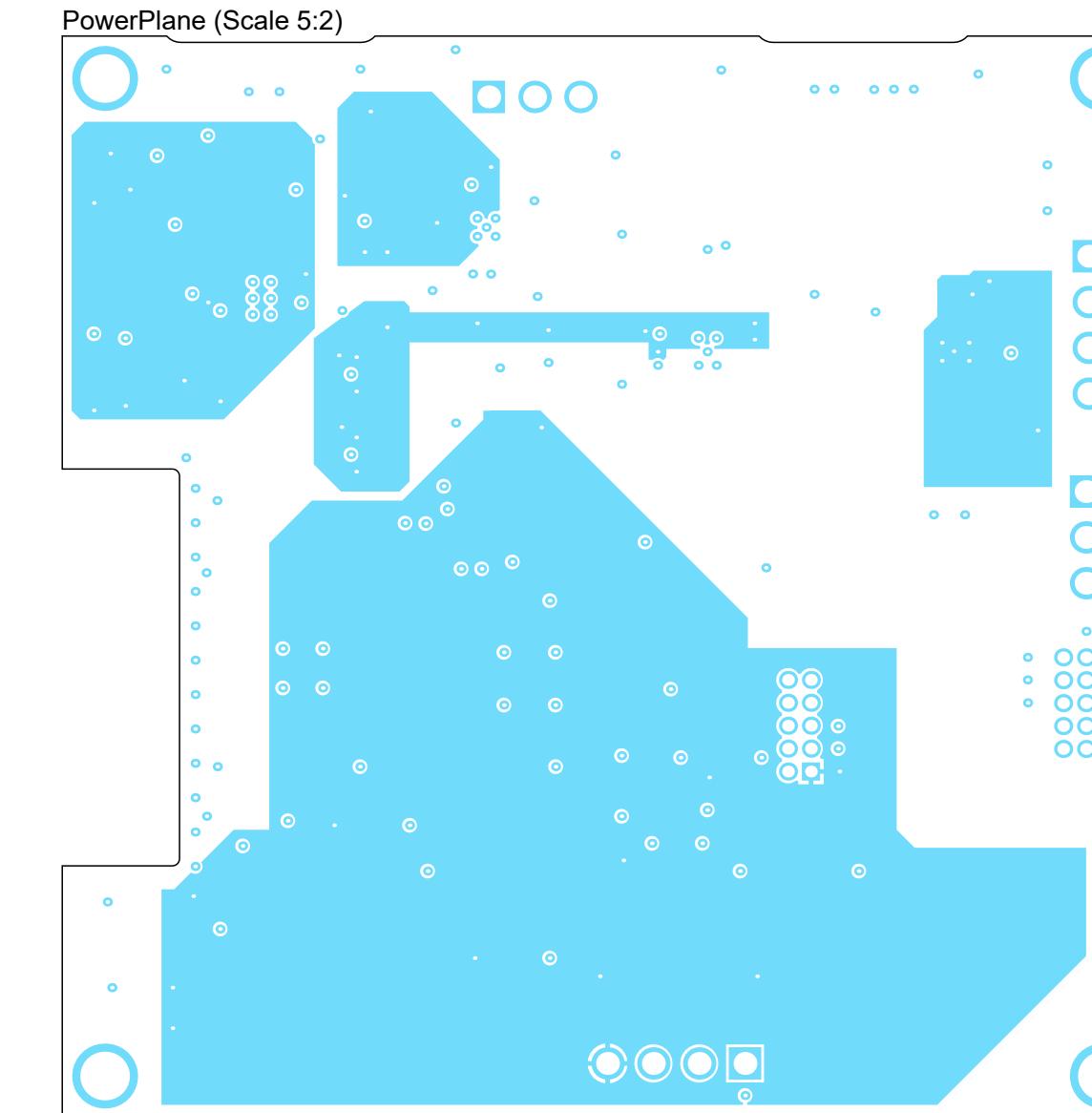
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PART NO: =PCB\_PART\_NUMBER

APPROVALS DATE

ENGINEER: YG &amp; JC

DESIGNER: YG &amp; JC

CHECKER: =PCB\_CHECKER

=PCB\_CHECKER

Reference Documents

BOM DOC: =DOC\_NO\_BOM

ASSY DOC: =DOC\_NO\_FAB\_DWG

SCH DOC: =DOC\_NO\_SCH\_DWG

NEXT ASSY

USED ON

PCB DOC: =PCB\_DWG\_NO

APPLICATION

**Altium**™200 S  
33rd St  
Philadelphia  
PA, 19104

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE:  
ESE516  
PROJECT

SIZE: CAGE CODE: DWG NO:

B =CAGE\_CO

REV:

FILE NAME: StarterBoardFabrication.PCBDwf

SCALE: SHEET: 7 OF 12

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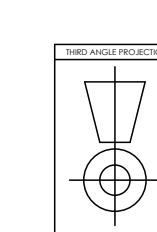
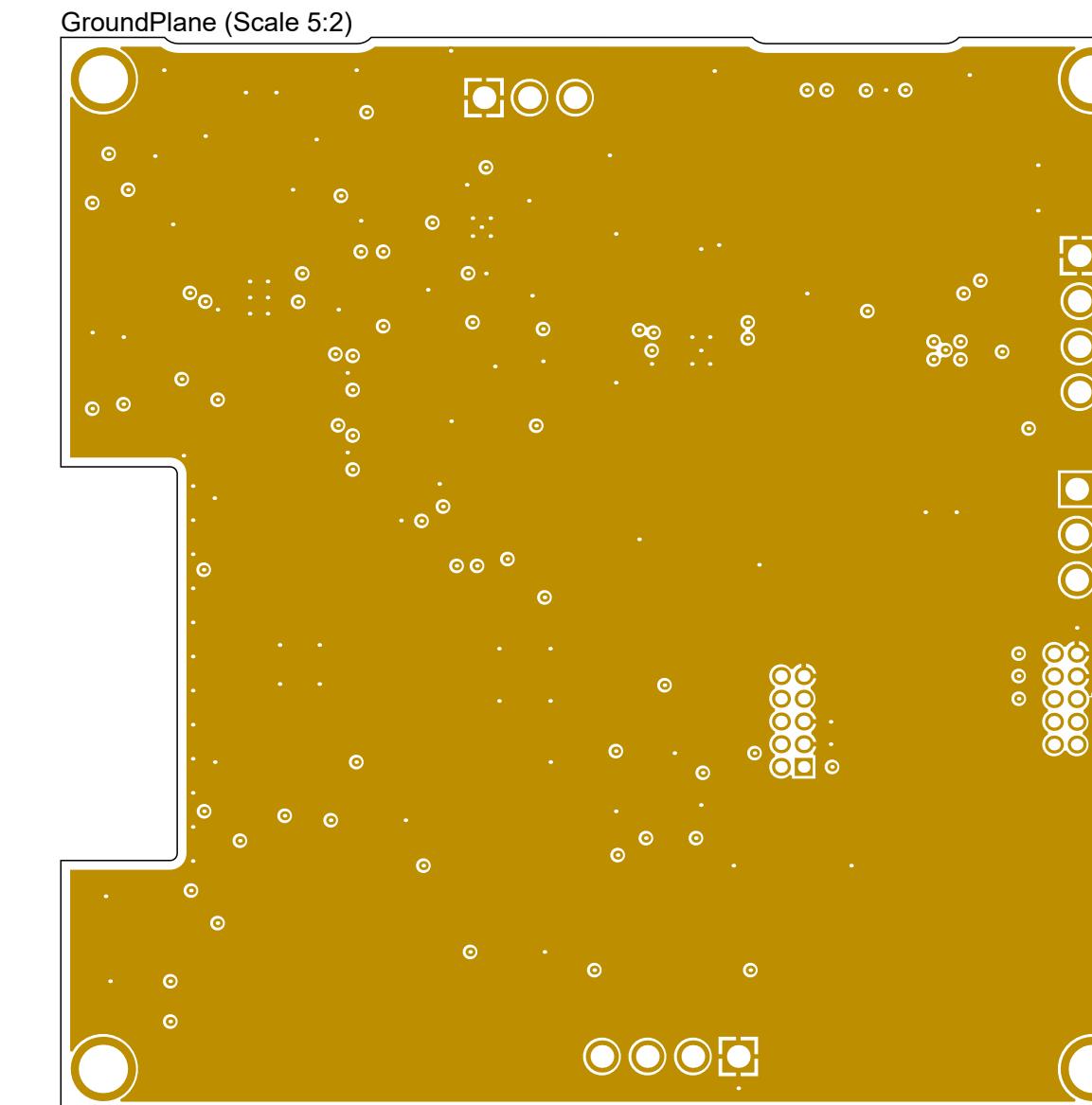
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| REVISIONS |  | DESCRIPTION | DATE | APPROVED |
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PART NO: =PCB\_PART\_NUMBER

APPROVALS DATE

ENGINEER: YG &amp; JC YG &amp;

DESIGNER: YG &amp; JC YG &amp;

CHECKER: =PCB\_CHECKER =PCB\_CHECKER

Reference Documents

BOM DOC: =DOC\_NO\_BOM

ASSY DOC: =DOC\_NO\_FAB\_DWG

SCH DOC: =DOC\_NO\_SCH\_DWG

NEXT ASSY USED ON PCB DOC: =PCB\_DWG\_NO

APPLICATION

**Altium**<sup>TM</sup>200 S  
33rd St  
Philadelphia  
PA, 19104

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE:  
ESE516  
PROJECTSIZE: CAGE CODE: DWG NO: REV:  
**B** =CAGE\_CODWG NO:  
=DOC\_NO\_ASSY\_.lfe

FILE NAME:

StarterBoardFabrication.PCBDwf

SCALE:

FILE NAME:

StarterBoardFabrication.PCBDwf

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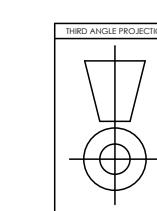
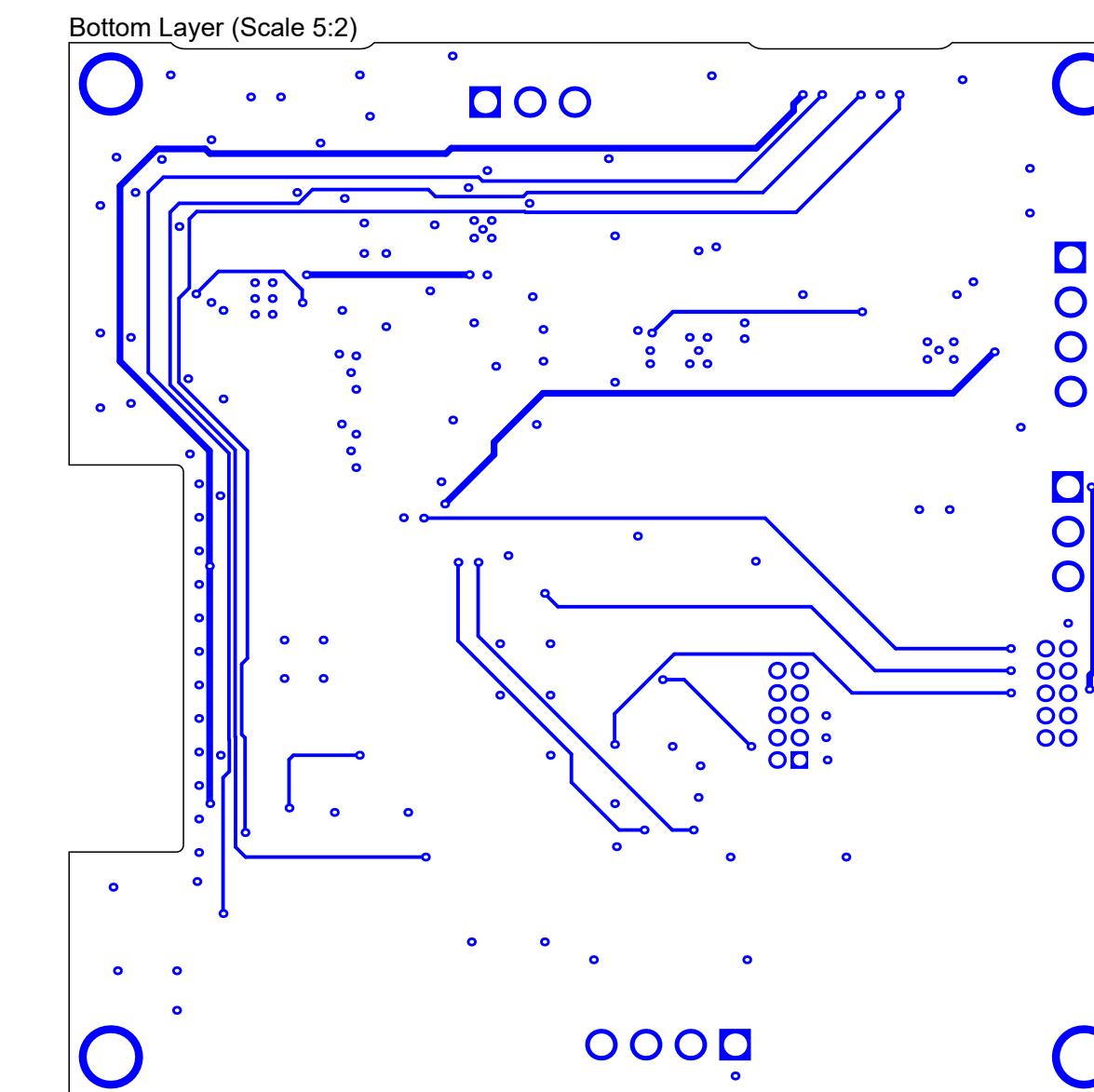
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PART NO: =PCB\_PART\_NUMBER

APPROVALS DATE

ENGINEER: YG &amp; JC YG &amp;

DESIGNER: YG &amp; JC YG &amp;

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Reference Documents

BOM DOC: =DOC\_NO\_BOM

ASSY DOC: =DOC\_NO\_FAB\_DWG

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NEXT ASSY USED ON PCB DOC: =PCB\_DWG\_NO

APPLICATION

200 S  
33rd St  
Philadelphia  
PA, 19104

**Altium**  
TM

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

ESE516  
PROJECT

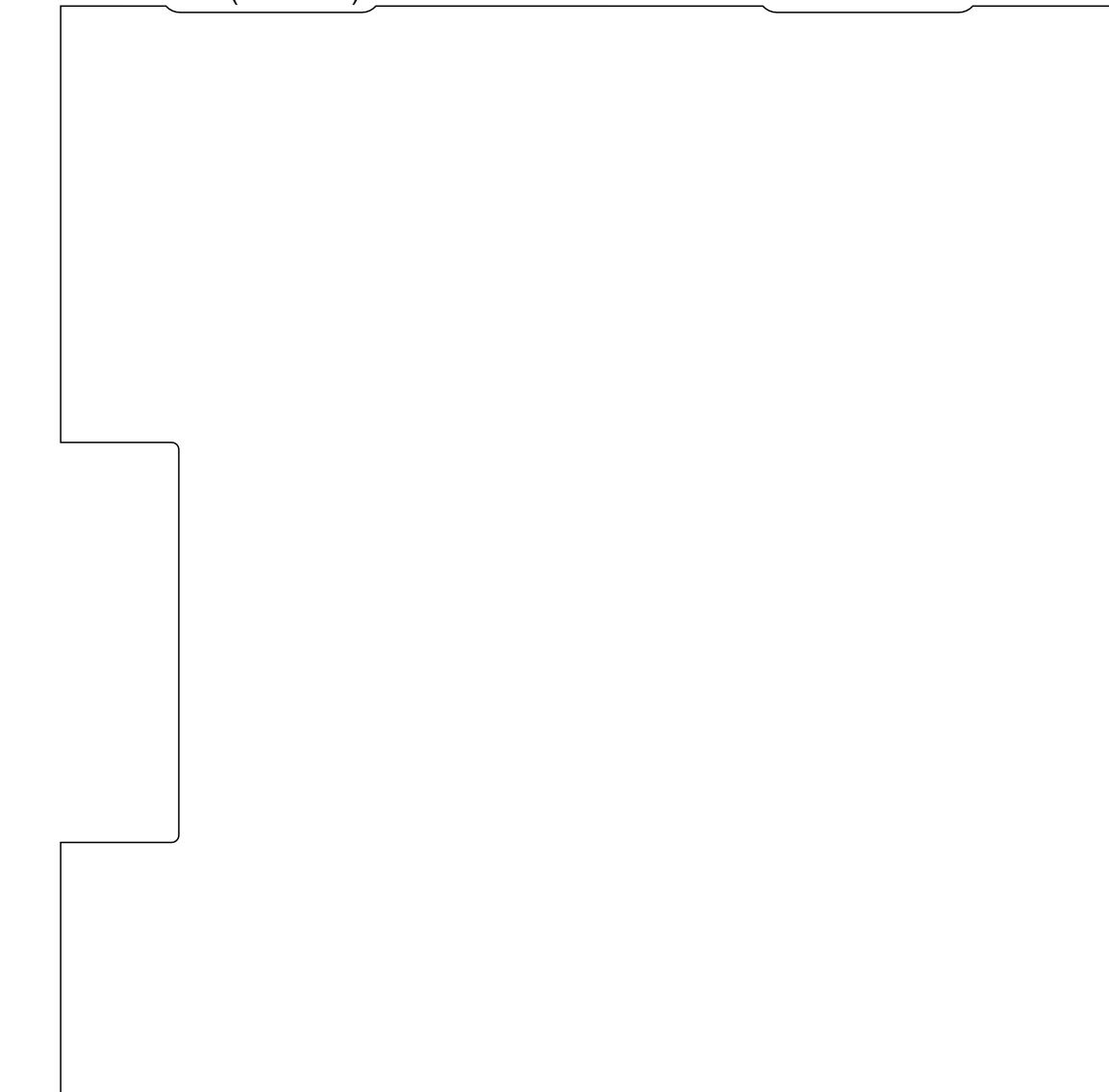
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Bottom Paste (Scale)



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| PART NO: =PCB_PART_NUMBER |                       |  |         |
| APPROVALS                 |                       | DATE                                       |         |
| ENGINEER:                 | YG & JC               | YG &                                       |         |
| DESIGNER:                 | YG & JC               | YG &                                       |         |
| CHECKER:                  | =PCB_CHECKER          | =PCB_CHECKER                               |         |
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| ASSY DOC:                 | =DOC_NO_FAB_DWG       |  |         |
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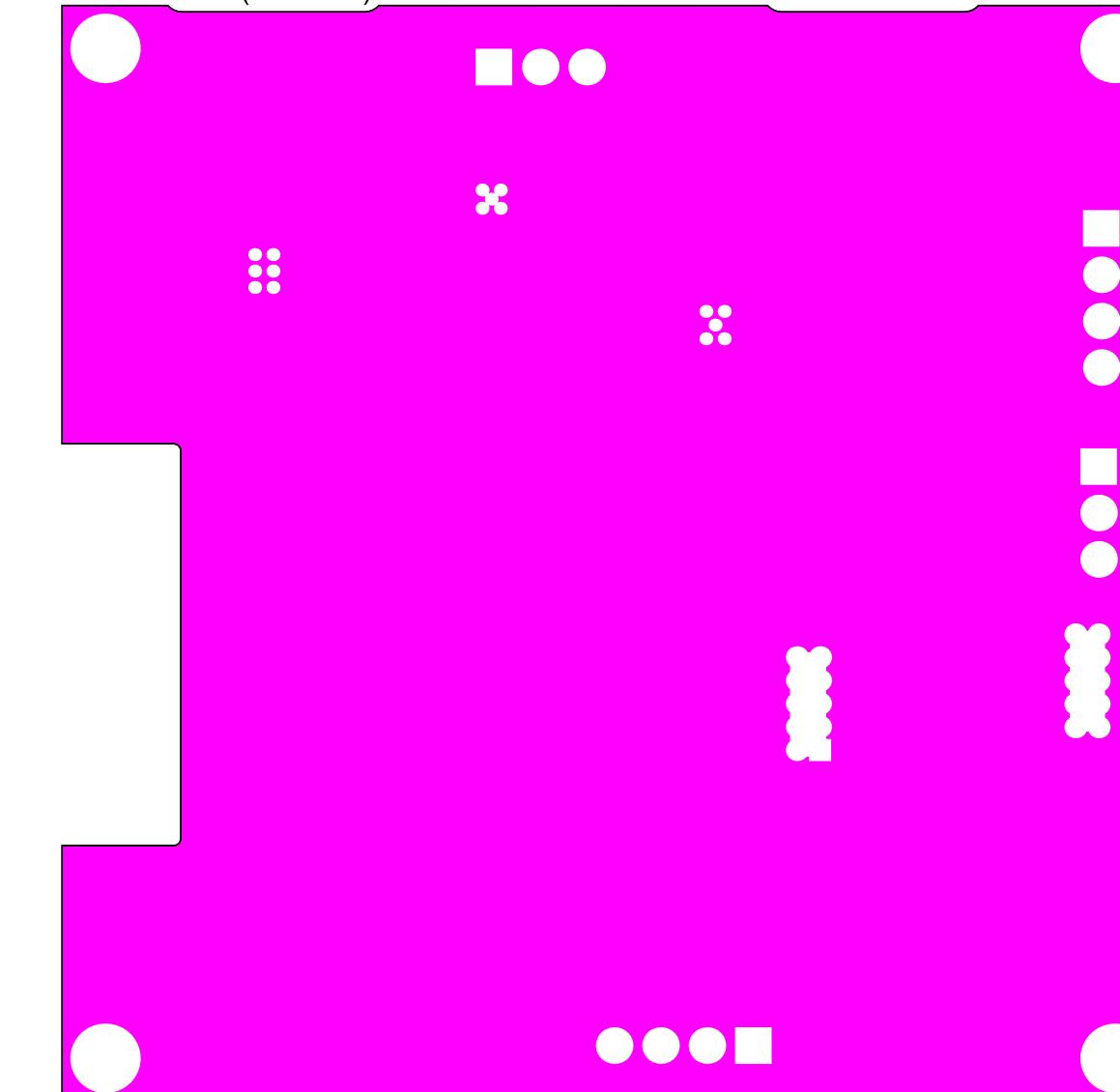
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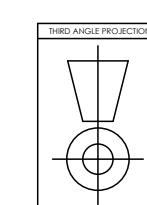
Bottom Solder (Scale)



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PART NO: =PCB PART NUMBER

|             |                                 |   |                     |   |                       |               |
|-------------|---------------------------------|---|---------------------|---|-----------------------|---------------|
| APPROVALS   | DATE                            | <b>Altium™</b>                            |                     | 200 S<br>33rd St<br>Philadelphia<br>PA, 19104 |                       |               |
| ENGINEER:   | YG & JC                         | YG &                                      |                     |   |                       |               |
| DESIGNER:   | YG & JC                         | YG &                                      |                     |   |                       |               |
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| BOM DOC:    | TITLE:<br><br>ESE516<br>PROJECT |   |                     |   |                       |               |
| ASSY DOC:   | =DOC_NO_BOM                     |   |                     |   |                       |               |
| SCH DOC:    | =DOC_NO_FAB_DWG                 |   |                     |   |                       |               |
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| SCALE:      |                                 | FILE NAME: StarterBoardFabrication.PCBDwf |                     |   | SHEET: 11 OF 12       |               |



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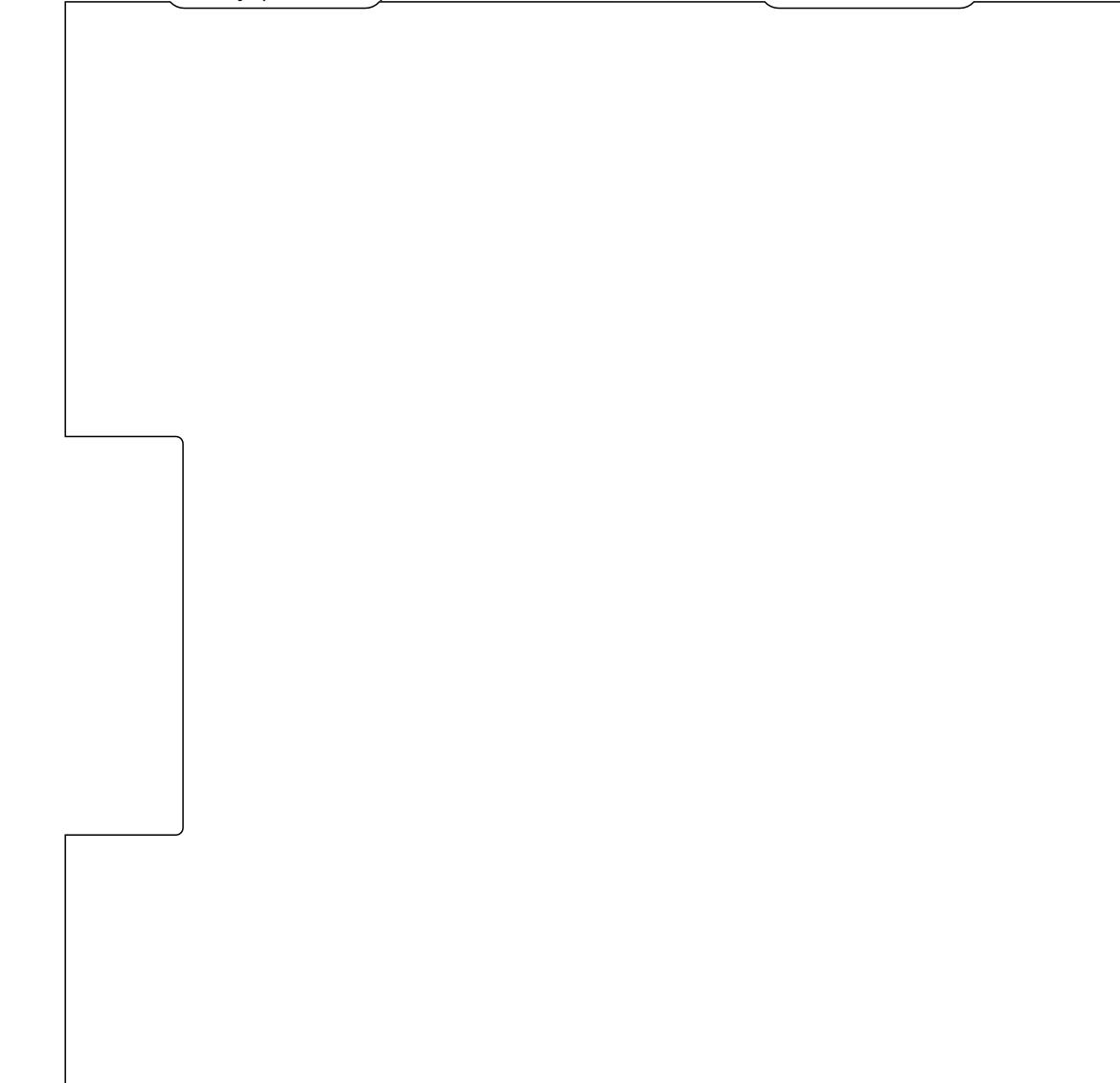
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Bottom Overlay (Scale 5:2)



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DWG NO:  
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|                           |                 |              |             |  |
|---------------------------|-----------------|--------------|-------------|--|
| PART NO: =PCB_PART_NUMBER |                 | APPROVALS    | DATE        | <b>Altium</b><br>200 S<br>33rd St<br>Philadelphia<br>PA, 19104 |
| ENGINEER:                 | YG & JC         | YG &         |             |  |
| DESIGNER:                 | YG & JC         | YG &         |             |  |
| CHECKER:                  | =PCB_CHECKER    | =PCB_CHECKER |             |  |
| Reference Documents       |                 |              |             |  |
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| ASSY DOC:                 | =DOC_NO_FAB_DWG |              |             |  |
| SCH DOC:                  | =DOC_NO_SCH_DWG |              |             |  |
| NEXT ASSY                 | USED ON         | PCB DOC:     | =PCB_DWG_NO |  |
| APPLICATION               |                 | SCALE:       | FILE NAME:  | StarterBoardFabrication.PCBDwf                                 |
|                           |                 |              |             | Sheet: 12 of 12  |

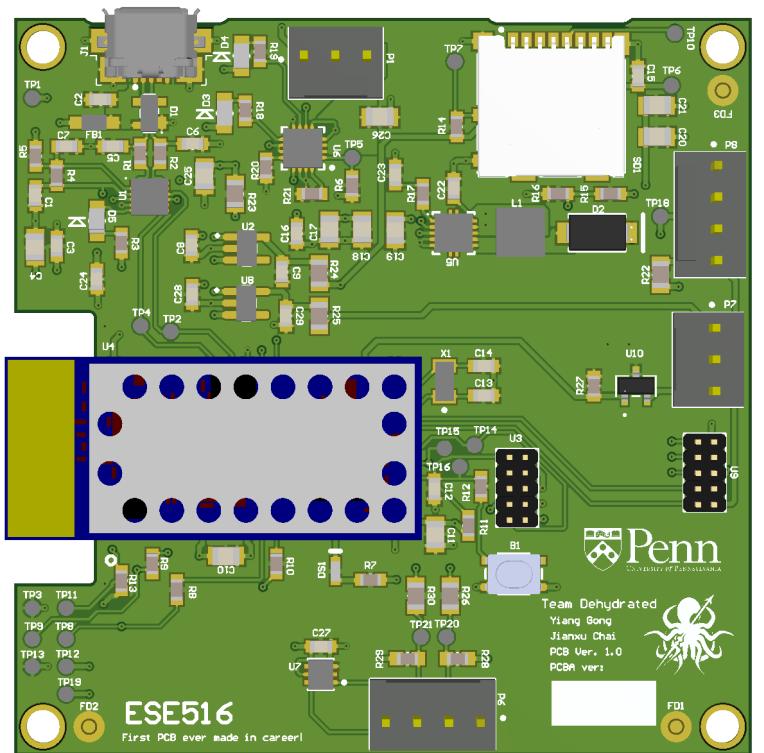
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| REV STATUS OF SHEETS      | SHEET |           |
|                           |       |           |
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| REVISIONS   |      |          |
|-------------|------|----------|
| DESCRIPTION | DATE | APPROVED |
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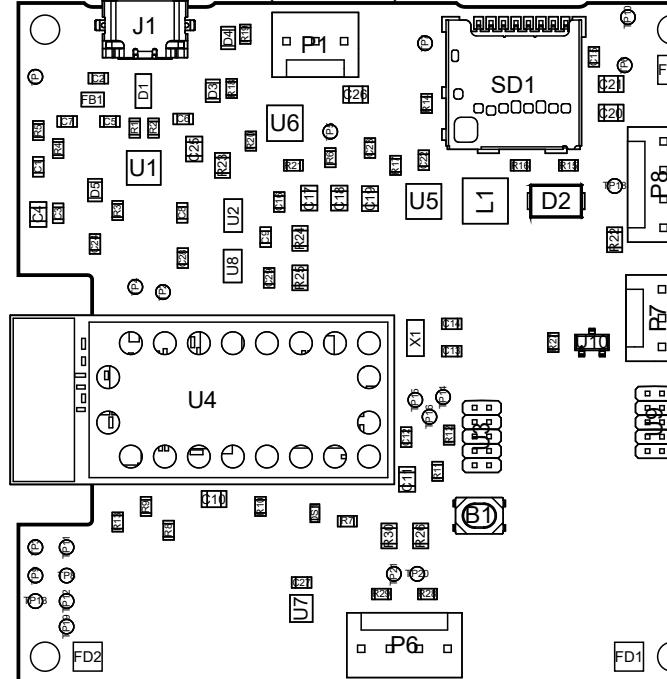
NOTES:

1. THIS ITEM IS ELECTROSTATIC SENSITIVE, AND NEED TO BE HANDLED ACCORDING.
2. WORKMANSHIP WILL CONFORM TO IPC-610 CLASS 2, IPC 7711 WILL APPLY TO ALL REQUIRED REWORK OR MODIFICATION.

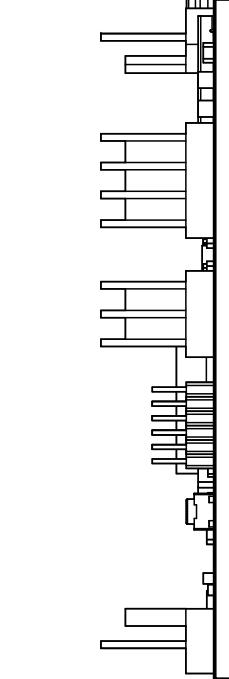
Realistic View



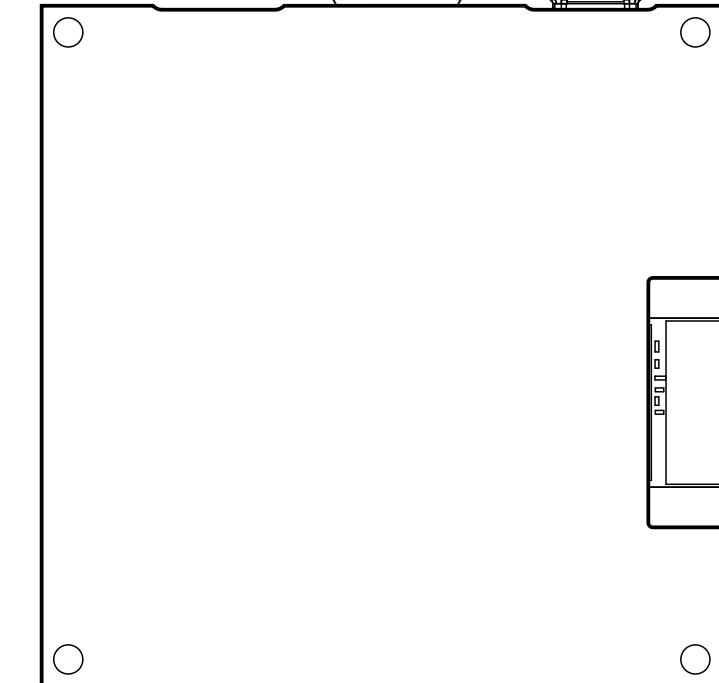
View from Top side (Scale 3:2)



View from Right side (Scale 3:2)



View from Bottom side (Scale 3:2)



PART NO: =PCB\_PART\_NUMBER

APPROVALS DATE

ENGINEER: YG & JC YG &

DESIGNER: YG & JC YG &

CHECKER: =PCB\_CHECKER =PCB\_CHECKER

Reference Documents

BOM DOC: =DOC\_NO\_BOM

ASSY DOC: =DOC\_NO\_FAB\_DWG

SCH DOC: =DOC\_NO\_SCH\_DWG

PCB DOC: =PCB\_DWG\_NO

APPLICATION

**Altium**  
2005  
33rd St  
Philadelphia  
PA, 19104

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE:

ESE516

PROJECT

SIZE: CAGE CODE: DWG NO:

**B** =CAGE\_CO

REV: .lfe

SCALE: FILE NAME: StarterBoardAssembly.PCBDwf SHEET: 1 OF 3

A

B

C

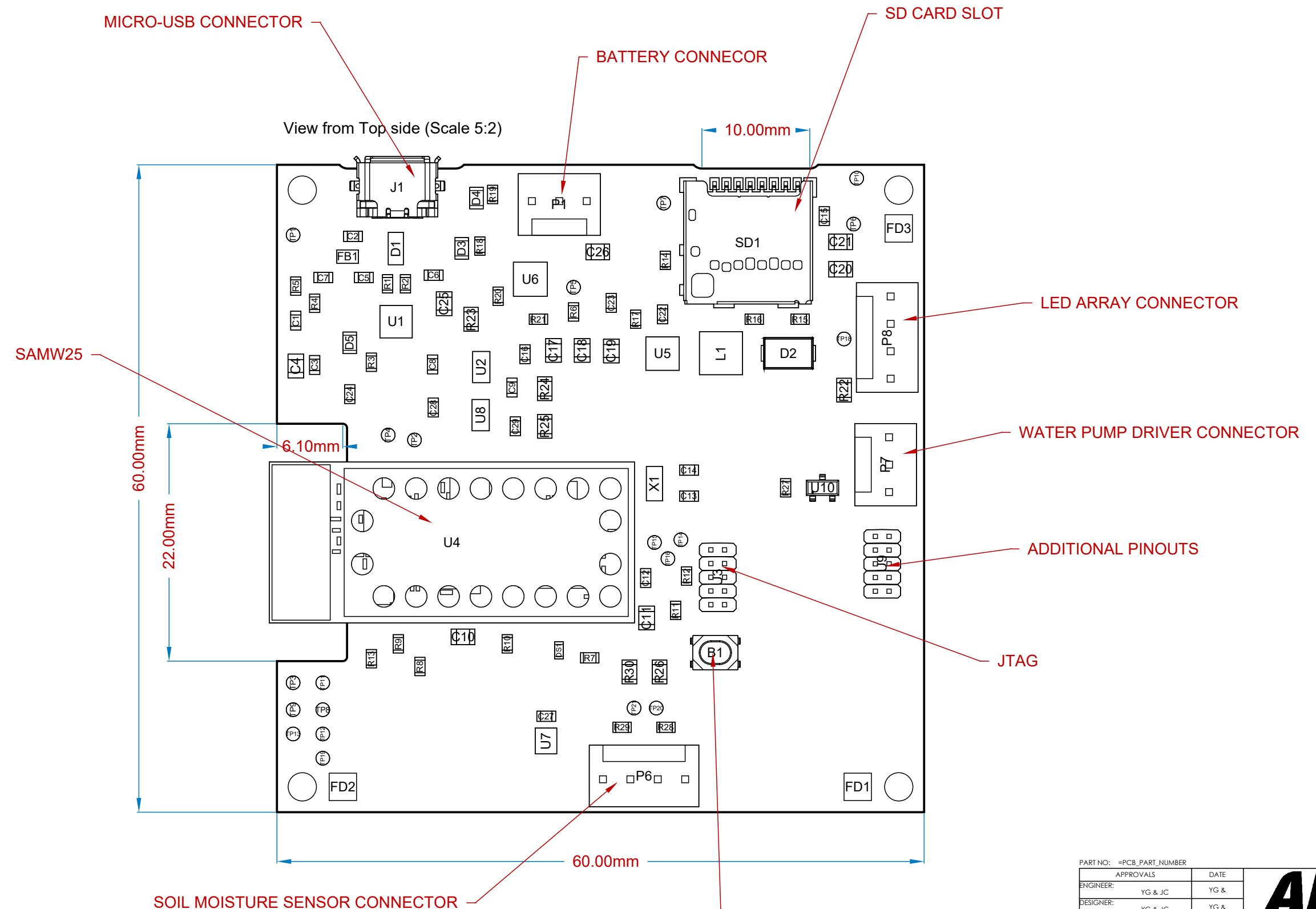
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E

F

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| REV STATUS OF SHEETS |  | REV |  |  |  |  |  |
|----------------------|--|-----|--|--|--|--|--|
| SHEET                |  |     |  |  |  |  |  |
|                      |  |     |  |  |  |  |  |
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|                      |  |     |  |  |  |  |  |



PART NO: =PCB\_PART\_NUMBER

APPROVALS DATE

ENGINEER: YG &amp; JC

DESIGNER: YG &amp; JC

CHECKER: =PCB\_CHECKER

=PCB\_CHECKER

Reference Documents

BOM DOC: =DOC\_NO\_BOM

ASSY DOC: =DOC\_NO\_FAB\_DWG

SCH DOC: =DOC\_NO\_SCH\_DWG

NEXT ASSY USED ON

PCB DOC: =PCB\_DWG\_NO

APPLICATION

**Altium**  
™200S  
33rd St  
Philadelphia  
PA, 19104

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE: ESE516

PROJECT

SIZE: CAGE CODE: DWG NO:

B =CAGE\_CO

REV:

FILE NAME: StarterBoardAssembly.PCBDwf

SCALE: SHEET: 2 OF 3

A

B

C

D

E

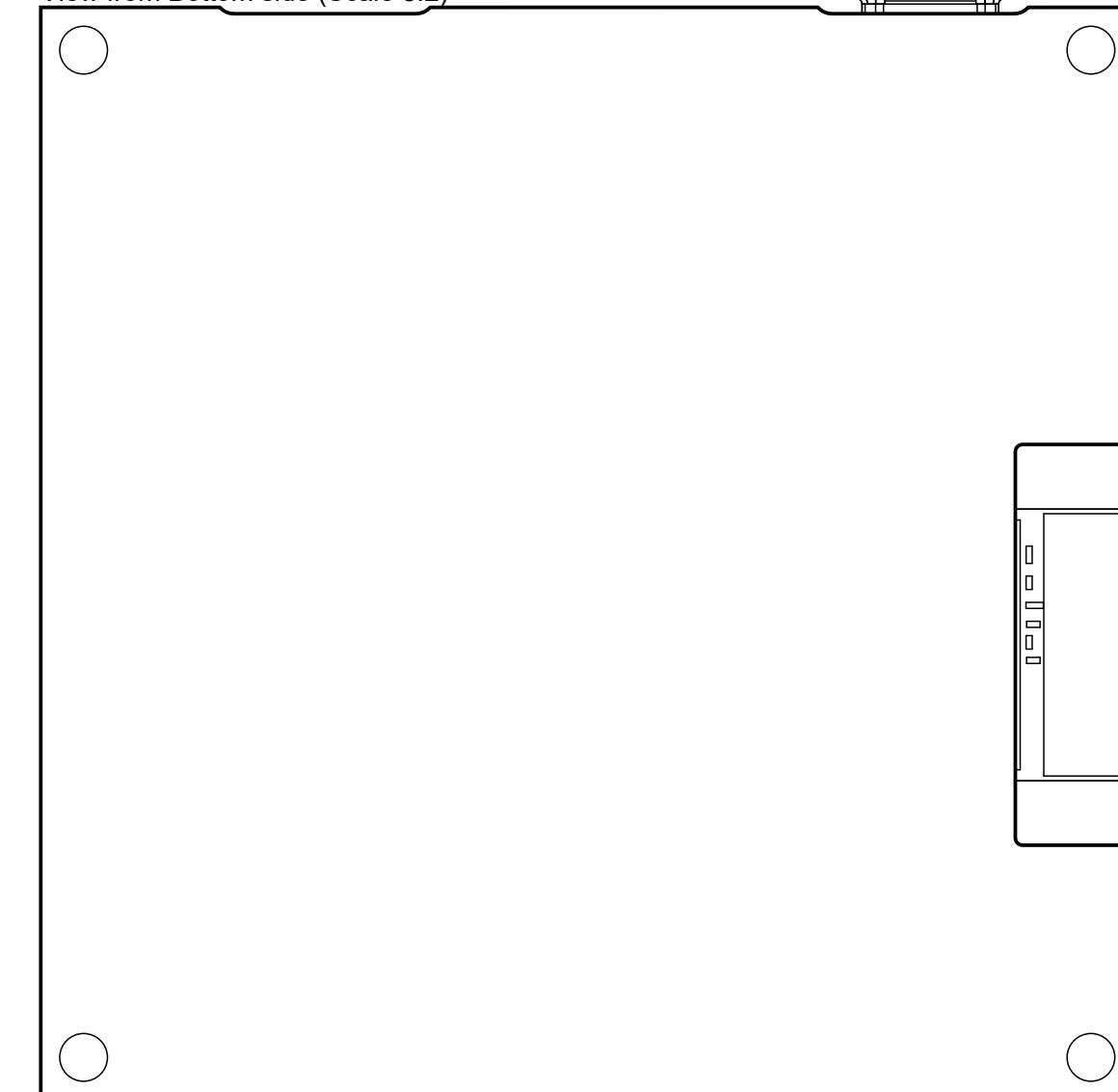
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| DWG NO:                 |       | =DOC_NO_ASSY_DWG | REV: | .lfe |
|-------------------------|-------|------------------|------|------|
| REV STATUS<br>OF SHEETS | SHEET |                  |      |      |
|                         |       |                  |      |      |
|                         |       |                  |      |      |
|                         |       |                  |      |      |
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| REVISIONS |  | DESCRIPTION | DATE | APPROVED |
|-----------|--|-------------|------|----------|
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|           |  |             |      |          |
|           |  |             |      |          |
|           |  |             |      |          |

View from Bottom side (Scale 5:2)



|                           |                     |              |             |   |
|---------------------------|---------------------|--------------|-------------|---|
| PART NO: =PCB_PART_NUMBER |                     | APPROVALS    | DATE        | <b>Altium</b><br>200S<br>33rd St<br>Philadelphia<br>PA, 19104 |
| ENGINEER:                 | YG & JC             | YG &         |             |   |
| DESIGNER:                 | YG & JC             | YG &         |             |   |
| CHECKER:                  | =PCB_CHECKER        | =PCB_CHECKER |             |   |
| BOM DOC:                  | Reference Documents |              |             |   |
| ASSY DOC:                 | =DOC_NO_BOM         |              |             |   |
| SCH DOC:                  | =DOC_NO_FAB_DWG     |              |             |   |
| NEXT ASSY                 | USED ON             | PCB DOC:     | =PCB_DWG_NO |   |
| APPLICATION               |                     | SCALE:       | FILE NAME:  | StarterBoardAssembly.PCBDwf                                   |
|                           |                     |              |             | Sheet: 3 of 3   |

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: ESE516 PROJECT

SIZE: CAGE CODE: DWG NO: REV:  
**B** =CAGE\_CO