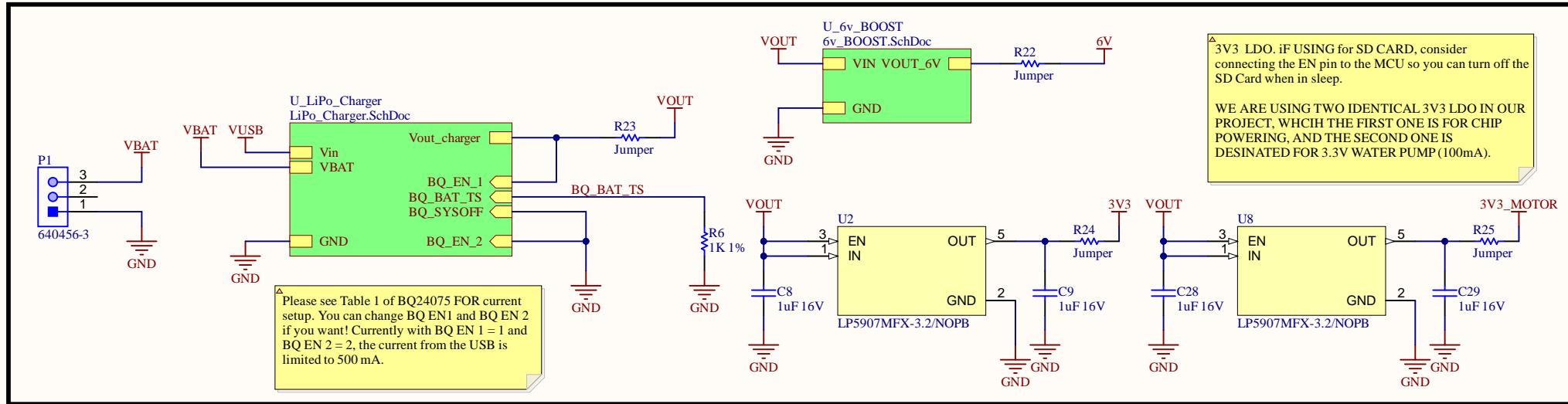


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REVISION	DESCRIPTION	DATE	APPROVED

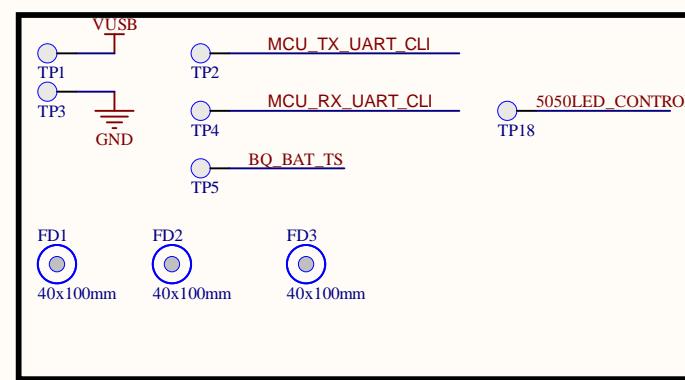
POWER SUPPLY - CHANGE ME TO YOUR POWER ARCHITECTURE



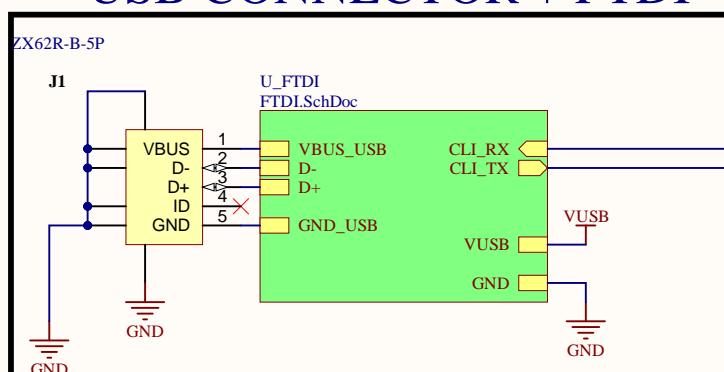
NOTES

In my project, the 4 components I have are the ambient light sensor, water pump, soil moisture sensor, and a led module. Within that range, the only component that will be soldered to board is the ambient light sensor. So I created a subsheet for that module and created three headers for the rest three components.

TEST POINTS AND FIDUCIALS

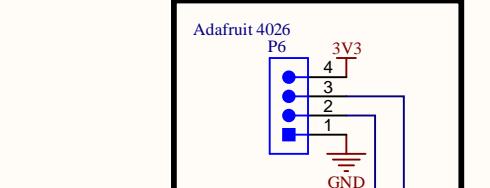


USB CONNECTOR + FTDI

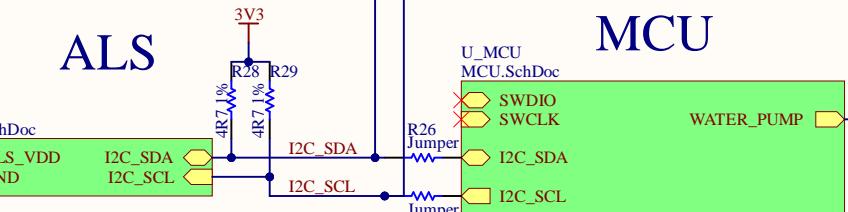


NOTE:
The FTDI Chip is an useful chip that allows us to convert USART messages into USB signals. It allows us to connect the MCU directly to the USB port of a computer and use the serial terminal (it is the same bridge used on the SAMW25 Xplained Board). The FTDI device also contains protection circuitry for the USB.

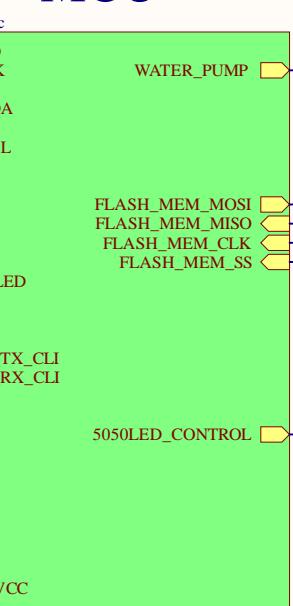
SOIL MOISTURE SENSOR HEADER



ALS

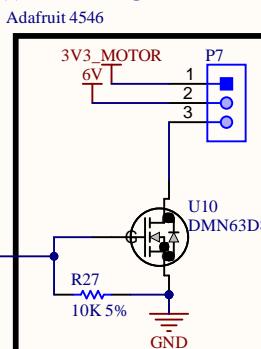


MCU



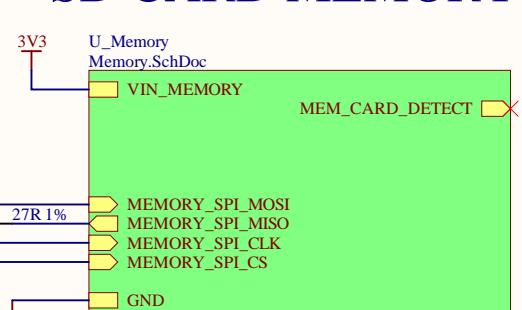
THIS HEADER IS PUT FOR SAVING PINS FOR LATER USE. THOSE PINS ARE NOT USED IN OUR CURRENT DESIGN.
Note: Only the required pins are exposed for the MCU. Remember to add the ports for the pins you need to be exposed!

WATER PUMP HEADER



Note: I put both a 3.3V and 6V to the header for convanienty of switching water pump.
I added a pull down resistor for the NMOS

SD CARD MEMORY



Note: This is the SD Card, which we will use for our project. PLEASE DO NOT ERASE! Connect a 3V3 rail to this SD Card.

The SD CARD needs 100 mA (worst case, most common is 30mA). If your existing power supply cannot handle this added current, please use the 3V3 LDO found in this project to power your SD Card.

APPROVALS	DATE	PROJECT	ENG:	Penn Engineering	200 S 33rd St
		ESE516	DSN:	UNIVERSITY OF PENNSYLVANIA	Philadelphia PA, 19104
		PROJECT REVISION:	DOCUMENT REVISION:		DESIGN ITEM:
		TITLE			
		Main Schematics			
		REFERENCE DOCUMENTS			
		BOM:			
		ASSY DWG:			
		FAB DWG:			
		PCB DWG:			
SCALE:	FILE NAME	MAIN.SchDoc	SHEET	1	OF 7

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DWG. NO.	1.0 2	REV. SHT.	REVISION	DESCRIPTION	DATE	APPROVED

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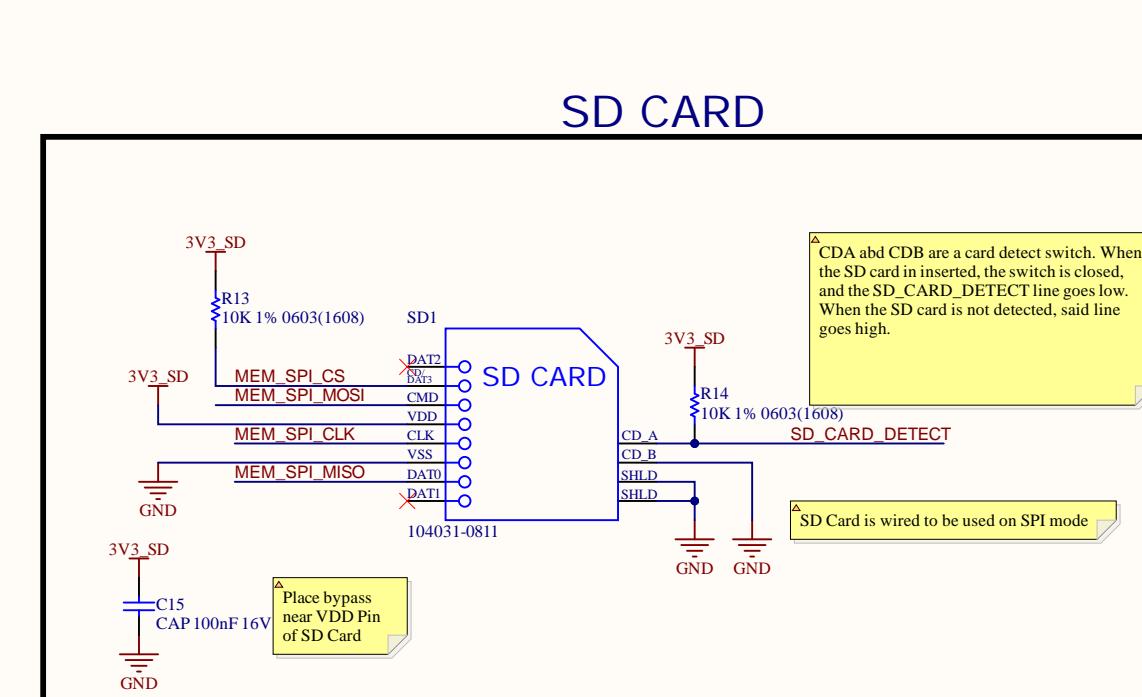
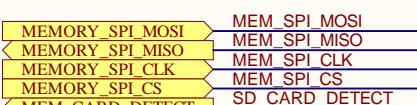
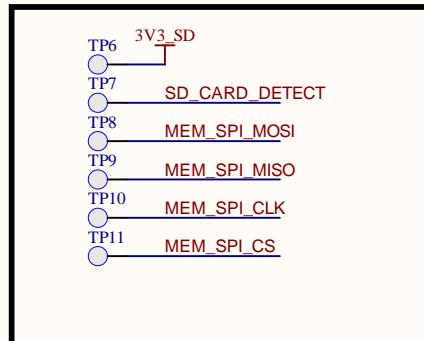
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TESTPOINTS



APPROVALS	DATE	PROJECT	Penn Engineering	200 S 33rd St Philadelphia PA, 19104
ENG: Yiang Gong & Jianxu Chai		ESE516		
DSN: Yiang Gong & Jianxu Chai		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:
CHK: Yiang Gong & Jianxu Chai				
REFERENCE DOCUMENTS		TITLE	Memory	
BOM:		ASSY DWG:		SIZE CAGE CODE DWG NO.
		FAB DWG:		
		PCB DWG:		REV 1.0
			SCALE: FILE NAME Memory.SchDoc	SHEET 2 OF 7

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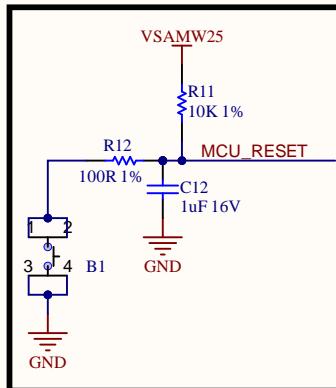
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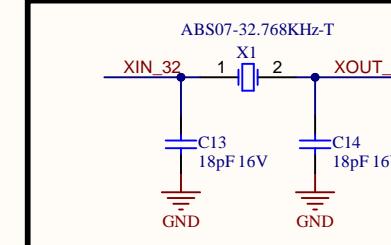
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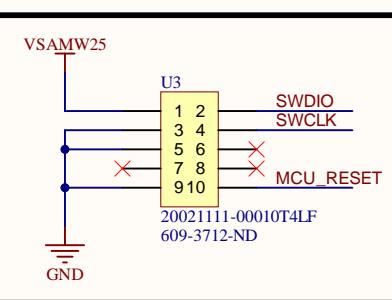
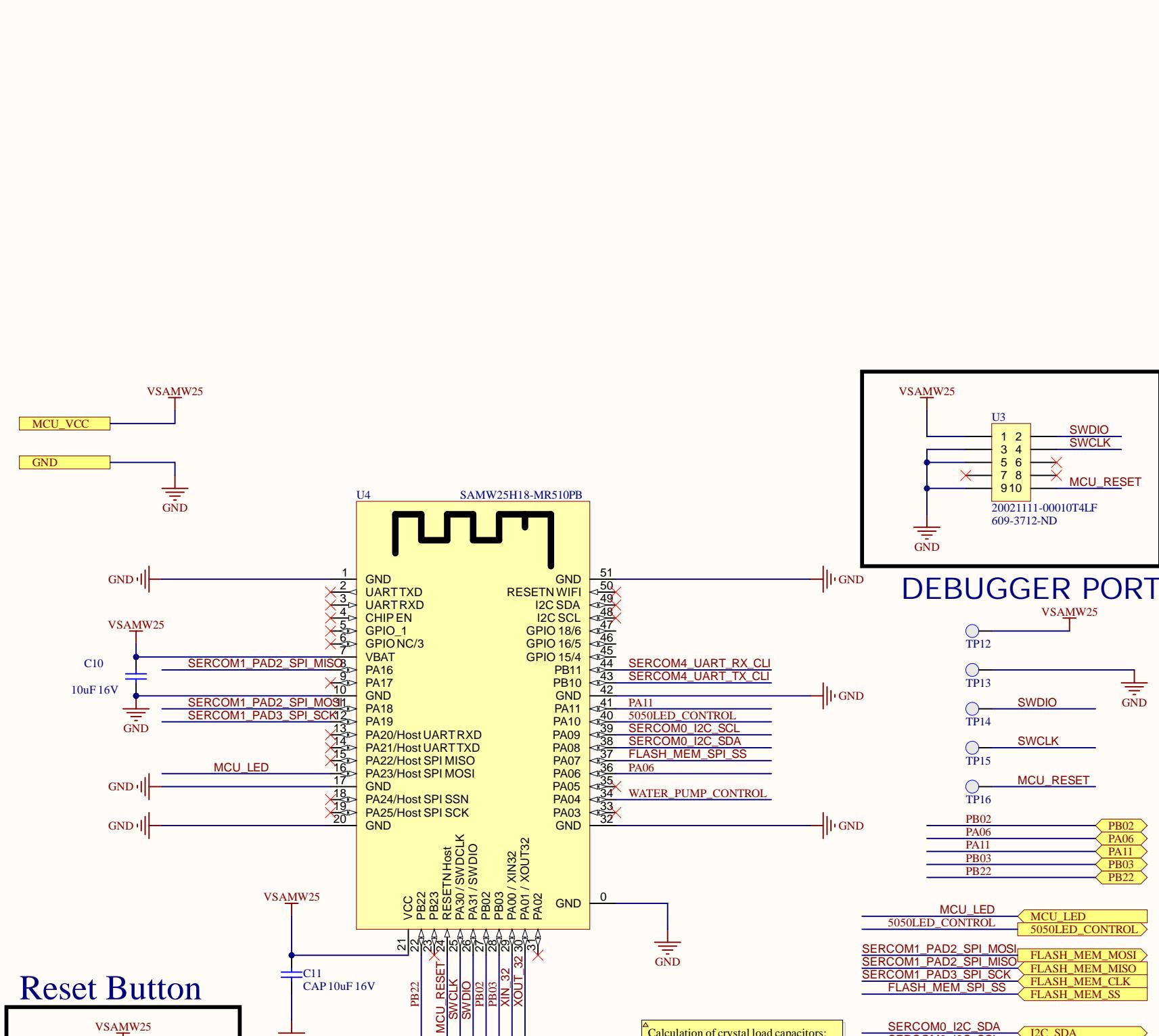
Reset Button



32.768 Crystal



Calculation of crystal load capacitors:
 $C_{ext} = 2 \times (C_{crystal} - C_{para} - C_{pcb})$
 Ccrystal = 12.5pF (from crystal datasheet)
 Cpara = 3.15pF (from MCU datasheet)
 Cpcb = 0.5pF (estimate)
 $C_{ext} = 2 \times (12.5pF - 3.15pF - 0.5pF) = 17.7pF$



DEBUGGER PORT

APPROVALS	DATE	PROJECT	ENG:	Penn Engineering	200 S 33rd St Philadelphia PA, 19104
		ESE516	Yiang Gong & Jianxu Chai		
		PROJECT REVISION:	DOCUMENT REVISION:		
		TITLE			
		MCU			
BOM:		REFERENCE DOCUMENTS			
ASSY DWG:		PCB DWG:			
FAB DWG:		SCALE:	FILE NAME	MCU.SchDoc	SHEET 3 OF 7
PCB DWG:		SIZE	CAGE CODE	DWG NO.	REV 1.0

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DWG. NO.	1.0 4	REV. SHT.	REVISION	DESCRIPTION	DATE	APPROVED

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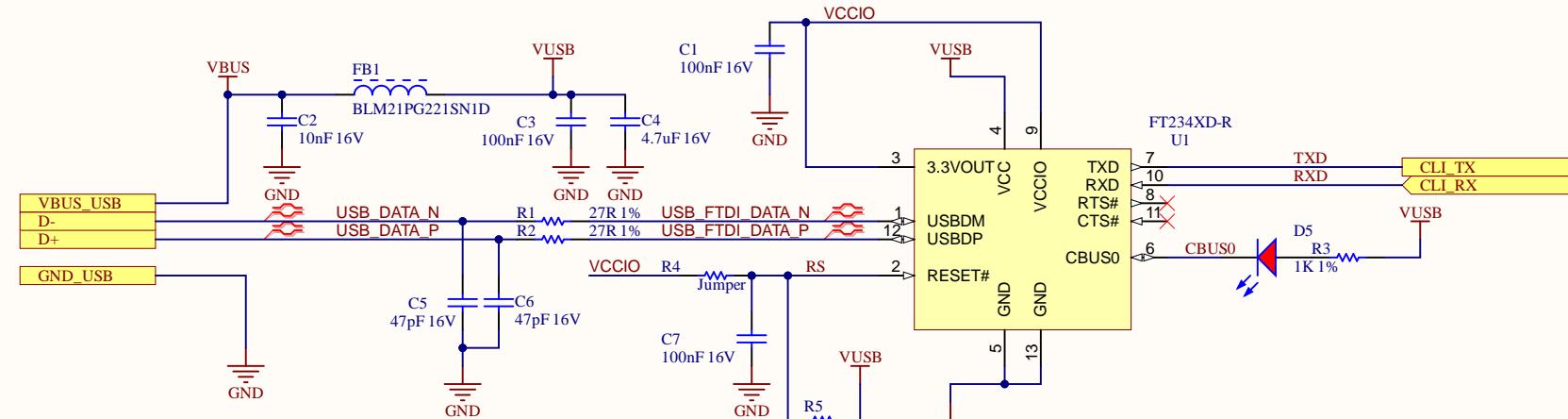
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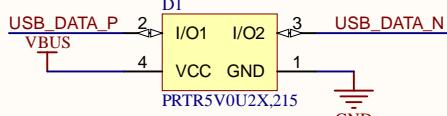
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FTDI CHIP



USB ESD PROTECTION



APPROVALS	DATE	PROJECT	Penn Engineering	200 S 33rd St Philadelphia PA, 19104
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DSN: Yiang Gong & Jianxu Chai		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:
CHK: Yiang Gong & Jianxu Chai				
BOM:		TITLE	FTDI	
ASSY DWG:		SIZE	CAGE CODE	DWG NO.
FAB DWG:		B		1.0
PCB DWG:		SCALE:	FILE NAME	FTDI.SchDoc

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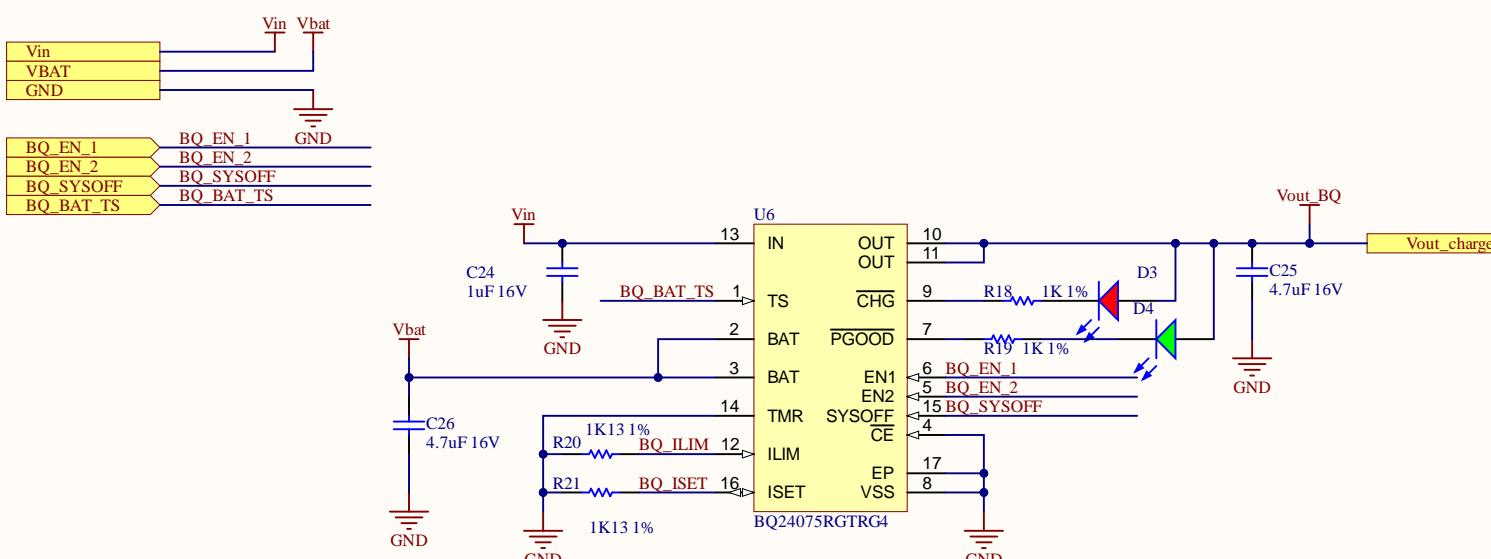
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DSN: Yiang Gong & Jianxu Chai		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:
CHK: Yiang Gong & Jianxu Chai				
BOM:		TITLE	LiPO_Chaerger	
ASSY DWG:		SIZE	CAGE CODE	DWG NO.
FAB DWG:		B		
PCB DWG:		SCALE:	FILE NAME	LiPo_Charger.SchDoc
			SHEET	5 OF 7

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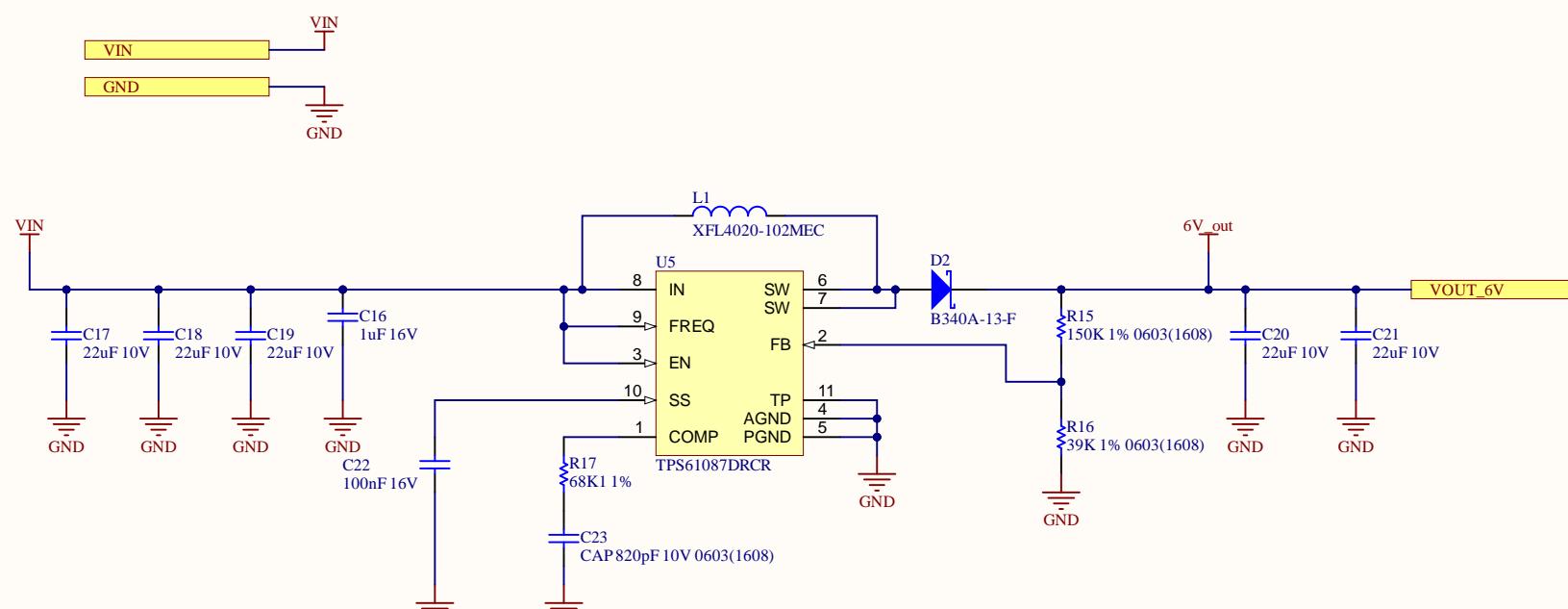
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TPS61087DSCR
VIN: 3.3V to 5.5V
OUT: 6V up to 1A

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ENG: Yiang Gong & Jianxu Chai		ESE516		
DSN: Yiang Gong & Jianxu Chai				
CHK: Yiang Gong & Jianxu Chai				
REFERENCE DOCUMENTS				
BOM:				
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FAB DWG:				
PCB DWG:		SCALE:	FILE NAME	6v_BOOST.SchDoc
				SHEET 6 OF 7

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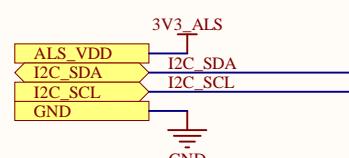
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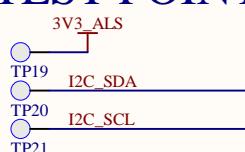
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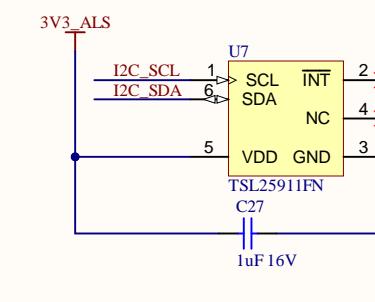
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TEST POINTS



AMBIENT LIGHT SENSOR

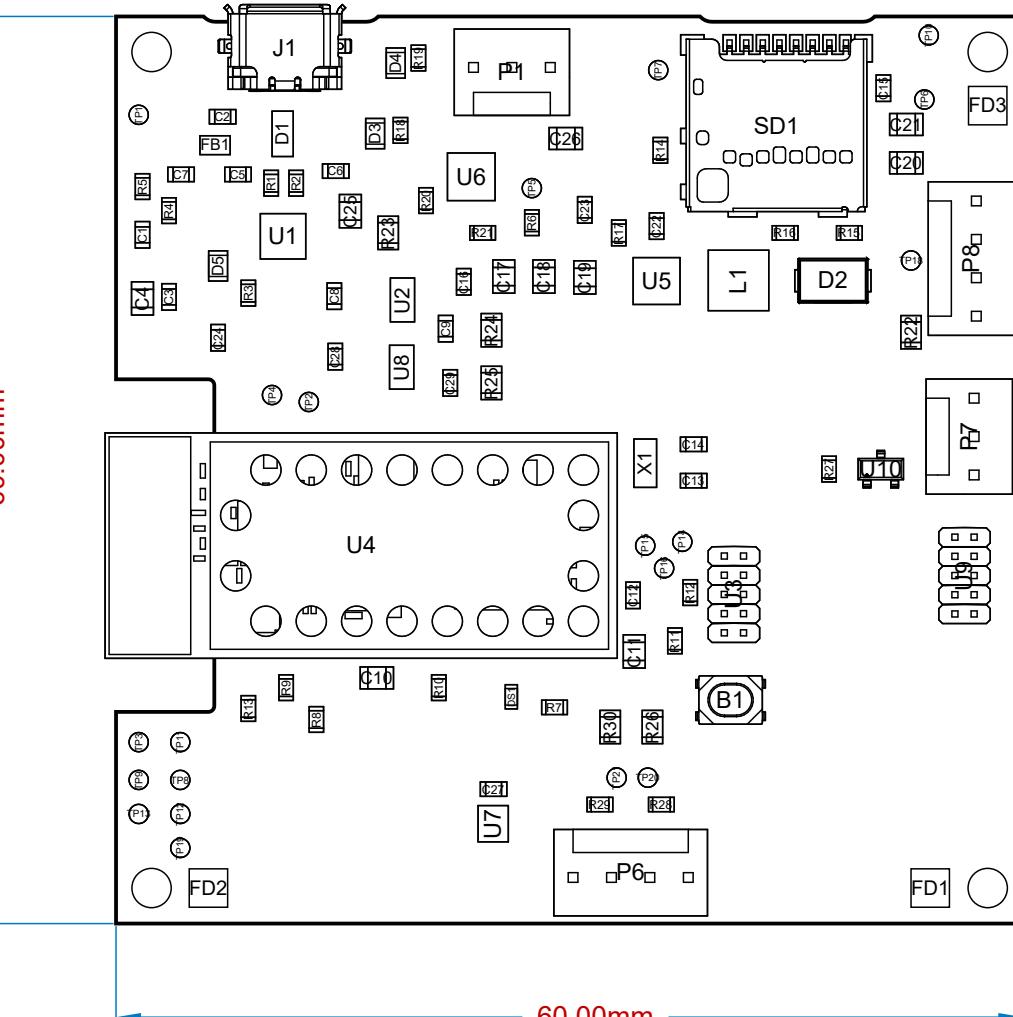


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DSN: Yiang Gong & Jianxu Chai		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:
CHK: Yiang Gong & Jianxu Chai				
BOM:		TITLE	Ambient Light Sensor	
REFERENCE DOCUMENTS				
ASSY DWG:		SIZE	CAGE CODE	DWG NO.
FAB DWG:		B		
PCB DWG:		SCALE:	FILE NAME	ALS.SchDoc
			SHEET	7 OF 7

Manufacture Notes:

Four (4) layers
Dimensions: 60mm x 60mm
Thickness: 0.062"
Material: FR4
Surface Finish: ENEPIG
Minimum Hole Diameter: 8 mils
Minimum Trace: 6 mils
Minimum Distance between Copper features: 10 mils
Solder Mask Color: Red

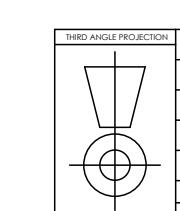
View from Top side (Scale 2:1)



Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Surface Material	Top Overlay			Legend	GTO
	Copper	Top Solder	0.03mm	Solder Resist	Solder Mask	GTS
		Top Layer	0.04mm		Signal	GTL
	Prepreg		0.33mm	PP-006	Dielectric	
	CF-004	GroundPlane	0.02mm		Signal	G1
	Core		0.71mm	Core-009	Dielectric	
	CF-004	PowerPlane	0.02mm		Signal	G2
	Prepreg		0.33mm	PP-006	Dielectric	
	Copper	Bottom Layer	0.04mm		Signal	GBL
	Surface Material	Bottom Solder	0.03mm	Solder Resist	Solder Mask	GBS
		Bottom Overlay			Legend	GBO

Total thickness: 1.53mm



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: YG & JC

DESIGNER: YG & JC

CHECKER: =PCB_CHECKER

=PCB_CHECKE

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

PCB DOC: =PCB_DWG_NO

APPLICATION

Altium
TM

200 S
33rd St
Philadelphia
PA, 19104

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE: ESE516

PROJECT

SIZE: CAGE CODE: DWG NO:

B =CAGE_CO

REV:

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B

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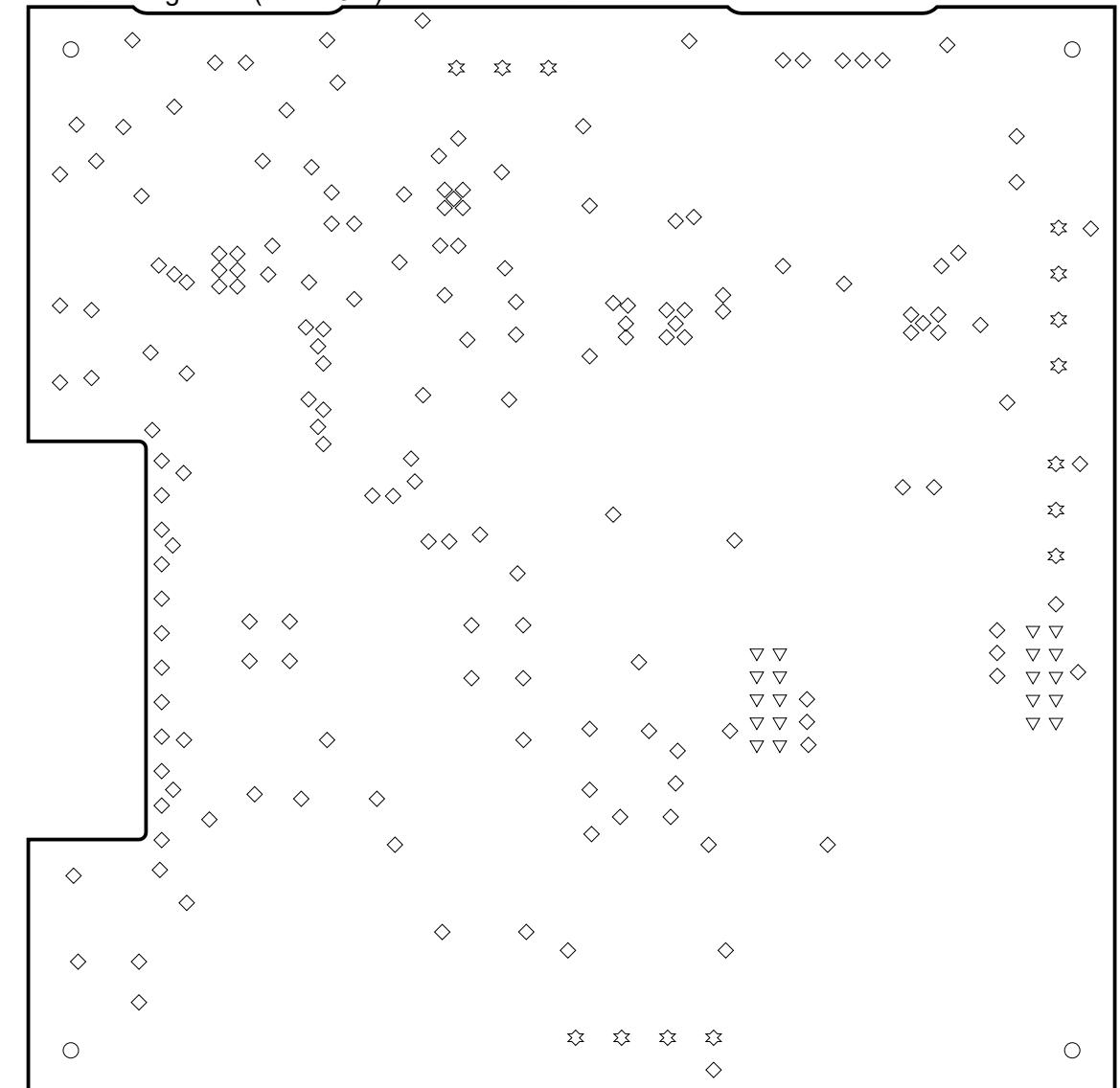
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SHEET										

REVISIONS		DESCRIPTION	DATE	APPROVED

Drill Table

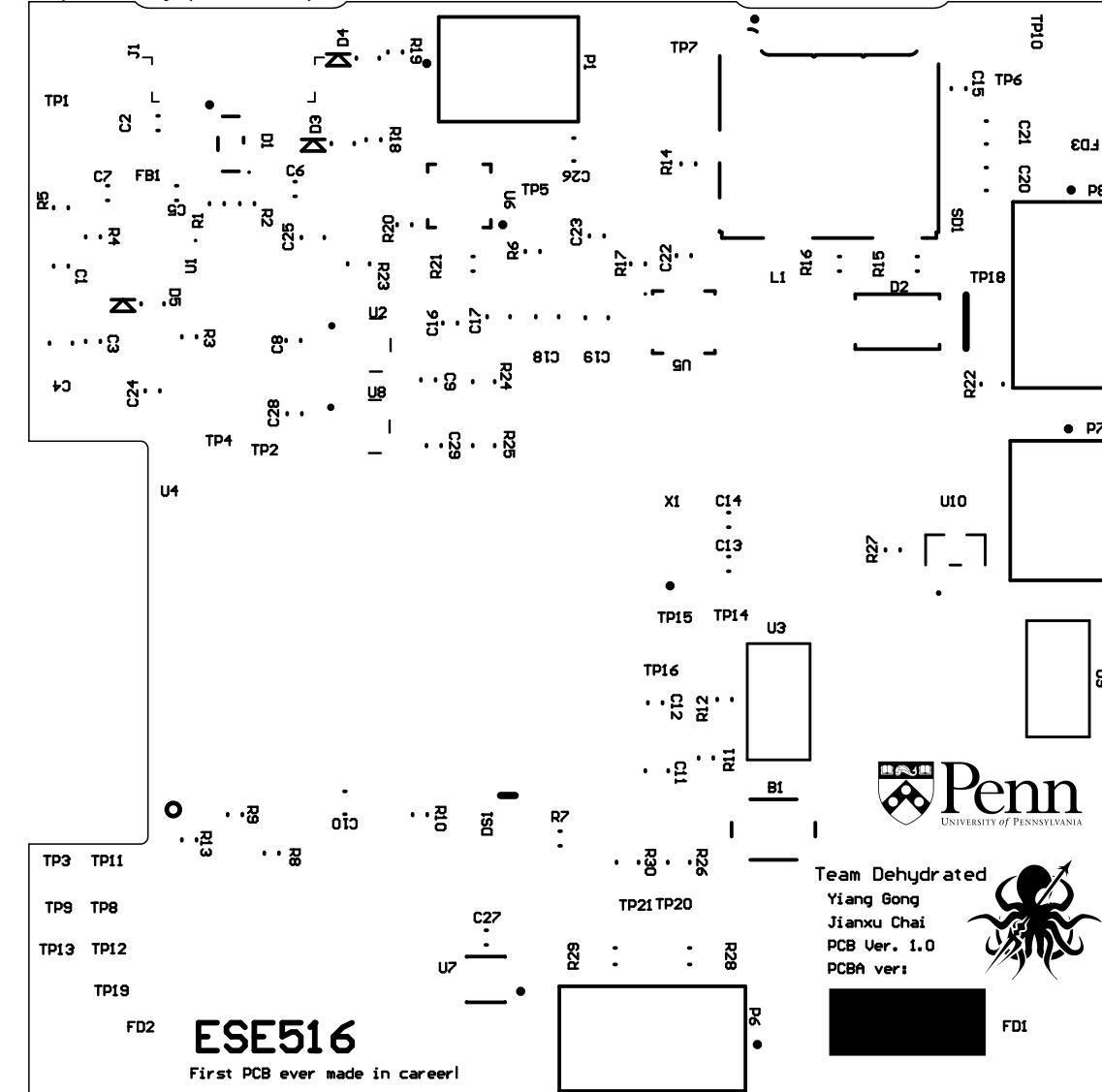
Symbol	Count	Hole Size	Plated	Hole Tolerance
◇	177	0.20mm	Plated	
▽	20	0.65mm	Plated	
❖	14	1.27mm	Plated	
○	4	2.70mm	Plated	
215 Total				

Drill Drawing View (Scale 5:2)



PART NO: =PCB_PART_NUMBER		APPROVALS	DATE	Altium 200 S 33rd St Philadelphia PA, 19104
ENGINEER:	YG & JC	YG &		
DESIGNER:	YG & JC	YG &		
CHECKER:	=PCB_CHECKER	=PCB_CHECKER		
Reference Documents				
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ASSY DOC:	=DOC_NO_FAB_DWG			
SCH DOC:	=DOC_NO_SCH_DWG			
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APPLICATION				
SIZE: B	CAGE CODE: =CAGE_CO	DWG NO: .lfe	REV: .lfe	
SCALE: 1:1	FILE NAME: StarterBoardFabrication.PCBDwf	Sheet: 2 of 12		

Top Overlay (Scale 5)



02 ESE51

First PCB ever made in c



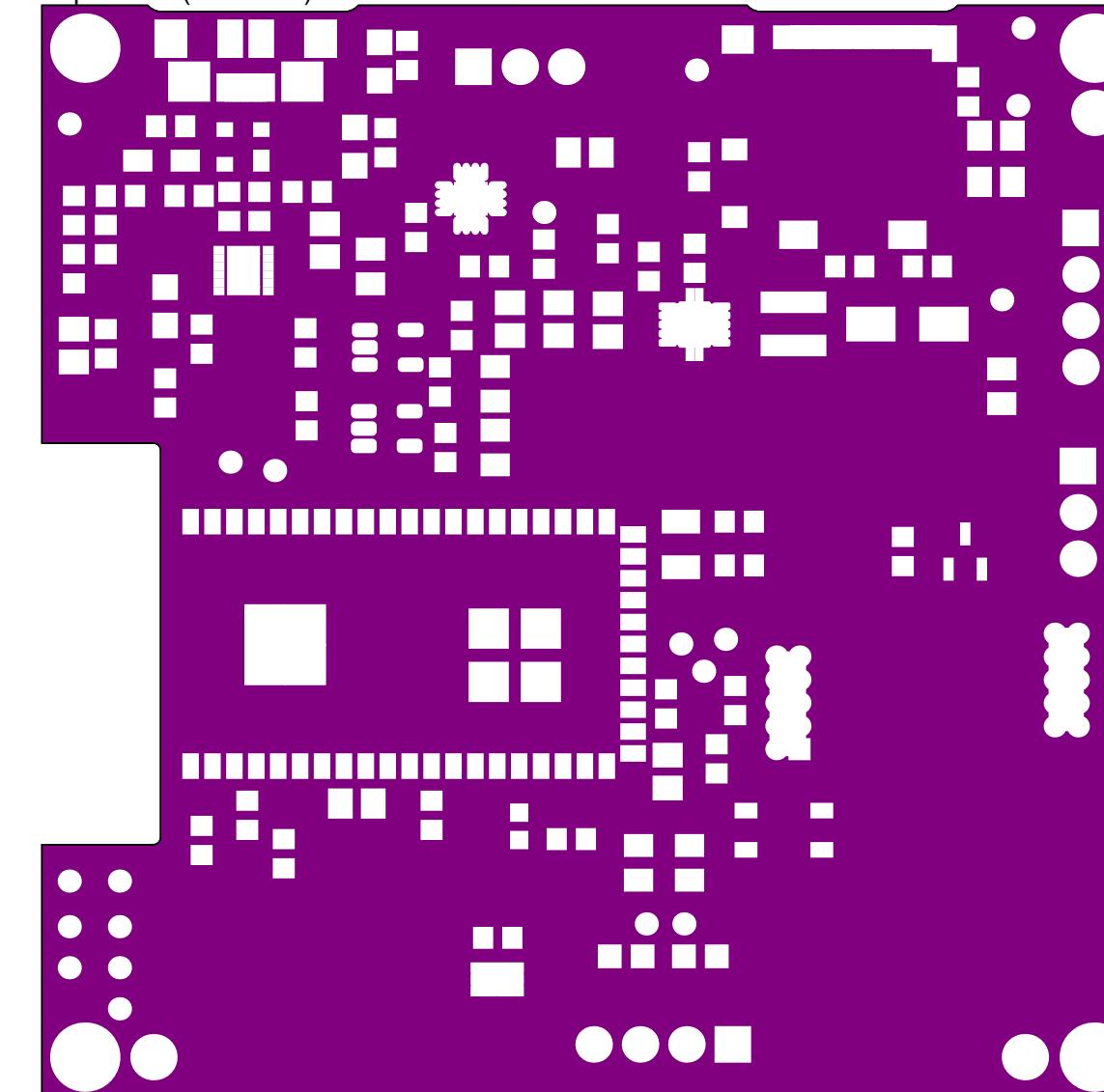
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Team Dehydrated
Yiang Gong
Jianxu Chai
PCB Ver. 1.0
PCBA ver:



Team Dehy
Yiang Gong
Jianxu Cha
PCB Ver. 1
PCBA ver.

Top Solder (Scale 5)



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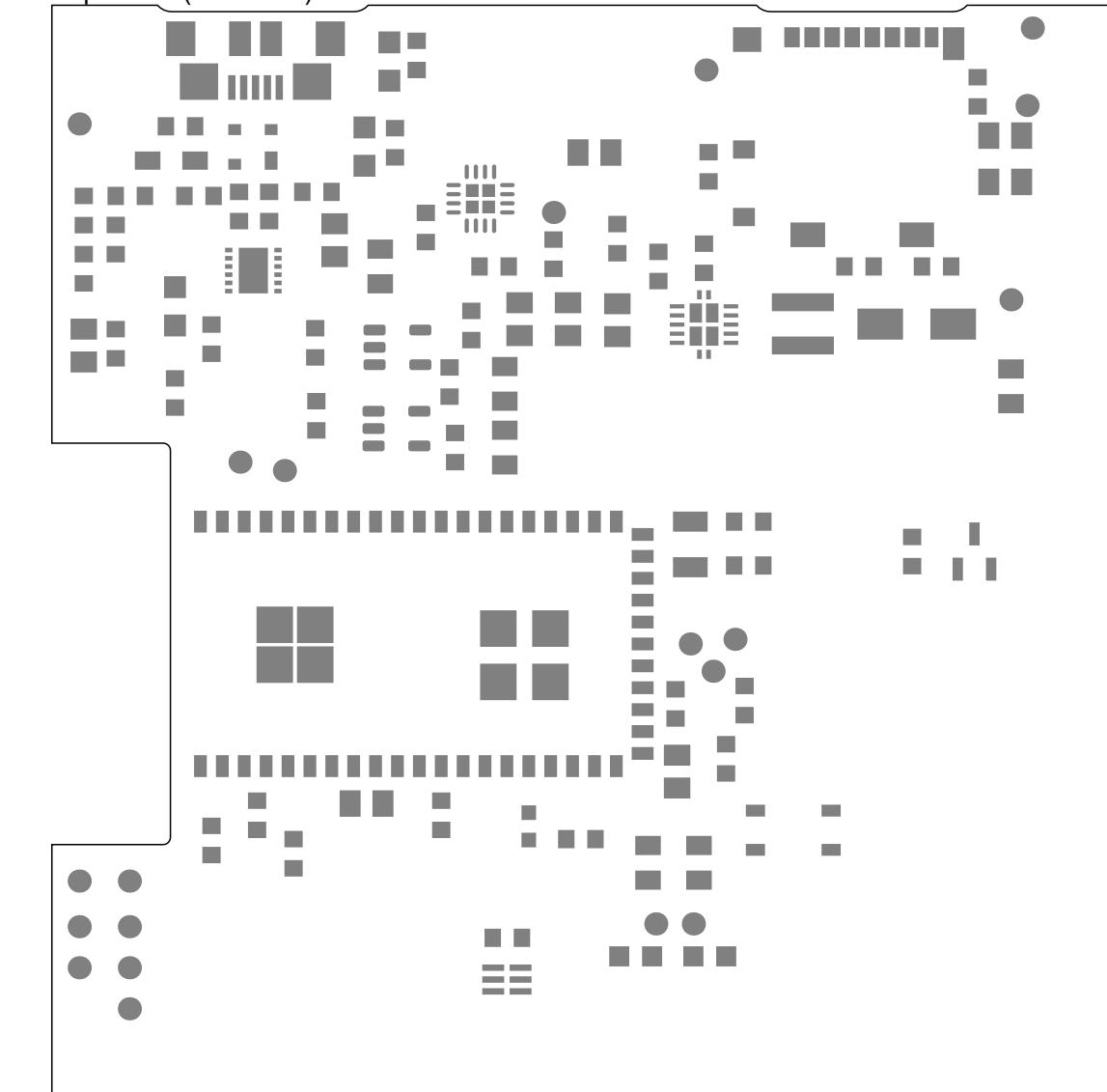
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REVISIONS		DESCRIPTION	DATE	APPROVED

Top Paste (Scale 5:2)



PART NO: =PCB_PART_NUMBER		APPROVALS	DATE	Altium 200 S 33rd St Philadelphia PA, 19104
ENGINEER:	YG & JC	YG &		
DESIGNER:	YG & JC	YG &		
CHECKER:	=PCB_CHECKER	=PCB_CHECKER		
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ASSY DOC:	=DOC_NO_BOM			
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NEXT ASSY	USED ON	PCB DOC:	=PCB_DWG_NO	
APPLICATION		SCALE:	FILE NAME: StarterBoardFabrication.PCBDwf	
		REV:	5 OF 12	

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: ESE516 PROJECT

SIZE: CAGE CODE: DWG NO: REV:

B =CAGE_CO

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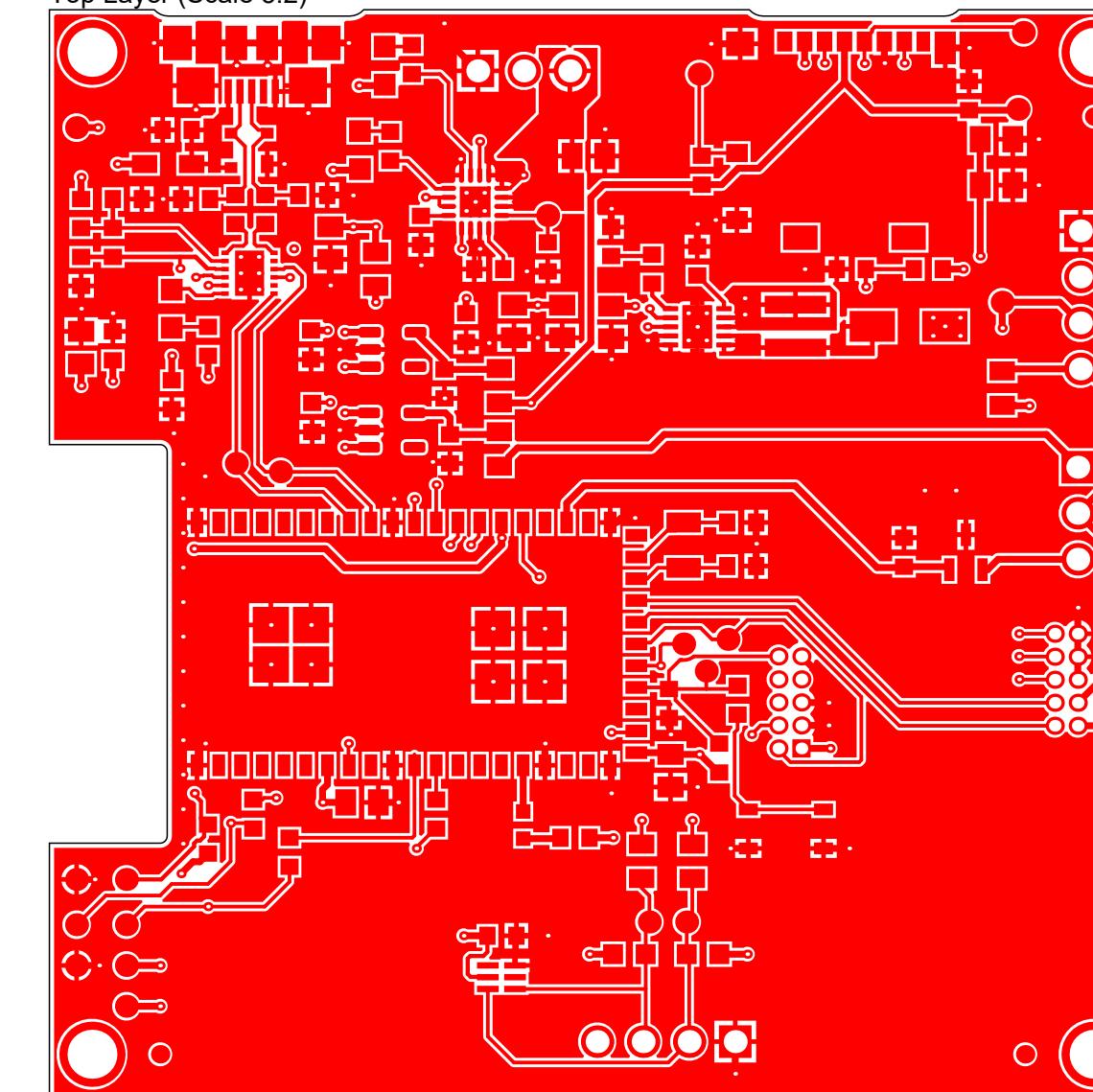
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REV STATUS OF SHEETS	SHEET			

REVISIONS		DESCRIPTION	DATE	APPROVED

1

Top Layer (Scale 5:2)



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PART NO: =PCB_PART_NUMBER		APPROVALS	DATE	Altium 200 S 33rd St Philadelphia PA, 19104
ENGINEER:	YG & JC	YG &		
DESIGNER:	YG & JC	YG &		
CHECKER:	=PCB_CHECKER	=PCB_CHECKER		
BOM DOC:	Reference Documents			
ASSY DOC:	=DOC_NO_BOM			
SCH DOC:	=DOC_NO_FAB_DWG			
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APPLICATION		SCALE: 1:1		
		FILE NAME:	StarterBoardFabrication.PCBDwf	
		REV:		

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: ESE516 PROJECT

SIZE: CAGE CODE: DWG NO: B =CAGE_CO

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DWG NO:
=DOC_NO_ASSY_.lfeDWG NO:
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6 OF 12

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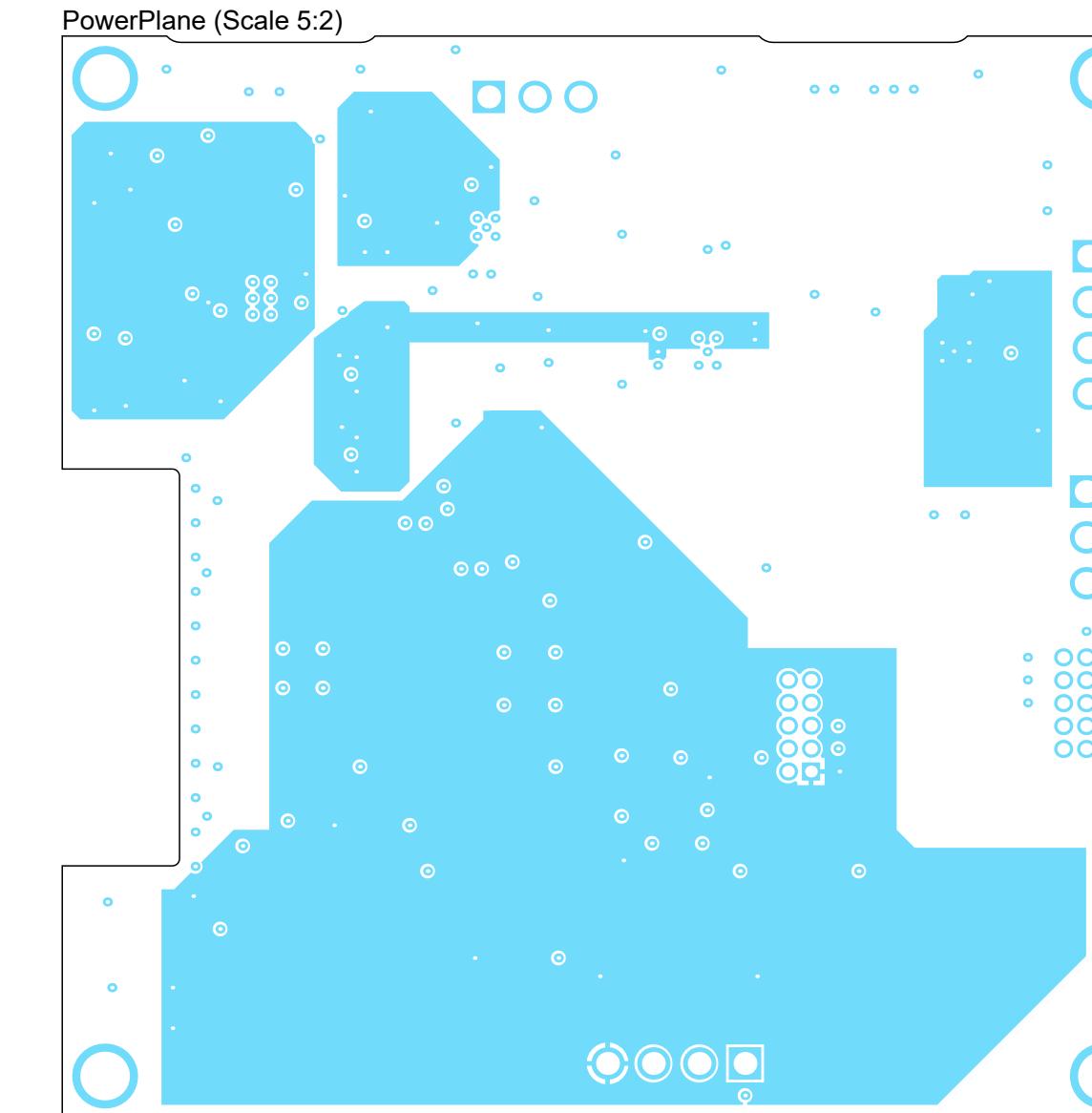
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REV STATUS OF SHEETS	SHEET		

REVISIONS		
DESCRIPTION	DATE	APPROVED



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: YG & JC

DESIGNER: YG & JC

CHECKER: =PCB_CHECKER

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Reference Documents

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ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

NEXT ASSY

USED ON

PCB DOC: =PCB_DWG_NO

APPLICATION

Altium™200 S
33rd St
Philadelphia
PA, 19104

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE:
ESE516
PROJECT

TITLE:

SIZE: CAGE CODE: DWG NO:

REV:

B =CAGE_CO

SCALE:

FILE NAME: StarterBoardFabrication.PCBDwf

SHEET: 7 OF 12

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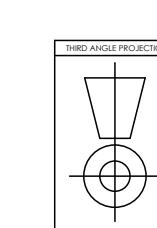
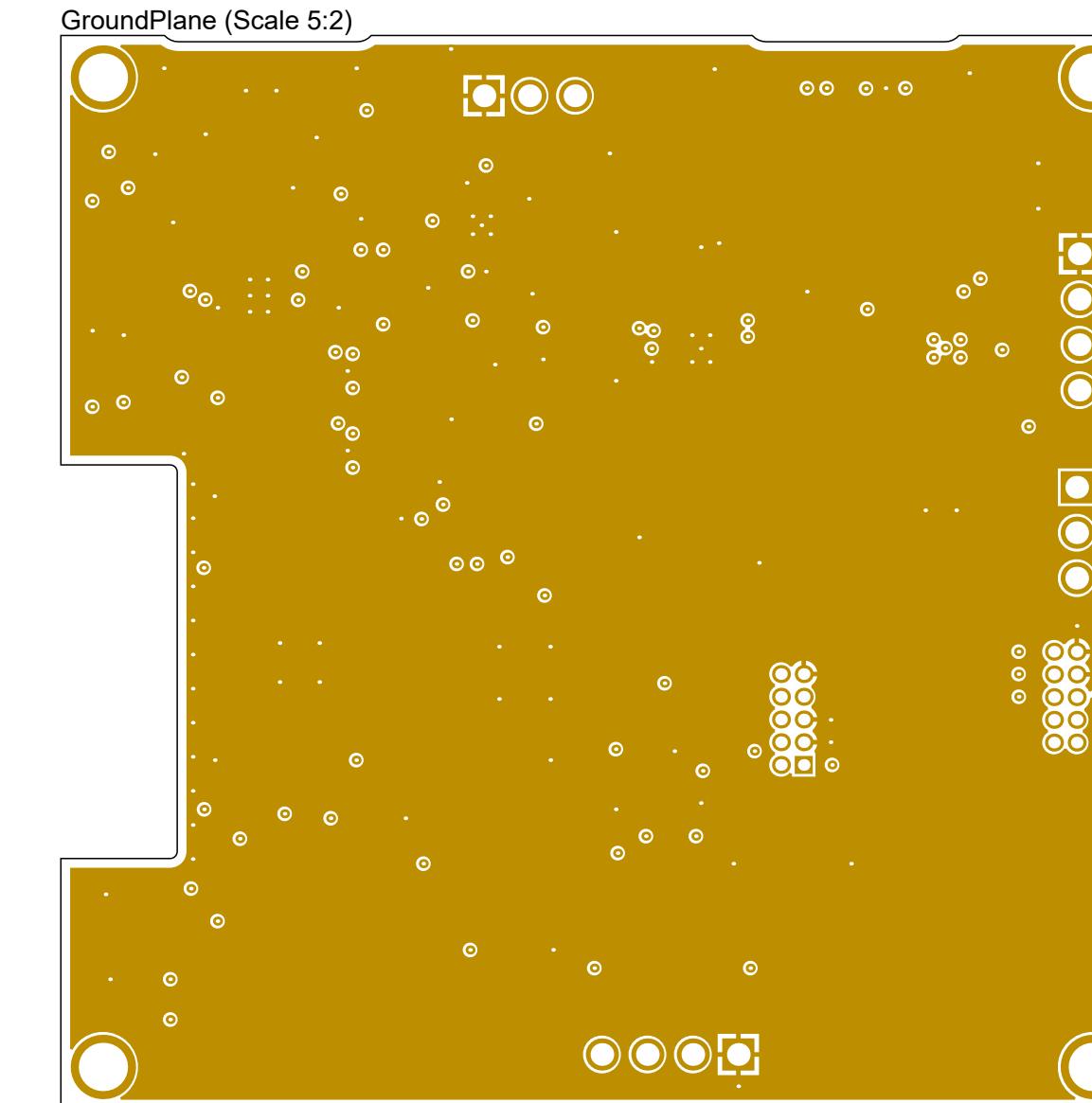
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DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe

REVISIONS		DESCRIPTION	DATE	APPROVED



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: YG & JC YG &

DESIGNER: YG & JC YG &

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Reference Documents

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APPLICATION

AltiumTM200 S
33rd St
Philadelphia
PA, 19104

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE:
ESE516
PROJECT

SIZE: CAGE CODE: DWG NO:

REV: B =CAGE_CO

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 8 OF 12

A

B

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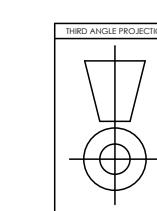
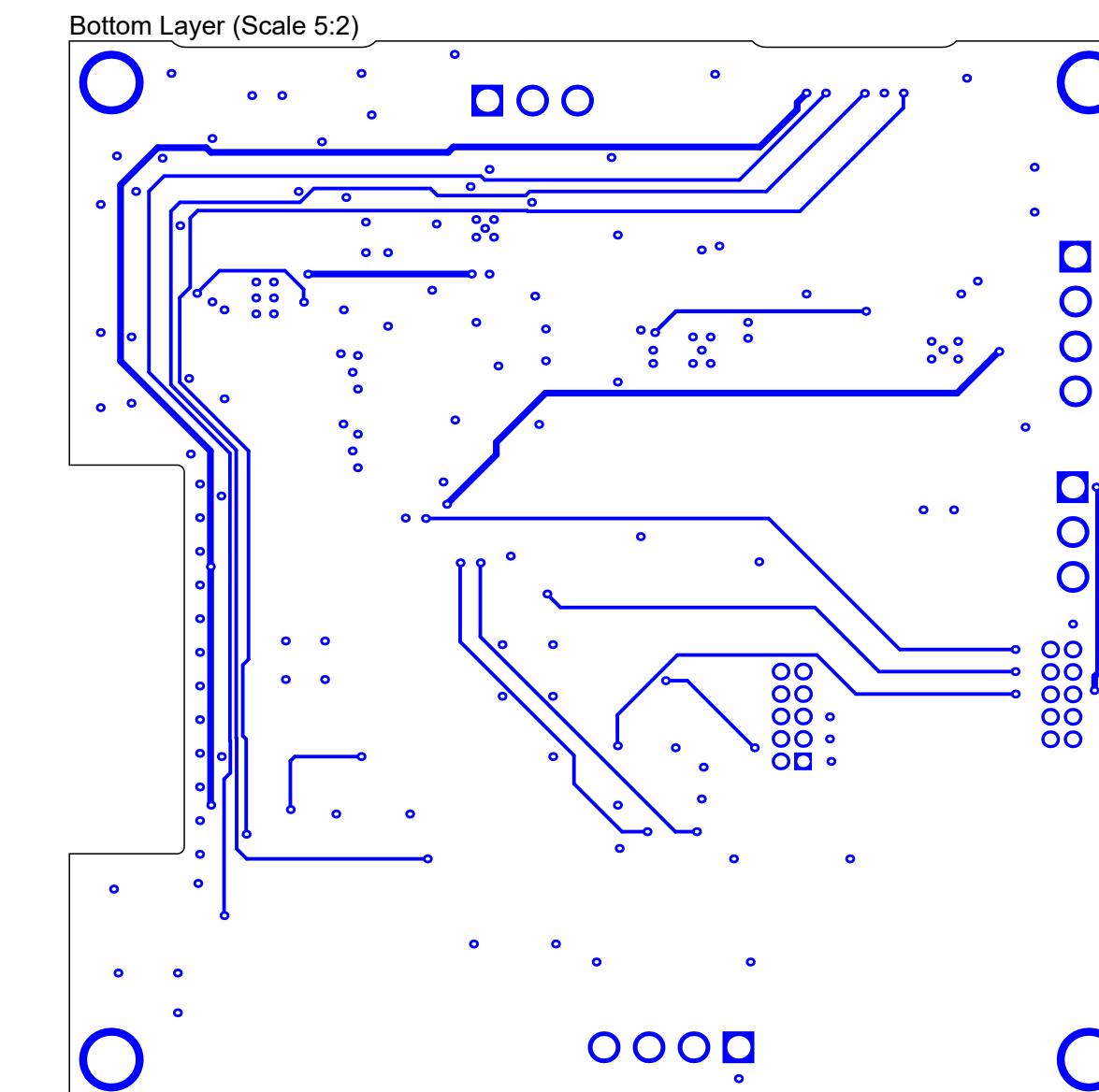
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REVISIONS		
DESCRIPTION	DATE	APPROVED



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: YG & JC YG &

DESIGNER: YG & JC YG &

CHECKER: =PCB_CHECKER =PCB_CHECKER

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APPLICATION

Altium
TM

200 S
33rd St
Philadelphia
PA, 19104

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision
TITLE: ESE516 PROJECT
SIZE: CAGE CODE: DWG NO: REV:
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1

DWG NO:
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9

OF

12

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B

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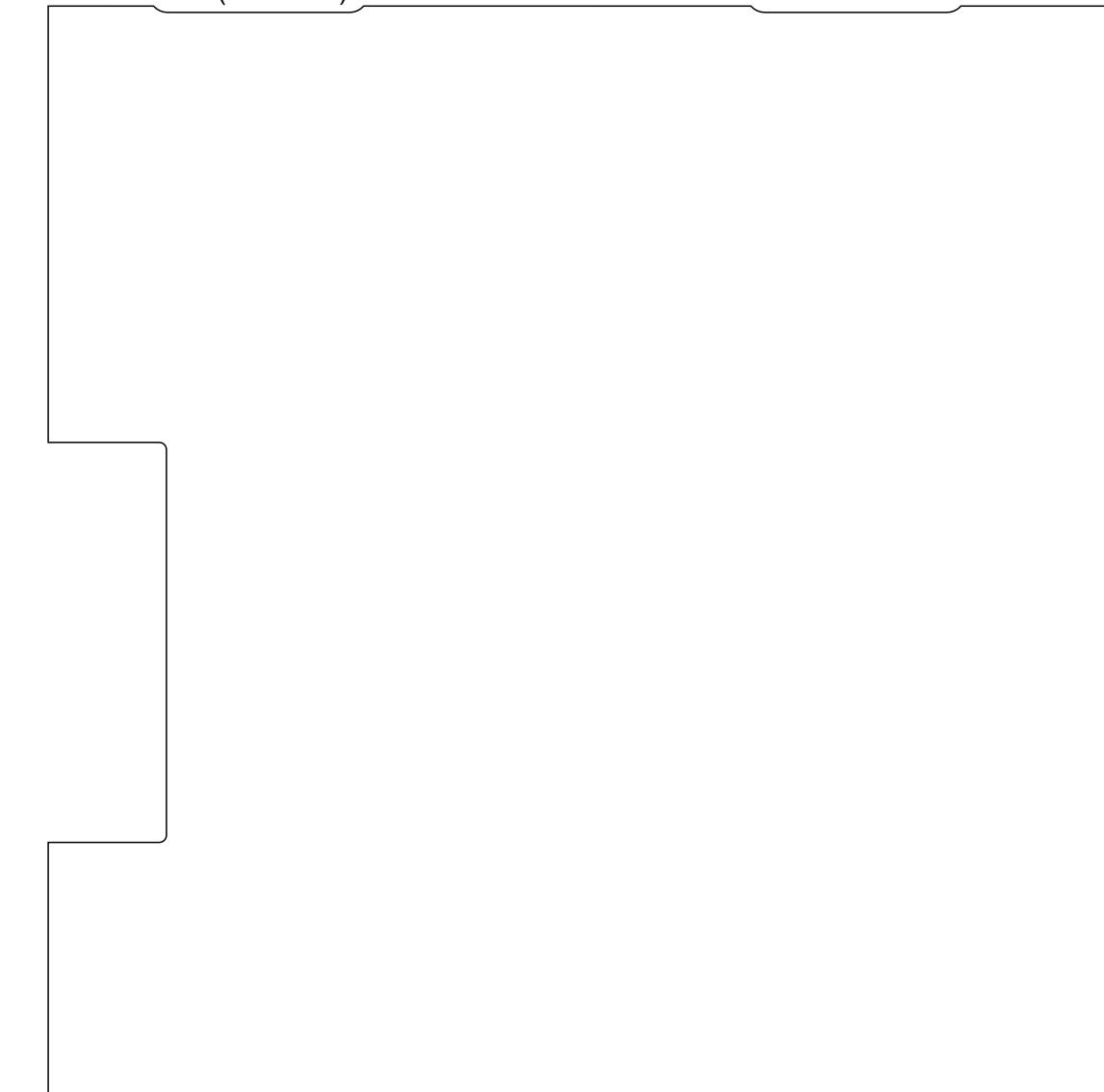
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DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
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Bottom Paste (Scale 5:2)



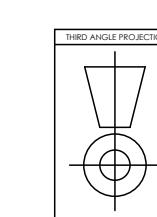
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PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: YG & JC

YG &

DESIGNER: YG & JC

YG &

CHECKER: =PCB_CHECKER

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Reference Documents

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APPLICATION

Altium
TM
200 S
33rd St
Philadelphia
PA, 19104

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE:
ESE516
PROJECT

SIZE: CAGE CODE: DWG NO:

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REV:

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf

SHEET: 10 OF 12

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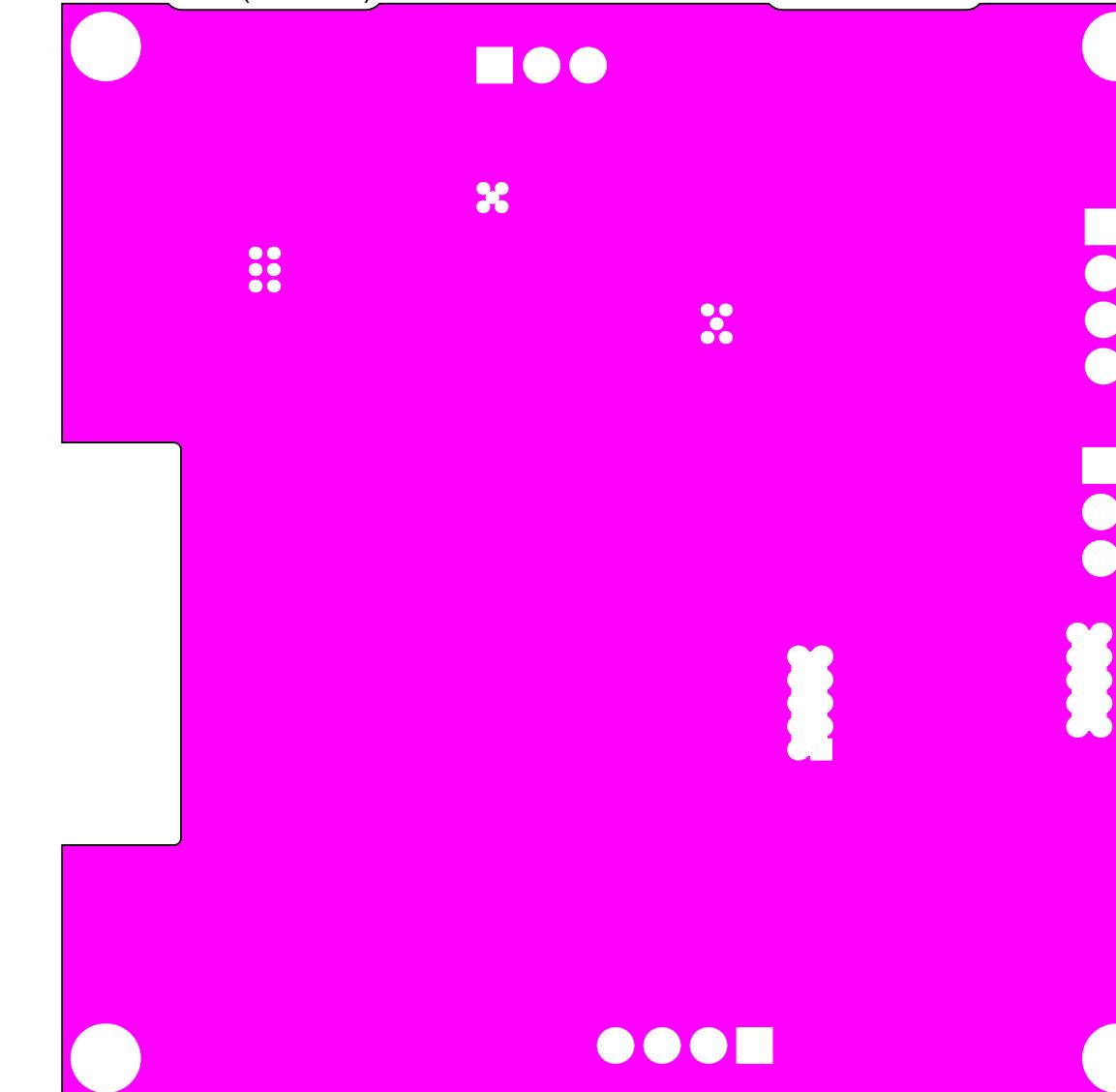
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DWG NO:		=DOC_NO_ASSY_DWG		REV:	.lfe	
REV STATUS OF SHEETS	SHEET	REV			ZONE	REV

REVISIONS		
DESCRIPTION	DATE	APPROVED

Bottom Solder (Scale 5:2)



PART NO: =PCB_PART_NUMBER		APPROVALS		DATE	Altium 200 S 33rd St Philadelphia PA, 19104
ENGINEER:	YG & JC	YG &			
DESIGNER:	YG & JC	YG &			
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SCALE: 1:1	FILE NAME: StarterBoardFabrication.PCBDwf	Sheet: 11	OF 12		

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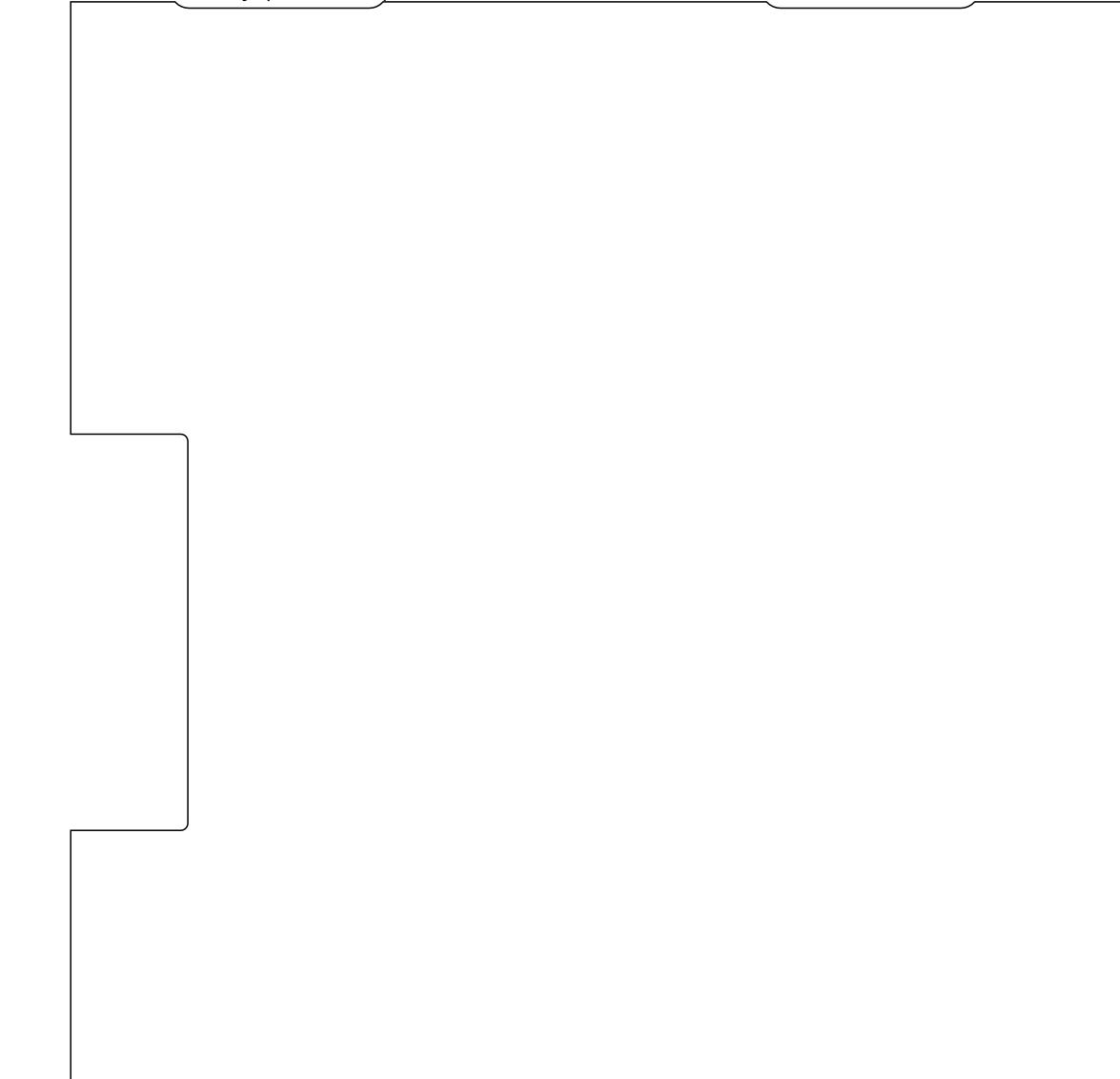
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DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		DESCRIPTION	DATE	APPROVED

Bottom Overlay (Scale 5:2)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: YG & JC

YG &

DESIGNER: YG & JC

YG &

CHECKER: =PCB_CHECKER

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Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

NEXT ASSY USED ON PCB DOC: =PCB_DWG_NO

APPLICATION

Altium™200 S
33rd St
Philadelphia
PA, 19104

.lfe

.Item

.ItemRevision

TITLE:
ESE516
PROJECT

SIZE: CAGE CODE: DWG NO:

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REV:

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.Item

.ItemRevision

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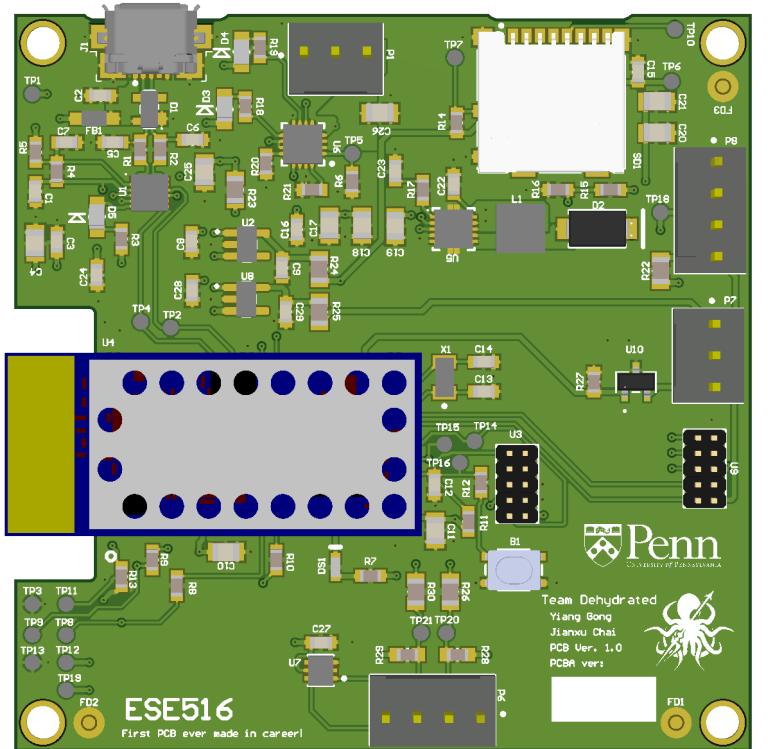
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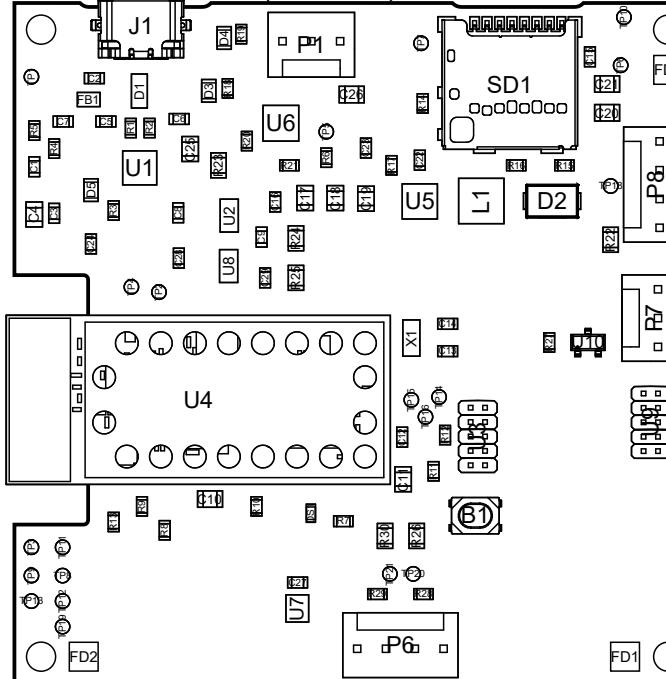
NOTES:

1. THIS ITEM IS ELECTROSTATIC SENSITIVE, AND NEED TO BE HANDLED ACCORDING.
2. WORKMANSHIP WILL CONFORM TO IPC-610 CLASS 2, IPC 7711 WILL APPLY TO ALL REQUIRED REWORK OR MODIFICATION.

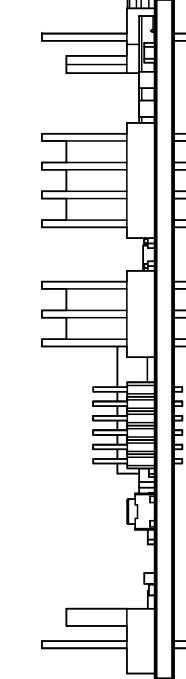
Realistic View



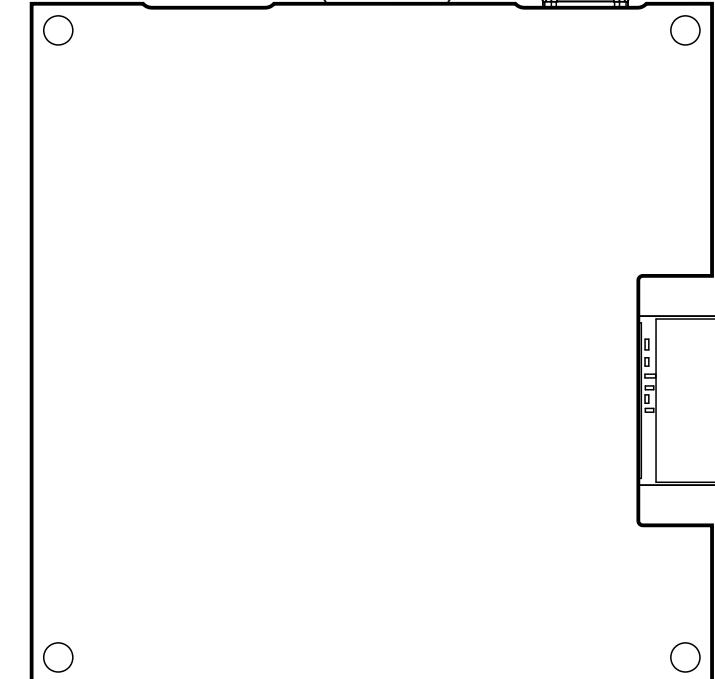
View from Top side (Scale 3:2)



View from Right side (Scale 3:2)



View from Bottom side (Scale 3:2)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: YG & JC YG &

DESIGNER: YG & JC YG &

CHECKER: =PCB_CHECKER =PCB_CHECKER

Reference Documents

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ASSY DOC: =DOC_NO_FAB_DWG

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NEXT ASSY USED ON

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APPLICATION

Altium
 2005
 33rd St
 Philadelphia
 PA, 19104

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE:
ESE516
PROJECT

SIZE: CAGE CODE: DWG NO: REV:

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SCALE: FILE NAME: StarterBoardAssembly.PCBDwf SHEET: 1 OF 3

A

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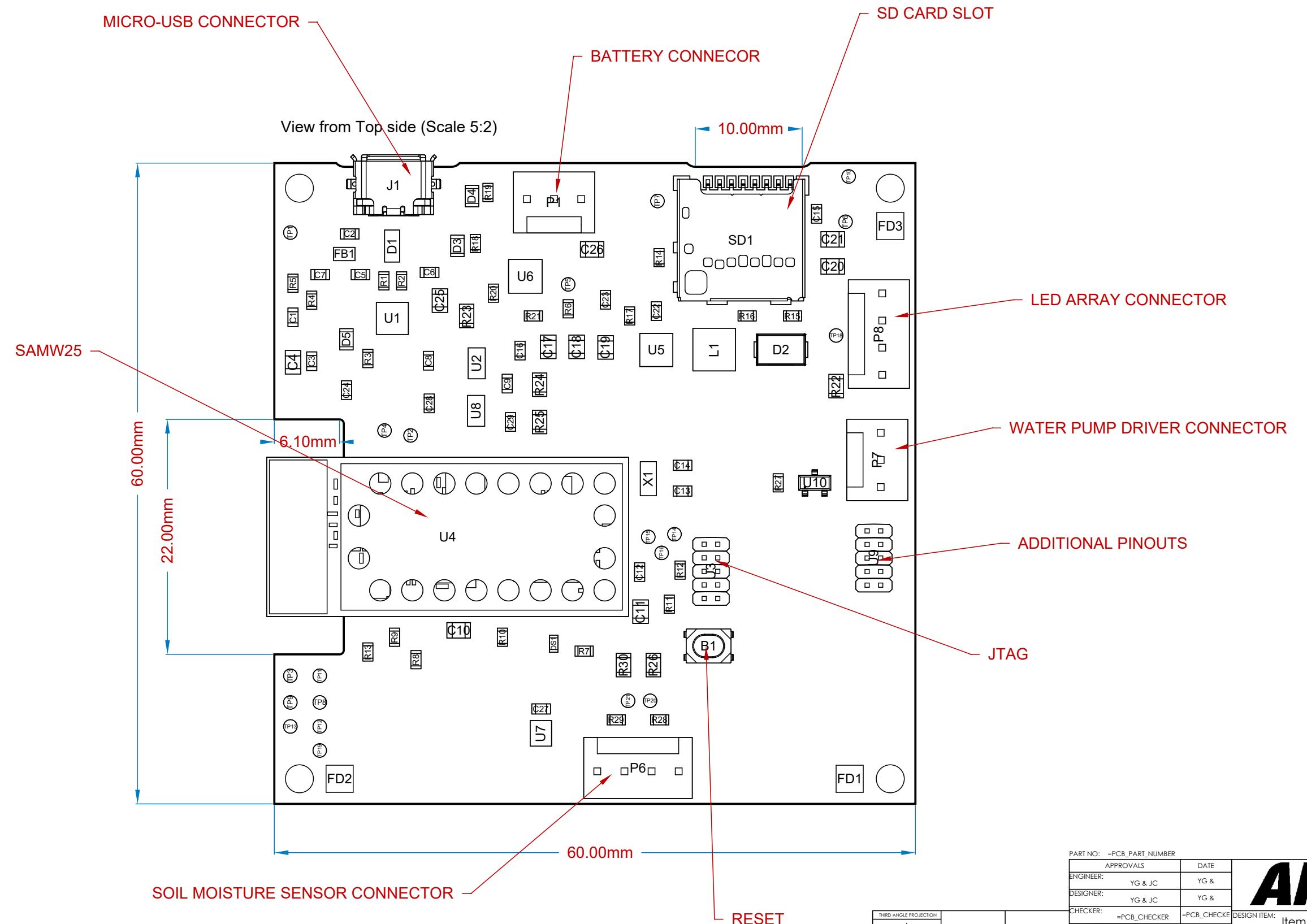
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REV STATUS OF SHEETS		REV					
SHEET							



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: YG & JC

DESIGNER: YG & JC

CHECKER: =PCB_CHECKER

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Reference Documents

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ASSY DOC: =DOC_NO_FAB_DWG

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NEXT ASSY USED ON

PCB DOC: =PCB_DWG_NO

APPLICATION

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE: ESE516

PROJECT

SIZE: CAGE CODE: DWG NO:

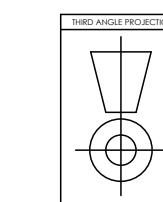
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REV:

DWG NO: .dwg

FILE NAME: StarterBoardAssembly.PCBDwf

SCALE: 2 OF 3

Altium™200S
33rd St
Philadelphia
PA, 19104

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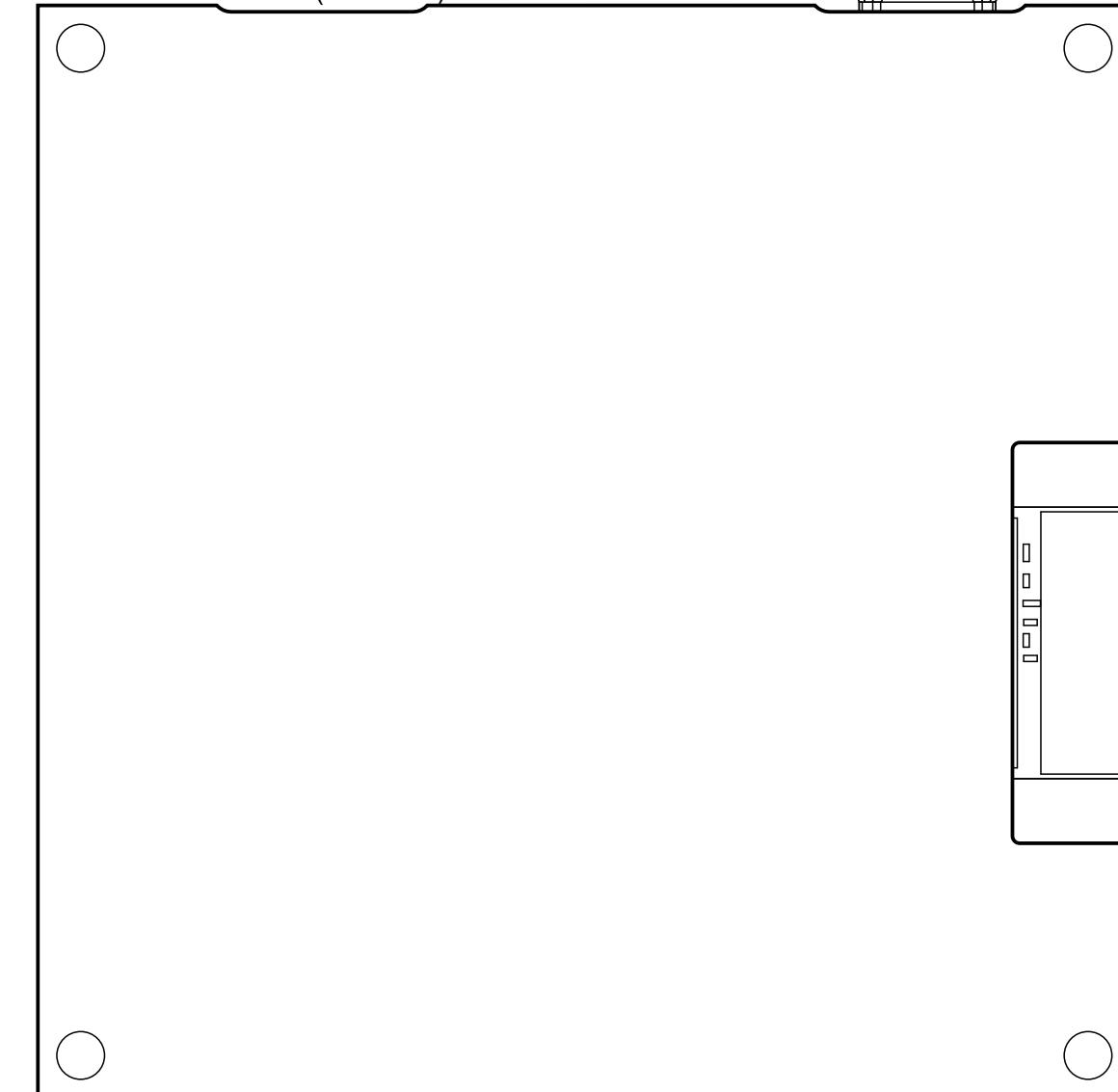
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DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		DESCRIPTION	DATE	APPROVED

View from Bottom side (Scale 5:2)



PART NO: =PCB_PART_NUMBER		APPROVALS	DATE	Altium 200S 33rd St Philadelphia PA, 19104
ENGINEER:	YG & JC	YG &		
DESIGNER:	YG & JC	YG &		
CHECKER:	=PCB_CHECKER	=PCB_CHECKER		
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APPLICATION		SCALE:	FILE NAME:	StarterBoardAssembly.PCBDwf
				Sheet: 3 of 3

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: ESE516 PROJECT

SIZE: CAGE CODE: DWG NO: REV:
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