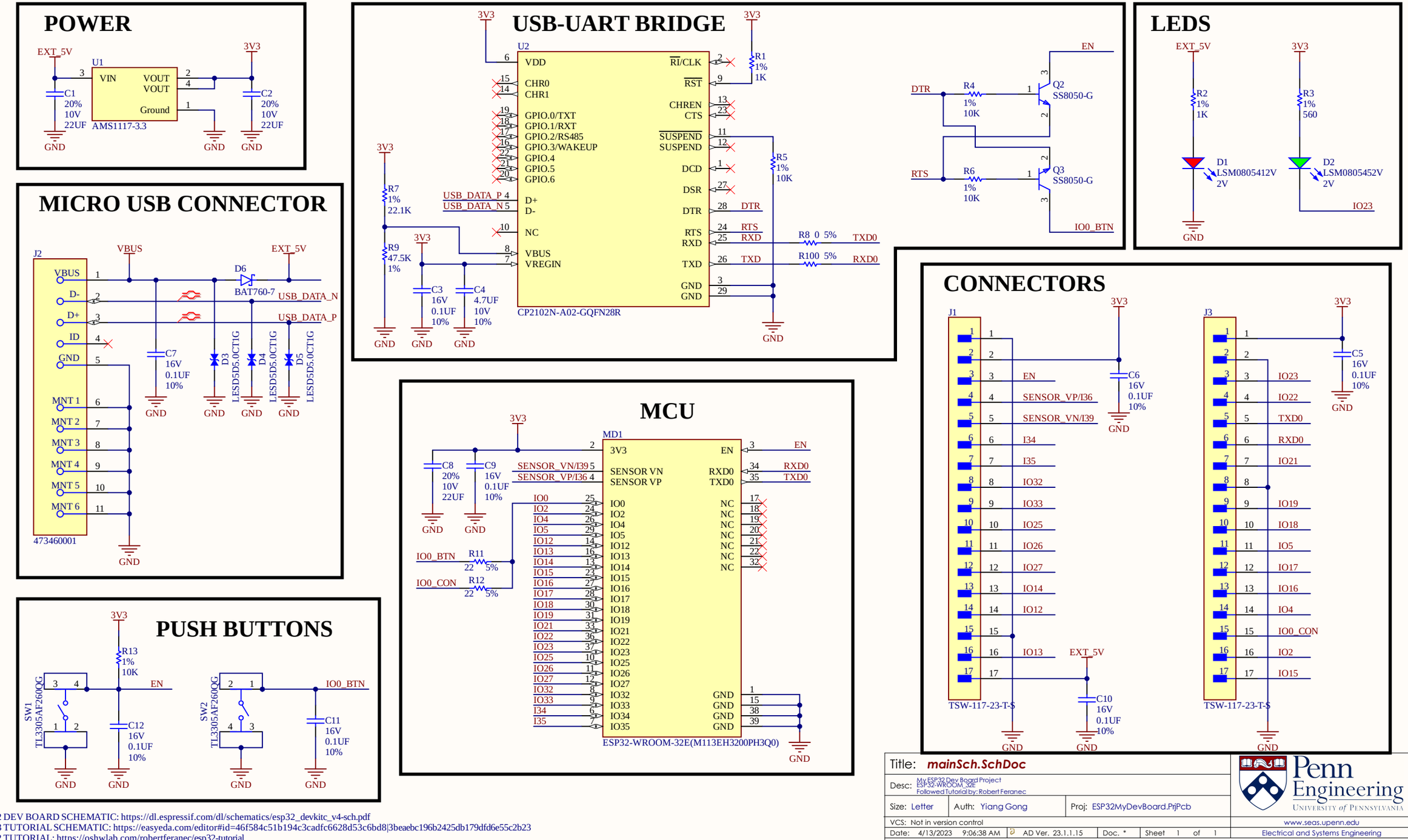

ESP32 DEV BOARD SCHEMATIC: https://dl.espressif.com/dl/schematics/esp32_devkitc_v4-sch.pdf
ESP23 TUTORIAL SCHEMATIC: https://easyeda.com/editor#id=46f584c51b194c3cadfc6628d53c6bd8|3beaebc196b2425db179dfd6e55c2b23
ESP32 TUTORIAL: https://oshwlab.com/robertferanec/esp32-tutorial

Title:	*mainSch.SchDoc*		
Desc:	My ESP32 Dev Board Project ESP32-WROOM_32E Followed Tutorial by: Robert Feranec		
Size: Letter	Auth: Yiang Gong	Proj: ESP32MyDevBoard.PrjPcb	
VCS: Not in version control			
Date: 4/13/2023 9:06:38 AM	AD Ver. 23.1.1.15	Doc. *	Sheet 1 of 1
File: C:\Users\Public\Documents\Altium\ESP32MyDevBoard\mainSch.SchDoc			

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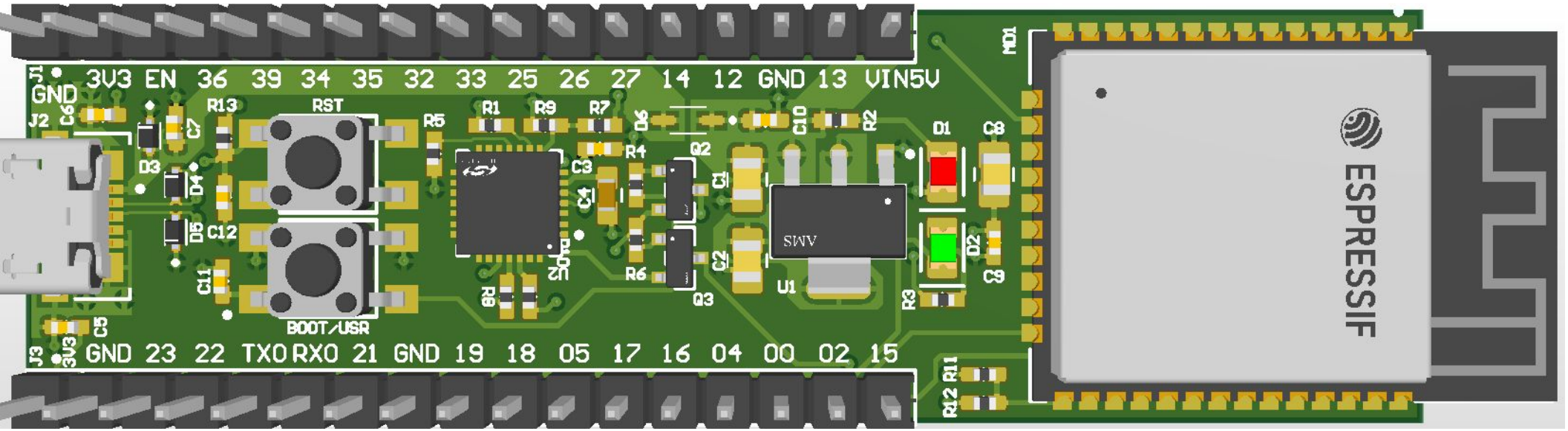
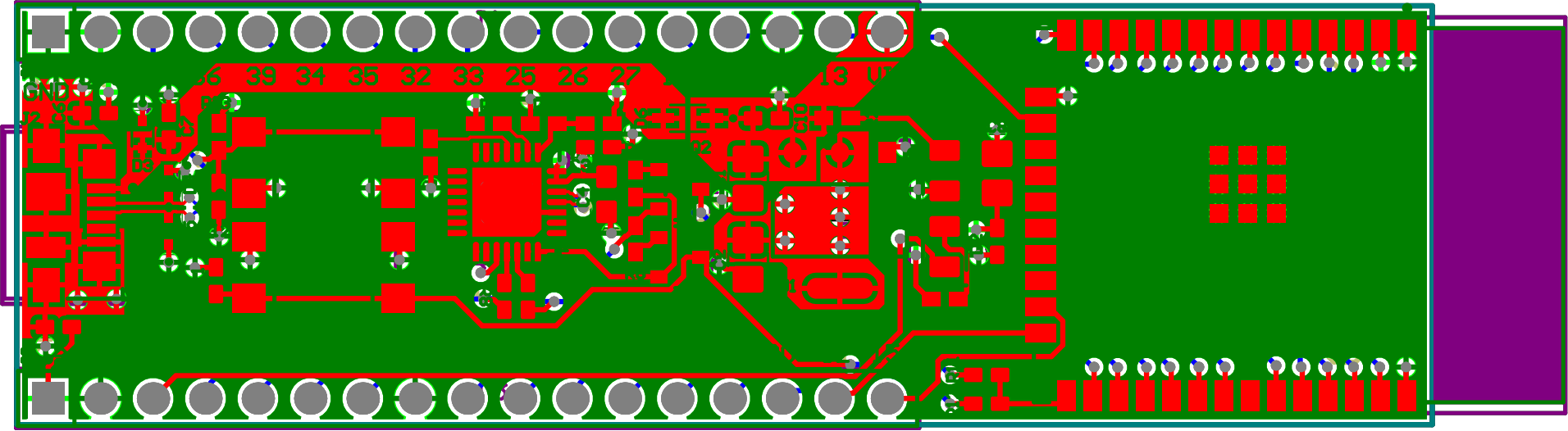
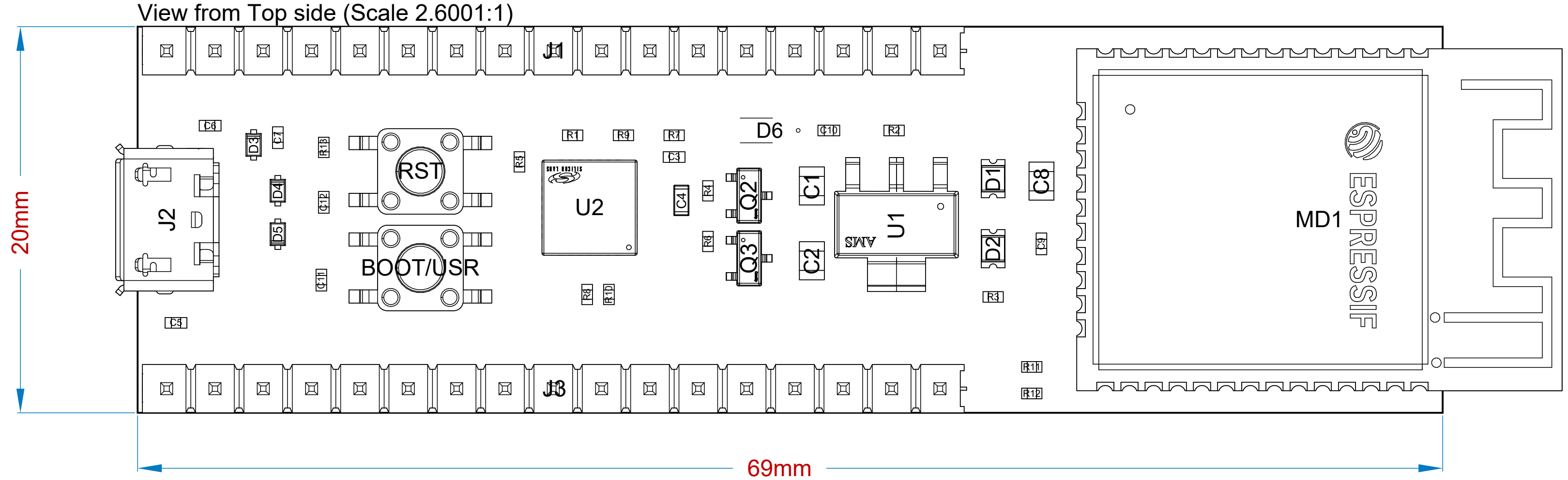

J1
GND 3V3 EN 36 39 34 35 32 33 25 26 27 14 12 GND 13 VIN5V
J2
RST
BOOT/USR
J3
3V3 GND 23 22 TXO RXO 21 GND 19 18 05 17 16 04 00 02 15
SWV
ESPRESSIF


GND
36
39
34
35
32
33
25
26
27
13

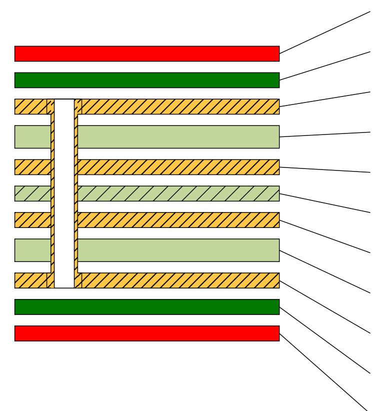
Four (4) Layers
Dimensions: 20mm x 69mm
Thickness: 0.062"
Material: FR4
All layers are unmirrored - should be able to "see straight through"
Scoring: none

Finished Thickness : 0.062 inches
Surface Finish : ENEPIG
Gold Fingers : No
Outer Layer Finish Copper : 1 Oz
Inner Copper : 0.5 oz Inners
Number of Holes Per Board: 234
Minimum Hole Size : 0.008 Inches or more
Minimum Trace (Outer layer) : 0.006 Inches
Minimum Space (Outer layer) : 0.006 Inches
Minimum Trace (Inner layer) : 0.006 Inches
Minimum Space (Inner layer) : 0.006 Inches
Solder Mask : Yes, Solder Mask Sides : Top and Bottom
Solder Mask Color : Black
Solder Mask Type : LPI
Solder Mask Finish : Standard (Semi-Gloss)
Silk Screen : Yes
Silk Screen Sides : Both
Silk Screen Color : White
Internal Slots : None
Counter Sink : No
Counter Bore : No
Edge Plating : No
Route and Retain : Yes
Scoring : Yes
Controlled Impedance : None
Controlled Dielectric : No
Thru-Hole Via in Pad : No
Thickness Tolerance : Plus or Minus 10%
Logo Allowed : In copper or silk screen
UL Marking Required : Yes
Rohs Marking : Yes
ITAR? : No

View from Top side (Scale 2.6001:1)



Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0mm	Solder Resist	Solder Mask	GTS
Copper	**Top Layer**	**0mm**		**Signal**	**GTL**
Prepreg		*0mm*	*PP-006*	*Dielectric*	
CF-004	**Ground**	**0mm**		**Signal**	**G1**
		0mm	*FR-4*	*Dielectric*	
CF-004	**Power**	**0mm**		**Signal**	**G2**
Prepreg		*0mm*	*PP-006*	*Dielectric*	
Copper	**Bottom Layer**	**0mm**		**Signal**	**GBL**
Surface Material	Bottom Solder	0mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1mm

Title: **PCB1FABRICATION.PCBDwf**
Desc:
Size: Letter | Auth: YIANG GONG | Proj: ESP32MyDevBoard.PrjPcb
='VCS: '+VersionControl_ProjFolderRevNumber
='Date: '+CurrentDate+' '+CurrentTime+ApplicationBuildNumber+DocumentNumber
='File: '+DocumentFullPathAndName

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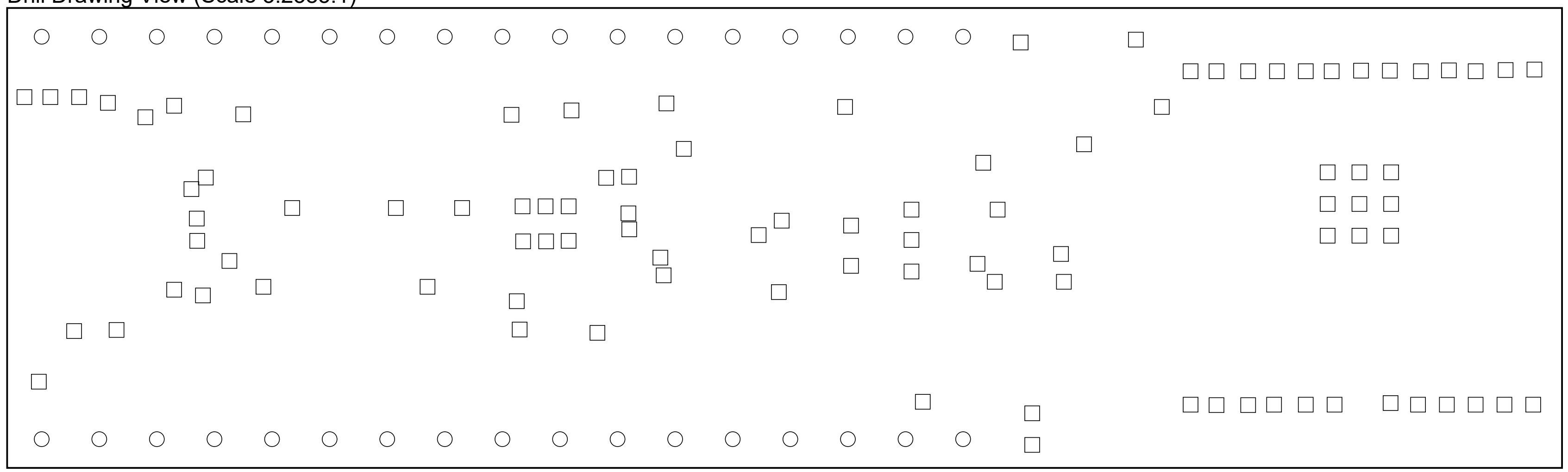
A	B	C	D

Drill Table

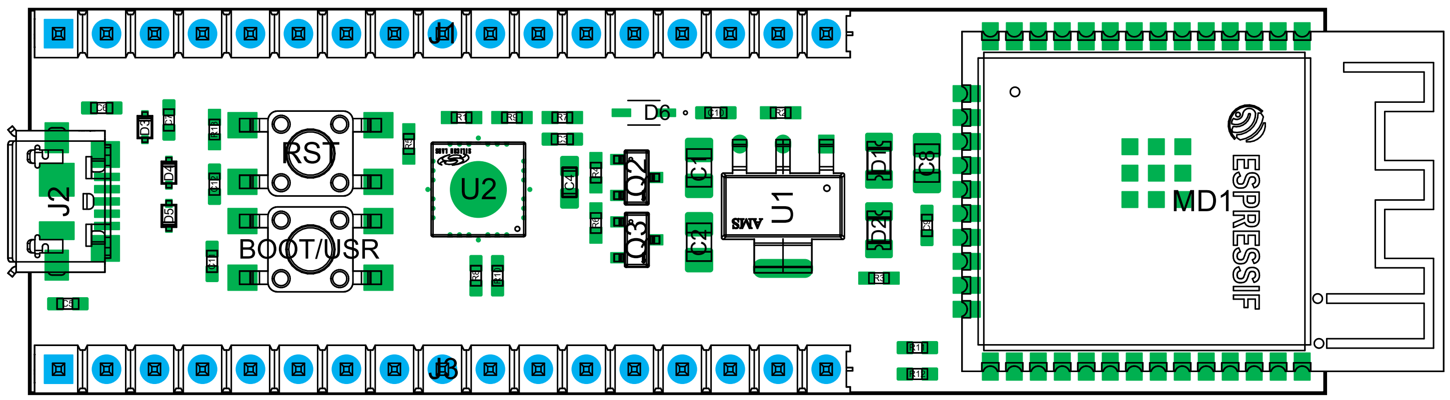
Symbol	Count	Hole Size	Plated	Hole Tolerance
□	97	0mm	Plated	
○	34	1mm	Plated	
	131 Total			

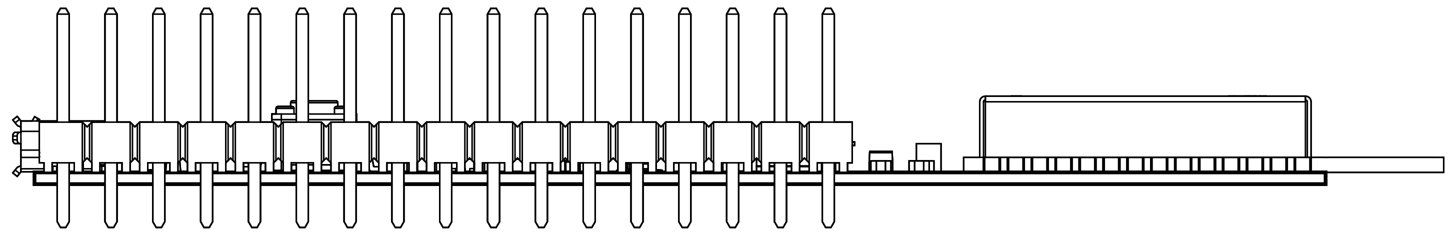
Drill Drawing View (Scale 3.2385:1)

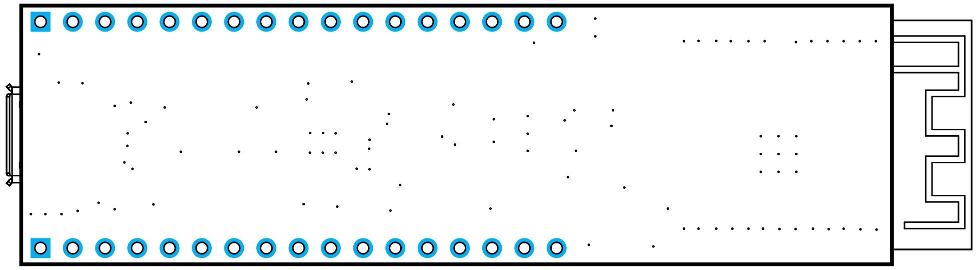


Title: ***PCB1FABRICATION.PCBDwf***	Penn Engineering University of Pennsylvania
Desc:	
Size: Letter · Auth: YIANG GONG · Proj: ESP32MyDevBoard.PrjPcb	
='VCS: '+VersionControl_ProjFolderRevNumber	www.seas.upenn.edu
='Date: '+CurrentDate+' · =CurrentTime+ApplicationBuildNumber · =DocumentName · Sheet =SheetNumber of =SheetTotal	Electrical and Systems Engineering
='File: '+DocumentFullPathAndName	

A	B	C	D







Note:

1. Text element with square border.
2. Text element with no border
3. Text element with circle border

Title: **PCB1FABRICATION.PCBDwf**		
Desc:		
Size: Letter	Auth: YIANG GONG	Proj: ESP32MyDevBoard.PrjPcb

='VCS: '+VersionControl_ProjFolderRevNumber
='Date: '+CurrentDate+' ='AD Ver: '+ApplicationBuildNumber ='Doc_ID: '+DocumentNumber Sheet 3 of 3
='File: '+DocumentFullPathAndName

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NOTES:

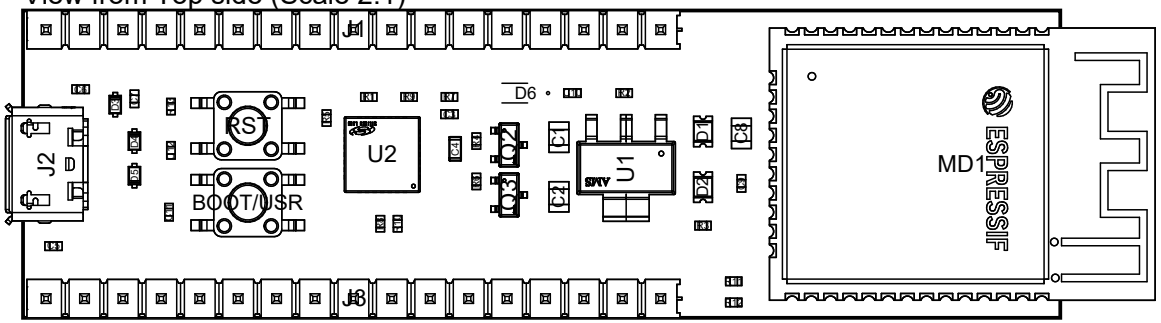
1. THIS ITEM IS ELECTROSTATIC SENSITIVE AND SHALL BE HANDLED ACCORDINGLY

2. WORKMANSHIP WILL CONFORM TO IPC-610 CLASS 2, IPC-7711 WILL APPLY TO ALL REQUIRED REWORK OR MODIFICATION

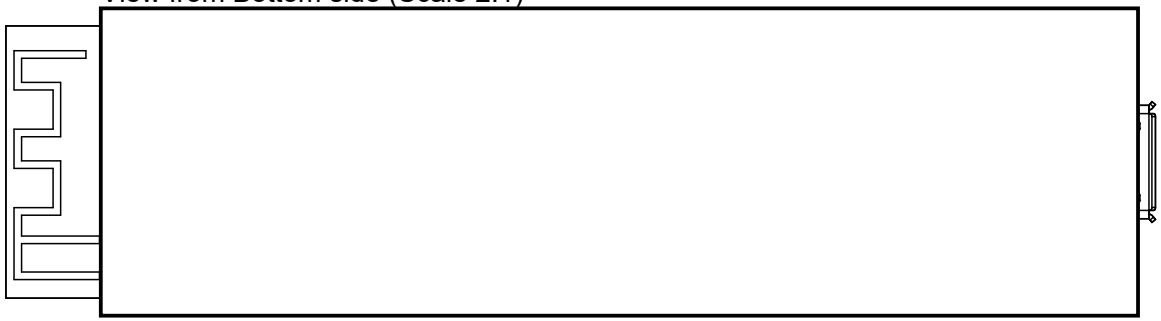
3. ASSEMBLY IS TO BE IDENTIFIED BY A LABEL INDICATING-
 SERIAL NUMBER
 PART NUMBER and REVISION
 VENDOR
 DATE CODE

4. THE SUPPLIED INSERTION DATA FOR THIS PCBA IS PROVIDED TO ASSIST PROGRAMMING, COMPONENT OFFSET AND ROTATION ARE RELATIVE TO THE ENGINEERING DESIGN ENVIRONMENT AND MAY NOT MATCH REEL PACKAGING OR FEED ORIENTATION, COMPONENTS, ESPECIALLY POLARIZED PARTS, MUST BE VERIFIED AGAINST THE ACTUAL PCBA DRAWING TO INSURE PROPER INSTALLATION

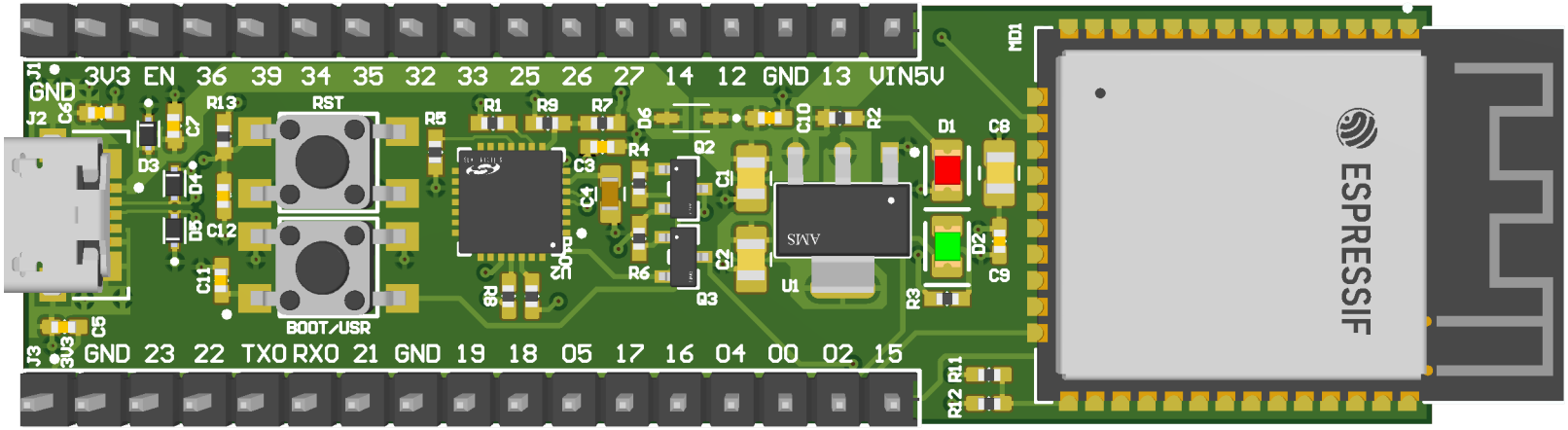
View from Top side (Scale 2:1)



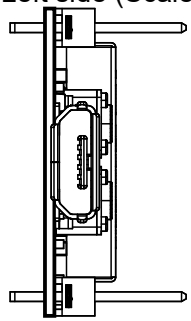
View from Bottom side (Scale 2:1)



Realistic View



View from Left side (Scale 2:1)



Bill Of Materials

Line #	Designator	Name	Quantity
1	C1, C2, C8	CAP 0805 22UF 10V 20% X5R	3
2	C3, C5, C6, C7, C9, C10, C11, C12	CAP 0402 0.1UF 16V 10% X7R	8
3	C4	CAP 0603 4.7UF 10V 10% X5R	1
4	D1	LSM0805412V	1
5	D2	LSM0805452V	1
6	D3, D4, D5	LESD5D5.0CT1G	3
7	D6	BAT760-7	1
	J1, J3	TSW-117-23-T-S	2
9	J2	473460001	1
10	MD1	ESP32-WROOM-32E (M113EH3200PH3Q0)	1
11	Q2, Q3	SS8050-G	2
12	R1, R2	RES 0402 1K 1%	2
13	R3	RES 0402 560 1%	1
14	R4, R5, R6, R13	RES 0402 10K 1%	4
15	R7	RES 0402 22.1K 1%	1
16	R8, R10	RES 0402 0 5%	2
17	R9	RES 0402 47.5K 1%	1
18	R11, R12	RES 0402 22 5%	2
19	SW1, SW2	TL3305AF260QG	2
20	U1	AMS1117-3.3	1
21	U2	CP2102N-A02-GQFN28R	1