Yibo Dong

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Education

East China Normal University (ECNU) , Shanghai, China 2022 – Present

Master student in Software Engineering (SE), expected June 2025. GPA: 91.1/100,Top 1%

Shanghai Jiao Tong University (SJTU), Shanghai, China 2017 – 2021

B.S. in Information Security, School of Electronic Information and Electrical Engineering. GPA: 83.5/100

Publications

LightF3: A Lightweight Fully-Process Formal Framework for Automated Verifying Railway Interlocking Systems Published in FSE'23.

Yibo Dong, Xiaoyu Zhang, Yicong Xu, Chang Cai, Yu Chen, Weikai Miao, Jianwen Li, and Geguang Pu.

Accelerating CAR-based Model-Checking with Multiple Unsat Cores Submitted to VMCAI'24.

Yibo Dong, Xiwei Wu, Jianwen Li, Geguang Pu and Ofer Strichman.

Revisiting Assumptions Ordering in CAR-Based Model Checking Submitted to TCAD.

Yibo Dong, Yu Chen, Jianwen Li, Geguang Pu and Ofer Strichman.

Work Experience

IVerifier: Formal Verification of Interlocking System June. 2022 – Present

Product Owner Shanghai Trusted Industrial Platform, China

Responsible for leading the team in developing **LightF3**, an automated framework for verifying interlocking systems, as well as designing new model checkers for hardware verification.

Certify: Static Analysis of C programs July. 2021 – May. 2022

Software Engineer Shanghai Trusted Industrial Platform, China

Responsible for developing static analysing tools for C code based on existing standards, e.g. MISRA-C.

Reasearch Experience

Accelerating CAR-based Model-Checking with Multiple Unsat Cores Jan.2024 – June. 2024

Main Contributor Supervised by Ofer Strichman from Technion and Jianwen Li from Software Engineering Institute, ECNU

- In SAT-based model checking, a key component is the ability to generalize states via strengthening them with the unsatisfiable cores returned by the SAT solver.
- I proposed and implemented a technique for generating multiple unsatisfiable cores in linear time and updating them simultaneously.
- This innovation significantly improved performance, solving more unsafe cases than any other publicly available model checker, including 7 unique instances from the HWMCC that had previously been unsolved.
- Our work was submitted to VMCAI'24 (International Conference on Verification, Model Checking, and Abstract Interpretation).

Revisiting Literal Ordering in CAR-Based Model Checking July. 2023 – Dec. 2024

Main Contributor Supervised by Ofer Strichman from Technion and Jianwen Li from ECNU

- In SAT-based model checking, the performance is sensitive to the order of assumptions in SAT solvers.
- I theoretically analyzed this issue, extended existing approaches, and proposed new ordering strategies.
- My implementation outperformed other strategies and state-of-the-art bug-finding algorithms like ABC-BMC on the HWMCC benchmark.

- Our paper was submitted to TCAD (IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems).

Formal Verification of Interlocking Systems June. 2022 – June. 2023

Main Contributor Supervised by Jianwen Li from ECNU

- The formal verification of interlocking systems has been a challenging problem due to the complexity of domain knowledge.
- Collaborating with our industrial partner, I designed a Domain Specific Language, RIS-FL, and implemented LightF3, a formal framework for verifying railway interlocking systems.
- We evaluated it using real station instances, successfully uncovering deep hidden bugs in existing designs.
- Our paper was accepted by FSE'23 (The ACM International Conference on the Foundations of Software Engineering).

Splitting Theory of C Programming Language Jan. 2020 – Jan. 2021

Main Contributor Supervised by QinXiang Cao from John Hopcroft Center for Computer Science, SJTU.

- We designed a decomposition theory for C programs based on Hoare logic, enabling the generation of necessary Hoare Triples for a given C program.
- Collaborating with my partner, we formalized the control flow of C programs (without concurrency) and completed the soundness proof in Coq.
- This pioneering exploratory work advanced the development of VST-A. One of a research from POPL'23 used our work as part of the foundation.

An Annotated variant CompCert-Clightgen Oct. 2019 – Jan. 2020

Sole Contributor Supervised by QinXiang Cao from SJTU

- In CompCert, Clightgen generates required correctness proofs in Coq for C programs.
- I extended this tool by allowing users to provide auxiliary proof information as annotations within C code, enabling VST to automatically complete proofs. I enhanced the annotation syntax, implemented the collection and parsing of annotations, and generated corresponding Coq commands.
- We developed a demo called VST-IDE for interpretive verification of annotated C programs. This project has continued to evolve, with a paper expected to be submitted to JAR (Journal of Automatic Reasoning) next year.

Automatic Correcting of Basic Math Proofs Mar. 2019 – Sept. 2019

Main Contributor Supervised by QinXiang Cao from SJTU

- We aimed to design an automatic grading tool for mathematical proofs written with Chinese keywords. The tool reads proofs about limit properties written in Chinese with Markdown formulas and validates them.
- I designed the parser for these proofs and implemented the translation into formal Coq proofs. Using Coq library components from collaborators, automatic grading is achieved.
- I completed a demo and presented it internally within the lab.
- Due to the extensive ambiguities in Chinese, we halted further development before incorporating NLP techniques.

Skills

- Languages: Mandarin(native), English(Fluent, IELTS 8.0 (L9 R8.5 W7.5 S6.5))
- Programming Languages: C/C++, Python, OCaml, Coq

♡ Honors and Awards

M Prize(Top 10%), Team Leader, The Mathematical Contest in Modeling April. 2019
1st Prize, Team Leader, Shanghai Jiao Tong University Engineering Mindset Competition Oct. 2019
ShangHai Marathon Volunteer 2017-2019