2CJ4 LAB Report

Set 3

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Cooperate with:

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is our own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario.

Part 1:

$\because V_o(t) = -\frac{1}{RC}\int_0^t V_i(x)\,dx + V_o(0)$ (known from background)

$\because (R = R_3)\ (C = C_3)$ (known from background) $\because$ frequency $= 1\,kHz$; Peak-to-peak amplitude $= 2V$

$\because R_3 = 10k\Omega$, $C_3 = 100nF$

$\therefore$ the period is $\frac{1}{1kHz} = 1ms$

$\because$ It is square wave $\therefore$ $V_1(t) = 1V \quad 0 < t < 0.5ms$

$V_2(t) = -1V \quad 0.5 < t < 1ms$

$$\therefore V_{o(1)} = -\frac{1}{RC}\int_0^{0.5ms} V_1(t)\,dt = -\frac{1}{(10k\Omega)(100nF)}\int 1V\,dt$$

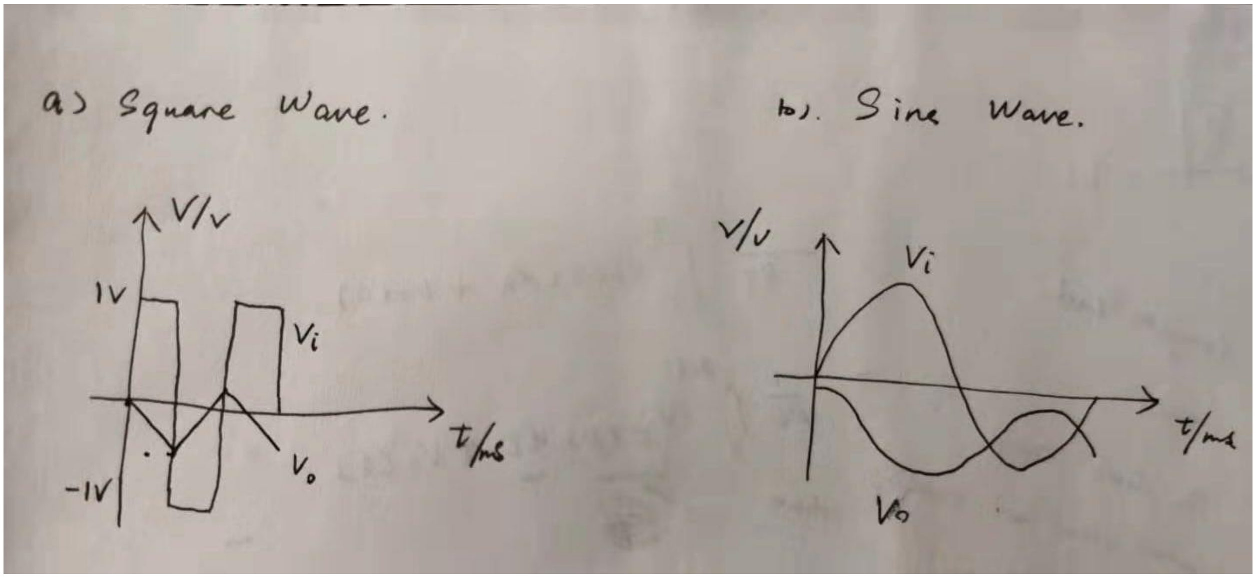
$$= -10^3(1)\,t = -10^3 t$$

$$\therefore V_{o(2)} = -\frac{1}{RC}\int_{0.5ms}^{1ms} V_2(t)\,dt = -10^3\int -1V\,dt$$

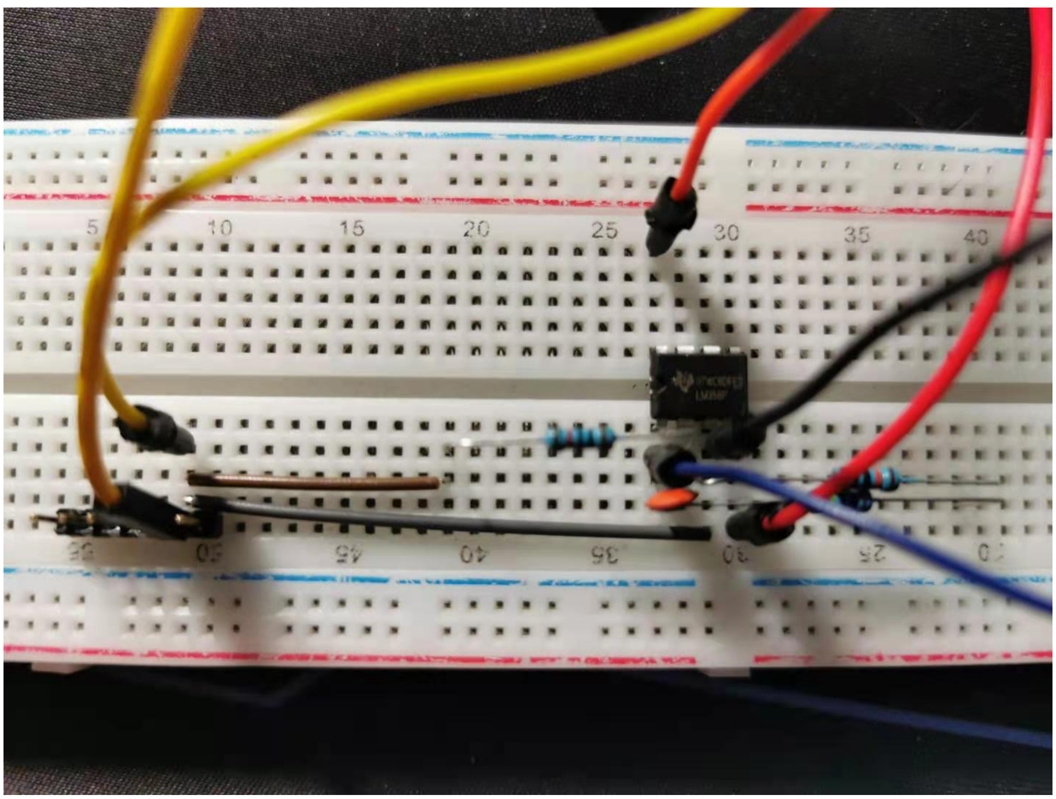
$$= -10^3(-1)\,t$$

$$= 10^3 t$$

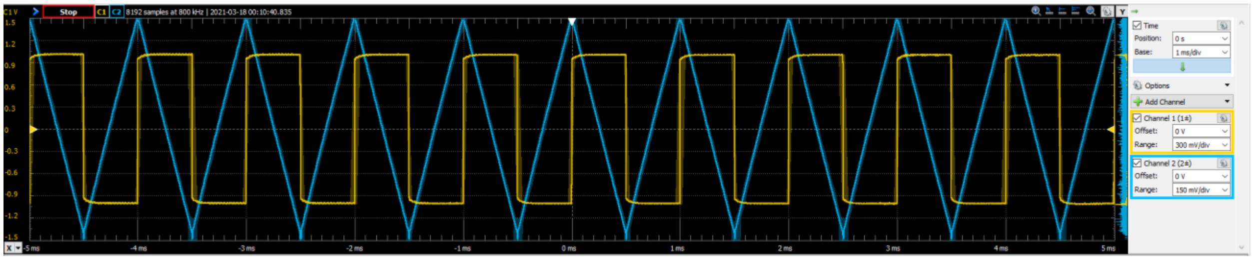
$$\therefore V_o = \begin{cases} -10^3 t & 0 < t < 0.5ms \\ 10^3 t & 0.5 < t < 1ms \end{cases}$$

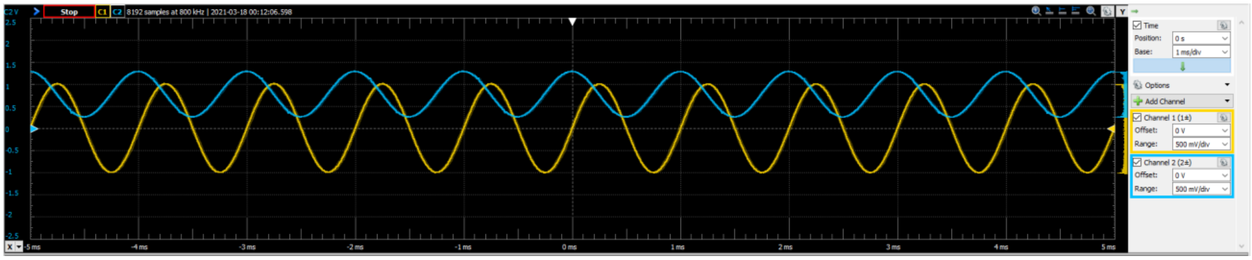


Part 2:



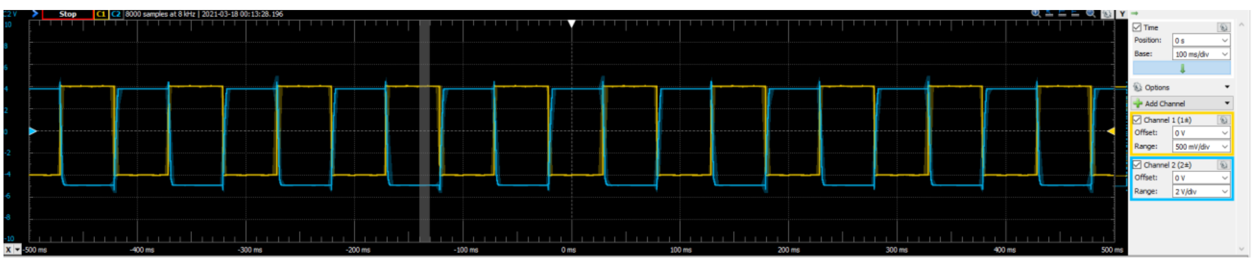
(yellow line represents Vi and the blue line is Vo)

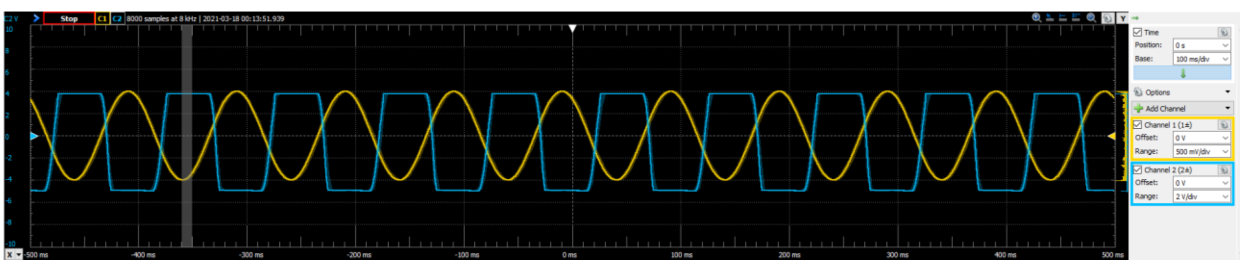




The design circuit is a reversed integrator. To act like a integrator, when the input is a square wave, the output should be a triangular wave, and has a positive slope when the input is negative, vice versa. Also, when the input is a sin wave, the output curve should be a cosine wave. With both types of inputs, the curve of Vo is the same as expected.

Part 3:





The circuit does not function like an integrator anymore when the input frequency is low. This is because when the period is larger than or close to the time constant of the capacitor, the charging model of the capacitor is not linear anymore (the charging current is becoming lower as the capacitor is almost full). In this case, the integrator is largely different from ideal.