2Ei5
Lab#2

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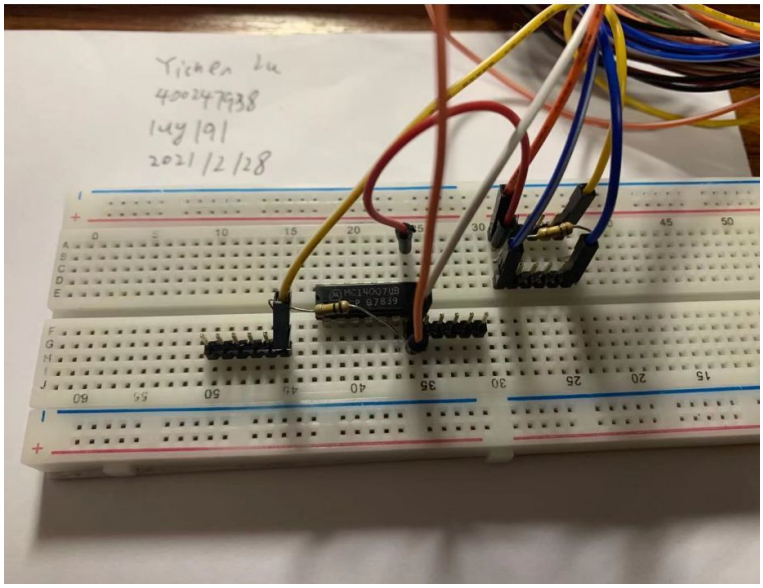
Lab section: L01
Date: Feb. 20 th 2021

As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is our own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario.

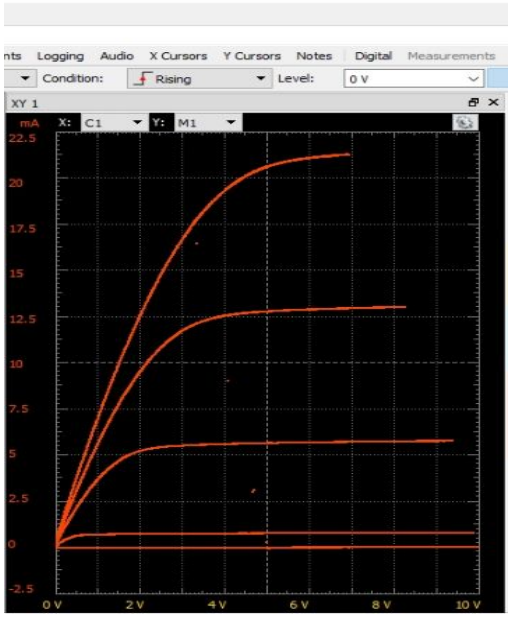
Submitted by Yichen Lu,luy191,400247938

Taks1:IV-characteristics

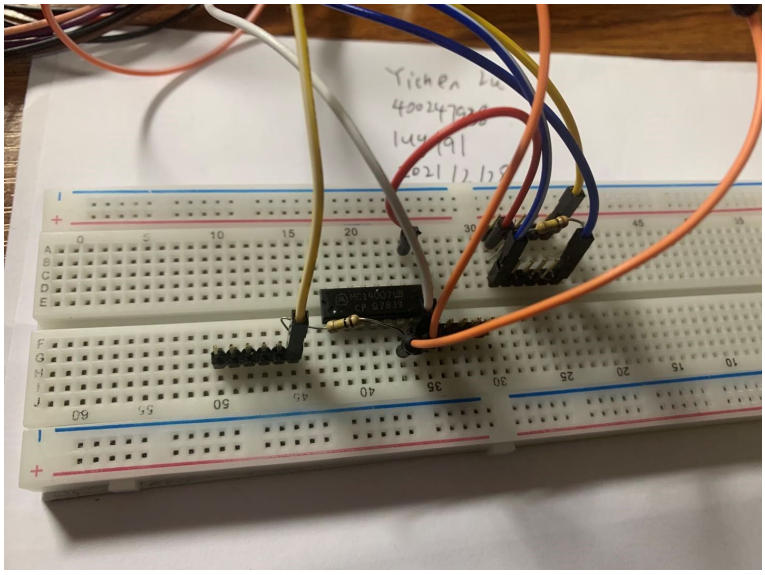
A. The picture of my physical circuit



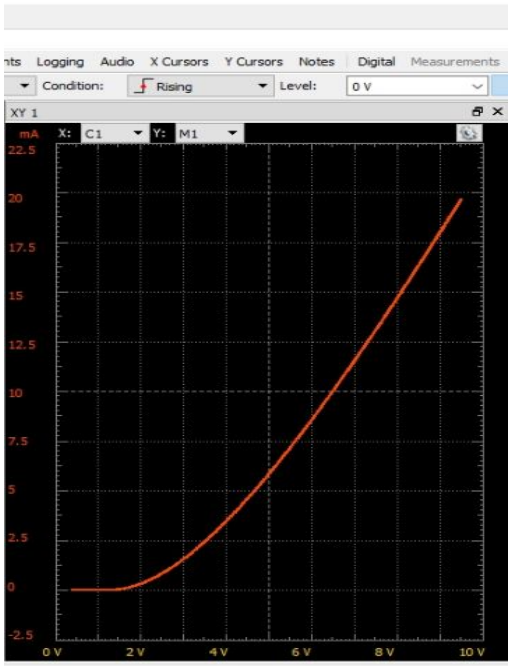
B.the iv-characteristics of an enhancement model n-channel MOSFET



C. The picture of my physical circuit



D. VGS vs ID after moving the 1+ wire to pin6



E. Data table

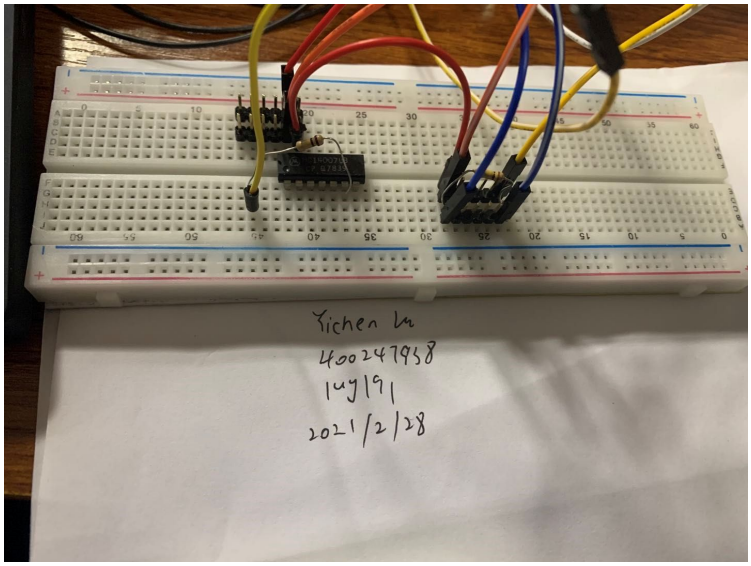
1.060895573	1.79E-05
1.071739473	1.79E-05
1.07896874	1.79E-05
1.093427273	1.79E-05
1.10065654	1.46E-05
1.107885807	1.46E-05
1.118729707	1.79E-05
1.129573607	1.46E-05
1.136802874	1.46E-05
1.147646774	1.46E-05
1.158490674	1.79E-05
1.169334574	1.46E-05
1.176563841	1.79E-05
1.187407741	1.46E-05
1.194637008	1.46E-05
1.209095541	1.46E-05
1.216324808	1.46E-05
1.227168708	1.46E-05
1.238012608	1.46E-05
1.248856508	1.46E-05
1.259700409	1.13E-05
1.270544309	1.79E-05
1.277773575	1.46E-05
1.288617476	1.46E-05
1.299461376	1.46E-05
1.310305276	1.46E-05
1.324763809	1.46E-05

F. Brief description

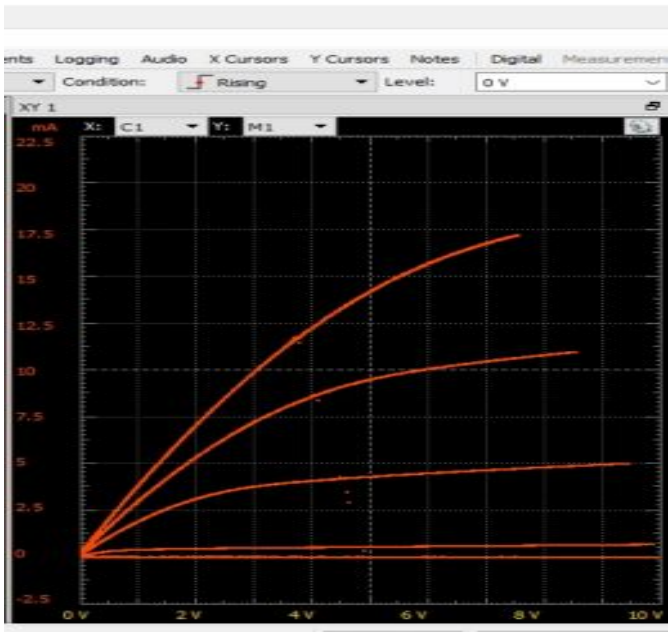
For theoretically expected behaviour, since we set up different 5 voltages, we would get 5 different curves with cutoff, linear and saturation. TTherefore, the graph is basically what I expected with the theoretical behaviour.

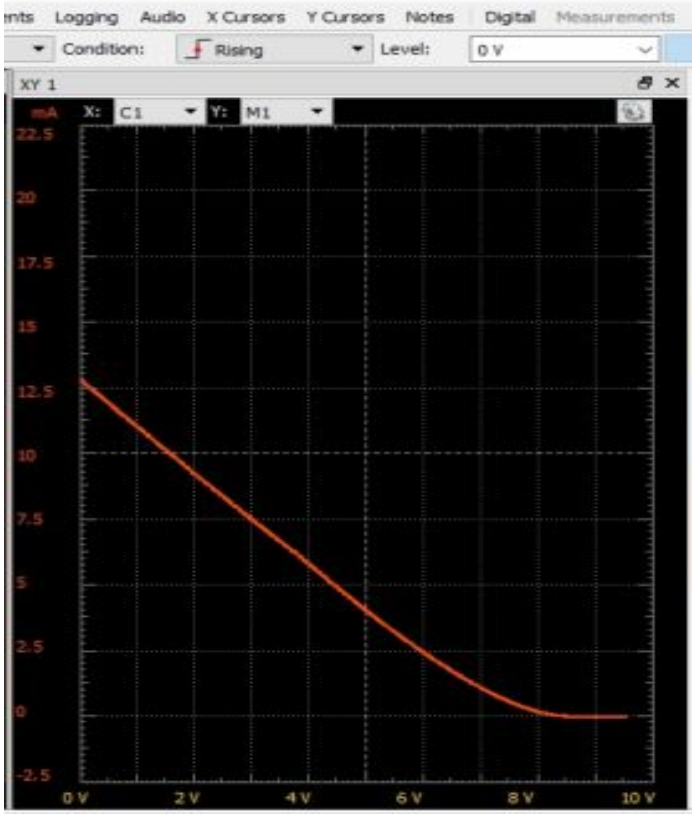
Task2:IV-characteristics of a PMOSFET

a. The picture of my physical circuit



b. The Iv-characteristics graph


Logging
Audio
X Cursors
Y Cursors
Notes
Digital
Condition:
Rising
Level:
0 V
XY 1
mA
X: C1
Y: M1
22.5
20
17.5
15
12.5
10
7.5
5
2.5
0
-2.5
0 V
2 V
4 V
6 V
8 V
10 V


Logging
Audio
X Cursors
Y Cursors
Notes
Digital
Measurements
Condition:
Rising
Level:
0 V
XY 1
mA
X: C1
Y: M1
22.5
20
17.5
15
12.5
10
7.5
5
2.5
0
-2.5
0 V
2 V
4 V
6 V
8 V
10 V

c. Data table

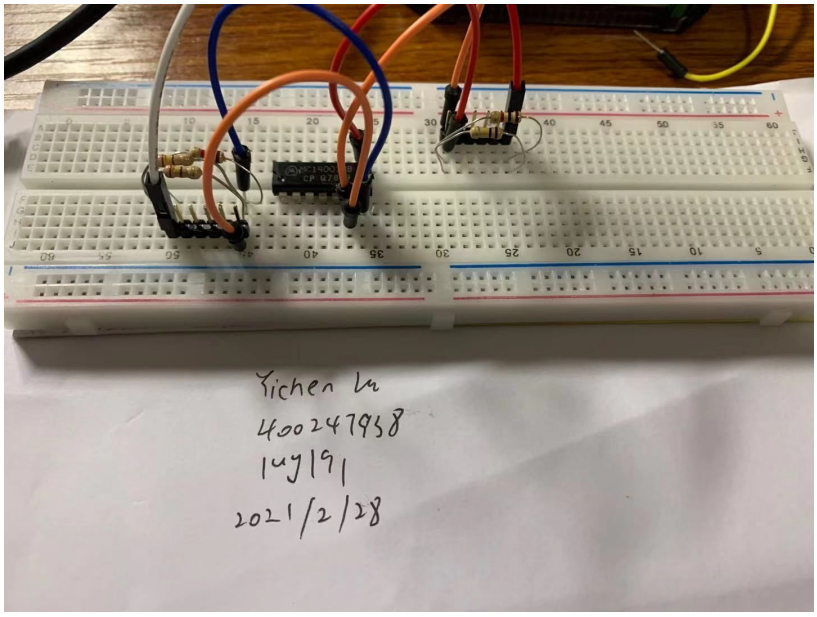
6.772016309	0.00201427343
6.753943142	0.00204382476
6.735869975	0.00207009261
6.721411442	0.00209964395
6.699723642	0.00212919528
6.681650475	0.00215546313
6.659962675	0.00218501446
6.645504141	0.00221456579
6.620201707	0.00224411712
6.605743174	0.00227366846
6.587670007	0.00230321979
6.562367573	0.00233933808
6.54790904	0.00236560593
6.529835873	0.00239187378
6.500918806	0.00242799208
6.486460272	0.00245425993
6.468387106	0.00248709474
6.446699305	0.00251992955
6.428626138	0.00255276437
6.406938338	0.00258559918
6.388865171	0.00261515051
6.370792004	0.00264798533
6.349104204	0.00267753666
6.331031037	0.00271037147
6.309343237	0.00274320628
6.287655437	0.0027760411
6.276811537	0.00280559243
6.251509103	0.00284171072
6.229821303	0.00287454554
6.208133502	0.00291066383
6.190060335	0.00294349864
6.168372535	0.00297304998
6.146684735	0.00300916827
6.128611568	0.00304528656
6.106923768	0.00307812138

d. Brief discussion

For theoretically expected behaviour, since we set up different 5 voltages, we would get 5 different curves with cutoff, linear and saturation. TTherefore, the graph is basically what I expected with the theoretical behaviour.

Task3:Voltage divider bias circuit

a. The picture of my physical circuit



(Since I did not find the 120kohm resistor, I used two 240kohm resistors in parallel each other.)

b. The measurement results

DC	3.623 V
True RMS	3.623 Ṽ

(Vd)

DC	-3.627 V
True RMS	3.627 Ṽ

(Vs)

DC	-411 mV
True RMS	411 mṼ

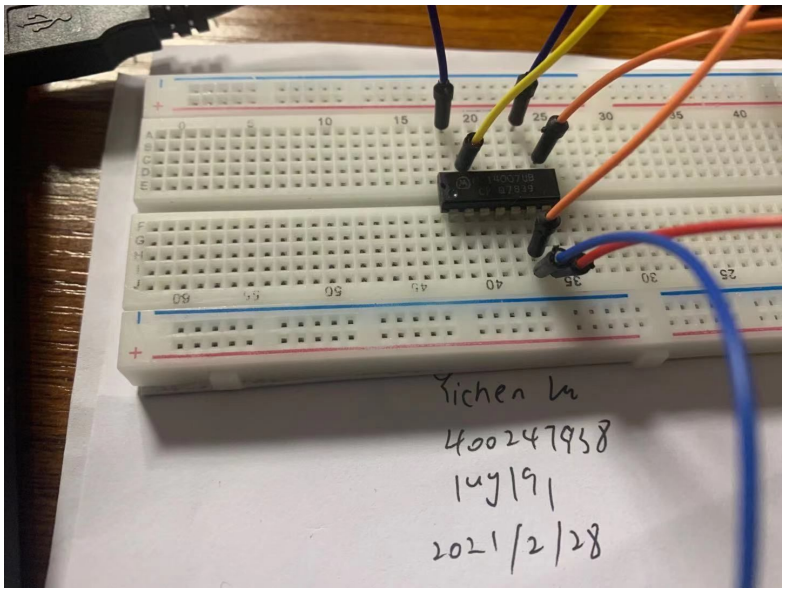
(Vg)

Vgs=5V;Id=(vgs-vs)/1k=1.391mA

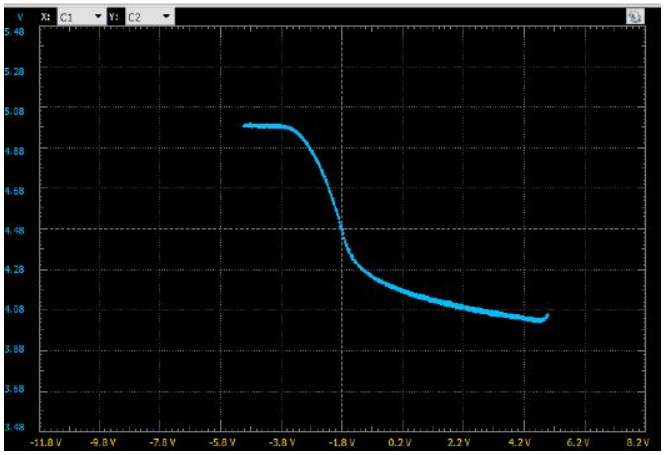
c. Brief discussion
The experimental value is basically what I expected in theoretical values. There are only small difference.

Task4: CMOS inverter

a. The picture of my physical circuit



b. The measurement results



c. Brief discussion

By comparing the experimental values and the theoretical values,the graph of the VTC diagram is almost the same as I expected. It may have some errors because of building in error of the MOSFET.