2Ei5
Project 4

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Lab section: L01
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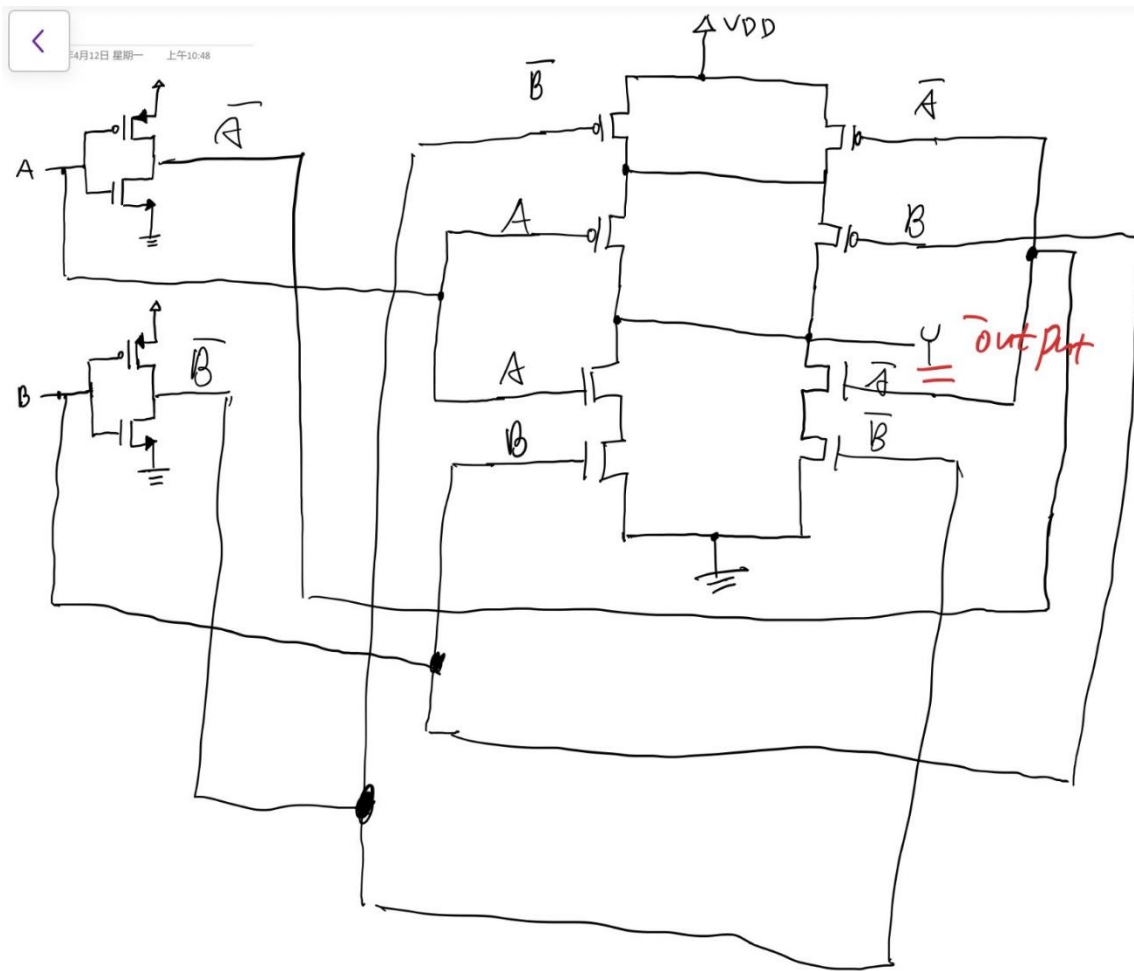
Page1:
 a. Schematic Circuit


 b. The ideal sizing for this circuit design is 2N or 2P. The ideal ratio between PMOS and NMOS sizes for the design is 1.

 c. In my opinion, I do not think that we can implement the ideal sizing in my hardware design because there would be some small errors of connecting the whole circuit. Therefore, there would be more propagation delay time for the actual design than the ideal design.
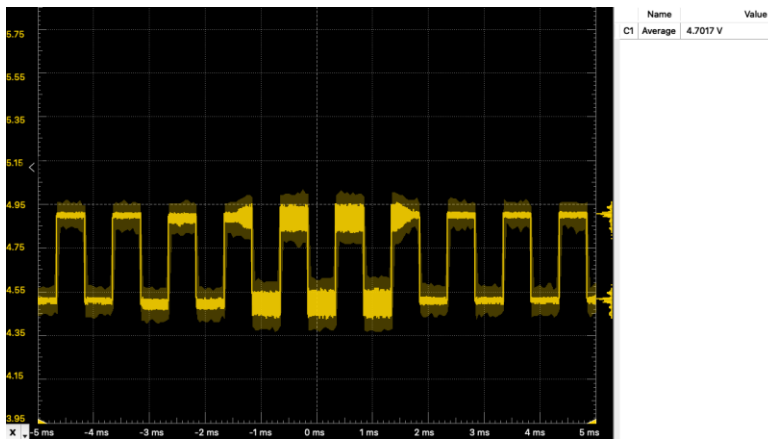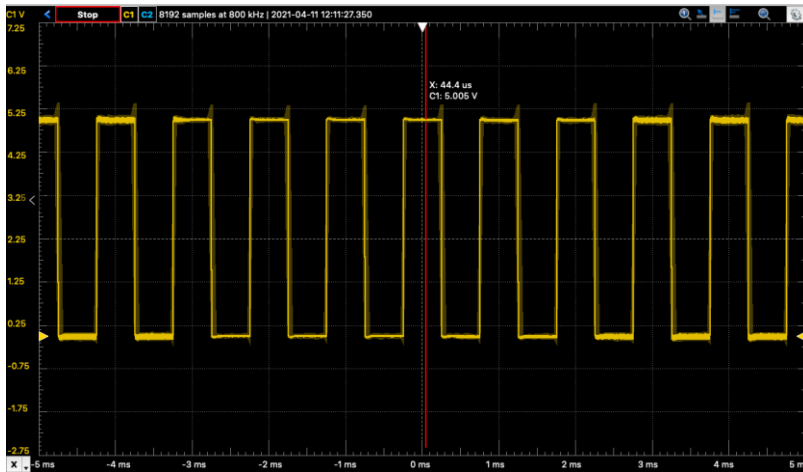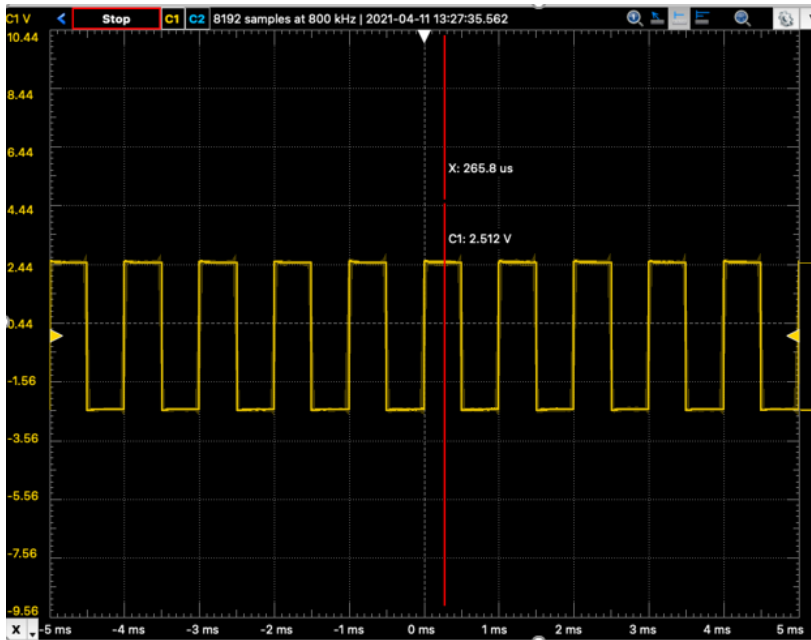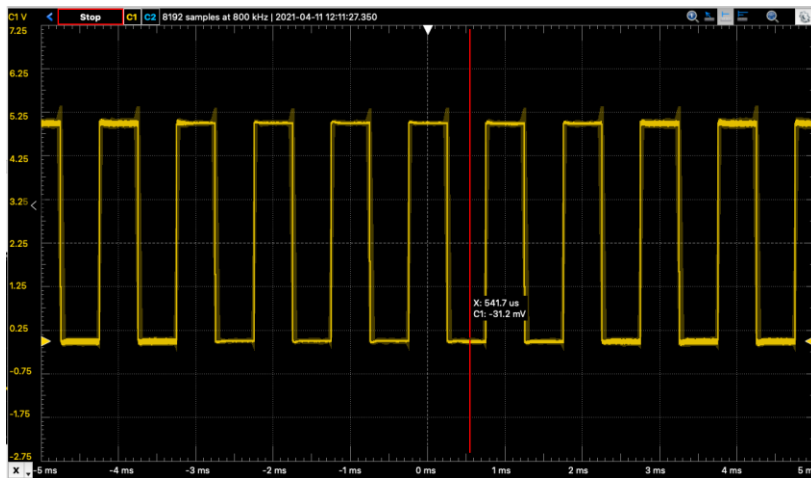
Page2:
 a.

b.

	Name	Value
C1	Average	4.7017 V

c.

Page3:

i.
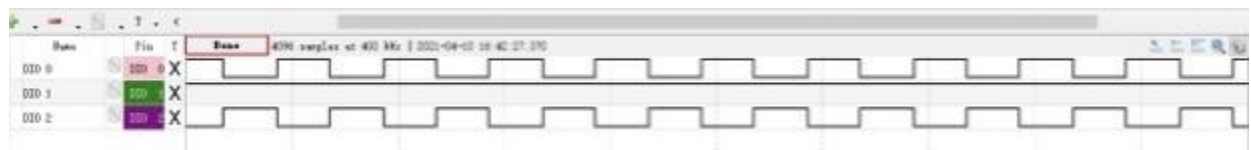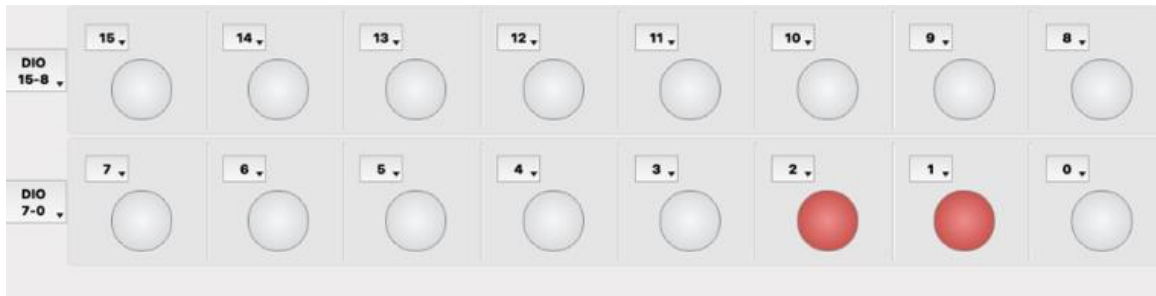
	Name	Value
C1	Average	327.26 uV
C1	RiseTime	1.8597 us
C1	FallTime	1.6033 us

ii.

$C = 100 nF$ propagation delay t_1

$$\tau_p = \left(\tfrac{1}{2}\right)(4.14\ C) = \left(\tfrac{1}{2}\right)(4.14)(100nF) = 2.07 \times 10^{-7} s$$

$$\tau_{pLH} = \left(\tfrac{1}{2}\right)(4.14\ C) = \left(\tfrac{1}{2}\right)(4.14)(100nF) = 2.07 \times 10^{-7} s$$

$$\tau_{pHL} = \left(\tfrac{1}{2}\right)(4.14\ C) = \left(\tfrac{1}{2}\right)(4.14)(100\ nF) = 2.07 \times 10^{-7} s$$