

2Ei5

Project 4

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Lab section: L01

Date: April 12nd 2021

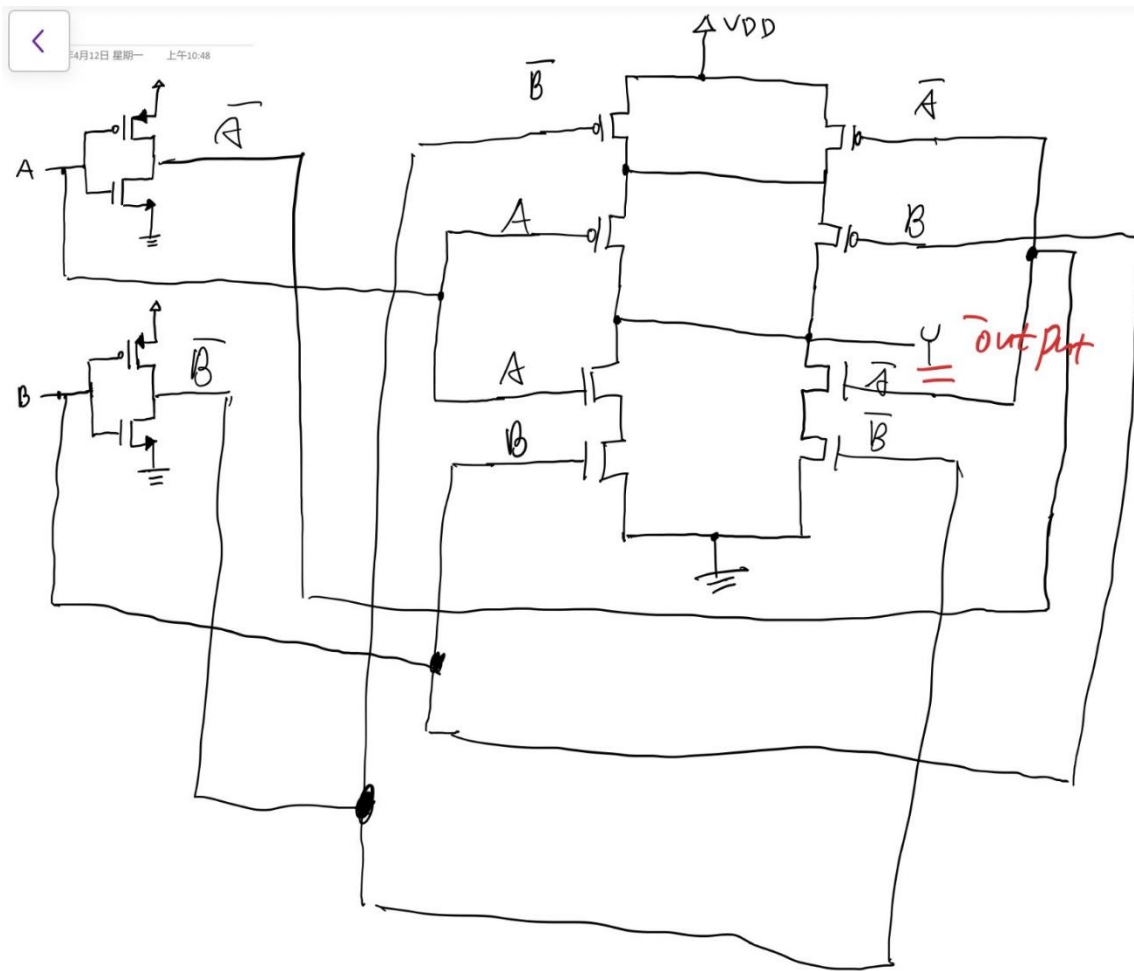
As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating.

Submitting this work with my name and student number is a statement and understanding that this work is our own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario.

Submitted by Yichen Lu, luy191, 400247938

Page1:

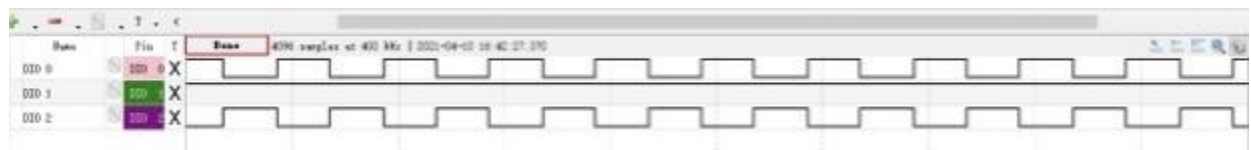
a. Schematic Circuit

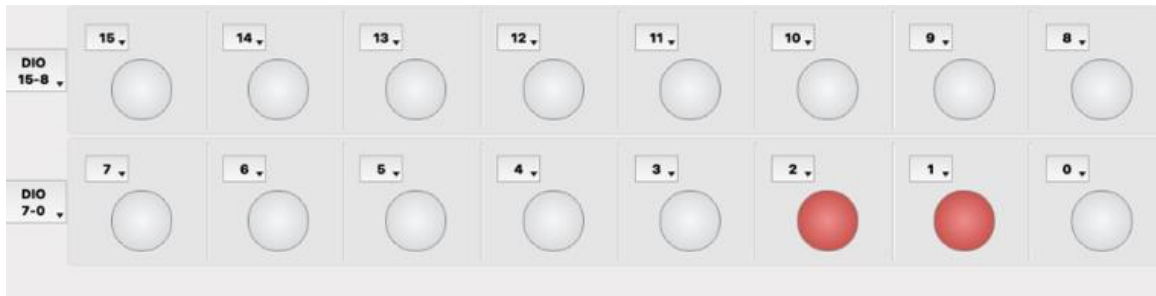


- b. The ideal sizing for this circuit design is 2N or 2P. The ideal ratio between PMOS and NMOS sizes for the design is 1.
- c. In my opinion, I do not think that we can implement the ideal sizing in my hardware design because there would be some small errors of connecting the whole circuit. Therefore, there would be more propagation delay time for the actual design than the ideal design.

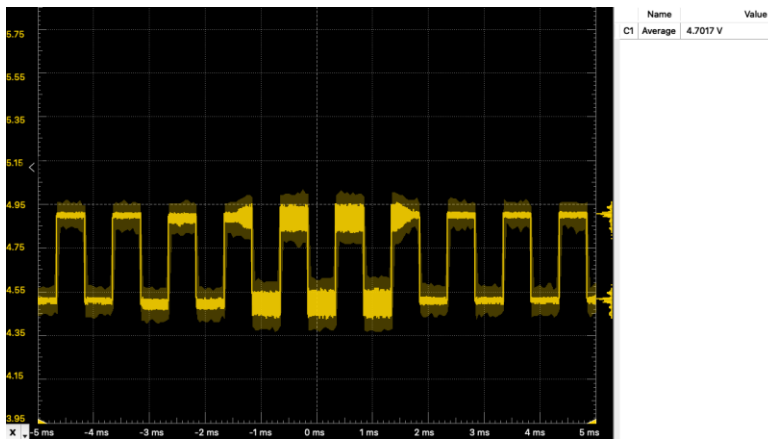
Page2:

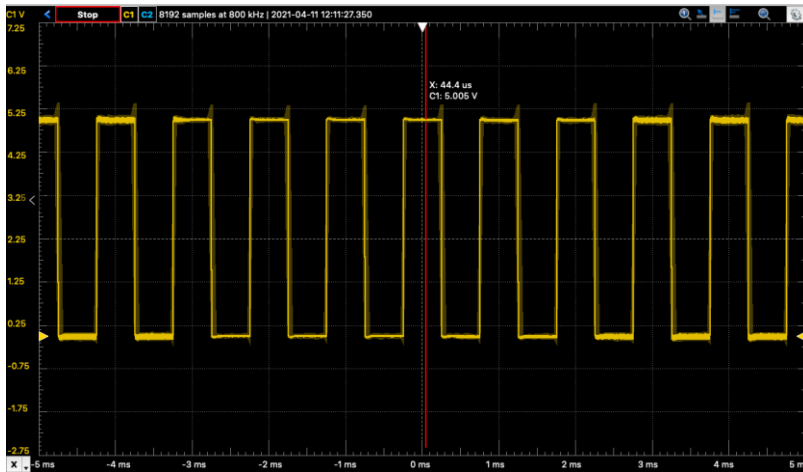
a.



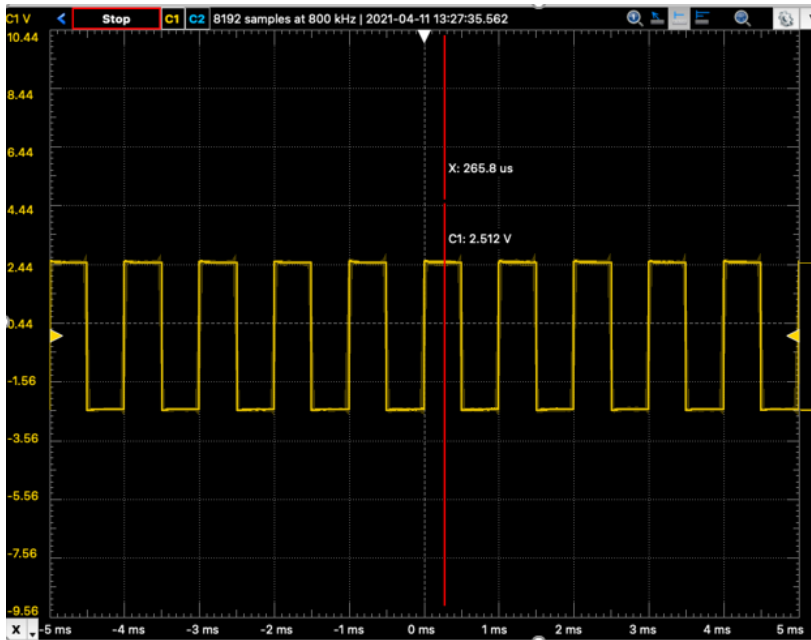
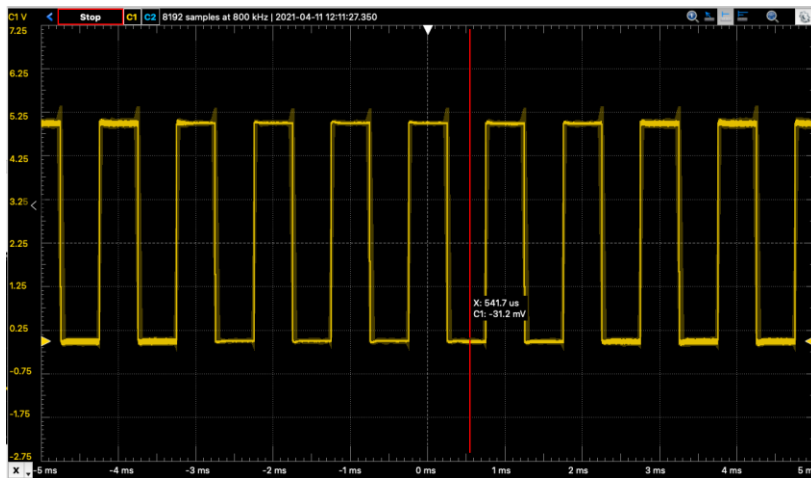


b.





C.



i.

Measurements		
	Add	Edit Show
	Name	Value
C1	Average	327.26 uV
C1	RiseTime	1.8597 us
C1	FallTime	1.6033 us

ii.

$C = 100 \text{ nF}$ propagation delay t_1

$$\tau_p = \left(\frac{1}{2}\right) (4.14 \text{ C}) = \left(\frac{1}{2}\right) (4.14) (100 \text{ nF}) = 2.07 \times 10^{-7} \text{ s}$$

$$\tau_{pLH} = \left(\frac{1}{2}\right) (4.14 \text{ C}) = \left(\frac{1}{2}\right) (4.14) (100 \text{ nF}) = 2.07 \times 10^{-7} \text{ s}$$

$$\tau_{pHL} = \left(\frac{1}{2}\right) (4.14 \text{ C}) = \left(\frac{1}{2}\right) (4.14) (100 \text{ nF}) = 2.07 \times 10^{-7} \text{ s}$$