3EJ4 LAB TWO

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Questions for Part 1:

Q1.

(1). The $V_{o,\,min}$ and I_o of the current sink determined from the simulation data are $V_{o,\,min}$ = -3 V, and I_o = 0.184807 mA in Fig (1a). The $V_{o,\,min}$ and I_o of the current sink determined from the measurement data were $V_{o,\,min}$ = -3 V, and I_o = 0.2006 mA in Fig (1b). The measured $V_{o,\,min}$ value was the same as the simulated value, and the measured I_o value was close to the simulated value.

(2). Based on the simulation data obtained in Step 1.2, the range of the simulated output resistance R_0 of the current sink for VCC larger than $V_{o,\,min}$ is [4.94E+07 Ω,7.64E+07 Ω]. In addition, based on the measurement data obtained in Step 1.2, the range of the measured output resistance R_0 of the current sink for VCC larger than $V_{o,\,min}$ is [4.03E+06 Ω,4.94E+07 Ω].

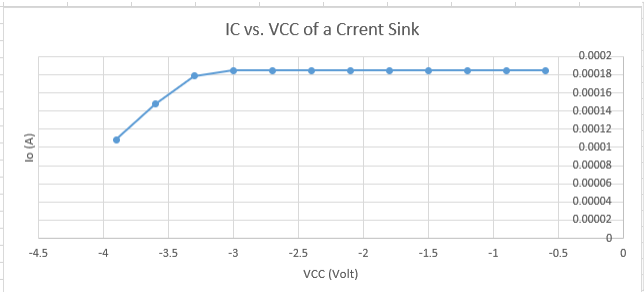
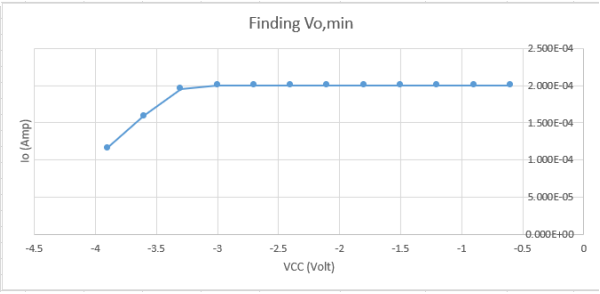


Fig (1a)



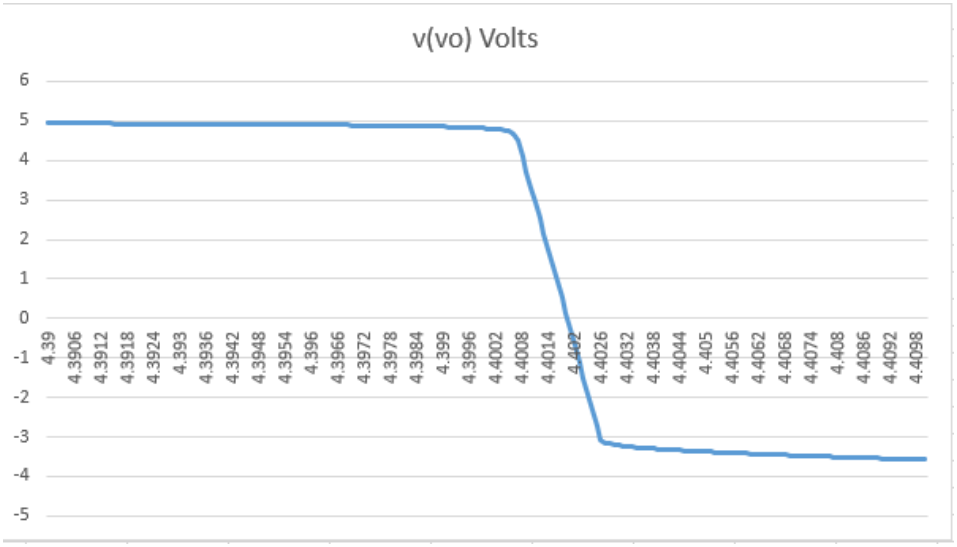
Fig(1b)

Q2.

The values of V_{o1} and V_{o2} are 4.94 V and -3.58 V respectively. Given my previous data, I found that these values are close to the maximum and minimum output voltages due to the value of Vsig at Vo1 and Vo2 being outside of the range the circuit works as an amplifier.

Q3.

(1). The simulated DC V_O vs. V_{sig} characteristics plot is shown in Fig (3a)



Fig(3a)

(2). Based on the simulation data, the DC input range of V_{sig} for this circuit work as an amplifier is between 4.4006V and 4.4027V, and the output voltage range of V_o is between 4.689626V and -3.14168V.

(3). When the V_{sig} value equals 4.4018V and V_o equals 0.124291, V_o is the most closed to 0V.

(4). The measured DC Vo vs Vsig characteristics plot is shown in Figure (3b).

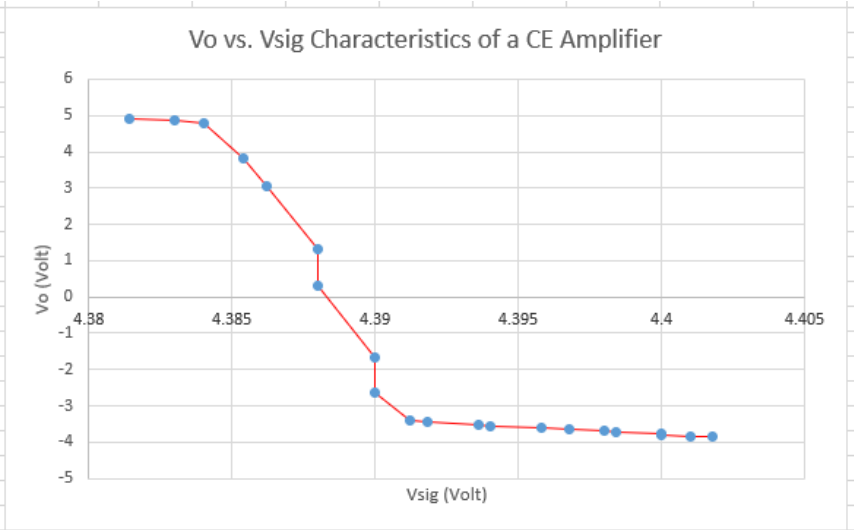


Figure (3b)

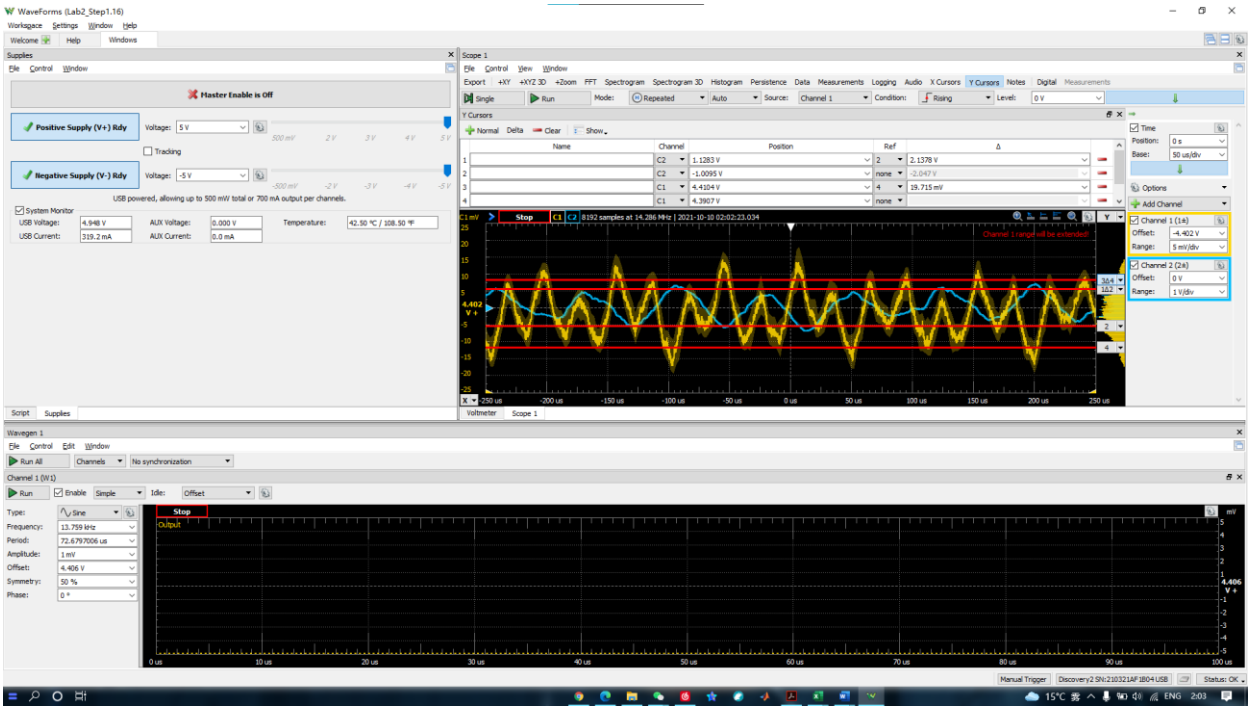
Q4.

(1) For the gain at low frequency(i.e., 100Hz), A_{vo} = **Δ**V_o / **Δ**V_{sig} = 4.04708072910916/ 0.002 which is around 2023.5, around 66.1dB. Additionally, the phase of intrinsic voltage gain at low frequency is 179.6 deg.

For the upper 3-dB frequency, it is about 14.4KHz which is around 63.0dB and the phase of intrinsic voltage gain is 134.9 degree.

(2) According to the measurement the magnitude of the gain in low frequency is about 63.3dB.

(3) The screenshot of my measurement results:

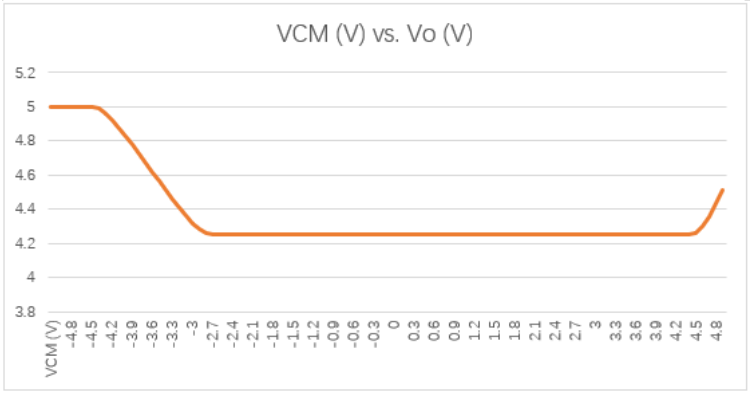


Questions for Part 2:

Q5.

(1). When V_{CM} = 0V, V_o = 4.2499904, V_E = -0.525365247734584 and I_{C2} = 9.09E-05A

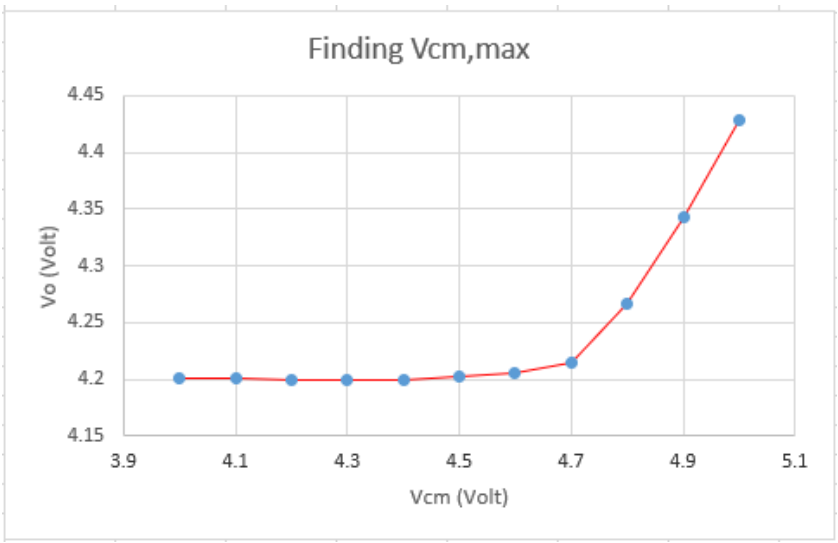
(2). Given the Fig(2b), we can get the range of the input common mode is from -2.8V to 4.4V.

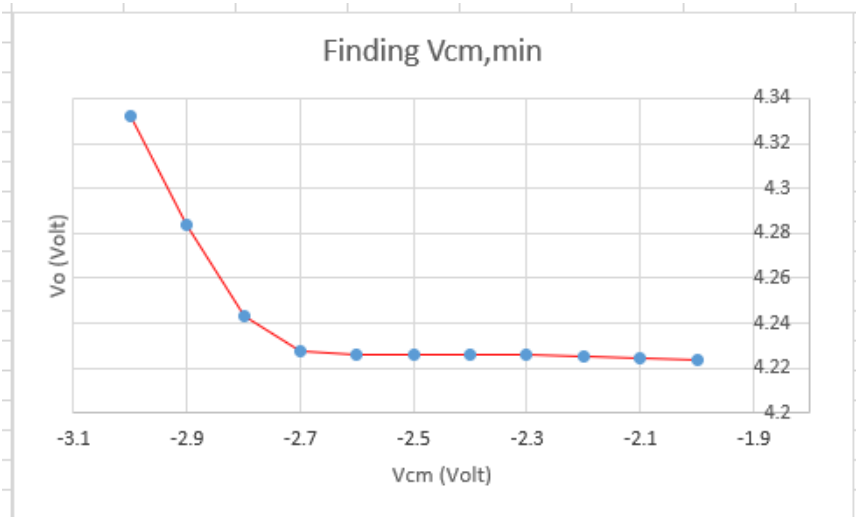


Fig(2b)

(3). Given the Fig(2b), -2.8V and 4.4V determines the upper and lower bounds. More specifically, we can notice that when V_{CM} is bigger than 4.4V, V_o will increase. In addition, when V_{CM} is smaller than -2.8V the V_o keeps decreasing. Moreover, when VCM is between -2.8V and 4.4V the V_o will remain almost the same.

(4). The measurement results are given below.





Given the graphs above, we can observe that $V_{CM,min}$ is around -2.7V and $V_{CM,max}$ is around 4.6V. Thus, the measured range is form -2.7V to 4.6V, which is extremely closed to the simulated range.

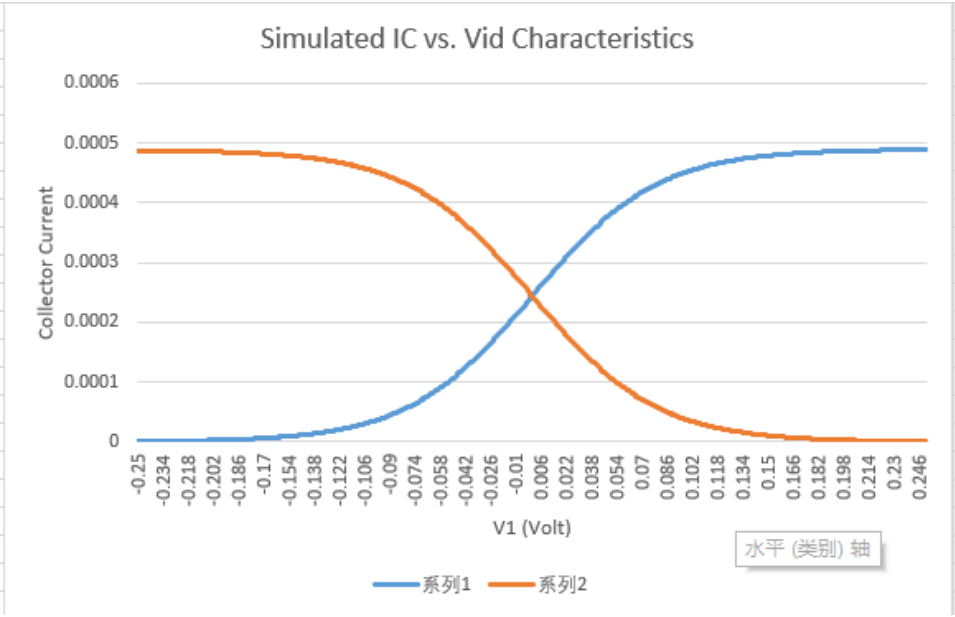
Q6.

The low-frequency voltage gain that I calculated is that A_{CM} = -86.9dB.

Questions for Part 3:

Q7.

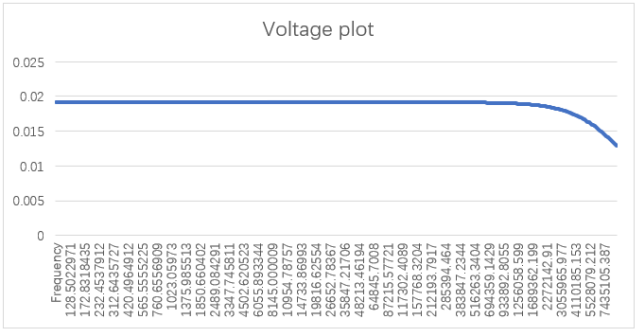
(1). Given the Fig(3a), the input differential-mode range is from -0.1023V to 0.1023V.

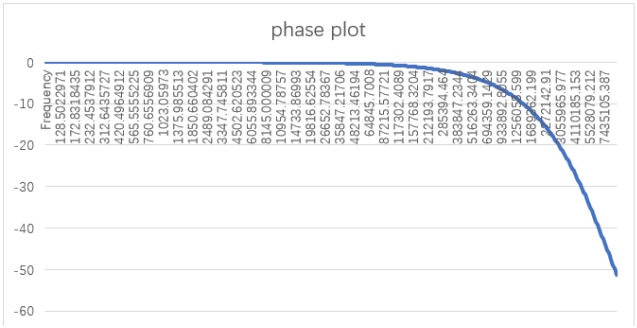


Fig(3a)

(2). Firstly, we need to observe the smallest voltage value that serious line one reaches the largest current, which is 0.203V. This value decides the upper bound. Hence, the upper bound is 0.203 / 2 = 0.1023V. In addition, we need to find the largest voltage value of serious line two that reaches the largest current, which is -0.203V. This value decides the lower bound. Hence, the lower bound is -0.205 / 2 = -0.1023V. Therefore, the range is from -0.1023V to 0.1023V.

Q8.



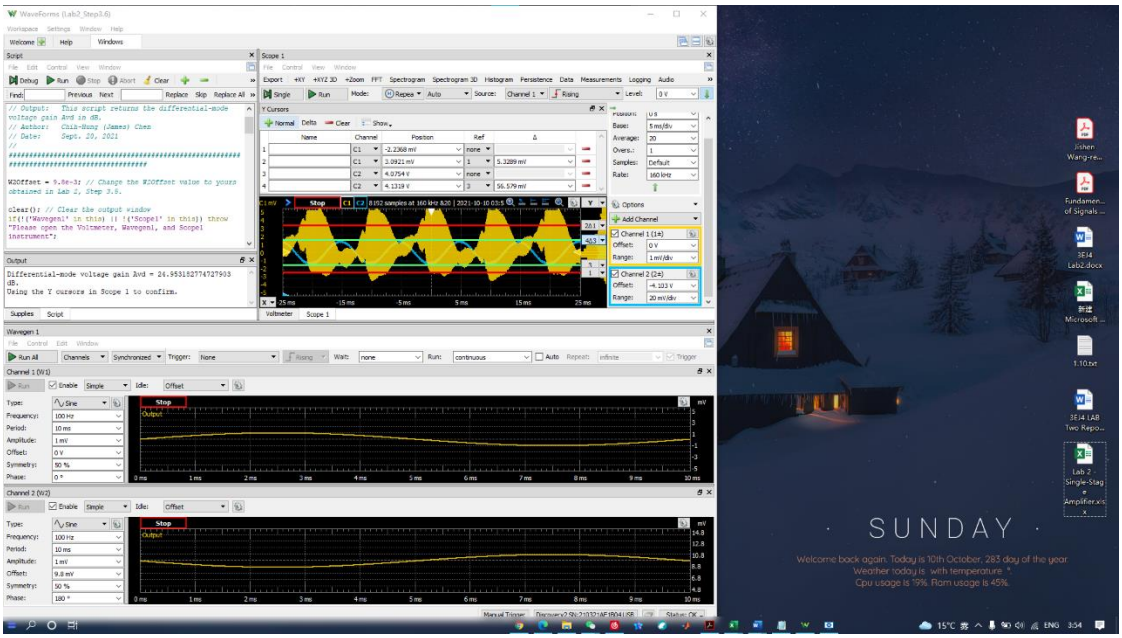


(1). The voltage gain A_d is 19.63dB when the phase is approximate 0 degree.

(2). The upper 3-dB frequency is 8145KHz with phase of -44.7degree. GBW for this is 1.39E+8 Hz

(3). The upper 3-dB frequency (8145KHz) is much higher than that in question four (14.4KHz).

(4). Based on the measurement, my gain is 14.5dB



Q9.

Based on the simulation data, the common-mode rejection ratio(CMRR) of the amplifier is that

$|A_d| / |A_{CM}| = 19.63dB – (-86.9dB) = 106.53dB$