Homework06

Chapter6

- **6.3** :

```
        .ORIG X3000
        LDI R0,CHANGE
        LDI R1,STATE      ;加载初始值

        AND R2,R2,#0
        ADD R2,R2,#1      ;初始化R2

  LOOP    BRZ FINAL
        ADD R2,R2,R2
        ADD R0,R0,#-1
        BRNZP    LOOP     ;设计R2

  FINAL   ADD R1,R1,R2
        STI R1,STATE      ;存储STATE
        TRAP x25

  CHANGE  .FILL x4000
  STATE   .FILL x4001
        .END
```

Chapter7

- **7.4** :

Symbol	Address
SAVE3	x3029
SAVE2	x302A
TEST	x301F
FINISH	x3027

- **7.18** :

a. `LDR R3,R1,#0`

b. `NOT R4,R4`

c. `ADD R4,R4,#1`

- **7.20** : The difference is the time of data to be stored into x4000. In (a), the data will be stored when the module is run; in (b), the data will be stored when the first past assemble process(the `.FILL X4000` is executed).