Yifan Qin

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EDUCATION

University of Notre Dame 2022 - present
Ph.D. Candidate, Computer science and engineering
Research interest: computing-in-memory, AI accelerator with post-CMOS designs
Working with Prof. Yiyu Shi & Prof. X. Sharon Hu

Huazhong University of Science and Technology 2018 - 2021
MS, Software engineering
Research interest: quantized low-bit neural networks with RRAM

Huazhong University of Science and Technology 2013 - 2017
BS, Electronic science and technology

AWARDS AND HONORS

Young Fellow (DAC) 2023 - 2024
William J. McCalla Best Paper Award at IEEE/ACM ICCAD (2 out of 750 submissions) 2023
Young Fellow (DAC) 2022 - 2023
Outstanding Graduates (HUST) 2020 - 2021
Outstanding Volunteer Docent (Wuhan Museum) 2015 - 2016
National 2nd Prize (Contemporary Undergraduate Mathematical Contest in Modeling) 2015

RESEARCH EXPERIENCE

University of Notre Dame Notre Dame, IN
Doctoral Researcher August 2022 - present
Established and implemented several methods to mitigate the impact of device variations on inference of NVCIM accelerators. Achieved high robust and efficient algorithms for NVCIM training and deployment.

AI Chip Center for Emerging Smart Systems(ACCESS) Hong Kong
Visiting student May 2024 - July 2024
Developed and implemented a fully quantized 1D convolutional system for ventricular arrhythmia detection on a CNN accelerator (40nm, TSMC). Led the full-stack design, from UI to backend, achieving low inference latency and high energy efficiency.

Huazhong University of Science and Technology Wuhan, Hubei
Master's Researcher, Research Assistant August 2018 - June 2022
Designed low-bit quantized CNNs for RRAM accelerators, addressing non-idealities of RRAM crossbars during inference. Developed a novel binary neural network RRAM accelerator with half area and maintained high accuracy.

PUBLICATION

Journal

[1] Han Bao, Yifan Qin, Jia Chen, Ling Yang, Jiancong Li, Houji Zhou, Yi Li, and Xiangshui Miao. "Quantization and sparsity-aware processing for energy-efficient NVM-based convolutional neural networks". In: *Frontiers in Electronics* 3 (2022), p. 954661.

[2] Yifan Qin, Han Bao, Feng Wang, Jia Chen, Yi Li, and Xiangshui Miao. "Recent progress on memristive convolutional neural networks for edge intelligence". In: *Advanced Intelligent Systems* 2.11 (2020), p. 2000114. (**Back Cover**).

[3] Yifan Qin, Rui Kuang, Xiaodi Huang, Yi Li, Jia Chen, and Xiangshui Miao. "Design of high robustness BNN inference accelerator based on binary memristors". In: *IEEE Transactions on Electron Devices* 67.8 (2020), pp. 3435–3441.

Conference

[1] Yifan Qin, Zhenge Jia, Zheyu Yan, Jay Mok, Manto Yung, Yu Liu, Xuejiao Liu, Wujie Wen, Luhong Liang, Kwang-Ting Tim Cheng, X. Sharon Hu, and Yiyu Shi. "A 10.60 µW 150 GOPS Mixed-Bit-Width Sparse CNN Accelerator for Life-Threatening Ventricular Arrhythmia Detection". In: *Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC)*. ACM. 2025.

[2] Likai Pei*, Yifan Qin*, Zephan M. Enciso, Boyang Cheng, Jianbo Liu, Steven Davis, Zhenge Jia, Michael Niemier, Yiyu Shi, X. Sharon Hu, and Ningyuan Cao. "Towards Uncertainty-Quantifiable Biomedical Intelligence: Mixed-signal Compute-in-Entropy for Bayesian Neural Networks". In: *2024 IEEE/ACM International Conference on Computer Aided Design (ICCAD)*. IEEE. 2024. (* contributed equally).

[3] Yifan Qin, Zheyu Yan, Zixuan Pan, Wujie Wen, Xiaobo Sharon Hu, and Yiyu Shi. "TSB: Tiny Shared Block for Efficient DNN Deployment on NVCIM Accelerators". In: *2024 IEEE/ACM International Conference on Computer Aided Design (ICCAD)*. IEEE. 2024.

[4] Yifan Qin, Zheyu Yan, Wujie Wen, Xiaobo Sharon Hu, and Yiyu Shi. "Sustainable Deployment of Deep Neural Networks on Non-Volatile Compute-in-Memory Accelerators". In: *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*. IEEE. 2024.

[5] Yifan Qin, Zheyu Yan, Wujie Wen, Xiaobo Sharon Hu, and Yiyu Shi. "Negative Feedback Training: A Novel Concept to Improve Robustness of NVCiM DNN Accelerators". In: *arXiv preprint arXiv:2305.14561*. 2023. (under review).

[6] Zheyu Yan, Yifan Qin, Xiaobo Sharon Hu, and Yiyu Shi. "On the viability of using LLMs for SW/HW co-design: An example in designing CiM DNN accelerators". In: *2023 IEEE 36th International System-on-Chip Conference (SOCC)*. IEEE. 2023, pp. 1–6.

[7] Zheyu Yan, Yifan Qin, Wujie Wen, Xiaobo Sharon Hu, and Yiyu Shi. "Improving realistic worst-case performance of NVCiM DNN accelerators through training with right-censored gaussian noise". In: *2023 IEEE/ACM International Conference on Computer Aided Design (ICCAD)*. IEEE. 2023, pp. 1–9. (**Best Paper,2 out of 750 submissions**).

PRESENTATIONS & TALKS

Computer science department, Shandong University (SDU) **Aug, 2024**
Electrical engineering department, Zhejiang University (ZJU) **Aug, 2024**
University of Michigan-Shanghai Jiao Tong University Joint Institute, Shanghai Jiao Tong University (SJTU) **Aug, 2024**
Electrical engineering department, Southern University of Science and Technology (SUSTech) **July, 2024**
AI Chip Center for Emerging Smart Systems (ACCESS), HK, PostGraduateStudent Sharing Session **June, 2024**

TEACHING EXPERIENCE

CSE-40868 Neural Networks, TA SP23

REVIWER FOR JOURNALS/CONFERENCE

ACM/IEEE International Conference on Computer-Aided Design (ICCAD) 2024

LEADERSHIP AND SERVICE

Member, Huazhong University of Science and Technology, Graduate school, Graduate Student Association, 2019-2020
Volunteer Docent, Wuhan Museum, 2015-2016
Team Captain, Huazhong University of Science and Technology, College Table Tennis Team, 2015-2016
President, Huazhong University of Science and Technology, Table Tennis Association, 2015-2016