

Yifan Yuan

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Educational Backgrounds

- MS/PhD, Department of Electrical and Computer Engineering, UIUC *August 2017 – Present*
 - Major: Computer Architecture and System
 - Advisor: Prof. Nam Sung Kim
- Bachelor, Institute of VLSI Design, Zhejiang University *September 2014 – June 2018*
 - Major: Electronic Information Engineering

Research Interest

- Networking hardware and system software
- FPGA and accelerator design for distributed systems

Publications

- **Y. Yuan**, M. Alian, Y. Wang, R. Wang, I. Kurakin, C. Tai, N. S. Kim. Don't Forget the I/O When Allocating Your LLC, *ISCA'21 full paper, NSDI'20 poster*
- **Y. Yuan**, Y. Wang, R. Wang, R. Chowdhury, C. Tai, N. S. Kim. QEI: Query Acceleration Can be Generic and Efficient in the Cloud, *HPCA'21*
- M. Alian, **Y. Yuan**, J. Zhang, R. Wang, M. Jung, N. S. Kim. Data Direct I/O Characterization for Future I/O System Exploration, *ISPASS'20*
- **Y. Yuan**, Y. Wang, R. Wang, J. Huang. HALO: Accelerating Flow Classification for Scalable Packet Processing in NFV, *ISCA'19*
- Y. Li*, **Y. Yuan***, I. Liu, D. Chen, A. Schwing, J. Huang. Accelerating Distributed Reinforcement Learning with In-Switch Computing, *NSDI'19 poster, ISCA'19 full paper* (*: Equal contribution)
- X. Wang, **Y. Yuan**, Y. Zhou, C. C. Coats, J. Huang. Project Almanac: A Time-Traveling Solid-State Drive, *EuroSys'19*
- Y. Li, J. Park, M. Alian, **Y. Yuan**, Q. Zheng, P. Pan, R. Wang, A. Schwing, H. Esmailzadeh, N. S. Kim. A Network-Centric Hardware/Algorithm Co-Design to Accelerate Distributed Training of Deep Neural Networks, *MICRO'18*

Patents

- R. Wang, T.-Y. C. Tai, Y. Wang, **Y. Yuan**, S. Paul, M. M. Khellah, S. Gobriel, C. Augustine, M. Ganguli, J.-S. Tsai, E. Verplanke, P. Autee, A. Layek, S. Narayana, B. Ganesh, J. B. Timbadiya, S. K. Muthukumar, R. Iyer, N. Jain, N. D. McDonnell, M. A. Goldschmidt, R. M. Sankaran, N. Ranganathan. Hardware Assisted Lookup Operations, *US Patent App. 63/130,663, filed Dec. 2020*
- R. Wang, **Y. Yuan**, Y. Wang, T.-Y. C. Tai, T. Hurson. Data Consistency and Durability over Distributed Persistent Memory Systems, *US Patent App. 62/986,094, filed Aug. 2020*
- Y. Wang, R. Wang, T.-Y. C. Tai, **Y. Yuan**, P. Pathak, S. Vedantham, C. Macnamara. Workload Scheduler for Memory Allocation, *US Patent App. 16/799,745, filed Feb. 2020*
- R. Wang, A. J. Herdrich, T.-Y. C. Tai, Y. Wang, R. Kondapalli, A. Bachmutsky, **Y. Yuan**. Offload of Data Lookup Operations, *US Patent App. 16/207,065, filed Nov. 2018*

Work Experiences

- Microsoft Research *June 2020 – August 2020*
 - Research Intern at Systems Research Group, Redmond, WA
 - Explored new functionality of commodity programmable switch.
- Intel Labs *May 2019 – August 2019*
May 2018 – August 2018
 - Research Intern at Networking Performance Lab, Hillsboro, OR
 - Conducted research on next generation high-performance network platform and I/O system.

Teaching Experience

- *ECE 411*: Computer Organization and Design (SP 2021)

Skills and Techniques

- *Programming languages*: C/C++, Verilog HDL, VHDL, Python, P4, Shell script, LaTeX, Matlab, etc.
- *Development skills*: Unix/Linux, FPGA, CUDA, DPDK, RDMA, programmable switch, gem5 simulator, sniper simulator, etc.

Selected Courses

- Computer Architecture; High-speed and Programmable Networks; Advanced Memory and Storage System; Distributed System; Advanced Computer Networks; Applied Parallel Programming; Computer Security; System-on-Chip Design; Introduction to VLSI Design; Digital System Design; Embedded System; Artificial Intelligence

Awards and Honors

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| • NSDI'20 Student Travel Grant | 2020 |
| • OSDI'18 Student Travel Grant | 2018 |
| • Scholarship for Academic Excellence | 2016 |
| • Third Prize in University Robot Contest | 2016 |
| • Scholarship for Academic Excellence | 2015 |