	STM32L1	STM32L4
	Up to 24 lines	Up to 40 lines (14 direct, 26 configurable)
EXTI	typedef struct{	typedef struct{
	IO uint32_t IMR;	IO uint32_t IMR1;
	IO uint32_t EMR;	IO uint32_t EMR 1 ;
	IO uint32_t RTSR;	IO uint32_t RTSR1;
	IO uint32_t FTSR;	IO uint32_t FTSR1;
	IO uint32_t SWIER;	IO uint32_t SWIER 1 ;
	IO uint32_t PR;	IO uint32_t PR 1 ;
	} EXTI_TypeDef;	uint32_t RESERVED1;
		uint32_t RESERVED2;
		IO uint32_t IMR 2 ;
		IO uint32_t EMR <mark>2</mark> ;
		IO uint32_t RTSR2;
		IO uint32_t FTSR2;
		IO uint32_t SWIER <mark>2</mark> ;
		IO uint32_t PR2;
		} EXTI_TypeDef;
	The selection of EXTI line source is performed	The mapping of the EXTICRx registers has been
	through EXTIx bits in SYSCFG_EXTICRx	changed.
	registers (in STM32L1 and STM32L4 series).	SVSSS SVTISS
	SVSSS SVEIGNA	SYSCFG_EXTICR1
	SYSCFG_EXTICR1	SYSCFG_EXTICR2
	SYSCFG_EXTICR2	SYSCFG_EXTICR3
	SYSCFG_EXTICR4	SYSCFG_EXTICR4
	SYSCFG_EXTICR4	EXTIx[2:0]:
	EXTIx[3:0]:	000: PA[x] pin
	0000: PA[x] pin	001: PB[x] pin
	0001: PB[x] pin	010: PC[x] pin
	0010: PC[x] pin	011: PD[x] pin
	0011: PD[x] pin	100: PE[x] pin
	0100: PE[x] pin	101: PF[x] pin
	0101: PH[x] (only PH[2:0])	110: PG[x] pin
	PH[3] is not used.	111: Reserved